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Summary

The design and construction of fast logic modules for nuclear instrumentation has always been a costly and time consuming effort. The demands for and on modules have increased considerably; greater quantities with improved performance capabilities are needed. Improved performance and reduced module cost are obtained by using commercially available emitter-coupled logic and a minimal amount of interface circuitry to form compatible functional circuits which can then be combined to create the various modules necessary for nuclear instrumentation. This paper describes the operation of several functional circuits that have been designed at the Lawrence Berkeley Laboratory to effectively utilize the Motorola MECL III [1,2] line of integrated logic circuits in NIM Standard[3] fast logic modules. The modules process pulses with rise and fall times of approximately 1 ns and can operate at pulse repetition rates in excess of 300 MHz, yet their cost is less than half that of commercially available 200 MHz units.

Introduction

Fast logic modules are used in nuclear instrumentation to perform logical operations, such as ANDing, ORing, coincidence recognition, or counting, on standardized pulses produced by discriminators or other logic modules. The primary goal in the design of these logic modules is to achieve fast operation: for example, the ability to resolve two pulses spaced very close together in time, or the ability to resolve a small time overlap (coincidence) of two or more pulses. The logic modules must be capable of accepting, processing, and outputting pulses of 1-ns rise and fall times at repetition rates to 300 MHz. Inside a module, several quite different functions usually must be performed: ANDing, ORing, latching, pulse width standardization, and fan-out. Integrated logic gates and flip-flops can be used directly for logic and latching functions; with additional discrete circuitry, they can also perform the more special purpose functions.

Motorola MECL III Circuits

The motorola MECL III line of integrated emitter-coupled logic gates and flip-flops was selected because of the exceptional rise, fall, and propagation-delay times (all less than 1 ns) and the fast flip-flop toggling rates (greater than 300 MHz). The circuit schematic for a single gate is shown in Fig. 1. The gates used are in two configurations: The MC 1660S (Dual four-input, OR-NOR gate) and the MC 1662S (Quad two-input, NOR gate). These gates are also available in a low input-impedance version that is not suitable for our purposes. Motorola recommends that the V_{CC} supply be grounded and the V_{EE} supply be -5.2 V. In this application, V_{CC} is grounded and V_{EE} is connected to the NIM Standard -6 V supply. This change in the V_{EE} supply voltage increases the gate power dissipation by approximately 15%, but since each module requires only a few gates, the additional power dissipation is more than offset by the advantage of using a standard, well-regulated supply. With V_{EE} at -6 V, the MECL III logic up-level is -0.8 V, the logic down-level is -2.0 V, the input threshold is -1.45 V, and the noise margin of the gate is about 250 mV. The logic up-level varies with temperature as the V_{BE} drop of the output transistor Q7 or Q8 in Fig. 1 (about 2.3 mV/° C), while the threshold voltage varies approximately as the V_{BE} drop of transistor Q6. Hence, the noise margin of a group of gates does not deteriorate as long as all gates are at the same temperature.

The flip-flop shown in Fig. 2 (MC 1670S) has the same logic-level characteristics as the gates. It operates on the master-slave principle; when both clock inputs, C1 and C2, are at a down-level, the master portion of the flip-flop follows the D input (set if D is up, or reset if D is down). When a clock input, C1 or C2, exceeds the threshold in rising to an up-level, the contents of the master are transferred to the slave and the outputs, and the master is disconnected from the D input. Simple binary toggling is achieved by inputting to one of the clocks and connecting the $\overline{Q}$ output to the D input, as shown.

All signals inside a unit will be MECL III levels; therefore, a level-shifting circuit is necessary at each input to convert NIM Standard logic levels (up-level is 0 V, down-level is -800 mV) to MECL III levels, and a level shifting circuit is necessary at each output to convert the MECL III levels back to NIM levels. It should be noted that MECL III levels could be shifted to NIM levels simply by using two supplies; V_{CC} = 0.8 V and V_{EE} = -4.4 V. The logic levels of the MECL III gates would then be 0 V and -1.0 V, which are compatible with the NIM Standard. This approach has been used successfully with the slower MECL II [4,5] line of gates; however, it has serious drawbacks in our application: First, it requires two supply regulators in each module. Second, it prevents the use of the ground plane for V_{CC}, which is virtually essential to accommodate the fast switching of up to 30 mA by the output transistors and to prevent other output transistors on the same V_{CC} from receiving and outputting transient spikes. These two considerations make the

use of a separate V_{CC} power supply impractical for MECL III applications.

The cost involved in having to restore MECL III levels to NIM levels in the single supply is minimal because the circuits so used are necessary for other reasons. The high-impedance current source outputs are preferred since the NIM Standard specifies a current output allowing the use of clipping lines and eliminating potential damage due to shorting. Similarly, input level shifting also is used for input protection.

Input Level Shifter

The NIM Standard levels (-200 mV maximum up, -600 mV minimum down) are centered about the MECL III threshold of -1.45 V by the simple emitter-follower circuit shown in Fig. 3. CR 1 is a germanium diode, while CR2 and Q1 are both silicon devices. The total dc drop from the input to the emitter of Q1 is then approximately 1 V, as required. Since the temperature variation of the diode-drops of CR1 and CR2 tend to cancel, the total voltage drop varies with temperature approximately as the V_{BE} drop of Q1; this variation tends to track the MECL III threshold variation, and reasonable noise margins are maintained.

The two diodes CR1 and CR2 provide the additional advantage of protection against input overloads; CR1 will reverse bias for positive overloads, and CR2 will reverse bias for negative overloads. The circuit is undamaged for ±100 V pulses of short (20 ns) duration. The dc overload protection is determined solely by the power dissipation in the termination resistor R1.

Since the circuit is an emitter follower, the propagation time is small (typically 650 ps) and the overall circuit provides a reasonable 50-Ω in-out termination (reflections of 10% for 1 ns rise time inputs and 25% for 100 ps rise time inputs).

It is undesirable to connect fast pulse signals to switches because the pulse deterioration is usually unacceptable. A variation on the basic input circuit, which allows for the front panel in/out switching of inputs, is shown in Fig. 4. The additional PNP transistor Q2 is used to switch the input, depending on the front-panel switch setting. If R5 is returned to +6 V, then the base is at 0 V, Q2 cannot conduct, and the output is at -6 V. With the front panel switch in the "in" position, R6 provides sufficient base current to saturate Q2, and the emitter of Q1 is connected through a low impedance to the output. The input diode CR1 is changed from a germanium diode to a silicon diode to offset the additional $V_{CE(SAT)}$ of Q2 and maintain a 1 V drop from input to output. The saturated switch adds approximately 100 ps delay to the propagation time of the basic input circuit shown in Fig. 3.

The saturated switch can also be used to switch signals between MECL III gates, as shown in Fig. 5. This scheme eliminates the necessity and propagation delay of an additional gate; however, it does shift the logic levels by the saturation voltage of Q1 and hence should be used only between gates in the same package to reduce the difficulties inherent in reduced noise margins. As in the case of the input circuit, the saturated switch has a propagation delay of approximately 100 ps.

Output Level Shifter

The MECL III logic levels are converted back to NIM Standard levels by the circuit shown in Fig. 6. The differential pair of transistors, Q1 and Q2, are driven by the complementary outputs of an MECL III gate. The pair is biased at 34 mA, providing the NIM Standard 17 mA into each of two 50-Ω loads. The transistors that are used (MMT 3960A) are designed especially for current-switch-pairs and have an f_T of approximately 2.2 GHz. The base resistors R3 and R4, and the series combination of R6 and C1 are included to reduce the ringing and overshoot of the output waveforms. Diodes CR1 and CR2 protect transistor Q2 and the output of the MECL III gate if both outputs are unterminated. The combination of large base drive (approximately 2.4 V differential), low output impedance, and fast transistors results in output rise times of less than 900 ps and fall times of less than 1.2 ns. Complementary outputs can be obtained from the collector of Q1; however, if both collectors are used to outputs, the rise and fall times are degraded by approximately 100 ps.

Pulse Standardizer

One of the most important functions in fast logic modules is the generation of a pulse with a precise width that is independent of input pulse width, rise time, and duty cycle. The circuit shown in Fig. 7 utilizes MECL III components and two transmission lines to realize this function. The output pulse width is determined by the propagation delay of a transmission line. For input pulse widths longer than the propagation delay time, the circuit acts as a differentiator; for input pulse widths less than the delay time, the circuit acts as a "one-shot."

A positive transition of the input applied to the clock will cause the flip-flop to toggle since the $\bar{Q}$ output is connected to the D input. Because of the regeneration present in the flip-flop, the waveforms at the Q and $\bar{Q}$ outputs are not dependent on the input pulse width and rise time. In addition, the flip-flop is a good amplitude discriminator; if the input amplitude does not exceed the threshold there is a negligible amount of feedthrough to the outputs.

The inputs of gate M1 are connected to the Q and $\bar{Q}$ outputs of the flip-flop, but the $\bar{Q}$ connection is through a transmission line. Hence, if $\bar{Q}$ is at a down-level, Q is at an up-level, and the output of M1 will be a down-level. When the flip-flop changes state, the input of M1 connected to Q will switch to a down-level, but the input connected to $\bar{Q}$ will not switch to the up-level until a

time equal to the propagation delay of the line has passed. Therefore, the output of M1 will be at an up-level for a time equal to the propagation delay of the transmission line. The argument can be reversed to show that the output of M2 will be at an up-level for one propagation delay time after $\overline{Q}$ switches to a down-level. Since M1 and M2 are "wire OR'ed," the output will be pulses with a width equal to one propagation delay whenever the flip-flop toggles, i.e., whenever an input pulse is applied. Since the pulse width is determined by a transmission line, it is precise and unaffected by temperature. The output pulse width is constant if input pulses are separated in time (from leading edge to leading edge) by more than two line propagation delays; if the separation is less, the output pulse width is half the separation. With the two lines cut to 1.5 ns, the circuit operates at pulse repetition rates in excess of 300 MHz without shrinking.

Retriggerable One-Shot

Most instrumentation applications require the ability to generate output pulses of continuously adjustable width; this function is normally accomplished by a monostable circuit. The circuit shown in Fig. 8 generates a pulse with a width adjustable over the range of 2 to 100 ns. The input pulse is required to have a constant width and amplitude; this requirement is satisfied by first passing the signal through a pulse standardizer circuit. Gates M1 and M2 in Fig. 8 represent the output portion of a pulse standardizer.

In the quiescent state, the current from the current-source transistor, Q1, flows through gates M1 and M2, and the voltage across capacitor C1 is equal to the MECL III down-level (-2.0 V). A positive going pulse from the output of either M1 or M2 will charge C1 to the MECL III up-level of approximately -0.8 V. This charging is very rapid since M1 and M2 are MECL III gates with emitter-follower outputs; it requires typically 1 ns to fully charge C1. Diode CR2 (a hot carrier device) is incorporated to clamp the capacitor voltage at a level determined by CR2, CR3 (silicon), and CR4 (germanium). This clamping action reduces the overshoot on the capacitor and insures a constant amount of charge for each input pulse.

After the input-pulse duration, the emitter-follower outputs of M1 and M2 become reverse-biased, and the current flowing through C1 is principally due to the current source, Q1. Hence C1 discharges linearly at a rate determined by the collector current of Q1 until the quiescent state is again reached. The minimum current that Q1 should conduct, and therefore the maximum pulse width attainable, is limited by the consideration that the collector current of Q1 should be much larger than the base current of Q2 and the leakage currents of M1, M2, and CR2.

The source current is varied by adjusting the emitter current of Q1. The base voltage of Q1 is determined by the Zener drop of CR1, and the emitter current is adjusted by R3. The variation of the V_{BE} drop of Q1 and the Zener drop of CR1 with temperature tend to cancel each other to maintain a collector current which is fairly independent of temperature.

Transistors Q2 and Q3 are emitter-followers to insure a large value of equivalent impedance across capacitor C1. Since the V_{BE} drops of Q2 and Q3 tend to cancel, the logic levels at the input of M3 are close to MECL III levels. Furthermore, the temperature variation of the V_{BE} drops of Q2 and Q3 also tend to cancel, so that the threshold variation with temperature of M3 tracks the temperature variation of M1 and M2 as intended in the design of the MECL III circuits. The base resistors R5 and R8 are included to reduce the ringing introduced by the emitter-followers.

The waveform at the input of M3 is a triangular pulse with a fast rise time (typically 1.5 ns) and a fall time which is adjustable over the range of 1.5 to 200 ns. The logic gates M3 and M4, because of their small input-transition region, restore this to a square pulse with an adjustable width of 2 to 100 ns. Overall variation of pulse width with temperature is less than 5% over the temperature range of 0 to 75°C.

An inherent feature of this one-shot is the lack of recovery time. Capacitor C1 can be charged back to its up-level at any point in the discharge cycle; the output width then extends to the preset width after the last input. Thus, if the time between periodic inputs is less than the preset width, a dc up-level is produced at the output. This feature is usually termed "updating."

Module Design

The circuits described above, used to shift input and output levels and to standardize pulses, can be combined with MECL III IC's in a "building block" approach to form any arbitrary logic function. The MECL III gates and flip-flops are used for the logic realization. Four such modules have been constructed and field tested at the Lawrence Berkeley Laboratory; Fanout, Fan-in, Coincidence unit, and Prescaler. The building block approach is illustrated for the first three units in Figs. 9, 10, and 11, respectively. The Prescaler utilizes MECL III flip-flops to form a decade counter with carry; MECL II circuits are used for BCD decoding and translation to TTL data levels.

The four units are housed in size #1 NIM modules and use LEMO connectors for pulse signals. The modules require the standard ±6 V, + 12 V NIM Standard power bins and require less than the 6 W of power allowed per module. All modules process pulses with rise and fall times of less than 1 ns and operate at repetition rates in excess of 300 MHz. The propagation delays of the modules are, between 4 ns (Fanout) and 12 ns (Coincidence).

Circuit board layout is a very critical part of these fast logic modules. Extreme care is necessary to avoid oscillation and pulse distortion. Signal lines must be less than 1.5 inches or must

be properly terminated microstrip- or coaxial-transmission lines. Adequate ground plane and supply-bypassing are essential. The application notes, available from Motorola, are very useful for circuit layout procedures.[1, 2, 6, 7]

Acknowledgments

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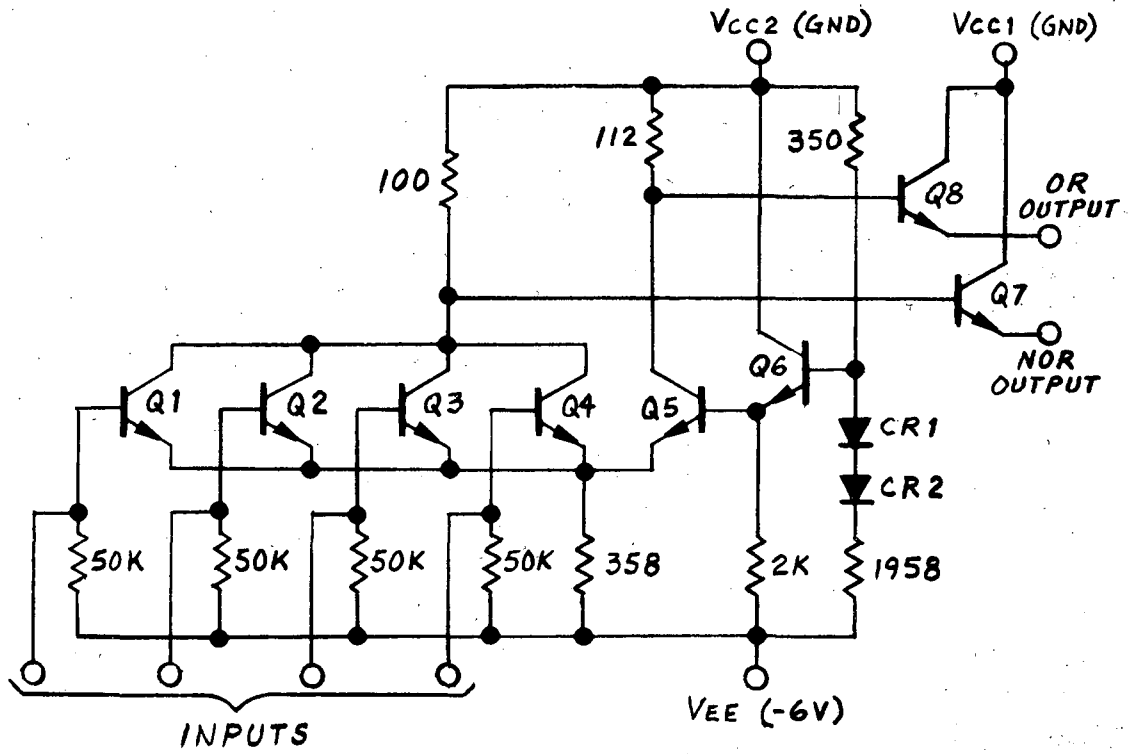

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Fig. 1. MECL III, 4-input OR-NOR gate; 1/2 MC1660S.

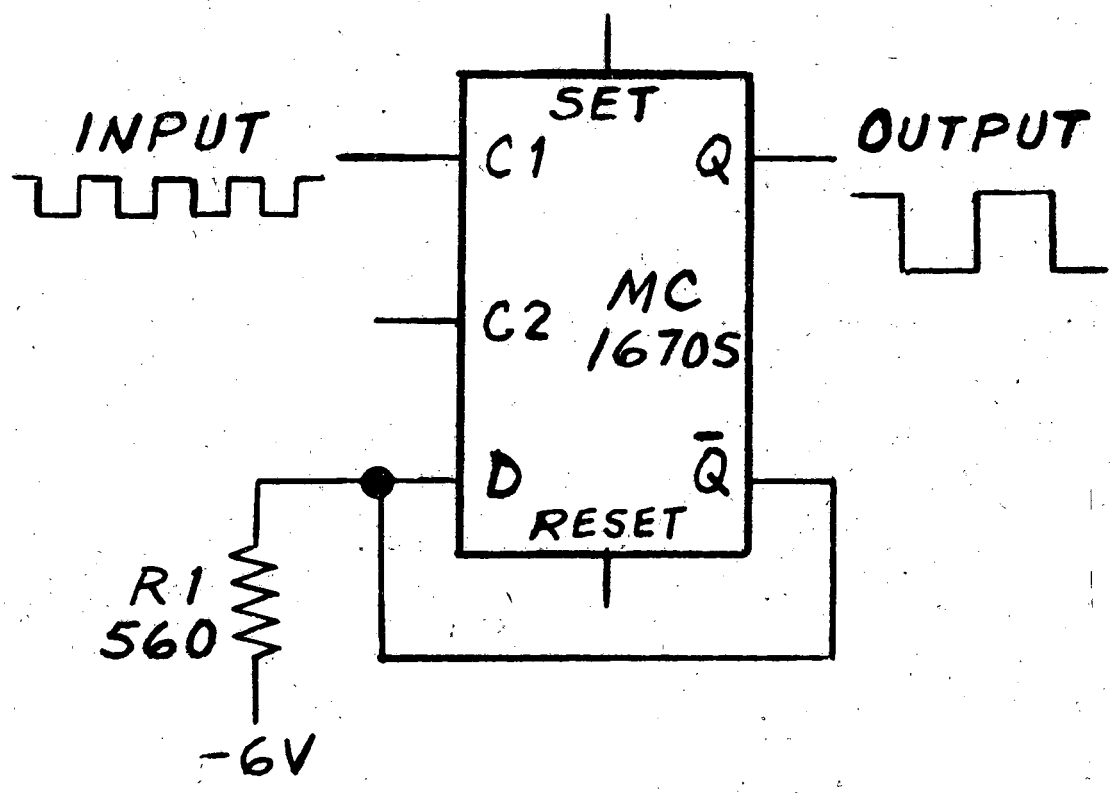

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Fig. 2. MECL III MC1670S connected for toggling.

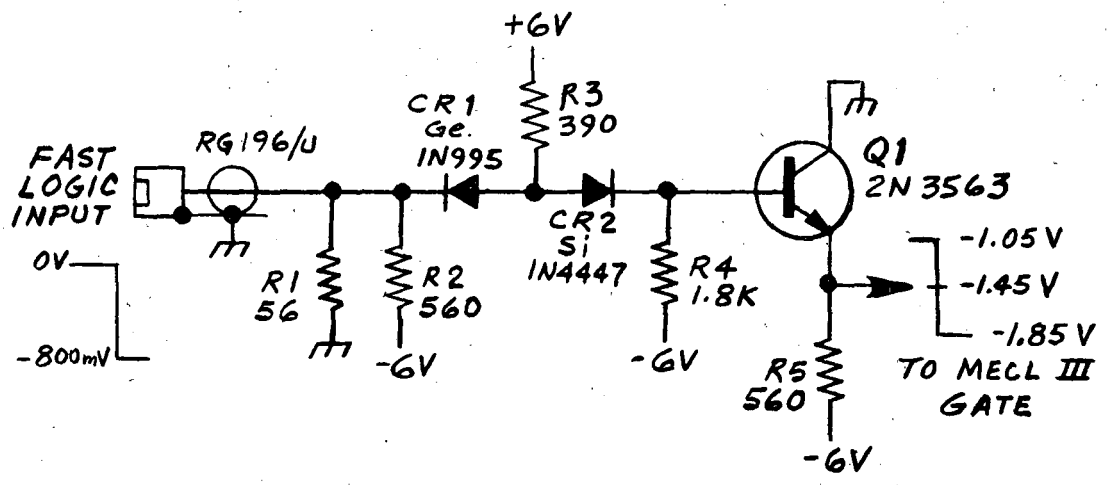

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Fig. 3. Basic NIM to MECL III input circuit.

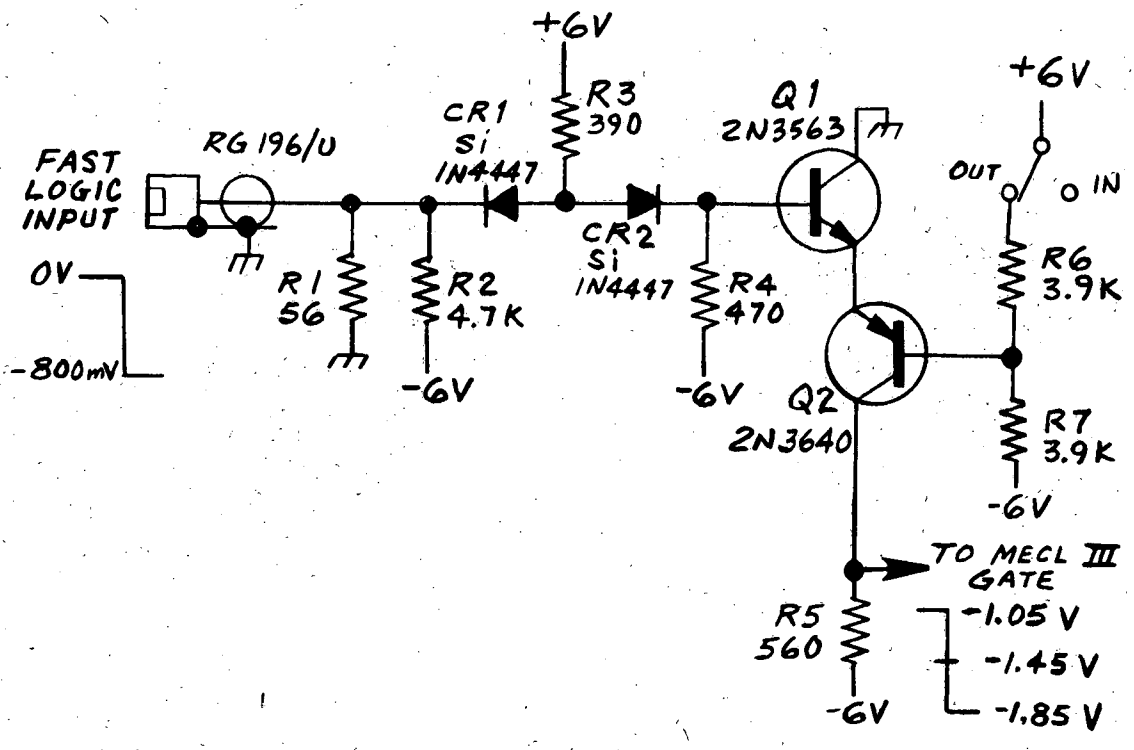

Fig. 4. Switchable input circuit.

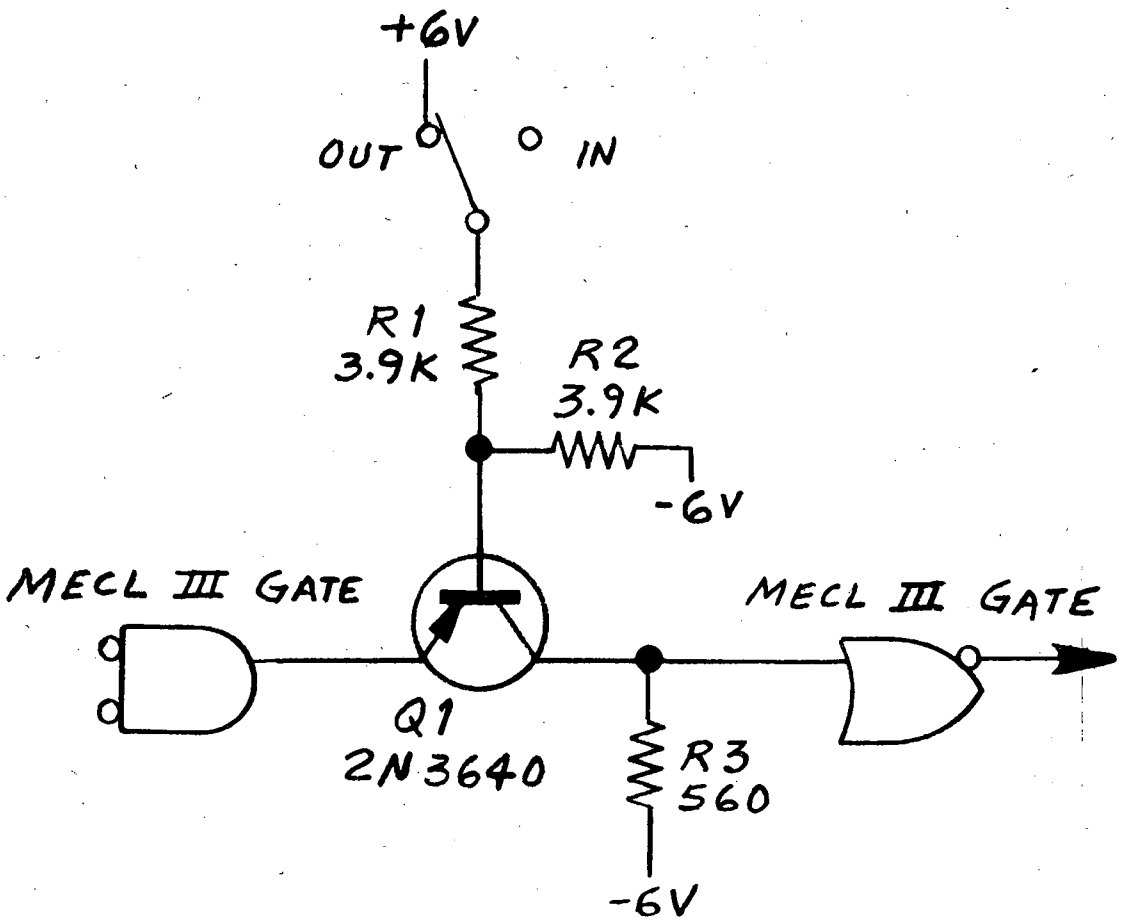

Fig. 5. Saturated switch used between MECL III gates.

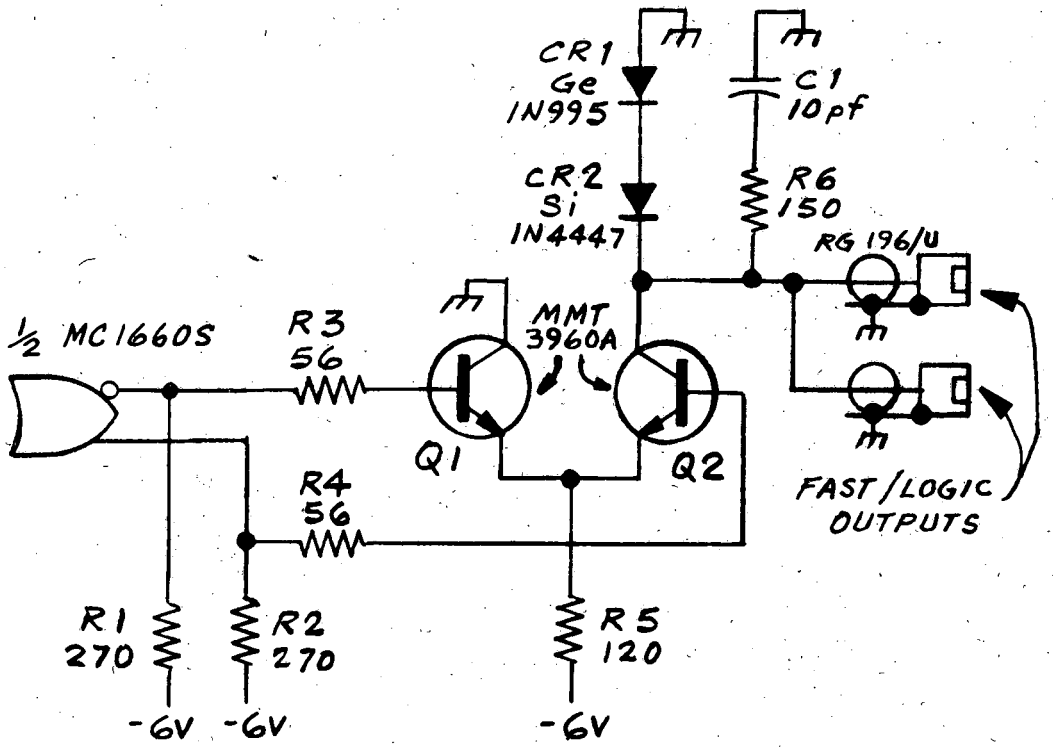

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Fig. 6. MECL III to NIM output circuit.

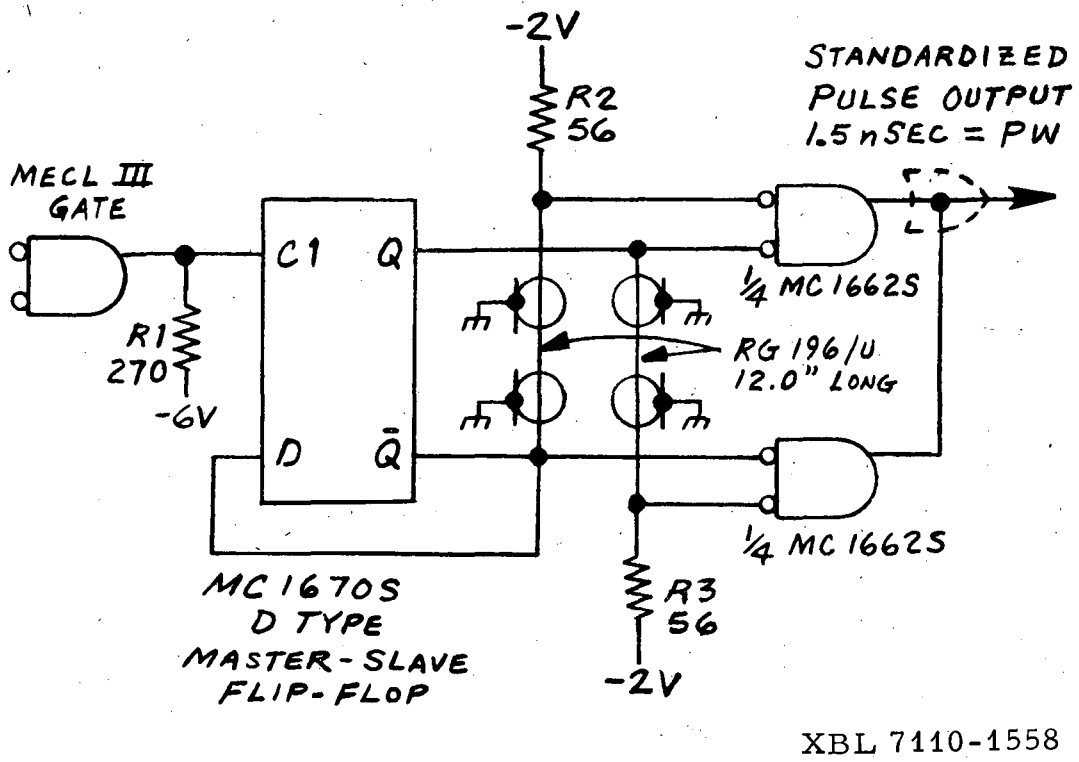

Fig. 7. Pulse Standardizer.

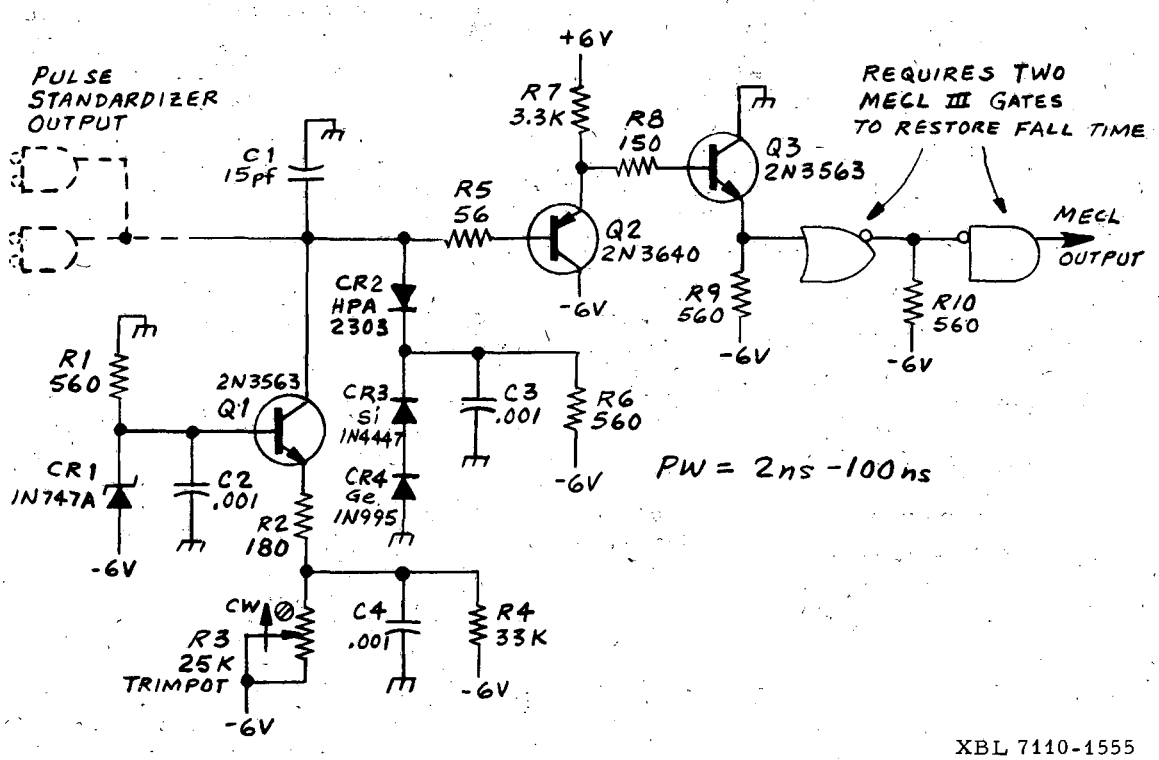

Fig. 8. Retriggerable one-shot.

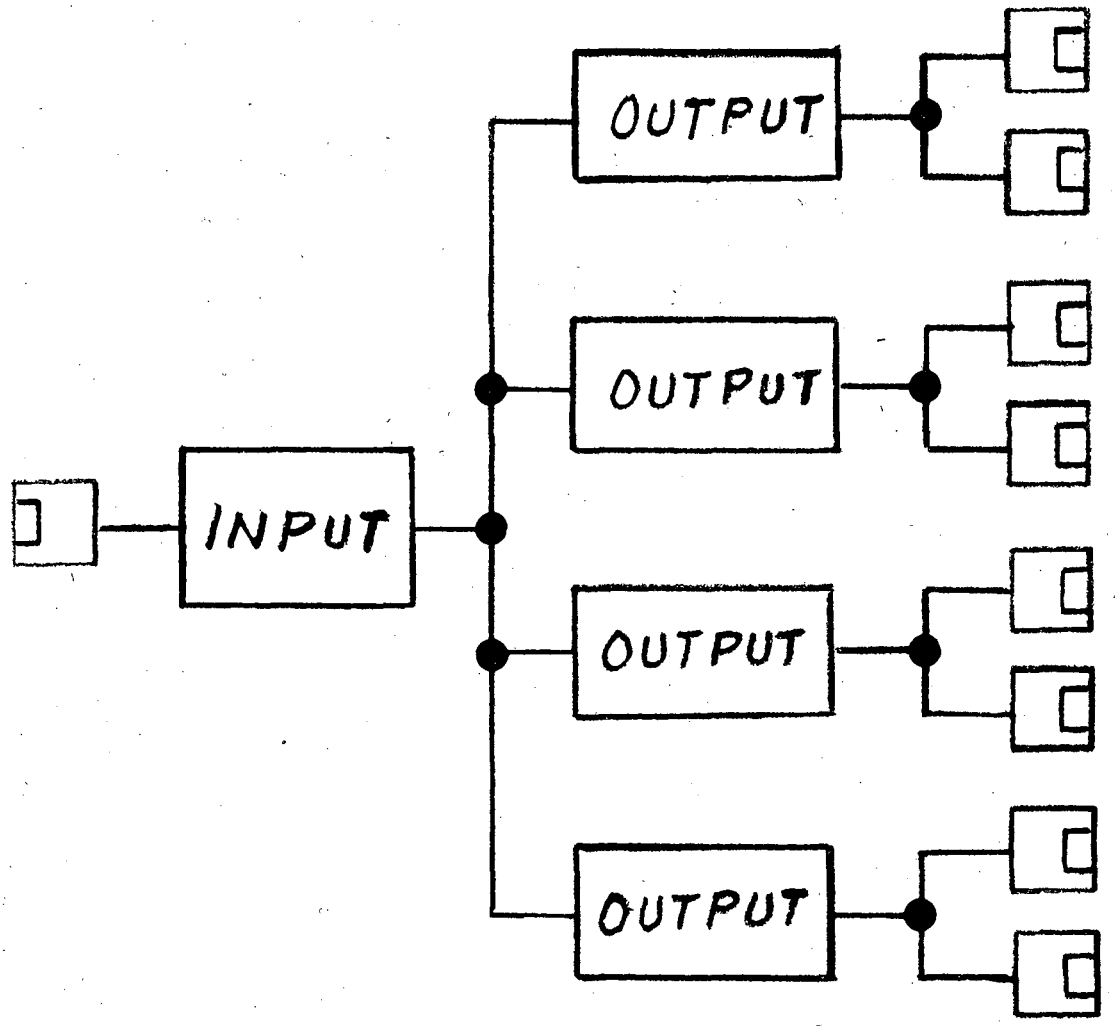

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Fig. 9. Fanout block diagram.

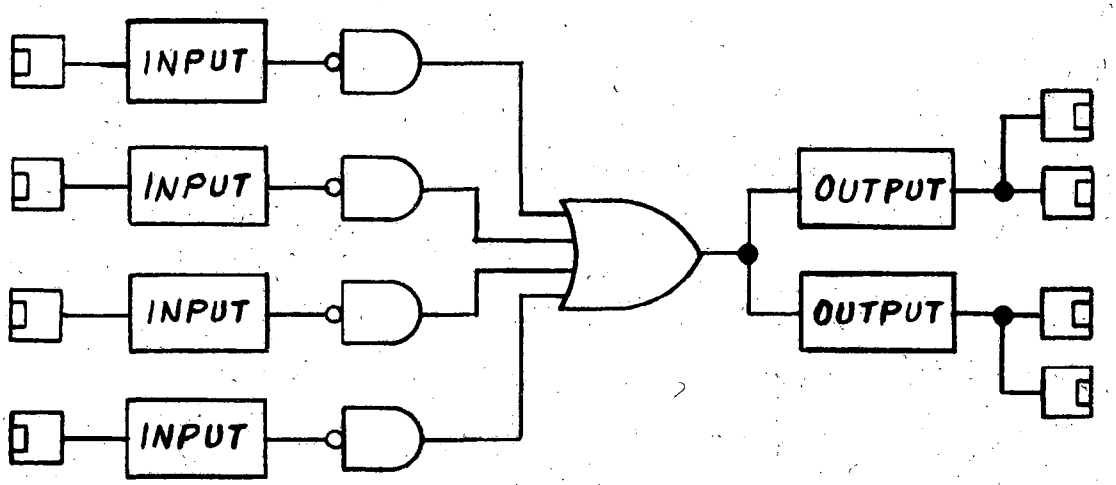

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Fig. 10. Fan-in block diagram.

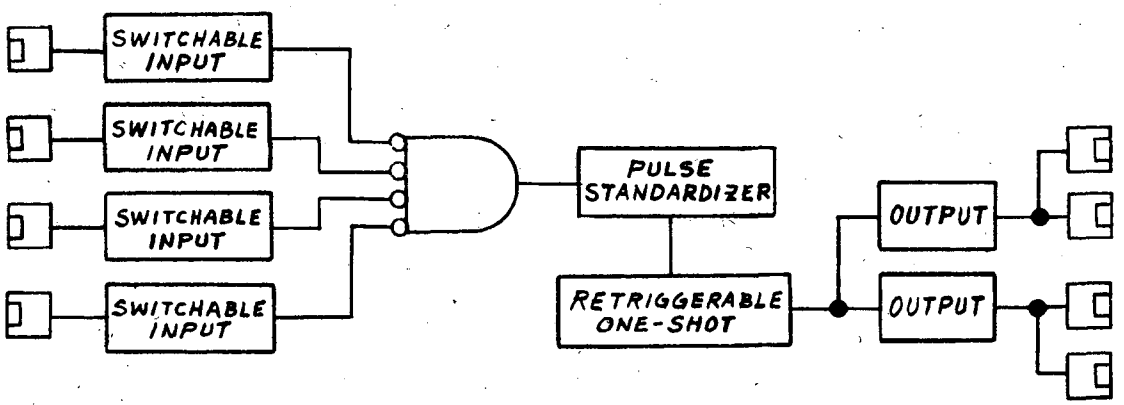

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Fig. 11. Coincidence block diagram.

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