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Understanding metal propagation in solid electrolytes due to mixed ionic-electronic conduction

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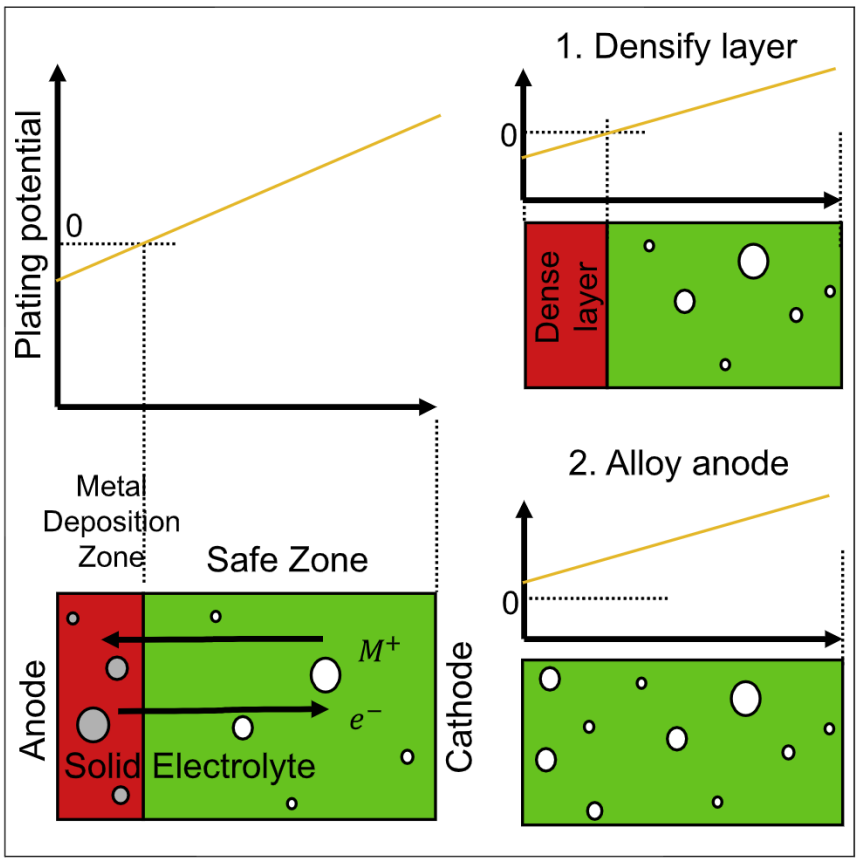

Internal Li deposition in isolated pores inside the solid electrolyte (SE) is found to be one of the main reasons for dendrites growth (short) in solid-state batteries, due to the presence of electronic conductivity of the SE. In this work we show for the first time a clear picture of how this happens and what the controlling factors are. We also propose several solutions to reduce/eliminate the dendrites growth caused by internal deposition.

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Highlights

Solid-state batteries can short due to the electronic conductivity of electrolyte

Internal Li deposition may fully fill in pores and fracture the solid electrolyte

A dense coating on the electrolyte surface can be one way to prevent dendrites

Lowering the anode equilibrium potential is the best way to prevent failure

3 **Understanding**
Dependency and conditional studies on material behavior

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Understanding metal propagation in solid electrolytes due to mixed ionic-electronic conduction

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SUMMARY

Metal penetration into a solid electrolyte (SE) is one of the critical problems impeding the practical application of solid-state batteries. In this study, we investigate the conditions under which electronic conductivity of the SE can lead to metal deposition and fracture within the SE. Three different stages for void filling (metal plating initiation, metal growth, and metal compression) in the SE are identified. We show that a micron-size isolated void in the SE near the anode can be quickly filled in by metal and fractured when the developed pressure in the void grows larger than the maximum pressure the SE material can sustain. We find that the anode voltage and applied current density play a significant role in determining the vulnerability to metal deposition. We discuss several strategies to prevent electronic conductivity-driven metal propagation in electrolytes that are not fully dense, including the densified layers between the anode and SE.

INTRODUCTION

Solid electrolytes (SEs) are widely believed to be compatible with metallic anodes for high-energy batteries because of their high mechanical strength and high ionic transference number.[1] However, metal penetration is frequently observed in SEs, including Li_2S-P_2S_5 (LPS),[2] $Li_7La_3Zr_2O_{12}$ (LLZO),[3] and beta-alumina.[4,5] Extensive studies have been conducted to explain the unexpectedly low maximum charging rate (critical current density [CCD]) that an SE can withstand without metal penetration (less than $1 mA/cm^2$).[6–8] Different mechanisms for metal propagation in SEs have been proposed, including possible low diffusivity of mobile cations at grain boundaries (GBs),[9] low relative density of SEs,[7] pre-existing microstructural defects (such as cracks and pores) on the surface of and in bulk SEs,[10] inhomogeneous plating resulting from contact loss between metal anodes and SEs,[11] and enhanced electronic conductivity in SEs resulting from vacancy generation during cycling.[4]

The proposed mechanisms for metal propagation in SEs can be categorized into two modes.[12] In the mechanisms that are controlled by microstructure and defects, the metallic phase nucleates at the anode/SE interface and propagates from the interface into the SE, leading to shorting upon contact with the cathode.[13] In this mode, the metal penetration is mainly caused by the uneven electrodeposition of metal at the anode/SE interface and in the SE, which is controlled by interfacial defects (such as surface roughness, pre-existing cracks)[14] and SE microstructure (such as percolating pores/GBs).[15] On the other hand, when electronic conductivity is an important factor in SE penetration, as has been recently argued,[16,17] the metallic phases can nucleate inside the SE, and shorting occurs when these nuclei

Progress and potential

Among the alternatives to conventional Li-ion batteries, solid-state batteries (SSBs) have the potential for high energy density with the use of a metal anode. However, the penetration of metal filaments into a solid electrolyte (SE) is an obstacle to the commercialization of metal anode SSBs. This work utilizes continuum modeling to study the mechanism of metal deposition within the SE due to the electronic conductivity of the SE. We show that metal deposition can happen in isolated micro-size voids within the SE and can cause catastrophic failure due to SE fracture. The vulnerability to metal deposition in the SE is investigated by controllable parameters (such as the cell voltage, applied current density, etc.), and suppression strategies of metal deposition are then proposed. These findings provide a deeper understanding of the Li penetration in the SE to eventually overcome the challenge in SSBs.

interconnect with each other through SE fracture. The dendrite growth in this mode requires the electronic conductivity of the SE to be high enough to transport electrons to pre-existing internal defects (such as vacancies, pores, and GBs). The two metal propagation modes may occur simultaneously in a real solid-state battery (SSB) system[4,5] making it difficult to study them separately.

The microstructure/defect-driven mechanism has been widely studied, and different strategies have been proposed to prevent or alleviate the propagation including decreasing the SE surface roughness[18] and increasing the anode/SE contact quality.[19] However, the electronic conductivity-driven mechanism has been much less explored both experimentally and theoretically. In early work, the deposition of sodium metal inside a β-alumina SE resulting from enhanced electronic conduction was studied.[4] Field-driven migration of silver metal particles on the surface of an SE (silver bromide single crystal) has also been observed, resulting from the mixed ionic-electronic conduction of the SE.[20] In more recent work, Li deposition inside bulk LLZO and LPS was directly observed using time-resolved operando neutron depth profiling.[16] The electronic conductivity in LLZO and LPS was believed to be mostly responsible for the Li dendrite formation in these SEs. Even nominally ionic conductors can have some level of electronic conductivity due to defects, impurities, or an intrinsically low band gap. In addition, the electronic conductivity of some inorganic ceramic SEs has been shown to increase rapidly under high voltage.[21,22] Work with density functional theory has shown that enhanced electronic conductivity can originate from point defects[23] and internal pores and crack surfaces in the SE.[24]

To systematically study the electronic conductivity-driven metal propagation in the SE, one must consider the SE as a mixed ionic-electronic conductor (MIEC).[25–27] In this work, we build an electro-chemo-mechanical model which incorporates mixed ionic-electronic conduction for SSBs[28,29] to describe metal propagation in an SE with microstructural defects (as shown in Figure 8 in the "modeling of the MIEC" section). We focus on isolated pore-type defects in this work (such as those in LPS) and neglect the effect of GBs. In the methodology section, a new framework for the metal deposition inside isolated pores of the SE and its coupling with SE fracture is established. The metal deposition in the void is divided into three stages (metal plating initiation, metal growth, and metal compression). The time needed to complete each stage is derived and related to the deposition-induced pressure in the void. The effects of void geometry (pore size, location), SE material properties (ionic/electronic conductivity and fracture toughness), and electrode chemical potentials on the metal deposition in the void are systematically investigated. We find that anode voltage, current density, and overall cell potential play a very significant role in determining the vulnerability for metal plating in the SE. Two efficient strategies to reduce/prevent electronic conductivity-driven metal propagation are proposed based on our analysis, including surface coating (or densification) and anode alloying. We point out difficulties with extrapolating results from symmetric cells or from non-metal anode cells to realistic SSBs that use a metal anode.

RESULTS

We present several solutions here, with the detailed methodology and modeling included in the "modeling of the MIEC" section. When the void size in Figure 8 is assumed to be infinitesimally small, the problem can be solved analytically (for details, see the supplemental information, section 2) and this analytical solution is useful to understand how voids create deviations in the potential and current. When the void is located within the range of SE where deposition can occur (region where the

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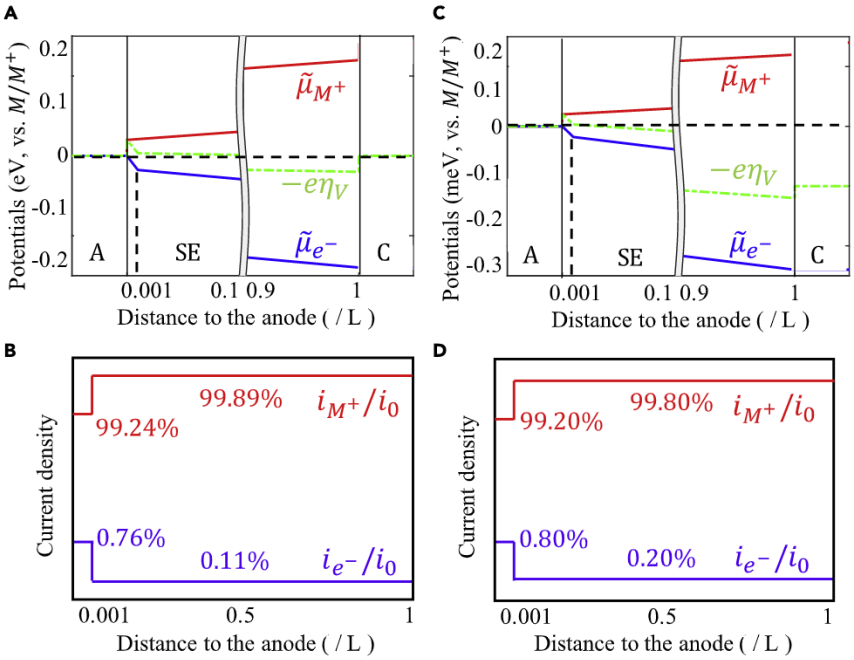

Figure 1. Potentials and current density profiles in the SSB cell

(A–D) Potentials and current density profiles in the SSB cell (A) and current densities (B) in the symmetric *M* cell. Potentials (C) and current densities (D) in an *M* metal anode cell ($\mu_M^A = 0$) with cathode chemical potential $\mu_M^C = -0.1\ eV$. A and C represent "anode" and "cathode." Lengths on the x axis of all plots is normalized by the SE thickness $L = 1mm$. The void is located $1\mu m$ from the anode. In (A) and (C), the potentials between $0.1L$ and $0.9L$ are hidden for a better view of the region near the anode and cathode. The current densities in (B) and (D) are not shown to scale due to their large difference in magnitude, but actual values are labeled on each line.

plating potential $\eta_V<0$), the ratio of deposition current density in the void (i_V) over the applied current density (i_0) is:

$$\omega = \frac{i_V}{i_0} = \frac{\left(\frac{R_C}{R_e}+\frac{L-a}{L}\right)\frac{\mu_M^A/F}{R_A i_0} + \left(\frac{R_A}{R_e}+\frac{a}{L}\right)\frac{\mu_M^C/F}{R_A i_0} + \left(\frac{L-a}{L} - \frac{R_C}{R_A}\frac{a}{L}\right)}{\frac{R_C}{R_e}+\frac{L-a}{L}+\frac{R_V}{R_e}+\frac{R_V}{R_A}+\frac{R_V R_C}{R_e R_A}+\frac{R_C}{R_A}\frac{a}{L}+\frac{R_e}{R_A}\frac{a(L-a)}{L^2}}. \qquad \text{(Equation 1)}$$

Here, the thickness of the SE is *L* and the void is located a distance *a* from the anode. The electronic resistance (R_e), charge-transfer resistance at the anode/SE interface (R_A), cathode/SE interface (R_C), and void/SE interface (R_V) are defined as $R_e = L/\sigma_{e^-}$, $R_A = \frac{RT}{i_{exc}^A F}$, $R_C = \frac{RT}{i_{exc}^C F}$, and $R_V = \frac{RT}{i_{exc}^V F}$, respectively. Equation 1 indicates that the ratio of plating current to total current, ω, is affected by the *M* chemical potential in the electrodes (μ_M^A, μ_M^C), the applied current density i_0, and the area-specific resistances (R_A, R_C, R_e, R_V).

Figure 1 shows the distribution of the potentials ($\tilde{\mu}_{e^-}$, $\tilde{\mu}_{M^+}$) and current densities (i_{e^-}, i_{M^+}) with typical parameters used in experiments: SE thickness $L = 1mm$, void located at $x = 1\mu m$, applied current density $i_0 = 0.2mA/cm^2$, ionic conductivity $\sigma_{M^+} = 0.1mS/cm$, electronic conductivity $\sigma_{e^-} = 10^{-3}\sigma_{M^+}$. Figures 1A and 1B show the potentials and current densities in a symmetric metal cell, and Figures 1C and 1D show same quantities in a cell with a metal anode and the cathode voltage raised by 0.1 V (chemical potential $\mu_M^C = -0.1\ eV$). While the cathode potential may appear to be unrealistically low, we show below that all relevant effects with a real cathode can be observed for this scenario. The plating potential η_V for *M* metal deposition in the void is multiplied by "$-e$" for unit consistency ($-e\eta_V = \tilde{\mu}_{M^+} + \tilde{\mu}_{e^-}$). The electronic current density (i_{e^-}) in Figures 1B

Table 1. Key parameters used in this work

Name	Symbol	Unit	Value	Ref.
Exchange current density at the electrode/SE interface	i^k_{exc}	mA/cm^2	1.3	Chiku et al.[30]
Exchange current density at the void/SE interface	i^V_{exc}	mA/cm^2	0.01	Tian et al.[17]
Ionic conductivity in the SE	σ_{M^+}	mS/cm	0.1	Bachman et al.[31]
Electronic conductivity in the SE	σ_{e^-}	mS/cm	10^{-4}	Han et al.,[16] Shin et al.,[32] Minami et al.[33]
Electric conductivity in the M metal	σ_M	mS/cm	10^5	Bastea and Bastea[34]
Fracture toughness of the SE	K_c	$MPa\cdot\sqrt{m}$	0.2	McGrogan et al.,[35] Rouxel and Yoshida,[36] Nose[37]
Bulk modulus of the M metal	K	GPa	11	Masias et al.[38]

and 1D are scaled to be comparable with the ionic current i_{M^+}, but the actual values are provided near each line.

For the material parameters in Table 1 and the current condition imposed, a gradient of the electronic potential ($\Delta\tilde{\mu}_{e^-} = 0.21\ eV$) drives electrons in the SE to migrate from the anode to the cathode, and a gradient of the electrochemical potential of M^+ ions in the SE ($\Delta\tilde{\mu}_{M^+} = 0.2\ eV$) drives M^+ to migrate from the cathode to the anode. A surface overpotential $\eta_{A/C} = 4.0\ mV$ is needed for the plating of M at the anode/SE interface and the stripping of M^+ ions at the cathode/SE interface (according to Equation 9). At the void, the slope of the electronic potential $\tilde{\mu}_{e^-}$ changes as some current is absorbed in the void (Figures 1B and 1D). This slope change is not noticeable in the ionic potential $\tilde{\mu}_{M^+}$ as the fraction of ionic current i_{M^+} absorbed in the void is negligible compared with the total i_{M^+}. In the symmetric cell, the deposition current in the void is only ~0.65% of the total applied current i_0 (Figure 1B). This value decreases to ~0.60% when the cathode potential is raised by 0.1 V (Figure 1D) as the electronic chemical potential ($\tilde{\mu}_{e^-}$) is lowered in the SE by the lower Li-ion chemical potential in the cathode. The fraction of current absorbed in the void increases rapidly as the void is closer to the anode, or when a higher current i_0 is applied. For example, when the void is located $0.1\mu m$ from the anode and the applied current density is $i_0 = 2\ mA/cm^2$, the deposition current density i_V increases to ~1.5% i_0.

It is important to evaluate the fraction of the SE that is susceptive to internal M deposition. We define the region in which M deposition can occur as $[0,a_0]$, where a_0 is the position where plating potential η_V (or deposition current i_V) is zero. The value of a_0 can be found by setting i_V in Equation 1 to zero, resulting in:

$$\frac{a_0}{L} \approx \frac{i_0 R_A + \frac{\mu^A_M}{F}}{i_0(R_A + R_C) + \left(\frac{\mu^A_M}{F} - \frac{\mu^C_M}{F}\right)} = \frac{\eta_A - V_A}{\eta_A + \eta_C + (V_C - V_A)}. \qquad \text{(Equation 2)}$$

Here, η_A and η_C are the Butler-Volmer overpotentials at the anode/SE and cathode/SE interfaces, and V_A and V_C are the equilibrium voltage in the anode and cathode, respectively. This equation can be understood fairly intuitively as it indicates that the fraction of the SE susceptible to plating is proportional to the amount by which the anode sits below the Li metal potential and inversely proportional to the overall potential drop across the electrodes. For example, a_0 reaches a maximum ($a_0 = 0.5L$) for a symmetric cell ($\mu^A_M = \mu^C_M = 0$, $R_A = R_C$). This can be understood as a symmetric metal cell keeps the electronic chemical potential high everywhere in the SE. In a real cell, the increasing of the cathode voltage reduces the fraction of the SE that is exposed to a negative plating potential. Even increasing the cathode potential to only 0.1 V in Figure 1C ($\mu^A_M = 0$, $\mu^C_M = -0.1\ eV$) decreases a_0 to $0.04L$. This decrease

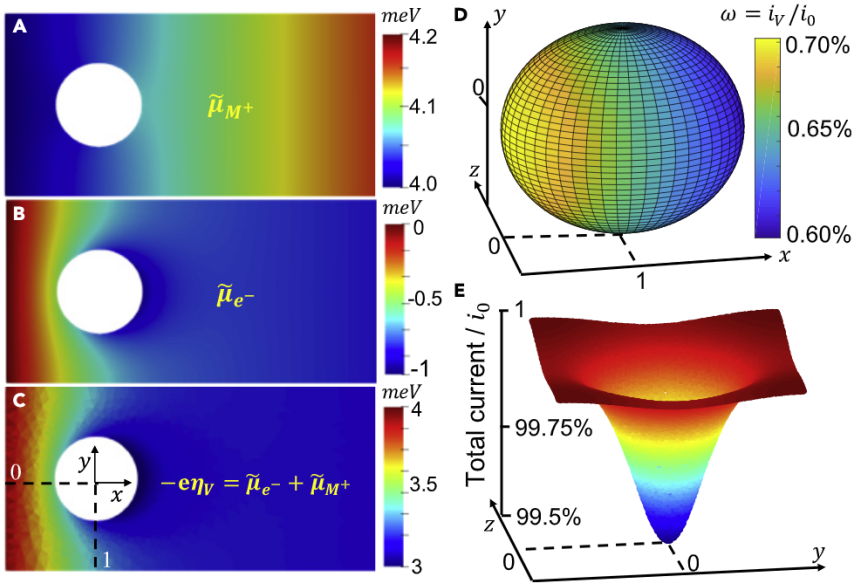

Figure 2. Distribution of potentials and current densities affected by the void in the SE

(A–C) Distribution of potentials in a symmetric SSB cell around the first void (with diameter d_V = 1μm and located at x = 1 μm, y = z = 0). Only values in the range: 0<x<4 μm, −1 μm<y<1 μm and z = 0 are shown here.

(D) Deposition current density around the first void.

(E) Total current density at the anode/SE interface. Both the vertical coordinate and the contour plot represent the magnitude of the deposition current. All the length units in the figures are in μm.

is also reflected in the plating potential ($-e\eta_V$), which is pulled down at the cathode side by an amount that is equal to the cathode voltage. Notably, in a metal anode cell, decreasing μ_M^C (increasing cathode voltage) can narrow the range in which M metal deposition occurs, but cannot stop the deposition because a_0 is always positive when the anode equilibrium voltage is zero ($\mu_M^A = 0$). However, it is possible to fully prevent metal deposition by increasing anode voltage (e.g., alloy anode). The increase in anode voltage needs to be just enough to offset the anode overpotential, $\frac{\mu_M^A}{F} \leq -\ i_0 R_A$ ($V_A \geq \eta_A$). For example, when $\mu_M^A \leq -4.0\ meV$ in Figure 1C, no deposition occurs regardless of the position of the void. This indicates that even minor anode voltage changes can modify the Li penetration behavior in the SE. Indeed, many demonstrations of SSB in which no Li metal penetration occurs use a non-metal anode.[39,40]

The previous results are obtained under the assumption of an infinitesimally small void, which allows the current distributions to be obtained analytically. To study the actual filling of finite voids and their perturbative effects on the current distributions we use numerical simulations. Computational details are given in the supplemental information, section 4. Figures 2A–2C shows a 2D cut (at z = 0) of the potentials at the start of metal plating near the void that is closest to the anode (detailed 3D potential distributions are shown in Figure S3). We only show deposition in the first void since its deposition current makes up more than 70% of the total deposition current in all voids of the SE. Similar to the 1D results shown in Figure 1A, the electronic potential $\tilde{\mu}_{e^-}$ is significantly perturbed around the void (Figure 2B), whereas little change is observed for the ionic potential $\tilde{\mu}_{M^+}$ (Figure 2A). Figure 2D plots the deposition current density (i_V) at the surface of the first void. The part of the surface in yellow color, indicating the largest current, is oriented toward the anode. The average deposition current density ($\bar{i}_V$) is 0.65% i_0, which is similar to the analytical

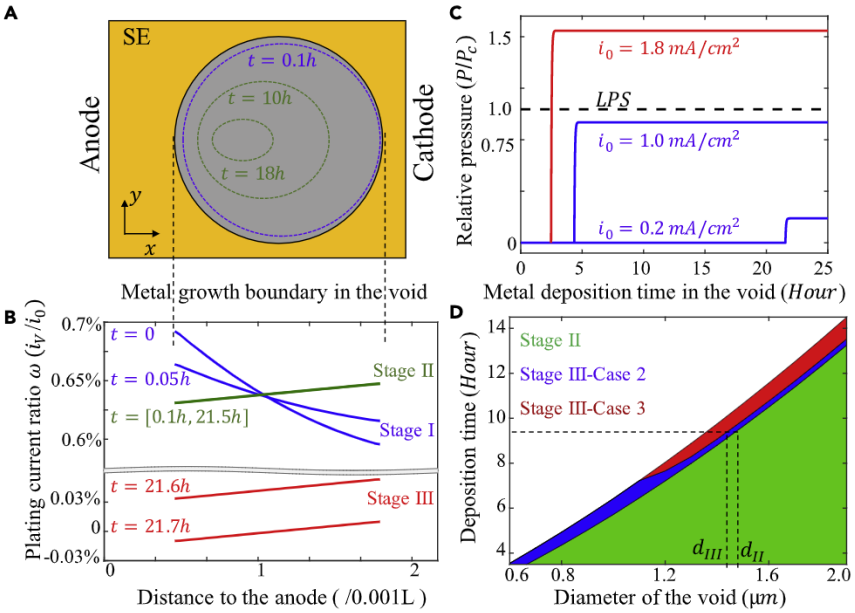

Figure 3. Evolution of *M* metal deposition from stage I to stage III in a spherical void in the SE

(A) Metal boundary at three deposition time. The metal thickness at $t = 0.1\ h$ is smaller than shown but scaled up ten times for a better view.

(B) Deposition current at different time. Each curve is averaged along *y* and *z* from the 3D data in Figure S3. The vertical axis is broken between 0.05% and 0.58%.

(C) Pressure in the void as function of time under three applied currents. The black line is the critical pressure for fracture of an LPS-type SE.

(D) Deposition time for different void sizes. The green area represents the time for metal growth (stage II), and the blue and red areas represent the time for metal compression, with blue for stage III-case 2 (no SE fracture) and red for stage III-case 3 (SE fracture). d_{II} is the critical diameter to separate stages II and III, and d_{III} is the critical diameter to separate stage III-case 2 and stage III-case 3, at the same deposition time.

value shown in Figure 1B. Figure 2E shows the magnitude of the total current density going into the anode. In this graph, the point ($y = z = 0$) is the projection of the void center in the anode plane. Shadowing by the void reduces the current by 0.5% at the point ($x = y = z = 0$) but the total current converges to the applied value ($i_0 = 0.2\ mA/cm^2$) far enough from the center. The shadowing effect rapidly increases as the void approaches the interface. For example, the current inhomogeneity increases from 0.5% to 4% when the void is moved from $0.001L$ to $0.0001L$ from the anode. Therefore, the total current distribution is not only affected by the electrode/SE interface [41] but also by pores within the SE.

The filling of the void occurs in a somewhat surprising way. At the start of charging ($t = 0$, beginning of stage I), *M* metal is plated on the surface of the void closest to the anode as the deposition is limited by the electronic current. However, the deposition current changes as more *M* metal is deposited. This is because plating of metal in the void changes the electronic current thereby modifying where the plating potential is largest. Figure 3A shows the evolution of the metal boundary (dashed ellipses) in the void under an applied current $i_0 = 0.2 mA/cm^2$, and Figure 3B shows the averaged deposition current along the *x* direction obtained by integrating the void surface current in the *y* and *z* coordinates (detailed results are given in Figures S3 and S4). Although our results indicate that metal deposition (stage I, as described in Figure 9 in the "modeling of the MIEC section") initiates more strongly on the anode-facing side of the void as it has the largest plating potential for deposition

(blue curves in Figure 3B), the current pattern changes quickly after deposition has started (green curve). Once a small layer of *M* metal is plated, electrons flow through the *M* metal because of its much larger electric conductivity ($\sigma_M = 10^5 mS/cm$), leading to an almost equipotential behavior of $\tilde{\mu}_{e^-}$ along the void surface where metal has already plated. Therefore, the pattern of the deposition current i_V becomes mostly determined by the ionic potential $\tilde{\mu}_{M^+}$ through the relation: $i_V \propto \eta_V \propto (\tilde{\mu}_{e^-} + \tilde{\mu}_{M^+})$. This causes metal deposition to become larger on the side of the void facing the cathode (stage II in Figure 9). This remarkable reversal of which side in the void the metal front grows the fastest is illustrated in Figure 3B. While initially the deposition current declines as one moves further away from the anode, after about 0.1 h (for the conditions in the simulation), the current reverses and the void starts to fill faster from the side facing the cathode.

Once the void fills up with metal, continued deposition causes the pressure to rapidly increase (stage III). This is shown as function of time (Equation 12) for three applied current densities i_0 in Figure 3C. The developed pressure *P* depends on i_0 because larger current densities create larger plating potentials in the void. Plating only stops when the pressure in the void increases the chemical potential of the metal *M* enough to balance this plating potential. Under some circumstances, this limiting pressure may be higher than the critical pressure for fracture. Fracture resistance of ceramics is measured by the fracture toughness K_c, which can be related to the maximum pressure can be sustained, $P_c = \frac{K_c}{f(d_V,a)\sqrt{\pi a}}$. As a reference, the horizontal black line in Figure 3C represents the critical pressure required to fracture an LPS-type SE (with $K_c = 0.2\ MPa\cdot\sqrt{m}$). The material will fracture when $P/P_c \geq 1$, indicating that, even for reasonable current densities, the pressure in a filled void in the SE can crack the SE. It should also be noted that the pressure inside an enclosed void can become considerably larger than the yield stress of Li metal. In our example, the pressure grows to over 100 MPa even for a reasonably low current density of 1.0 mA/cm^2. Notably, slightly different values for the LPS fracture toughness K_c are reported in the literature within the range $(0.2 \sim 0.23)\ MPa\cdot\sqrt{m}$. [35,36] The maximum pressure P_c may increase by ~ 10% if the largest K_c is used. However, this small effect on the SE fracture is negligible compared with other factors, such as the void size and location, and the electronic conductivity of the SE, as discussed in the following.

When cracking does not occur, a dynamic equilibrium takes over in the void. Once the pressure builds up in the void, the deposition current i_V decreases, as shown by the red curves in the bottom panel of Figure 3B, and as prescribed by Equation 11. Because the pressure *P* is the same everywhere in the *M* metal, the deposition current uniformly shifts down until deposition and stripping in the void is balanced. At this point metal enters from the side facing the cathode, and leaves the void on the side facing the anode.

Figure 3D shows the total time needed to reach the different stages in different sized voids for an applied current density $i_0 = 1 mA/cm^2$. For times and diameters in the green area of the graph, the void is being filled with metal (stage II). The blue and red areas represent the stage III growth. For conditions in the blue area, a dynamic equilibrium of *M* metal deposition/dissolution is present in the void (stage III-case 2). Fracture occurs in the red area (stage III-case 3). Figure 3D shows that the total deposition time to finish all three stages is dominated by the time required for filling the void during stage II (green area). In our specific case, if the charging time is less than 4 *h*, voids with diameters larger than 0.8 μm will not be filled at the end of the charge and, therefore, no pressure will be developed. These voids may get depleted of metal again in the discharge process. However, if the charging time is long or if

the applied current is larger (approaching the CCD), more (and larger) voids will reach the irreversible stage III-case 3 (SE fracture, red area). The results in Figure 3D also indicate that, while larger voids take longer to fill, which may appear beneficial, they are at greater risk of propagating fracture once they are filled.

As shown in Figure 3D, at the same deposition time, there are two critical void diameters that separate the different stages: d_{II} is defined to separate stage II and stage III (the size when void space equals to metal volume and no pressure is developed), and d_{III} is defined to separate stage III-2 and stage III-3 (the size when the terminate pressure P_T equals the maximum pressure P_c). The cell charging time is usually defined by the cell capacity C_A and the applied current density ($t = \frac{C_A}{i_0}$). By comparing the charging time and the total time needed to reach different stages, it is possible to relate the cell capacity (C_A), the applied current density (i_0), and the critical void diameters (d_{II}, d_{III}), as given in Equation 3 (for details see the supplemental information, section 3):

$$d_{II} = \frac{6\overline{V}_M}{F}\omega C_A \qquad \text{(Equation 3a)}$$

$$e^{-c_2\frac{C_A/i_0}{d_{III}}} + \frac{c_3}{\omega i_0\sqrt{d_{III}}} = 1. \qquad \text{(Equation 3b)}$$

The plating current ratio ω is defined in Equation 1 ($\omega = i_V/i_0$). The constant c_2 and c_3 are: $c_2 = \frac{6K\overline{V}_M^{\,2} i_{exc}^V}{RTF}$ and $c_3 = \frac{K_C\overline{V}_M i_{exc}^V}{RTf}$ (refer to Table S1 for definitions of other variables). Equation 3a shows that the critical diameter d_{II}, below which a void is filled by metal, is proportional to the cell capacity C_A and the plating ratio ω (depending on the applied current, electrode chemical potentials, electronic conductivity, and void location in Equation 1). Notably, in the symmetric cell ($\mu_M^A = \mu_M^C = 0$, $R_A = R_C$), the plating ratio ω only depends on the SE properties (electronic conductivity and void location), and therefore d_{II} is only a function of C_A. Equation 3b can only be solved numerically but an inverse parabolic relation can be observed between d_{III} and i_0. This is because a small void requires a higher critical pressure for SE fracture ($P_c \propto 1/\sqrt{d_V}$). Even though less time is required to completely fill in smaller voids, they are less able to fracture the SE. To limit the number of variables for analysis, and represent a realistic scenario, we extend our analysis in Figure 4A under the constraint of a fixed areal capacity $C_A = 4\ mAh/cm^2$ for an M metal symmetric cell, as has been used in many experiments. [13,40,42] For a given void located 1 μm from the anode, the condition of the void at the end of the charge can be determined according to its diameter d_V and the applied current i_0, as shown in Figure 4A.

When the void size in the SE is large ($d_V > d_{II} = 0.8\ \mu m$, Equation 3a), the charging time is not sufficient for the metal to completely fill the void (green area in Figure 4A). Smaller voids can act as fully reversibly metal reservoirs when the current density is small enough (blue area), but will fracture under charging with high current densities (red area). The boundary between these two areas defines a CCD that the SE can withstand before fracture. The CCD increases as the void diameter decreases, as explained in Equation 3b.

Figure 4B shows the relative deposition current ($\bar{i}_V/i_0$) of the voids in the SE under an applied current $i_0 = 0.2 mA/cm^2$ for different electronic conductivities as a function of the position of the void. The deposition current decreases rapidly when voids are positioned deeper within the SE. This is because both the electrochemical potential of electrons ($\tilde{\mu}_{e^-}$) and the plating potential ($-e\eta_V = \tilde{\mu}_{M^+} + \tilde{\mu}_{e^-}$) decrease rapidly (Figure S5). For SE materials with higher electronic conductivity, the average deposition

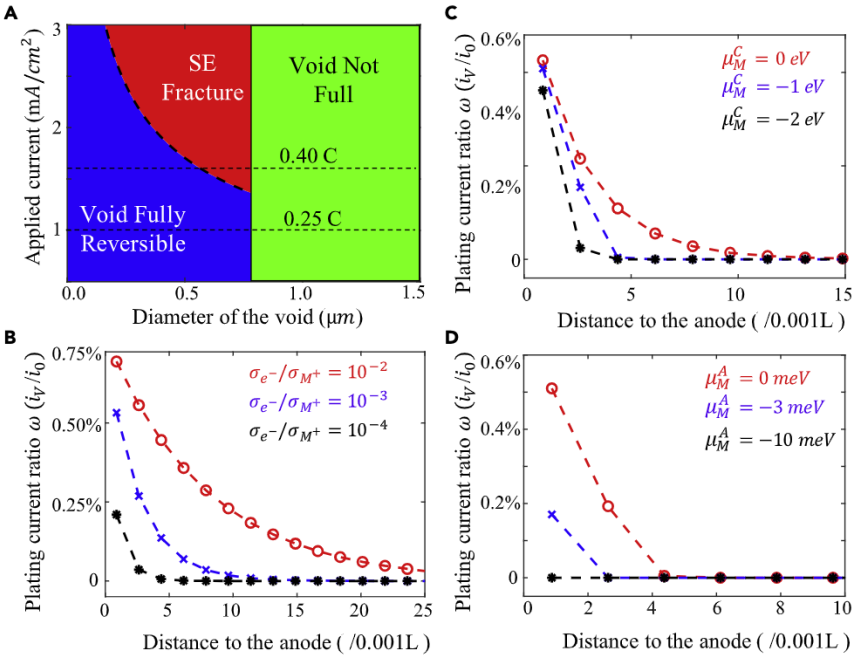

Figure 4. Deposition status in the void and effects of key parameters

(A) Evolution of voids in an SE as function of void diameter and applied current. For the green area the void is never filled upon charging. In the blue area the void will be filled but the pressure developed is not sufficient to fracture the SE. For conditions in the red area the void will fracture. The areal capacity is 4 mAh/cm^2. The two horizontal lines (0.25*C* and 0.40*C*) indicate the C-rate for the corresponding applied current.

(B–D) Distribution of deposition current i_V under applied current density of $0.2mA/cm^2$, at three different SE electronic conductivities (B), three different *M* chemical potentials in the cathode when the anode is *M* metal (C), and three different *M* chemical potentials in the anode when *M* chemical potential in the cathode is $\mu_M^C = -1\ eV$ (D).

current is larger and decays much more slowly. However, the deposition current still decays to a negligibly small value for voids located deeper than 0.02*L*. Therefore, preparing a sufficiently dense or void-free surface of the SE at the anode side can be an efficient strategy to prevent *M* metal deposition in the voids of the SE.

Figures 4C and 4D evaluate the effect of cathode and anode chemical potential under an applied current $i_0 = 0.2mA/cm^2$ and electronic conductivity $\sigma_{e^-} = 10^{-4}mS/cm$. Although lowering the *M* chemical potential in the cathode increases the decay rate of the deposition current in the voids deeper in the SE (Figure 1C, a_0 shifts toward the anode), it does not decrease the magnitude of the deposition current in the first void significantly, which is the void most vulnerable to SE fracture. Therefore, changing the *M* chemical potential in the cathode is not an efficient strategy to prevent *M* metal deposition in the void. However, lowering the *M* chemical potential in the anode (even by a few *meV*) not only rapidly decreases the deposition current in the first void but also increases the decay rate of the deposition current in the voids across the SE. Therefore, an alloy anode with sufficiently low *M* chemical potential will prevent *M* metal deposition in the void.

DISCUSSION

In this paper we investigated the effect of electronic conductivity in an SE on possible plating of metal inside pores of the SE. Our findings show that metal deposition in the SE is indeed possible and depends in a substantial way on the electronic

and ionic conductivity, the local current density and location of the void, the anode voltage, and the anode-cathode voltage difference. For symmetric metal cells, the SE is most vulnerable to plating as half of the SE is exposed to a favorable plating potential. In contrast, cells in which a real cathode is used, the large potential gradient in the SE limits metal deposition to voids close to the anode, although this region can propagate as filled voids back-connect to the anode.

Three different plating conditions are identified in this work, one of which leads to electrolyte fracture by pressure build up in the void and defines a CCD. The results in Figures 3 and 4 show that the maximum applied current that the SE can withstand due to *M* metal deposition in the void is highly related to the microstructure of the SE (e.g., the void sizes and locations). Our analysis also indicates that CCD will depend on the time of charging. Most CCD values from experiments are obtained for cycling times of less than 2 h. But longer charging times that displace more metal to the anode will reduce the CCD as the sub-critical voids (blue/red regions in Figure 4A) that were not filled under short-time charging conditions, may become filled and turn critical under longer charging time. Therefore, to obtain a meaningful and rigorous CCD of an SSB cell, maintaining long charging at each i_0 is necessary. Moreover, when comparing CCDs between different SSB cells, the CCD must be correlated to the cell capacity (determining the total charging time), SE microstructure (determining the void size and time to completely fill in the voids), and SE material properties (such as the electronic conductivity and SE fracture toughness). The correlation between the cell performance (or CCD) and SE microstructure has been widely studied in both oxide-type SEs[26,27] and sulfide-type SEs.[1,43] Notably, the void size in the SE rather than the SE porosity is the real factor affecting the CCD. For example, investigating LLZO Hatzell and colleagues[26,27] concluded that smaller void size yields higher CCD, consistent with our work. These authors also showed that lower SE porosity leads to lower CCD, which may seem inconsistent with our work (Figure 4A). This apparent discrepancy in findings stems from the different synthesis methods used for sulfide and oxide SEs. Whereas the holding/cold pressing used for sulfides reduces SE porosity and pore size,[43] oxide SEs are sintered, which reduces SE porosity but increases pore size.[26] It should also be noted that the CCD value in the work of Hatzell and colleagues ($\sim 0.1\ mA/cm^2$) was much smaller than that in our current work ($\sim 1\ mA/cm^2$). This is because the LLZO material used in their work was polycrystalline with GBs for which the electronic conductivity is larger[44] and the fracture toughness is smaller than their intrinsic bulk values.[45] Therefore, a larger deposition current and lower critical pressure is expected (Figures 4A and 4B), leading to a lower CCD for a polycrystalline sample. Single-crystal LLZO exhibits a higher tolerance to the applied current. Experimentally a Li/LLZO/Li cell was found to short after 5 *min* under an applied current $i_0 = 5\ mA/cm^2$,[46] whereas we obtained a time of ~ 25 *min* when our ideal model (no pre-cracks at the anode/SE interface, as created in the experiment) is applied with the parameters used in Swamy et al.[46] (SE porosity of ~3% and fracture toughness of 0.6 $MPa\cdot\sqrt{m}$). Models incorporating GBs could be built to investigate the case of polycrystalline materials (such as LLZO).

An important finding in our work is the relation between the size of a pore and the current density above which it becomes susceptible to fracture by *M* filling, as shown, for example, in Figure 4A. While small voids may fill with metal, they may not build up enough pressure to crack and hence will not contribute to shorting of the cell. But the size above which voids become critical and fracture decreases as the current density increases (Figure 6A). This implies that, at higher current density, more of the pores can contribute to the creation of a metal-percolating path that shorts the cell. Through this mechanism porosity and CCD are intricately related.

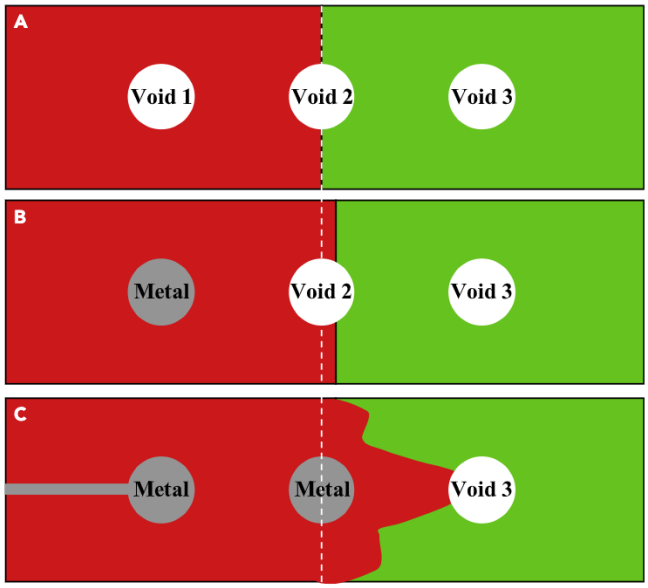

Figure 5. Scheme of successive cracking events caused by void filling

In each stage the part of the SE that is susceptible to plating is shown in red, and the "safe" part is shown in green. Li is stripped on the right side of the cell and deposited on the left side. (A) Initial potential distribution with no metal in any voids, (B) void 1 is filled by *M* metal, and (C) void 1 is cracked and connected to the anode and void 2 is filled by *M* metal. The vertical dashed line is located at the middle of the cell.

Although we have focused on the pores nearest to the anode, it is clear how failure can propagate further into the SE. Once a pore cracks toward the anode the crack will further fill with metal and adopt the anode electrical potential, thereby extending the region where the metal plating potential is negative further into the SE. Figure 5 illustrates this possible evolution of the plating front in an *M* symmetric cell. Initially, half of the SE volume is susceptible to metal deposition (red area in Figure 5A). When void 1 fills and cracks, the crack that extends toward the anode will fill and connect the void to the anode potential. This moves the front for potential metal deposition further toward the other electrode (Figure 5C) making void 3 now susceptible to plating. Such successive fracture events between disconnected pores can bridge connected porosity and ultimately penetrate the SE.

The key issue to prevent Li metal propagation through the electrolyte is to prohibit initiation of metal plating in the vulnerable region near the anode, as illustrated schematically in Figure 6. The fraction of the SE that sees a negative plating potential (a_0/L) is approximately the ratio of the anode surface overpotential (η_A) and the cell voltage $V_C - V_A$ (Equation 2). This area increases with current density because η_A increases, as can be seen from the linearized Butler-Volmer equation ($\eta_A \approx i_0 R_A$). One should note that the relevant current density is the local current density, which may be very different from the average current density due to inhomogeneous contact at the interface.[14] From this analysis, three strategies to reduce Li plating in the SE become apparent: (1) create a dense layer between the metal anode and porous SE either by introducing a coating between the anode and SE or by densification to obtain a thin "void-free" layer near the SE surface; (2) decrease the *M* chemical potential in the anode (raise its voltage); and (3) improve contact between the anode and the SE to reduce the local current density, as a lower current density reduces the depth of the SE that is susceptible to plating. The first two solutions are schematically shown in Figures 6B and 6C.

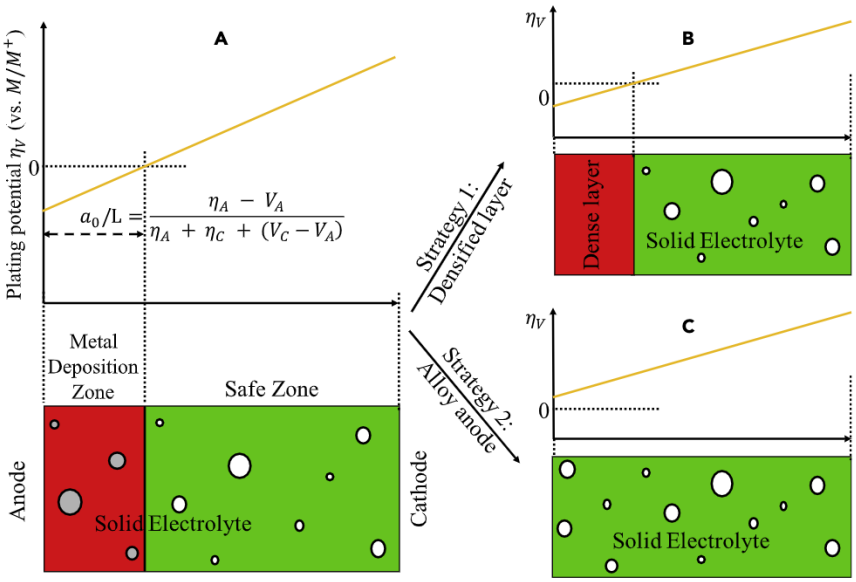

Figure 6. Strategies to prevent metal deposition inside the SE

(A) Schematic illustration of the metal deposition in voids of the SE. Deposition happens in the region of negative plating potential ($[0, a_0]$, red area). This region (a_0/L) is affected by the Butler-Volmer overpotentials at the anode/SE (η_A) and cathode/SE (η_C) interfaces, and the equilibrium voltage in the anode (V_A) and cathode (V_C), respectively. Two strategies to reduce Li plating in the SE: (B) create a dense layer between the metal anode and porous SE, and (C) increase the equilibrium voltage in the anode above the Butler-Volmer overpotentials at the anode/SE interface ($V_A > \eta_A$).

We investigated in more detail the first two strategies with the models and parameters used in the previous section. If the buffer or densified layer accommodates the full region where the plating potential is negative no Li plating will occur in the SE as it is never exposed to any Li plating conditions. Note that, in a symmetric cell, the vulnerable region for plating is half the thickness of the SE (Figure 1A) making the use of an interfacial buffer layer impractical. But we show in Figure 7A that even in this case the negative effects of plating can be mitigated. A metal symmetric cell with a void (0.5μm in diameter) near the anode is modeled in Figure 7A under a fixed areal capacity of $C_A = 4\ mAh/cm^2$. The "void-free thickness" of the SE in the x axis is defined as the void distance to the anode minus the void radius, as shown in the inset figure. When the void-free thickness is 0.5 μm, the SE will be fractured if the applied current density is larger than 1.6 mA/cm^2 (a similar conclusion can be found in Figure 4A when the void diameter is 0.5 μm). However, when the void-free thickness increases to $2 \sim 3\ \mu m$, the void will stay in stage I ("void not full" in Figure 7A) during the whole charging process. Therefore, creating a thin void-free layer at the anode/SE interface is an efficient way to alleviate metal propagation in the void.

Densifying the SE surface not only decreases the metal deposition in the SE but also decreases the "shadow effect": voids positioned deeper in the SE cause less current inhomogeneities at the anode/SE interface (Figure 2D). Although synthesizing an ideal dense SE layer may be difficult and impractical, a very low SE porosity with small voids also works (Figure 4A), either by using smaller SE particles[15] or applying high-pressure hold pressing.[43] It has been shown experimentally in Cheng et al.[15] that an SE heterostructure (with smaller SE particles at the surface layer and larger SE particles in the middle layer) not only exhibits much lower interfacial resistance (owing to better anode/SE interfacial contact) but also higher CCD (because of

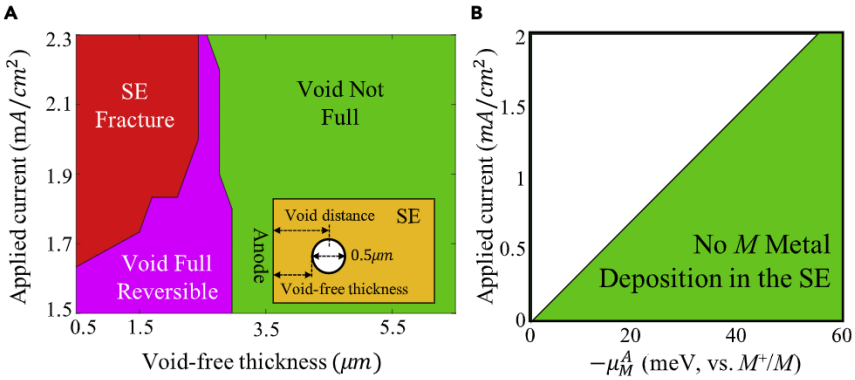

Figure 7. Example of the two strategies for preventing metal deposition in a real SSB cell

(A) Evolution of voids as a function of the void-free thickness and applied currents with an area capacity of 4 mAh/cm^2. The three regions have the same meaning as in Figure 4A. The inset describes the void geometry.

(B) Safe operating zone as a function of the *M* chemical potential in the anode μ_M^A and the applied current. The "No *M* metal deposition in the SE" means no deposition regardless of the position of the voids in the SE.

the denser SE surface). Notably, it is not necessary to densify the entire sample; a thin layer is sufficient to achieve similar improved performance in terms of Li dendrite resistance.

Using a coating or buffer layer between electrodes and the SE is widely used to achieve better chemical stability to prevent the formation of uncontrollable SE interphase[5,25] or to reduce interfacial contact loss.[47] Although these objectives are important in preventing cell degradation, our study points out that the improved cell performance after adding the coating/buffer layer might partially stem from the void-free layer contacting the SE surface (Figure 5A).

Tuning the *M* chemical potential in the anode is shown to be a good strategy to prevent/alleviate metal propagation in the SE (Figures 4C and 4D). Figure 7B shows the requirements for the anode *M* chemical potential to completely prevent *M* metal propagation in the SE as a function of applied current. As long as the *M* chemical potential in the selected anode material is in the green region, no deposition will occur in the voids regardless of the positions of the voids. *M* metal alloying is a good strategy to control the *M* chemical potential in the anode and has been widely studied in the literature.[39,40] Both the Li-Mg alloy anode and the Ag-C composite anode have shown to lead to great cell performance with high specific and areal capacity. Although an alloy anode may provide better interfacial contact and chemical stability at the anode/SE interface, which results in better cell performance, the lower chemical potential in the alloy anode is also beneficial for preventing metal deposition in the SE. Our findings in this context also indicate that symmetric cells may not be representative of full-cell dynamics in terms of *M* metal deposition in voids (or CCD) as they present the worst conditions for *M* metal deposition in the SE. Conversely, our work also shows that solid-state batteries with a non-metal anode, such as Si or graphite, will not suffer from *M* plating in the SE and hence their impressive cycling results cannot be extrapolated to metal anode SSBs.[48]

It should be noted that in our work we only focused only on electronic conductivity-driven metal propagation (metal deposition in the SE), and metal may penetrate an SE for a variety of reasons.[49,50] Hence, our results provide an upper limit for

experimental observations. In addition, the SE fracture model used in this work is based on classical fracture mechanics with the assumption of viscoelasticity for the *M* metal in the voids. More advanced fracture models for *M* metal insertion in a confined space[51,52] can be incorporated for a more accurate evaluation of the critical pressure allowed in the SE, the maximum pressure developed in the *M* metal, and the time needed to fracture the SE. One should also consider that the electronic conductivity in the SE may be enhanced locally during cycling by the generation of vacancies or by chemical reactivity of the electrolyte.[53,54] Any increase of electronic conductivity near the anode will increase the *M* metal deposition rate in the SE (Figure 4B). Our modeling was performed with a spherical void geometry. However, the void morphology in a real SE material can be much more complicated in terms of pore connectivity and tortuosity. Because the spherical voids used in this work have the lowest curvature of all shapes with the same volume, the results obtained should cause the smallest inhomogeneity of potentials and deposition current. Therefore, the *M* metal deposition rate in a real SE material with more complicated pore structure is likely to be higher than the results predicted.

Conclusion

The existence of electronic conductivity in SEs is believed to be a key reason for metal penetration in SSB cells. In this work, we developed a computational framework that integrates electronic and ionic transport, Li deposition, and mechanical events. Our model indicates that a small electronic conductivity is indeed sufficient to trigger metal propagation in the SE whenever porosity is present near the anode. Large pores are particularly problematic as they can build up enough pressure to crack the SE when they become completely filled. In contrast, small porosity may fill and empty in a reversible manner. We find that symmetric cells may overestimate the growth of metal through the SE as half the SE is exposed to plating conditions. In full cells the part of SE in which plating conditions are favorable is initially confined to a small region near the anode. Fracturing in this region may, however, extend the plating-susceptible region further into the SE and eventually lead to metal penetration in the SE and cell shorting. Our work also establishes a relation between CCD, microstructure features, fracture toughness, and the intrinsic electronic and ionic conductivity of the SE. Creating a densified layer on the SE near the anode, or alloying the metal anode, are proposed as two strategies to prevent/alleviate the metal deposition in the SE.

EXPERIMENTAL PROCEDURES

Resource availability

Lead contact

Further information and requests for resources and reagents should be directed to and will be fulfilled by the lead contact, Gerbrand Ceder (gceder@berkeley.edu).

Materials availability

This study did not generate new unique reagents.

Data and code availability

All data and code associated with the study have not been deposited in a public repository but are available from the lead contact upon reasonable request.

Modeling of the MIEC

Figure 8 illustrates the setup of the model. A MIEC SE with a void (shown as the white area) is contained between two electrodes. As we focus here on possible metal plating and cracking around the void, we assume flat interfaces and perfect contact

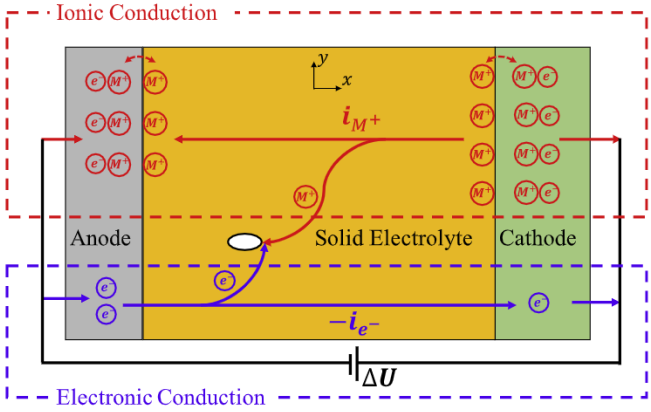

Figure 8. Schematic illustration of the MIEC model for an SSB cell during charging

The movements of cations and electrons can be described by an equivalent circuit that has ionic conduction and electronic conduction connected in parallel under the same externally applied potential ΔU. The top part (in the red box) represents the ionic conduction, where cations M^+ are removed from the cathode, migrate across the SE, and plate onto the anode. The bottom part (in the blue box) represents electronic conduction, which lets electrons flow from the anode to the cathode. Metal deposition occurs in the void (white area).

with the electrodes. The effect of surface roughness has been studied in our previous work and can mainly be considered as a local increase in current density.[14,51]

During the charging process shown in Figure 8, M^+ ions migrate from the cathode to the anode with partial current density i_{M^+} (red lines); meanwhile, electrons move from the anode to the cathode with partial current density i_{e^-} (blue lines, the direction of i_{e^-} is opposite to the flux direction of electrons). The partial current densities i_{M^+} and i_{e^-} are vectors, and related at the SE interfaces through the following boundary conditions:

$$(i_{M^+} + i_{e^-}) \cdot n^C = -i_0 S_0, \quad \text{at SE/cathode interface,} \qquad \text{(Equation 4)}$$

$$(i_{M^+} + i_{e^-}) \cdot n^A = -i_0 S_0, \quad \text{at SE/anode interface,} \qquad \text{(Equation 5)}$$

$$(i_{M^+} + i_{e^-}) \cdot n^V = 0, \quad \text{at SE/void interface.} \qquad \text{(Equation 6)}$$

The externally applied current density (i_0) is a constant scalar under galvanostatic conditions. The surface area of the SE (S_0) at both the anode and cathode side, and their outward unit normal vectors ($n^A = [-1, 0, 0]^T$ and $n^C = [1, 0, 0]^T$) are constant because flat surfaces are assumed. Note that i_{M^+} i_{e^-} are treated as vectors. Equations 4 and 5 show that a total current $i_0 S_0$ flows into the SE from the cathode/SE interface, and flows out of the SE into the anode/SE interface. Equation 6 states that no net charge accumulation occurs in the void: the magnitude of the ion flux ($i_{M^+} \cdot n$) should be the same as the magnitude of the electronic flux ($-i_{e^-} \cdot n$).

For an SE in which the mobile M^+ has a charge of +1 (such as Li^+ and Na^+), transport of cations and electrons can be described by the Ohmic relations:

$$i_{M^+} = -\frac{\sigma_{M^+}}{F} \nabla \tilde{\mu}_{M^+}, \quad i_{e^-} = \frac{\sigma_{e^-}}{F} \nabla \tilde{\mu}_{e^-}. \qquad \text{(Equation 7)}$$

The partial current densities (i_{M^+}, i_{e^-}) are driven by their respective electrochemical potentials in the SE ($\tilde{\mu}_{M^+}$ for M^+ and $\tilde{\mu}_{e^-}$ for electrons). We assume no cross-coupling between ionic (electronic) current and electronic (ionic) electrochemical potentials.[55] Transport equations are solved under steady-state condition, and, apart

from the void, no accumulation of carriers occurs in the SE,[56] so that Laplacian equations can be applied:

$$\nabla^2\tilde{\mu}_{M^+} = 0, \quad \nabla^2\tilde{\mu}_{e^-} = 0. \qquad \text{(Equation 8)}$$

All charge-transfer reactions (stripping at the cathode side, plating at the anode side, metal deposition in the void) are described by the Butler-Volmer relation:

$$i_k = i_{exc}^k\left(e^{\frac{\alpha_a F\eta_k}{RT}} - e^{-\frac{\alpha_c F\eta_k}{RT}}\right). \qquad \text{(Equation 9)}$$

The charge-transfer current density across the interfaces (i_k, $k = A$ for the anode/SE interface and $k = C$ for the cathode/SE interface) is defined as positive for an anodic reaction. The exchange current density i_{exc}^k represents the reaction rate of the M/M^+ reactions. The anodic and cathodic coefficients (α_a, α_c) satisfy the relation $\alpha_a + \alpha_c = 1$; R, T, and F are the gas constant, temperature, and Faraday constant, respectively. The surface overpotential η_k is the difference between the M chemical potential in the electrode (μ_M^k, $k = A$ for the anode and $k = C$ for the cathode) and the electrochemical potential ($\tilde{\mu}_{M^+} + \tilde{\mu}_{e^-}$) at the SE/electrodes interfaces: $F\eta_k = \mu_M^k - (\tilde{\mu}_{M^+} + \tilde{\mu}_{e^-})$.[28,57,58]

Equation 9 describes the surface overpotential (η_k) for an M^+ ion to move from the electrode to the SE (anodic reaction) or from the SE to the electrode (cathodic reaction). All potentials can be related through the following equation:

$$-F\Delta U = \tilde{\mu}_{e^-}^A - \tilde{\mu}_{e^-}^C = \left(\tilde{\mu}_{M^+}^{SE,C} - \tilde{\mu}_{M^+}^{SE,A}\right) + (F\eta_C - F\eta_A) + \left(\mu_M^A - \mu_M^C\right). \qquad \text{(Equation 10)}$$

The first equality ($-F\Delta U = \tilde{\mu}_{e^-}^A - \tilde{\mu}_{e^-}^C$) is the definition of the externally measured potential (ΔU). This potential is also the driving force for electronic current across the SE when there is non-negligible electronic conductivity. The first two terms on the right-hand side of Equation 10 constitute the overpotentials needed: $\tilde{\mu}_{M^+}^{SE,C} - \tilde{\mu}_{M^+}^{SE,A}$ is the driving force to move M^+ across the SE, and $F\eta_C - F\eta_A$ is the contribution of the surface overpotentials at the electrode/SE interfaces. Added to these is the term $\mu_M^A - \mu_M^C$, which is the thermodynamic open-circuit voltage (Nernst equation: $-F\Delta U^{OCV} = \mu_M^A - \mu_M^C$).

Two conventions are used in this work: (1) the anode voltage is always zero: $\tilde{\mu}_{e^-}^A = 0$ (therefore, $F\Delta U = \tilde{\mu}_{e^-}^C$ in Equations 10), and (2) the chemical potential of M in M metal (μ_M^M) is zero, meaning the other (electro)chemical potentials are set with respect to μ_M^M. Therefore, for a symmetric cell with M metal as the electrode, the chemical potential of M in the electrode (μ_M^A, μ_M^C) is zero: $\mu_M^A = \mu_M^C = 0$. Notably, the effect of mechanical stress on the charge-transfer kinetics at the electrode/SE interfaces is neglected in our treatment, consistent with the small value of "stack pressure" that is typically applied in experiments (<10 *MPa*).[14] The possibility of SE fracture is included when metal deposits inside the void because large stress can build up when metal is deposited in a confined space. No space-charge layer is assumed in this work due to its negligible effect in SSBs.[56,59] The nucleation energy of M metal is also neglected as in similar work.[28,60]

With both M^+ ions and electrons available inside the SE, metallic M can deposit in the void when the potential at the location of the void is in the appropriate range. Because we have set the equilibrium potential for the M anode equal to zero, the plating potential is equal to the overpotential for Li plating. Figure 9 presents a schematic illustration of the deposition process. Before cycling, no metal is present in the void. Equation 9 indicates that M metal deposition (cathodic reaction: $M^+ + e^- \rightarrow M$) in a

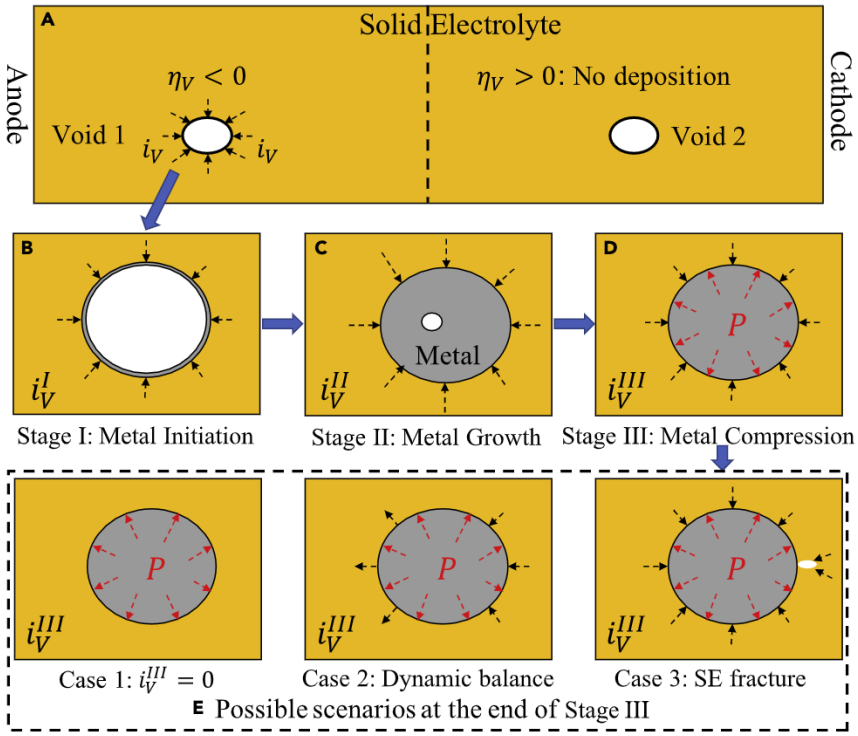

Figure 9. Schematic illustration of different stages of metal deposition in the void

(A) Voids close to the cathode side (void 2) have positive plating potential (η_V>0), and no deposition occurs. Voids close to the anode side (void 1) have negative plating potential (η_V<0), and metal will be deposited.

(B) Stage I (metal initiation) of the metal deposition at a rate of i_V^I. The gray color at the surface of void 1 represents a thin layer of *M* metal.

(C) Stage II (metal growth) with a deposition rate of i_V^{II}. Most of the space of the void is occupied by *M* metal.

(D) Stage III (metal compression) with a deposition rate of i_V^{III}. A hydrostatic pressure (*P*) is built up to counterbalance the metal insertion.

(E) The three possible scenarios at the end of the metal compression stage. Case 1: zero deposition rate at the metal/SE interface. Case 2: equal amount of deposited *M* metal and dissolved *M* metal, leading to zero net *M* metal insertion. Case 3: SE fracture due to high pressure.

void only occurs when the plating potential (η_V, where "*V*" stands for void) at the location of the void is negative. During charging, the plating potential increases from negative near the anode side (void 1 in Figure 9A) to positive near the cathode (void 2). When initiated, metal deposition will start with a thin layer of *M* metal plating on the surface of void 1 under deposition rate i_V^I (Figure 9B). We refer to this as "stage I: metal initiation." After this stage, the void is gradually filled by *M* metal under deposition rate i_V^{II} (Figure 9C), which we refer to as "stage II: metal growth." When the void is fully filled with metal, a hydrostatic pressure (*P*) will build up as new *M* metal continues to insert into the confined space. This pressure in turn reduces the plating potential and decreases the deposition rate i_V^{III} (Figure 9D). This is "stage III" and involves metal compression. The metal compression stage can end in three different ways depending on the deposition rate (i_V^{III}), the pressure (*P*) developed, and the strength of the SE material (Figure 9E). We define case 1 as when the pressure is high enough to completely suppress *M* metal deposition at any location in the void before SE fracture occurs. In case 2, the pressure in the void modifies the plating potential η_V, leading to plating of half of the metal/SE interface (η_V<0) while stripping of the other half (η_V>0). The total amount of *M* metal inserted is zero because the deposition on one

side of the void is balanced by the stripping on the other side. In this scenario, observed experimentally,[20] the void participates in metal transport through the conductor. Case 3 occurs when the pressure (P) becomes large enough to fracture the SE. Cases 1 and 2 are reversible, whereas case 3 is not. If, at the end of the cell charging, a void near the anode is not completely filled (stages I or II), or completely filled (stage III-case 1 or -case 2), M metal in the void will gradually dissolve when the cell discharges. However, if the SE fracture occurs (stage III-case 3), deposition current will concentrate near the fractured area due to the larger curvature, leading to further fracture of the SE and propagation of M metal. [51] Notably, cases 1 and 2 can also become irreversible if the M metal is chemically reactive with the SE material. Part of the deposited metal may then react with the SE during plating and less metal will dissolve when the cell discharges. This complication is currently not included.

The various conditions under which metal deposition occurs in the SE can be described by the following modified linear Butler-Volmer relation

$$i_V = \begin{cases} 0, & \text{if } \eta_V>0 \quad \textit{No deposition} \\ i^V_{exc}\dfrac{F\eta_V}{RT}, & \text{if } \eta_V<0 \quad \textit{Stage I \& II} \\ i^V_{exc}\dfrac{\left(F\eta_V - P\overline{V}_M\right)}{RT} & \text{if } P>0 \quad \textit{Stage III} \end{cases}. \qquad \text{(Equation 11)}$$

In Equation 11, $\overline{V}_M$ and i^V_{exc} are the molar volume of M and the exchange current density, respectively. From Equation 9 the plating potential η_V is: $F\eta_V = \mu^V_M - \tilde{\mu}^{SE}_{e^-} - \tilde{\mu}^{SE}_{M^+}$, where μ^V_M is the chemical potential in the M metal ($\mu^V_M = 0$). The electrochemical potentials of M^+ and e^- in the SE ($\tilde{\mu}^{SE}_{M^+}$ and $\tilde{\mu}^{SE}_{e^-}$) can be obtained by solving Equations 4–8. The exchange current density i^V_{exc} at the void/SE interface is much smaller than that at the electrodes/SE interface since the charge-transfer reaction in the void is limited by the electron transport in the SE due to the low electronic conductivity.[17] As a result, the deposition current (i_V) and the plating potential (η_V) can be obtained from the linearized Butler-Volmer relation in stages I and II, because $\eta_V \ll \frac{RT}{F}$. The deposition currents in stages I and II (i^I_V, i^{II}_V) can be very different because M^+ ions are plated at the "interface" of the SE and void during stage I but at the interface of the SE and M metal during stage II.

The effect of pressure P on the deposition current (i_V) is described by adding the $P\overline{V}_M$ term to the Butler-Volmer relation in Equation 11, III.[28,57,61] It is possible to calculate the pressure P in the void as a function of time (t) once the void is filled. The result has the expected decaying exponent form (for details see the supplemental information, section 1):

$$P = \frac{\oint_{\partial V}\left(F\eta^0_V\right)\,dS}{\overline{V}_M \cdot S}\left(1 - e^{-c_1 t}\right). \qquad \text{(Equation 12)}$$

Here, the constant $c_1 = \frac{K\overline{V}_M^{\,2}}{RTF}\frac{S}{V}i^V_{exc}$, the volume ($V$), and surface ($S$) of the M metal are the same as the void during stage III. The bulk modulus of the M metal (K) is assumed to be constant (e.g., $K_{Li} = 11GPa$).[62] The initial plating potential (η^0_V) is the value at the end of stage II (M metal completely fills in the void but no pressure is present).[51,52] When the terminal pressure P_T is greater than the critical pressure, $P_T \geq P_c = \frac{K_c}{f(d_V,a)\sqrt{\pi a}}$ [63], fracture of the SE will occur. K_c is the fracture toughness of the SE and $f(d_V, a)$ is a geometric factor (with d_V the void diameter and a the crack length).[51,64]

Analytical solutions for the 1D case are derived in the supplemental information, section 2. An in-house developed code based on the finite element method and the MOOSE framework[65] is implemented to solve all coupled PDEs numerically for 2D/3D cases. The parameters used in this work are obtained from experimental measurements of LPS-type SE, as shown in Table 1. For key parameters with different reported measurements, the values that lead to the largest metal deposition inside the SE and the easiest SE fracture are selected so as to get the most limiting conditions for stability against plating (for example, the highest electronic conductivity is selected from the range $(10^{-6} \sim 10^{-4})\ mS/cm$ [16,32,33], and the lowest fracture toughness is selected from the range $(0.2 \sim 0.23)\ MPa\cdot\sqrt{m}$).[35–37] The effects of these variations on the internal metal deposition are discussed separately in the results section. A complete list of all parameters and variables is provided in Table S1 in the supplemental information.

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.matt.2021.08.004.

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AUTHOR CONTRIBUTIONS

Q.T. planned the project with G.C. Q.T. derived all equations, programmed all codes, and calculated all data with the help of S.C. and T.S. The manuscript was written by Q.T. and was revised by S.C., T.S., and G.C. with the help of the other authors. All authors contributed to discussions.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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