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July 1968

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ABSTRACT

This paper presents a comprehensive description of the design and operation of a wide-band direct-coupled pulse amplifier, with a voltage gain of 10 and a risetime of 1 nsec. Computer-aided analysis and simulation are used to optimize the design and to predict the performance of the amplifier. Good agreement is obtained between the predicted and experimental results.

In an attempt to improve the frequency response through the elimination of parasitic capacitive and inductive effects, the amplifier has been fabricated as a Hybrid I.C.<sup>†</sup> by use of thin-film resistors and silicon chip transistors mounted on a ceramic substrate.

I. INTRODUCTION

In many high energy nuclear physics experiments, there is need for relatively low-gain wide-band pulse amplifiers to be used in conjunction with photomultiplier tubes and scintillation counters. With very high counting rates ( $10^8$  pps), the shift of the baseline must be minimized. Also in many experiments in which only one event of many is of interest, the amplifier must not introduce dead time due to pulse stretching, or generate multiple pulses at the output when overloaded. These considerations led to the design of a direct-coupled discrete-component amplifier with a voltage gain of 10 and a risetime of approximately 1 nanosecond.<sup>[1]</sup>

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<sup>†</sup> Hybrid integrated circuit

Though transistors with a high gain-bandwidth product ( $f_t$ ) were used (the 2N4958 and 2N2857 have a minimum  $f_t$  of 1 GHz), it seemed reasonable to believe that the high frequency performance may be limited by parasitic inductance and capacitance. Even the small amount of stray capacitance associated with ordinary carbon resistors may limit the high frequency performance. In an attempt to improve the frequency response through the elimination of these parasitic effects, the amplifier has been fabricated as a Hybrid I.C., using thin-film Nichrome resistors and silicon chip transistors mounted on a ceramic substrate.

## II. CIRCUIT DESCRIPTION

The amplifier circuit diagram is shown in Fig. 1. In the quiescent condition,  $Q_1$  and  $Q_2$  are conducting approximately 5 mA and have a collector-to-emitter voltage of 7.5 volts. These steady-state conditions were chosen for two reasons. First, the gain-bandwidth products ( $f_t$ ) of the transistors were found to be the greatest for collector currents in the range 5 to 15 mA. Thus, since the amplifier is designed for negative input pulses which increase the current in both transistors, the steady-state collector current was chosen to be at the lower limit of this range. Secondly, it is desirable the  $Q_2$  operate as nearly as possible in the common-emitter configuration, in order to maximize its voltage gain. Thus the zener diode was chosen for a low breakdown resistance while at the same time maintaining a reasonable collector-to-emitter voltage.

With the application of a negative input signal, the current in  $Q_1$  and  $Q_2$  increases. When the current in  $Q_2$  exceeds approximately 25 mA, the zener diode  $D_2$  comes out of reverse breakdown and exhibits a large impedance, reducing the gain of  $Q_2$  substantially. In this way the output current is limited to approximately 20 mA, or 1 V into a 50- $\Omega$  load.

The feedback network consists of the feedback resistor  $R_F$ , the trimming capacitor  $C_E$ , and the series combination of the diode  $D_1$  and the resistor  $R_{E1}$ . Without the diode  $D_1$ , the amplifier output baseline would have a large negative temperature coefficient, due primarily to the temperature dependence of the base emitter junction of  $Q_1$ . Inclusion of  $D_1$  is an attempt to perform some temperature compensation. The resistor  $R_{E1}$  is added to the forward resistance of the diode  $D_1$  to adjust the midband gain.

### III. CIRCUIT ANALYSIS

The basic feedback amplifier equation [2] is given by

$$A_v = \left( \frac{a_v}{1 + a_v f_v} \right),$$

where  $a_v$  is the open-loop voltage gain,  $f_v$  is the feedback transfer function, and  $A_v$  is the closed-loop voltage gain of the amplifier.

If, for a first-order analysis, each transistor is represented by its single capacitor hybrid  $\pi$  model, the open-loop amplifier can be modeled as shown in Fig. 2. [3] With this circuit model, the open-loop voltage gain can be represented by a two-pole transfer function of the form

$$a_v = \frac{a_{vo}}{\left(1 + \frac{p}{p_1}\right)\left(1 + \frac{p}{p_2}\right)},$$

where  $p_1 = \left( \frac{1}{R_{\pi 01} C_{\pi 1}} \right)$ ,  $p_2 = \left( \frac{1}{R_{\pi 02} C_{\pi 2}} \right)$ , and  $a_{vo}$  is the midband

voltage gain.  $R_{\pi 01}$  and  $R_{\pi 02}$  are the driving point impedances associated with  $C_{\pi 1}$  and  $C_{\pi 2}$  respectively. [4]

The voltage-ratio feedback signal is most easily provided by a voltage divider network, where the feedback function is

$$f_v = \frac{R_E}{R_E + R_F}$$

Then the closed-loop gain is given by

$$A_v = \frac{a_{vo}}{\left(1 + \frac{p}{p_1}\right)\left(1 + \frac{p}{p_2}\right) + \frac{a_{vo} R_E}{R_E + R_F}} = \frac{a_{vo}'}{\left(1 + \frac{p}{p_1'}\right)\left(1 + \frac{p}{p_2'}\right)}$$

In terms of the root locus diagram in Fig. 3, the application of feedback has caused the two open-loop poles to first move together, and then to split into the complex frequency plane. [5]

Consider, now, the feedback network of  $R_E$ ,  $C_E$ , and  $R_F$  used in the amplifier of Fig. 1. The capacitor  $C_E$  provides broadbanding. With this feedback network,

$$f_v = \frac{Z_E}{Z_E + R_F} = \frac{\left( \frac{R_E}{1 + p C_E R_E} \right)}{\left( \frac{R_E}{1 + p C_E R_E} \right) + R_F} = \frac{\frac{R_E}{R_E + R_F}}{\left( 1 + p C_E \frac{R_E R_F}{R_E + R_F} \right)} ;$$



$$\text{now } A_{vo} = \frac{a_{vo} \left(1 + \frac{p}{z_E}\right)}{\left(1 + \frac{p}{p_1}\right)\left(1 + \frac{p}{p_2}\right)\left(1 + \frac{p}{p_E}\right) + \frac{a_{vo} R_E}{R_E + R_F}} = \frac{a_{vo}' \left(1 + \frac{p}{z_E}\right)}{\left(1 + \frac{p}{p_1}\right)\left(1 + \frac{p}{p_2}\right)\left(1 + \frac{p}{p_E}\right)},$$

where

$$z_E = p_E = \left( \frac{1}{C_E [R_E || R_F]} \right).$$

To predict the effects of  $C_E$  on the frequency response, the relative position of the poles and zero in the complex frequency plane must be determined. This is done in the next section with the help of computer-aided analysis.

#### IV. COMPUTER ANALYSIS

The response of the amplifier of Fig. 1 was predicted through the use of Calahan's Linear Network Analysis Program. [6] The amplifier was represented by the idealized circuit model of Fig. 4. This circuit model is idealized in the sense that the only parasitic charge storage elements included are those due to the transistors and diodes. The remaining circuit elements are assumed to be free of parasitics. The actual case, which takes into account (a) the parasitics due to the nonideal circuit elements, and (b) the stray capacitance and inductance due to the physical circuit layout, is considered later.

With the steady-state operating conditions of  $I_{C1} = I_{C2} = 5 \text{ mA}$  and  $V_{CE1} = V_{CE2} = 7.5 \text{ V}$ , the following small-signal transistor circuit model parameters were determined:

$$g_{m1} = g_{m2} = \frac{qI_C}{kT} = 0.192 \text{ mho},$$

$$\beta_{01} = 40, \quad \beta_{02} = 90,$$

$$r_{\pi 1} = \frac{\beta_{01}}{g_{m1}} = 208 \text{ } \Omega, \quad r_{\pi 2} = \frac{\beta_{02}}{g_{m2}} = 470 \text{ } \Omega,$$

$$f_{t1} = f_{t2} = 1.4 \text{ GHz},$$

$$C_{\mu 1} = 0.7 \text{ pF}, \quad C_{\mu 2} = 1.0 \text{ pF},$$

$$C_{\pi 1} \approx C_{\mu 2} = \frac{g_m}{\omega_t} - C_{\mu} \approx 21 \text{ pF},$$

$$r_{x1} = r_{x2} = 50 \text{ } \Omega.$$

The zener diode is modeled by a parallel RC circuit with the element values,

$$R_{D2} = 6 \text{ } \Omega,$$

$$C_{D2} = 500 \text{ pF}.$$

The series combination of the forward-biased diode,  $D_1$ , and resistor,  $R_1$ , is modeled by a pure resistance,  $R_{D1} = 25 \text{ } \Omega$ . The diffusion capacitance of the diode can be neglected, since it is effectively in shunt with the variable trimming capacitance,  $C_E$ . The 4-K $\Omega$  collector resistance,  $R_{C2}$ , is neglected, since it is

effectively in shunt with the much smaller 50- $\Omega$  load resistance,  $R_L$ . Similarly, the emitter resistance,  $R_{E2}$ , and the bias resistor can be neglected, since for ac considerations, they are both in shunt with much smaller resistors. The input of the amplifier is terminated in a 50- $\Omega$  resistance,  $R_{B1}$ , and is driven from a 50- $\Omega$  source. The effective source resistance, then, is seen to be  $R_S = 25 \Omega$ .

With the circuit model of Fig. 4, the poles and zeros were computed for different values of  $C_E$ . The dominant poles and zeros for the upper band edge are plotted in Fig. 5. These poles and zeros correspond to  $p_1'$ ,  $p_2'$ ,  $p_E'$ , and  $z_E$  of the previous discussion. The variation of the poles with  $C_E$  is not easily determined analytically, since it requires the solution of a cubic equation. With computer-aided analysis, however, the positions of the poles for different values of  $C_E$  are easily found, and their locus can be plotted. The results of the analysis, shown in Fig. 5, show the pole  $p_E'$  and zero  $z_E$  to be very close together for all values of  $C_E$  in the range of interest. Hence what occurs is an approximate pole-zero cancellation and thus the effect of this pole-zero pair on the frequency response is almost negligible. The more important effect, however, is the motion of the other two poles,  $p_1'$  and  $p_2'$ , with varying  $C_E$  and a constant midband loop gain. In Fig. 5 it is seen that for increasing  $C_E$ , the poles  $p_1'$  and  $p_2'$  first split into the complex frequency plane, and become increasingly more complex, with their real parts remaining approximately constant. After they reach approximately 45-deg. radials, the locus bends and the poles move towards the  $j\omega$  axis with approximately constant imaginary parts. In terms of this locus, the broadbanding effect is easily seen due to the increasing radial angle of the two poles,  $p_1'$  and  $p_2'$ .

Computer plots were also obtained for the output response to specified input voltage waveforms. The plot of Fig. 6a shows the output transient response predicted for an ideal step-function input. The desired output waveform is that with 10% overshoot, the case with  $C_E = 30$  pF, on which the risetime is measured and found to be

1.1 nsec. All risetimes are measured from the 10% to 90% points on the leading edge of the pulse.

The fastest pulse generator available had a risetime of 0.75 nsec with an overshoot of less than 5%, as measured on a Tektronix Model 661 sampling oscilloscope. Fig. 6b shows the output voltage waveform predicted for an input pulse with a risetime of 0.75 nsec. With an output overshoot of 10%, the risetime is seen to be 1.25 nsec.

#### V. HYBRID I.C. AMPLIFIER

Several factors limit the frequency response of an amplifier, the most important being the gain-bandwidth product,  $f_t$ , of the transistors. The frequency limitations of the transistors, however, are inherent in their design, and hence cannot be readily improved upon. Two factors, in particular, that may restrict the frequency response of a wide-band pulse amplifier are

- (a) The components used are not ideal and may have a certain amount of parasitic inductance and capacitance associated with them.
- (b) Component lead lengths and the overall physical layout may introduce parasitic inductance and capacitance into the circuit.

From Fig. 1 it can be seen that, except for the trimming capacitor,  $C_E$ , the circuit components are all resistors. Thus, the fabrication of resistors which are purely resistive becomes a topic of prime concern. Then, lead inductance can be reduced by fabricating the circuit as small as possible to minimize the lead lengths.

## VI. FABRICATION

The Hybrid I.C. amplifier, shown in Fig. 7, was constructed on a small disc of alumina, 200 mils in diameter and 25 mils thick. The construction consisted basically of depositing a layer of Nichrome V onto the surface of the ceramic, using standard vacuum deposition techniques. Then, by use of photo-lithographic techniques, part of the Nichrome was chemically etched to leave the desired resistor pattern in Nichrome, on the surface of the ceramic. Aluminum was next deposited on the surface; and, again by use of photo-lithographic methods, the aluminum was etched to leave the desired interconnections between resistors. Finally, the ceramic disc was fastened to the header, and the diode and transistor chips were fastened to the ceramic with a conducting cement. After the cement was cured, the necessary connections to the transistors, diodes, and the header were made with 0.7-mil-diameter gold wire.

The Nichrome resistors exhibited parasitic capacitance effects similar to those found in carbon resistors. The optimum resistivity, at which point the resistors appeared to be purely resistive, was found experimentally to be approximately 50  $\Omega$ /square. This, then, became the main constraint governing the layout of the Hybrid amplifier, shown in Fig. 7. The location of the various resistors and their measured values is shown in Fig. 7. Finally, Fig. 8 shows the actual circuit diagram with the measured resistor and parasitic values indicated.

## VII. RESULTS

The Nichrome resistors used in the Hybrid I.C. amplifier exhibited very small parasitic capacitances, as shown in Fig. 8. The 0.4-pF capacitance shown at the input and output is due to the pin capacitance of the header.

For computer analysis, the Hybrid I.C. amplifier was represented by the circuit model of Fig. 9. The element values are the same as those of Fig. 4 (the idealized circuit model) except for deviations due to the actual resistance and capacitance values of the Nichrome resistors, and the header pin capacitance. Computer analysis based on this model showed the poles to be slightly nearer the origin, as expected, than for the ideal case. This is shown in Fig. 10, where the computed poles and zeroes of both the actual and ideal amplifiers are plotted for  $C_E = 30$  pF, corresponding to 10% overshoot.

The computer plots of Fig. 11 show the computed output response for an ideal step-function input and a 0.75-nsec risetime step input, respectively. Comparison with the computer plots of Fig. 6 (the ideal case) shows the risetimes to be almost identical, as expected. With the ideal step-function input, the computed risetime is found to be 1.1 nsec. For the 0.75-nsec risetime input pulse, the output risetime is 1.25 nsec.

The experimentally measured risetime of the Hybrid I.C. amplifier was 1.35 nsec. The output waveform is shown in Fig. 12, with an amplitude of 500 mV and 10% overshoot. The input pulse, pictured in Fig. 13, had a slight overshoot, and a risetime of 0.75 nsec.

Figure 14 shows the effects of overdriven operation on the output pulse, as the input amplitude is increased from 10 mV to 100 mV to 1 V. The overshoot of the saturated output pulse is due to the discharge of the zener diode capacitance,  $C_{D2}$ .

The performance characteristics given above were measured with a Hewlett-Packard 215A pulse generator, and a Tektronix 661 sampling oscilloscope.

### VIII. CONCLUSION

We have shown the Hybrid I.C. construction technique to be an effective means of reducing parasitic inductance and capacitance due normally to circuit components and the physical layout. Unfortunately, the frequency response of this amplifier is limited mainly by the frequency characteristics of the transistors; consequently, the reduction of parasitics had little effect on the overall performance. As faster transistors are developed, however, parasitic elements may again become the limiting factor.

APPENDIX I

Details of Hybrid I. C. Construction

The Hybrid I. C. Circuit was constructed on a small unglazed disc of #772 alumina, a type of ceramic produced by the American Lava Corporation. The disc was 0.2 in. in diameter and 0.025 in. thick, and had a specified surface roughness of less than 8  $\mu$ . The alumina discs were heated to 150°C in a vacuum of  $10^{-6}$  mm Hg. Nichrome V was then evaporated from a tungsten filament onto the alumina. The amount of Nichrome V deposited was controlled by the number of loops of Nichrome V wire hung on the filament. This method was used because the unglazed surface of the ceramic substrate required a thicker layer of Nichrome V to achieve the desired resistivity than could be obtained with Nichrome V wire used as the filament itself. The 50- $\Omega$ /square resistivity was obtained by using three loops, each made from a 2 cm length of 50-mil-diameter Nichrome V wire.

Immediately following the Nichrome deposition, the disc was coated with Shipley #AZ-111 photoresist, and spin dried. This step was repeated to insure that there were no pinholes in the photoresist layer. The discs were then baked under a sunlamp for 10 min. to dry the photoresist. The photoresist was now light-sensitive, and ready to be exposed.

Previously, a mask had been made of the desired resistor pattern to be left after etching, just as would have been done in the fabrication of an integrated circuit. The discs were now positioned under this mask, and exposed to light of high ultraviolet content, to expose the photoresist on the portion of the Nichrome to be removed. Exposure time was typically 15 sec. at a distance of 8 in. between the lamp and the disc. The photoresist was then developed by immersion in a 1:1 mixture of AZ-303 developing solution and deionized water for 15 sec. This was immediately followed by a rinse in deionized water and another 10-min bake under the sunlamp to harden the remaining photoresist.



The Nichrome was then etched in a solution of [6]

- (a) 7.9 grams ceric sulphate,  $C_e(SO_4)_2$ ,
- (b) 35 ml concentrated  $HNO_3$ ,
- (c) 130 ml deionized water.

The etch time was controlled visually, typically 2 min. Finally the remaining photoresist was removed with acetone.

The next step was to put the discs into the vacuum again and evaporate aluminum onto the surface. The aluminum can be effectively deposited at any pressure below  $10^{-5}$  mm Hg. The amount of aluminum deposited must form a layer thick enough to have a low resistivity, but at the same time thin enough to allow the Nichrome resistor pattern underneath to be seen, in order to align the second mask. The subsequent photoresist process was identical to that used for the Nichrome, with the exception that cold phosphoric acid ( $H_3PO_4$ ) was used to etch the aluminum (hot  $H_3PO_4$  attacks the Nichrome).

At this point, the fabrication of the Nichrome resistors and their aluminum interconnections is complete. The next step was to cement the disc to a 10-pin TO-5 header, and subsequently, to cement the transistor and diode chips to the disc. This was accomplished with a conductive silver cement (DuPont Silver Preparation #5504A). The actual cementing process was done under a 10X microscope, with a pair of tweezers and a steady hand. The cement was cured by baking at  $160^\circ C$  for 1 hour, and then at  $260^\circ C$  for 2 hours. Finally, the remaining connections to the transistor and diode chips were made with a thermal compression wire ball bonder, using 0.7-mil-diameter gold wire.

ACKNOWLEDGMENTS

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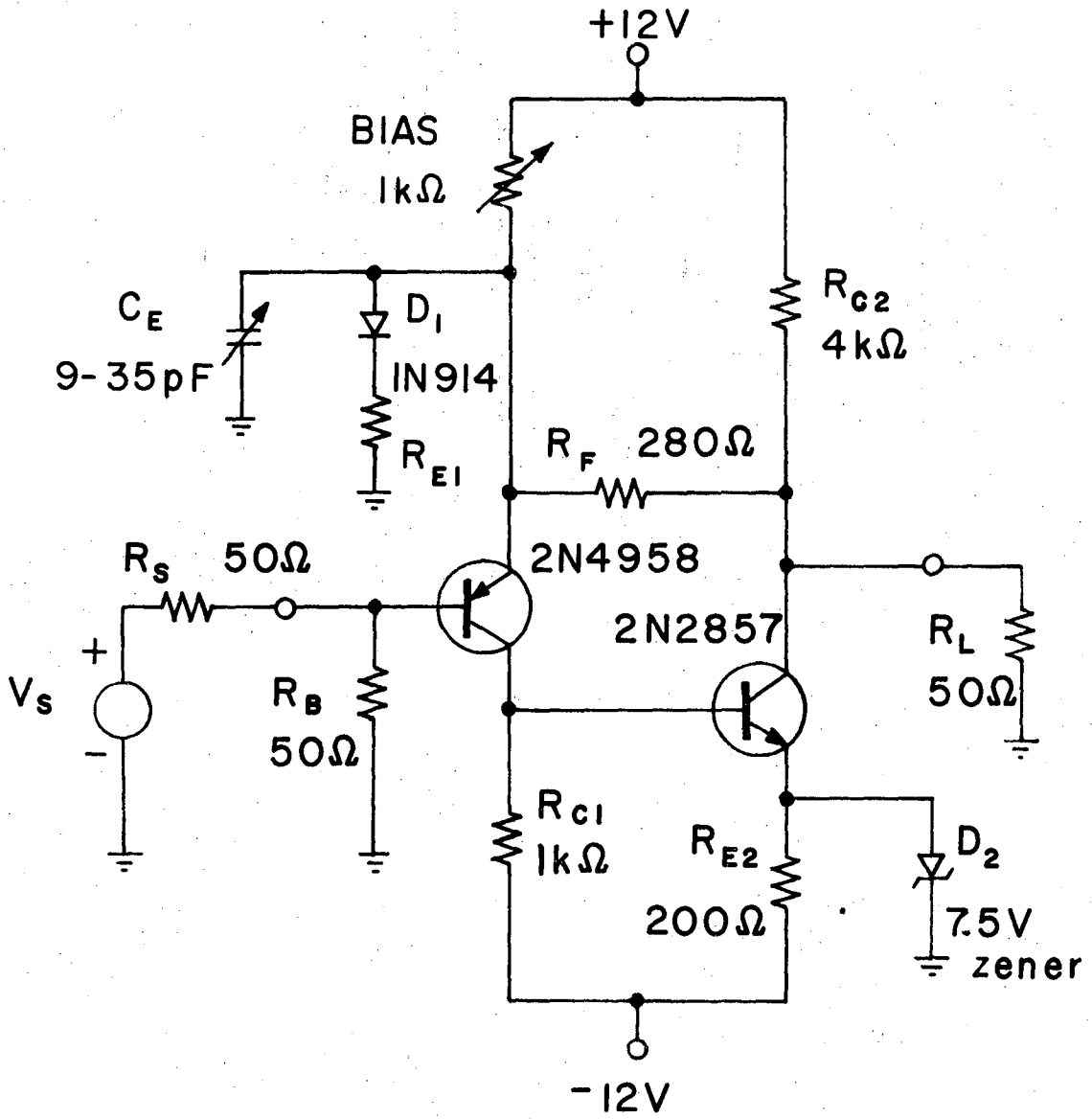
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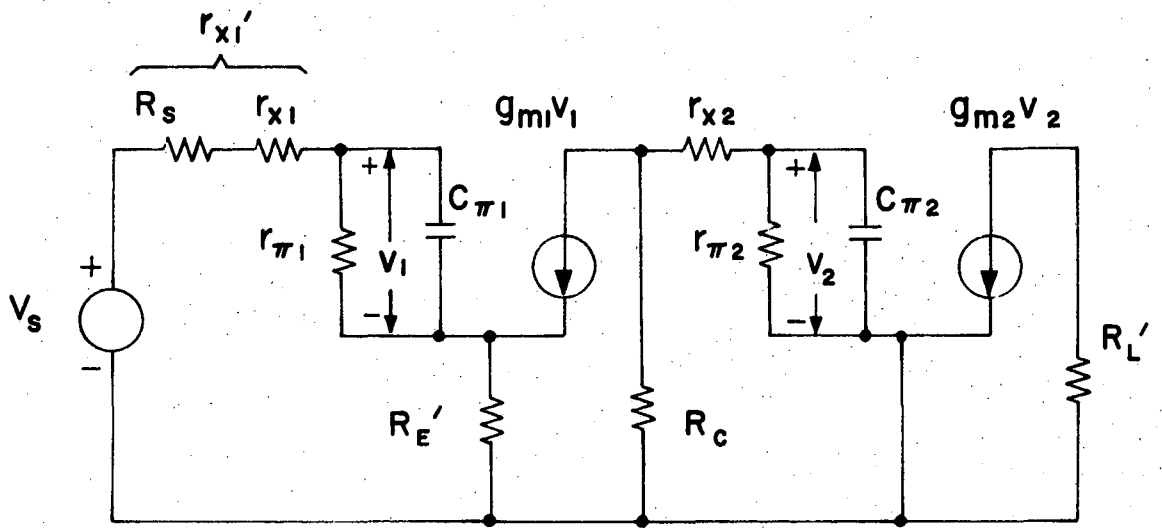
FIGURE CAPTIONS

- Fig. 1. Schematic diagram of the amplifier.
- Fig. 2. Open-loop amplifier model.
- Fig. 3. Root locus diagram of the feedback amplifier.
- Fig. 4. "Ideal" amplifier circuit model.
- Fig. 5. Effect of  $C_E$  on dominant poles and zeros.
- Fig. 6. Computer plot of "ideal" output transient response.
- (a) Step-function input.
  - (b) Pulse generator input.
- Fig. 7. Photomicrograph of the Hybrid I.C. amplifier.
- Fig. 8. Schematic diagram of the Hybrid I. C. amplifier.
- Fig. 9. Hybrid I. C. amplifier circuit model.
- Fig. 10. Root locus diagram comparing the "actual" amplifier with the "ideal".
- Fig. 11. Computer plot of the "actual" output transient response.
- (a) Step-function input.
  - (b) Pulse generator input.
- Fig. 12. Output waveforms.
- Fig. 13. Input waveforms.
- Fig. 14. Output waveforms-overdriven response.



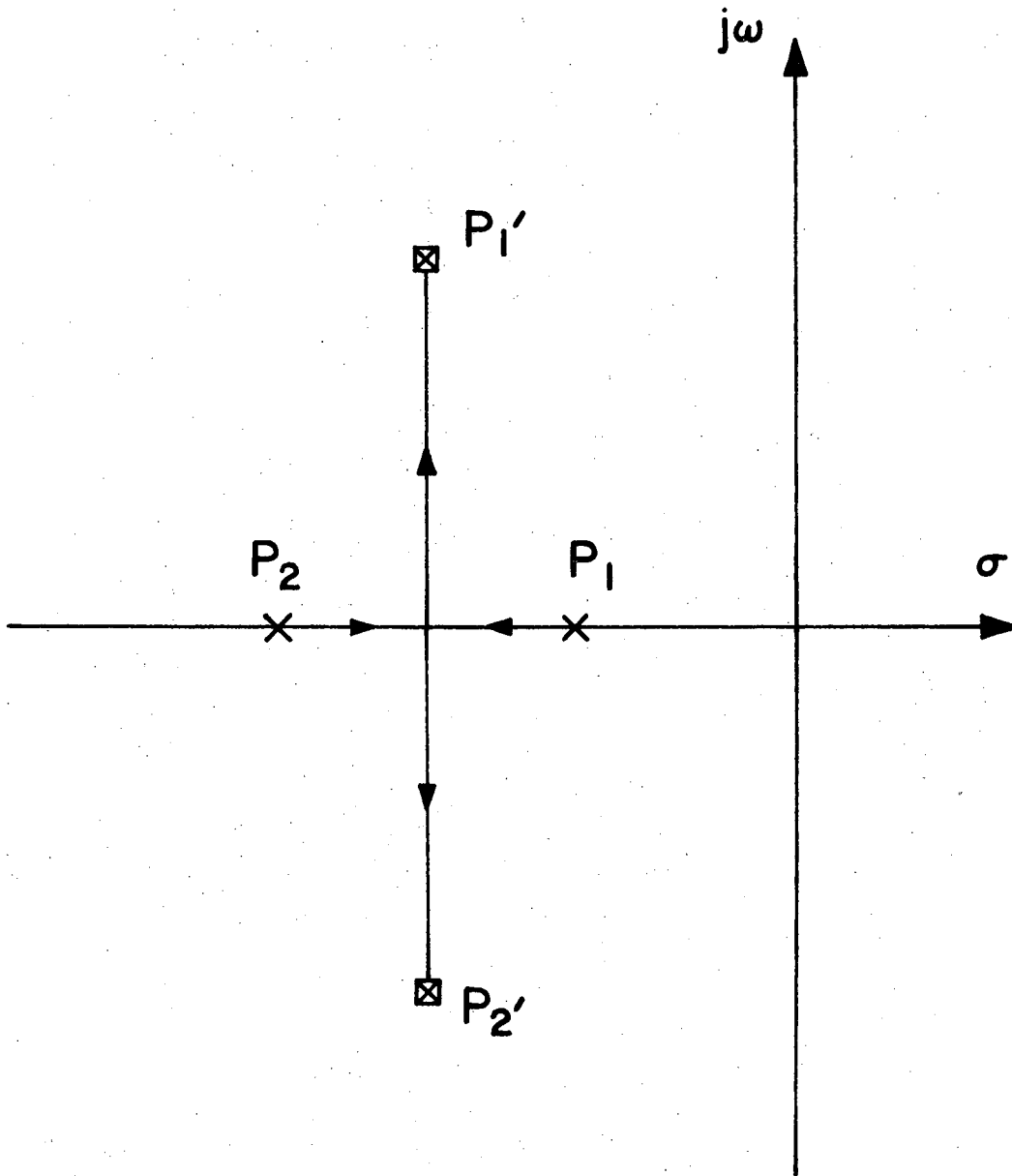
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Fig. 1



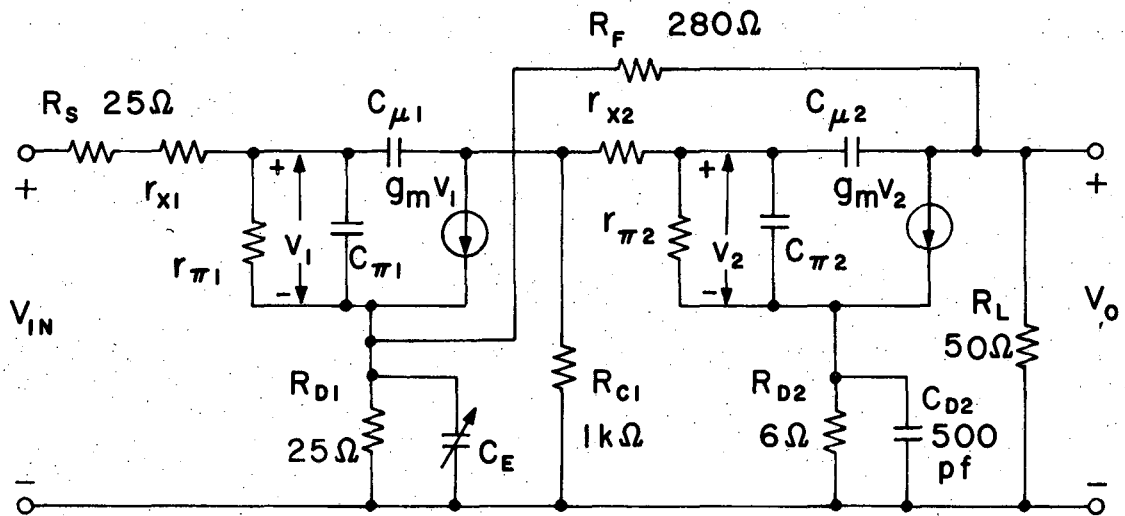
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Fig. 2



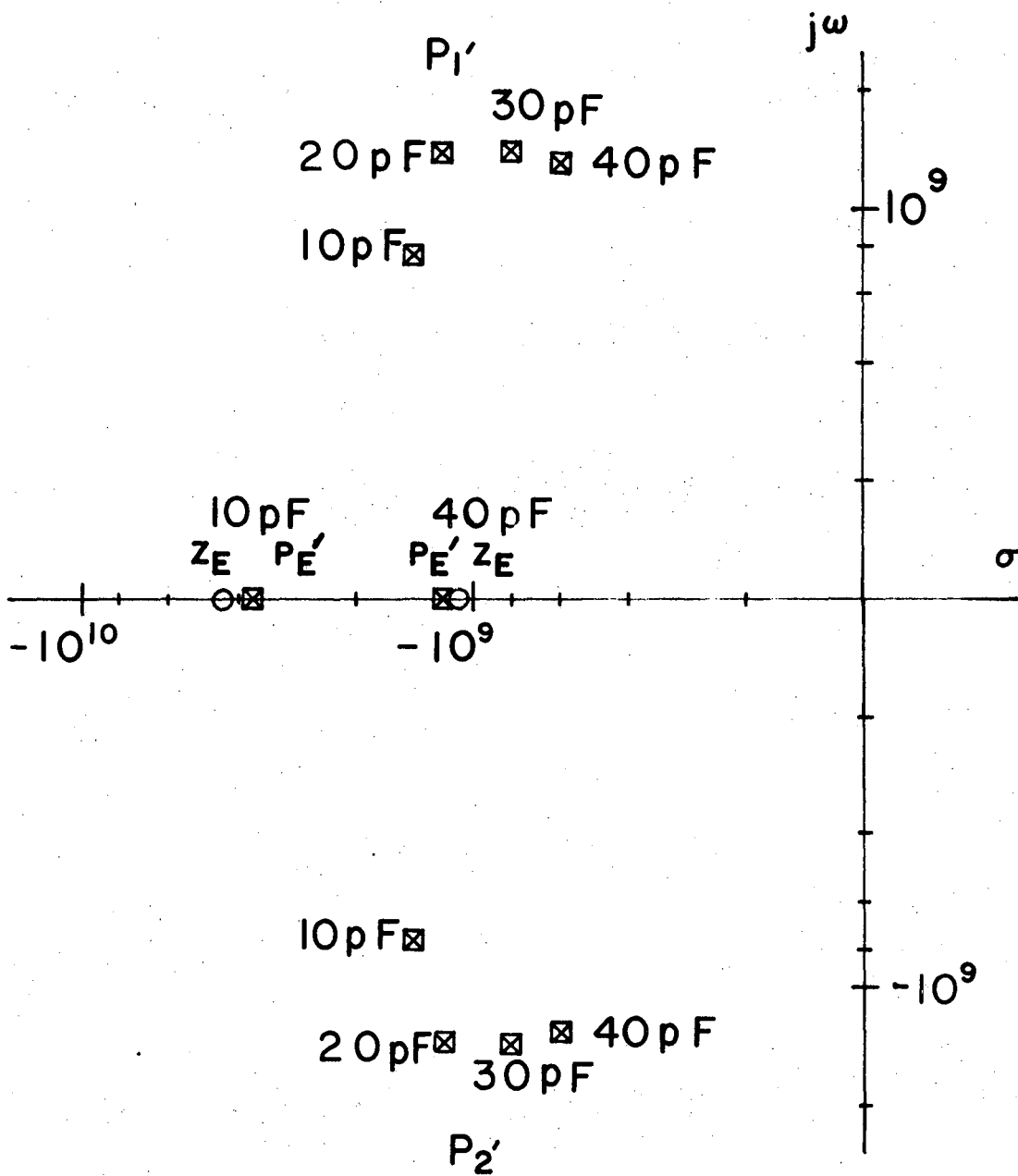
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Fig. 3



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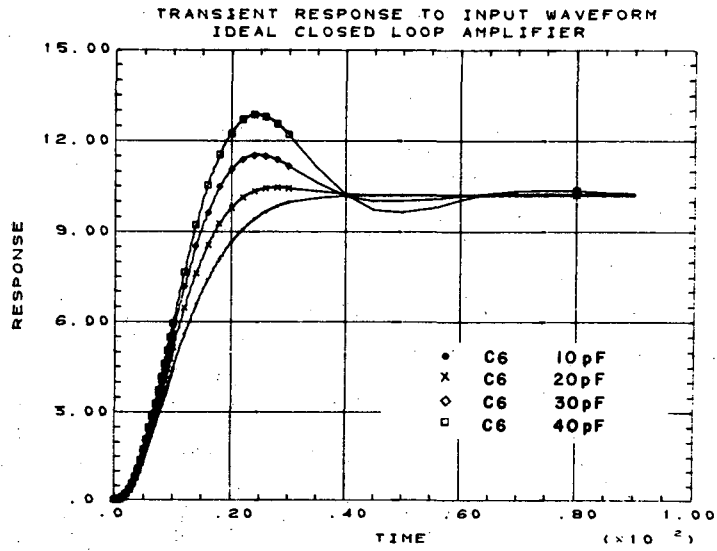
Fig. 4



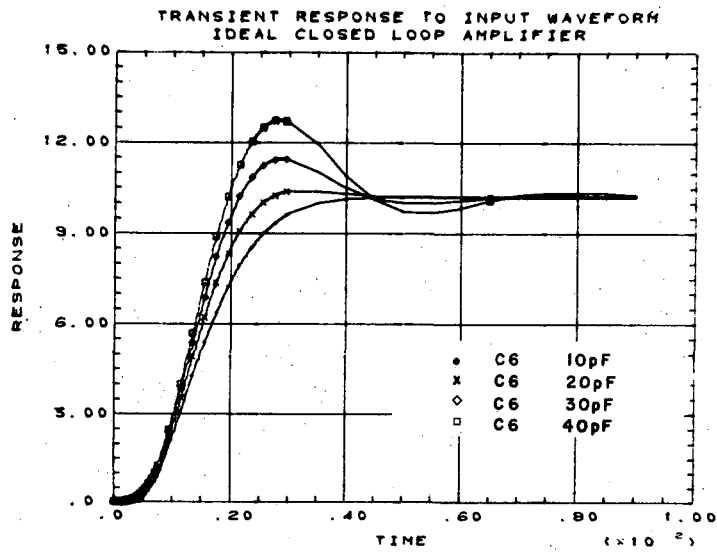
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Fig. 5





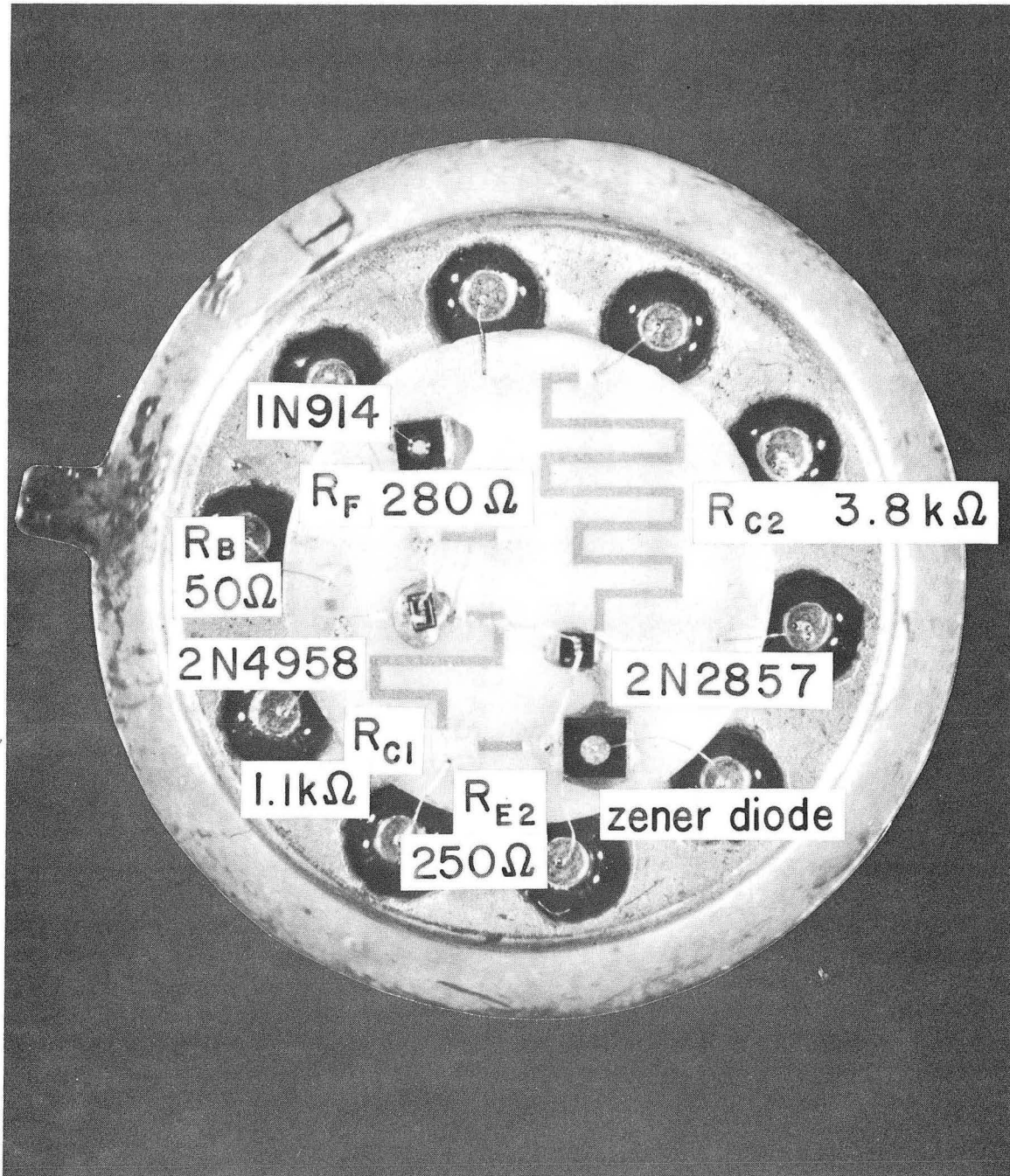
(a)



(b)

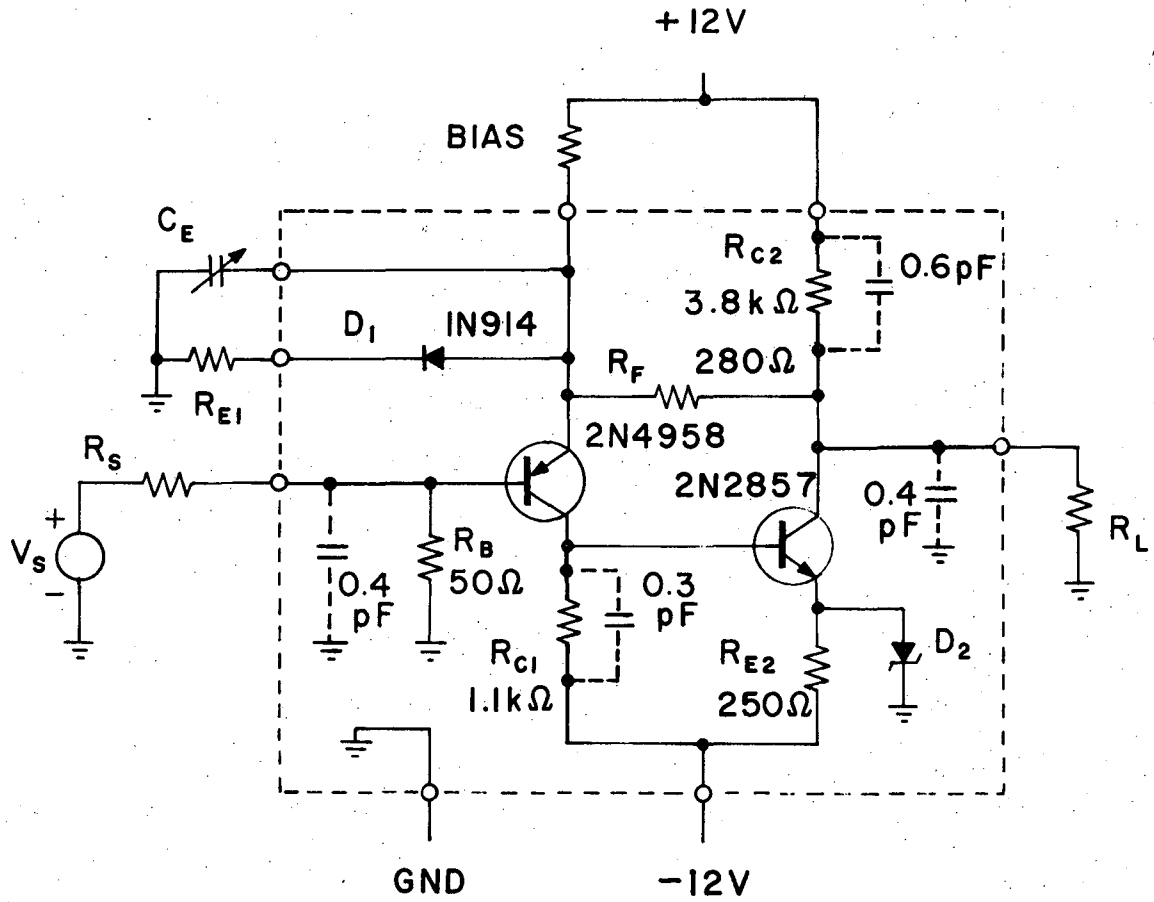
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Fig. 6



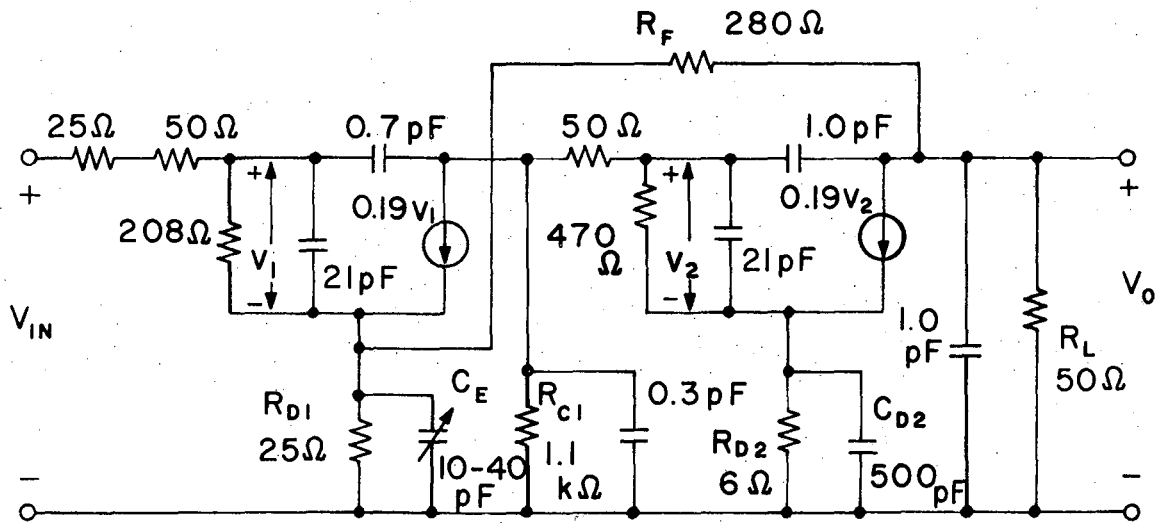
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Fig. 7



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Fig. 8



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Fig. 9

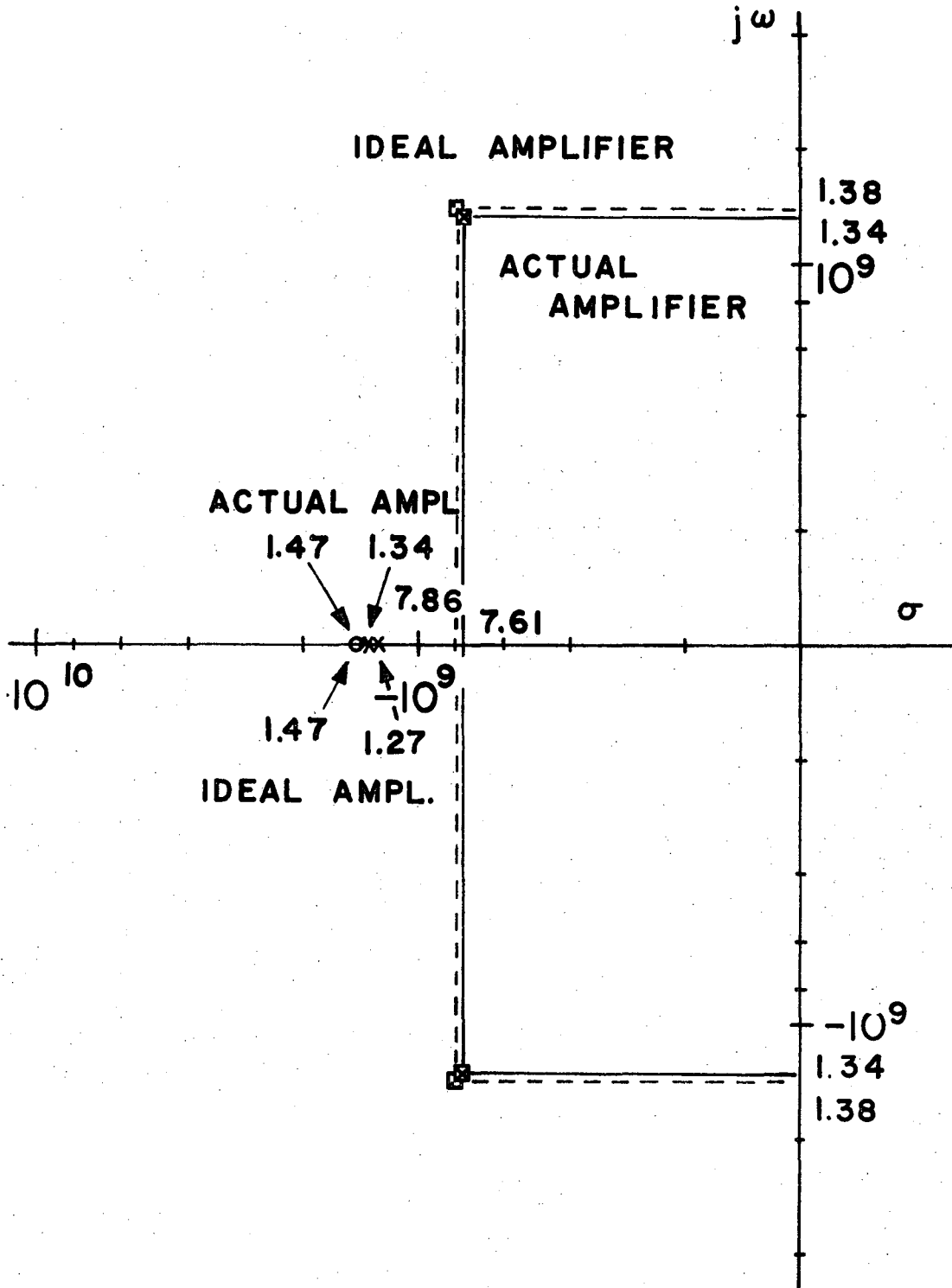
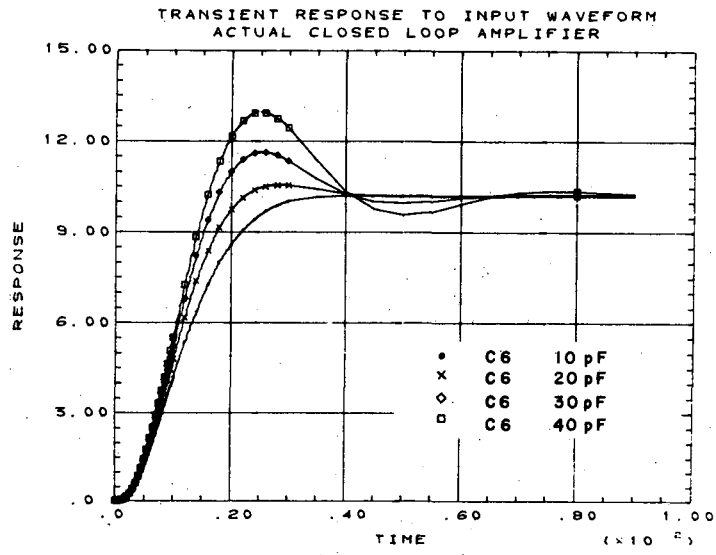
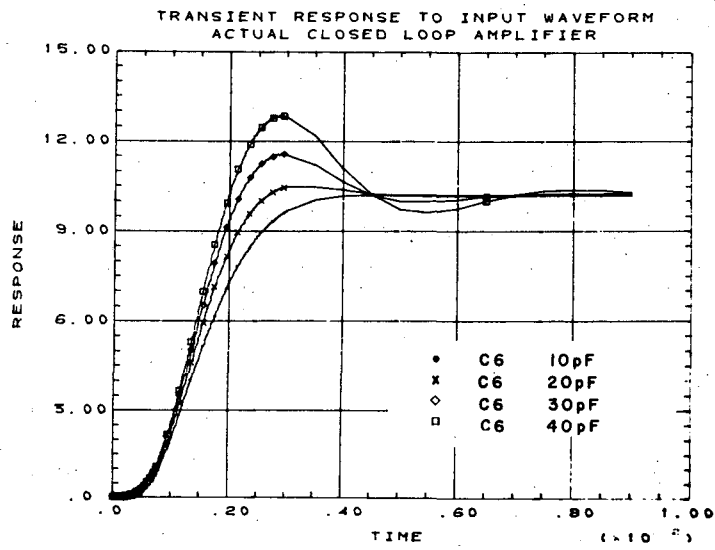


Fig. 10

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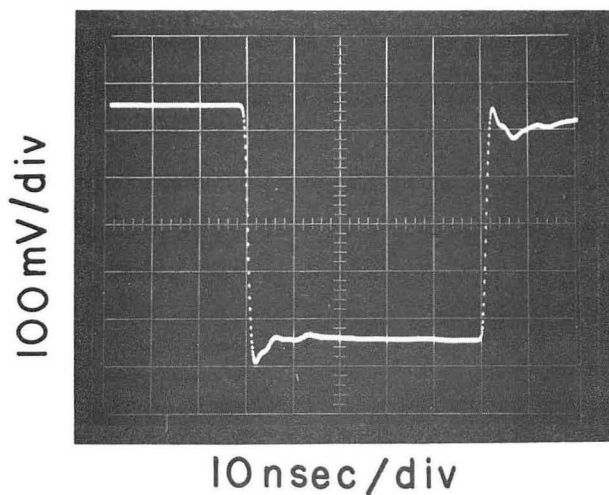
(a)



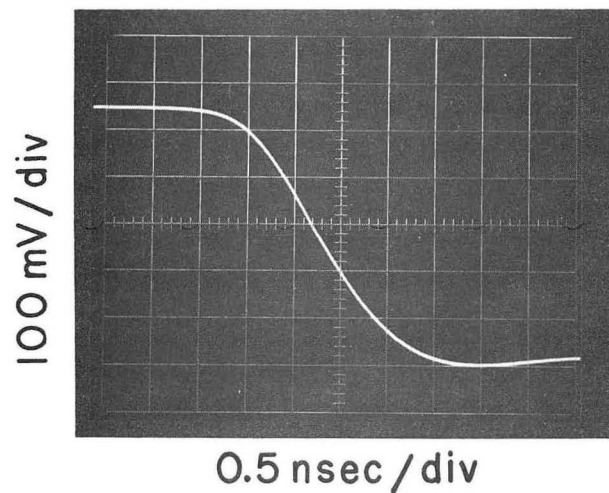
(b)

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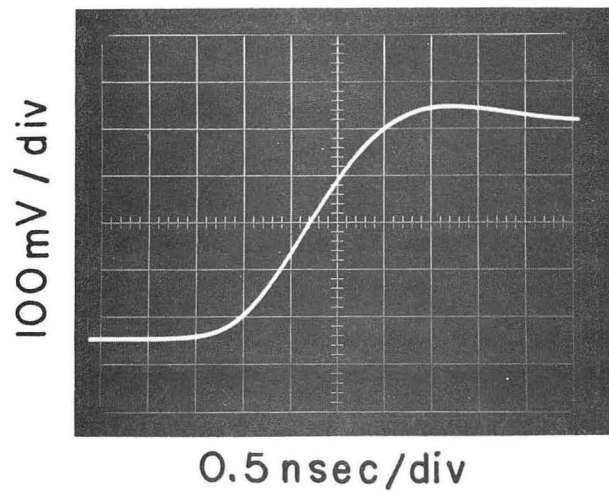
Fig. 11



Output pulse



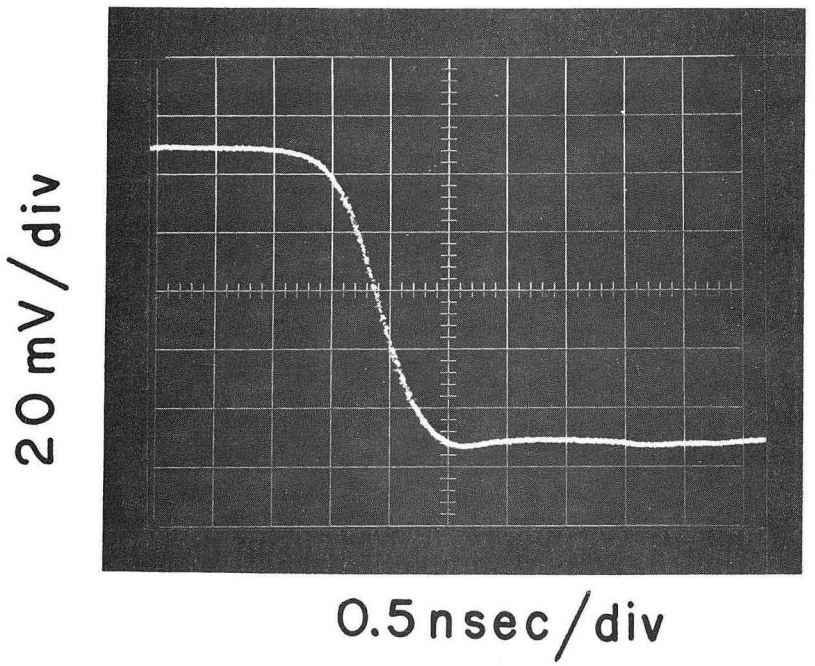
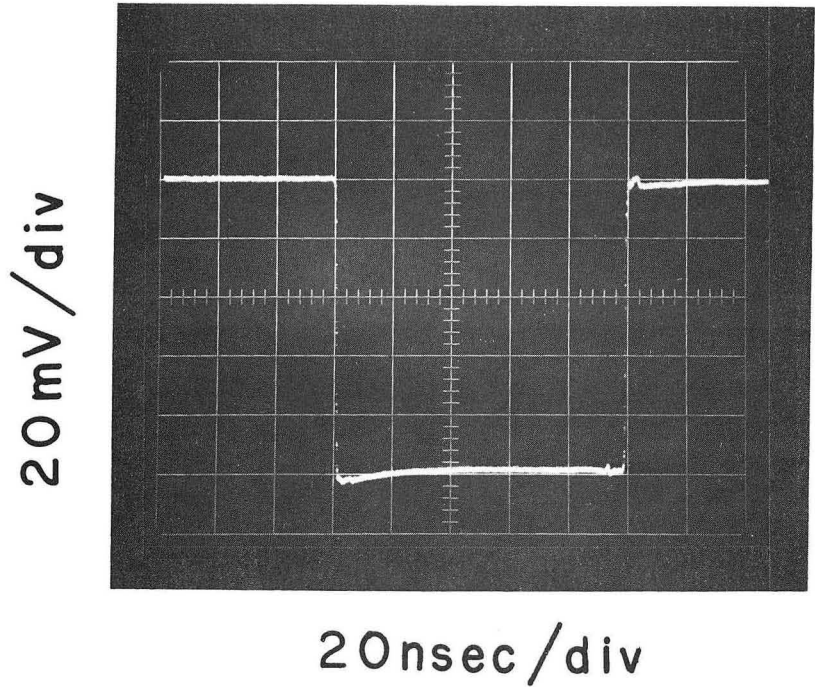
Rise time



Fall time

XBB 688-4797

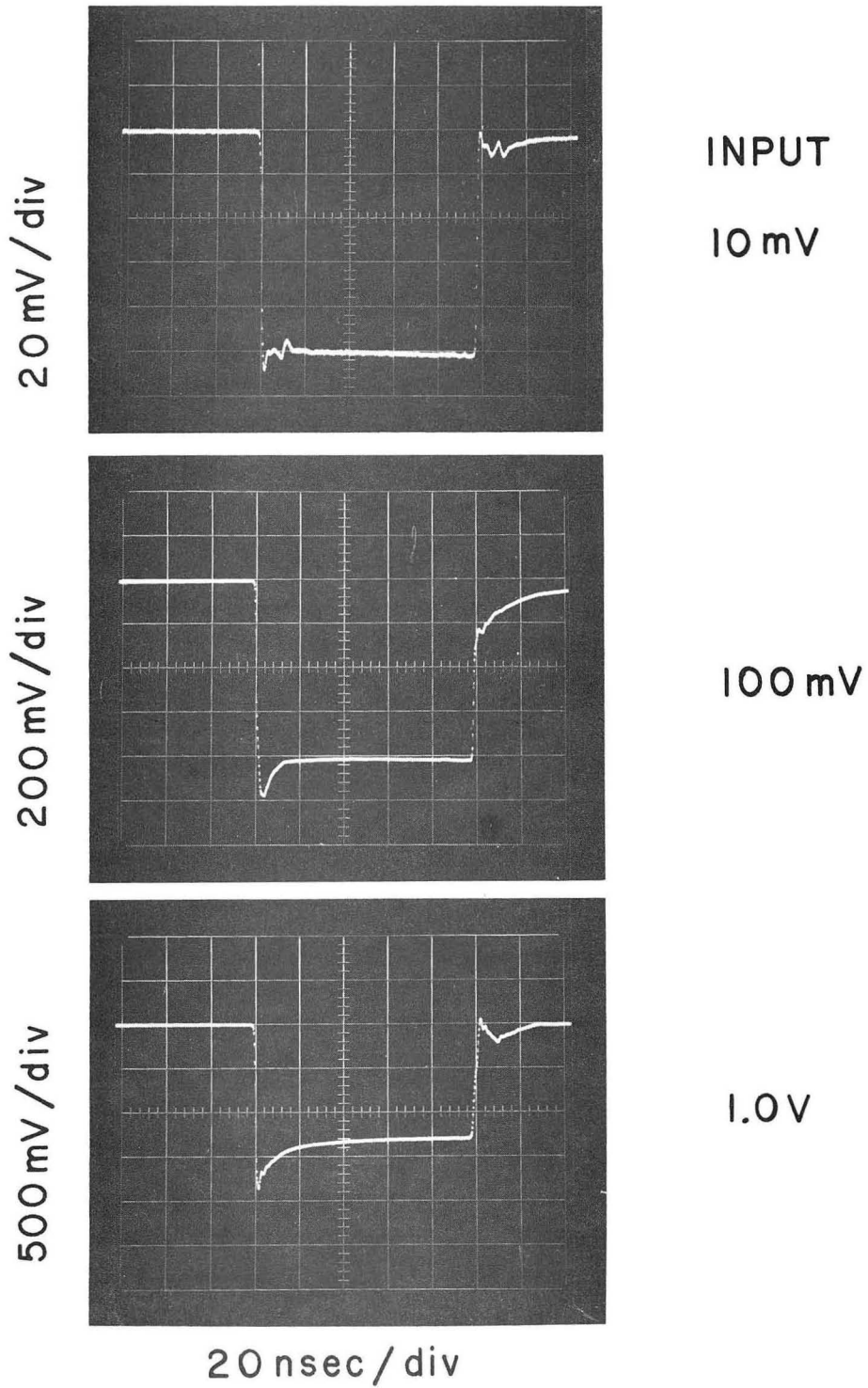
Fig. 12



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Fig. 13





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Fig. 14

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