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GAMAC SYSTEMS TEST MODULES

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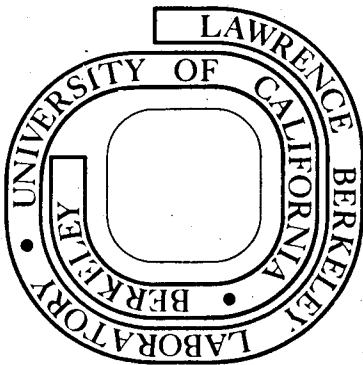
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## CAMAC SYSTEMS TEST MODULES

by

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**SUMMARY** Two CAMAC test modules have been developed at the Lawrence Berkeley Laboratory. One of these is a general purpose test module that includes the capability to test systems that use one or more of the three modes of Q response for Read and Write operations described in the CAMAC 1972 Specification. The second unit tests data transfer systems that synchronize by "handshaking" via the Look-at-Me signal.

### 1. CAMAC SYSTEM TEST MODULE

In addition to testing the Q response operations for Read and Write transfers, the CAMAC System Test Module has a WRITE/READ storage register, an A and F storage register, fixed data switches, a IAM push-button, and has bit indicator LED's for the R lines, the L line and the I line. It is therefore a general purpose system debugging tool.

The three modes of Q-response Read and Write transfer operations (Read only in this module) described in the CAMAC 1972 Specification are tested as follows:

ADDRESS SCAN MODE. To test systems that sequentially access sub-addresses until all registers in a module are read out, this module provides access to the WRITE/READ storage register for four sub-addresses, 0-3. A logic "1" Q-response is generated for READ commands,  $N \cdot A \cdot (0-3) \cdot F(0)$ : for  $N \cdot A (4) \cdot F (0)$  the Q-response is logic "0".

STOP MODE. To test systems that transfer data at one address until

Q-response signifies the end-of-block condition, this module simulates an eight-word block of data on READ command  $N \cdot A(12) \cdot F(0)$ . Q-response is logic "1" for transfers 0-7, and logic "0" for subsequent transfer attempts. The 4-bit binary word count register is presented to the R-lines, 1-4, during each  $N \cdot A(12) \cdot F(0)$  command.

REPEAT MODE. To test systems that rely on Q as a readiness response to a Read command, this module establishes a maximum data transfer rate by means of a "not ready" one-shot. A logic "1" Q-response is obtained on consecutive dataway  $N \cdot A(13) \cdot F(0)$  cycles only when an internal deadtime has elapsed since the last logic "1" Q-response to that same command.

To aid in determining whether proper Q-control of the system is functioning, a 24-bit binary counter scales each logic "1" Q-response and the count of this register is presented on the R-lines for every  $N \cdot A(13) \cdot F(0)$  command.

## 2. CAMAC SYSTEM TEST MODULE FOR L-SYNCHRONIZED BLOCK TRANSFERS

The performance of CAMAC systems that synchronize word transfers in blocks of data by recognizing the assertion of a logic "1" on the L-line as a "data ready" signal can be tested by this module.

This module simulates an eight-word block data source. Once a test transfer sequence is initiated by the dataway Execute Command, the module asserts a logic "1" on the L-line, clears to logic "0" when acknowledged by a dataway Read command, and reasserts the logic "1" after a delay from the Read Command time; cyclicly, until the eighth Read Command which terminates the sequence. The count of the Word Count Register is presented as dataway bits R1-R4 in

response to each Read Command, so a properly operating system will fill successive word locations with the binary count of one through eight.

This test module has been used to check the performance of a system which uses an EG&G BD-011 branch driver and a DEC PDP-11 computer. The BD-011 is modified to accept an "inhibit" signal via a 50 CM front panel connector. When asserted, this inhibit signal prevents the BD-011 from issuing CAMAC commands. To test the modified BD-011 system this module provides the front panel inhibit signal in lieu of the dataway L signal for block transfer control.

DETAILED INFORMATION AVAILABLE      Information on these CAMAC system test units is available from the Lawrence Berkeley Laboratory, Technical Information Division. Complete technical information can be obtained for the cost of reproducing prints. Ask for:

CAMAC SYSTEM TEST MODULE  
12x9991-P2 with all prints

CAMAC SYSTEM TEST MODULE FOR  
L-SYNCHRONIZED BLOCK TRANSFERS  
12x2251-P1 with all prints

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