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Modeling the Electrical Effects of Metal Dishing Due to CMP for On-Chip Interconnect Optimization

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***Abstract*—A dishing model is developed to investigate the electrical effects of metal dishing in the damascene process, based on experimental data and physical analysis. A metric for dishing, the Dishing Radius, has been defined. A study utilizing this model shows that the impact of dishing on performance can be mitigated at both the process and design stages. More specifically, process improvement is most effective when the dishing radius is less than 50 μm. During design, dishing effects can be suppressed by uniformly splitting a wide line into several narrower lines; the most beneficial number of line-splitting is between two and four from both efficiency and performance considerations.**

***Index Terms*—Chemical–mechanical planarization (CMP), damascene process, dishing radius, erosion, line-splitting, metal dishing.**

I. Introduction

IN CONTEMPORARY copper back-end-of-line (BEOL) technology, chemical–mechanical polishing (CMP) is widely used as the primary technique to planarize the metal surface and define metal layer thickness. Compared to the conventional chemical etching process used in Al technology, CMP has the benefit of high Cu removal rate. However, CMP also introduces undesirable side-effects, including dielectric erosion and metal dishing. Fig. 1 illustrates their influences on metal line dimensions after CMP. Both effects originate from the material property differences between dielectrics and metal under chemical and mechanical stresses: Since Cu is softer than silicon dioxide, it is more sensitive to the chemical slurry, and, hence, its polishing rate is faster; consequently, the metal thickness is lower than expected (erosion) and its surface exhibits a cylindrical shape after polishing (dishing). Both erosion and dishing degrade the process quality, cause significant yield losses in BEOL, and negatively affect interconnect performance, especially for wide global interconnects [1]–[4].

Many attempts have been made to suppress dielectric erosion and metal dishing and incorporate them into design considerations. Stine *et al.* studied the physical and electrical effects of metal-fill patterning practices for oxide CMP processes [5]. Their work pointed out that pattern density is the key metric that determines the variations in interlayer dielectric (ILD) thickness post CMP process. Ouma *et al.* designed test masks and effectively modeled oxide CMP process using the concepts of planarization length and pattern density [6]. Zhang *et al.* presented an empirical approach to reduce dishing by adjusting the applied pressure and slurry design [7]. Nguyen *et al.* proposed the modeling of dishing in CMP process based on the mechanics of wafer-pad contact; the fitting results were good but the model was only valid for a limited over-polishing time [8]. In short, while dielectric erosion has been extensively studied [9]–[12], practical and quantitative understanding of the dishing effect remains unclear. With rapid technology scaling and increasingly tighter design budgets, it is crucial to carefully consider these layout dependent effects in both the process and the layout design stages, in order to meet the objectives at 65-nm technology generation and beyond. More importantly, the understanding of these effects bridges BEOL technology and interconnect electrical performance. As a consequence, optimal solutions to reduce dishing and erosion in CMP will likely involve a combination of both technology and design optimizations.

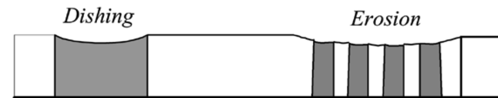

Fig. 1. Cross-sectional view of metal dishing and erosion effects after CMP process.

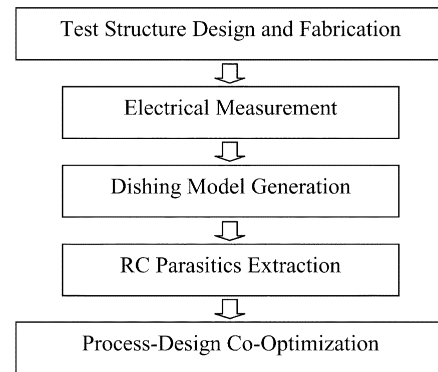

Fig. 2. Investigation of the metal dishing impact on interconnect performance.

In this paper, we perform extensive experimental and simulation studies to investigate the effects of metal dishing in Cu CMP process. Fig. 2 shows the overall flow of this work. Section II presents the test mask design and electrical measurements to characterize the dishing effect. Based on the experimental results and physical considerations, an analytical dishing model is developed, which captures major CMP process characteristics and is scalable with interconnect layout size. For model simplicity, an effective dishing parameter (dishing radius) is introduced and can be directly extracted from test structures (Section II). Then, using this scalable model, the impact of the

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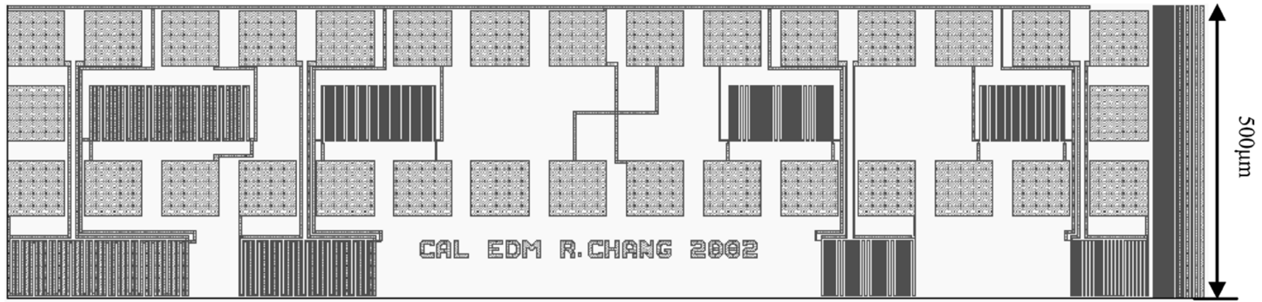


Fig. 3. Cell design for the electrical characterization of dishing effect in Cu damascene process.

TABLE I
THEORETICAL AND MEASURED COPPER LINE RESISTANCES

Line *w* (μm)	Liner (μm)	Cu *t* (μm)	Line Length (μm)	Measured R (Ω)	Theoretical R(no dishing) (Ω)	Difference in R (%)
5	0.08	0.5	3961.0	35.18	32.16	9.39
4	0.08	0.5	3992.2	43.52	40.80	6.67
3	0.08	0.5	4023.4	58.10	55.47	4.74
2	0.08	0.5	4054.6	87.23	85.89	1.56
1.6	0.08	0.5	4067.1	111.69	109.69	1.82
1.2	0.08	0.5	4079.6	154.35	151.37	1.96
0.8	0.08	0.5	4092.1	246.63	243.27	1.38
0.4	0.08	0.5	4104.6	620.34	613.31	1.14

dishing effect on interconnect performance is analyzed in Section III. Specifically, we employ this new model to examine the efficiency and tradeoffs of process and design techniques for the purpose of suppressing dishing effect and minimizing its impact on circuit performance. Section IV summarizes this paper.

II. EXPERIMENTAL WORK AND METAL DISHING MODEL

A. Test Chip Design

The impact of metal dishing is characterized by measuring post-CMP line resistance (R). Since the dishing effect causes a nonplanar metal surface (as shown in Fig. 1), and since it reduces the conductive cross-section it leads to larger resistance, as compared to the theoretical value of R for a line with planar surface. Therefore, in the design of test structures, the key consideration is its suitability for electrical testing of R (E-test). Furthermore, since metal thickness loss caused by dishing exhibits strong correlation to metal width (e.g., wider lines suffers dishing more severely) [8], the design of test cells particularly focuses on the relationship between the amount of dishing and line width (w).

Fig. 3 shows the mask layout of a test cell. Each cell contains eight serpentine-shaped metal lines that vary in line width (0.4, 0.8, 1.2, 1.6, 2.0, 3.0, 4.0, and 5 μm); the line length is 4 mm; and the target line thickness is 0.4 μm. These dimensions are chosen from typical global on-chip interconnects. Depending on w, the estimated line resistance is within the range of 30 to 650 Ω, so that R can be easily extracted by an automatic impedance test. For each line, there are two pads at each end that are used as probe contacts during E-test (Fig. 3), [13]. Four-point measurement, which applies current through the two outer pads and measures voltage difference between the two inner pads, is employed to measure the resistances of the lines. On the right side of the E-test cell, eight long lines are laid out for scanning electron microscopy (SEM) test, which can provide the cross-sectional view of metal lines after CMP. Overall, an E-test cell has a dimension of 1900 by 525 μm. In order to decouple dishing effect from erosion, pattern densities are approximately uniform across the cell, so that metal thickness loss caused by erosion is the same across different serpentine-shaped test lines. Moreover, because the cell footprint is relatively small, but arguably comparable to the characteristic length of Cu erosion (a few hundred of microns depending on the process [6]), our test lines have about the same pattern density and are thus expected to suffer the same level of erosion. So, for test lines with different widths, their differences in the increment of R after CMP are mainly caused by dishing. The test chips are fabricated at the Berkeley and the RPI micro-fabrication laboratories, using a single damascene process.

B. Measurement Results and Analytical Dishing Model

Table I lists the measured R for various lines and the corresponding theoretical values, which are calculated based on the measured neighboring oxide thickness assuming ideal rectangular metal cross sections without dishing. As expected, the measured R is larger due to dishing effect and wider lines suffer more severe resistance increase. For instance, R increases by

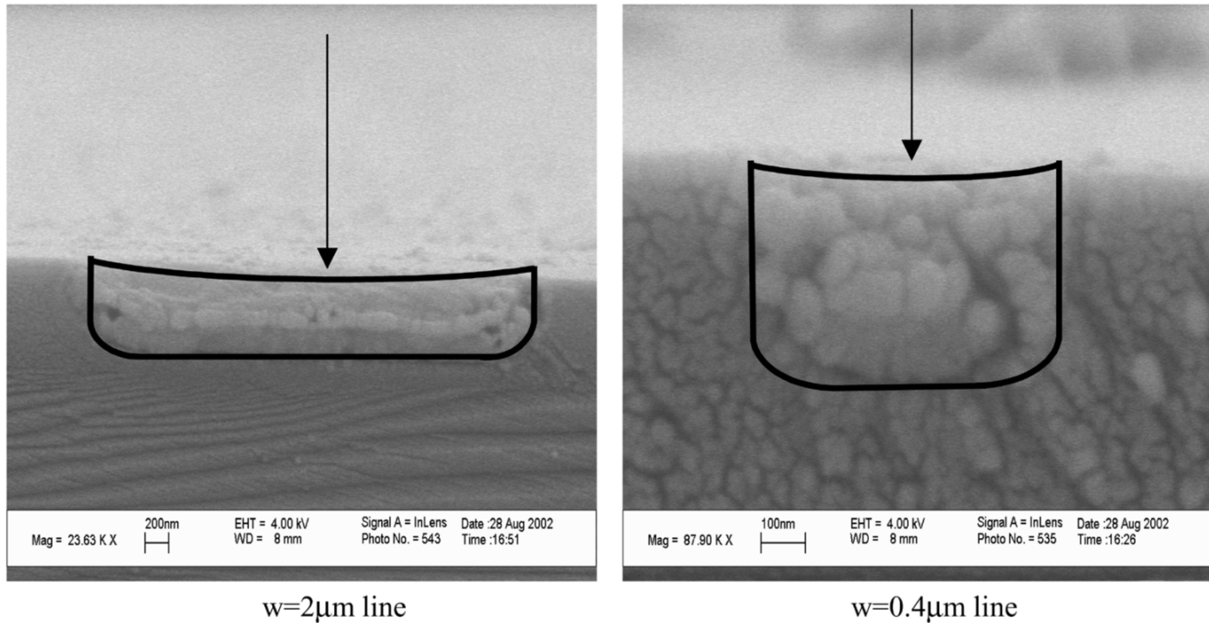


Fig. 4. Post-CMP cross-sectional SEM pictures.

9.4% when $w = 5\ \mu$m, while it is only 1.1% larger than theoretical value if $w = 0.4\ \mu$m. Fig. 4 shows the cross-sectional SEM pictures for 0.4- and 2-μm-wide lines, which confirms the observation that wider lines experience more dishing than narrower ones. In addition, these pictures illustrate the nonplanar shape of metal surfaces under dishing, which can be approximated by the segment of a circle [8], [14].

Such a concave-cylindrical surface is the result of both the overall mechanical polishing and the statistical behavior of the polishing pad asperities in a CMP system [15]. During CMP, material removal happens at the mechanical contact between the pad asperities and metal surface, and, at a relatively slower rate, on the dielectrics. Although the pad asperities have different sizes and heights, they come to contact with every line feature with equal probability. As a consequence, the concave-cylindrical topology forms during overpolishing. To empirically model this effect (in a matter consistent with its physical basis), we introduce the concept of dishing radius (R_{dish}) that captures the cylindrical metal surface after CMP. Under this model, line resistance under dishing is calculated as

$$R = \frac{(\rho \cdot \mathrm{length})}{\left[w(t-dt)+\frac{wR_{\mathrm{dish}}}{2}\sqrt{1-\left(\frac{w}{2R_{\mathrm{dish}}}\right)^2}-R_{\mathrm{dish}}^2\sin^{-1}\left(\frac{w}{2R_{\mathrm{dish}}}\right)\right]} \quad (1)$$

where the parameters are defined in Figs. 5 and 6.

For typical on-chip interconnect structures, R_{dish} is independent of line dimensions, but is a function of process parameters (e.g., the pad asperity size, slurry chemistry, over-polish time, etc.). The value of R_{dish} can be easily extracted by matching the measured *R* (Table I) with model predictions [(1)]. Such an extraction is demonstrated in Fig. 7. Note that this extraction can separate dishing from erosion, due to their different dependences on *w*: while erosion only has a weak dependence on line width, dishing is strongly related to *w*. Since the measurements may be noisy, we use the least square method to extract R_{dish} by averaging out the measurement noise. For this process, the extracted R_{dish} is about 40 μm. A larger R_{dish} represents better planarity of polished metal surface. In Fig. 7, metal conductance is almost linearly dependent on *w* since R_{dish} is much larger than *w* of the test lines.

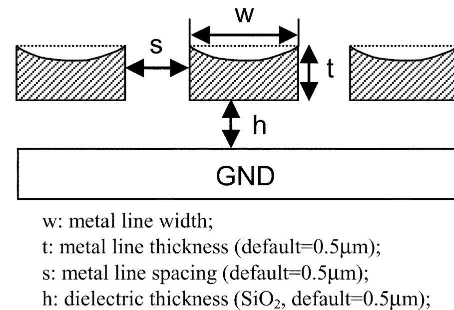
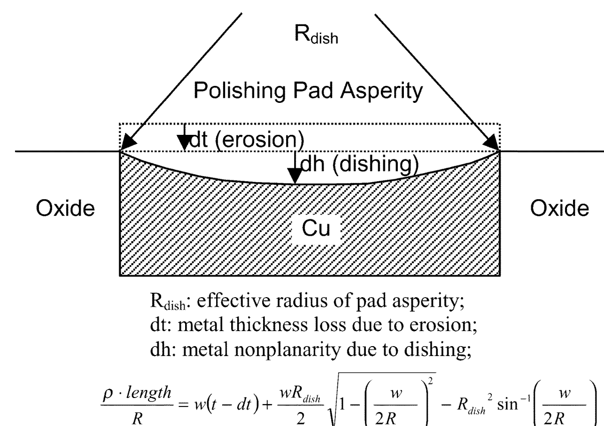


Fig. 5. Two-dimensional cross-sectional view and parameter definitions of global interconnect structure (lines above one ground plane).



$$\frac{\rho \cdot length}{R} = w(t-dt) + \frac{wR_{dish}}{2}\sqrt{1-\left(\frac{w}{2R}\right)^2} - R_{dish}{}^2 \sin^{-1}\left(\frac{w}{2R}\right)$$

Fig. 6. Metal dishing model for copper damascene process.

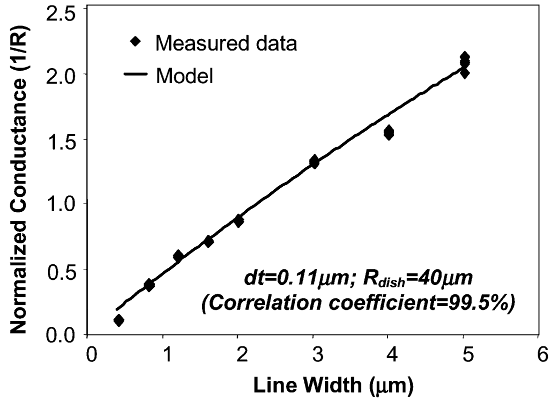


Fig. 7. Model parameters extracted from measurement.

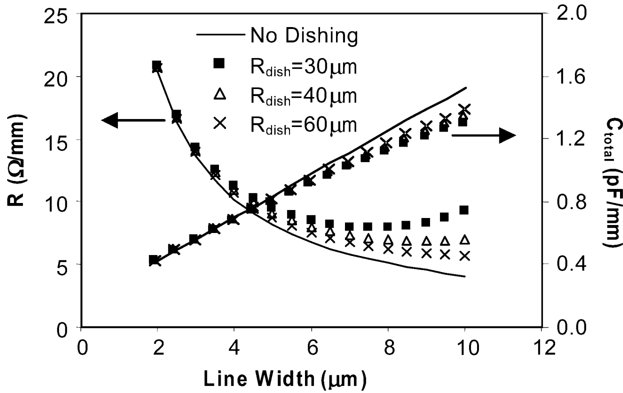


Fig. 8. Simulations showing the dependence of RC parasitics on dishing and line width ($C_{\mathrm{total}} + C_{\mathrm{ground}} + 2 * C_{\mathrm{coupling}}$).

III. Interconnect Design With Dishing Considerations

In contemporary silicon technology, dielectric erosion and copper dishing have become the yield-limiting factors in backend-of-the-line (BEOL) process. Although better CMP process control is needed to mitigate their negative effects in circuit performance, it is also beneficial to include these manufacture concerns into the design stage in order to avoid chip yield loss. In this section, possible solutions for dishing suppression are examined from both process and design perspectives. In particular, the efficiencies and tradeoffs of these techniques are investigated by means of simulation.

A. Performance Metric: RC Delay

In order to evaluate the impact of metal dishing, the *RC* product is employed as a performance metric that can be easily related to interconnect layout specifications, such as line width and space [16]. Although more complicated metrics, such as RLC delay or full waveform models may be more accurate, the simple *RC* product predicts the correct performance scaling with line size tuning and is suitable for design optimizations at the early stage. Based on R_{dish} model in Figs. 6 and 8 shows the Raphael simulation results for resistance and total capacitance (C_{total}), given various dishing radius and line width values. While the resistance increases significantly for wider lines and smaller R_{dish}, C_{total} is relatively insensitive to dishing. Therefore, it is necessary to incorporate the dishing effect in *R* calculation [(1)]. On the other hand, since the impact of dishing is negligible for capacitance, we can adapt the analytical formulas in [17] to calculate C. As a result of the dishing effect, the *RC* delay may go up with increasing w, in direct contrast to the dependence of delay on *w* without dishing, as shown in Fig. 9. In our experiments, the minimum delay is achieved at $w_{\mathrm{opt}} \sim 4\ \mu$m (note that for an ideal CMP without dishing, w_{opt} is infinite). Furthermore, with the linkage between dishing and line width, delay sensitivity to line width variation behaves nonmonotonically (Table II), reaching a minimum at $w = w_{\mathrm{opt}}$. In comparison, when there is no dishing, the delay sensitivity continuously decreases with increasing w. Overall, the inclusion of the dishing effect restricts the design space and complicates performance analysis.

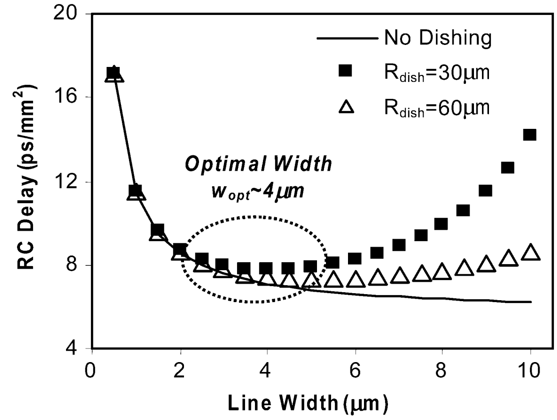


Fig. 9. Simulations showing the optimal line width ($\mathrm{W_{opt}}$) due to dishing.

TABLE II
RC Delay Sensitivity to 20% Width Variation

w (μm)	ΔRC (no dishing)	ΔRC (R_{dish}=40μm)
2.0	6.24%	5.74%
4.5	3.48%	0.8%
6.0	2.75%	4.27%

B. BEOL CMP Process Improvement Considerations

The delay penalty from dishing can be mitigated either by improving the CMP process or by physical layout techniques at the design stage. These solutions are more essential at future technology nodes as the timing budget becomes tighter. For instance, metal-filling is a commonly used technique to reduce the intra-die variations in metal planarity. By inserting small metal islands in a blank area, metal pattern density can be balanced, and, thus, dielectric erosion is mitigated.

To suppress metal dishing, various attempts have been made to improve the quality of the CMP process (i.e., increase R_{dish}). One of the methods developed in recent years focuses on better slurry design: after the first-step slurry, which has high Cu removal rate, another type of slurry is used when polishing reaches the barrier layer. The second-step slurry is selective in that it has higher removal rate for the barrier layer, while the polishing rate is much lower for Cu and dielectrics. In future advanced BEOL technologies, where more complex materials will be involved,

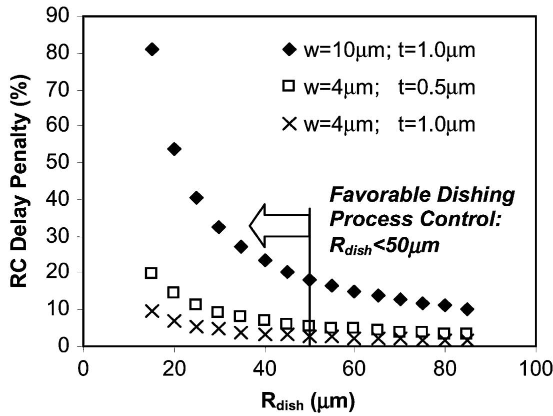


Fig. 10. When $R_{\rm dish} < 50\ \mu$m, improving process control can efficiently reduce delay penalty due to dishing. (Step size of $R_{\rm dish}$ increasing: 5 μm; h = 1.0 μm).

this multistep slurry strategy is crucial in controlling the metal planarity. Besides slurry optimization, other methods, including spindle engineering and polishing pad design, are also helpful in reducing the variation of metal thickness.

With better process control, $R_{\rm dish}$ can be increased, reducing the impact of dishing on signal delay. On the other hand, the efficiency of these approaches diminishes when $R_{\rm dish}$ goes further up. As illustrated in Fig. 10, we simulate the difference in *RC* delay between an ideal process (without dishing) and the realistic case (with dishing) under various dishing conditions. For a variety of line dimensions (i.e., w and t), we observe that it is only favorable to suppress dishing via process control when $R_{\rm dish} < 50\ \mu$m. Beyond that, the gain of dishing radius increase becomes negligible. Thus, for practical concerns, $R_{\rm dish} \sim 50\ \mu$m is the upper-limit of CMP process enhancement.

C. Layout Design Techniques for Dishing Suppression

Besides process improvement, the dishing effect can also be mitigated by layout design techniques, such as inserting holes into a wide line (metal-drilling) or dividing a wide metal line into narrower lines (line-splitting, as shown in Fig. 11). These techniques can alleviate the performance penalty due to dishing, since narrower metal segments are more robust to dishing (Fig. 9). Furthermore, the application of narrower lines also enhances thermal robustness of high-speed interconnects [18]. In the case of wide Cu lines, either metal-drilling or line-splitting increases the aspect ratio of the wire. Hence, the surface-area-to-volume ratio is improved, resulting in more efficient heat dissipation.

In terms of the impact on interconnect performance, metal-drilling and line-splitting are electrically similar to each other, and thus we only focus on line-splitting in this paper. For a fixed pattern density (hence the same expected erosion), the larger the number of split lines (N), the smaller the impact of dishing, as illustrated in Fig. 12. The tradeoff of this approach is the extra cost of chip area: in the regions with wider lines that need to be split, area cost goes up linearly with increasing *N*, assuming minimum space is applied between narrower lines. For future generation interconnects, if we consider the liner effects, line splitting implies even more area cost due to more volume of the higher resistance barrier layer in the line-splitting case, which has to be compensated by using lines wider than *w/N*. Fig. 12 further indicates that the performance gain via line-splitting drops to a negligible level when *N* exceeds five. Therefore, considering the area cost penalty during splitting, a practical approach may only require *N* values between two and four. In addition to area concerns, line-splitting also introduces extra fringing capacitances. Fig. 13 demonstrates that when $N > 5$, more splitting leads to a delay penalty from the larger $C_{\rm total}$, which almost equals the *RC* penalty due to the dishing of the original wide line. In conclusion, from both efficiency and performance considerations, *N* between two and four is optimal for typical on-chip interconnects.

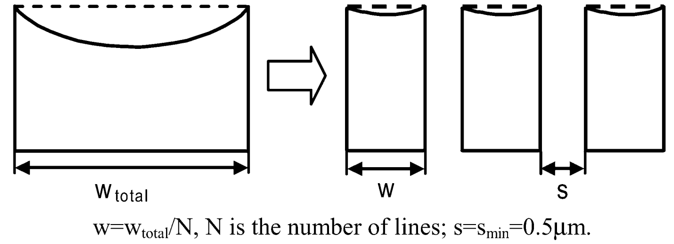


Fig. 11. Line-splitting suppresses dishing, but sacrifices area and increases capacitance.

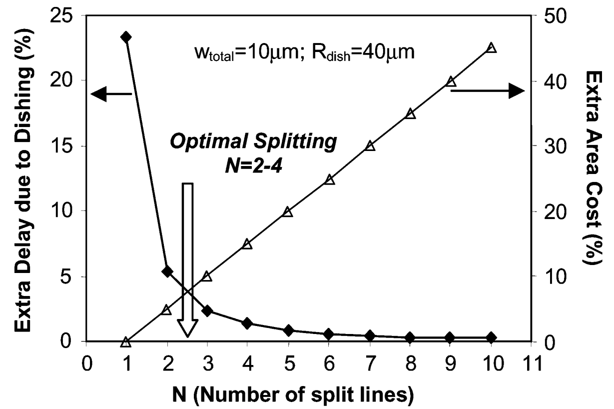


Fig. 12. Gain in *RC* delay drops fast when splitting lines.

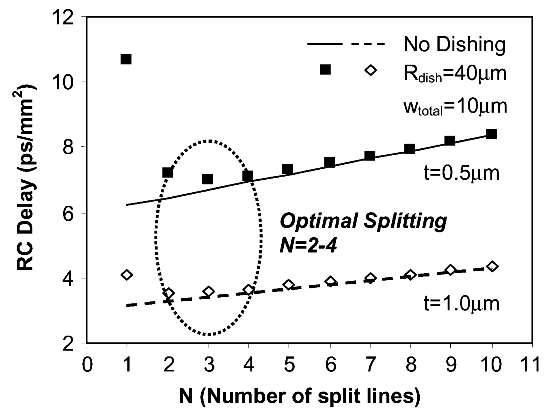


Fig. 13. To minimize line delay, optimal splitting is 2–4.

IV. Conclusion

In this paper, we introduce the dishing radius concept and present a dishing model that captures the correlation between line width and metal dishing. Based on the analysis and modeling on the electrical effects of dishing, it is observed that process improvements for dishing reduction are desirable up to the point when the dishing radius $R_{\rm dish}$ is more than 50 μm. On the other hand, if it is not possible to raise the dishing radius above 50 μm or so, then during the layout design stage, splitting a wide line to two, three, or four narrower lines seems to counteract the effects of dishing. With excellent model scalability, this new model can be easily incorporated with other interconnect process concerns (e.g., electromigration and metal filling) for further interconnect technology-design co-optimization.

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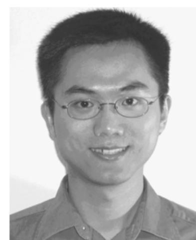

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