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Design of a CMOS On-Chip Slot Antenna With Extremely Flat Cavity at 140 GHz

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Abstract—A novel design for a fully on-chip antenna operating at 140 GHz that can be fabricated with standard CMOS technology is proposed. In addition to the traditional microstrip feeding, the slot antenna is backed with an extremely thin cavity formed by two CMOS inner metal layers and vias in between. The proposed cavity prevents radiation from going inside the lossy silicon substrate and enhances the radiation of the slot antenna. It is also shown that the antenna radiation is not affected significantly by other metallic parts on the chip. Good agreement is achieved between results from a frequency-domain solver, HFSS, and a time-domain solver, CST. The simulated gain is around $-2$ dBi, and the radiation efficiency is around 18%, despite ohmic losses enhanced by the extreme flatness. The input 10-dB bandwidth is around 5 GHz. The total area of this antenna is $1.2 \times 0.6 \text{mm}^2$ (0.1564$\lambda_0 \times 0.283\lambda_0$ at 140 GHz).

Index Terms—Cavity, CMOS, millimeter wave (MMW), on-chip antenna (OCA), passive imaging, RFIC, slot antenna.

I. INTRODUCTION

CMOS technology is considered an excellent platform for highly integrated operating at millimeter-wave (MMW) frequencies in terms of its low cost and weight. Various transceiver designs without integrated antennas have been implemented on single die using CMOS technology at MMWs [1], [2]. However, to achieve a fully integrated system, it is highly desirable to incorporate the antenna with the front-end circuit. With an integrated antenna, the system size could be shrunken to unprecedented levels, and on-chip antennas (OCAs) have been proposed to minimize antenna feed interconnection losses. It is interesting to note that MMW OCAs are useful even when they operate at a frequency much higher than the one in the CMOS active components—for example, when self-mixing or other circuit techniques are supported in part by the Semiconductor Research Cooperation under Grants 1962.001 and 2009-VJ-1962.

The authors are with the Department of Electrical Engineering and Com-puter Science, University of California, Irvine, Irvine, CA 92617 USA (e-mail: shijip@uci.edu, f.capolino@uci.edu). Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

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Another major concern in the integration of OCAs is the electromagnetic interference (EMI) resulting from mutual coupling between the antenna and the high-frequency front end. In OCA solutions, the antenna and circuit front end are utmost close to each other compared to other solutions (e.g., AIP and antenna out of package). Therefore, the EMI affects the system significantly due to the substrate coupling [11], which could considerably degrade the proper operation of the integrated antenna and circuits. In practice, it is desirable to use a ground plane between the silicon substrate and insulating layers (Fig. 1) to avoid EMI through the silicon substrate.

In this letter, a cavity-backed slot antenna is proposed to shield the wave from penetrating into the lossy substrate and also to block the wave traveling inside the insulator layers. Although the cavity height $h$ is only 9.6 $\mu$m (around $0.009\lambda_d$, where $\lambda_d$ is the wavelength in silicon dioxide inside the cavity), a good antenna gain is achieved. According to simulation results, the antenna performance could be rarely affected by the outer metals used by the circuitry if designed properly, which makes it a good candidate for an array element. A cavity was also proposed in [13] for a CMOS OCA design. However, the cavity was used to excite an external dielectric resonator antenna, which requires additional processes, and the radiation mechanism is different from the one described here.
Fig. 1. (a) Cross-section (lateral) view of CMOS chip environment with six metal layers over the silicon substrate. (b) Cross-section view of the cavity M1 as ground.

Fig. 2. Top view of the cavity and slot antenna fed by a microstrip.

The cavity is designed to resonate at its mode close to 140 GHz. Electric and magnetic fields inside the cavity have the expression \[ E_z = E_0 \sin \frac{\pi x}{a} \sin \frac{\pi y}{b} \quad H_z = \frac{j\pi E_0}{\omega \mu b} \sin \frac{\pi x}{a} \cos \frac{\pi y}{b}. \] (1)
In Fig. 3(c) and (d), the antenna input reflection coefficient and radiation efficiency are plotted versus frequency for different slot lengths. For slot length values \( L \) equal to 0.8 and 0.9 mm, much smaller than cavity length \( (a = 1.2 \text{ mm}) \), two resonances could be distinguished. The lower one is around 137 GHz, which is the resonant frequency of \( \text{TE}_{110} \) mode inside rectangular cavity [14], whereas the higher resonance mainly depends on the slot length \( L \). When \( L \) gets larger, the slot resonant frequency approaches the cavity one and a wider bandwidth is achieved. \( L \) is chosen as 1 mm for a tradeoff between bandwidth and gain at 140 GHz. It should also be noticed that at the cavity resonant frequency, a large amount of surface current is induced inside the inner boundary of cavity which results in high conduction losses, which degrades the antenna radiation efficiency at 137 GHz as shown in Fig. 3(c). This is the reason for the reflection coefficient notch around 137 GHz in Fig. 3(b).

We stress that the extreme flatness \( h = 9.6 \mu \text{m} \) of the cavity, constrained by the CMOS process, results in high losses. Indeed, it can be shown [14] that the power of the resonant \( \text{TE}_{110} \) mode lost in conduction losses is proportional to \( V^2 (\lambda_d / h)^2 \), where \( V = E_0 h \) is the potential difference between the bottom and top metals at the center of the cavity.

It should be noted that to satisfy the CMOS design rule related to metal density, \( 2 \times 2 \mu \text{m}^2 \) rectangular dummy holes are periodically bored on the top and bottom surfaces of the cavity, namely M6 and M1. Simulation results prove that as long as the holes are electrically small enough (in our case, \( 2 \times 2 \mu \text{m}^2 \)), the effect of these holes is negligible.

III. PARAMETRIC ANALYSIS

To understand how the performance is affected by the dimension of antenna parameters, key parametric analysis results are shown in this section.

Fig. 4 shows the broadside gain while varying the slot offset \( (D) \) to the center of the cavity in terms of different slot widths \( (W) \). The negative values of \( D \) indicate the slot is on the side of the microstrip feeding (at \( y < b/2 \) line), whereas “0” offset means the slot is exactly at the center of the cavity. As shown in Fig. 4, the peak gain is asymmetric when the slot is placed at opposite sides of the cavity. It can be explained by the fact that there are two different slot feeding mechanisms: 1) the direct feeding from microstrip, and 2) the \( \text{TE}_{110} \) mode of the cavity. Indeed, the feeding microstrip, besides exciting the slot, also excites the cavity, which in turn excites the slot. The cavity \( \text{TE}_{110} \) resonant mode has a magnetic field \( H_y \) field component as in (1), which has opposite signs for \( y \) larger or smaller than \( b/2 \). Correspondingly, the excited surface current on the inner part of the top side of the cavity has opposite directions at two sides of the cavity. Vice versa, the slot excitation from the microstrip does not change when placing the slot on either side of the cavity center (\( y = b/2 \)). Therefore, when the slot is placed at \( y > b/2 \), the radiation is enhanced since the two exciting mechanisms are constructive. Vice versa, when the slot is located at \( y < b/2 \), the two exciting mechanisms are destructive, which therefore weakens the antenna radiation. The same trend is observed for any slot widths considered.

Fig. 5 shows how the cavity size, location, and size of the slot affect the broadside gain of the antenna at 140 GHz. The results in the figures are obtained by varying two parameters each time while keeping the others as equal to the values mentioned in Section II. The final optimized dimension is indicated by small loops. Fig. 5(a) shows that the peak gain exists when the cavity size is around \( 1.2 \times 0.6 \text{ mm}^2 \). It should be noted from Fig. 5(a) that the gain could be increased to \(-1.8 \text{ dB}\) when cavity length is 1.3 mm, but the impedance bandwidth gets narrower in the case when the cavity gets longer. Fig. 5(b) and (c) shows that the gain reaches its peak while the length and width of the slot are around 1 mm and 20 \( \mu \text{m} \), respectively. These results verify that the slot and cavity is optimized in the 140-GHz frequency band.

IV. STABILITY ANALYSIS OF ANTENNA PERFORMANCE

The performance of an OCA is affected by the EMI between the antenna and its surroundings, which include the Si substrate, the silicon-dioxide layers, and the metallic parts in the circuit section, as for example shown in [11]. To relieve this problem, the cavity is used to shield the wave from traveling through the...
Fig. 6. (a) E- and H-plane gain pattern at 140 GHz with and without extra metal area (d = 2 mm) alongside the top metal layer of the antenna in the H-plane. (b) E- and H-plane gain pattern at 140 GHz with and without extra metal area (T = 2 mm) alongside the top metal layer of the antenna in the E-plane.

silicon-dioxide layers and substrate. This also renders the antenna performance not sensitive to the thickness and size of the Si substrate. To demonstrate how effectively this cavity-backed slot works, an extra metal piece shown in Fig. 6(a) is added in the top metal layer to somehow represent the metal used for circuits. This metal piece is placed alongside the slot antenna in the H-plane direction and shares the same width as the cavity. Fig. 6(a) shows the gain pattern in E- and H-planes at 140 GHz with and without the 2-mm-wide extra metal piece.

Comparing the patterns in Fig. 6(a), it is observed that the peak gain direction stays very close to the broadside direction (θ = 0°), with its value steady around −2 dB while the total radiation pattern is altered slightly. Next, the same examination is applied by placing the metal piece in the E-plane of the antenna as shown in Fig. 6(b). The simulation results in Fig. 6(b) show that: 1) the broadside gain does not change significantly; and 2) the gain pattern is changed moderately in the E plane, i.e., the direction of peak gain shifts when the area of the extra metal is increased. This suggests placing the circuit part of the chip in the H-plane direction. Anyway, though further studies should focus on this part of the research, these preliminary results seem to show that the EMI between antenna and circuit is significantly low.

V. CONCLUSION

This letter has introduced a design for a CMOS on-chip antenna with a cavity used to enhance the slot antenna radiation and shield the radiating section from the lossy silicon substrate. Despite the extreme flatness (thickness) of the cavity, constrained by the CMOS process, the antenna has 5-GHz input bandwidth around 140 GHz, 20-GHz gain bandwidth, and −2 dBi maximum gain. Considering that this antenna has a ground on M1, it exhibits good efficiency compared to previously published results. Furthermore, it has been shown the cavity-backed antenna is not significantly affected by the presence of nearby conductors. Results are confirmed by agreement between HFSS and CST simulations.

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