Design of a CMOS On-Chip Slot Antenna With Extremely Flat Cavity at 140 GHz

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***Abstract*—A novel design for a fully on-chip antenna operating at 140 GHz that can be fabricated with standard CMOS technology is proposed. In addition to the traditional microstrip feeding, the slot antenna is backed with an extremely thin cavity formed by two CMOS inner metal layers and vias in between. The proposed cavity prevents radiation from going inside the lossy silicon substrate and enhances the radiation of the slot antenna. It is also shown that the antenna radiation is not affected significantly by other metallic parts on the chip. Good agreement is achieved between results from a frequency-domain solver, HFSS, and a time-domain solver, CST. The simulated gain is around -2 dBi, and the radiation efficiency is around 18%, despite ohmic losses enhanced by the extreme flatness. The input 10-dB bandwidth is around 5 GHz. The total area of this antenna is 1.2×0.6 mm^2 ($0.56\lambda_0 \times 0.28\lambda_0$ at 140 GHz).**

***Index Terms*—Cavity, CMOS, millimeter wave (MMW), on-chip antenna (OCA), passive imaging, RFIC, slot antenna.**

I. Introduction

CMOS technology is considered an excellent platform for highly integrated operating at millimeter-wave (MMW) frequencies in terms of its low cost and weight. Various transceiver designs without integrated antennas have been implemented on single die using CMOS technology at MMWs [1], [2]. However, to achieve a fully integrated system, it is highly desirable to incorporate the antenna with the front-end circuit. With an integrated antenna, the system size could be shrunken to unprecedented levels, and on-chip antennas (OCAs) have been proposed to minimize antenna feed interconnection losses. It is interesting to note that MMW OCAs are useful even when they operate at a frequency much higher than the one in the CMOS active components—for example, when self-mixing or other circuit techniques are used [3], [4].

Antenna in package (AIP) is another viable solution for an integrated radiating system at millimeter waves. It provides more design flexibility and shows good performance, including high gain and wide bandwidth at 60 GHz [5]. In [6], 10% bandwidth and more than 80% radiation efficiency was achieved. However, OCA solutions need to be explored to realize a fully integrated radio on single chip and avoid transmission losses due to chip-to-package interconnections.

OCAs have already been designed based on dipole, folded dipole, slot, and inverted-F [7]–[9] with radiation off (orthogonal to) the chip. For most CMOS processes, the thickness between the topmost metal layer and bottom metal layer (h) is usually only around $5 \sim 15$ μm. Thus, to avoid very low radiation efficiency, the bottom metal layer is often not used as ground shielding between insulator layers and silicon substrate. However, this makes the antenna radiate mainly in the low resistivity silicon substrate, still resulting in extremely low antenna gains (i.e., low efficiency) at MMW frequencies. For example, the 140-GHz OCA implemented in 65-nm CMOS by [10] has a measured gain of only -25 dB. Besides the conduction and dielectric loss, the guided mode excited in high dielectric permittivity ($\varepsilon_r \approx 10$) silicon substrate [11] is the cause of another efficiency loss. The Yagi–Uda antenna structure in [12], which radiates in the lateral side direction of the chip, also shows low radiation efficiency. For future applications of MMW transceivers with OCAs, such as MMW imaging and multi-gigabit-per-second short-range wireless communications, it is strongly desirable to achieve high-efficiency antennas, which would lead to integrated transmitters and receivers with efficiency much higher than the current state of the art.

Another major concern in the integration of OCAs is the electromagnetic interference (EMI) resulting from mutual coupling between the antenna and the high-frequency front end. In OCA solutions, the antenna and circuit front end are utmost close to each other compared to other solutions (e.g., AIP and antenna out of package). Therefore, the EMI affects the system significantly due to the substrate coupling [11], which could considerably degrade the proper operation of the integrated antenna and circuits. In practice, it is desirable to use a ground plane between the silicon substrate and insulating layers (Fig. 1) to avoid EMI through the silicon substrate.

In this letter, a cavity-backed slot antenna is proposed to shield the wave from penetrating into the lossy substrate and also to block the wave traveling inside the insulator layers. Although the cavity height h is only 9.6 μm (around $0.009\lambda_d$, where λ_d is the wavelength in silicon dioxide inside the cavity), a good antenna gain is achieved. According to simulation results, the antenna performance could be rarely affected by the outer metals used by the circuitry if designed properly, which makes it a good candidate for an array element. A cavity was also proposed in [13] for a CMOS OCA design. However, the cavity was used to excite an *external* dielectric resonator antenna, which requires additional processes, and the radiation mechanism is different from the one described here.

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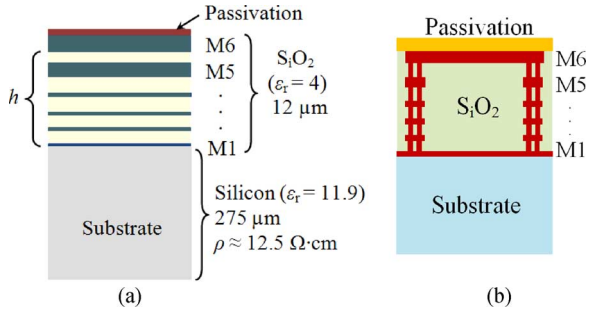

Fig. 1. (a) Cross-section (lateral) view of CMOS chip environment with six metal layers over the silicon substrate. (b) Cross-section view of the cavity M1 as ground.

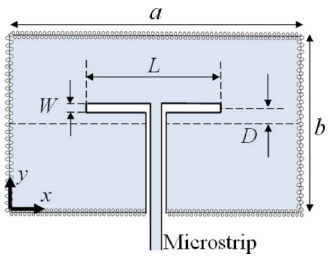

Fig. 2. Top view of the cavity and slot antenna fed by a microstrip.

Fig. 1 illustrates the side (lateral) view of a chip environment used in this letter. The total thickness from the top metal layer (M6) and bottom metal layer (M1) including metal layers is around 12 μm. The silicon substrate has the thickness of 275 μm with the dielectric constant of 11.9 and resistivity of 12.5 $\Omega \cdot$ cm. All realistic values of metal conductivity (3.39×0^7 S/m for M5~M6 and 2.34×10^7 S/m for M1~M4) are considered in the simulations.

II. On-Chip Antenna Configuration

Figs. 1(b) and 2 illustrate the proposed configuration for the on-chip cavity-backed slot antenna, which consists of a cavity, slot aperture, and a passivation layer, on top of a silicon substrate. The slot aperture is implemented on the top metal layer (M6). The cavity is formed by the lowest metal layer (M1) connected to the top metal layer (M6) through vias in between. Due to the limit on the minimal gap between adjacent vias, multiple layers of vias are realized to provide a good shielding for the cavity, as shown in Fig. 1(b). The antenna is fed from the edge of the cavity by a designed 50-Ω microstrip line with width 14 μm on M6. It should be noted that the transmission-line structure in the cavity side mainly functions as a microstrip line instead of a grounded coplanar waveguide (G-CPW) since h is less than half of the gap (16 μm) between the center and side metals at M6. The slot is excited by the microstrip line and also by the back cavity. The cavity, besides interacting with the slot, is also excited by the field of the microstrip.

The cavity is designed to resonate at its TE_{110} mode close to 140 GHz. Electric and magnetic fields inside the cavity have the expression [14]

$$E_z = E_0 \sin\frac{\pi x}{a} \sin\frac{\pi y}{b} \quad H_x = \frac{j\pi E_0}{\omega\mu b} \sin\frac{\pi x}{a} \cos\frac{\pi y}{b}. \quad (1)$$

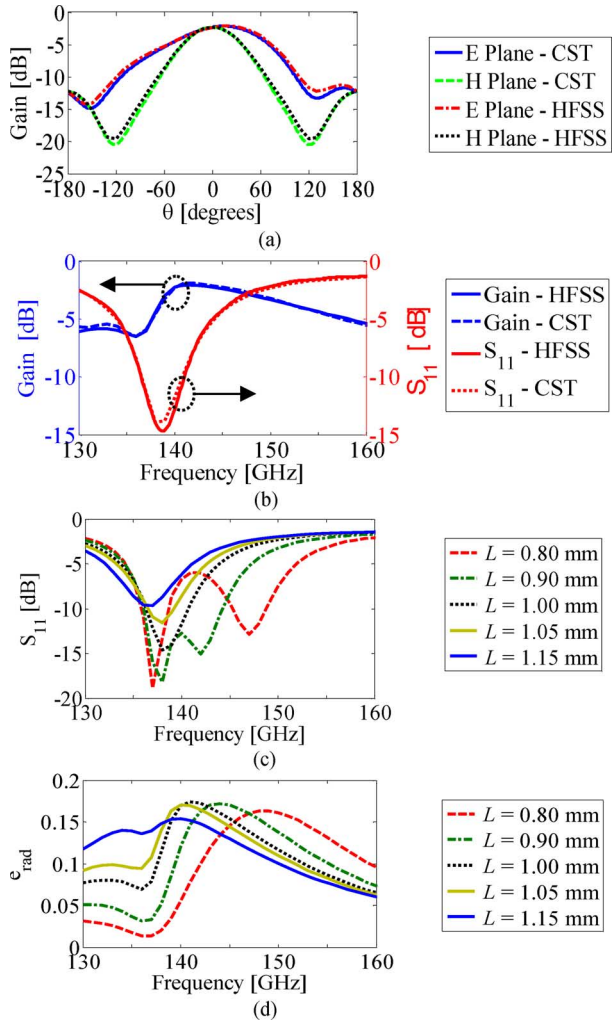

Fig. 3. (a) Comparison of simulated gain results of the cavity-backed slot antenna along the E and H-planes at 140 GHz. Results from CST and HFSS are in good agreement. (b) Input reflection coefficient (S_{11}) and broadside gain versus frequency. (c), (d) S_{11} and radiation efficiency versus frequency for different slot lengths.

Note that the magnetic field H_x has opposite signs for y larger or smaller than $b/2$, and this affects the excitation of the slot. The slot is designed and optimized in terms of gain and impedance bandwidth. The width and length of the cavity, the slot width and length, and the slot offset to the center of the cavity are respectively $a = 1.2$ mm ($= 0.56\lambda_0$ at 140 GHz), $b = 0.6$ mm ($= 0.28\lambda_0$), $W = 20$ μm, $L = 1$ mm, and $D = 10$ μm.

Fig. 3(a) and (b) shows the simulated gain along the E and H-planes and the input reflection coefficient of the optimized antenna. Results have been obtained from two different full-wave solvers, HFSS and CST, which are in good agreement. The operating frequency is 140 GHz, and the input 10-dB bandwidth is larger than 5 GHz. The maximum gain of the antenna at broadside ($\theta = 0°$) is -2 dBi, which is significant for an antenna over a ground plane that is only 9.6 μm thick. Fig. 3(b) shows the simulated gain versus frequency of the antenna. The peak appears around 140 GHz, and the 3-dB gain bandwidth is from 136 to 156 GHz, which allows for gigabit-per-second communication data rates at MMW frequencies. The extremely low thickness is the major limitation for obtaining larger bandwidth.

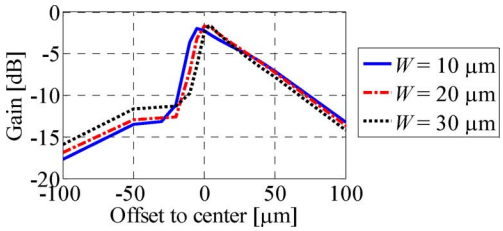

Fig. 4. Broadside gain at 140 GHz versus offset of slot to the center of cavity (D) for various slot widths (W).

In Fig. 3(c) and (d), the antenna input reflection coefficient and radiation efficiency are plotted versus frequency for different slot lengths. For slot length values L equal to 0.8 and 0.9 mm, much smaller than cavity length ($a = 1.2$ mm), two resonances could be distinguished. The lower one is around 137 GHz, which is the resonant frequency of TE_{110} mode inside rectangular cavity [14], whereas the higher resonance mainly depends on the slot length L. When L gets larger, the slot resonant frequency approaches the cavity one and a wider bandwidth is achieved. L is chosen as 1 mm for a tradeoff between bandwidth and gain at 140 GHz. It should also be noticed that at the cavity resonant frequency, a large amount of surface current is induced inside the inner boundary of cavity which results in high conduction losses, which degrades the antenna radiation efficiency at 137 GHz as shown in Fig. 3(c). This is the reason for the reflection coefficient notch around 137 GHz in Fig. 3(b). We stress that the extreme flatness $h = 9.6$ μm of the cavity, constrained by the CMOS process, results in high losses. Indeed, it can be shown [14] that the power of the resonant TE_{110} mode lost in conduction losses is proportional to $V^2(\lambda_d/h)^2$, where $V = E_0 h$ is the potential difference between the bottom and top metals at the center of the cavity.

It should be noted that to satisfy the CMOS design rule related to metal density, 2×2 μm^2 rectangular dummy holes are periodically bored on the top and bottom surfaces of the cavity, namely M6 and M1. Simulation results prove that as long as the holes are electrically small enough (in our case, 2×2 μm^2), the effect of these holes is negligible.

III. Parametric Analysis

To understand how the performance is affected by the dimension of antenna parameters, key parametric analysis results are shown in this section.

Fig. 4 shows the broadside gain while varying the slot offset (D) to the center of the cavity in terms of different slot widths (W). The negative values of D indicate the slot is on the side of the microstrip feeding (at $y < b/2$) line, whereas "0" offset means the slot is exactly at the center of the cavity. As shown in Fig. 4, the peak gain is asymmetric when the slot is placed at opposite sides of the cavity. It can be explained by the fact that there are two different slot feeding mechanisms: 1) the direct feeding from microstrip, and 2) the TE_{110} mode of the cavity. Indeed, the feeding microstrip, besides exciting the slot, also excites the cavity, which in turn excites the slot. The cavity TE_{110} resonant mode has a magnetic field H_x field component as in (1), which has opposite signs for y larger or smaller than $b/2$. Correspondingly, the excited surface current on the inner part of the top side of the cavity has opposite directions at two sides of the cavity. Vice versa, the slot excitation from the microstrip does not change when placing the slot on either side of the cavity center ($y = b/2$). Therefore, when the slot is placed at $y > b/2$, the radiation is enhanced since the two exciting mechanisms are constructive. Vice versa, when the slot is located at $y < b/2$, the two exciting mechanisms are destructive, which therefore weakens the antenna radiation. The same trend is observed for any slot widths considered.

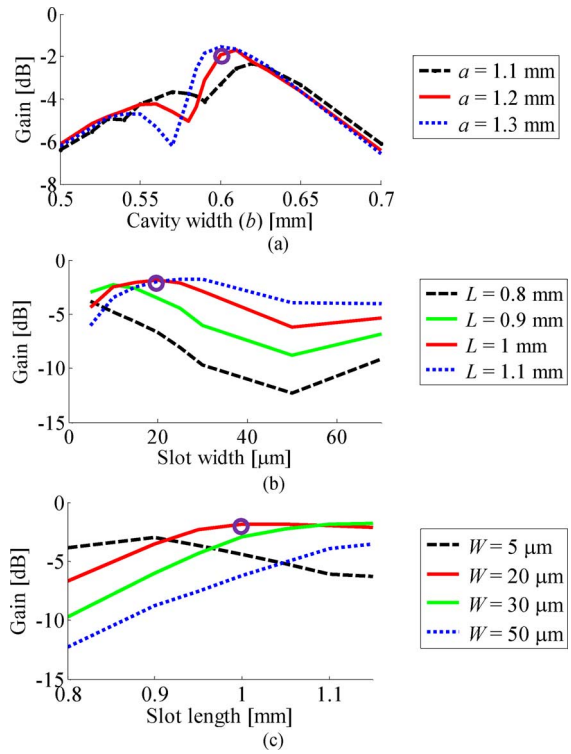

Fig. 5. Broadside gain at 140 GHz versus (a) width of the cavity for different cavity lengths, (b) slot width for different slot lengths, and (c) slot length for different slot widths.

Fig. 5 shows how the cavity size, location, and size of the slot affect the broadside gain of the antenna at 140 GHz. The results in the figures are obtained by varying two parameters each time while keeping the others as equal to the values mentioned in Section II. The final optimized dimension is indicated by small loops. Fig. 5(a) shows that the peak gain exists when the cavity size is around 1.2×0.6 mm^2. It should be noted from Fig. 5(a) that the gain could be increased to -1.8 dB when cavity length is 1.3 mm, but the impedance bandwidth gets narrower in the case when the cavity gets longer. Fig. 5(b) and (c) shows that the gain reaches its peak while the length and width of the slot are around 1 mm and 20 μm, respectively. These results verify that the slot and cavity is optimized in the 140-GHz frequency band.

IV. Stability Analysis of Antenna Performance

The performance of an OCA is affected by the EMI between the antenna and its surroundings, which include the Si substrate, the silicon-dioxide layers, and the metallic parts in the circuit section, as for example shown in [11]. To relieve this problem, the cavity is used to shield the wave from traveling through the

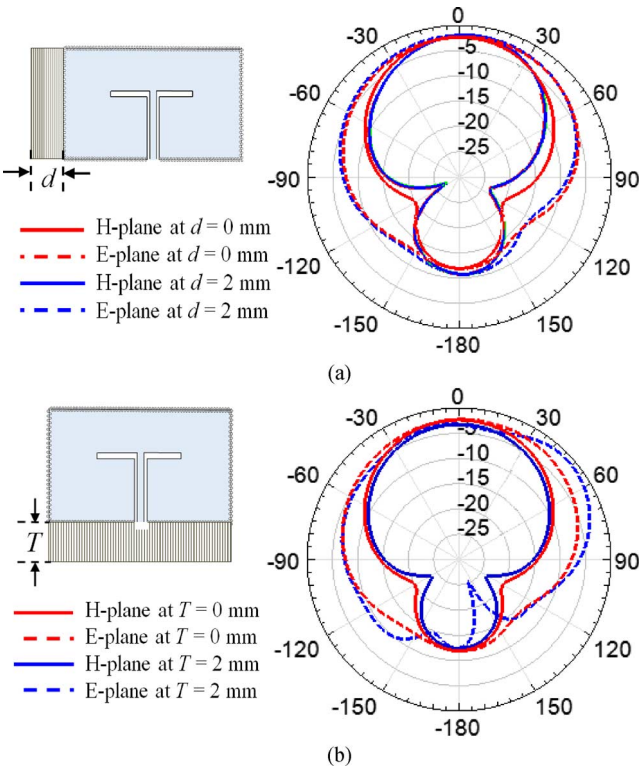

Fig. 6. (a) E- and H-plane gain pattern at 140 GHz with and without extra metal area ($d = 2$ mm) alongside the top metal layer of the antenna in the H-plane. (b) E- and H-plane gain pattern at 140 GHz with and without extra metal area ($T = 2$ mm) alongside the top metal layer of the antenna in the E-plane.

silicon-dioxide layers and substrate. This also renders the antenna performance not sensitive to the thickness and size of the Si substrate. To demonstrate how effectively this cavity-backed slot works, an extra metal piece shown in Fig. 6(a) is added in the top metal layer to somehow represent the metal used for circuits. This metal piece is placed alongside the slot antenna in the H-plane direction and shares the same width as the cavity. Fig. 6(a) shows the gain pattern in E- and H-planes at 140 GHz with and without the 2-mm-wide extra metal piece.

Comparing the patterns in Fig. 6(a), it is observed that the peak gain direction stays very close to the broadside direction ($\theta = 0°$), with its value steady around -2 dB while the total radiation pattern is altered slightly. Next, the same examination is applied by placing the metal piece in the E-plane of the antenna as shown in Fig. 6(b). The simulation results in Fig. 6(b) show that: 1) the broadside gain does not change significantly; and 2) the gain pattern is changed moderately in the E plane, i.e., the direction of peak gain shifts when the area of the extra metal is increased. This suggests placing the circuit part of the chip in the H-plane direction. Anyway, though further studies should focus on this part of the research, these preliminary results seem to show that the EMI between antenna and circuit is significantly low.

V. Conclusion

This letter has introduced a design for a CMOS on-chip antenna with a cavity used to enhance the slot antenna radiation and shield the radiating section from the lossy silicon substrate. Despite the extreme flatness (thickness) of the cavity, constrained by the CMOS process, the antenna has 5-GHz input bandwidth around 140 GHz, 20-GHz gain bandwidth, and -2 dBi maximum gain. Considering that this antenna has a ground on M1, it exhibits good efficiency compared to previously published results. Furthermore, it has been shown the cavity-backed antenna is not significantly affected by the presence of nearby conductors. Results are confirmed by agreement between HFSS and CST simulations.

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