UC Santa Barbara

UC Santa Barbara Electronic Theses and Dissertations

Title

III-Nitride Vertical-Cavity Surface-Emitting Lasers: Growth, Fabrication, and Design of Dual Dielectric DBR Nonpolar VCSELs

Permalink

https://escholarship.org/uc/item/0js053zj

Author

Leonard, John Thomas

Publication Date

2016

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA

Santa Barbara

III-Nitride

Vertical-Cavity Surface-Emitting Lasers

Growth, Fabrication, and Design of Dual Dielectric DBR Nonpolar VCSELs

A dissertation submitted in partial satisfaction of the requirements for the degree

Doctor of Philosophy

in

Materials

by

John T. Leonard

Committee in charge:

Professor Shuji Nakamura, Chair
Professor James S. Speck
Professor Steven P. DenBaars
Professor Jon Schuller

March 2016

The dissertation of John T. Leonard is approved.

_____

James S. Speck

_____

Steven P. DenBaars

_____

Jon Schuller

_____

Shuji Nakamura (Committee Chair)

March 2016

III-Nitride

Vertical-Cavity Surface-Emitting Lasers

Growth, Fabrication, and Design of Dual Dielectric DBR Nonpolar VCSELs

Copyright © 2016

by

John T. Leonard

To my parents, my siblings, and Kate;

for inspiring me to be creative in all aspects of life

Acknowledgements

There are so many people I owe my good fortune to. In terms of my academic growth, I would like to start by thanking my Father for suggesting to go into the field of Materials Science as an undergraduate student at North Carolina State University (NCSU). Studying the fundamental concepts about materials science taught me so many interesting and illuminating things about the sub-atomic, atomic, nano-, and micro- world around us. I would also like to thank Prof. Jon-Paul Maria and his graduate students at NCSU for introducing me to inorganic electronic materials, and the procedures and research tools used in fabricating thin-films. Through my experience in Prof. Maria's group, I was able to find an internship in Dr. Biwu Ma's group at Lawrence Berkeley National Lab (LBNL). I am very grateful to Dr. Ma and his group for giving the opportunity to learn more about organic electronics, photovoltaics in particular. While at LBNL I saw a visiting researcher testing the OLEDs he was working on. When I saw the OLED light up, I realized that testing and studying light emitters was where my interest really lay, partly because I just loved how visually rewarding testing a light emitter was. Upon apply to graduate school, Dr. Maria and a number of other professors at NCSU, submitted many very kind recommendation letters for me. As my GPA was nothing special and my GRE scores weren't too good either, these recommendation letters from people who truly believed in my potential were particularly important to me. Fortunately, I was accepted to UC Santa Barbara, where Prof. Shuji Nakamura kindly allowed me to join his group.

I am especially grateful to Prof. Nakamura for putting me on the III-nitride VCSELs project before my first year of graduate school even started. I initially hoped that I would

work on LEDs, as they were much easier to understand, but by working on VCSELs I have gained such a deep appreciation for the fundamental nature of light and its interaction with materials. The complexity of VCSELs has allowed me to discover new and interesting things day after day. Beyond this, I am also grateful to Prof. Nakamura, Prof. Steve DenBaars, and Prof. Jim Speck for advising me in a very trusting manner, allowing me to freely pursue the VCSEL project goals that I found to be most interesting and important. Furthermore, I am thankful to them for believe in my ability to get the nonpolar VCSELs working reliably, because there were essentially two years where the project produced no new results, and similar III-nitride VCSEL projects had been canceled in the past. Beyond my PI advisors, I would also like to thank Dr. Dan Cohen for assisting in advising me, and for be a great knowledgeable, critical, and insightful collaborator. Dan has spent many hours helping to edit my publications and his questioning comments greatly improved the quality of my publications while simultaneously encouraging me to understand the fundamental concepts underlying VCSEL performance. I would also like to thank Dr. Bob Farrell who spent a great deal of time guiding me through the process of writing my first paper, and who was always very generous with his time in meeting one-on-one with people, and leading group meetings generally. Additionally, I would like to thank Dr. Tal Margalith for assisting in running group meetings and making strong efforts to encourage graduate students in the group to present research updates more frequently. Many thanks are also to Dr. Erin Young. Erin and I did not collaborate for much of my PhD career, but one time we were both testing devices in the same room and she mentioned that she had been working on MBE tunnel junctions. She kindly agreed to try growing such tunnel junctions on a VCSEL, leading to a real breakthrough in my graduate work and the III-nitride VCSELs field generally.

Besides the advising and collaborations from the professors and staff scientists at UCSB, I am also extremely thankful for the great collaboration and discussions with the III-nitrides group as a whole. In particular, my discussions with Ben Yonkee about a plethora of research topics, technical challenges, and general ideas truly enhanced my understanding of III-nitrides and light emitters generally. Ben's deep understanding of fundamental semiconductor physics brought a great deal of technical insight to my work. Furthermore, I am thankful to Ben, and Justin Iveland, for being great office mates and friends overall. Our discussions on research, technology in general, and the woes and oddities of graduate student life were always enjoyable.

Beyond my office mates, I would like to thank Seunggeun Lee and Charles Forman for their diligent self-motivated attitude while being trained by me. I have always felt that some things are best learned by simply doing them yourself, and it can sometimes be difficult to encourage new students to have this mentality if they are not self-motivated. However, Charles and Seunggeun, who worked with me on a number of projects, including the UV VCSEL project and violet VCSEL project, were always willing to go try things on their own. I am especially thankful to Charles for taking over my III-nitrides VCSEL project upon my graduation. Because I was so invested in writing this thesis in the last several months of my graduate school carrier, I was unable to offer much in-person, in-lab training to him on the project, yet he has enthusiastically taken over the project without the need for much in-person guidance.

Outside of my academic work at UCSB, I am deeply humbled by Dr. Dan Haegar's kind recommendation for an internship at Apple working on display technology. I only worked with Dan during my first year at UCSB, yet he believed in my potential, and

essentially opened up one of the best possible career paths I could have hoped to obtain out of graduate school. My internship at Apple truly changed my life and made me realize what specific field I wanted to focus on after I graduated. I am grateful to all the team members I worked with at Apple, however I am particularly grateful to Dr. Dmitry Sizov, who spent a great deal of his busy schedule to get me up to speed and help me understand the project I was working on. I am also grateful to my manager at Apple, Dr. Jean-Jacques Drolet, who was always enthusiastically happy, insightful, and genuinely interested in whether or not I was having fun doing my internship.

Though these acknowledgments to all the people who have aided my technical career and development are certainly valuable, of equal value are those outside my technical career who have influenced my life more generally. First, I would like to thank my close friends Riley Zecca, Anuraag Pendyal, and Ricky Serrano, who have brought so many great memories to my life. Such good friends are hard to find, and they have deeply influence my perception of the world and helped me appreciate many concepts outside my core technical field, including philosophy, music, literature, world culture, and more.

Last, but certainly not least, I am so grateful for my immediate and extended family. When I was young my parents introduced me to so much wonder in the world through science fiction shows, such as star-trek, and educational and informative shows, such as NOVA and NPR. These deeply influenced my passion for learning and understanding how the universe and world works on a fundamental level, and led me to the fields of engineering and science. Their belief in me, despite my lack of strong literary skills (I almost failed several end-of-grade exams) and arithmetic skills (I could never remember my times-tables and nearly failed geometry), helped me to have confidence that I could pursue whatever

field I was interested in. In the end, I have found that failing and struggling so much at an early age has taught me more than continually succeeded and easily understanding things would have, as it gave me a sense of perseverance and fearlessness that I could overcome any obstacle if I simply worked hard enough. Beyond these lessons, my mother in particular, has instilled a deep sense of creativity in my life by encouraging me to be artistic at a young age. I continue to enjoy creating art to this day, but I also feel that this creativity has overflown to my technical career. Beyond artistic ability, I am grateful to my father for giving me an appreciation for the value of continual learning and education. Besides my parents, I am grateful to my siblings, Braden, Kendal, and Katie, for always being there for me and for being loving in general, despite our sometimes overly competitive natures. Finally, I would like to thank my girlfriend, Kate Gable, and her family. Kate has brought so much happiness to my life and has kept me from becoming too much of a workaholic. Kate has been so selfless in moving with me to California from North Carolina, and then to San Jose for my Apple internship, and I am deeply thankful for her sacrifices. Furthermore, Kate has filled my life with so much new music, fashion, and fun generally, making me a more well-rounded individual. Beyond Kate herself, her family has been such a joy to be around and they have been so generous in their support of me throughout the years.

In all, I am only who I am today and I am only at this place in my career today, because of the generosity of so many people around me. I have truly been blessed with good fortune to have so many kind and selfless people come into my life. Words cannot express the immense gratitude I feel for all those who have believed in me. My hope is that my life will bring me the opportunity to reciprocate the generosity others have shown me, so that I may make a meaningful contribution to the advancement of the quality of life for humanity.

Curriculum Vitae

John T. Leonard, Ph.D.

March 2016

Fundamental Motivation & Interests

I love solving complex technological problems to improve the quality of life for humanity

My primary technical field of interest is display & sensor technology. My other general fields of interests include technology management, robotics, artificial intelligence, transhumanism, interplanetary space travel, and finance.

Personal Information

Email: jtleona01@gmail.com
LinkedIn: https://www.linkedin.com/in/JohnTLeonard
Twitter: https://twitter.com/1JohnLeonard1
Google Scholar: https://scholar.google.com/citations?hl=en&user=R4TDG8sAAAAJ

Education & Experience

University of California, Santa Barbara (UCSB)
        Ph.D., Materials Science   Aug. 2012 –Mar. 2016
          III-Nitride Vertical-Cavity Surface-Emitting Lasers (VCSELs)
            Advisors: Shuji Nakamura, James S. Speck, Steven P. DenBaars
            Staff Scientists: Daniel A. Cohen, Erin C. Young, Robert M. Farrell, Tal Margalith
        Additional Study: Technology Management
Apple, Hardware, Display Technology
        Graduate student Intern   Jul. 2015–Mar. 2015
          Manager: Jean-Jacques Drolet
          Primary Supervisor: Dmitry Sizov
North Carolina State University (NCSU)
        B.S., Material Science (major), Physics (minor)   Aug. 2008–May 2012
        Undergraduate Student Researcher   Oct. 2009–Jun. 2012
          Transparent Conductive Oxides (TCOs)
            Advisor: Jon-Paul Maria
Lawrence Berkeley National Lab (LBNL)
        Undergraduate Student Intern   Jun. 2011–Aug. 2011
          Organic Photovoltaics
            Advisor: Biwu Ma
            Supervisors: Teresa Chen, Sibel Leblebici

Software & Modeling Skills

LabView, Mathematica, Matlab, SiLENSe, Waveguide optics modeling, SRIM/TRIM (ion implantation simulation), COMSOL, FIMMWAVE, Microsoft Office, Adobe Suite

Materials Fabrication Techniques

Metal-organic chemical-vapor deposition (MOCVD), ion beam deposition (IBD), RF/DC sputtering, pulsed laser deposition (PLD), thermal/e-beam evaporation, photolithography, photoelectrochemical (PEC) etching, plasma-enhanced chemical vapor deposition (PECVD), reactive-ion etching (RIE), ion-coupled plasma (ICP), dicing saws, chemical-mechanical polishing, flip-chip bonding.

Materials Characterization Techniques

Photoluminescence, SEM, AFM, profilometry, UV-Vis spectroscopy, XRD, 4-pt probe, LIV characterization (pulsed & DC), ellipsometry, Hall test, laser scanning confocal microscopy, general vacuum system construction/maintenance

General Interests/Activities
Learning
Drawing & digital media
Strategy video games
Building things
Hiking

Honors & Awards
SSLEEC Outstanding Researcher Award   2015
Summa Cum Laude   2012
NSF GRFP Honorable Mention   2012
American Ceramic Society (ACerS) Hoffman Scholarship   2011
Society of Plastics Engineers (SPE) Senior Scholarship   2011
MSE Engineers' Council Representative   2011
Dr. Robert Stoops Scholarship (NCSU MSE Scholarship)   2010
MSE Freshman Scholarship   2008
5th in NC High School Wrestling State Championship   2008
2nd in NC Freestyle Wrestling State Championship   2007

Publications

- **J. T. Leonard**, E. C. Young, B. P. Yonkee, D. A. Cohen, C. Shen, T. Margalith, T. K. Ng, S. P. DenBaars, B. S. Ooi, J. S. Speck, S. Nakamura, "Comparison of Nonpolar III-nitride Vertical-Cavity Surface-Emitting Lasers with Tunnel Junction and ITO Intracavity Contacts," *Proc. SPIE Gall. Nitride Mater. Devices XI*, 2016.
- **J. T. Leonard**, B. P. Yonkee, D. A. Cohen, L. Megalini, S. Lee, J. S. Speck, S. P. DenBaars, and S. Nakamura, "Nonpolar III-Nitride Vertical-Cavity Surface-Emitting Laser with a Photoelectrochemically Etched Air-Gap Aperture," Appl. Phys. Lett., vol. 108, p. 031111, 2016.
- **J. T. Leonard**, E. C. Young, B. P. Yonkee, D. A. Cohen, T. Margalith, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Demonstration of a III-nitride vertical-cavity surface-emitting laser with a III-nitride tunnel junction intracavity contact," Appl. Phys. Lett., vol. 107, no. 9, p. 091105, 2015.
- **J. T. Leonard**, D. A. Cohen, B. P. Yonkee, R. M. Farrell, T. Margalith, S. Lee, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Nonpolar III-Nitride Vertical-Cavity Surface-Emitting Lasers Incorporating an Ion Implanted Aperture," Appl. Phys. Lett., vol. 107, p. 011102, 2015.
- **J. T. Leonard**, D. A. Cohen, B. P. Yonkee, R. M. Farrell, S. P. Denbaars, J. S. Speck, and S. Nakamura, "Smooth e-beam-deposited tin-doped indium oxide for III-nitride vertical-cavity surface-emitting laser intracavity contacts," J. Appl. Phys., vol. 118, p. 145304, 2015.
- C. O. Holder, **J. T. Leonard (Corresponding Author)**, R. M. Farrell, D. A. Cohen, B. Yonkee, J. S. Speck, S. P. DenBaars, S. Nakamura, and D. F. Feezell, "Nonpolar III-nitride vertical-cavity surface emitting lasers with a polarization ratio of 100% fabricated using photoelectrochemical etching," Appl. Phys. Lett., vol. 105, no. 3, p. 031111, 2014.
- S. Mishkat-Ul-Masabih, **J. T. Leonard**, D. A. Cohen, S. Nakamura, and D. F. Feezell, "Thermal analysis of flip-chip GaN-based VCSELs with dielectric distributed Bragg reflectors," IEEE Photonics Technol. Lett., Under Review.
- C. Shen, T. K. Ng, **J. T. Leonard**, A. Pourhashemi, H. Oubei, B. Alias, M. Sharizal, S. Nakamura, S. DenBaars, J. S. Speck, A. Ahmed, E. Munir, and B. S. Ooi, "High-modulation-efficiency, integrated waveguide modulator-laser diode at 448 nm," ACS Photonics, Under Review.
- B. P. Yonkee, R. M. Farrell, **J. T. Leonard**, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Demonstration of low resistance Ohmic contacts to p-type (2021) GaN," Semicond. Sci. Technol., vol. 30, no. 7, p. 075007, 2015.
- L. Megalini, L. Y. Kuritzky, **J. T. Leonard**, R. Shenoy, K. Rose, S. Nakamura, J. S. Speck, D. A. Cohen, and S. P. Denbaars, "Selective and controllable lateral photoelectrochemical etching of nonpolar and semipolar InGaN/GaN multiple quantum well active regions," Appl. Phys. Express, vol. 8, p. 066502, 2015.
- B. P. Yonkee, E. C. Young, C. Lee, **J. T. Leonard**, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Demonstration of a III-nitride edge-emitting laser diode utilizing a GaN tunnel junction contact," Opt. Express, Under Review, 2016.
- N. A. Estrich, D. H. Hook, A. N. Smith, **J. T. Leonard**, B. Laughlin, and J.-P. Maria, "Ga-doped ZnO conducting

antireflection coatings for crystalline silicon solar cells," *J. Appl. Phys.*, vol. 113, no. 23, p. 233703, 2013.

Conferences

- **J. T. Leonard**, E. C. Young, B. P. Yonkee, D. A. Cohen, C. Shen, T. Margalith, T. K. Ng, S. P. DenBaars, B. S. Ooi, J. S. Speck, S. Nakamura, "Comparison of Nonpolar III-nitride Vertical-Cavity Surface-Emitting Lasers with Tunnel Junction and ITO Intracavity Contacts," SPIE Photonics West (SPIE OPTO), 2016
- **J. T. Leonard**, D. A. Cohen , B. P. Yonkee, R. M. Farrell, T. Margalith ,S. Lee, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Nonpolar III-Nitride Vertical-Cavity Surface-Emitting Lasers Incorporating an Ion Implanted Current Aperture," Compound Semiconductor Week (CSW), 2015.
- **J. T. Leonard**, C. O. Holder, R. M. Farrell, D. A. Cohen, B. Yonkee, J. S. Speck, S. P. DenBaars, S. Nakamura, and D. F. Feezell, "100% Polarization Locked Nonpolar III-Nitride Vertical-Cavity Surface Emitting Lasers Fabricated Using Photoelectrochemical Etching Techniques,"56th Annual Electronic Material Conference (EMC), 2014.
- C. Shen, **J. T. Leonard**, A. Pourhashemi, H. Oubei, M. S. Alias, T. Khee, S. Nakamura, S. P. Denbaars, J. S. Speck, A. Y. Alyamani, M. Munir, and B. S. Ooi, "Low Modulation Bias InGaN-based Integrated EA- Modulator-Laser on Semipolar GaN Substrate," in Photonics Conference (IPC), 2015, vol. 4, pp. 581–582.
- B. P. Yonkee, E. C. Young, **J. T. Leonard**, C. Lee, S. H. Oh, S. P. DenBaars, J. S. Speck, S. Nakamura, "Hybrid MOCVD/MBE GaN Tunnel Junctions," 11th International Conference on Nitride Semiconductors, 2015
- B. P. Yonkee, E. C. Young, **J. T. Leonard**, C. Lee, S. H. Oh, J. S. Speck, S. Nakamura, "Hybrid MOCVD/MBE GaN Tunnel Junctions," 6th International Symposium on Growth of III-Nitrides, 2015
- E. C. Young, B. P. Yonkee, **J. T. Leonard**, F. Wu, S. P. DenBaars, S. Nakamura, J. S. Speck, "Ammonia molecular beam epitaxy technology for UV light emitters," Summer Topicals Meeting Series (SUM), 2015.
- B. P. Yonkee, B. Saifaddin, **J. T. Leonard**, J. S. Speck, S. P. DenBaars, S. Nakamura, "Flip Chip Blue (20-21) GaN LEDs Using Photoelectrochemical Etching for Substrate Removal," Compound Semiconductor Week (CSW), 2015.

Patents

- E. C. Young, B. P. Yonkee, **J. T. Leonard**, T. Margalith, J. S. Speck, S. P. DenBaars, S. Nakamura, "Hybrid Growth Method for III-Nitride Tunnel Junction Devices." Docket 30784.588-US-P1. Prepared by Gates & Cooper LLP, Jul. 2015.
- E. C. Young, B. P. Yonkee, **J. T. Leonard**, T. Margalith, J. S. Speck, S. P. DenBaars, S. Nakamura, "III-Nitride tunnel junction with modified p-n interface," UC Case #2016-245. Prepared by Gates & Cooper LLP, Nov. 2015.
- D. A. Cohen, **J. T. Leonard**, L. Megalini, S. P. DenBaars, S. Nakamura, "Group III-N Laser with Transparent Conducting Oxide Cladding". Docket 30794.585-US-P1. Prepared by Gates & Cooper LLP, Dec. 2014.
- **J. T. Leonard**, D. A. Cohen, S. P. DenBaars, J. S. Speck, S. Nakamura, "Control of Morphological and Optoelectronic Characteristics of Transparent Conductive Oxides Using Multi-Layer Physical Evaporation Techniques," Docket 30794.569-US-P1**,** Prepared by Gates & Cooper LLP, Aug. 2014.

Press Releases/Magazine Articles

- M. Cooke, "Tunnel junction for vertical-cavity surface-emitting laser," Semiconductor Today, 2015.
  http://www.semiconductor-today.com/news_items/2015/sep/ucsb_220915.shtml
- M. Cooke, "Lowering threshold currents for m-plane III-nitride VCSELs," Semiconductor Today, 2015.
  http://www.semiconductor-today.com/news_items/2015/jul/ucsb_290715.shtml
- AIP News Staff, "New deposition technique enhances optoelectronic properties of lasers", AIP Publishing, 2015.
  https://www.aip.org/publishing/journal-highlights/new-deposition-technique-enhances-optoelectronic-properties-lasers
- M. Cooke, "Photo-electro-chemical etch & vertical-cavity laser diodes", Semiconductor Today, 2014.
  http://www.semiconductor-today.com/news_items/2014/AUG/UCSB-2_180814.shtml

Ph.D. Program Technical Accomplishments

- Demonstrated the first III-nitride tunnel junction VCSEL
- Demonstrated the first III-nitride ion implanted aperture VCSEL
- Improved UCSB VCSEL performance from ~100 kA/cm^2 to ~3 kA/cm^2 threshold current densities
- Built over 10 LabView programs for device characterization used by all III-nitrides research group members
  - Designed automated Excel report generation for improved data collection & analysis
- Designed over 100 MOCVD growth recipes for VCSELs, edge-emitting lasers, and LEDs
- Designed over 5 fabrication process flows
- Designed over 5 lithography mask layouts
- Carried out over 100 electrical and optical VCSEL simulations
- Carried out flip-chip VCSEL fabrication on a regular basis
  - Processed VCSELs with different process flows in parallel to maximize results
- Selected as reviewer for 3 publications
- Trained 2 incoming graduate students
- Graduated in less than 4 years

Independent Technical Courses & Reading

- Display & Sensor technology
  - R. R. Hainich and O. Bimber, *Displays, Fundamentals & Applications*. Boca Raton, FA: CRC Press LLC, 2011.
  - R. Lyon, et. al, *Google Photo Tech Edu,* Google Tech. Talks, 2007. [PhotoTech Edu YouTube Playlist](#)
  - S. Greengard, *The Internet of Things: The MIT Press Essential Knowledge Series*, MIT Press, 2015.
- Management & Business
  - E. Schmidt, J. Rosenberg, *How Google Works*, Grand Central Publishing, 2014.
  - W. Isaacson, *Steve Jobs*, Simon & Schuster Publishing, 2015.
  - A. Vance, *Elon Musk: Tesla, SpaceX, and the Quest for a Fantastic Future*, Ecco Publish, 2015.
  - J. Sutherland, *Scrum: The Art of Doing Twice the Work in Half the Time,* Crown Business, 2014.
  - M. Buckingham, C. Coffman, *First, Break All the Rules: What the World's Greatest Managers Do Differently*, Simon & Schuster Publishing, 1999.
  - J. Collins, *Good to Great: Why Some Companies Make the Leap...And Others Don't*, Harper Business, 2001.
  - P. Thiel, B. Masters, *Zero to One: Notes on Startups, or How to Build the Future,* Crown Business,2014.
  - J. R. Hackman, *Collaborative Intelligence: Using Teams to Solve Hard Problems*, Berrett-Koehler Publishers, 2011.
  - D. Kahneman, *Thinking, Fast and Slow,* Farrar, Straus and Giroux Publishing, 2013.
  - S. R. Covey, *The 7 Habits of Highly Effective People: Powerful Lessons in Personal Change,* Simon & Schuster, 2013.
  - K. Schulz, *Being Wrong : Adventures in the Margin of Error,* Ecco / HarperCollins, 2010.
  - B. Fitzpatrick, B. Collins-Sussman, *Team Geek: A Software Developer's Guide to Working Well with Others*, O'Reilly Media, 2012.
  - F. B. Cross, *Business Law: Contracts*, The Great Courses, Course No. 561.
  - F. B. Cross, *Business Law: Negligence and Torts,* The Great Courses, Course No. 562
  - M. A. Roberto, *The Art of Critical Decision Making,* The Great Courses, Course No. 5932.
  - J. Kaufman, *The Personal MBA: Master the Art of Business,* Portfolio, 2012.
- Robotics, Artificial Intelligence, & Virtual Reality
  - M. Rothblatt, *Virtually Human: The Promise and The Peril of Digital Immortality,* St. Martin's Press, 2014.
  - R. Kurzweil, *The Singularity Is Near: When Humans Transcend Biology,* Penguin Books,2006.
  - R. Kurzweil, *How to Create a Mind: The Secret of Human Thought Revealed*, Penguin Books, 2013.
  - N. Bostrom, *Superintelligence: Paths, Dangers, Strategies*, Oxford University Press, 2014
  - P. W. Singer, *Wired for War: The Robotics Revolution and Conflict in the 21st Century*, Penguin Books, 2009.
  - M. Shanahan, *The Technological Singularity,* MIT Press, 2015.
  - J. Blascovich, J. Bailenson, *Infinite Reality: Avatars, Eternal Life, New Worlds, and the Dawn of the Virtual Revolution,* HarperCollins, 2011.
- Cybersecurity & Cryptography
  - P. Rosenzweig, *Thinking about Cybersecurity: From Cyber Crime to Cyber Warfare*, The Great Courses, Course No. 9523
  - P. Vigna, M. J. Casey, *The Age of Cryptocurrency: How Bitcoin and Digital Money Are Challenging the Global Economic Order*, St. Martin's Press, 2015.
- Interplanetary Space Travel
  - C. Impey, *Beyond: Our Future in Space*, W. W. Norton & Company, 2015.
- Finance
  - A. Lo, *Finance Theory I, MIT Open Course Ware*, Course No. 15.401.
  - C. Fullenkamp, *Financial Literacy: Finding Your Way in the Financial Markets*, The Great Courses, Course No. 5831.
  - S. Novella, *Your Deceptive Mind: A Scientific Guide to Critical Thinking Skills*, The Great Courses, Course No. 9344.
  - M. G. Goldsby, *The Entrepreneur's Toolkit*, The Great Courses, Course No. 5992.
  - R. P. DeGennaro, *How the Stock Market Works* The Great Courses, Course No. 5852.
  - M. Finke, *Money Management Skills,* The Great Courses, Course No. 5231
  - J. Schwartz, *Finance and Accounting for the Non-Financial Manager*, The Great Courses, Course No. NA.
  - M. Griffis, L. Epstein, *Trading for Dummies*, For Dummies, 2013
  - E. Tyson, *Investing for Dummies*, For Dummies, 2014
  - E. Tyson, *Personal Finance for Dummies*, For Dummies, 2012

Abstract

III-Nitride Vertical-Cavity Surface-Emitting Lasers

Growth, Fabrication, and Design of Dual Dielectric DBR Nonpolar VCSELs

by

John T. Leonard[1]

Vertical-cavity surface-emitting lasers (VCSELs) have a long history of development in GaAs-based and InP-based systems, however III-nitride VCSELs research is still in its infancy. Yet, over the past several years we have made dramatic improvements in the lasing characteristics of these highly complex devices. Specifically, we have reduced the threshold current density from ~100 kA/cm^2 to ~3 kA/cm^2, while simultaneously increasing the output power from ~10 µW to ~550 µW. These developments have primarily come about by focusing on the aperture design and intracavity contact design for flip-chip dual dielectric DBR III-nitride VCSELs. We have carried out a number of studies developing an Al ion implanted aperture (IIA) and photoelectrochemically etched aperture (PECA), while simultaneously improving the quality of tin-doped indium oxide (ITO) intracavity contacts, and demonstrating the first III-nitride VCSEL with an n-GaN tunnel junction intracavity contact. Beyond these most notable research fronts, we have analyzed numerous other parameters, including epitaxial growth, flip-chip bonding, substrate removal, and more, bringing further improvement to III-nitride VCSEL performance and yield. This thesis aims to give a comprehensive discussion of the relevant underlying concepts for nonpolar

---

[1] jtleona01@gmail.com

VCSELs, while detailing our specific experimental advances. In Section 1, we give an overview of the applications of VCSELs generally, before describing some of the potential applications for III-nitride VCSELs. This is followed by a summary of the different material systems used to fabricate VCSELs, before going into detail on the basic design principles for developing III-nitride VCSELs. In Section 2, we outline the basic process and geometry for fabricating flip-chip nonpolar VCSELs with different aperture and intracavity contact designs. Finally, in Section 3 and 4, we delve into the experimental results achieved in the last several years, beginning with a discussion on the epitaxial growth developments. In Section 4, we discuss the most noteworthy accomplishments related to the nonpolar VCSELs structural design, such as different aperture and intracavity contact developments. Overall, this thesis is focused on the nonpolar VCSEL, however our hope is that many of the underlying insights will be of great use for the III-nitride VCSELs community as a whole. Throughout this report, we have taken great effort to highlight the future research fronts that would advance the field of III-nitride VCSELs generally, with the goal of illuminating the path forward for achieving efficient CW operating III-nitride VCSELs.

Table of Contents

Preface

Why, he wondered, did so many people spend their lives not trying to find answers to questions—not even thinking of questions to begin with? Was there anything more exciting in life than seeking answers?

– Isaac Asimov, Prelude to Foundation

Vertical-cavity surface-emitting lasers (VCSELs) are found in a broad range of applications, spanning many fields, and continue to find new and interesting applications every year. These complex devices offer anyone who studies them unique insights and perspectives on optoelectronics and the interplay between light and matter. Arguably the most valuable aspect of studying VCSELs is the fact that they can be fabricated in many different ways, giving researchers a limitless field in which they can innovate and explore their creative design ideas. Furthermore, the complex nature of VCSELs forces researchers to develop modeling and simulation expertise to achieve insight into the fundamental properties of such devices. While the complexity of VCSELs makes them sometimes daunting to study and understand, it is the very complexity that makes them interesting and which will give you the opportunity to learn something new day after day. By reading this thesis, I hope you find a wealth of valuable technical insight, but more importantly, I hope you develop an appreciation for the value of solving complex problems, working with complex systems, and seeking answers.

1. Introduction

"The principal applications of any sufficiently new and innovative technology always have been – and will continue to be – applications created by that technology."

– Herbert Kroemer

Vertical-cavity surface-emitting lasers (VCSELs) were first proposed in 1977 by Kenichi Iga.[1,2] Iga's original sketch for a "surface-emitting laser" is shown in Figure 1. Since then they have been developed for a vast array of applications, covering many different wavelengths, and continue to find new applications to this day. Currently, AlGaAs/GaAs-based and InAlGaAs/InP-based VCSELs are the most mature types of VCSELs, but many research fronts still remain, including the development of GaN-based (III-nitride) VCSELs, emitting in the UV, violet, blue, and green wavelength regimes, as well as a number of other GaAs-based material systems. This introduction will give a brief history of VCSELs and their applications, before analyzing some of the potential applications for III-Nitride VCSELs specifically. Following this review of past and potential applications, the different material systems used to fabricate VCSELs will be analyzed, with an emphasis on III-Nitrides. This will be followed by an overview of fundamental III-nitride VCSEL design concepts. Establishing an understanding of the history of VCSELs, and the many different device designs employed in the past, will give the reader a more complete perspective from which to view the present state of III-nitride VCSELs research, while simultaneously enhancing their ability to see new research frontiers in the field. If the reader finds difficulty understanding any of the terminology or general concepts in optics related to the discussions in this thesis, we recommend referring to Refs. 3–7 for more comprehensive

discussions. Overall, this thesis covers the relevant concepts and experimental developments leading to the nonpolar III-nitride dual dielectric DBR VCSELs and intracavity contacts reported in Refs. 8–13. These results build on the initial nonpolar VCSELs work from C. Holder, reported in Refs. 14–16.

1.1. History of Applications

1.1.1. Data Transmission & Transceivers

As of 2015, VCSELs were a well-established commercialized technology for ~17 years, however it took nearly 17 years for these devices to reach this state. The initial target market was short-haul multimode silica fiber optics networks for data transmission rate of 1 Gbit/s.[4] Initially, VCSELs were an attractive alternative to edge-emitters (self-pulsating AlGaAs/GaAs edge-emitters were the state-of-art technology in the mid-1990s) because of their higher speeds, larger range of temperature stability, relatively low manufacturing costs

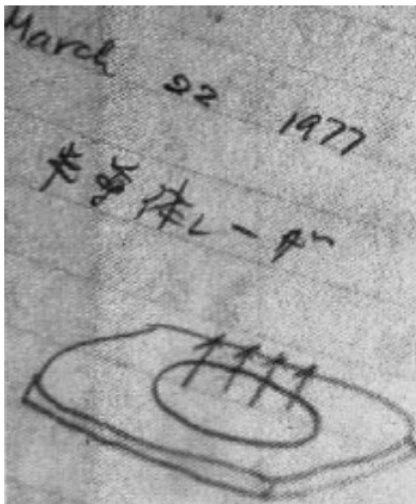$$Loss(dB/km), \alpha = -\frac{10}{L} Log_{10}\left(\frac{P_{out}}{P_{in}}\right)$$

Figure 1 Kenichi Iga's original schematic of a "surface-emitting laser" (March 22nd, 1977).[2]
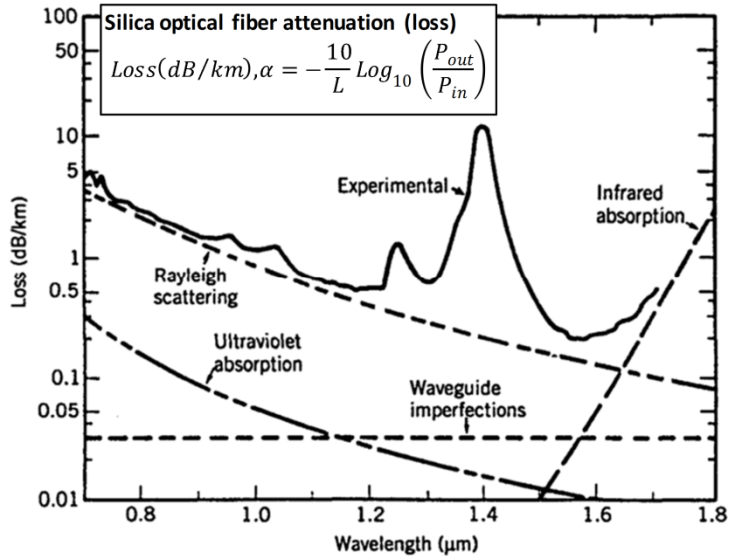
Figure 2 Single-mode silica fiber attenuation (loss) vs. wavelength (1979). The dashed lines show the theoretically predicted contributions to fiber loss at different wavelengths.[7]

(due to the fact that edge-emitters had to be cleaved to form the laser facet before testing), the ability to perform on-wafer probing, and the reduced laser-to-fiber alignment tolerance.[4] Today, edge-emitting laser diodes (EELDs) are more favorable for long-haul data transmission, while VCSELs are more favorable short-haul data transmission, thus each device occupies its own niche area of data transmission. By 2013, VCSEL transmission rates of 10 Gbit/s were being regularly achieved, with 25 Gbit/s transmission rates expected very soon.[4,17,18] These higher bandwidths are especially necessary if VCSELs are to replace copper interconnects for chip-to-chip communication.[19] Presently, extrinsic factors such as parasitic circuit elements,[20] high junction temperatures, and multi-mode lasing constrain AlGaAs/GaAs-based VCSEL (850 nm) data transmission systems (transceivers) from regularly achieving over 10 Gbit/s.[19] Beyond the high data transmission rates, AlGaAs/GaAs-based VCSELs are also promising transceivers because of their relatively low manufacturing cost and simplified system integration.[19] InAlGaAs/InP-based VCSELs (1300 nm) have also been developed for single-mode-fiber interconnects, however this material system proved much more difficult to develop compared to AlGaAs/GaAs-based VCSELs, causing many companies to abandon this technology.[21]

As we mentioned previously, VCSELs are not appropriate for long-haul data transmission. The primary reason for this is that the short cavity length of VCSELs implies that one must have a very high reflectivity (HR) mirror (>99 %) on the top and bottom of the cavity, in order to minimize mirror loss (Section 1.4.4). These HR mirrors result in a small amount of stimulated emission escaping the cavity into free space (milliwatts), or into an optical fiber. Because optical data transmission signals suffer from attenuation (absorption loss) when they propagate down a fiber,[7] a long-haul data transmission system must also
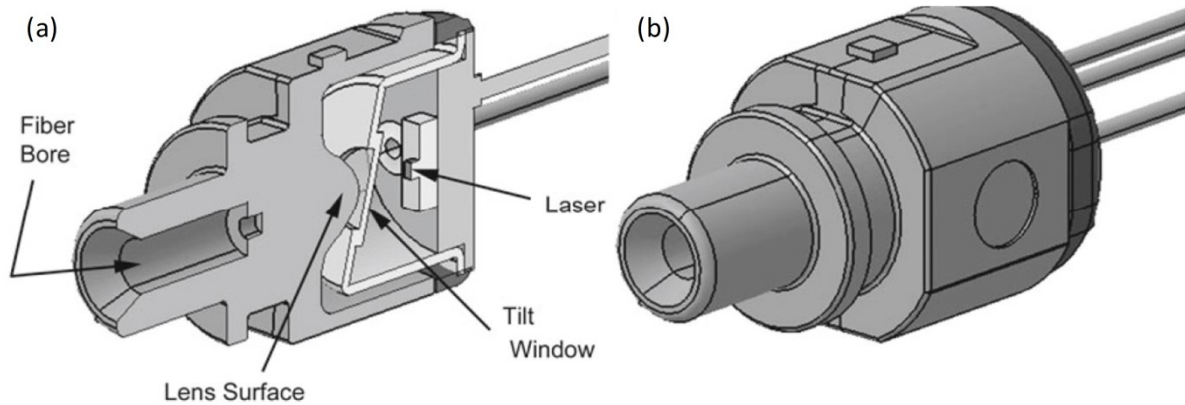
Figure 3 Schematic of a VCSEL-based silica fiber transceiver package. The housing and lens are combined in a single molded piece. (a) shows the cross-section.[4]

have a high power signal source, making VCSELs more appropriate for short-haul data transmission. The degree of attenuation for an optical data communication signal from a laser depends on the emission wavelength of the laser, as can be seen in Figure 2. There are a number of other subtle effects, such as chirp,[7] which make VCSELs unfavorable for long-haul data transmission, but we will not discuss those here.

Figure 3 shows a schematic of a complete package for a VCSEL-based silica fiber transceiver commonly used today.[4] More recently (2000-2010), VCSEL-based transceivers have been intensely researched for parallel optical links for supercomputers. This application introduces a number of unique and interesting device design criteria, which we will not discuss in detail here. In general though, VCSEL-based parallel optical links are a big driver for photonic integrated chips (PICs).[4] Figure 4 shows an example of a VCSEL-
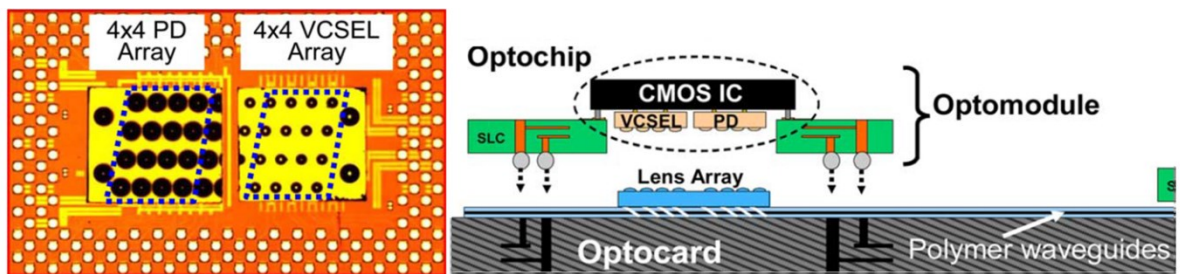

Figure 4 Schematic of Terabus 16+16 channel transceiver integrated circuit. The schematic on the right displays the flip-chip mounted packaging scheme of the VCSEL and photodiode array.[22]

based parallel link package.[22] Here, we can see the high density of different components or devices on these chips introduces a high level of packaging complexity. Furthermore, we can see that VCSELs are really the only type of laser appropriate to this application, as they allow one to achieve a high density of parallel links by fabricating VCSEL arrays, while simultaneously allowing one to vertically stack components as a result of a VCSELs emission normal to the substrate.

An emerging variation of traditional VCSEL based silica fiber optic data transmission, is VCSEL based plastic optical fiber (POF) data transmission.[23,24] Figure 5 shows the attenuation spectrum for two different kinds of POFs. Comparing the silica fiber attenuation (Figure 2) to POF loss (Figure 5), we can see that POFs are generally much more lossy, thus they are more appropriate for short-haul data transmission that requires a very inexpensive fiber. This could include data transmission within an automobile, in in-home networks, or between two laptops. For the case of step index PMMA POF (Figure 5(a)), there are a number of low loss regimes in the visible spectrum. For 650 nm data transmission, AlGaInP/GaAs-based VCSELs are well suited,[25] however for shorter wavelengths (green and blue), III-nitride VCSELs have great potential. The improved
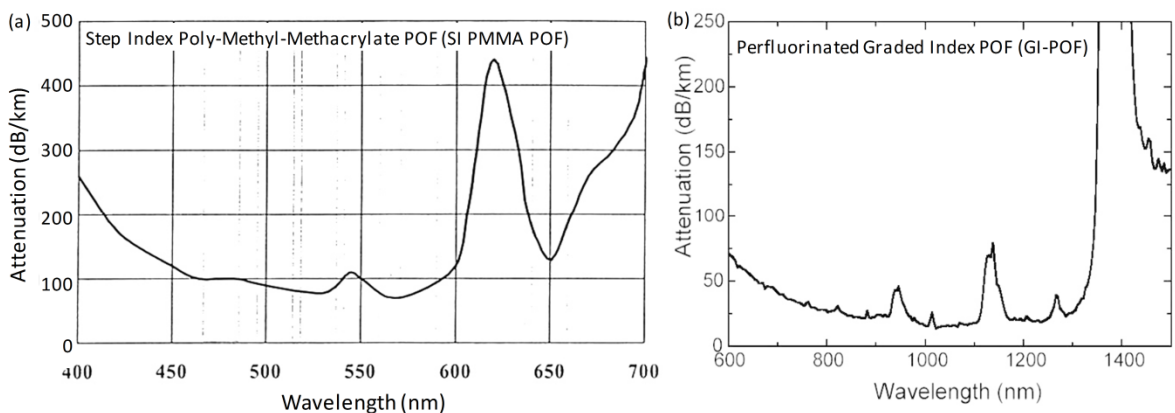

Figure 5 Examples of attenuation spectrums for (a) step index (SI) PMMA POFs and (b) perfluorinated graded index (GI) POFs.[24]

5

temperature stability of III-nitride emitters generally, compared to GaAs- or InP-based emitters generally, makes using III-nitride VCSELs with PMMA POFs particularly compelling. That being said, perfluorinated POFs have low loss in regimes similar to silica fibers (infrared), allowing the POF industry to leverage the more mature AlGaAs/GaAs-based VCSEL technology until III-nitride VCSELs reach maturity. An overview of the advantages and disadvantages of the different kinds of POFs can be found in Ref. 24.

A growing sector for POF applications is in optical video links. Currently optical video links tend to use 850 nm VCSELs.[4] This form of video link has the potential to improve over copper based video links when a display is very large and/or has very high resolution, requiring large amounts of graphics data to be transmitted rapidly. This includes displays in stadiums, airports, train stations, and central city areas. However, a more compelling application of optical video links is in applications that require a minimal amount of electromagnetic interference in data transmission, which is the case for many medical examination techniques, such as CT, MRI, PET, and digital x-ray analysis.[4] Optical video links have trouble competing with more traditional HDMI technologies in consumer applications because they general have a larger form factor than the copper interconnect packages due to the packaging in TO cans.[4]

In summary, VCSEL-based transceiver technology is quite mature, but it continues to find interesting new applications that push the boundary of state-of-the-art AlGaAs/GaAs-based and InAlGaAs/InP-based VCSEL technology. Beyond the use of VCSELs in supercomputer and server farms, they are also found in some more common consumer electronics, such as gigabit Ethernet cables and laptops (mostly Apple products) using Thunderbolt. Additional details on VCSEL transceivers can be found in Refs. 4,26.

1.1.2. Mice & Doppler Interferometers

Around 2004, infrared VCSELs were incorporated in computer mice, where they are widely used to this day. Silica fiber based data transmission applications and optical mice are the two largest VCSEL markets today.[4] VCSEL based optical mice are advantageous to LED based optical mice because they offer improved reliability in tracking, simpler optics, and higher system efficiency, thereby reducing power consumption for longer battery lifetimes. Generally infrared VCSELs are used in higher-end mice, while red LEDs are used in cheaper mice. The most advanced approach to using a VCSEL in optical mice involves the VCSEL serving as a detection and demodulation system via self-mixing interface in the laser cavity (Doppler interferometry), which can be monitored via a photodetector underneath the VCSEL.[4,27–29] Because Doppler interferometry is very sensitive to changes in the frequency of light emitted from the cavity, it is critical for Doppler interferometer VCSELs to have single longitudinal and lateral mode emission characteristics with a stable polarization.[4] The requirement for single mode emission implies the aperture diameter is smaller for Doppler interferometer VCSELs compared to transceiver VCSELs. This implies that a higher degree of control over aperture diameter variation is also necessary for Doppler interferometer VCSELs, which can be particularly difficult when wet oxidation is used to define the aperture in an AlGaAs/GaAs-based VCSEL. The basic concept of a VCSEL and integrated photodetector being used as a Doppler interferometry system can be applied to enumerable motion sensing applications beyond computer mice, such as motion tracking of finger or eye gestures,[4,28] monitoring manufacturing processes, internal and external velocity measurements in automotive and robotic applications,[30] measuring fluid flow rates,[31] and
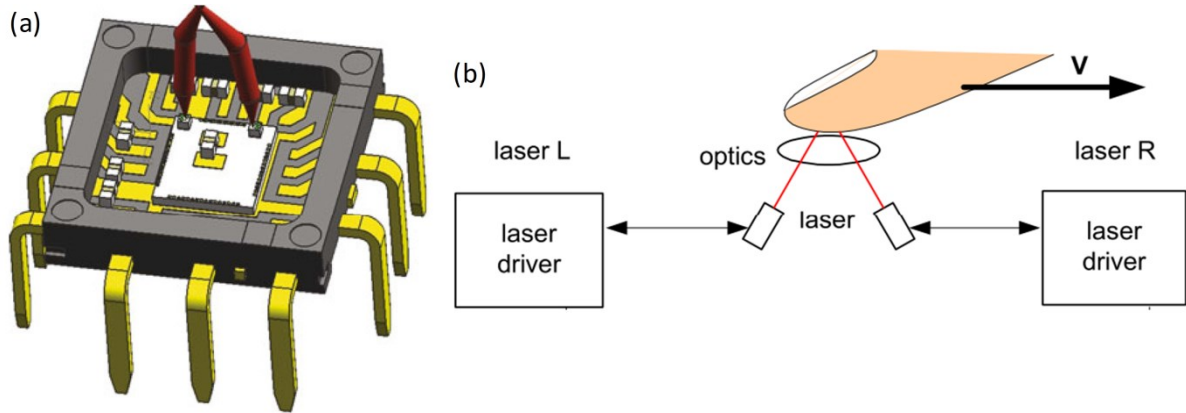
Figure 6 The Philips Twin-Eye VCSEL-based Doppler interferometer sensor. (a) shows a schematic of the package with the emission from the two VCSELs. (b) shows the basic operating principal for the device, where the two VCSEL Doppler interferometers track the movement of a finger.[4,28]

detecting range.[32] Figure 6 shows one example of a motion sensing chip manufactured by Philips (the Twin-Eye sensor), which employs two Doppler interferemoeter VCSELs.[28] With the increasing market volume for sensors used in the internet of things (IoT) sector, it is likely that VCSEL based Doppler interfermoetry systems will continue to find a wealth of applications. Compared to edge-emitters, VCSELs are especially well suited for laser based sensing in IoT applications, due to their low threshold currents and thus low power consumtion characteristics. In general, the ultimate sensing distance is half the coherence length the emitted VCSEL light. Currently Doppler interferometry VCSEL sensors operate up to a few meters.[4]

Another application related to VCSEL Doppler interferometers is VCSEL based miniature atomic clocks.[33,34] Atomic clocks are critical for satellites and space crafts in general. With the ramping up of interplanetary space travel,[35] it is likely that this application sector will become of increasing importance, due to the strict low weight and low power consumption requirements in space crafts. VCSEL based atomic clocks basically work by exciting an atomic transition in an element (Cesium for AlGaAs/GaAs-based VCSEL atomic clocks). The atomic transition is then detected, giving a highly precise time counter. Though

there is not a huge market for space travel at the moment, if miniature atomic clocks become efficient enough, they could replace conventional quartz crystal oscillators, allowing them to be incorporated into watches or other devices in the internet of things (IoT) sector.

1.1.3. Laser Printing & VCSEL Arrays

In 2003, Xerox debuted the world's first VCSEL-based electrophotographic printer, DocuColor 1256GA, which employed a 780 nm single-mode 8×4 VCSEL array, allowing a print resolution of 2400 dots per inch (dpi).[4] Using a VCSEL array for printing (i.e. in a raster output scanner (ROS)) not only improves resolution, but also printing speed and power consumption, due to the ability to perform parallel scanning using the array, and due to the low power consumption of VCSELs. This initial demonstration of a product was preceded by nearly a decade of research at Xerox, which began in 1995, and generated the first VCSEL-based light exposure system.[36] As is the case for Doppler interferometer VCSELs, laser printer VCSELs also require single lateral mode operation due to the
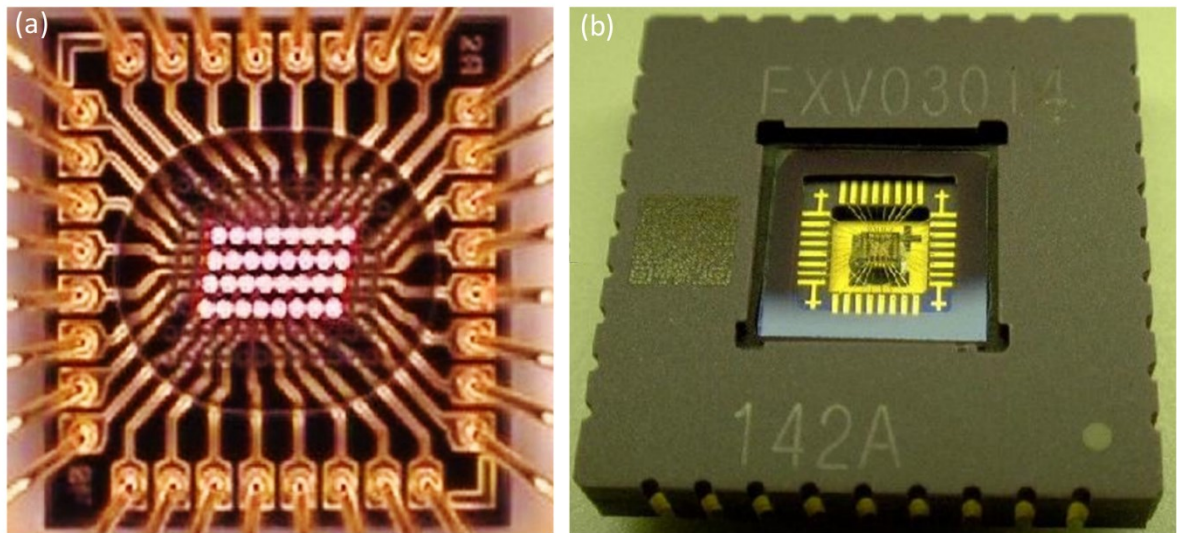

Figure 7 (a) microscope image of an 8 × 4 single-mode 780 nm VCSEL array used in Xerox laser printers. (b) the full package VCSEL array in a leadless chip carrier (LCC) package.[36]

necessity for a well-controlled beam profile to generate a pixel. This in-turn requires the use of small aperture diameter devices, which creates the necessity for precise control of the oxide aperture. To improve the control of the wet oxidation aperture formation for 780 nm VCSELs, Xerox uses a reflectometry technique called OPTALO (optical probing technique of AlAs lateral oxidation), which is briefly discussed in [36]. Figure 7 shows images of a Xerox 780 nm VCSEL array for a ROS system in a laser printer. The ROS works by sending the modulated laser light to a polygon mirror, which rotates and reflects the beam through a lens and onto a photoconductor. The rastering of the beam on the photoconductor allows the formation of the image pattern. Charged toner is then applied to the photoconductor and subsequently the print paper, where it is fused thermally or mechanically.[4] Beyond the circular beam-profile, low output beam divergence, and low power consumption, VCSELs in the form of a VCSEL array are particularly well suited for printing applications because the print speed is directly proportional to the number of beams guided to the photoconductor. A comprehensive discussion on the challenges and properties of VCSELs for laser printing can be found in Ref. 4,36.

Beyond their applications in laser printers, VCSEL arrays can be found in a number of emerging applications. In the sector of high power lasers, Philips has manufactured a 10 kW AlGaAs/GaAs-based VCSEL module (808 nm) for high power density industrial sintering and annealing.[37–40] Figure 9 shows this 10 kW VCSEL array module. As can be seen, the module is actually composed of a large assembly of individual VCSEL array chips. Figure 9(b) in particular demonstrates the extremely high packing density that can be achieved in VCSEL arrays. Another emerging application of VCSEL arrays is in computed radiography (a form of x-ray scanning), where Vixar is developing a VCSEL based laser

a) VCSEL array cross-section **b)** VCSEL array top view **c)** 8 W VCSEL array chip on board

d) 2D array of VCSEL array chips **e)** 400 W VCSEL emitter **f)** 24-emitter, 9.6 kW module
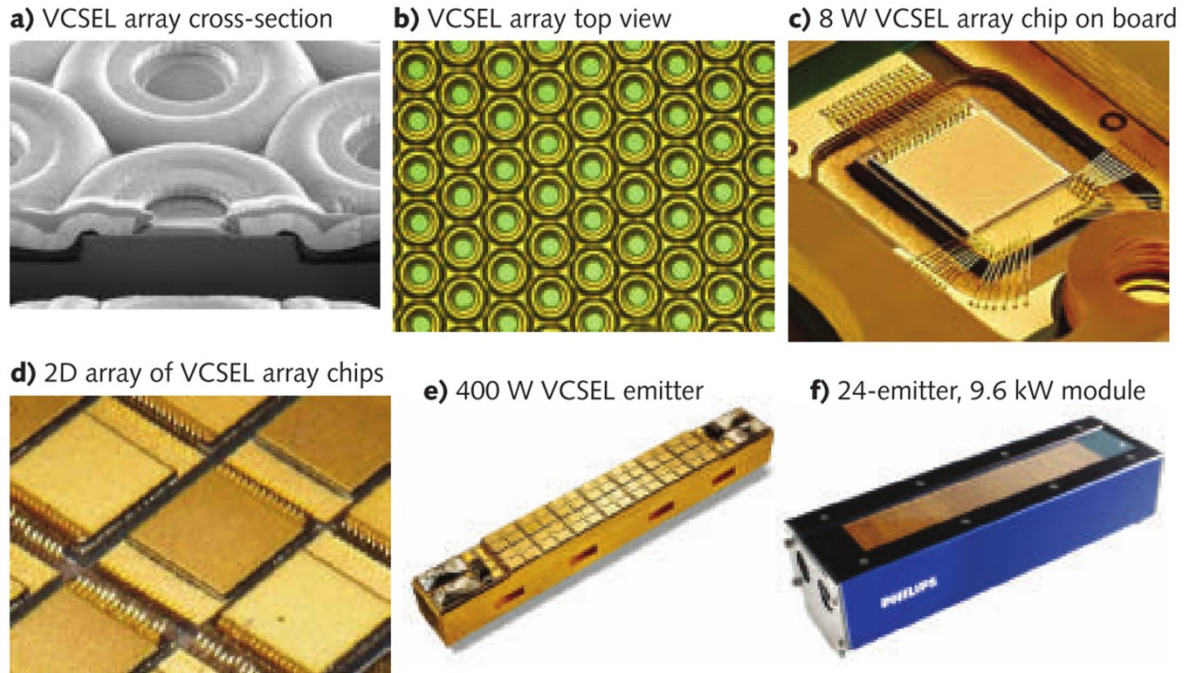
Figure 9 A Philips 10 kW GaAs-based VCSEL array module. (a) shows a cross-section of an individual VCSEL. (b) shows an optical microscope image of a single array chip. (c) shows the complete chip with wire bonds. (d) shows the 2D array of VCSEL array chips. (e) shows a 400 W emitter sub-module. (f) shows the completed 10 kW module. [38–40]

scanner, shown in Figure 8.[25] Though these high power arrays are only appropriate for relatively niche applications, they represent a general proof of the potential for a single low-power VCSEL to be combined into a 2D array for high power applications.

In summary, VCSELs have a long history of progress and development with different applications presenting new challenges. We have covered many of the primary

Figure 8 Photos of a 2" solid-state scanner from Vixar, used for computed radiography, a form of X-ray imaging.[25]

applications for VCSELs, however there are other more obscure applications which we have not discussed. All the applications discussed thus far have used red and infrared VCSELs, however with so many applications for these long wavelengths alone, it is easy to imagine that there are a plethora of potential applications for VCSELs emitting in the ultra-violet (UV), violet, blue, and green regime. By understanding the history of red and infrared VCS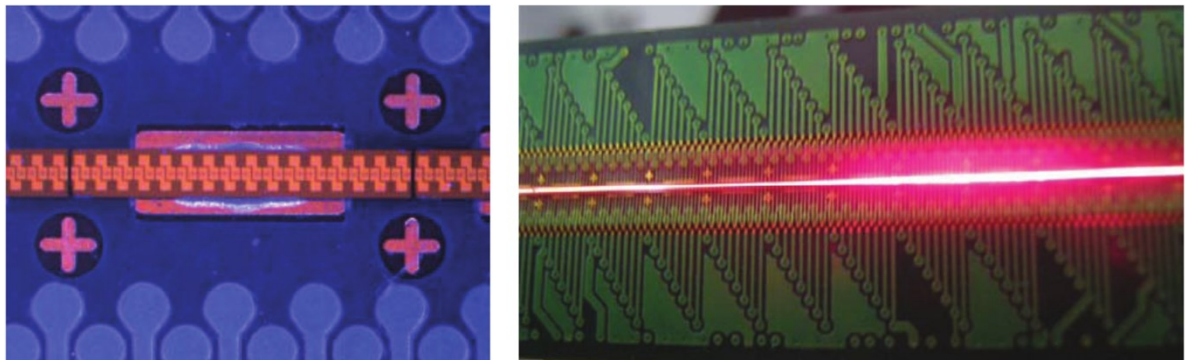EL applications, we can now more clearly speculate on the potential applications for III-nitride VCSELs, many of which have their parallels in AlGaAs/GaAs-based and InAlGaAs/InP-based VCSEL applications.

1.2. III-Nitride VCSEL Applications

III-nitride VCSELs share many of the intrinsic properties of the more mature AlGaAs/GaAs- and InAlGaAs/InP-based VCSELs on the market today, however because they open the door for an extended range of emission wavelengths (green, blue, violet, and UV), they also offer great potential for a number of new applications. The primary sectors for III-nitride VCSELs include transceiver, sensor, illumination, and display technology.

1.2.1. III-Nitride Transceiver Technology

In recent years, visible light communication (VLC), sometimes called light-fidelity (LiFi) data transmission, has become of great interest to academic and industry researchers alike. One of the most popular demonstrations of this concept was in 2011 when Harald Haas gave a TED talk titled "Wireless data from every light bulb".[41] This technology could
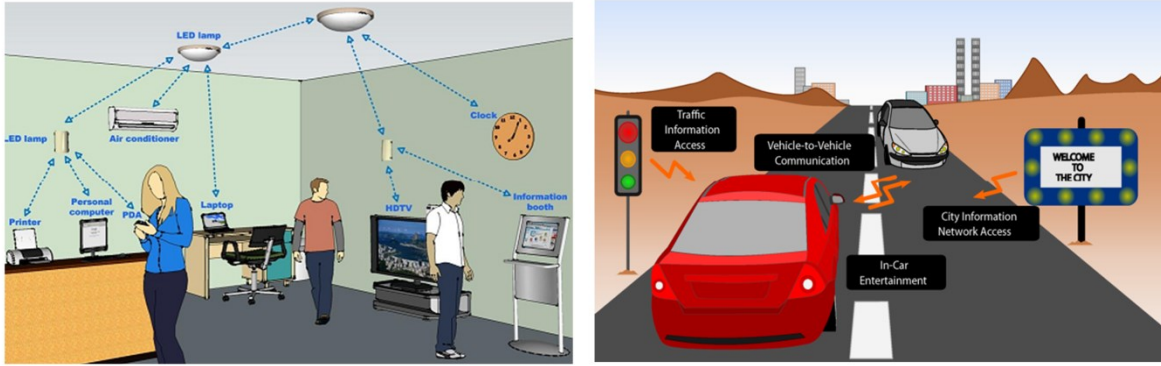
Figure 10 Illustration of visible light communication (VLC) application in buildings (left) and in automobiles (right).[387]

be incorporated into a number of places, including in buildings,[42,43] as well as for car-to-car communication or car-to-traffic signal communication,[44] as shown in Figure 10.

Though the technology is interesting from a research prospective, at a first glance it can seem like there is not a critical need for such capabilities, however there are a number of technology trends that motivate the development of VLC. First, the ever increasing volume of wearable electronics and general items in the IoT sector is causing a saturation of wireless bandwidth resources.[45] To put it simply, there is a finite bandwidth over which traditional RF wireless technologies can transmit data, and that bandwidth is becoming increasingly crowded. Furthermore, the visible light spectrum is not currently regulated by the Federal Communications Commission (FCC), which would allow data comm. companies to avoid bandwidth allocation fees. Finally, with network security becoming an increasingly important issue, VLC is poised to offer an additional level of security as the data transmission signal can only be detected by line-of-site methods, prevent hackers outside a building from entering a network through a VLC connection. It should be noted that no one is suggesting that VLC is a replacement for more mature wireless technologies, it is simply a method for opening up more bandwidth to improve wireless performance and user experience overall.

Generally, the concept of VLC essentially the same as conventional data transmission in fiber optic networks, but here we simply use visible light transmitting in free-space (air) to send data. As was the case in the initial development of fiber optic networks, the first generation VLC transceivers are modulated III-nitride LEDs. However, because LEDs have very low modulation bandwidths (< 2 GHz) compared to lasers (> 2 GHz), it is certain that they will be replaced by III-nitride lasers in order to achieve higher data transmission rates. To achieve higher modulation bandwidths for LEDs, researchers have been investigating using micro-LEDs,[46–48] in order to reduce the RC time constant. However, LEDs are intrinsically limited by their long carrier lifetimes, making their theoretical maximum modulation bandwidths well below theoretical maximum for lasers. Recently, our group has demonstrated the first laser based VLC system using an edge-emitting laser diode (EELD), proving the potential for laser based VLC.[49,50] Furthermore, in collaboration with B. S. Ooi's group at KAUST, C. Shen and I have performed initial modulation frequency measurements on III-nitride VCSELs, showing a modulation
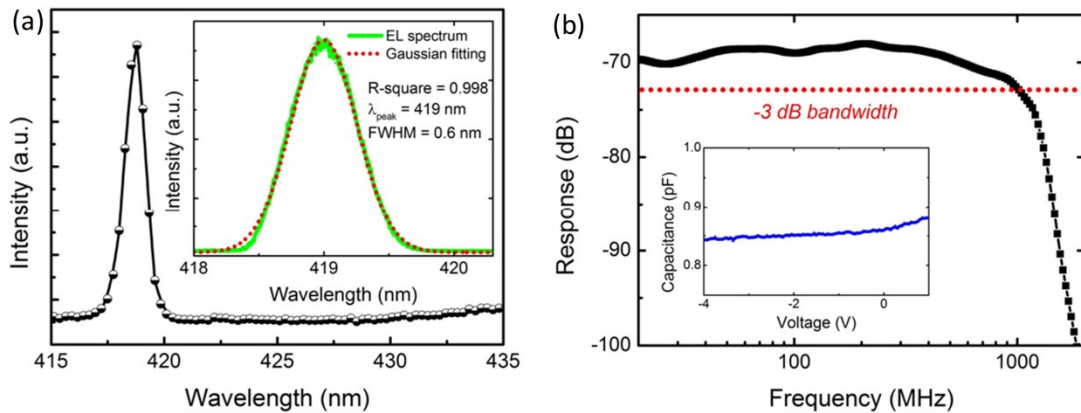
Figure 11 (a) emission spectrum of a 10 μm aperture diameter IIA+TJ VCSEL. The inset shows a high resolution measurement fitted using a Gaussian function, with a peak emission wavelength of 419 nm and a FWHM of 0.6 nm. (b) Modulation response of the 10 μm aperture diameter IIA+TJ VCSEL, showing a -3 dB bandwidth of 1 GHz. This bandwidth is limited by the frequency response of the amplified photodiode (APD) used for the measurement, not the VCSEL itself. The inset shows the CV characteristics of the device. The LIV LIV and emission profile data for this device can be seen in Figure 93.

bandwidth ~1 GHz, which was limited by the frequency response of the photodetector, not the VCSEL itself. These results are summarized in Figure 11. This first demonstration of VCSEL modulation, which has yet to be published in a journal as of the writing of this thesis, experimentally proves the potential for III-nitride VCSEL VLC systems. However, because the frequency response shown in this measurement was limited by the photodiode detecting the VCSELs power, we do not yet know what the true modulation bandwidth is for the VCSEL itself. Generally speaking though, because the modulation bandwidth is inversely proportional to the active region volume, VCSELs have the potential to yield even higher modulation bandwidths than EELDs. Furthermore, because VCSELs emit normal to the substrate, they can be easily incorporated into current LED packaging systems. To achieve a strong signal, a VCSEL VLC system would need to be made of a 2D VCSEL array, which may present some challenges in reducing parasitic capacitances, however these are simply technical challenges that can be overcome with proper development. Thus it is quite possible that III-nitride VCSEL based VLC will become the standard for VLC in the long run. To achieve white light emission, while simultaneously transmitting data, such III-nitride VCSELs would need to emit violet (405 nm) or blue (450 nm) light to photopump a phosphor. More comprehensive discussions on VLC can be found in Refs. 51,52.

Beyond VLC, III-nitride VCSELs also have great potential in plastic optical fibers, discussed previously. Here, green (~625 nm) III-nitride VCSELs may compete with red AlGaInP/GaAs-based VCSELs in PMMA POF applications, which could be used for automobiles and optical video links. Figure 5(a) shows the attenuation spectrum for PMMA POFs, where it can be seen that the loss is fairly low in the blue and green regime, thus blue

III-nitride VCSELs may also be used for this application, which encompasses many sectors, as described previously.

1.2.2. III-Nitride Sensor Technology

One of the largest markets where III-nitride VCSELs could be used as a sensor is in biosensing. The high modulation speeds and narrow FWHM of III-nitride VCSELs can be advantageous to many techniques involving optical probing of biomaterials, such as fluorescence lifetime imaging microscopy (FLIM).[53] Furthermore, the small form factor and low power consumption of VCSELs makes them advantageous to emerging lab-on-chip technologies, shown in Figure 12. In this application, a set of III-nitride VCSELs with different emission wavelengths could be assembled to perform fluorescence probing of different species and/or biochemical tags (Figure 12 (right)). Furthermore, if these VCSELs were used as Doppler interferometers, they could detect the fluid flow rate.[31]

Beyond their applications in biosensing, UV, violet, and blue III-nitride VCSELs integrated into a Doppler interferometry systems may also open the door for a number of other interesting applications. One can easily imagine using an array of VCSELs in a
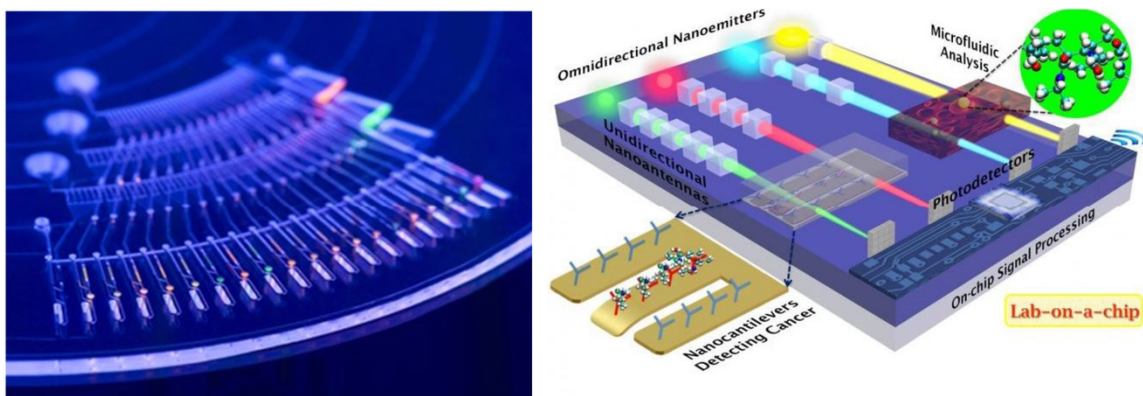

Figure 12 Photograph (left) and schematic (right) of a lab-on-chip (LOC) system.[388]

Doppler interferometry system to perform rapid surface mapping in production lines or general R&D.[28] The shorter wavelength would allow improved resolution, while simultaneously giving the potential for integrating surface mapping with photoluminescence for probing material quality. In III-nitrides processing alone, a large 2D III-nitride VCSEL array with Doppler interferometer and photoluminescence capabilities could be built to allow instantaneous surface roughness and active region quality analysis of large wafers immediately after growth. Because nonpolar m-plane VCSEL arrays have a 100 % polarization ratio, as a result of the intrinsic nature of the valence band structure on m-plane InGaN MQWs, these III-nitride VCSELs are especially well suited for Doppler interferometry applications, where a stable polarization is necessary.

Overall, it is clear that fabricating a III-nitride VCSEL Doppler interferometer would probably be the most difficult III-nitride device to fabricate, however the benefits and the wide-spread markets available for such a device make it a compelling investment. With the recent advances in III-nitride tunnel junction technology, presented in this thesis and elsewhere,[11,12] it appears that all the critical components are now available to build such a device, thus the only remaining challenge is actually getting in the lab and making it happen.

As mentioned in the previous section, VCSELs can also be used in miniature atomic clocks. The advantage of a III-nitride m-plane VCSEL for an atomic clock would be the intrinsic 100% polarization ratio,[8] allowing mode locking for improved sensitivity. atomic clocks,[33,34] While AlGaAs/GaAs-based VCSEL atomic clocks excite cesium transitions,[34] UV III-nitride VCSELs (369 nm) could be used to excite Yb ions for miniature atomic clocks. Beyond the polarization advantages of on nonpolar III-nitride VCSELs, GaN-based
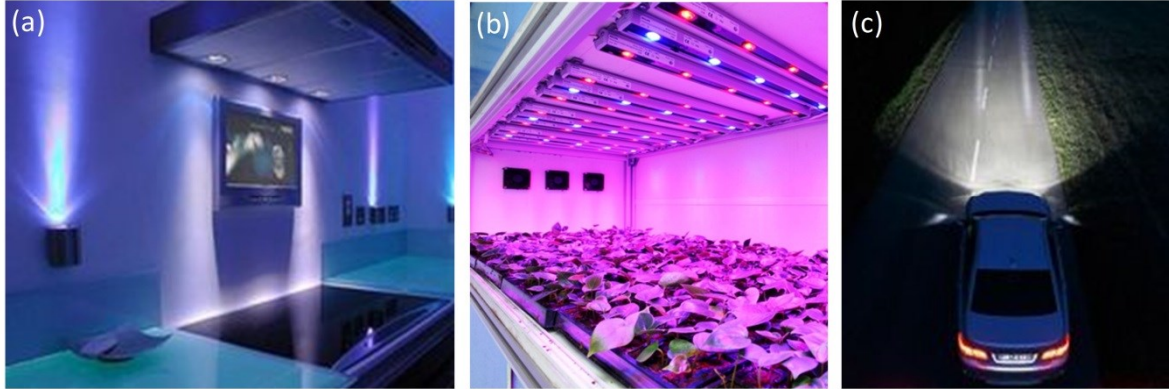
Figure 13 Examples of illumination sector applications for III-nitride VCSELs. (a) shows directional lighting in indoor applications (homes, museums, theaters, hotels, casinos, etc.), (b) shows directional lighting in industrial (vertical) plant growth, (c) shows laser-based lighting in automobile headlights. The concept shown in (c) can also be applied to aircraft lighting (drones or commercial airliners). ((a) and (b) are from Google Images, (c) is from Ref. [389])

light emitters have a much better temperature stability than AlGaAs/GaAs-based and light

emitters (Section 1.3).[54]

1.2.3. III-Nitride Illumination Technology

Laser based lighting has gained increased attention in recent years.[55–59] The basic

idea of laser based lighting is to use a laser instead of an LED to illuminate a phosphor. In

the field of illumination, III-nitride VCSELs are most well suited for applications requiring

directional illumination, such as mood lighting for hotels, museums, theaters, or homes,

directional lighting for industrial (vertical) plant growth, or for automobile or aircraft

(drones or commercial airliners) headlights (Figure 13). Compared to EELDs, VCSEL

arrays are particularly well suited for these applications because they can be easily

integrated with existing LED infrastructure, and because they have emission normal to the

substrate, unlike edge-emitters. For applications where Lambertian emission is desirable,

having many low power VCSELs distributed over a substrate, rather than a single high

power point source, such as an EELD, would actually be advantageous, as the highly

directional laser light would not need to be scattered as much in the case of a VCSEL array, in order to achieve more Lambertian emission profiles from the phosphor (i.e. matching the angular intensity distribution of LED emission). Another alternative to achieving a larger angular distribution of illumination is reflect the laser beam across a digital micromirror, such as those used in digital light projection (DLP) systems, and have the mirror raster over the desired angular emission range. If a VCSEL system were implemented with a rastering mirror, one could potentially couple a LiDAR or Doppler interferometer with an illumination system. In a similar way, one could combine a visible light communication (VLC or LiFi) system with a lighting system. At the time of this writing, only one modeling paper has analyzed the potential for III-nitride VCSELs based lighting,[55] though the angular emission pattern was not considered.

Using a III-nitride VCSEL as a transceiver, sensor, and illumination source together would have huge potential in many industries and would probably find new applications as well. One of the more obvious applications would be to simply integrate this III-nitride VCSEL based Doppler interferometer/transceiver/illuminator into automobile or drone headlights in order to give distance/velocity tracking, vehicle-to-vehicle communication abilities, and general illumination for any operators or persons nearby. In a similar implantation, this module could be installed in traffic lighting for monitor speeds, automatically turning lights on or off to save power, or to communicate traffic or emergency data to cars driving by. If this same system were integrated into a conventional VLC system, one could develop a method for dynamically adjusting the laser beam data signal to track a person acquiring that signal, which may potentially improve general connectivity and signal strength. Another application for this technology could be in camera flashes. Here, one

could primarily use the Doppler interferometer and illumination capabilities to perform a rapid laser scan of an imaged area. This could then be coupled with an app to build 3D images of objects just by taking picture with a smartphone. Making 3D data generation widely available to consumers would allow some companies, such as Nike, to design custom products like shoes, pants, shirts, etc.. Also consumers could use this technology to easily 3D print any object they take a picture of. This would completely disrupt supply chains and revolutionize the way humans purchase, design, and acquire new products. Naturally, these ideas are only a small collection of potential applications and it is without a doubt than many applications leveraging III-nitride VCSEL based illumination sources may not have even been thought of yet.
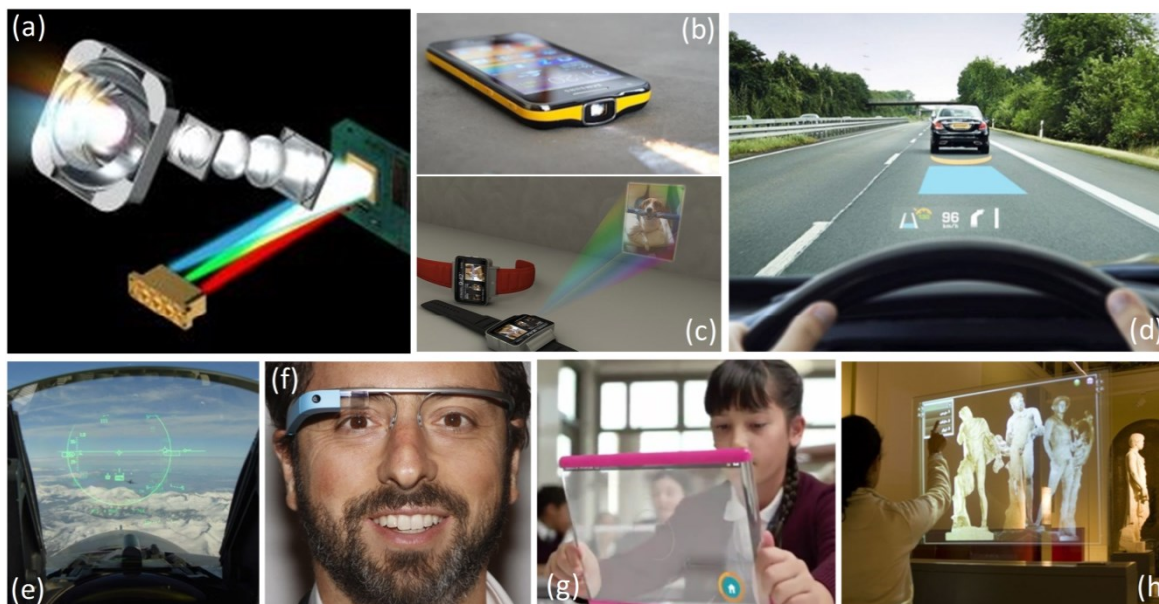
Figure 14 Examples of potential applications of VCSELs in display technology. (a) shows a basic schematic for a digital light processing (DLP) system which is the basic system used for projection technology. Here III-nitride VCSELs would serve as the green and blue light source. (b) and (c) shows pico projectors in phones and wearable electronics. (d) and (e) show heads-up displays for an automobiles and aircrafts, where a III-nitride VCSEL could be used for green and blue illumination. (f), (g), and (h) show applications using diffractive optics/holographic optical elements for dispalys. (f) shows Sergey Brin wearing a Google Glass augmented reality head-set. (g) shows a glass plate display from Cornings concept video "A Day Made of Glass... Made possible by Corning. (2011)". (g) shows a holographic projection screen setup with touch screen functionality from Sax3d GmbH.[60]

1.2.4. III-Nitride Display Technology

III-nitride VCSEL applications in display technology offers one of the most complicated, interesting, and largest market volumes of all the different sectors described previously. Because of the highly directional and coherent nature of VCSEL emission, they are most well suited to displays leveraging holographic/diffractive optics technology and projection technology.[60] This includes the applications shown in Figure 14, such as wearable electronics, augmented reality head-sets (Google Glass), heads-up displays in automobiles and aircrafts, pico-projectors, as well as holographic projection screens. VCSELs are also advantageous to these applications because of their small form factor and low input power, which would improve battery life. The circular beam profile and low divergence angle is also advantageous for diffractive optics based displays.[60] In more conventional liquid-crystal displays (LCDs) (or light-valve displays generally), VCSELs could be used as the backlight source, however light-valve displays are beginning to be surpassed by self-luminance displays, such as organic LEDs (OLEDs), or RGB LED pixel arrays. These self-luminance displays offer a higher color gamut, higher pixel density, and simpler driving architecture than LCDs. Overall, it is apparent that the display technology sector as a whole is on the verge of an intense technological disruption which will expand the ways in which humans interact with displays, through augmented reality, virtual reality, and more, while simultaneously creating more efficient and higher quality conventional displays for flat screen units. III-nitride VCSELs still have a long way to go until they can be effectively integrated into display systems, however these applications may help drive their development.

Beyond these near future technologies, there are some more applications that are probably quite distant, but really awesome all the same. Specifically, these include applications that integrate biology and semiconductor devices. There is an entire field investigating optical stimulation of neurons for various applications where III-nitride VCSELs could provide unique capabilities due to their low power consumption, small beam profile, and narrow line-width.[61] In the realm of display technology integration with biology, one could implement more integrated near eye displays by building a collimated pico-projector in a contact lens that projects directly onto the retina (Figure 15(a)). Further in the future, this technology could be adapted to be directly implanted into the eyeball, completely integrating display technology with biology (Figure 15(b)).. At first glance, this proposal may seem crazy, but there are actually already retinal implants in humans today (Figure 16). Currently, these retinal implants (i.e. the Retina Implant AG) are photodetectors that allow people with damaged retinas or blindness to acquire a small degree of vision, but there is no clear limitation on extending and improving on this technology.[60]

In summary, III-nitride VCSELs technology may be in its infancy, but there is a
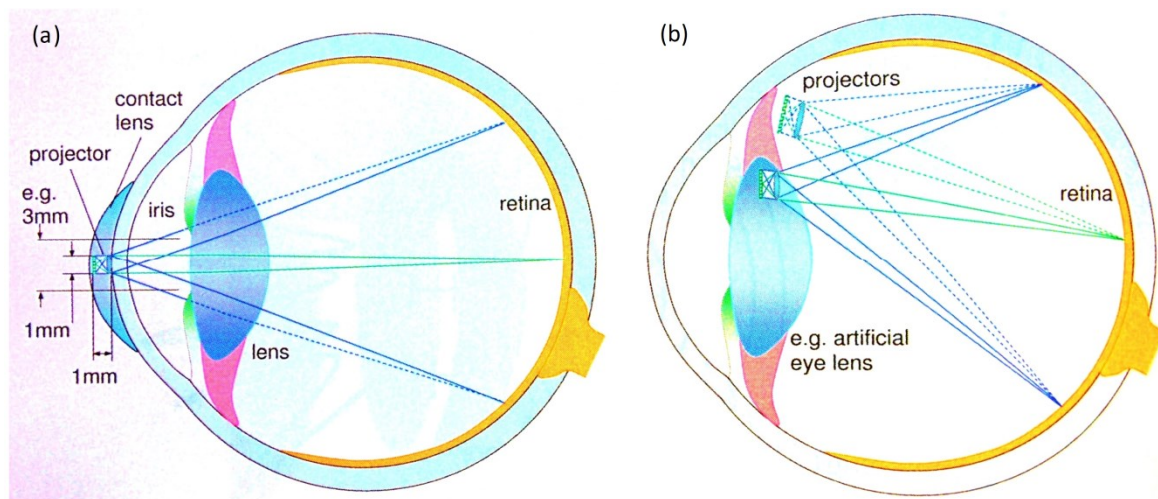
Figure 15 (a) Schematic of a collimated pico-projector embedded in a contact lens. This design is a trade-off between size and resolution, but suffers from vignetting (fading at the edge of images) by the iris. (b) An eye implanted pico-projector schematic. This design overcomes the issues with the contact lens design. [60]
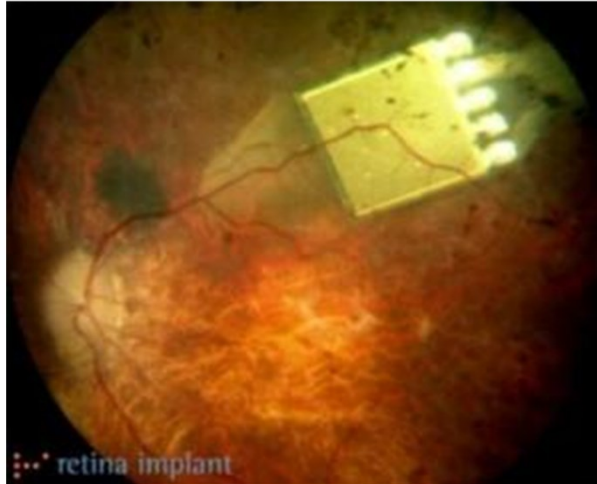
Figure 16 Image of the Retina Implant AG subretinal photodetector implant device used to restore partial vision to blind people.[60]

huge market of applications waiting for them to reach useful efficiency levels. Many of these markets are future tech. markets that have not reached saturation, and thus when people often think about III-nitride VCSELs they cannot readily see applications. However, when we have a more in-depth knowledge of technology trends and future tech. applications and systems in general, we can more easily identify applications for III-nitride VCSELs. Yet, there are likely many applications for III-nitride VCSELs which were not even considered here, thus whenever we consider applications for new semiconductor devices, we should always remember the words of Herbert Kroemer: "The principal applications of any sufficiently new and innovative technology always have been – and will continue to be – applications created by that technology."

1.3. Material Systems

VCSELs are predominantly fabricated from III-V compounds. These are listed in Figure 17, along with other common semiconductor materials. Figure 17 plots these materials as a function of bandgap (gap energy) and bandgap wavelength vs. lattice constant.
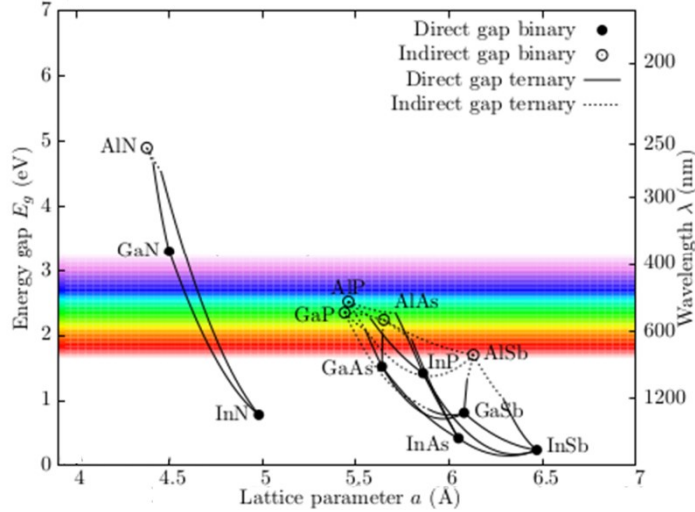
Figure 17 Common semiconductor materials plotted as a function of energy gap (bandgap) and wavelength vs. lattice constant. The lines connecting the binary compounds indicate ternary compounds. Solid lines indicate compositions with a direct bandgap, while dashed lines indicate indirect bandgap compositions. [390]

The lines connecting the binary compounds define the ternary compound properties, where a solid line indicates a direct bandgap, while a dashed line implies and indirect bandgap. As discussed previously, AlGaAs/GaAs-based and InAlGaAs/InP-based VCSELs are the most mature devices, however beyond InGaN/GaN-based (III-nitride) VCSELs, there are a number of other material systems at various stages of maturity, including AlGaInP/GaAs-based VCSELs,[25] GaAsSb/GaAs-based VCSELs,[62–64] dilute nitride GaInNAs/GaAs-based VCSELs,[65–68] highly strained GaInAs/GaAs QW VCSELs,[69–73] and GaAs-based quantum dot VCSELs.[74,75] It is of note that historical convention has led many authors to simply refer to AlGaAs/GaAs-based VCSELs as "GaAs-based VCSELs", though there are many different types of GaAs-based VCSELs. In general the term GaAs-based implies the epitaxial structure is grown on a GaAs substrate, while "InP-based" implies growth on an InP substrate. This section will briefly cover the unique material properties of AlGaInP/GaAs (red), AlGaAs/GaAs (near-IR), and AlGaInAs/InP (IR) systems that influence VCSEL design, before giving more details on III-nitrides generally and their idiosyncratic characteristics that influence InGaN/GaN-based VCSEL design.

Table 1 Room temperature properties of common III-V compounds.[6,117] Bowing parameters for some of the properties for ternary and quaternary compounds can be found in Refs. [3,6].

Quantity	Symbol	AlAs	GaAs	InAs	AlP	GaP	InP	AlN	GaN	InN	(Unit)
Crystal structure		Z	Z	Z	Z	Z	Z	W	W	W	–
Gap: Direct (D) / Indirect (I)		I	D	D	I	I	D	D	D	D	–
Lattice constant	$a_0 =$	5.6611	5.6533	6.0584	5.4635	5.4512	5.8686	3.112	3.191	3.545	Å
	$c_0 =$								5.185	5.703	Å
Bandgap energy	$E_g =$	2.168	1.42	0.354	2.45	2.26	1.35	6.28	3.425	0.77	eV
Intrinsic carrier concentration	$n_i =$	10	2×10^6	7.8×10^{14}	0.044	1.6×10^0	1×10^7	9.4×10^{-34}	1.9×10^{-10}	920	cm^{-3}
Effective DOS at CB edge	$N_c =$	1.5×10^{19}	4.4×10^{17}	8.3×10^{16}	2.0×10^{19}	1.9×10^{19}	5.2×10^{17}	6.2×10^{18}	2.3×10^{18}	9.0×10^{17}	cm^{-3}
Effective DOS at VB edge	$N_v =$	1.7×10^{19}	7.7×10^{18}	6.4×10^{18}	1.5×10^{19}	1.2×10^{19}	1.1×10^{19}	4.9×10^{20}	1.8×10^{19}	5.3×10^{19}	cm^{-3}
Electron mobility	$\mu_n =$	200	8 500	33 000	60	110	4600	300	1500	3200	cm^2/Vs
Hole mobility	$\mu_p =$	100	400	450	450	75	150	14	30	–	cm^2/Vs
Electron diffusion constant	$D_n =$	5.2	220	858	1.6	2.8	120	7	39	80	cm^2/s
Hole diffusion constant	$D_p =$	2.6	10	12	11.6	1.9	3.9	0.3	0.75	–	cm^2/s
Electron affinity	$\chi =$	3.50	4.07	4.9	3.98	3.8	4.5	1.9	4.1	–	V
Minority carrier lifetime	$\tau =$	10^{-7}	10^{-8}	10^{-8}	10^{-6}	10^{-6}	10^{-8}	–	10^{-8}	–	s
Electron effective mass	$m_e^* =$	$0.146\, m_e$	$0.067\, m_e$	$0.022\, m_e$	$0.83\, m_e$	$0.82\, m_e$	$0.08\, m_e$	$0.40\, m_e$	$0.20\, m_e$	$0.11\, m_e$	–
Heavy hole effective mass	$m_{hh}^* =$	$0.76\, m_e$	$0.45\, m_e$	$0.40\, m_e$	$0.70\, m_e$	$0.60\, m_e$	$0.56\, m_e$	$3.53\, m_e$	$0.80\, m_e$	$1.63\, m_e$	–
Relative dielectric constant	$\varepsilon_r =$	10.1	13.1	15.1	9.8	11.1	12.4	8.5	8.9	15.3	–
Refractive index near E_g	$\bar{n} =$	3.2	3.4	3.5	3.0	3.0	3.4	2.15	2.5	2.9	–
Absorption coefficient near E_g	$\alpha =$	10^3	10^4	10^4	10^3	10^3	10^4	3×10^5	10^5	6×10^4	cm^{-1}
Thermal conductivity	$\kappa_L =$	0.91	0.44	0.27	1.30	0.77	0.68	2.85	1.30	0.45	W/Kcm

- D = Diamond. Z = Zincblende. W = Wurtzite. DOS = Density of states. CB = Conduction band. VB = Valence band.
- The Einstein relation relates the diffusion constant and mobility in a non-degenerately doped semiconductor: $D = \mu\,(kT/e)$
- Minority carrier diffusion lengths are given by $L_n = (D_n \tau_n)^{1/2}$ and $L_p = (D_p \tau_p)^{1/2}$
- The mobilities and diffusion constants apply to low doping concentrations ($\approx 10^{15}$ cm^{-3}). As the doping concentration increases, mobilities and diffusion constants decrease.
- The minority carrier lifetime τ applies to doping concentrations of 10^{18} cm^{-3}. For other doping concentrations, the lifetime is given by $\tau = B^{-1}(n+p)^{-1}$, where $B_{GaN} \approx 10^{-10}$ cm^3/s. $B_{GaAs} = 10^{-10}$ cm^3/s. $B_{GaP} \approx 10^{-13}$ cm^3/s.

1.3.1. AlGaAs/GaAs-Based VCSEL Material System

The AlGaAs/GaAs-based material system (near-IR emission wavelengths (i.e. 850 nm and 980 nm)) is arguably one of the most well behaved semiconductor material systems. Observing Figure 17, we see very little difference in the lattice contrast between AlAs (5.661 Å) and GaAs (5.6533 Å), giving good lattice matching over the entire range of compositions.[25] The specific lattice constants for the III-V binary compounds being considered here can be seen in Table 1, along with other common semiconductor properties. Besides the good lattice matching between the different compositions composing a AlGaAs/GaAs-based VCSEL's epitaxial layers, this material also benefits from having a
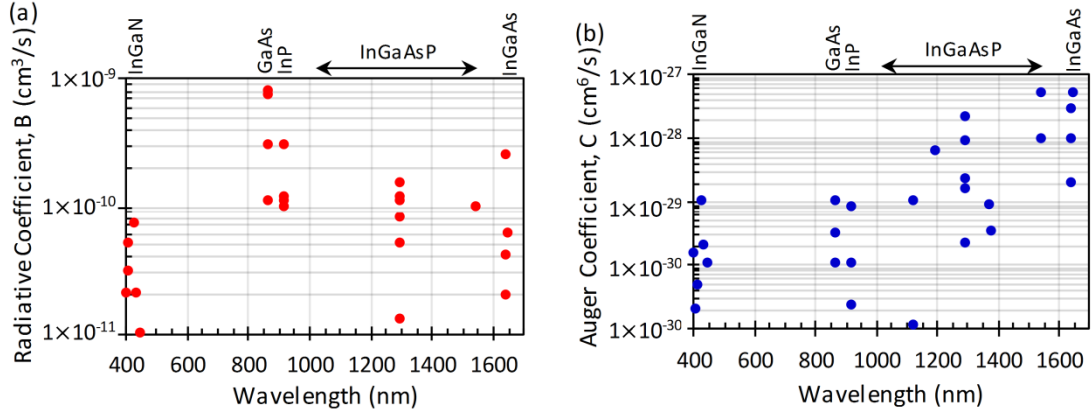
Figure 18 (a) room temperature radiative (bimolecular) recombination coefficients, B, for common III-V compounds discussed here. The radiative recombination coefficient decreases with increasing temperature ($B \propto T^{-3/2}$), due to Fermi-spreading (thermal redistribution) of carriers.[3,6] (b) room temperature Auger recombination coefficients, C, for common III-V compounds discussed here.[6,155,391–398] It is of note that the Auger recombination process for III-nitrides is an indirect, phonon-assisted, process,[399] while longer wavelength semiconductors have a direct Auger recombination process.[3] This difference results in materials dominated by direct Auger recombination processes having Auger coefficients that are more sensitive to temperature.[3,6,400] In both cases, C increases with temperature.

high thermal conductivity (Table 1),[6] a high mobility (i.e. low electrical resistivity) for n-type *and* p-type layers (Table 1), and a high radiative recombination coefficient, *B*, for GaAs QWs (> 1×10^{-10} cm^3/s (Figure 17(a))). In Figure 17(b) we also see that the Auger recombination coefficient is lower than other deeper IR emitting semiconductor materials. Furthermore, the low lattice mismatch allows one to achieve a favorable index contrast for forming high quality epitaxially grown distributed Bragg reflectors (DBRs) and waveguide layers, without suffering from cracking or relaxation. AlGaAs/GaAs-based VCSELs are generally grown using molecular beam epitaxy (MBE).[4]

In AlGaAs/GaAs-based VCSELs, the DBRs are composed of alternating layers (~¼-wave optical thickness) of high and low Al composition AlGaAs layers. For 850 nm emitting devices, where GaAs or InGaAs QWs are used,[4] the Al compositions can be around 15% and 90%,[76] however for longer wavelengths (i.e. 980 nm), where InGaAs QWs are necessary, the low composition AlGaAs layer can simply be replaced by GaAs. Because these epitaxial DBR layers are not only optically active, but also electrically active (i.e.

current transports through them to the active region), their compositions must be uniparabolically graded between the high and low AlGaAs compositions (Figure 19(a)), in order to reduce the series resistance resulting from heterobarriers in the mirrors.[3,77] On top of this, the doping level in the mirror must be varied in order to minimize the free-carrier absorption. This is accomplished by modulating the doping so that the highly doped layers are aligned to the nulls of the standing-wave (i.e. mode/electric field) in the cavity, while the low doped layers are aligned to peaks of the cavity mode (Figure 19(b)).[3] This basic concept of aligning layers with high loss to the nulls of the cavity mode can be applied to many different layers in VCSELs generally, and is a critical consideration for III-nitride VCSELs with ITO intracavity contacts. Furthermore, as will be seen in the III-nitride VCSELs, AlGaAs/GaAs-based VCSELs use a higher number of QWs (e.g. 5QWs for an 850 nm VCSEL [78]) compared to AlGaAs/GaAs-based edge-emitters (1-2 QWs). This is discussed in detail in section 1.4, but it is basically a result of VCSELs generally having a higher total loss (i.e. threshold modal gain) than edge-emitters, and due to the fact that a higher number of QWs allows one to more easily compensate for high levels of loss in a laser.[3,11] Another
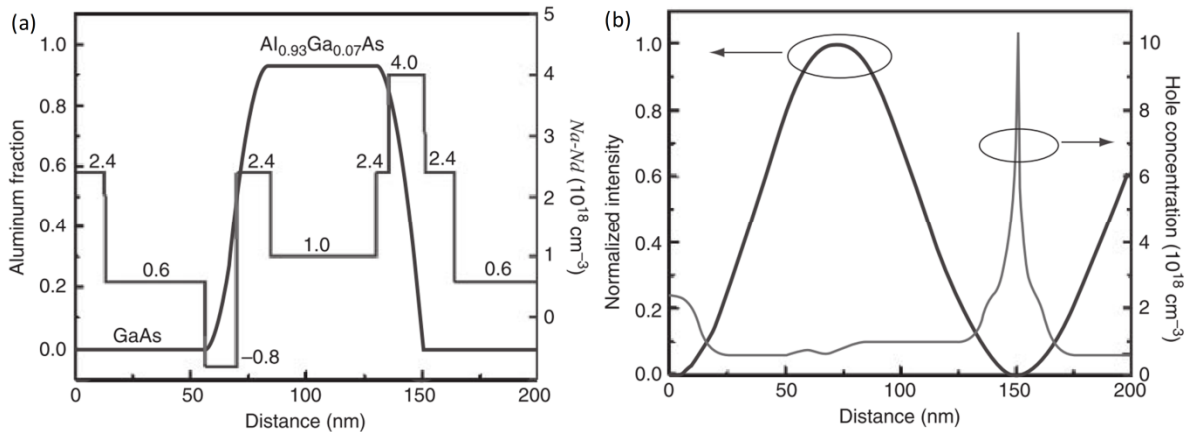

Figure 19 (a) example of uniparabolically graded AlGaAs/GaAs-based VCSEL DBR compositions modulated doping profile, and (b) the overlap between the normalized intensity of the cavity mode and the hole concentration in the p-DBR.[3] Because one of the ¼-wave layers is GaAs, this specific structure is appropriate for a 980 nm VCSEL using InGaAs QWs.

notable advantage of the AlGaAs/GaAs-based VCSEL material system is that the GaAs substrates themselves have low absorption loss for wavelendths exceeding 920 nm. This greatly simplifies the processing for 980 nm InGaAs QW devices, as they can be designed to be bottom emitting.[4]

Finally, the AlGaInAs/GaAs-based VCSEL material system is advantageous to VCSEL fabrication because of the ability to easily form oxide apertures using the well established water steam lateral oxidation of high $Al_{0.98}Ga_{0.02}As$ or AlAs layers.[79] The process involves hydrolyzing the sidewalls of the AlGaAs or AlAs layers in a steam atmosphere furnace at ~400–500 °C, to yield lateral oxidation in the form of Al_xO_y.[4,79,80] This oxide gives very strong electrical and optical confinement which can be controlled to a high degree in terms of its position relative to the standing wave peaks and nulls in the cavity, as well as the degree of tapering of the aperture. A tapered oxide aperture is achieved by varying the Al composition in the oxide layer, which takes advantage of the strong dependence of the oxidation rate on Al composition.[81] This is truly an enabling technology for this material system and greatly simplifies the processing and overal design of these devices.[82–84]

1.3.2. AlGaInAs/InP-Based VCSEL Material System

In the InAlGaAs/InP material system (around 1.3 μm emission wavelengths), the epitaxial growth and processing is complicated by the fragility of bulk InP wafers and the susceptibility to contamination of etched active region sidewalls exposed to air, which can degrade performance. Furthermore, this material system suffers from high Auger

recombination, as well as low radiative recombination coefficients (Figure 18) due to inter-valence band absorption (IVBA).[1] Additionally, the index contrast between epitaxially grown InGaAsP or InGaAlAs DBR layers is small compared to GaAs-based DBRs (~2X smaller),[85] requiring the growth of many more mirror periods to achieve a high reflectivity.[1] This has led most InAlGaAs/InP-based VCSELs to have a hybrid DBR design, where the n-side of the device has an epitaxially grown DBR, while the p-side has dielectric DBR layers, such as MgO, CaF$_2$, ZnS, Al$_2$O$_3$, and a-Si.[1,4] Another alternative approach to achieve a hybrid DBR design is to epitaxially grown GaAs/AlAs mirrors on a GaAs substrate and epitaxially bond to the separately grown GaInAsP/InP epitaxial layers.[86–88] This allows one to take advantage of the improved electrical and thermal conductivity in the GaAs/AlAs DBRs (Table 1). The thermal conductivity of GaAs/AlAs layers is about an order of magnitude higher than the ternary/quaternary InGaAsP or InGaAlAs epitaxial DBR layers grown on InP substrates.[89]

Beyond the requirement for more DBR mirror periods due to the low index contrast, the longer emission wavelength relative to AlGaInAs/GaAs-based VCSELs implies that InAlGaAs/InP-based VCSEL layers are generally thicker, making each ¼-wave DBR layer thicker. The increased total thickness of InP-based DBRs, combined with the lower thermal conductivity for each layer, results in the InP-based DBRs being 20-40X more thermally resistive than GaAs-based DBRs.[4] InP-based mirrors can be made thiner using AlAsSb epitaxial layers, which give a higher index contrast,[90] but the thermal resistance is still greater than GaAs-based DBRs.

The other primary challenge for InP-based VCSELs is that inability to use the lateral wet-oxidation from the GaAs-based VCSELs to yield effective lateral confinement. Because

lateral oxidation is not easily achieved, the aperture is often formed using a buried tunnel junction, and/or a selective undercut etch close to the active region to form an air-gap aperture.[4,91–93] This air-gap aperture is fabricated by selectively etching InAlAs or AlGaInAs in a solution of citric acid and hydrogen peroxide.[92,93]

1.3.3. AlGaInP/GaAs-Based VCSEL Material System

The AlGaInP/GaAs material system is well established for red LEDs, EELDs, and VCSELs. For the case of VCSELs, the primary emission wavelength is 650 nm, where a minimum attenuation can be achieved for POF data transmission (Figure 5).[4] As their name suggests, these VCSELs are actually composed of two different material systems: AlInGaP and AlGaAs. AlGaAs alone can actually provide a direct bandgap down to ~640 nm (Figure 17), however oxygen contamination resulting in non-radiative deep level traps and an onset of carriers populating the indirect band prevent good performance below 750 nm.[4]   For
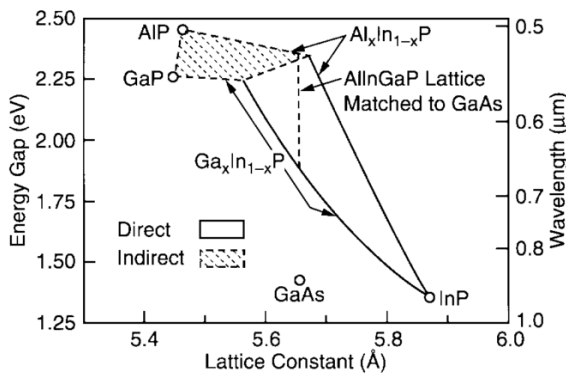
Figure 20 Energy gap and wavelength vs. lattice constant for the relevant compounds used in AlGaInP/GaAs-based VCSELs. The complete AlGaInP quaternary composition is written as $(Al_xG_{1-x})_yIn_{1-y}P$. A 1.9 to 2.26 eV bandgap range (red to green emission) is obtained while simultaneously being lattice matched to GaAs substrates [94]
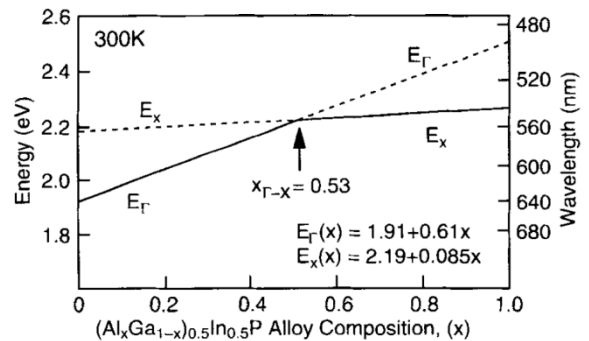
Figure 21 Room temperature bandgaps and wavelengths of the Γ and X bands vs. alloy composition, x, for $(Al_xGa_{1-x})_{0.5}In_{0.5}P$. The direct to indirect transition occurs at $x = 0.53$ (555 nm) [96]

wavelengths below 700 nm, the quaternary compound AlGaInP (or AlInGaP) must be used. This theoretically allows one to extend the emission wavelengths from 700 nm to ~550 nm, as is shown in Figure 20. Also of note from Figure 20, is the fact that AlGaInP is lattice matched to GaAs over its entire composition range. Unfortunately, the efficiency of AlInGaP active regions decreases as wavelength decreases, experiencing a catastrophic fall-off at 555 nm ($x \approx 0.53$ - 0.56) due to the transition from direct (Γ-band) to indirect (X-band) recombination, as is shown in Figure 22.[94–96] The general decrease in efficiency from longer to shorter wavelengths is partially due to a reduction in carrier confinement for shorter wavelengths, which is particularly problematic for VCSELs due to their high carrier density operation.[4]

A notable advantage of the AlGaInP material system, compared to AlGaAs, is the ability to grow efficient devices using metal-organic chemical-vapor deposition (MOCVD), also known as metal-organic vapor-phase epitaxy (MOVPE). This growth technology, which also yields the most efficient III-nitride emitters, is advantageous to MBE because it does not require high-vacuum conditions, yields high growth rates, and can be easily scaled to allow growth on multiple wafers at once. Interestingly, the AlGaInP material system actually faces many of the same challenges as the III-nitrides, primarily as a result of the high activation energies for Mg and Zn p-type dopants. These high activation energies result in low hole concentrations. This issue has been partially overcome by using GaAs substrates with a 6° miscut in the [111]A direction, which improves the p-doping efficiency,[97] while simultaneously improving the carrier confinement by introducing disorder (i.e. increasing the bandgap) of the MQW barriers.[98,99] However, the poor p-type conductivity has been a significant limitation for efficient current spreading in large area devices, such as LEDs.[94]

For LEDs, this has led to extensive development of wafer fusion bonding of AlGaInP epitaxial layers to highly conductive and transparent p-type GaP substrates, which is particularly complicated in the AlGaInP/GaP system due to the high degree of crystallographic alignment necessary to achieve efficient electrical performance.[94] For the case of AlGaInP VCSELs, the issue is not as critical due to the smaller active area and the ability to grow thick epitaxial p-type DBRs.

Similar to GaAs-based VCSELs with 850 nm emission wavelengths, AlGaInP/GaAs-based VCSELs use alternating layers of high and low Al content AlGaAs DBR layers. For the case of red VCSEL n-type DBRs (n-DBRs), $Al_{0.5}Ga_{0.5}As$/AlAs ¼-wave layers are commonly used.[4] These epitaxial DBR ¼-wave layers have low index contrast, thus ~45 or more mirror periods are necessary to achieve the high reflectivity required for non-emitting side of the VCSELs.[4] Because a larger separation in the composition between the ¼-wave layers results in a higher band offset between each layer, using pure AlAs is not ideal from an electrical perspective. However, alloy scattering of phonons generally lowers the thermal conductivity of ternary compounds, relative to their binary compound constituents, thus AlAs is favorable for heat dissipation.[4] Naturally, using the uniparabolic grading techniques described in Figure 19, can balance these electrical and thermal trade-offs, however this also results in a decrease in reflectivity.[100] On the emitting side of the device (top-emitting, p-side) ~30 $Al_{0.5}Ga_{0.5}As$/$Al_{0.95}Ga_{0.95}As$ periods are used.[4] The lower number of periods increases output power, making the device top-side emitting, while moving away from AlAs improves the p-DBR electrical conductivity. Using Zn as the p-type dopant is generally unfavorable due to its tendency to diffuse, which can change the position of the p-n junction in the device, or destroy QW performance.[101] Carbon has a

lower diffusion coefficient than Zn, making it a more ideal dopant for p-type AlGaAs layers.[102]

Beyond the ability to grow epitaxial p- and n-DBRs for AlGaInP/GaAs-based VCSELs, their fabrication is also simplified by the ability to form oxide apertures in the same way as is done in AlGaAs/GaAs-based VCSELs. Overall, the device design of AlGaAs/GaAs-based VCSELs and AlGaInP/GaAs-based VCSELs is very similar due to their similar material advantages. In comparison, the AlGaInP/InP-based share many material issues faced in III-nitride VCSELs, making them more challenging to fabricate.

1.3.4. III-Nitride Material System

The III-nitrides are wide-bandgap semiconductors with emission wavelengths extending from the UV to red (Figure 17, Table 1). The first demonstration of optically pumped stimulated emission in the III-nitride material system occurred in 1971.[103] However it was not until Shuji Nakamura's Nobel prize winning discoveries in the 1990's,[104–111] that III-nitrides research began to accelerate, rapidly leading to commercially viable blue and
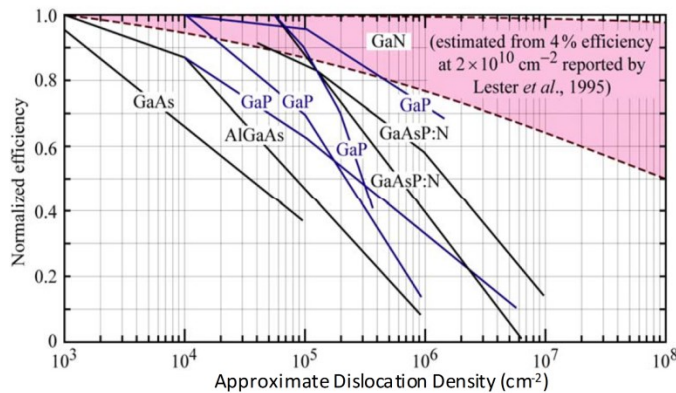
Figure 22 Normalized efficiency vs. approximate dislocation density, measured via etch pit density, showing the high sensitivity of long wavelength emitters to dislocations and the comparably low sensitivity of nitrides to dislocations.[113,117]
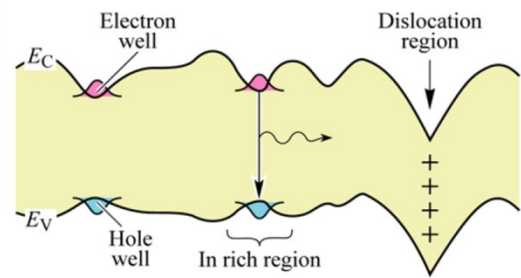
Figure 23 Schematic band diagram conceptually showing how indium fluctuations in the plane of an InGaN QW can lead to localized states that prevent non-radiative recombination at dislocations.[117]

violet light-emitters.[112] Prior to Nakamura's demonstrations of high efficiency nitrides with activated p-GaN, researchers were also not very optimistic about nitrides because of their high dislocation densities. At the time, it was well known that GaAs-based light-emitters were highly sensitive to dislocations (Figure 22), leading many to assume nitrides, with high dislocation densities, would not perform well.[113] However, III-nitrides are less sensitive to non-radiative recombination in dislocations (Figure 22), though they do still improve in efficiency with decreasing dislocation density.[114] The most popular explanation for the reduced sensitivity to dislocations in III-nitrides is InGaN composition fluctuations causing local potential minimas (carrier localization), which prevent carriers from recombining at non-radiative dislocation sites (Figure 23),[112,115,116] however a number of other explanations have also been proposed.[117]

Nitrides are typically grown in the hexagonal, wurtzite, crystal structure, however metastable cubic, zinc-blende nitrides can also be grown in atypical conditions. Figure 24 shows the wurtzite lattice for III-nitrides, with various planes and in-plane directions identified. The asymmetry introduced by the crystal structure, along with the spontaneous polarization field pointing in the c-direction, causes each plane to have very different properties. Initially, III-nitrides could only be grown in the c-direction using such non-lattice matched substrates as sapphire (a_0 = 4.758 Å) or SiC (a_0 = 4.758 Å). [6] Today, these are still the most common growth substrates, with Cree, Inc. being the primary company using III-nitride/SiC technology, and most other companies using III-nitride/sapphire technology. However, in the past decade, bulk GaN substrates have been gaining traction due to the improvements in bulk GaN growth. Naturally, this is the ideal substrate for homoepitaxial growth, however researchers and manufacturers still struggle to achieve reliable growth of
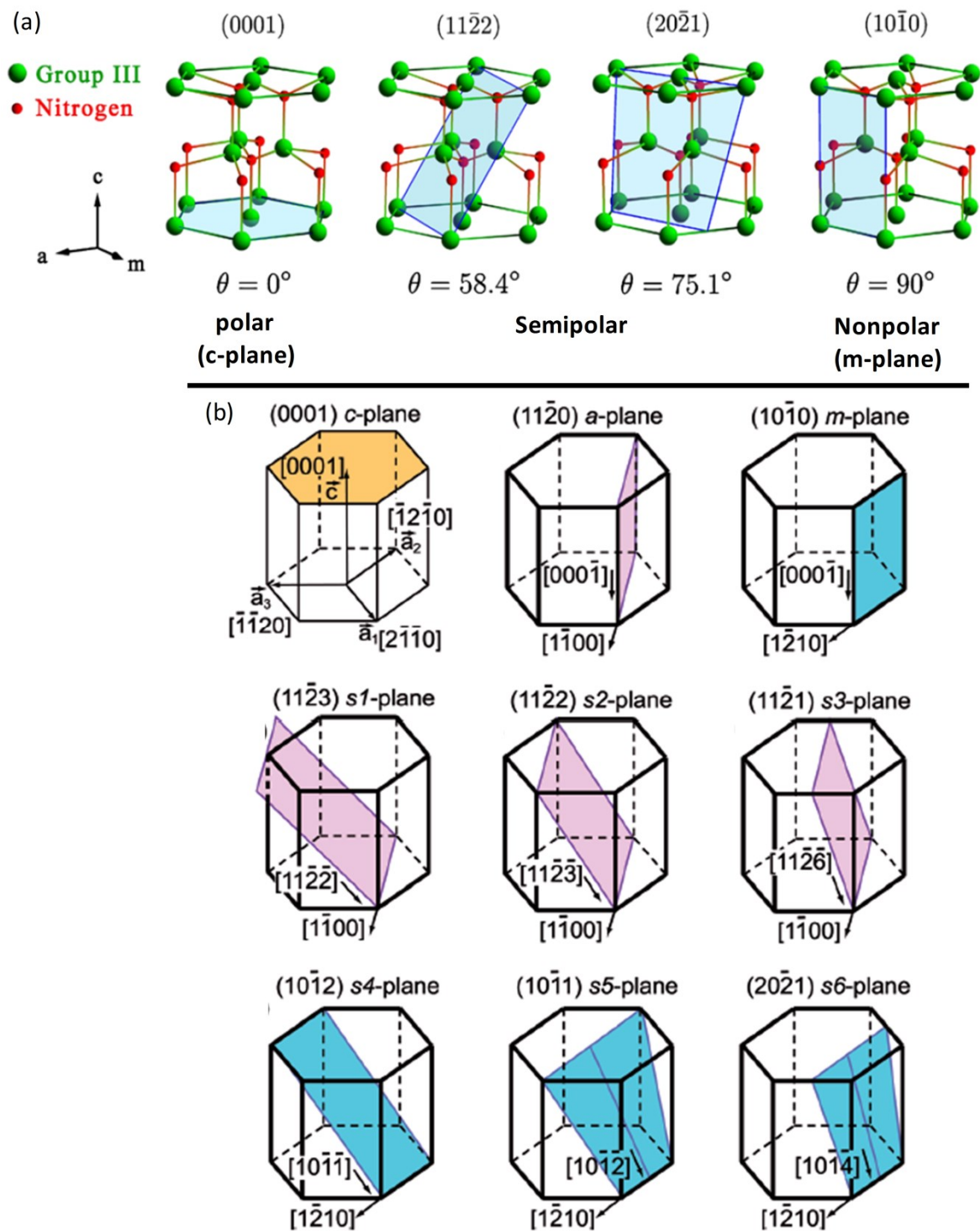
Figure 24 (a) Wurtzite crystal lattice for III-nitride compounds, with common growth planes identified as a function of inclination angle, θ, relative to the (0001) c-plane. The atomic position of the nitrogen atoms and group III atoms in the lattice are shown.[119] (b) Additional schematic diagrams of the III-nitride lattice, with more semipolar and nonpolar planes identified, along with their in-plane directions. In the labels for the semipolar planes, "s" stands for semipolar.[401]

thick, high quality, bulk GaN ingots with large diameters, limiting its competitiveness with other materials that can be more easily grown into large ingots.[118] Most recently, III-nitride/Si substrate technology has received heavy research interest and tremendous progress has been made in this field.[119] Another substrate technology of interest is bulk AlN substrates, which would be particularly well suited for UV emitter applications. For each of these systems, the effect of the III-nitride crystal growth plane (c-plane, semipolar, or nonpolar) on device performance has been intensely researched, with UCSB dominating the field of nonpolar and semipolar epitaxy on bulk GaN substrates. Here, we will predominately focus on homoepitaxy on bulk-GaN, m-plane in particular, as this plane offers unique VCSEL emission characteristics and flip-chip processing techniques.

1.3.4.1. Built-In Polarization Fields

Nonpolar and semipolar III-nitride epitaxy is primarily of interest due to the reduction in electron-hole wave function overlap caused by the spontaneous and piezoelectric polarization fields parallel to the c-direction in InGaN QWs. This is known as the quantum confined Stark effect (QCSE). The name originates from Johannes Stark, who, in 1913, discovered the splitting or shifting of atomic or molecular spectral lines in the presence of an electric field, which is now known as the Stark effect. The parallel in QWs is that the transition energy (bandgap) for confined electrons and holes is reduced under an electric field. In III-nitride QWs, there are two polarization fields (built-in electric fields) present when the diode is unbiased: the spontaneous polarization and the piezoelectric polarization. The spontaneous polarization always points towards the nitrogen face (N-face) and is a result of strong electronegativity of the nitrogen atom creating a strong dipole in the
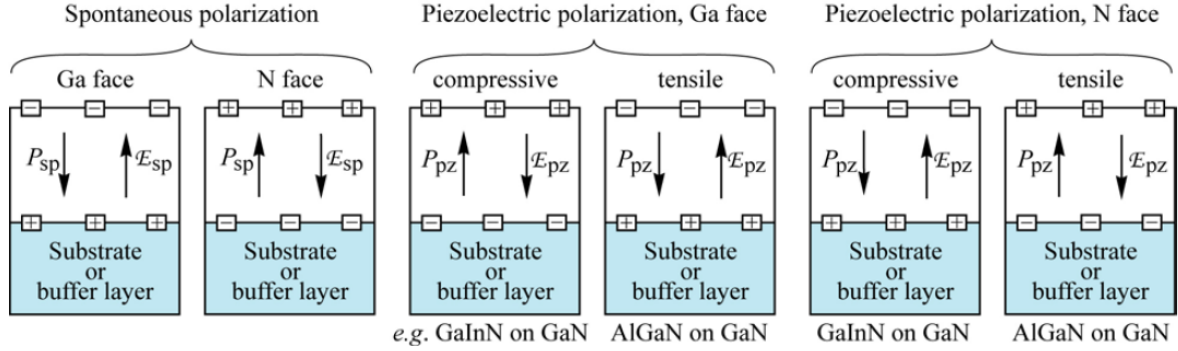
Figure 25 Surface charges and the spontaneous polarization (P_{sp}) and piezoelectric polarization (P_{pz}) field directions for growth on different c-plane faces and with InGaN or AlGaN QWs. The polarization fields point opposite the electric fields (E_{sp} and E_{pz}). c-plane light-emitters are typically grown on the Ga-face with InGaN QWs (for visible light emission) and GaN barriers.[117]

III-N bond.[119,120] The direction of the piezoelectric polarization depends on the strain state (compressive or tensile) for the QW.[117,120] The different cases relevant for III-nitrides are shown in Figure 25 with each device oriented in the c-direction. C-plane III-nitride light emitters are typically grown on the Ga-face, with InGaN QWs on GaN barriers, resulting in the spontaneous polarization pointing towards the n-side of the device, and the piezoelectric polarization point towards the p-side of the device (Figure 25). Due to the increasing in-plane lattice constants of InGaN with increasing In composition, the strength of the polarization is dependent on the allow composition. Furthermore, the asymmetry of the crystal leads to the polarization *in the direction of growth* being dependent on the crystal orientation relative to the c-direction. In Figure 26(a) we see the polarization fields for the case of c-plane InGaN and AlGaN QWs with GaN barriers. The polarization is shown to increase with increasing Al or In composition. For the case of InGaN, the piezoelectric polarization dominates over the spontaneous polarization. Figure 26(b) shows how the polarization, in the growth direction, changes as a function of crystallographic orientation relative to the c-axis. Considering Figure 26(b) with Figure 24 will give the reader a better crystallographic understanding of what the polarization field is like in the growth direction on each plane. In Figure 24 we can see many of the common semipolar and nonpolar planes
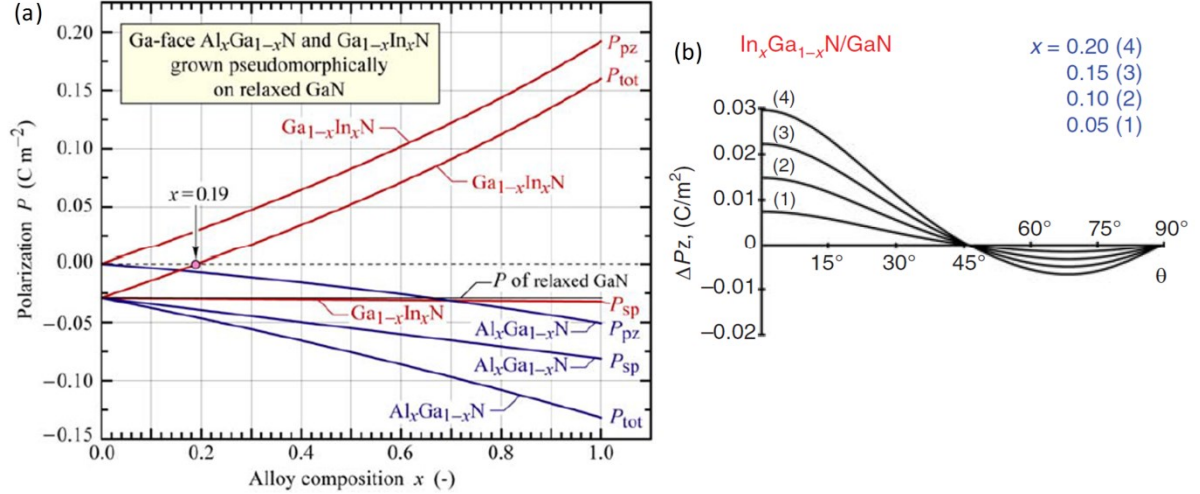
Figure 26 (a) magnitude and direction of spontaneous and piezoelectric polarization in c-plane InGaN and AlGaN QWs with GaN barriers.[117] The strength of the polarization increases with increasing In or Al composition. For InGaN, the piezoelectric field is much stronger than the spontaneous field. For AlGaN, the spontaneous field is stronger than the piezoelectric field. (b) The dependence of the total polarization in the growth (z) direction, ΔP_z, on the crystallographic orientation, θ, relative to the c-direction.[402,403] $\theta = 0°$ corresponds to the conventional c-plane orientation, making $\Delta P_z(\theta = 0°)$ equal to P_{tot} in (a). $\theta = 0°$ corresponds to m-plane. The different crystal planes in the lattice are shown in Figure 24.

on the wurtzite lattice structure. m-plane, which is the primary plane of interest here, is 90°

rotated from c-plane, resulting on no built in polarization in the direction of growth (Figure

26), and no N-face or Ga-face perpendicular to the growth direction. It is important to

realize that the reduced field in the growth direction with increasing angle from the c-

direction (Figure 26(b)) does not imply the fields are disappearing, they have simply rotated

into the plane of the QW. This can be most easily seen in Figure 27, where the band diagram

for an In$_{0.15}$Ga$_{0.85}$N/GaN QW on c-plane and m-plane is shown, along with a schematic

showing the relative surface charges, polarization fields, and crystallographic phases (Ga-

and N-face). In the lower half of Figure 27 we can also see how the QCSE affects the band

structure. Specifically, the QCSE results in a bending of the bands that separates the

electron-hole wave functions. This then results in a reduction of the effective transition

energy for the QW, making the c-plane QW have a 2.60 eV transition energy (~477 nm),

while the nonpolar, m-plane QW has a 2.81 eV transition (~441 nm). The sign and position
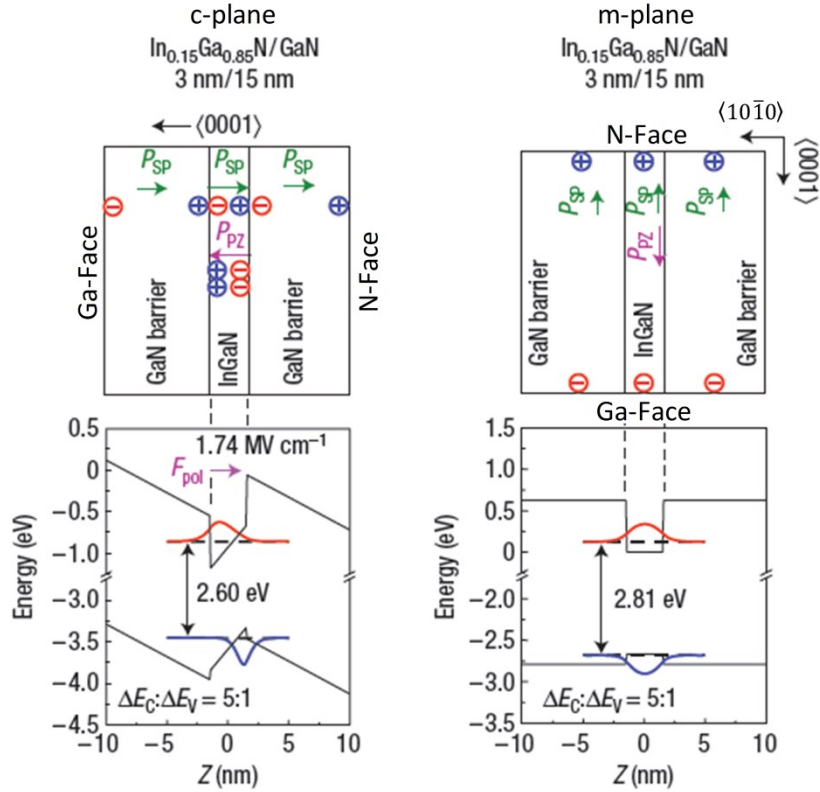
Figure 27 (Top) schematic diagrams showing the direction of polarization fields and the position of surface charges for c-plane and m-plane In$_{0.15}$Ga$_{0.85}$N/GaN QWs. (Bottom) The band structures for the c-plane and m-plane QWs. The QCSE on c-plane results in the bands bending, separating the electron-hole wavefunctions and reducing the transition energy to 2.60 eV from 2.81 eV, for the case of nonpolar m-plane. The conduction band to valence band offset ratio (ΔE_C:ΔE_V) is also shown.[404]

of the surface charges is also important to take note of as it has particular implications for photoelectrochemical (PEC) etching, as is discussed in Section 3.3.1.

Beyond the reduced transition energy caused by the QCSE, the spatial separation of the electron-hole wave functions, decreases the overlap integral (Figure 28(a)), resulting in a reduced radiative recombination rate (the radiative recombination rate is proportional to the electron-hole wave function overlap integral),[3] which then decreases the internal quantum efficiency. Furthermore, with increasing injected current, the bands begin to flatten due to the screening of the built-in polarization fields, causing the transition energy to increase, leading to a large blue shift to shorter emission wavelengths (Figure 28(b)).[121] As can be seen in Figure 28, using nonpolar and semipolar planes can mitigate QCSE related
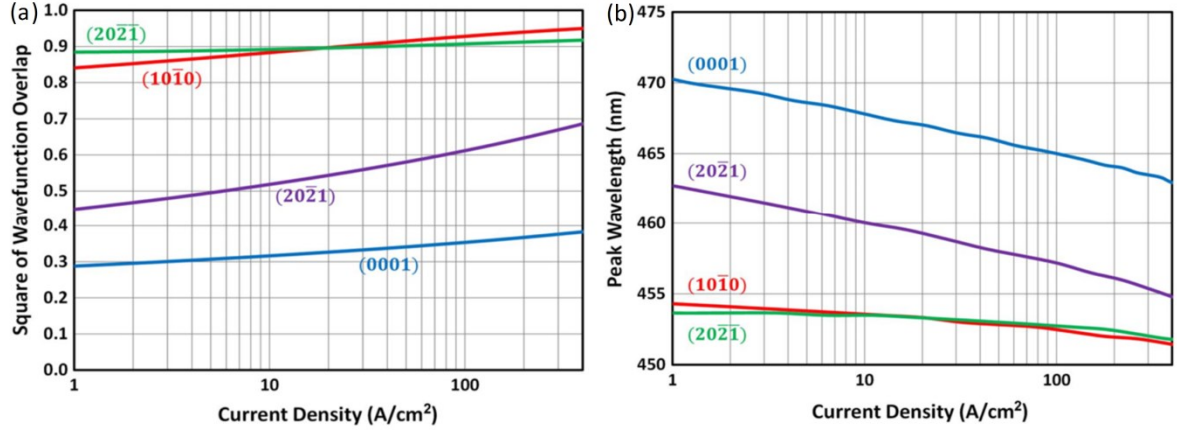
Figure 28 SiLENSe simulations of $In_{0.23}Ga_{0.77}N/GaN$ single QWs on c-plane (0001), m-plane($10\bar{1}0$), and the semipolar planes ($20\bar{2}\bar{1}$) and ($20\bar{2}1$). (a) Square wave function overlap integral vs. current density. (b) Peak wavelength vs. current density.[121]

phenomena on c-plane. Furthermore, using nonpolar and semipolar orientations can also result in a reduced efficiency droop, increased acceptable QW thickness, and reduced leakage current.[119,121] Many of the implications for reducing or eliminating the QCSE are more advantageous for LEDs than lasers, as the carried density in laser QWs clamps at threshold.[3] For lasers, nonpolar and semipolar planes are primarily of interest for their increased material gain and their intrinsically polarized valence band orbitals, which leads to polarized emission.

1.3.4.2. Strain, Gain, & Polarized Emission

The peak material gain is predicted to increase with increasing inclination angle towards m-plane.[122–128] Figure 29 shows the peak material gain vs. QW inclination angle for the case of 3 nm $In_{0.15}Ga_{0.85}N/GaN$ QWs and 3 nm $GaN/Al_{0.2}Ga_{0.8}N$ QWs (carrier density, $N = 2 \times 10^{13}$ cm^{-2}).[122,129] This change in the gain is fundamentally related to the broken in-plane symmetry when the crystal is oriented off the c-axis. The broken symmetry causes the shear strain, ε, matrix elements to vary as a function of inclination angle, as is shown in
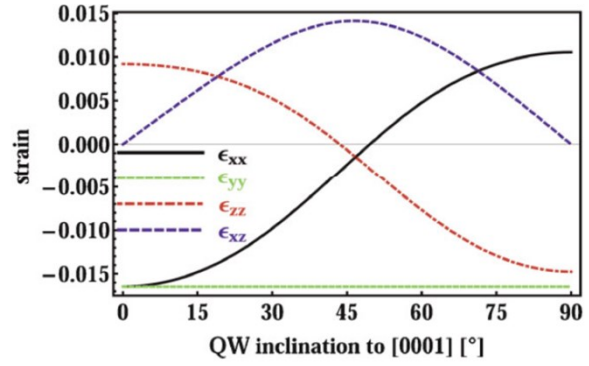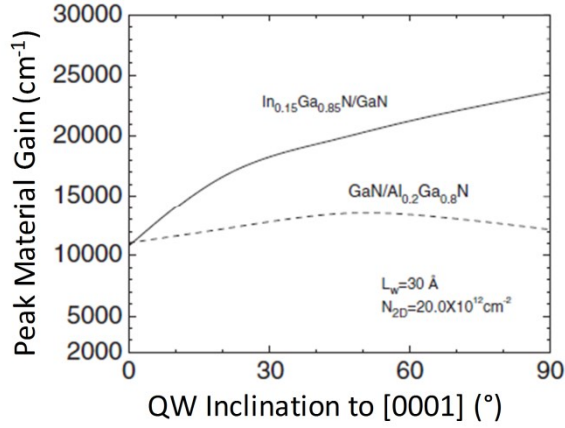
Figure 29 Simulated peak material gain vs. QW inclination off the [0001] c-axis. The case of a 3nm$In_{0.15}Ga_{0.85}N$/GaN QW and a 3nm GaN/$Al_{0.2}Ga_{0.8}N$ QW are shown, for a carrier density of $N = 2 \times 10^{13}$ cm^{-2}. For InGaN/GaN QWs, m-plane ($\theta = 90°$) has the highest peak material gain.[122]

Figure 30 Strain vs. QW inclination off the c-axise. The in-plane strain component ε_{xx} is highest for m-plane ($\theta = 90°$).[124,127,405]

[123,124,127] The band structure in k-space is defined by the shear strain, thus the anisotropic

strain leads to anisotropy in the band structure. The case of the c-plane and m-plane valence

band structures are shown in Figure 31.[127] Here, 3.5 nm $In_{0.15}Ga_{0.85}N$/GaN QWs valence

subbands are shown, with the A1 and B1 valence subbands being the primary bands of

interest, as they will contribute the most carriers to recombination for light emission. On c-

plane, the bands are symmetric about the Γ-point due to the isotropic strain. On m-plane, we

see the anisotropy introduced by the anisotropic strain. The change in the curvature in the

bands leads to a change in the effective mass of holes, as the effective mass of carriers is

inversely proportional to the band curvature, with the average hole effective mass decreasing

with increasing inclination angle towards m-plane. It is also of note that the anisotropy in the

band structure implies the hole effective mass is anisotropic, with holes being lighter when

they travel along the k_y' direction (parallel to the a-direction (a‖) on m-plane)[122,130] This

reduced mass of holes on m-plane is interesting, however it doesn't seem to yield any

significant enhancements in device performance. A more important difference between the

two band structures is the increase in the separation between the A1 and B1 valence
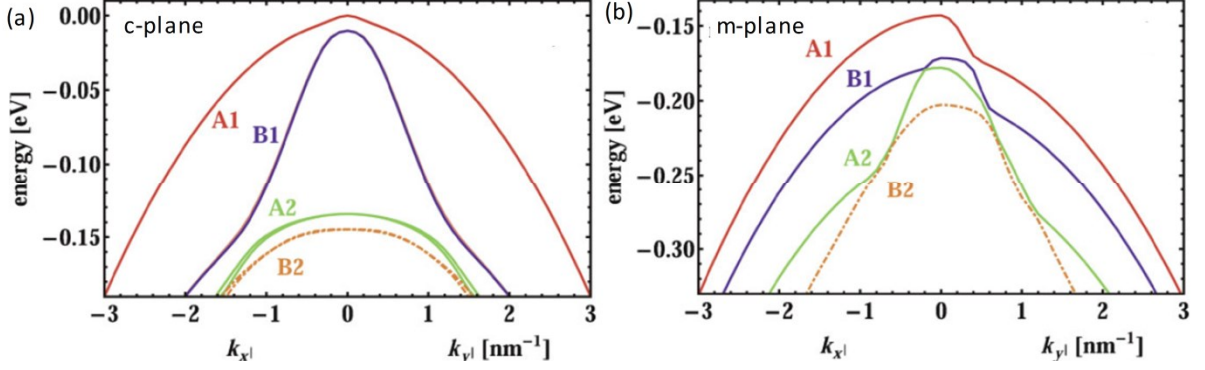
Figure 31 k-space valence structure for c-plane and m-plane orientations of 3.5 nm $In_{0.15}Ga_{0.85}N/GaN$ QWs. C-plane is seen to be axis symmetric, while m-plane is asymmetric. The A1, B1, A2, and B2 valence subbandsare shown. The A1and B1 subbands are sometimes referred to as the heavy-hole (HH) and light-hole (LH) subbands, depending on their relative curvature (the hole effective mass is inversely proportional to the valence band curvature (higher curvature, lighter holes)). The separation between the first and second valence subband increases with increase inclination towards m-plane.[127]

subbands at the Γ-point, $\Delta E_{A1/B1}$. The evolution of $\Delta E_{A1/B1}$ as a function of inclination angle is shown in Figure 32(a). This figure also shows the decrease in the relative Γ-point energy as the inclination increases towards m-plane. The decrease in the Γ-point energy implies a larger bandgap, resulting in shorter wavelength emission for m-plane, as discussed previously. Along with the increase in $\Delta E_{A1/B1}$ on m-plane, we also see an increase in the degree of polarization of the (optical) transition matrix element $|M|^2$ for the A1 and B1 subbands. Here, we do not need to have a very fundamental understanding of what the transition matrix element actually is to understand the implications of this change in polarization, for our purposes, it is sufficient to simply think of the optical matrix element as being proportional to the radiative recombination efficiency or transition efficiency/strength for a given valence subband. This implies that a higher transition matrix element is more favorable for radiative recombination and will yield a higher material gain. The degree of polarization (polarization ratio) for $|M|^2$, P_m, shown in Figure 32(b) is defined as

$$(1) \qquad P_m = \frac{|M_{y'}^m|^2 - |M_{x'}^m|^2}{|M_{y'}^m|^2 + |M_{x'}^m|^2},$$

(a) 0.00

Energy [eV]

A1
B1
A2
B2

$(10\bar{1}2)$ $(11\bar{2}2)$ $(10\bar{1}1)$ $(20\bar{2}1)$

0.025
0.020
0.015
0.010

$\Delta E_{A1/B1}$ [eV]

QW inclination to [0001] [°]

(b)

A1
B1

$(10\bar{1}2)$ $(11\bar{2}2)$ $(10\bar{1}1)$ $(20\bar{2}1)$

polarisation degree of $|M|^2$

QW inclination to [0001] [°]
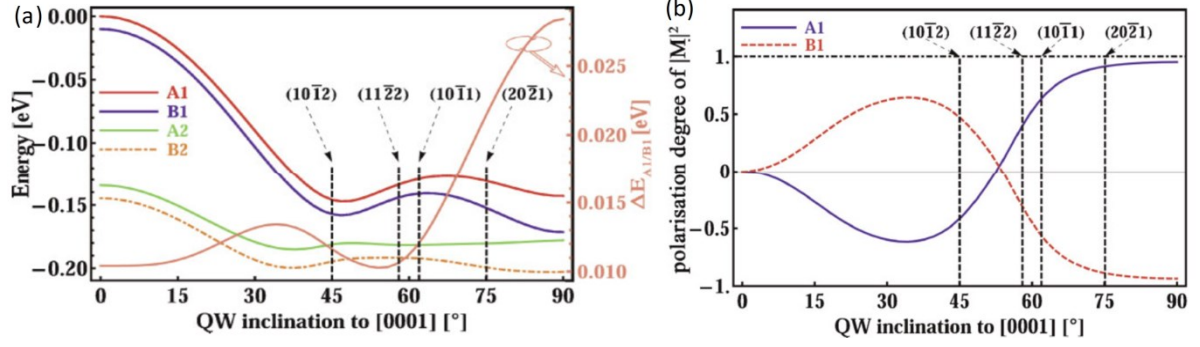
Figure 32 (a) Relative Γ-point energy vs. QW inclination angle for the A1, B1, A2, and B2 valence subbands for 3.5 nm $In_{0.15}Ga_{0.85}N$/GaN QWs. The A1 and B1 bands are the primary bands of interests as they contribute the majority of carriers for light emission. The separation between the A1 and B1 valence subbands, $\Delta E_{A1/B1}$, is also plotted. Experimental values for $\Delta E_{A1/B1}$ can be found in Ref. [406]. (b) The polarization degree of the (optical) transition matrix element $|M|^2$ (i.e. polarization ratio) vs. inclination angle. The polarization degree, P_m, is defined by Eqn (1). $P_m=1$ implies complete polarization parallel to y' (parallel to the a-direction ($a\|$) on m-plane), while $P_m= -1$ implies complete polarization parallel to x' direction (parallel to the c-direction ($c\|$) on m-plane).[127,407]

where $\left|M_{y'}^m\right|$ and $\left|M_{x'}^m\right|$ are the transition matrix elements for conduction band to valence band transitions with orthogonal polarization vectors.[119,127] The meaning of this will become more clear soon. Regardless, from Figure 32(b), we see that c-plane is predicted to have 0 polarization for the A1 and B1 subbands, while for m-plane, each subband is expected to be completely polarized, with the A1 band giving emission polarized parallel to the a-direction (y') and the B1 band giving emission polarized parallel to the c-direction (x'). Because the A1 band will contribute more to the total emission, the light emitted from an m-plane surface will be predominantly polarized in the $a\|$ direction. To more fully understand why this is the case, we must consider the dependence of the transition strength on the angle between the electrons k-vector and an incident electric field.[3] This is dependence is commonly referred to as the spherical representations of the valence subbands (i.e. the angular momentum Eigen functions). Figure 33 shows schematic representations of this concept. In Figure 33(a) we see the complete band structure for bulk c-plane GaN with the spherical representation of the bands overlain with the relevant valence band. Also shown is the conduction bands (CB) interaction strength vs. angle of incident electric field. The

spherical shape of the CB implies that the conduction band interacts with all electric field orientations in the same way (i.e. any electron-hole transition is only defined by the shape of the valence bands spherical representation). Figure 33(b) shows top-down views of the spherical representations of the A1 and B1 valence subbands for the 3.5 nm $In_{0.15}Ga_{0.85}N$/GaN QWs on various crystal orientations. For all cases the k-vector points out of the page.[3] To understand how these shapes lead to polarized emission, first imagine an electric field incident on the crystal shown below each spherical representation. The field oscillates in the plane of the crystal shown and may oscillate in any radial direction about the center of the crystal. The spherical representations of the valence bands represent the intensity with which a carrier in that band would interact with an electric field oscillating parallel to an arbitrary direction. Thus in the case of c-plane, we can see that both the A1
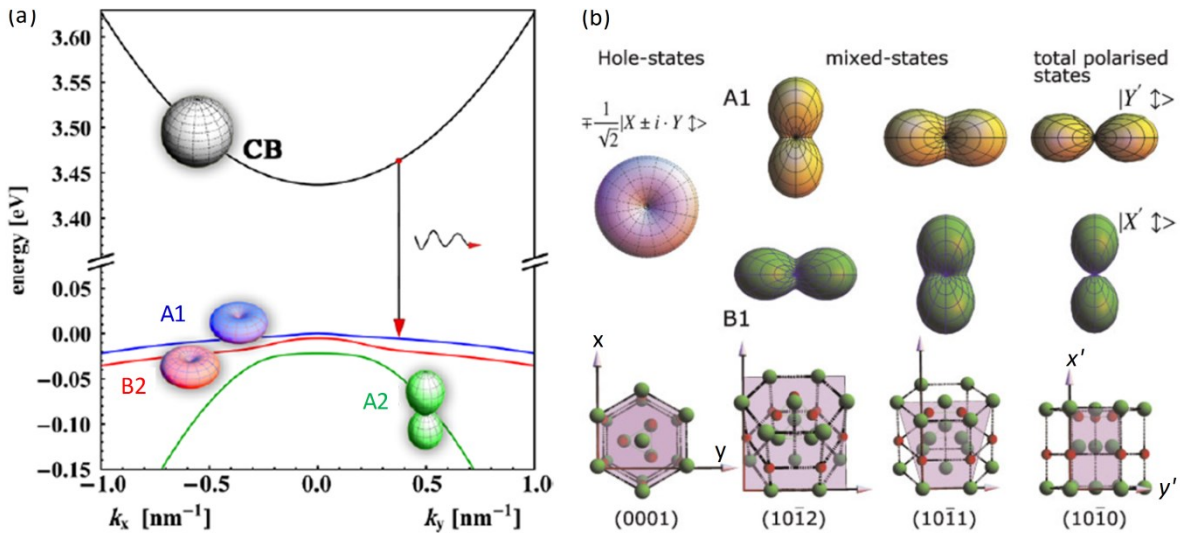
Figure 33 (a) Bulk c-plane oriented GaN band structure showing the spherical representations of the valence bands (angular momentum eigenfunctions) overlain on the relevant valence band.[119] (b) top-down view of the spherical representations (i.e. the dependence of the transition strength on the angle between the electrons k-vector and an incident electric field) for the A1 and B1 valence subbands for various III-nitride crystal orientations with 3.5 nm $In_{0.15}Ga_{0.85}N$/GaN QWs. The k-vector points out of the page in each case. For c-plane, the A1 and B1 bands have the same shape. For all other planes, the anisotropic strain leads to anisotropic shapes. On m-plane, each respective band has a polarization ratio of 100%, with the A1 band interacting with an electric field most intensely when it is parallel to the a-direction, giving a∥ polarized emission, while the B1 band has the strongest transitions when an electric field is parallel to the c-direction, giving c∥ polarized emission.[127]

and B1 subbands have circularly symmetric interaction strengths, meaning the polarization of a given transition does not matter on c-plane. As we move towards m-plane, we see the anisotropic strain leading to anisotropy in the spherical representations. Looking at Figure 32(b) alongside Figure 33(b) we can see how the degree of polarization corresponds to each spherical orbital, where it can be realized that the degree of polarization is proportional to the ratio of the width of the orbital along the *x'* direction relative to the width along the *y'* direction, or visa-versa. The m-plane orbital is seen to have a 100% polarization ratio for the A1 and B1 subbands, giving the ideal dumbbell shape seen in Figure 33(b). This implies that any transition occurring from the A1 subband on m-plane will yield light that is polarized parallel to the a-direction (*y'* direction) with a polarization ratio of 100 %, while any transition occurring from the B1 subband will yield light polarized parallel to the c-direction with a polarization ratio of 100%. Because the carriers in the A1 band have a higher probability of recombining, they will dominate the total emission intensity. Thus, if the total emission from these two bands is analyzed through a linear polarizer filter and spectrometer,
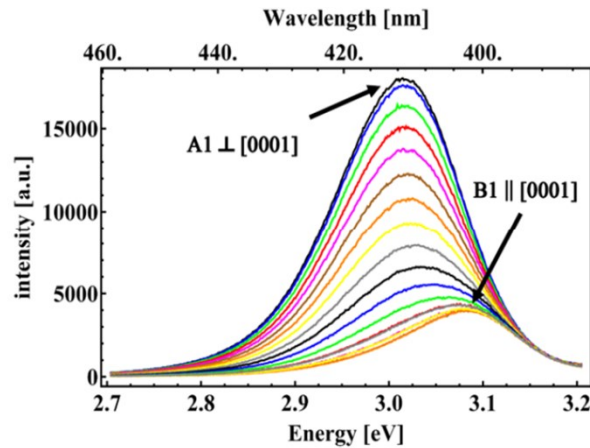
Figure 34 Spontaneous emission spectrum vs. linear polarizer angle for a nonpolar m-plane QW measured at room temperature. The linear polarizer was rotated 5° between each spectrum measurement. The a∥ emission is the most intense, corresponding to the peak interaction strength for the A1 valence band. The c∥ emission has a slightly higher peak energy due to the large transition energy between the conduction band and the B1 subband, while the intensity is lower than that of the a∥ intensity due to the lower number of carriers recombining from the B1 subband.[119]

one would obtain a polarization ratio of less than 100 % because the A1and B1 subbands with orthogonal polarizations would add on top of each other, with the A1 polarized emission dominating, giving m-plane emission predominantly polarized parallel to the a-direction. In experimental measurements, the polarization ratio (i.e. the degree of polarization) is defined as

$$\rho = \frac{I_{\parallel} - I_{\perp}}{I_{\parallel} + I_{\perp}},$$ (2)

where $I_{\parallel}$ for m-plane is the intensity of light polarized along to the a-direction, and $I_{\perp}$ is the intensity of light polarized along the (0001) c-direction.[8] The polarization dependent spontaneous emission spectra for a violet m-plane QW is shown in Figure 34. Besides the most intense emission being a$\parallel$ polarized, corresponding to A1 subband transitions, we can also see the emission intensity for the c$\parallel$ polarization is higher in energy, due the larger separation between the conduction band and the B1 valence subband.

In the case of a laser, the nature of the polarized emission is somewhat more complicated due to the carrier clamping at the threshold condition. Specifically, when the active region is under bias, the equilibrium Fermi level (E_F) separates into the hole (valence band) quasi-Fermi level (E_{Fv}) and the electron (conduction band) quasi-Fermi level (E_{Fc}). To achieve population inversion, required for lasing, the separation between the quasi-Fermi levels must be greater than the separation between the first valence subband and the conduction band (approximately equal to the band-gap). This is shown schematically in Figure 35. Here, we can see the occupation probability functions, f_1 and f_2, overlain with the quasi-Fermi level positions. Also, on the right side we the constant density of state functions, $\rho(E)$, for each subband, resulting in the characteristics staircase function. When this is multiplied by the occupation probabilities, f_1 and f_2 (i.e. the fraction of filled (for

electrons) or empty states (for holes)), we get the electron and hole distribution functions for the conduction and valence subbands, shown in the dot-shaded areas on the right side of Figure 35. The area under these curves is then the total carrier density. In order to maintain charge neutrality, the shaded area under the electron and hole distribution function curves must be equal. In general, the valence band has many more states per unit energy than the conduction band. This implies that the electron quasi-Fermi level must separate more from the equilibrium Fermi level, penetrating further into the conduction band, in order to yield an equal density of states to that of the hole quasi-Fermi level. [3] At threshold, the carrier density is clamped, thus the quasi-Fermi levels clamp. If the threshold carrier density can be reached purely by carriers from the 1st valence subband, then the 2nd valence subband will not contribute to the stimulated emission. Furthermore, because the valence band has many more states per unit energy, it is less likely that the hole quasi-Fermi level will penetrate far enough into the valence subbands to result in carriers from the 2nd valence subband
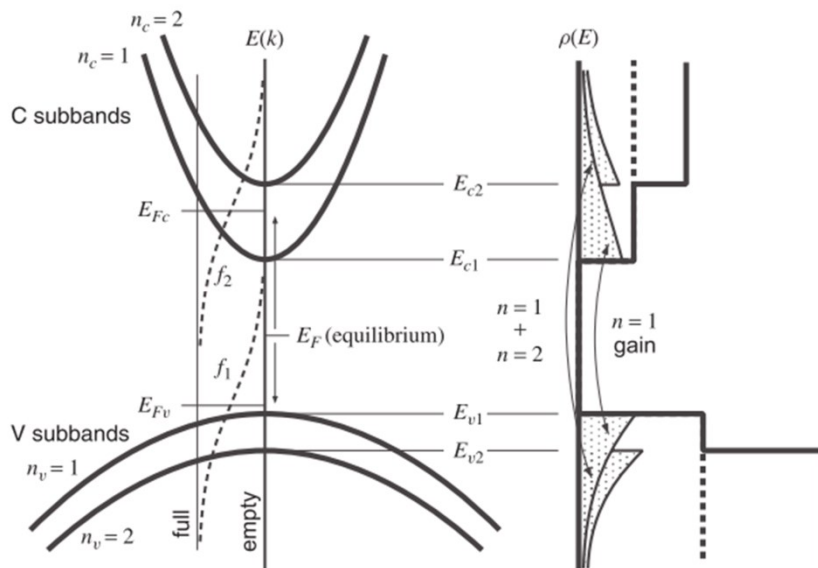
Figure 35 Schematic representation of QW subbands (left) and the corresponding density of states (right), demonstrating the relationship between carrier population, electron and hole quasi-Fermi levels, and the gain at the subband edges. n=1 refers to the first (A1) valence subband, while n=2 refers to the second (B1) valence subband.[3]

contributing to stimulated emission.

With the realization that the 2nd valence subband is unlikely to contribute to stimulated emission, we can now understand why III-nitride nonpolar VCSELs give a‖ polarized emission with a polarization ratio of 100 %, as is shown in Figure 36. When the normalized intensity is plotted on a polar plot as a function of the polarizer angle (Figure 36(b)), we obtain the same dumbbell shape as is predicted for the m-plane A1 valence subband spherical representation (Figure 33(b)). Seeing the stimulated emission from nonpolar VCSELs is polarized also highlights the more complicated nature of the material gain on m-plane QWs. As was shown in Figure 28(a), the peak material gain is highest for m-plane. However, we can now recognize that m-plane has anisotropic gain, with the highest material gain resulting from a cavity mode (electric field) being polarized parallel to the a-direction. Simulations of the a‖ and c‖ gain for m-plane $In_{0.12}Ga_{0.88}N$/GaN QWs are shown in Figure 37.[125]

It should be noted that c-plane VCSELs have been shown to have emission with a polarization ratio of ~80 %,[131–133] which is likely a result of strain introduced by V-defects
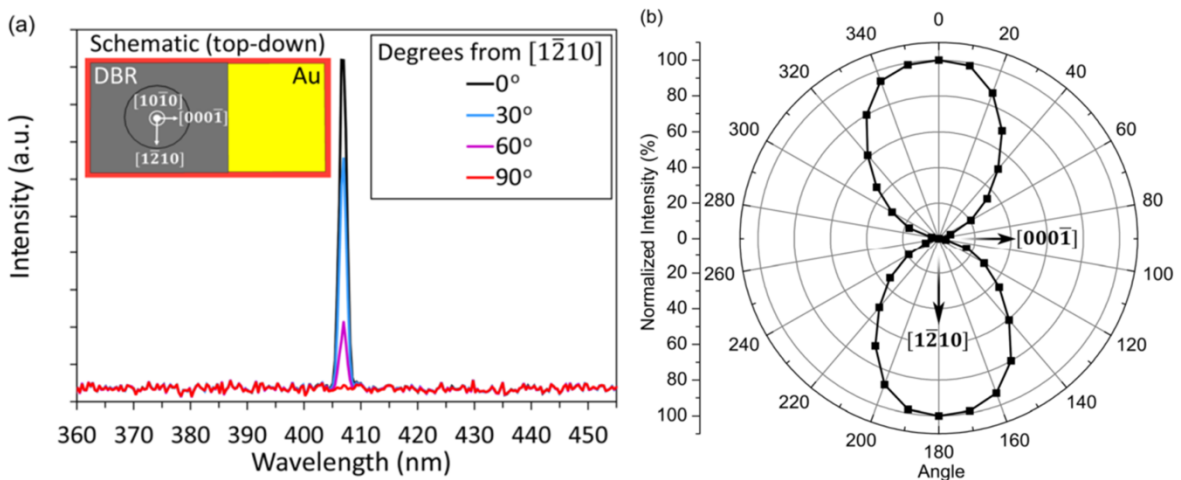
Figure 36 (a) Emission spectra vs. linear polarizer angle for a nonpolar m-plane VCSEL. (b) Normalized intensity peak intensity vs. polarizer angle plotted on a polar plot, demonstrating a‖ polarized emission with a 100% polarization ratio.[8]
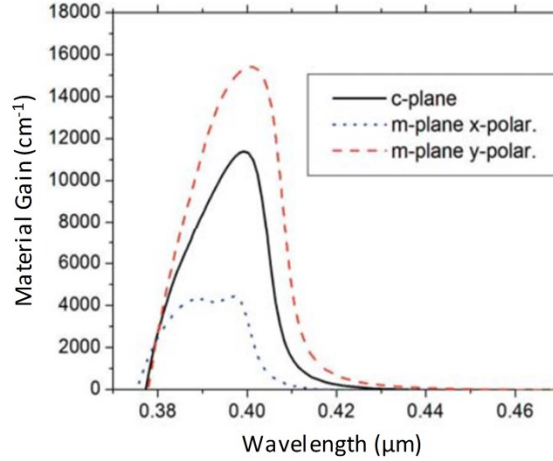
Figure 37 Simulated material gain for a 5 QW $In_{0.12}Ga_{0.88}N$/GaN active region on c-plane and m-plane. The c-plane gain is isotropic, while the m-plane gain is highest for the mode (electric field) polarized parallel to the a-direction (y-polar), corresponding to highest interaction strength with the A1 valence subband.[125]

or the dielectric DBR layers.[119] However, because of the circularly symetric nature of the valence subband spherical representations (Figure 33), one would expect an array of c-plane VCSELs to have random polarizations, giving an average of 0 % polarization. In comparison, the intrisnics polarization of the A1 valence subband gaurentees that an array of m-plane VCSELs would have a polarizatio ratio of 100 %.[12,15] Having a well controlled polarization can be useful for many of the applications discussed in the introduction. Additional discussion on the material properties of m-plane III-nitrides can be found in Section 3.

1.4. III-Nitride VCSEL Design

With an understanding of the history of VCSELs and the basic material properties relevant to each system, we are now ready to consider the different VCSEL. However, to put VCSEL designs in perspective, let us first consider how VCSELs compare to other light emitters.

1.4.1. Design Overview and Advantages

The three primary light-emitting devices used today are light-emitting diodes (LED), edge-emitting laser diodes (EEL or EELD), and VCSELs. Figure 38 shows schematic comparisons of the basic device footpring and emission profile for EELDs, VCSELs, and LEDs. Here, we see that VCSELs have circular output beams with a low beam divergence angle. Like an LED, the beam emits normal to the substrate. The reduced device footprint for VCSELs implies that efficient devices will have a reduced threshold current, and thus reduced thermal heating, compared the EELDs. The small form factor and the emission normal to the substrate also allows VCSELs to be easily fabricated into high density 2D arrays for high-power applications (Figure 39). A number of applications for VCSEL arrays are discussed in Section 1.1.3. For III-nitride nonpolar VCSELs, such arrays are polarization locked, as discussed in Section 1.3.4.2.[12] Table 2 summarizes some of the previously mentioned advantages of VCSELs, while also noting some additional advantages. The simplified mounting and packaging, in particular, make VCSELs excellent laser sources over EELDs for many of the niche applications described in Section 1.1.

Considering the classification of VCSELs more broadly, we can recognize that
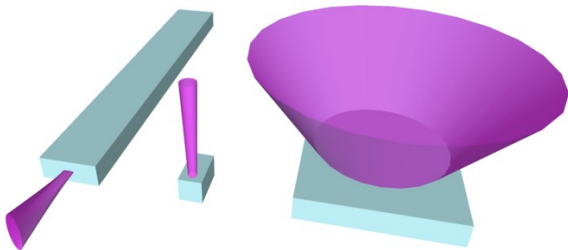
Figure 38 Comparison of profiles, approximate geometries, and approximate divergence angles of edge-emitting laser diodes (EELDs) (left), VCSELs (center), and LEDs (right)
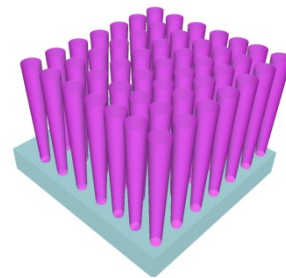
Figure 39 Schematic of a high-density 2D VCSEL array used for high-power applications.

VCSELs are actually only one type of laser within the field of surface-emitting lasers. Though VCSELs are certainly the most well-known surface-emitting lasers, there are others which offer unique properties, including the vertical-external-cavity surface-emitting laser (VECSEL),[134] microdisk (whispering-gallery mode) lasers,[135–140] surface-emitting distributed feedback (SE-DFB) laser,[141–143] electron-beam pumped surface-emitting laser (eVCSEL),[144] and a number of more obscure surface-emitting lasers.[145] *VECSELs* are particularly interesting as they allow one to achieve large output powers (100s of milliwatts) while simultaneously achieving excellent beam quality. These surface-emitting lasers are also appropriate for applications requiring a frequency doubled laser, which were commonly used to achieve green lasing before III-nitride green lasers were developed, and passive mode-locking, which allows the production of a sub-picosecond pulsed laser.[134]

Within the field of VCSELs there are enumerable ways to vary device design to improve optical, electrical, or high-frequency driving performance. Before discussing these specific designs, let us first consider a general structure for a VCSEL. For any laser, a coherent electric field in the cavity (i.e. the mode) can only be formed with sufficient optical confinement in a cavity. Confinement must occur in the axial (longitudinal), lateral, and transverse direction. Schematics showing the directions of confinement in an EELD and VCSEL can be seen in Figure 40. In an EELD, the axial direction (z-direction) is along the

Table 2 Comparison of VCSEL advantages over edge-emitting laser diodes (EELs or EELDs) and LEDs

VCSELs vs. EELs	VCSELs vs. LEDs
Low threshold current	High modulation bandwidth
High efficiency at low power	Focused output beam
Slowly divergent circular beam	Narrow spectrum
Wafer-level testing, low cost	Small operating current
Simplified mounting and packaging	High output power
Two-dimensional arrays	High power conversion efficiency

length of the laser bar, where the confinement is achieved via the reflection of the EELD facets.[3,146] In contrast, the axial direction for a VCSEL, more commonly called the longitudinal direction, is normal to the substrate, where the confinement is achieved via the high reflectivity (HR) top and bottom DBRs. Viewing Figure 40, we can also see that the EELD has different forms of lateral confinement (y-direction) and transverse confinement (x-direction), where the lateral confinement is most commonly achieved via etching a ridge (ridge waveguide), defining the width of the EELD. In the EELD, the transverse confinement is achieved via the epitaxial stack, where the high refractive index active region (high In composition InGaN) is surrounded by lower index separate confinement heterostructure (SCH) layers (low composition InGaN) and cladding layers (GaN and/or AlGaN). In comparison, the VCSEL has radial symmetry in the plane normal to the axial direction, thus the lateral (x-direction) and transverse confinement (y-direction) are achieved using the same method. In a VCSEL, there are many more ways to achieve lateral confinement than longitudinal confinement. Furthermore, the lateral confinement is significantly more complicated than the longitudinal confinement because it effects not only
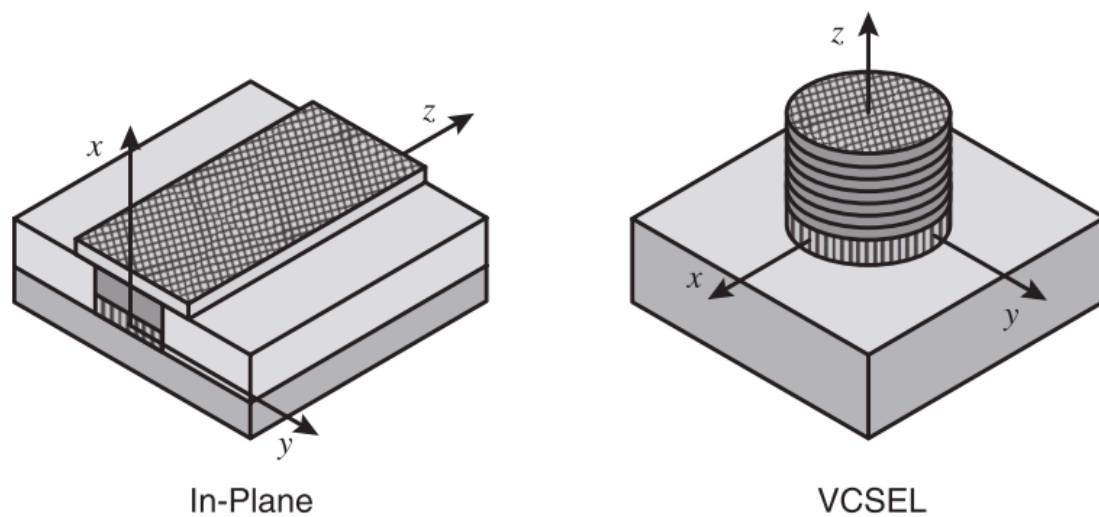
In-Plane   VCSEL

Figure 40 Schematic of an in-plane lasers (i.e. EELD) and VCSEL, showing the coordinate system for modal confinement.[3]

the number of lasing modes, each with slightly different emission wavelengths, just as does the lateral confinement, but is also defines the emission beam profile (i.e. the near-field and far-field pattern), which can be an important criteria for many applications.

To consider the general design of a VCSEL in more detail, we can view Figure 41. Here we see schematic representations of the longitudinal and lateral mode (electric field) profiles. Whether the device has a single longitudinal mode, or multiple longitudinal modes, the longitudinal mode profile always looks the same, though the wavelength of the electric fields for each longitudinal mode in a multi-longitudinal mode VCSEL will be different. A critical criterion for maximizing the confinement factor in a VCSEL is achieving a proper alignment of one of the longitudinal mode peaks (anti-nodes) to the center of the MQW active region, as is shown in Figure 41. This results in a maximum enhancement factor, Γ_{enh}, thereby increasing the total confinement factor. In contrast to the longitudinal mode, the lateral mode profiles vary significantly from mode to mode. In Figure 41 we show the most commonly drawn/considered fundamental linear-polarized (LP) mode, with an azimuthal modal index, l, of 0, and a radial modal index, m, of 1, making it the $LP_{0,1}$ mode (the lowest order LP mode). The lasing behavior of the lateral mode depends on a number of factors, including the aperture design and diameter, the specific operating current above threshold, and the current spreading profile across the aperture. Beyond the mode profiles, we also see the top and bottom DBRs in Figure 41. This particular VCSEL can be identified as a top-emitting device due to the lower reflectivity of the top DBR, resulting from the lower number of mirror periods (9P vs. 12P). Most VCSELs are top-emitting, as the substrate tends to be absorptive, however, 980 nm AlGaAs/GaAs-based VCSELs are often bottom emitting due to the highly transparent and thermally conductive nature of GaAs substrates at
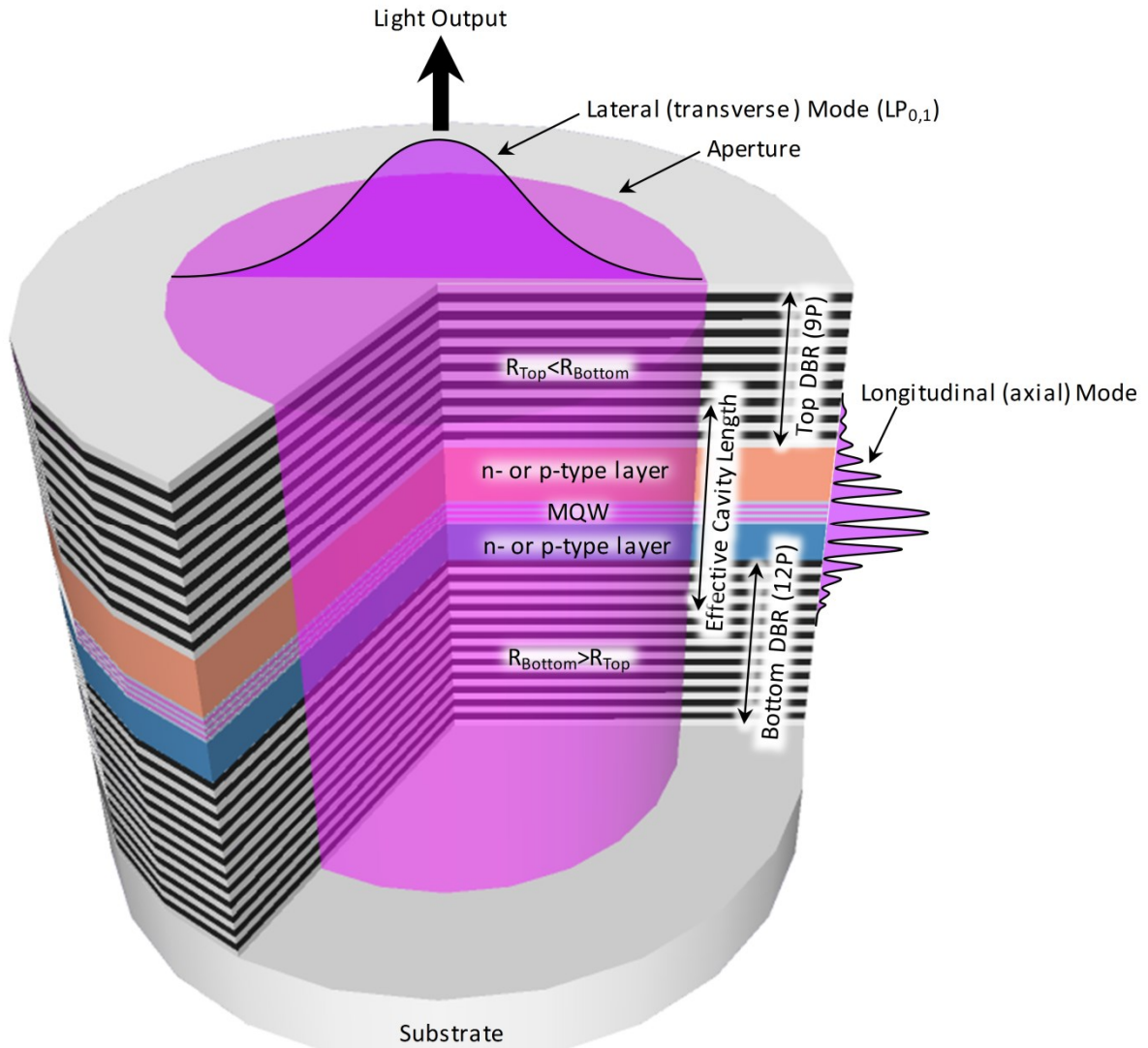
Figure 41 Simple schematic of a VCSEL. This particular device is top-emitting due to the bottom DBR having a higher reflectance (R_{bottom}) than the top DBR (R_{top}). This higher reflectance is a result of the bottom DBR having more mirror periods (P). This example shows a 12P bottom DBR and 9P bottom DBR. The lateral, or transverse, mode (electric-field) is also shown. Here we show only the fundamental linearly polarized (LP) mode, which is the $LP_{0,1}$ mode. The 0 and 1 are referred to as the *l* and *m* modal index. A VCSEL can lase with many lateral modes with different intensity distributions in the aperture. The longitudinal, or axial, mode is also shown. This mode (electric-field) is typically plotted in terms of the normalized electric-field amplitude (E^2-field). In a VCSEL, the peak of the E^2-field is aligned to the MQW active region in order to maximize the enhancement factor (Γ_{enh}) of the laser , which increases the total confinement factor (Γ). The effective cavity length is also shown. This is the true cavity length of a VCSEL, as it takes into account the partial penetration (decay) of the mode into the DBRs. A VCSEL can lase single longitudinal mode, or it may be a multi-longitudinal mode laser. Whether a VCSEL has single or multi-*longitudinal* mode performance does not affect whether it has single or multi-*lateral* mode performance.

that wavelength (Section 1.3.1). The final most significant general design consideration in a VCSEL is the cavity length. We will discuss specific implications of the cavity length later in the text, here we simply wish to highlight the fact that the cavity length is not simply equal to the thickness of the n-type, p-type, and MQW regions, as the mode penetrates into the DBR layers (Figure 41). To account for the modal penetration into the DBRs, VCSEL researchers use the effective cavity length approximation, which essentially approximates the DBR as a simple single-layer mirror with some effective thickness (the effective DBR penetration depth) and some interface reflectivity, equal to the reflectivity of the DBR (Section 1.4.3).

1.4.2. Fundamental Laser Equations

Mirrors are necessary to form a cavity for any laser. In the case of an edge-emitter, the reflectance resulting from the index contrast at the lasers facets is enough to confine the axial mode without any additional coatings, such as DBRs, though such high-reflectivity (HR) or anti-reflectivity (AR) coatings are commonly used to improve performance. In a VCSEL, the longitudinal (axial) mode cannot be confined without DBRs, making them critical to the operation of the device. This is fundamentally rooted in the threshold modal gain and differential efficiency equations. The threshold modal gain, Γg_{th}, is defined as ,

$$(3) \qquad \Gamma g_{th} = \Gamma_{fill}\Gamma_{xy}\Gamma_{enh}g_{th} = \alpha_i + \alpha_m + \alpha_s = \alpha_i + \frac{1}{L_{eff}}\ln\left(\frac{1}{\sqrt{R_p R_n}}\right) + \alpha_s,$$

where Γ is the confinement factor, Γ_{fill} is the fill factor, Γ_{xy} is the lateral confinement factor, Γ_{enh} is the enhancement factor, α_i is the internal loss, α_m is the mirror loss, α_s is the scattering loss, L_{eff} is the effective cavity length, R_p is the p-DBR (power) reflectance (in

the III-nitride flip-chip VCSEL design, primarily of interest here, the p-DBR is the non-emitting side), and R_n is the n-DBR mirror reflectance.[3,9] The differential efficiency, which is a measure of the efficiency of light-output, is defined as

$$(4) \qquad \eta_{d,top} = F_{top}\eta_i \frac{\alpha_m}{\Gamma g_{th}}.$$

Here, we have actually defined the top-side differential efficiency, $\eta_{d,top}$, where we assume the top-side to be the emitting side (though some VCSELs are bottom emitting), since VCSELs are generally designed to minimize the emission on the non-emitting side of the device. In contrast, there are a number of EELD applications which use the emission from both sides of the laser. In Eqn. (4), F_{top} is the fraction of light emitted out the top-side of the device (i.e. out of the n-DBR), and η_i is the injection efficiency.[3] For a given current, a device with a higher differential efficiency will have a higher output power, assuming the two devices being compared have the same aperture diameter. The paragraphs that follow discuss Eqn. (3) and Eqn. (4) in detail.

In Eqn. (3), the (total) confinement factor, Γ, is broken up into its constituent parts for a VCSEL: the fill factor, Γ_{fill}, the lateral confinement factor, Γ_{xy}, and the enhancement factor, Γ_{enh}. The fill factor is define as

$$(5) \qquad \Gamma_{fill} = N_{qw}L_A/L_{eff},$$

where N_{qw} is the number of QWs, and L_A is the active (A) QW thickness (i.e. the thickness of 1 QW), and L_{eff} is the effective cavity length. The confinement factor and enhancement factor are not as easily calculated. The confinement factor can be approximated using 2D wave optics simulations, such as FIMMWAVE, assuming a simple core-cladding model. The enhancement factor requires simulating the mode profile in the cavity and calculating the overlap between a peak of the mode and the active region.[3] The maximum possible

enhancement factor is equal to 2. In an EELD, because the cavity length is so long, the individual peaks and nulls in the axial mode cannot be resolved, thus the enhancement factor is not applicable.

In Eqn. (3), we also see the threshold material gain, g_{th}. This is the required total gain from a set of MQWs composing an active region necessary to reach threshold. If an active region is of poor quality, it may be unable to reach this threshold material gain value, preventing lasing, even in the most well designed laser cavity. It is also important to note that many students new to lasers tend to focus purely on the changes in the threshold material gain between different cavity designs, however this is only valid when the confinement factor does not change between the different designs. It is very easy to get misleading results when only comparing designs based on changes in the threshold material gain.

Next in Eqn. (3), we see the threshold modal gain, Γg_{th}, is equal to the total loss in the cavity, being composed of the internal loss, α_i, the mirror loss, α_m, and the scattering loss, α_s. The internal loss accounts for the various sources of absorption in the material, such as free carrier absorption,[147] or absorption associated with the extinction coefficient, k (the imaginary part of the refractive index), which is proportional to the absorption coefficient, α ($\alpha = 4\pi k/\lambda$). Often times the scattering loss, α_s is dropped from the equation, since it should not be present in an ideal structure. However, the scattering loss can manifest itself in many different forms, making it an important source of loss to keep in mind. In VCSELs, scattering loss is primarily introduced through surface/interface roughness,[9] or roughness around the aperture.[148,149] In EELDs, scattering loss can also result from rough facets, tilting of the facets, or roughness along the length of the EELD.[150–154]

The final term, the mirror loss, α_m, is often called "useful loss". To understand why this is the case, we note that the differential efficiency (Eqn. (4)) increases with increasing mirror loss. This is because the mirror loss is inversely proportional to the p-DBR reflectance, R_p, and the n-DBR mirror reflectance, R_n, as is shown in in Eqn. (3) ($\alpha_m = 1/L_{eff}\ln(1/\sqrt{R_p R_n})$). By reducing the top-side mirror reflectance, we increase the mirror loss, but we also we increase the differential efficiency, by increasing the fraction of light emitted out the top-side of the device, thereby increasing the output power of the devices. Recognizing the relationship between the differential efficiency and threshold modal gain, the two primary equations governing the operation of a laser, can eliminate a great deal of uncertainty about which loss term a given source of loss should be coupled into. For example, in a VCSEL, a significant portion of the mode decays into the DBR. If the DBR layer is absorptive, then do we account for the DBR absorption loss in the mirror loss term or the internal loss term? Because the threshold modal gain is simply a summation of all the sources of loss, it does not really matter which term a specific source of loss is couple into. However, when we consider the differential efficiency, we realize that absorption loss in the DBR would certainly not increase light output, thus it would not increase the differential efficiency, therefore it should not be coupled into the term for mirror loss. Likewise, if the DBR or intracavity contact has a rough surface, leading to a significant amount of scattering loss, one should not simply couple this loss into the mirror loss term because the scattering of the coherent laser light would certainly not increase the stimulated emission output power.

Beyond this general realization, the mirror loss term is also very important because it illuminates one of the fundamental differences between an EELD and VCSEL. In an EELD,

the effective cavity length, which is equal to the laser bar length, is very long (typically in the range of 1,000-10,000 μms), this implies that the reflectivity of the mirrors can be fairly low and the mirror loss will not be unacceptably high to prevent lasing (for specifics on III-nitride EELD mirror loss details, see Ref. 146). In contrast, in a VCSEL, the effective cavity length is very short (typically 1,000s of nms). This short cavity length implies that the p-DBR and n-DBR of a VCSEL must have a very high reflectance (> 99%, with non-emitting side (p-side) being more reflective than the emitting side (n-side)) in order to reduce the mirror loss to an acceptable level. This requirement for a very high mirror reflectance is also why VCSEL are low power lasers (typically 0.1-5 mWs), compared to EELD (typically 100s-1,000s of mW). Specifically, by using a very high reflectance DBR, we significantly reduce the amount of light escaping the cavity per-pass, thus lowering the output power. The low power of a VCSEL often leads many outside the field to think that the devices do not have many applications, however because VCSELs are very small devices, they actually have a very high output power density, allowing the fabrication of high-power emitters composed of 2D VCSEL arrays (Section 1.2). The other primary implication of the shorter cavity length, is the change in the cavity resonance (Fabry-Perot) mode spacing. This is discussed in detail in the next section, however for now it is sufficient to say that the shorter cavity length for VCSELs allows truly single (longitudinal and lateral) mode emission, and also leads to the parabolic-like threshold current vs. temperature dependence (EELDs have exponential threshold current vs. temperature behavior).

The primary implication of differential efficiency equation (Eqn. (4)) in relation to the threshold modal gain equation (Eqn. (3)), has already been discussed. However, beyond the dependence of the differential efficiency on mirror loss, we can also see that it is heavily

dependent on the injection efficiency and fraction of light emitted out the top of the device. The injection efficiency, η_i, is important to highlight here because it points to a very growth/material quality related factor governing the laser performance. The injection efficiency is very difficult to extract from VCSELs, however processing a set of EELDs with a similar active region design as is used in the VCSEL, allows one to carry out length-dependent measurements to extract the injection efficiency. This is something that is commonly done in GaAs- and InP-based VCSELs, but has been unexplored in III-nitrides due to the difficulty in obtaining high quality etched facets for III-nitride EELDs. Besides the injection efficiency, we also see the differential efficiency is directly proportional to the fraction of light emitted out the top-side of the device, defined as

$$(6) \qquad F_{top} = \frac{1-R_{top}}{(1-R_{top})+\frac{R_{top}}{R_{bottom}}(1-R_{bottom})}.$$

This relationship basically highlights the fact that the top-side DBR (i.e. the n-DBR), assumed to be the emitting side of the device, should have a lower reflectance than bottom side DBR (p-DBR), in order to maximize the fraction of light emitted from that side.

The final fundamental laser equation to consider is the relationship between the threshold modal gain and threshold current density. The most popular method for describing this relationship is simply to use a two-parameter or three-parameter fit in a phenomenological function describing experimental measured trends.[3,155] Here, we will simply focus on the three-parameter fit model, which has the form

$$(7) \qquad \Gamma g(J) \approx N_{qw}\Gamma_1 g_0 \ln\left(\frac{J+J_s}{N_w J_{tr_1}+J_s}\right),$$

which can also be written as

$$(8) \qquad J_{th} = (N_w J_{tr_1} + J_s)\exp(\Gamma g_{th}/\Gamma_1 N_w g_0) - J_s,$$

where N_{qw} is the number of QWs, Γ_1 is the *average* confinement factor *per well*, Γ is the total confinement factor, g_0 is the empirical gain coefficient,[155] J_{tr_1} is the transparency current density *per well*,[155] and J_s is a linearity parameter.[155] This describes the general trend of the modal gain vs. current density. It shows that the modal gain increases with increasing current. To calculate the threshold current density, we solve Eqn. (3), set the solution equal to Eqn. (7), and solve for the current density, where the current density is now the threshold current density. Specific simulation results illuminating this equation for different number of QWs and different cavity designs can be found in Section 3.4.1.

In summary, the equations governing the performance of a laser are highly interdependent. There is often a tendency for researchers new to the field to focus on one parameter or the other, however this can lead to the over-optimization of one particular performance metric, such as threshold current density, with the sacrifice of other very important performance metrics, such as output power. Indeed, from Eqn. (3), we can see that we can minimize our threshold modal gain by maximizing the mirror reflectance on both sides of a laser cavity, thereby minimizing the mirror loss, however this will result in basically no light escaping from the cavity (i.e. a low differential efficiency), thus such a laser would be useless for all practical purposes. For this reason, when designing a laser, one must consider each term before deciding one design is better than another.

1.4.3. The Transmission Matrix Method

Before going into the details on the different kinds of DBRs and their relative advantages and disadvantages, we first need to understand some of the fundamental equations used to analyze DBRs. The simplest way to simulate the reflectance spectrum for

a DBR is to use the transmission matrix method (TMM). This is a very simple and elegant formalism for describing the interaction of electromagnetic waves with materials. It can not only be used to describe DBR reflectance spectra, but can also be used to simulate the mode profile in a cavity. All simulations of modes in this thesis use 1D TMM simulations to construct the electric-field (mode) profiles, from which one can calculate the relevant laser parameters discussed in the previous section (Section 1.4.2).

The TMM breaks up a propagating electric fields interaction with a material into two parts: (1) the interaction with bulk of the material/layer, and (2) the interaction with the interface of the material/layer. The transmission matrix describing the propagation/interaction of the field through the bulk of a layer, T_{layer} is defined as

$$(9) \qquad T_{layer} = \begin{pmatrix} e^{i\beta L} & 0 \\ 0 & e^{-i\beta L} \end{pmatrix},$$

where β is the propagation constant, and L is the thickness/length of the particular layer (i is the imaginary unit). Sometimes the product of βL is written as the phase, ϕ. The propagation constant is defined as

$$(10) \qquad \beta = \frac{2\pi n}{\lambda},$$

where λ is the wavelength of interest, and n is the *complex* refractive index, defined as

$$(11) \qquad n = n_{real} - i\,k.$$

Here, k is the extinction coefficient, which is related to the absorption coefficient, α, through the equation

$$(12) \qquad k = \frac{\alpha\,\lambda}{4\,\pi}.$$

It is worth noting that these equations are generally presented in the literature assuming only the real component of the complex refractive index is of interest. The real component is

typically what people are talking about when they mentioned the "refractive index", and is generally what is meant by "n". In modeling lasers though, it is critical to use the complex index in order to account for internal absorption. Here, we will try to present the most general forms of the TMM equations, making them appropriate for use with complex refractive indices, propagation constants, and electric field components. In discussions and equations relevant to the TMM, method n will always refer to the complex index, however elsewhere in this thesis, n will generally refer to only the real component of the complex index.

With an understanding of the transmission matrix describing the electric field propagation through a layer, we can now consider the transmission matrix describing the interaction with an interface. For light passing across an interface from layer 1 to layer 2, the matrix is defined as

$$(13) \qquad T_{12} = \frac{1}{r_{12}} \begin{pmatrix} 1 & r_{12} \\ r_{12} & t_{12}^2 + r_{12}r_{12}^* \end{pmatrix},$$

where r_{12} is the (complex) interface reflectivity for light passing from layer 1 to 2, r_{12}^* is the complex conjugate of r_{12}, and t_{12} is the related interface transmissivity. The reflectivity is defined as

$$(14) \qquad r_{12} = \frac{n_2 - n_1}{n_2 + n_1},$$

where n_1 and n_2 are the *complex* refractive indices for layer 1 and 2, respectively. The interface transmissivity is defined as

$$(15) \qquad t_{12} = \sqrt{1 - \left(\frac{n_2 - n_1}{n_2 + n_1}\right)\left(\frac{n_2 - n_1}{n_2 + n_1}\right)^*}.$$

Here, we explicitly write out the components of Eqn. (14) in Eqn. (15) because r_{12} can actually be modified to account for the scattering of light at the interface.[9] However, while

scattered light will certainly reduce the reflectivity, it will not increase the transitivity of a coherent (in-phase) light wave, which is really what t_{12} is describing, thus it is better for more general purposes to explicitly write out Eqn. (15) in terms of the complex indices of layer 1 and 2.

With these simple building blocks, we can now perform 1D TMM simulations of a cavity mode (electric field), simulate the reflectance spectra for a stand-alone DBR, simulate the reflectance spectra of an arbitrary Fabry-Perot cavity (which is essentially what a VCSEL is), and analyze many more parameters. To simulate a DBR, the matrix only needs to be evaluated once in each layer and at each interface. For example, if we have a DBR composed of m mirror periods of SiO_2 and Ta_2O_5 ¼-wave layers and capped with GaN on the top and Au on the bottom, and we are interested in the reflectance of light coming from the GaN layer, the total transmission matrix for the stack, T_{Total}, would have the form

$$(16) \quad T_{Total} = T_{12}^{GaN/SiO_2}\left(T_{Layer}^{SiO2}T_{12}^{SiO_2/Ta_2O_5}T_{Layer}^{Ta_2O_5}T_{12}^{Ta_2O_5/SiO_2}\right)^{m-1}T_{Layer}^{SiO2}T_{12}^{SiO_2/Ta_2O_5}T_{Layer}^{Ta_2O_5}T_{12}^{Ta_2O_5/Au}.$$

The (power) reflectance, R, is then calculated according to the equation

$$(17) \qquad R = \frac{T_{Total}(2,1)T_{Total}(2,1)^*}{T_{Total}(1,1)T_{Total}(1,1)^*},$$

where the indices in the parentheses refer to the coordinates of a specific matrix element. Similarly the transmission can be calculated according to the equation

$$(18) \qquad T = \sqrt{1 - \frac{T_{Total}(2,1)T_{Total}(2,1)^*}{T_{Total}(1,1)T_{Total}(1,1)^*}}.$$

Simulating the electric field in a cavity (i.e. the mode) is a bit more complicated, but still relatively simple. First, the mode being simulated must be for a resonance wavelength (frequency), otherwise it will not be confined to the cavity and the profile will basically

show a giant field in free space and no field in the cavity. Next, because we are actually interested in the profile slightly beyond the edge of the cavity, i.e. in air, we must also add some T_{layer} matrices to the front and back ends of Eqn. (18). To make the simulation as simple as possible, it is best to just set these two layers to be ¼-wave thick (i.e. a ¼-wave of air and a ¼-wave of gold). To calculate the electric field (mode) intensity, E^2, we use the equation

$$(19) \qquad E^2 = \frac{T(1,1)+T(2,1)^2}{n_{Re}}.$$

Where T represents the product of all transmsission matricies up to that point in the structure. So, to evaluate the field at an arbitrary position in the structure, we simply break up the transmission through a layer, T_{layer} (Eqn. (9)) into an arbitrary amount of T_{layer} matrices representing the field's propagation over an arbitrary distance L. We multiply each T_{layer} matrix for the distance L by the previous T_{layer} matrix, until an interface is reached, where we then use the T_{12} matrix. At each point, before multiplying instantaneous T_{Total} by the next matrix, we evaluate E^2 for that particular point. This then gives us the mode profile vs. distance in a cavity. Additional details on the TMM can be found in Ref. 3.

Carrying out this TMM simulation of the mode allows one to easily determine some classical VCSEL internal parameters, including the gain per pass, G, the loss per pass, A_i, the top-side transmission per pass (i.e. the transmission up per pass), $T_{m,up}$, and the bottom-side transmission per pass (i.e. the transmission down per pass), $T_{m,down}$. Sometimes these terms are written as "round-trip" instead of "per-pass", where the "per-pass" value is simply ½ the round trip value. These dimensionless terms can be related to the more popularly used laser terms from Eqn. 55 by simply multiplying by the effective cavity length. Specifically, the set of relevant equations are

$$(20) \qquad G = A_i + \frac{T_{m,up}+T_{m,down}}{2} = \Gamma g_{th} L_{eff},$$

$$(21) \qquad A_i = \alpha_i L_{eff},$$

$$(22) \qquad \frac{T_{m,up}+T_{m,down}}{2} = \frac{\ln(1/R_{top})+\ln(1/R_{bottom})}{2} = \alpha_m L_{eff}.$$

With the classical internal parameters for VCSELs calculated from the TMM, the final step

for converting from the dimensionless values to the more commonly used laser parameters

Γg_{th}, α_i, and α_m is to determine the effective cavity length, L_{eff}. Most of the components

defining the cavity length, such as the n-type, p-type, and active region, have well defined

thicknesses, however, as mentioned previously, because the mode has a significant intensity

distribution in the DBRs themselves, some of the DBR layers will also makeup part of the

effective cavity length. To account for this, a formalism has been developed that essential

treats a DBR stack as a single layer and an interface with the same reflective properties as

the full DBR stack.[3] The effective modal penetration depth into a DBR, $L_{DBR,eff}$, is the

"length" of this single layer representation. It is calculated according to the equation

$$(23) \qquad L_{DBR,eff} = \frac{1}{2}m_{eff}\Lambda\left(\frac{1}{1+r^2} - \frac{1}{2\,m_{eff}}\right),$$

where m_{eff} is the effective number of mirror periods, Λ is the thickness of 1 mirror period

($\Lambda = \frac{\lambda}{4\,n_2} + \frac{\lambda}{4\,n_1}$), and r is equal to Eqn. (14), where layer 2 is the higher index material in

the DBR stack, and layer 1 is the lower index material in the stack. Here, it is better to *not*

use the complex refractive indices (i.e. only use the real part), as a non-zero extinction

coefficient (i.e. absorption) in a DBR layer should be accounted for in the value for the

internal loss, not the mirror loss, due to the implications on the differential efficiency

discussed in the previous section (Section 1.4.2). The effective number of mirror periods,

m_{eff}, is defined as

$$(24) \qquad m_{eff} = \frac{\tanh(m \ln(n_2/n_1))}{\tanh(\ln(n_2/n_1))} \; .$$

After the effective DBR penetration depths for the p-DBR and n-DBR are calculated, one

simply adds these thicknesses the cumulative thickness of the other cavity layers to get the

effective cavity length.

In VCSELs, it is most common to refer to the cavity length in terms of its optical

thickness. The cavities optical thickness, χ, is defined by the equation

$$(25) \qquad \chi = \frac{L_{eff} n_{eff}}{\lambda} ,$$

where n_{eff} is the effective index of the cavity. The effective index is obtained by

performing a weighted average of each layers refractive index relative to its interaction with

the mode (i.e. the magnitude of the E^2-field throughout the layer obtained using the TMM).

Naturally, the thicker a cavity is, the less the DBR layers contribute to the total effective

cavity length. Likewise, the thicker the cavity, the less the refractive indices of the DBR

layers will contribute to the total effective index of the cavity.

To carry out any of these calculations, we require refractive index dispersion data for

all the relevant layers being considered. Figure 42 gives index dispersion data for the various

materials used in the dual dielectric DBR VCSELs discussed in this thesis. In Figure 42(a)

we see index dispersion data for various InGaN compositions, with the $In_{0.1}Ga_{0.9}N$

dispersion being the most relevant to 405 nm emitting VCSELs. Figure 42(b) shows AlGaN

index dispersion. In all III-nitride VCSELs, AlGaN is used for the electron-blocking layer

(EBL). The VCSELs presented here typically have 15-20% Al content AlGaN EBLs.

Because this layer is a very small fraction of the entire cavity, the specific index value is not

very important, so we simply used the $Al_{0.15}Ga_{0.85}N$ dispersion data. It is of note that m-

plane actually has birefringent index dispersion, as a result of the anisotropic strain,
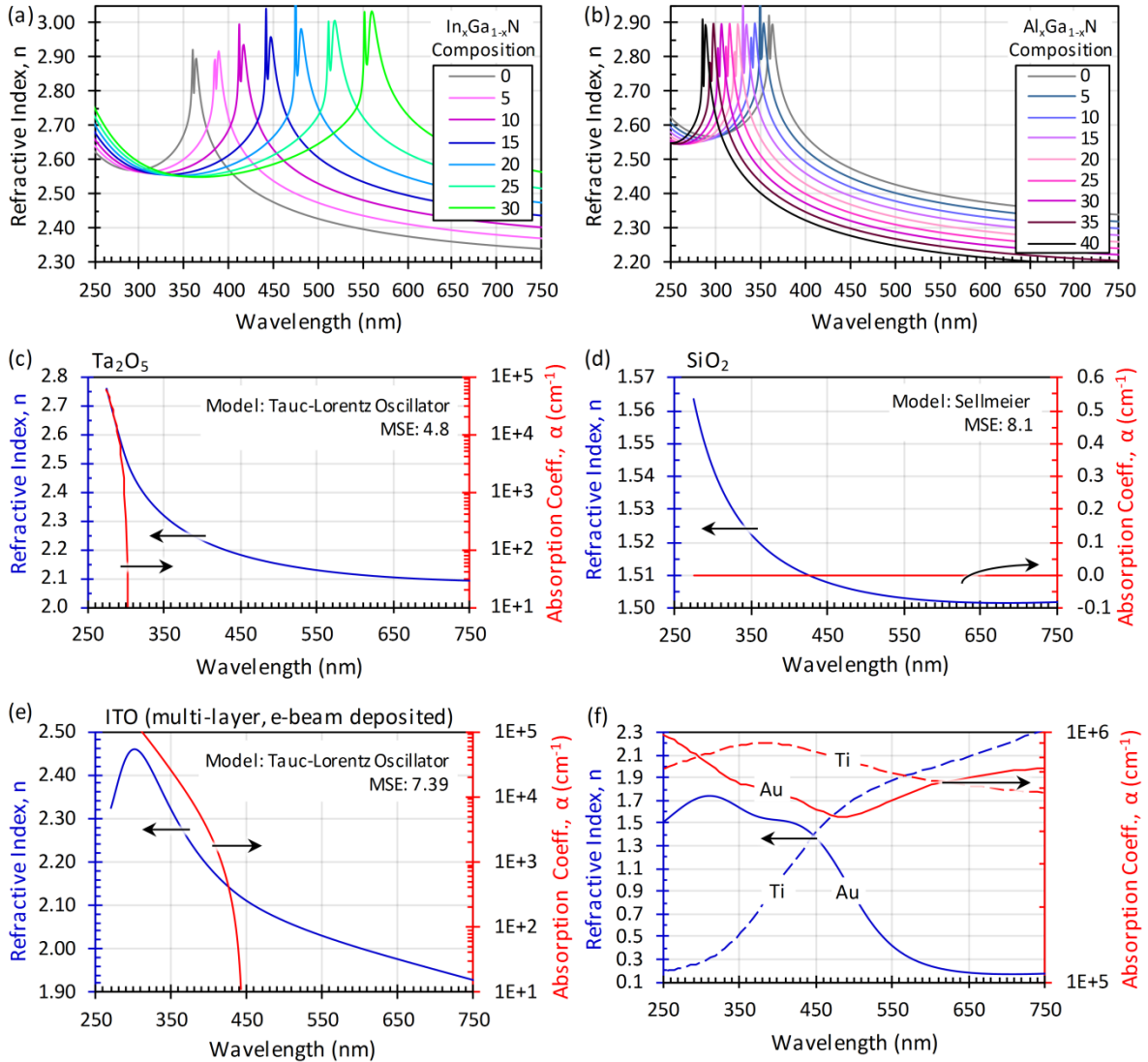
Figure 42 Refractive index dispersion data for the various materials used in the violet (405 nm) dual dielectric DBR VCSEL presented here. (a) shows InGaN dispersion for various compositions.[408] (b) shows AlGaN dispersion for various compsotions.[408] (c), (d), and (e) show experimentally measured dispersion curves for Ta$_2$O$_5$, SiO$_2$ and ITO. The ellipsometry models used to fit the experimental data are stated in the inset. The mean-square-error (MSE) for the fit is also shown, with all samples showing a low MSE (<10). The Ta$_2$O$_5$ and SiO$_2$ films were deposited on Si substrates via ion-beam deposition (IBD) which is also used to form the DBRs in the dual dielectric VCSELs. The ITO films were optimized multi-layer e-beam deposited films on Si substrates.[9] (f) shows index dispersion for Ti and Au, which is coated on the back-side of the p-DBR and represents the last two layers on the back-side of the device in the model. The Ti and Au dispersion data is taken from Refs. 409,410.

discussed in Section 1.3.4.2, however these minor changes in the refractive index do not really effect the actual experimental results very much, and we are only interested in the refractive index dispersion for a field polarized parallel to the a-direction anyways. Comparing (a) and (b) to the rest of the figures in Figure 42, we note that there is no

absorption coefficient dispersion plotted. This is because the epitaxial layers of the cavity can have significantly varying absorption coefficient depending on the crystal quality, doping levels, and contamination levels. Because of this, we generally use very rough estimates for the absorption coefficients in each of the epitaxial layers. Though this may bring into question the accuracy of the models in presenting physically true results that would be manifest in a measured device, the main goal of modeling is to discover relative trends in changing laser design, rather than giving as accurate of a threshold modal gain, or other parameter, as possible. That being said, even the simple models presented in this thesis do seem to have a good correlation with the threshold modal gain and threshold current density of the more recent generations of nonpolar VCSELs. Next, in (c) and (d) we see the dispersion for the dielectric layers (SiO_2 and Ta_2O_5) used in the dielectric DBRs for the VCSELs presented here. It is of note that both these materials show no absorption loss near 405 nm, thus they are lossless DBRs. (e) shows the measured dispersion for the multi-layer e-beam deposited ITO films[9] used prior to the develop of tunnel junction (TJ) intracavity contacts.[11] As can be seen, the absorption coefficient of ITO at 405 nm is quite large (~2000 cm^{-1}), which is a very fundamental issue for achieving high performance violet VCSELs. This is discussed in more detail in Section 4.1. Finally, (f) shows the index dispersion for Ti and Au. These layers do not really interact with the mode, as they are coated on the back-side of the p-DBR, but they are necessary for modeling and they can introduce significant absorption losses if too few p-DBR layers are used.

With a brief background in the TMM and its applications to VCSEL and DBR modeling, we are now in a good position to discuss DBR and VCSEL designs more generally.

1.4.4. Distributed Bragg Reflectors (DBRs)

1.4.4.1. General DBR Design Considerations

There are three primary types of distributed Bragg Reflectors (DBRs): (1) epitaxial DBRs, (2) dielectric DBRs, and (3) air-gap DBRs. In III-nitride VCSELs, only dielectric and epitaxial DBRs have been used to date, however a number of groups have demonstrated the fabrication of III-nitride air-gap DBRs,[156–158] and air-gap DBRs have also been demonstrated for InP-based VCSELs.[159] While air-gap DBRs have some optical advantages (wide mirror stop-band, large index contrast, etc.), they are certainly the worst DBRs in terms of thermal performance, making them mostly of interest from a research perspective. In choosing a DBR for a VCSEL design, there are 3 basic considerations: (1) The ease of fabrication/growth, (2) the index contrast between the ¼-wave layers and the resulting DBR stop-band, and (3) the thermal conductivity of each of the layers. The poor electrical conductivity and high absorption loss in the p-type III-nitrides[160–164] has led all researchers to use dielectric DBRs for the p-side of the device (p-DBR). III-nitride VCSELs with an epitaxial n-DBR and a dielectric p-DBR are known as hybrid DBR VCSELs, whereas VCSELs with dielectric p- and n-DBRs are known as dual-dielectric DBR VCSELs. These two types of VCSELs are schematically represented in Figure 43. The epitaxial DBR can be formed from an AlN/GaN (or AlGaN/GaN) stack,[132,165] or an AlInN/GaN stack.[166–169] AlN/GaN-based epitaxial DBRs are difficult to grow due to the high lattice mismatch between AlN and GaN (Table 1), leading to catastrophic cracking.[165,170] This effect is particularly difficult to overcome in VCSEL DBRs because many mirror periods are necessary to achieve the very high reflectance (>99 %) required to minimize the mirror loss.
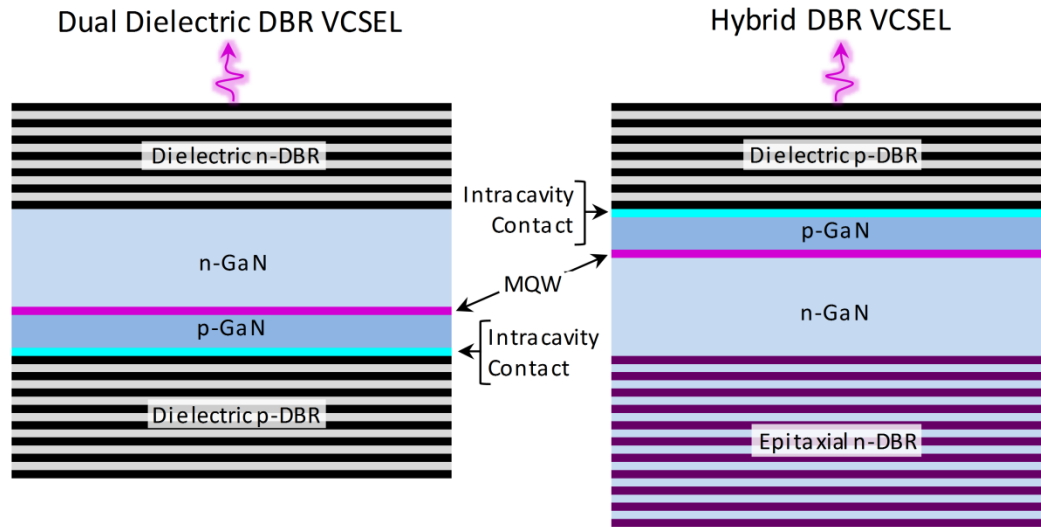
Figure 43 Schematic representations of typical dual dielectric DBR (left) and hybrid DBR (right) VCSEL cavity designs. The fact that the dual dielectric DBR VCSEL emits out the n-DBR side, implies it is a top-emitting flip-chip VCSEL. The hybrid DBR is shown to be emitting out the p-DBR side, thus it is not a flip-chip device.

Furthermore, because all demonstrated hybrid DBR III-nitride VCSELs are top-emitting, making the epitaxial DBR on the non-emitting side of the device (Figure 43), the reflectance of the epitaxial DBR needs to be as close to 100% as possible. If hybrid DBR VCSELs were designed to be bottom-emitting, one could possibly reduce the total thickness of the DBR stack, thereby mitigating many of the strain related issues of associated with AlN/GaN epitaxial DBRs. Another issue unique to c-plane epitaxial DBRs is the presence of V-defects. Figure 44(b) and (c) show TEM cross-sections of an AlN/GaN epitaxial n-DBR used on a 450 nm c-plane VCSEL, where the presence of V-defects can be seen. The V-defects introduce a significant amount of interface roughness, leading to scattering loss and local variations in the DBR reflectance.[132] Here, we also see superlattices (SLs) present in the DBR, which serve to prevent cracking by compensating the strain built-up in the underlying layers. In contrast, to AlN/GaN-based DBRs, AlInN/GaN-based DBRs do not suffer from the same strain related issues. Unfortunately, AlInN is notoriously difficult to grow, tending to yield films with significant compositional clustering. However, a
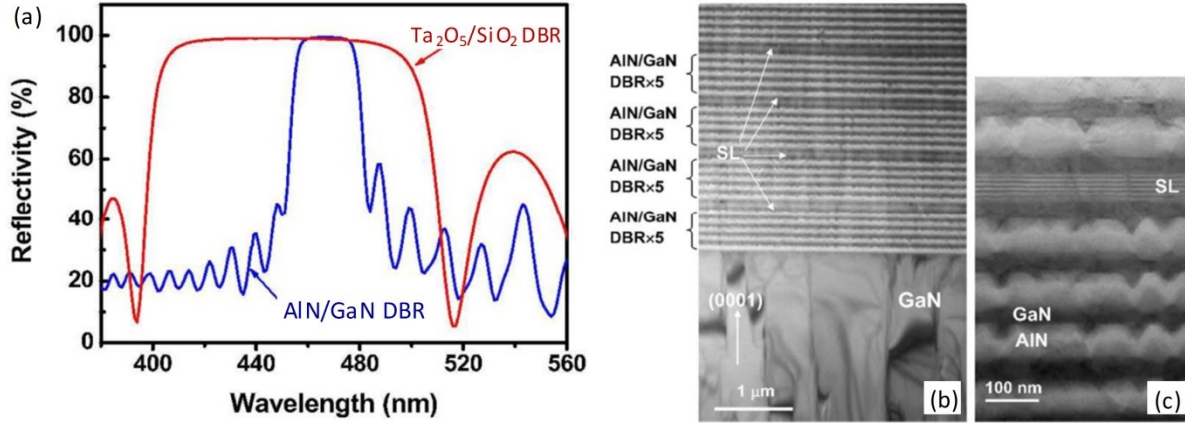
Figure 44 (a) Reflectivity spectrum for a Ta_2O_5/SiO_2 dielectric p-DBR and AlN/GaN epitaxial n-DBR used on a 450 nm c-plane VCSEL. (b), (c) cross-sectional TEM images showing the AlN/GaN DBR stack. The superlattice (SL) structure is used to prevent cracking caused by the large lattice mismatch between the AlN and GaN layers. The DBR is seen to have a significant degree of interface roughness, which can increase scattering loss in a VCSEL. The interface roughness is caused by V-defects, commonly observed in c-plane growth.[132]

AlInN/GaN-based, blue emitting, hybrid DBR, c-plane VCSEL has been demonstrated, though the threshold current density was very high (~130 kA/cm^2).[166]

In both cases, one of the disadvantages of an epitaxial DBR is the small index contrast between the ¼-wave layers. This small index contrast not only requires the growth of many periods in order to achieve a high reflectivity, but it also results in a narrow stop-band for the DBR, which cannot be overcome by simply growing more periods. The stop-band of a DBR is the spectral width (i.e. the range of wavelengths) over which the DBR has a high mirror reflectance. This can be seen in Figure 44(a), where reflectance spectra from an AlN/GaN epitaxial n-DBR and Ta_2O_5/SiO_2 dielectric p-DBR are shown. The DBRs were designed for a blue emitting (~450 nm) c-plane VCSEL.[132] The epitaxial DBR has a stop-band of ~70 nm, while the dielectric DBR has a stop band of ~35 nm, due to the larger index contrast between the ¼-wave layers (Figure 50). As will be seen more clearly in the simulations to follow, the DBR always has its peak reflectance at the resonance wavelength, however a wider stop-band implies a smaller deviation from this peak reflectance for incident light that has a slightly longer or shorter wavelength than the DBRs resonance

wavelength. Therefore a wide stop-band can be advantageous for VCSELs because it gives a larger room for error when the VCSELs cavity (Fabry-Perot) resonance wavelength is unintentionally detuned (due to experimental variation) from the DBRs resonance wavelength.

Besides the large index contrast and wide stop-band of dielectric DBRs, they are also advantageous due to the relatively simply nature of their fabrication. Dielectric DBRs can be deposited using conventional sputtering techniques, which are much less complicated and less expensive than MOCVD- or MBE-based epitaxial growth techniques. Furthermore, because sputtered films tend to deposit in amorphous or polycrystalline phases, there is not a concern with cracking. Despite the comparable simplicity, dielectric DBR depositions do require a very high degree of control and reproducibility over very long deposition times (~6-12 hrs.), which can be an issue for many standard sputtering systems. Thus, ion-beam deposition (IBD), which is typically used for depositing high-quality optical films with a high degree of surface uniformity and repeatability, is the best deposition technique for fabricating dielectric DBRs. Unfortunately, these tools are still considerably more expensive than standard magnetron (DC & RF) sputtering systems, which are more commonly used in academic settings. This is a significant limitation for academic researchers generally, since standard magnetron sputtering systems can often yield films with a non-uniform thickness across the substrate, and also have less stable deposition rates than IBD systems. Furthermore, magnetron sputter systems tend to have more intense plasma energies interacting with the substrate, which can cause p-GaN plasma damage through thin ITO intracavity contacts. Fortunately, UCSB's cleanroom (the Nanofab) has an IBD system (Veeco Nexus IBD), which is used to fabricate all dielectric DBRs reported here.

The final parameter to consider in choosing a DBR is the thermal conductivity of each of the layers. Table 3 shows the thermal conductivity for the primary layers of interest in analyzing the epitaxial and dielectric DBR thermal performance. It is of note that phonon scattering reduces the thermal conductivity of ternary compounds, relative to binary compounds,[6,89] however our analysis is aimed at a simple relative comparison, rather than a highly precise validation, so we do not need to be concerned with these specific variations. As can be seen from Table 3, the dielectric layers have a significantly (~3 orders of magnitude) lower thermal conductivity than the III-nitride layers. Even without analytical simulations, one can easily imagine that heat will more effectively transfer away from the active region through an epitaxial III-nitride DBR, compared to a dielectric DBR. In fact, as will be seen in Section 1.4.4.3, dual dielectric DBR VCSELs essentially rely on lateral dissipation of heat around the dielectric DBRs. This makes it much more difficult to achieve CW operation with dual dielectric DBR VCSELs. Yet, as will be demonstrated in simulations, with proper cavity design, the thermal performance of flip-chip dual dielectric DBR VCSELs can be engineered to be on-par with hybrid DBR VCSELs.

In summary, the dual dielectric DBR design and hybrid DBR design both have unique advantages and disadvantages. In general though, the dual dielectric DBR design can more easily yield high reflectivity DBRs and increase the tolerance for error when a

Table 3 Typical thermal conductivity values for relevant materials used in epitaxial and dielectric DBR designs. [6,411–413] Thermal conductivity values for other common III-V compounds can be found in Table 1.

Material	Thermal Conductivity (W/cm-K)
GaN	1.3
AlN	2.85
ITO	0.05
Ta_2O_5	0.0045
SiO_2	0.007
Au	3.17

VCSELs cavity resonance wavelength is unintentionally detuned from the DBRs resonance wavelength. Furthermore, because we can achieve similar thermal performance in properly optimized dual dielectric DBR designs, compared to hybrid DBR designs, the dual dielectric DBR VCSEL is likely the most promising VCSEL design for high yield manufacturing.

1.4.4.2. DBR Reflectance Spectra

To achieve the desired threshold condition for a VCSEL, one must have an understanding of the mirror reflectance spectra for the DBRs. For the non-emitting side of the device (i.e. the p-side for a flip-chip VCSEL), the DBR must have as close to 100% reflectance as possible. On the emitting side of the device (i.e. the n-side for a flip-chip VCSEL), the DBR reflectance depends on the desired mirror loss for the particular design, which is based on the desired differential efficiency and threshold current density (Section 1.4.2). Additionally, because the mirror loss also depends on the cavity length, VCSELs with different cavity lengths will have different requirements for the DBR reflectance on the emitting side of the device. From now on, unless otherwise stated, our discussion will be focused on flip-chip dual dielectric DBR devices, implying that the n-DBR is on the emitting side and the p-DBR is on the non-emitting side. To change the DBR reflectance, one varies the number of mirror periods. However, it should be noted that there a many experimentally related effects that can result in the true reflectance being different from the designed reflectance. Some of the more obvious causes of error are: deviation in the refractive index and ¼-wave thickness of the materials from the simulated values, as well as variations in the deposition rates as the DBR stacks are deposited. Overall, it is difficult to determine the degree to which these effects change the reflectance because it is difficult to
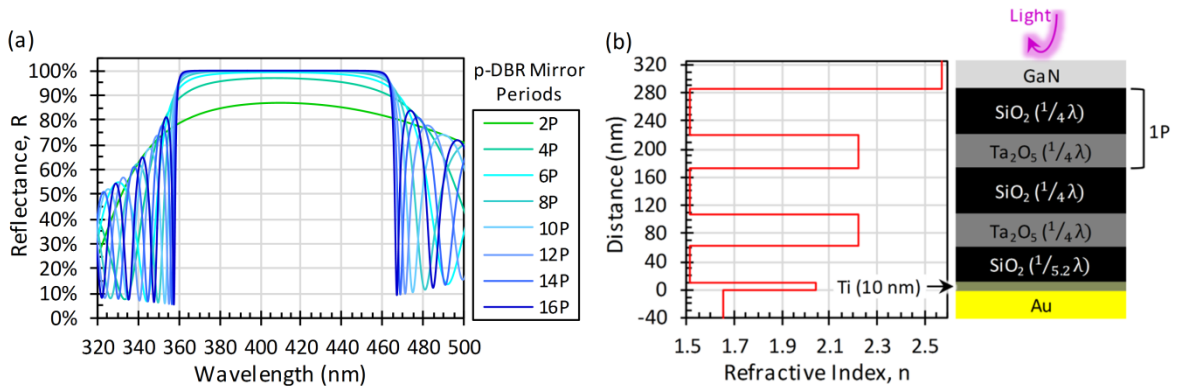
Figure 45 TMM simulations of a TJ VCSEL p-DBR. (a) shows the reflectance spectra as a function of number of mirror periods (P). (b) shows the refractive index profile and a schematic of the modeled structure. The simulation does not take into account index dispersion. It uses the 405 nm refractive index values fromFigure 42.

accurately measure a reflectance of > 99%, as most reflectance measurements require a reference mirror with a well-defined reflectance in order to calibrate the spectrometer being used. Getting a reference mirror that has a precisely quantified reflectance down to 0.01% is not easy. Overall, it is probably not worth anyone's time trying to make such a precise measurement, when you can just process a VCSEL and see how it performs.

As the p-DBR should always be design to have as high of a mirror reflectance as possible for a flip-chip VCSEL, we will focus on simulating this DBR. The simulations reported here use the TMM (Section 1.4.3), with the 405 nm wavelength refractive index values from Figure 42. The DBR is designed for a 405 nm resonance. Index dispersion is not taken into account. The absorption coefficient (i.e. complex component of the refractive index (the extinction coefficient)) is assumed to be 0. This is a good assumption because the laser equations in Section 1.4.2 require us to account for any material absorption in the internal loss term, not the mirror loss term. Figure 45(a) shows the p-DBR mirror reflectance spectra as a function of the number of SiO_2/Ta_2O_5 mirror periods (P). Figure 45(b) shows the refractive index profile and a schematic of the simulated structure. The Ti/Au layers are what are used as conformal coatings to the DBR on the flip-chip structure, where the Au is
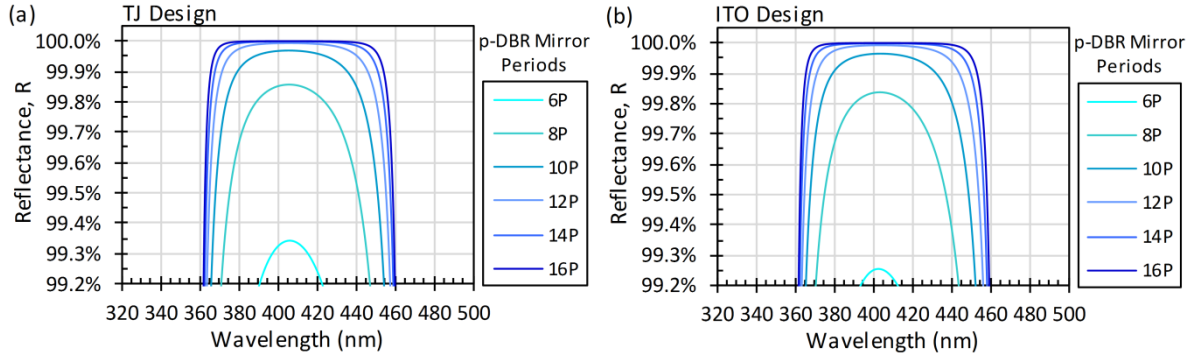
Figure 46 (a) Zoomed-in version of Figure 45(a), showing the number of mirror periods that yield > 99% reflectance for a TJ VCSEL p-DBR. Above 12 periods, the peak reflectance is not significantly changed, however using 16 periods in actual devices allows one to over compensate for any reduced interface reflection coming from experimental variation and error. (b) shows similar simulations for an ITO VCSEL p-DBR, where we now have included an ¼-wave ITO layer and $1/8^{th}$-wave Ta_2O_5 spacer layer in between the GaN and SiO_2 layers seen in Figure 45(b). Overall, the reflectance spectra in the TJ VCSEL p-DBR and the ITO VCSEL p-DBR are very similar.

present in order to achieve the Au-Au compression bond used in our flip-chip device. The $1/_{5.2}$-wave SiO_2 layer serves as a phase matching layer. For many mirror periods, only a very small fraction of the lights electric field reaches this layer, making it unimportant, but for DBRs with < 10 mirror periods, it helps increase the reflectance. The final layer of note in Figure 45(b) is the GaN cap layer. Here, we show the light is incident from the GaN side of the cavity, which is how it would be incident in the VCSEL itself. Because we do not include the ITO layer in this model, this design corresponds to a TJ VCSEL. Figure 46(b) shows simulation results for an ITO VCSEL p-DBR, which will be discussed more later. Viewing Figure 45(a), we can see the high index contrast between the dielectric layers yields a fairly high reflectance with only 2 mirror periods. With increasing mirror periods, the peak reflectance increases, along with the average reflectance over the stop-band. Above 6 periods, the reflectance is > 99%. Figure 46(a) shows the zoomed-in version of the reflectance spectra from Figure 45(a). Here, we can more clearly see the small, but significant (for VCSELs) changes in the peak reflectance and average reflectance across the stop-band. Very little change in the peak reflectance is observed above 12P, however we

chose to use a 16P p-DBR design to attempt to compensate for any potential decrease in the interface reflectance coming from experimental variation. Figure 46(b) shows the reflectance spectra for an ITO VCSEL p-DBR, where we now have included a ¼-wave ITO layer and $1/8^{th}$-wave Ta_2O_5 spacer layer in between the GaN and SiO_2 layers seen in Figure 45(b). Again, it is best to assume the absorption coefficient is zero here, in order to avoid the convolution of the mirror loss and internal loss contributions to the differential efficiency and modal gain (Section 1.4.2). Overall, the reflectance spectra for the two different designs are quite similar, with the ITO VCSEL p-DBR having a slightly lower mirror reflectance for a given number of mirror periods.

To conclude, the peak reflectance does not change significantly above 12 periods, however this assumes there are no experimental variations present. To compensate for any experimental deviations from the ideal case, it is recommended to use 16P p-DBRs.

1.4.4.3. DBR Design Thermal Analysis

With the basic structure for the p-DBR determined, we can now consider the thermal implications of using a 16P SiO_2/Ta_2O_5 p-DBR. Because we are mostly concerned with a more direct comparison of the thermal performance of dual dielectric DBR VCSELs relative to hybrid DBR VCSELs, we will not investigate the effects of cavity length in this section. The effect of cavity length on thermal performance is discussed in Section 1.4.5.2. Here, we will focus on 7λ cavities (~1.2 μm), as most III-nitride VCSELs reported by academic groups have used cavity lengths equal to or close to this value.[10–15,132,166] It is notable that industry groups have generally used thicker (~23λ) cavities, which will be discussed in detail in Section 1.4.5.[171–175] To model the thermal performance of the devices, we use
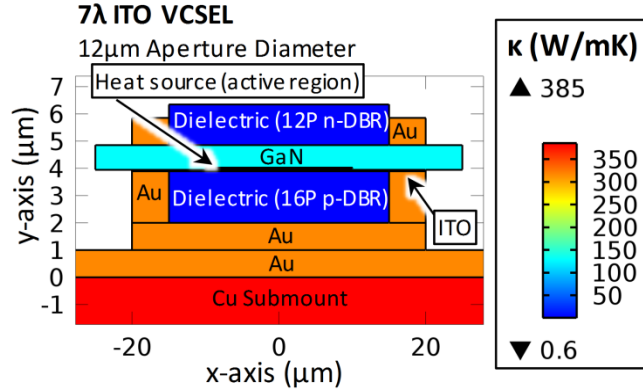
Figure 47 Schematic of the simplified 7λ dual dielectric DBR ITO VCSEL structure used to model the thermal performance using COMSOL. The 2D-axis symmetric geometry is used, thus the device has a cylinder-like geometry, with the central longitudinal axis at the 0 point of the x-axis. The layers are colored according to their thermal conductivity, shown in the key to the right of the plot. The device has a 12 µm aperture diameter. The ¼-wave ITO layer is essentially too thin (~50 nm) to resolve in the picture, however the position of it is identified.

COMSOLs 2D axis-symmetric module, with the "Heat transfer in solids" physics package. A schematic for a representative modeled dual dielectric DBR flip-chip ITO VCSEL can be seen in Figure 47. Here, we see much of the fine detail of the structure is simplified. Specifically, the Ti/Au coatings have been simplified to be just Au, the epitaxial layers are simplified to be just GaN, and the SiO_2/Ta_2O_5 dielectric DBRs are simplified to be a uniform dielectric medium. Each layer is colored according to its thermal conductivity, shown in the key on the right and stated in Table 3. For the DBR layers, the lateral and vertical thermal conductivities can be defined by the equations

$$(26) \qquad k_{eff,L} = \frac{d_1 k_1 + d_2 k_2}{d_1 + d_2}$$

$$k_{eff,V} = \frac{d_1 + d_2}{d_1/k_1 + d_2/k_2},$$

where d_1 and k_1 are the thickness and thermal conductivity of layer 1 (SiO_2), and d_2 and k_2 are the thickness and thermal conductivity of layer 2 (Ta_2O_5).[176] For the SiO_2/Ta_2O_5 dielectric DBR, with a 405 nm resonance wavelength (i.e. ¼-wave SiO_2 is ~66.79 nm, ¼-wave Ta_2O_5 is ~45.61 nm), the effective lateral and vertical thermal conductivities are

~0.006 W/cm-K and ~0.0057 W/cm-K, respectively. Because these are essentially the same value, we just assume the thermal conductivity in the DBR is isotropic, with a value of ~0.006 W/cm-K, which simplifies the model. It should also be noted that we assume all input power generates heat in the active region, which is a rather pessimistic assumption, primarily because power will also be dissipated in the form of stimulated and spontaneous emission. Thus these models can be thought of as worst-case scenarios for the amount of heat generated for a given input power to a device. For the steady-state analysis, all layers are set to an initial temperature of 23 °C. The boundary conditions are then defined with the areas exposed to air following the surface-to-ambient radiation equations (defined in COMSOL), and the bottom and edges of the Cu submount layer having a constant temperature of 23 °C. The active region is the set as the input power point (i.e. heat source), and the simulation is run until steady-state is reached. To visualize the thermal performance of the device, we focus on the temperature profile (i.e. the temperature increase, ΔT, relative to the initial temperature) and total flux profile. The flux profile gives insight to the path by which thermal dissipation occurs.

Figure 48 shows the temperature increase profile (a_1, b_1, c_1) and total thermal flux vectors overlain on the thermal conductivity profile (a_2, b_2, c_2) for a dual dielectric DBR 7λ ITO VCSEL ($a_{1,2}$), a dual dielectric DBR 7λ TJ VCSEL ($b_{1,2}$), and a representative hybrid DBR 7λ VCSEL ($c_{1,2}$). All devices have 12 µm aperture diameters. The input power for the profiles shown corresponds to 0.25 W. To model the TJ VCSEL the ¼-wave ITO layer is simply replaced by a 200 nm GaN layer. The hybrid DBR VCSEL is approximated by replacing the p-DBR, Cu submount, and Au on the p-side of the device with GaN. Naturally, a real hybrid DBR design is slightly different, but the geometry shown here allows us to
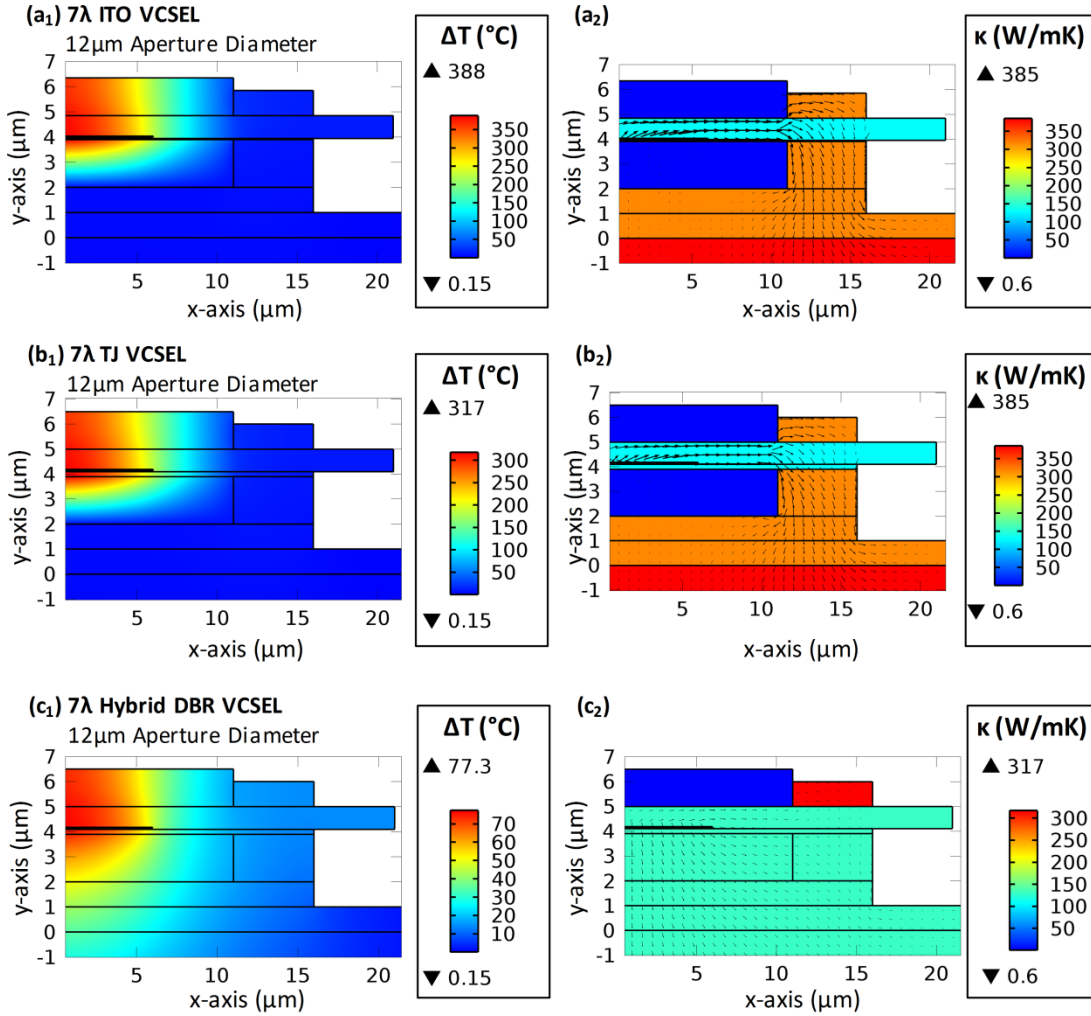
Figure 48 (a_1, b_1, c_1) temperature change, ΔT, profiles and (a_2, b_2, c_2) thermal flux vectors overlain on thermal conductivity profiles. (a) shows a 7λ ITO VCSEL, (b) shows a 7λ TJ VCSEL (200 nm TJ thickness), and (c) shows a comparative 7λ hybrid DBR VCSEL, where the Au, Cu submount, and DBR on the bottom of the device have been replaced with GaN layers. The models were performed using COMSOL and assume all input power goes to heat generation. The input power for the profiles shown here is 0.25W. A schematic with the label layers for the ITO VCSEL can be seen in Figure 47.

more clearly see the effect of the dielectric p-DBR on the device performance. Comparing

temperature rise in the ITO VCSEL (a_1) to the TJ VCSEL (b_1), we can see that replacing the

thin, poorly thermally conductive ITO layer, with the GaN TJ layer reduces to temperature

increase from 388 °C to 317 °C. However, both of these dual dielectric devices still have

significantly larger temperature increases compared to the hybrid DBR VCSEL (c_1), which

shows a peak temperature increase of 77.3 °C for 0.25 W input power. The reason for this

can be understood by observing the total thermal flux vectors overlain on the thermal conductivity profiles (a_2, b_2, c_2). In these diagrams, the size of the black arrow indicates the strength of the flux. It is also of note that the strength of the flux is shown on a log scale. Because we can only slightly resolve the flux arrows in the p-DBR layers on this log scale, we can easily realize that they would not even be seen on a linear scale, highlighting further the significant thermal dissipation impedance introduced by using a dielectric p-DBR. Observing the dual dielectric DBR TJ and ITO VCSEL flux profiles (a_2, b_2), we can see that the heat must spread laterally around the p-DBR before dissipating into the submount. In contrast, the in the hybrid DBR VCSEL, the epitaxial p-DBR allows efficient vertical dissipation of heat, resulting in a significantly lower temperature rise. Besides observing the temperature increase profiles and thermal flux profiles for specific input powers, we can also analyze the temperature rise as a function of input power. Figure 49(a) shows the temperature change, ΔT, vs. input power profiles for the 7λ ITO VCSEL, TJ VCSEL, and equivalent hybrid DBR VCSEL, all with 12 µm aperture diameters. As was seen in Figure 48, the dual dielectric DBR TJ and ITO VCSELs have significantly higher temperatures for a given input power, compared to the equivalent hybrid DBR VCSEL, due to the thermally insulating dielectric p-DBR layers. Figure 49(b) shows how the temperature change vs. input power slope changes with aperture diameter. Naturally, larger aperture diameters imply a lower input power density for a given input power, thus they have a smaller temperature change. A similar trend of the increase in the slope of the temperature change vs. input power for different aperture diameters, is followed for the differential resistance vs. aperture diameter properties of VCSELs, as larger aperture diameter devices have lower contact resistances due to the larger intracavity contact area. Overall the aperture diameter
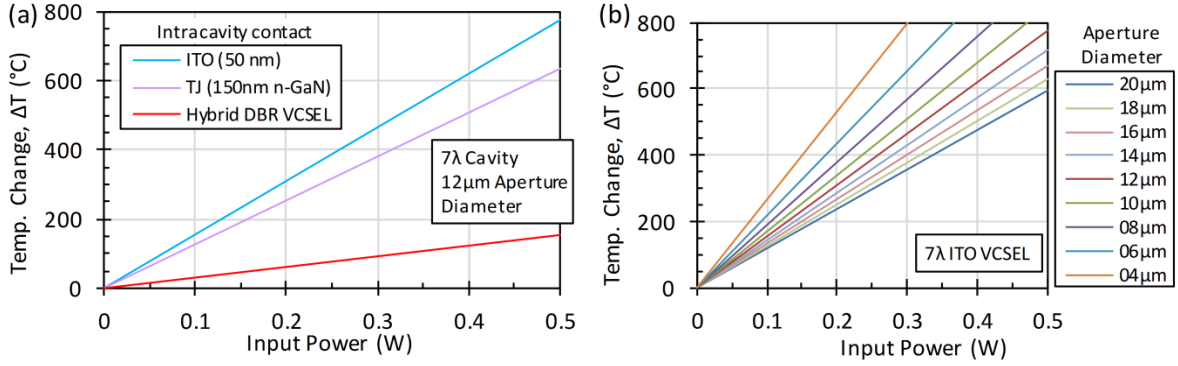
Figure 49 (a) temperature change, ΔT, vs. input power for the 7λ ITO VCSEL, TJ VCSEL, and equivalent hybrid DBR VCSELs from Figure 48. The dual dielectric DBR TJ VCSEL and ITO VCSEL both have significant thermal performance limitations due to the thermally insulating nature of the dielectric p-DBR layer, requiring the lateral dissipation of heat. (b) the effect of aperture diameter on temperature change vs. input power for the ITO VCSEL.

dependence of VCSEL performance is complicated due to the variation in lateral confinement and current spreading with different aperture diameters, thus one should not simply assume that a larger aperture diameter VCSEL will have better thermal performance. Figure 49(b) is of most use when one has actual experimental data with threshold voltage and current vs. aperture diameter, which can then allow one to compare the relative temperature rise expected.

Overall, these models highlight the fundamental reason why flip-chip dual dielectric DBR VCSELs fabricated by our group have yet to achieve CW operation. Understanding that we are fundamentally limited to the lateral dissipation of heat around the p-DBR, we can realize two design methods for improving thermal dissipation in the dual dielectric DBR flip-chip VCSEL: (1) increase the cavity thickness to reduce the lateral thermal spreading resistance, and (2) decease the distance between the aperture edge and the Au coating on the p-DBR (i.e. improve the p-DBR to aperture alignment tolerance). These effects will be considered in Section 1.4.5.2.

1.4.5. The Longitudinal Mode and Cavity Thickness Effects

1.4.5.1. Optical Effects

A laser is characterized as multi-mode or single mode. Within these characterizations, a laser can either be multi-lateral mode and single longitudinal mode, single lateral mode and multi-longitudinal mode, or single lateral and single longitudinal mode in nature. The last case is the only truly single mode device. The longitudinal mode, and axial mode more generally (i.e. for EELDs), behavior is defined by the overlap between the gain spectrum and the cavity resonance (Fabry-Perot) modes. Fabry-Perot modes exist in any arbitrary cavity, whether there is a gain medium or not. The Fabry-Perot (cavity) mode spacing is defined by the equation

$$(27) \quad d\lambda = \frac{\lambda^2}{2\, n_{g,eff} L_{eff}},$$

where λ is the lasing wavelength, $n_{g,eff}$ is the effective group index, and L_{eff} is the effective cavity length.[3] The refractive index, n, is a ratio that defines the relative speed of a light in a medium to the speed of light in vacuum ($n = 1$) (higher index, lower speed). In a similar manner, the group index, n_g, defines the group velocity of an envelope of a pulse of light in a medium, relative to the velocity of the envelope in vacuum. Mathematically, the group index is defined as

$$(28) \quad n_g = n - \lambda \frac{\partial n}{\partial \lambda}.$$

Because the VCSEL is composed of many different layers, each with different refractive index dispersion profiles (defining $\partial n / \partial \lambda$), and with different relative interactions with the

84
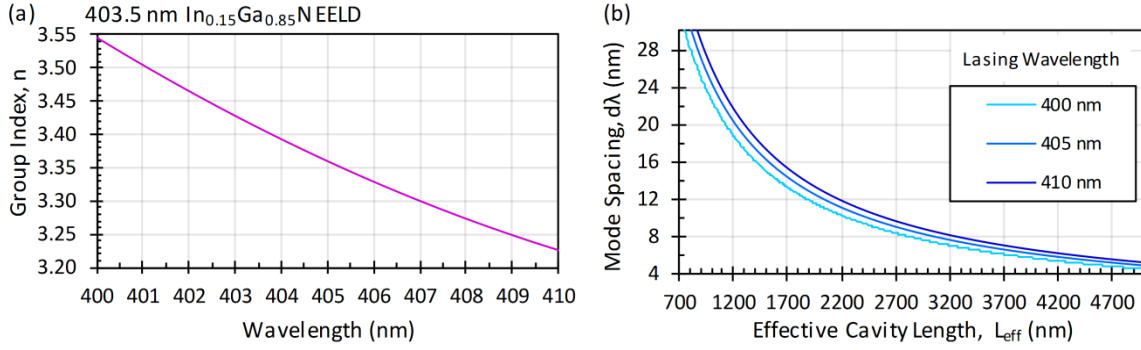
Figure 50 (a) Group index dispersion measured on a 403.5 nm InGaN EELD.[381] Group index values for various III-nitride VCSEL layers are also given in Refs. 199,365. (b) Calculated mode spacing vs. effective cavity length for different violet emission wavelengths. The calculation was performed using Eqn. (27). 7λ, 13λ, and 23λ cavities have effective cavity lengths of ~1.2 μm, ~2.1 μm, and ~3.7 μm, respectively.

mode (defined by the modal intensity, E^2, profile in that layer), it is more precise to consider the effective group index, which is defined by the effective refractive (cavity) index, n_{eff}, and the effective index dispersion. Thus an ideal determination of the group effective index would essentially weight the index dispersion for each layer relative to its interaction with the mode. Building a model to do this can be a bit tedious for rapid device analysis, so for practical experimental purposes, it is better to just use reported group index values from the literature. Figure 50(a) shows experimentally measured group index dispersion data for a 403.5 nm emitting $In_{0.15}Ga_{0.85}N$ EELD. This data can be considered a good first-order approximation for the group index dispersion in a violet VCSEL. Using Figure 50(a) and Eqn. (27), we plot the mode spacing vs. effective cavity length for a laser with a central emission wavelength of 400 nm, 405 nm, and 410 nm (Figure 50(b)). The cavity length range shown is a typical range for III-nitride VCSELs, with the academic groups primarily fabricating ≤7λ (L_{eff} ≈ 1200 nm) cavities with mode spacing's of ~20 nm,[8,10–15,131–133,166,177,178] and the industry groups typically fabricating ~23λ (L_{eff} ≈ 3700 nm) cavities with a mode spacing of ~7 nm.[171–175,179,180] It is of note that this difference in cavity length is likely one of the primary reason why dual dielectric DBR VCSELs from academic groups

have generally been lower power than those fabricated by industry groups, however this is primarily related to thermal and current spreading improvements resulting from thicker cavities (Section 1.4.5.2). To determine if a given cavity length will yield single longitudinal mode emission, one must consider the overlap of the gain spectrum with the mode spacing. In a passive cavity (i.e. one without a light-emitting region), one can most easily observe the mode Fabry-Perot mode spacing (experimentally) by viewing the reflectance spectrum of the cavity, where sharp drops in the reflectance will be observed at the resonance wavelengths, though with VCSEL quality DBRs, the line-widths of the resonance fringe is so small that is it difficult to resolve without an extremely high resolution spectrometer. For our simple simulation based analyses, the reflectance spectrum and can be easily simulated using the TMM (Section 1.4.3). The index dispersion data for various layers of interest for the dual-dielectric DBR violet (405 nm) VCSELs considered here are shown in Figure 42. The specific details of the cavities modeled in the following discussion are not critical at the moment, as our primary object is first to understand how the gain spectrum interacts with the Fabry-Perot resonance spectrum.

Figure 51 shows the (TMM) simulated cavity reflectance spectrum, as seen from the top-side (n-side) of a flip-chip VCSEL, overlain with the (SiLENSe) simulated gain spectrum vs. current density, and the (TMM) simulated threshold material gain values for 7λ TJ and ITO VCSELs (a), and 23λ TJ and ITO VCSELs (b). The TMM simulations do not account for index dispersion, making the resonance spacing larger than the more accurate values shown in Figure 50, but we are more interested in a qualitative analysis here anyways. For each device, the active region is composed of 7QWs with 3 nm InGaN active (A) QW widths, 1 nm GaN barriers (B), and a 5 nm EBL (7QW, A3 nm, B1nm, EBL 5 nm

86
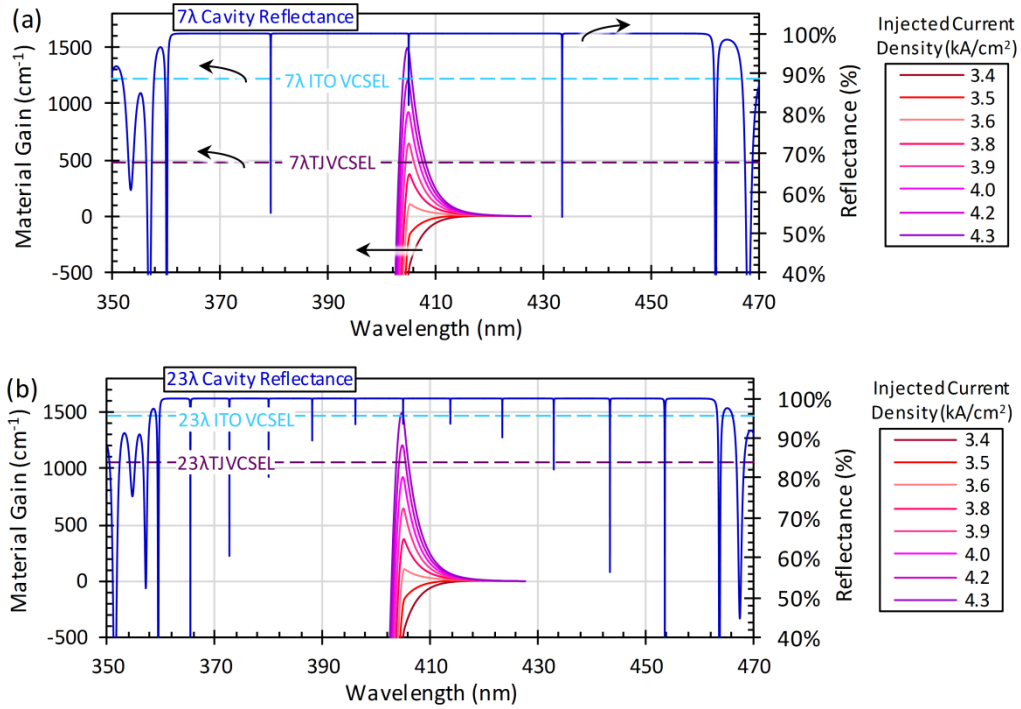
Figure 51 Top-down (TMM) simulated reflectance spectra overlain with (SiLENSe) simulated material gain vs. current density and (TMM) simulated threshold material gain for 7λ TJ and ITO VCSELs (a), and 23λ TJ and ITO VCSELs (b). For each device, the active region is composed of 7QWs with 3 nm InGaN active (A) QW widths, 1 nm GaN barriers (B), and a 5 nm EBL (7QW, A3 nm, B1 nm, EBL 5 nm design). The TMM simulations do not account for index dispersion, making the resonance mode spacing larger than one would observe in actual devices. Figure 50 should be used for a more precise prediction of cavity resonance mode spacing vs. cavity length.

design). As was mentioned previously (Section 1.4.2), one should not compare the threshold

material gain for VCSELs with different cavity lengths and different numbers of QWs, as

the confinement factors will be significantly different, however comparing the threshold

material gain for a TJ vs. ITO VCSEL design with the same cavity length is appropriate

because there is no significant variation in the confinement factor. Viewing the reflectance

spectrum in Figure 51(a), we see the Fabry-Perot (cavity) resonance mode spacing is very

large compared to the gain spectrum, thus lasing will only occur at the fundamental

resonance wavelength, 405 nm, where the peak material gain wavelength is aligned to the

405 nm cavity resonance wavelength. Moving to the 23λ case, we see the mode spacing

decreases, but there is still only a very small material gain value at the cavity resonance

wavelengths shorter than and longer than 405 nm. Therefore both the 7λ and 23λ devices would be expected to have single longitudinal mode emission. It should be noted that in the 23λ case, the smaller mode spacing will result in significantly more of the spontaneous emission spectra, with a much wider spectral width than the gain spectrum, overlapping with cavity resonance wavelengths, thus relatively intense emission will be observed at the resonance wavelengths besides 405 nm, however this will only be spontaneous emission. If we imagine increasing the cavity thickness well beyond 23λ (~3.7μm) to 100s or 1,000s of μm, it is easy to recognize that the longitudinal (axial) mode spacing would be very small and many cavity resonance wavelengths would overlap with the gain spectrum. This is indeed what occurs in EELDs, which is why standard EELDs are multi-longitudinal mode devices. To achieve single longitudinal mode lasing in an EELD, one must use a distributed feedback (DFB) laser design, which has not been very heavily investigated for III-nitride EELDs. This wavelength selectivity is part of the reason why VCSELs are so desirable for many highly sensitive systems. For many other applications though, the beam shape is more important than the wavelength selectivity. In VCSELs the beam profile is defined by the lateral confinement, whereas in edge-emitters, it is defined by the transverse confinement. Both devices can be fabricated to achieve single mode emission beam profiles. Moving back to Figure 51 and observing the threshold material gain values for the ITO vs. TJ VCSEL designs in each of the cavity lengths, we can also note the significant decrease in threshold material gain required if we use a TJ VCSEL design. In the longer cavity, the difference in threshold material gain between the ITO and TJ design is smaller because the ¼-wave ITO layer occupies a smaller proportion of the total cavity, resulting in it contributing to a smaller fraction of the total internal loss.

Besides viewing the cavity resonance overlap with the gain spectrum, it is also important to consider the distribution of the longitudinal mode intensity (E^2-field) in the cavity for different wavelengths. Of course, the fundamental longitudinal mode (405 nm) is of the most interest, so we will start by considering this first. Figure 52(a) shows the (TMM) simulated 405 nm longitudinal mode intensity and refractive index profiles for a 23λ TJ VCSEL. The 16P p-DBR (back-side) and 10P n-DBR (top-side) are labeled, along with the other relevant layers in the device. Looking at the 7QW active region, we can see a peak of the standing wave is aligned to the center of the active region, leading to a strong enhancement factor. Evidently the width of the modal peaks is fairly narrow, thus one should generally use very narrow barriers in VCSELs in order to increase the overlap of the intense portions of the mode with the active QWs, thereby maximizing the enhancement factor.

Viewing the reflectance spectrum for Figure 51(b), we can see that we would also expect a mode to be confined to the cavity for the resonance wavelengths of 396 nm and 414 nm, as well as the fundamental cavity resonance wavelength of 405 nm. Figure 52(b) shows the mode profiles for these three wavelengths, overlain on the refractive index profile in the center of the 23λ TJ VCSEL. Here, we see that even though the 396 nm and 414 nm modes are confined to the cavity, they are not properly aligned to the active region of the cavity, thus they would have a very poor confinement factor. This implies that these modes would have virtually no interaction with the QWs, meaning it would be impossible to achieve stimulated emission at these two modes, even if there was a significant overlap with the material gain spectrum at these wavelengths. Though we do not explicitly show it here, it is also important to realize that the spacing between the peaks and nulls of the standing wave
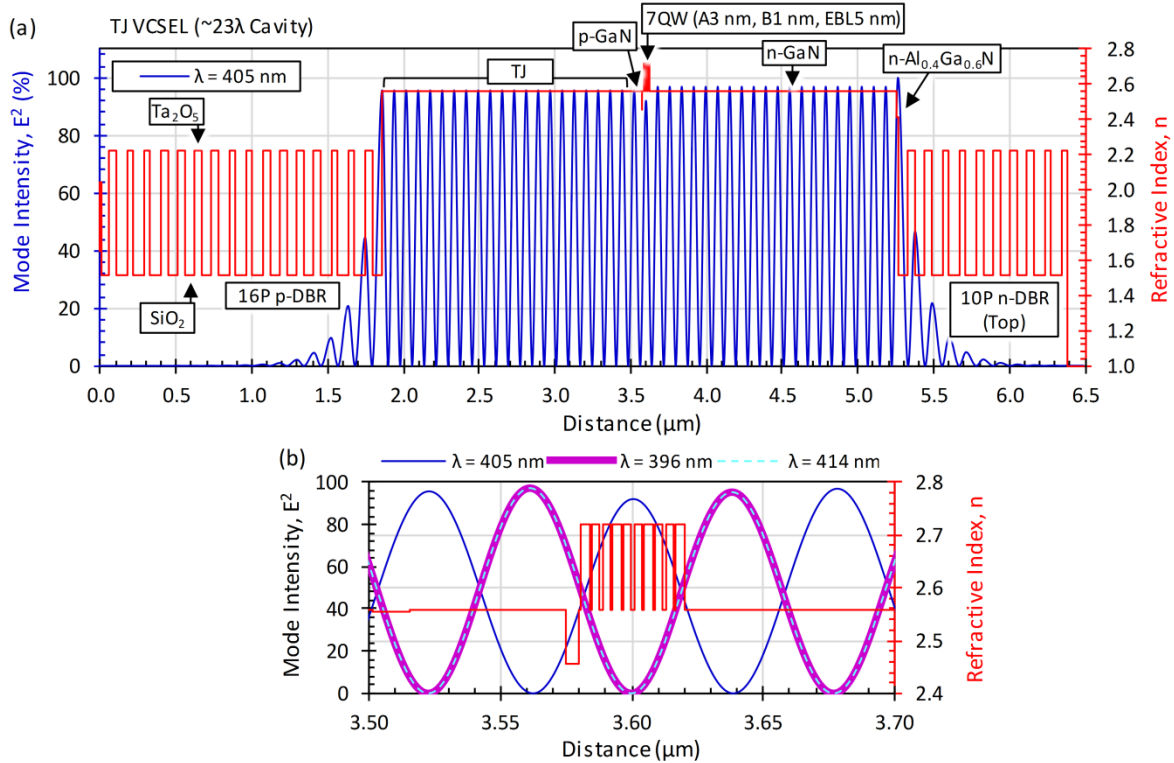
Figure 52 (a) (TMM) simulated 405 nm longitudinal mode intensity and refractive index profile for a 23λ TJ VCSEL. (b) Refractive index profile and mode profiles for the 405 nm, 396 nm, and 414 nm cavity resonance wavelengths. The modes for the different resonance wavelengths are confined in the cavity, however, only the fundamental mode is properly aligned to the active region of the device.

for any particular resonance wavelength is inversely proportional to the cavity length. This implies that for very long cavities, such as those used for EELDs, one will be unable to resolve the individual peaks and nulls of the field, and so you will essentially see an envelope function of the field. This is why EELDs do not have enhancement factors, and it is also why they lase at every resonance wavelength that overlaps with a significant portion of the gain spectrum.

In summary, for VCSELs, the multi-longitudinal mode behavior is defined by both the cavity resonance mode spacing and the resulting overlap between the cavity resonance wavelengths and the gain spectrum, as well as the particular enhancement factor for the mode of a particular cavity resonance wavelength. Indeed, for the 23λ TJ VCSEL case we examined, the two resonance wavelengths nearest to the fundamental resonance wavelength

(405 nm) had modes with essentially zero overlap with the active region, which would result in an enhancement factor of approximately zero.

1.4.5.2. Thermal Effects

As we saw in the previous section, there is a large range of cavity thicknesses that will yield single longitudinal mode emission, so what is the motivation for using a thicker cavity. Considering the fundamental laser equations (Section 1.4.3), specifically the mirror loss, we can imagine that having a longer cavity would allow us to reduce the top-side n-DBR mirror reflectance and maintain a low mirror loss, but achieve a higher differential efficiency (by increasing the fraction of light emitted out the top-side of the device). However the more notable improvements from using a thicker cavity are from reduced thermal and current spreading resistance. Here, we will focus on thermal improvements, as we have not carried out complete simulations on the current spreading vs. cavity thickness effects, however it is easy to recognize that having a thicker cavity would improve the current spreading uniformity across an aperture, particularly for large aperture diameter devices, which are favorable for high power applications. Some implications of the poor current spreading in 7λ ITO VCSELs are discussed in Section 4.2.

To analyze the relative effect of cavity length on thermal performance, we use COMSOL models similar to those described in Section 1.4.4.3. Here, we will focus on TJ VCSEL designs, which are more promising for future violet emitting dual dielectric VCSELs. Figure 53 shows the temperature change profiles (a_1, b_1, c_1) and thermal flux vectors overlain on the thermal conductivity profiles (a_2, b_2, c_2) for a 7λ (a), 13λ (b), and 23λ (c) TJ VCSEL, all with 0.25 W input powers and 12 μm aperture diameters. Moving from
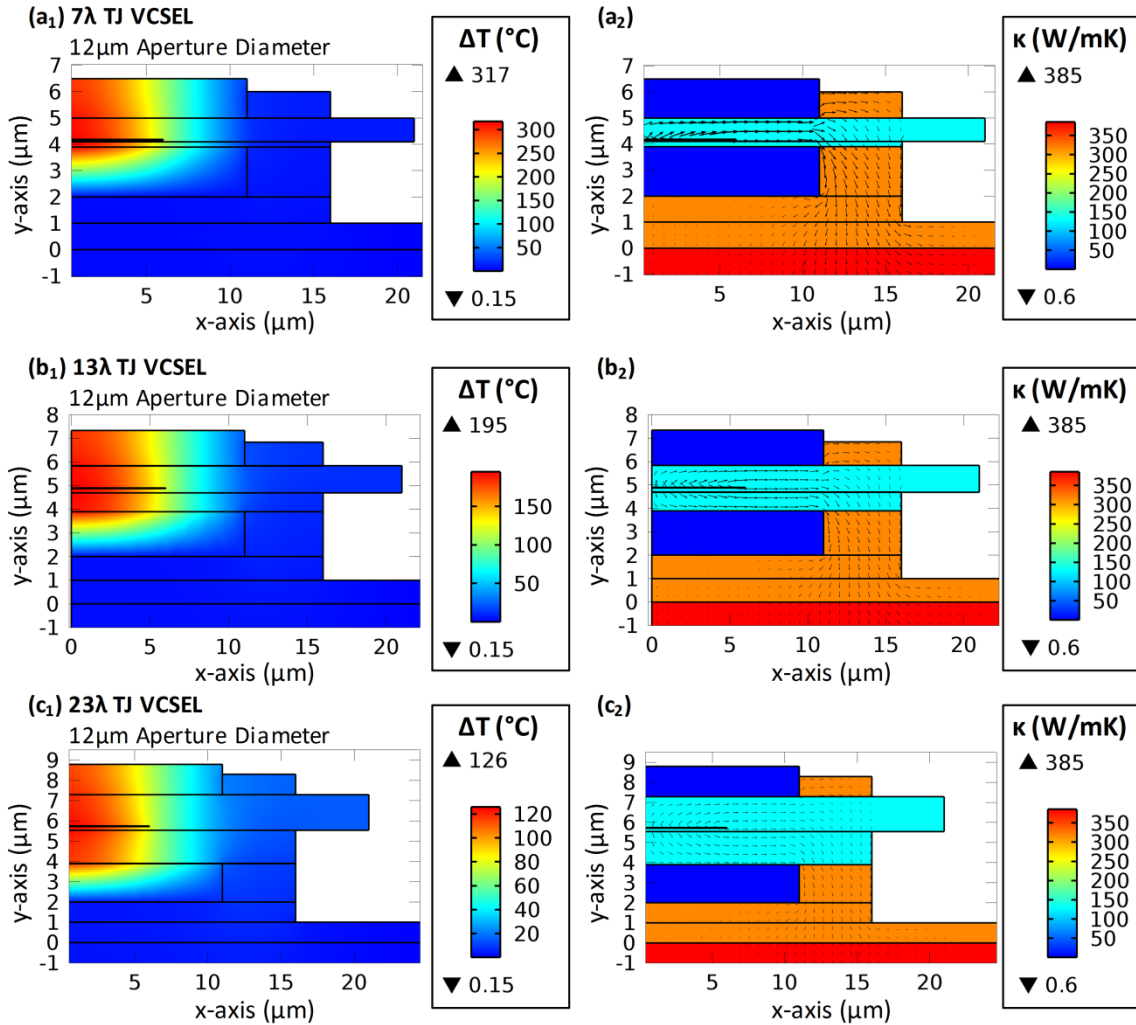
Figure 53 COMSOL simulations of TJ VCSELs with different cavity lengths. The input power for all the structures is 0.25 W. (a_1), (b_1), and (c_1) show the temperature change, ΔT, profiles, while (a_2), (b_2), (c_2) show the total thermal flux vectors overlain on the thermal conductivity, κ, profiles, for the 7λ, 13λ, and 23λ TJ VCSEL, respectively. Additional details on the simulations can be found in Section 1.4.4.3. The results highlight the importance of thick cavity designs for efficient thermal dissipation in dual dielectric DBR VCSELs.

the 7λ (a_1) to the 23λ (c_1) VCSEL, we reduce the temperature change by more than 2X.

Considering this drastic improvement in thermal performance, it is not surprising that all

published VCSELs from our group, with ~7λ cavity designs, have lased under pulsed

current injection,[8,10–15] while Nichia's published dual dielectric DBR VCSELs, with ~23λ

cavities (approximated from the mode spacing observed in the emission spectra), have

shown some of the highest power CW emission characteristics. Viewing Figure 53(a_2), (b_2),
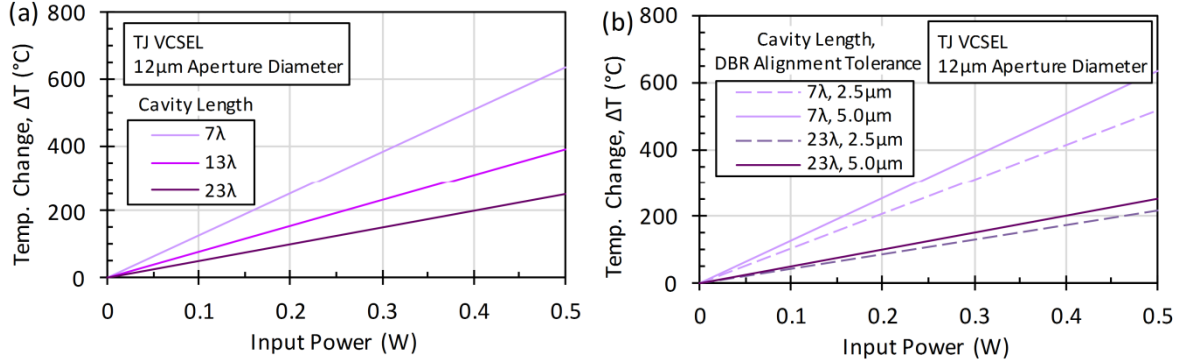
Figure 54 (a) Temperature change vs. input power trends for the 7λ, 13λ, and 23λ TJ VCSELs shown in Figure 53. (b) shows the effect of the aperture to p-DBR alignment tolerance on the temperature change vs. input power trends for the 7λ and 23λ TJ VCSELs, where the previous models all assumed a 5 μm alignment tolerance. The alignment tolerance shows a more significant effect on thermal dissipation for thinner cavities.

and (c_2), we can gain additional insight by observing the change in the flux vector distribution and strength in the cavity. In the 7λ TJ VCSEL, we see the flux vector is very strength due to the large temperature gradient between the active region and the Cu submount. Additionally, we see that most of the thermal dissipation actually occurs laterally on the n-side of the device. As we increase the TJ thickness on the p-side of the device (and increase the n-GaN thickness on the n-side of the device by a less significant amount), the thermal flux is more equally distributed on the p-side and n-side of the device, causing the overall thermal gradient between the active region and the Cu submount to be significantly reduced. This same general trend can be seen in Figure 54 (a), where we plot the temperature change vs. input power for the three different TJ VCSEL cavity lengths.

Because the thermal dissipation occurs laterally in dual dielectric DBR VCSELs, it is easy to imagine that improving the p-DBR to aperture alignment tolerance would improve thermal performance, as it would allow one to place the Au layer (i.e. the contacts to the TJ) closer to the edge of the aperture, thereby reducing the lateral distance for heat to travel before reaching the highly conductive metal layers on the p-side of the device. Figure 54(b) shows the temperature change vs. input power for 5 μm and 2.5 μm p-DBR to aperture

alignment tolerances on the 7λ and 23λ TJ VCSELs. All the previous simulations assumed 5 μm alignment tolerances, as this is easily achievable using a contact aligner (discussed more in Section 2). Here, we can see more quantitatively that improving the alignment tolerance has a significant impact for 7λ TJ VCSELs, but does not change the thermal performance much for 23λ VCSELs.

In summary, the most effective way to improve the thermal performance of a dual dielectric DBR VCSEL is to increase the cavity length. This significantly reduces the thermal spreading resistance away from the active region. For thick cavities, reducing the alignment tolerance from 5 μm to 2.5 μm, only marginally improves performance.

1.4.6. Lateral Confinement and LP Modes

Besides the longitudinal mode and cavity thickness effects present in a VCSEL, one must also consider the lateral mode. This topic is particularly complicated for III-nitride VCSELs because many of the published devices show anomalous filamentary lasing in the aperture (i.e. a randomly distribution of lasing spots within the aperture), instead of the well-controlled linearly-polarized (LP) mode profiles one would expect to observe. Furthermore, recent results suggest that poor current spreading in 7λ cavities can lead high order LP modes to preferentially lase over lower order modes. In this section we will cover the various aspects of lateral confinement relevant to dual dielectric DBR VCSELs, with a focus on using simulations to gain insight into III-nitride VCSEL behavior. Specific details on aperture designs and the implications for lateral confinement in III-nitride VCSELs will be discussed in Section 4.2. The main goal of this section is outline some of the more

fundamental concepts necessary to consider lateral confinement and the LP modes in VCSELs generally.

The lateral confinement in a VCSEL can generally be considered to be similar to the lateral confinement in a fiber optic, thus having a basic understanding of fiber optics can be very useful for understanding VCSELs.[7] In fiber optics, the lateral confinement is defined by the refractive index between the core and cladding of the fiber. In a VCSEL, the core is the aperture of the device, whereas the cladding is the area outside the aperture. Because a VCSEL is made up of many different layers within the core and cladding, the core-cladding index contrast must be converted into the effective core-cladding index contrast, Δn_{eff}, where the core index is equal to the effective cavity index, $n_{eff,core} = n_{eff}$ (Eqn. (25)), and the cladding index is equal to the effective cladding index, $n_{eff,clad}$, which is obtained in the same way the effective cavity index is obtained, but we average over the refractive index values for the layers outside the aperture of the device. If the core-cladding index contrast is equal to zero, no index confinement occurs and the laser is purely gain guided. This implies that the modal confinement is achieved by current injection into the aperture leading to a carrier density induced increase in the refractive index in the aperture, which then leads to a small degree of core-cladding index contrast. Thus, even in the gain guided case, there is really index guiding, but the index guiding is not present until current is injected into the aperture. Additional details on the lateral mode confinement in a gain-guided structures can be found in Refs. [181,182].

For discussing the lateral confinement generally, it is important to realize that the refractive index of a material is related to the specific temperature of the material, as well as the carrier density of the material. As was stated previously, an increase in carrier density

can lead to an increase in index.[183,184] Similarly, an increase in temperature can lead to an increase in refractive index.[185] The relationship between refractive index, carrier density, temperature, and bandgap can be qualitatively recognized from some very general concepts in materials science (i.e. the Clausius–Mossotti equations). Basically, all material properties are related to bond strength. A higher bond strength implies a larger electron affinity, which implies a larger bandgap (i.e. bond strength is proportional to bandgap). Similarly, electrons which are more tightly bound to a crystal would interact with an electric field passing through the crystal less. If the velocity of this electric field (i.e. light) passing through the crystal is only slightly decreased, relative to its velocity in vacuum, then the material must have an index slightly greater than that of vacuum (i.e. $n = 1$). Thus the refractive index is inversely proportional to the bond strength and bandgap, E_g. Considering these general trends with Table 1 and the periodic table, it is not surprising to see $E_{g,AlN} > E_{g,GaN} > E_{g,InN}$ and thus $n_{AlN} < n_{GaN} < n_{InN}$. Extrapolating these relationships to temperature effects, we can easily imagine that a higher temperature would lead to weaker bonds, thus inducing a lower electron affinity, lower bandgap, and higher refractive index. Considering the carrier density effect, we can imagine that a higher carrier density implies fewer electrons are strongly bound, thus the refractive index is increased. Naturally, all of this analysis is qualitative, but it is useful to keep these general relationships in mind.

With this conceptual framework of refractive index effects and the core-cladding index contrast in mind, we are now ready to consider the lateral confinement in more detail. We saw previously that a VCSEL would be purely gain-guided if no core-cladding index contrast is present prior to current injection. This is generally not very favorable because of the weak modal confinement, which can lead to extra loss in the device, however most III-

nitride VCSELs designs are very weakly index guiding, which is likely why most devices suffer from filamentation (Section 4.2). For an index guided VCSELs, the number of potential laterally confined modes is defined by the effective index contrast between the core and cladding, as well as the aperture diameter of the VCSEL. More specifically, for *multi-mode* fibers or VCSELs, the number of confined modes, N_m, can be approximated as

$$(29) \quad N_m \approx \frac{1}{2}V^2,$$

where V is the normalized frequency.[7] The normalized frequency for a given core-cladding design is defined as

$$(30) \quad V = k_0 \frac{1}{2}d\sqrt{n_{eff,core}{}^2 - n_{eff,clad}{}^2} = \frac{2\pi}{\lambda}\frac{1}{2}d\sqrt{n_{eff,core}{}^2 - n_{eff,clad}{}^2},$$

where k_0 is the free-space wavenumber, d is the aperture diameter, and λ is the mode (lasing) wavelength. This relationship highlights the fact that a higher core-cladding index contrast actually favors multi-mode operating devices, which is undesirable for many applications. Yet, as we will be seen in Section 4.2, a higher core-cladding index contrast is favorable for lateral confinement. Thus, in order to achieve single mode operation while using a VCSEL design with a high core-cladding index contrast, researchers have used a number of surface-relief designs, or introduced patterned lossy (metal[186] or Zn-diffused[187,188]) areas in the aperture. [4] Because III-nitride VCSELs research is still in its infancy, these more complicated mode selection techniques have not been investigated. However, in the III-nitrides, non-uniform current spreading has recently been shown to lead to significant lateral mode selection, though in a rather non-ideal manner (Section 4.2).[13] Considering Eqn. (29) and Eqn. (30), we can also make some general conclusions about the relative number of modes expected from III-nitride VCSELs vs. GaAs-based and InP-based VCSELs. Specifically, assuming a set of VCSELs, emitting in the violet, red, and infrared

regime, have the same aperture diameters and core-cladding contrast, the normalized frequency will be greatest for the violet VCSEL, thus it will support the highest number of possible modes. Overall, the short wavelength for III-nitride VCSELs implies that it is virtually impossible to achieve single mode operation just by varying the diameter of the device.

Each of the laterally confined modes, commonly referred to as linearly-polarized (LP) modes, has a different mode profile, identified according to its radial and azimuthal (i.e. around the circumference of the aperture) distribution of the electric field. Each mode has two indices used for labeling purposes: (1) the radial modal index, m, and (2) the azimuthal index, l. Thus an arbitrary mode is identified as the LP_{lm} mode. It should be noted that LP modes are actually made up of combinations of EH, HE, TE, and TM modes,[4,7,189] but going into detail on this is not of much practical use here. To understand which LP mode is the 1st order, 2nd order, 3rd order, etc. mode, we must consider the relationship between an arbitrary normalized frequency, V, and the normalized propagation constant, b, for the confined LP modes. The normalized propagation constant is defined as

$$(31) \quad b = \frac{n_{mode} - n_{eff,clad}}{n_{eff,core} - n_{eff,clad}},$$

where n_{mode} is effective index for the given mode.[7] The fundamental (1st order) mode has an n_{mode} slightly less than $n_{eff,core}$. The higher the order of the mode, the nearer the n_{mode} value is to the $n_{eff,clad}$ value, and thus the higher the normalized propagation constant, b, for that particular mode. If a specific mode has an n_{mode} value less than the $n_{eff,clad}$ value, then it will not be confined to the aperture (core) of the VCSEL or fiber. The normalized frequency vs. normalized propagation constant trends for an arbitrary VCSEL or fiber-optic are shown in Figure 55. The details of the calculations necessary for generating this plot are
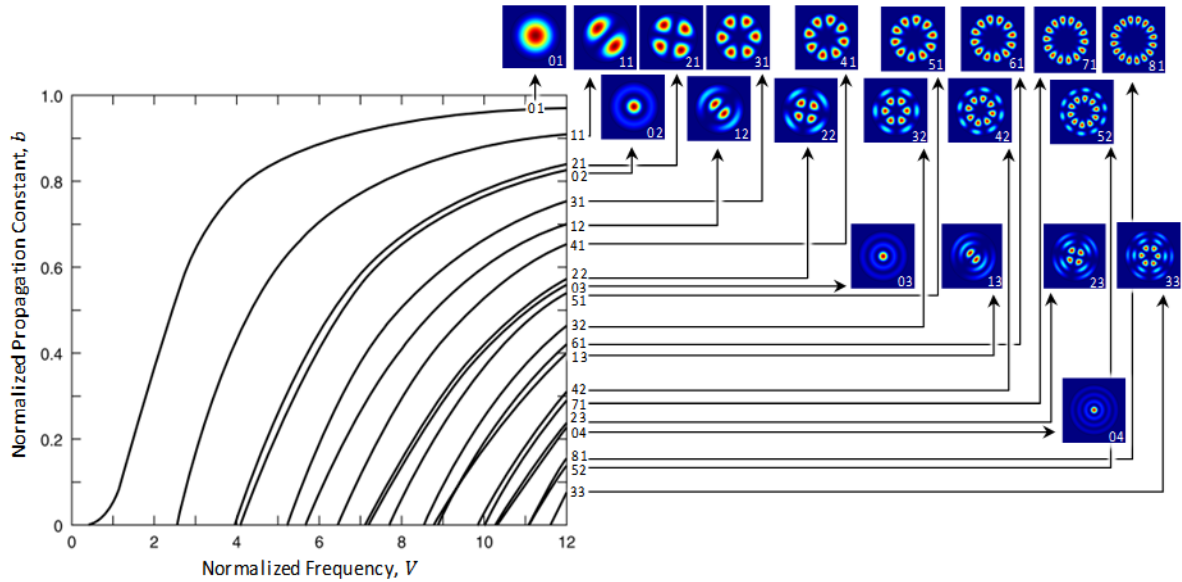
Figure 55 Normalized propagation constant (Eqn. (31)) vs. normalized frequency (Eqn. (30)) for confined LP_{lm} modes.[189] The values of the azimuthal modal index, l, and the radial modal index, m, for each mode are labeled to the right of the plot. COMSOL simulations of the lateral mode profiles (E^2-fields) in the core (aperture), as would be seen from a top-down view of a VCSEL, are shown to the right of the plot.

somewhat tangential to the focus of this thesis, however they can be found in Ref.[7] and Ref.

[189]. Figure 55 shows why the number of modes depends on the normalized frequency, as

stated in Eqn. (29). Here, we also see that for a given normalized frequency, each of the

confined modes will have a unique normalized propagation constant, and thus a unique

mode index, n_{mode}, which defines the order of the mode. The mode with the highest

propagation constant for any normalized frequency is the 1st order (fundamental) mode. As

seen in the lateral mode profiles (E^2-fields) in Figure 55, the fundamental mode is the LP_{01}

mode. This is the mode profile that is most commonly drawn in VCSEL schematics (Figure

41). Using Figure 55 with Eqn. (30) one can easily predict the number of modes expected

from a particular cavity design, as well as the shape of the modes. For normalized

frequencies greater than 12, Eqn. (29) can be used to approximate the number of confined

modes. If the mode profiles for modes of a higher order than those shown in Figure 55 are

required, then a simple 2D core-cladding model can be made in COMSOL, using the
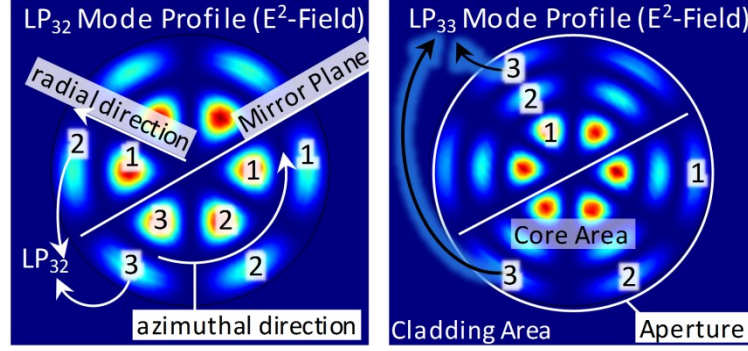
Figure 56 Schematics detailing the labeling nomenclature for LP_{lm} mode profiles. The azimuthal direction, corresponding to the azimuthal modal index, l, is labeled, along with the radial direction, corresponding to the radial modal index, m. The LP_{32} and LP_{33} modes are shown. The mode profiles were generated using a 2D core-cladding model in COMSOLs "Electromagnetic Waves, Frequency Domain" physics package and a "Mode Analysis" study.

"Electromagnetic Waves, Frequency Domain" physics package with a "Mode Analysis" study, to generate the mode profiles for confined and unconfined modes. Furthermore, this type of simulation can be used to analyze non-circular apertures (squares, ovals, etc.), which can display some interesting mode behavior.[190,191] Additional details on these types of simulations can be found in Section 4.2. To identify the correct azimuthal and radial modal index (lm) for a generated mode, one can refer to Figure 56, where the nomenclature is explained schematically.

The lateral confinement for any particular LP mode is defined as,

$$(32) \quad \Gamma_{xy} = \frac{P_{core}}{P_{core} + P_{cladding}}$$

where P_{core} is the total power of the mode confined to the core of the device (i.e. within the aperture), and $P_{cladding}$ is the total power of mode outside the cladding. In general, when making first approximations on the performance of a particular design, it is best to just assume $\Gamma_{xy} = 1$, since the confinement factor can not only vary from mode to mode, but also varies depending on the aperture diameter of the device. Once most of the details of a design are determined, one can easily get an idea for the lateral confinement vs. aperture diameter by focusing on the fundamental mode (LP_{01}). Using a 2D core-cladding fiber model in

FIMMWAVE[192] allows you to easily simulate the lateral confinement vs. aperture diameter for the fundamental mode. However, a similar analysis can be carried out using COMSOL, though some additional coding is required to have COMSOL calculate the lateral confinement factor. Results for the confinement factor vs. aperture diameter for different lateral confinement schemes in III-nitride VCSELs are discussed in Section 4.2.

Beyond the dependence of the *LP* mode behavior on the more passive design specifications, such as core-cladding index contrast, the *LP* mode behavior also depends on a number of more dynamic effects, such as the drive current,[193–195] internal heating,[196] gain offset parameter,[197] and current spreading. The degree to which each of these more dynamic properties affect the *LP* mode depends on the particular structure of interest and there is no experimental work investigating these effects for III-nitride VCSELs, primarily due to the anomalous filamentary lasing that is often observed. However, it is important to be aware of
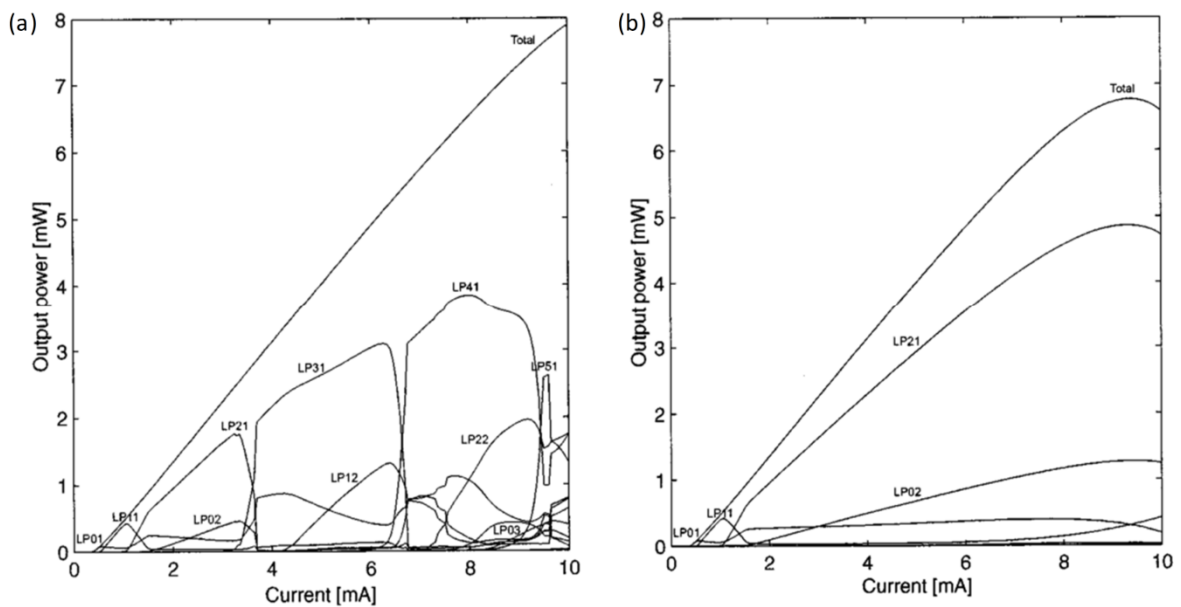
Figure 57 Simulations of the output power vs. current for a GaAs-based VCSEL with an oxide aperture. The contribution to the total power from each of the different LP modes is shown. (a) shows the performance with internal heating accounted for (i.e. under CW operation), while (b) shows the "cold" cavity characteristics (i.e. the performance under pulsed operation). The significant difference in mode selection vs. current is due to thermal lensing under CW operation.[193]

these concepts, thus we will highlight some of the theoretical work reported in the literature.

Figure 57 shows simulation results for an oxide-aperutre GaAs-based VCSEL with heating included (i.e. under CW operation) (a), and without heating included (i.e. under pulsed operation (a "cold" cavity)) (b). The specific values of the LI curve are not really important here, rather we are simply highlighting the dependence of the LP mode section and power for a particular mode, on the drive current for VCSELs. Comparing Figure 57(a) to Figure 57(b), we see that a VCSEL operating under pulsed current injection (i.e. a cold cavity) would have much more stable mode performance over a larger range of currents. This is because under CW operation, the internal heating generated under CW operation creates significant temperature gradients in the cavity, leading to significant changes in the mode selection behavior. Naturally, these results cannot be easily extrapolated to III-nitride VCSELs due to the significant variations in overall device design and material properties, however it is important to recognize that the thermal gradient in a GaAs-based VCSEL would likely be similar to that of a hybrid DBR III-nitride VCSEL, due to the similar vertical dissipation of heat. In comparison, a dual dielectric DBR III-nitride VCSEL would have a significantly different thermal gradient profile, as was seen in Section 1.4.5.2. This further highlights the fact that the dynamic effects shown in simulation-based publications are difficult to generalize for III-nitride VCSELs due to the significantly different thermal behavior in dual dielectric DBR and hybrid DBR VCSELs. Regardless, this dependence of *LP* mode on drive current is why the LI curve for multi-mode VCSELs can sometimes look "bumpy", as the device switches from one mode to the other. This behavior has been observed experimentally, even in III-nitride VCSELs with filamentary lasing characteristics.[8]
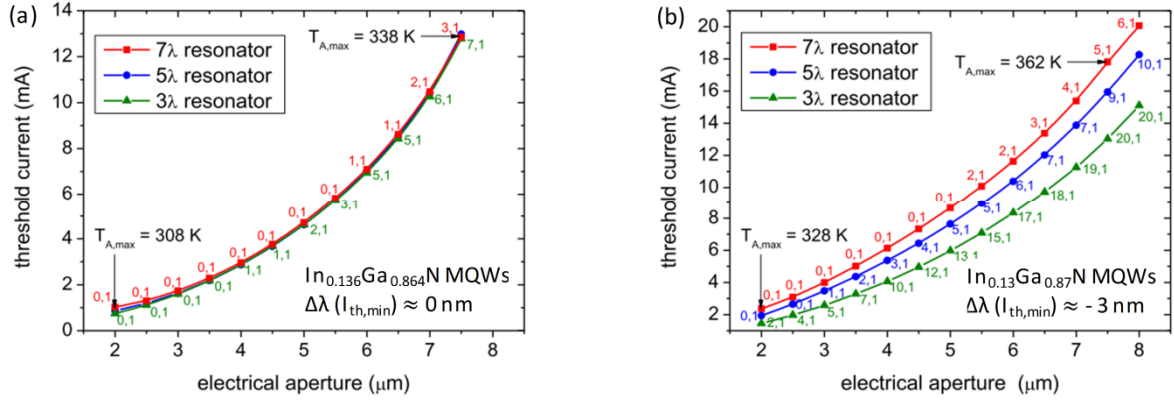
Figure 58 Threshold current vs. aperture *radius* for a simulated 414 nm (cavity resonance wavelength) emitting hybrid DBR III-nitride VCSEL. (a) shows a case where the gain offset parameter, $\Delta\lambda$, is equal to 0 nm (via tuning of the InGaN composition), while (b) shows a case where the gain offset parameter is equal to -3 nm. In each case, each threshold current point has the corresponding $LP_{l,m}$ mode denoted by the *l, m* indices. The gain offset parameter is equal to the peak gain wavelength minus the cavity resonance wavelength. The simulations show that detuning the gain offset can lead to significant variation on the lasing *LP* mode at threshold. The aperture dependence of the *LP* mode also indicates the strong effect current spreading can have on mode selection.[197]

The dependence of mode behavior on operating current has been the most popularly investigated dynamic behavior for lateral confinement in VCSELs, however some recent simulations from Ref. [197] highlight the importance of the gain offset parameter on mode selection. Figure 58 shows the threshold current vs. aperture radius for a simulated 414 nm (cavity resonance wavelength) emitting hybrid DBR III-nitride VCSEL.[197]   Figure 58(a) shows the case where the cavity resonance wavelength is equal to the peak gain wavelength, giving a gain offset of 0 nm, while (b) shows the case where the peak gain wavelength is 3 nm shorter than the cavity resonance wavelength, making the gain offset – 3 nm. For each plotted point, the first lasing *LP* mode is shown. Overall, the results show that using a detuned gain offset can reduce the threshold current, which has also been demonstrated in other material systems, but the detuning also results in a significant variation in the first lasing *LP* mode. Furthermore, the increase in the order of the first lasing LP mode with increasing aperture radius also highlights the significant effect current spreading can have on

mode selection. This particular trend is in agreement with some reported experimental results on dual dielectric DBR VCSELs with air-gap apertures, formed via PEC etching.[13]

In summary, we have described some of the underlying concepts necessary to understand and interpret the lateral confinement and LP mode behavior in III-nitride VCSELs. Due to the highly dynamic behavior of the lateral mode, investigating the lateral mode properties for III-nitrides VCSELs is a research front full of opportunity. From an experimentalist's perspective, developing self-consistent 3D models to precisely predict the *LP* mode behavior for a particular design can be a bit tedious, and experimental variations may lead to significantly different results anyways. Thus it is probably better to just design highly parallel experiments, process a bunch of devices, and generally do things the Google way: "fail fast, learn, iterate". That being said, some good guiding insight can be gained from simple 2D core-cladding models, which will be discussed for specific III-nitride VCSEL designs in Section 4.2. Some other useful references relevant to lateral confinement and LP modes include Refs. [149,198–202].

2. Flip-Chip Dual Dielectric DBR VCSEL Process Flows

"It's supposed to be hard. If it wasn't hard, everyone would do it. The hard is what makes it great."

– A League of Their Own

When I first began VCSELs research many graduate students working on EELDs and LEDs seemed to feel sorry for me because the VCSEL process was so complicated. Initially, I too wished I had some simpler process to make my life a bit easier, but as I became more involved in the project, I began to realize that it is the very complexity of the VCSEL process, and the complexity of VCSELs generally, that make them so interesting to research. Complexity makes things harder and more challenging, but it is the challenge that makes things fun. Thus, if you are a graduate student involved in processing VCSELs, I encourage you to view the complex process as an opportunity to learn and explore more, rather than a burden. In this section we will outline the general process for fabricating dual dielectric DBR flip-chip nonpolar VCSELs with ion implanted apertures (IIAs), buried tunnel junction (BTJ) apertures, or photoelectrochemically etched apertures (PECA) (i.e. an air-gap aperture).

Figure 59 and Figure 60 shows schematics of the process flows for IIA, BTJ, and PECA VCSELs. In Figure 59 details the different process steps for each of the aperture designs. Figure 60 shows the processing steps following the aperture patterning. The schematics shown in Figure 60 are for the IIA VCSEL, however the BTJ and PECA VCSELs would have essentially the same processing steps with variations in the actual structure of the device due to the different aperture designs. The process flow in spreadsheet

form can be found in Table 5, though we will discuss many of the details in this section as well.

Viewing Step (1) in Figure 59, we see the general epitaxial structure grown via MOCVD. The details of this structure are discussed in Section 3.3. The primary detail of note here is the presence of the sacrificial MQW and n-$Al_{0.4}Ga_{0.6}N$ etch-stop layer. The Sacrificial MQW is the enabling feature for the flip-chip substrate removal using photoelectrochemical (PEC) undercut etching, while the n-$Al_{0.4}Ga_{0.6}N$ layer allows the cavity length to be precisely defined. It should be noted that nonpolar VCSELs have been successfully fabricated without the n-AlGaN etch stop-layer,[10] however leaving this layer out makes the device more susceptible to KOH induced roughening on the n-side of the device. Of course, prior to any processing, p-GaN must be activated. Here, p-GaN activation is achieved by placing the sample in a furnace at 600 °C for 15 min, with an air ambient.

Step (2) is the mesa 1 etch, where a reactive ion etch (RIE) is used to etch to a depth of ~1/2 the total thickness of the n-GaN layer. More specifically, one must etch past the active MQW, but not past the sacrificial MQW. The dry etch uses a BCl_3/Cl_2 chemistry with an etch rate of ~120 nm/min. Prior to etching, the chamber is cleaned with an O_2 plasma and coated with BCl_3.

Following Step (2) the process flow is segmented into the different processes for the IIA, BTJ, and PECA. In the BTJ process, Step (2.1-BTJ) shows the MBE growth of the n^{++}GaN TJ contact layer. This is only the first layer of the complete BTJ structure. Following this step, the BTJ process, as well as the IIA and PECA process, require the aperture to be patterned (Step (3)). In the BTJ, this is achieved by simply using a standard photoresist (PR) pattern, followed by a dry etch (RIE) to slightly below the p^{++}GaN layer in

106
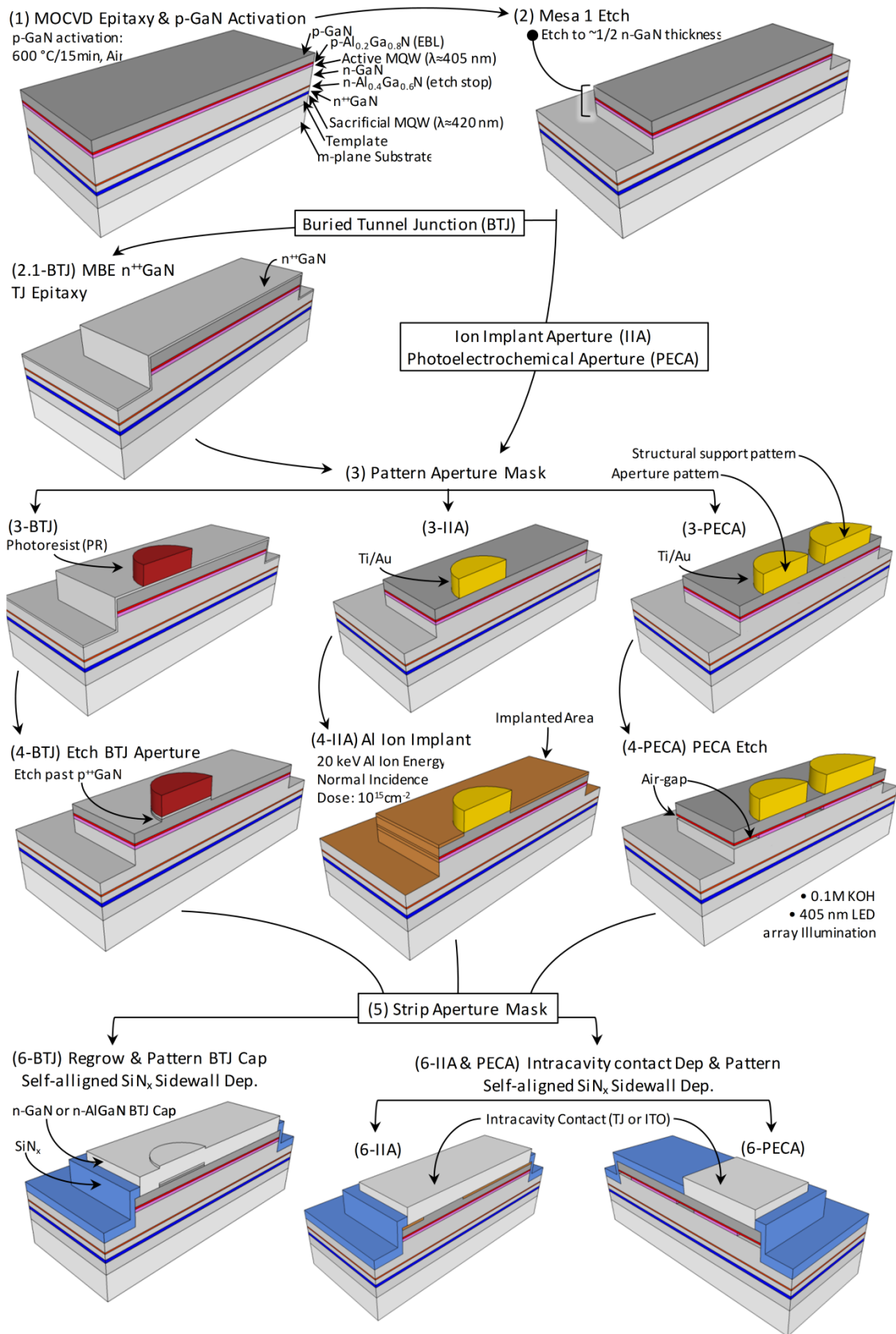
Figure 59 Part 1 of IIA, PECA, & BTJ VCSEL process flow schematics
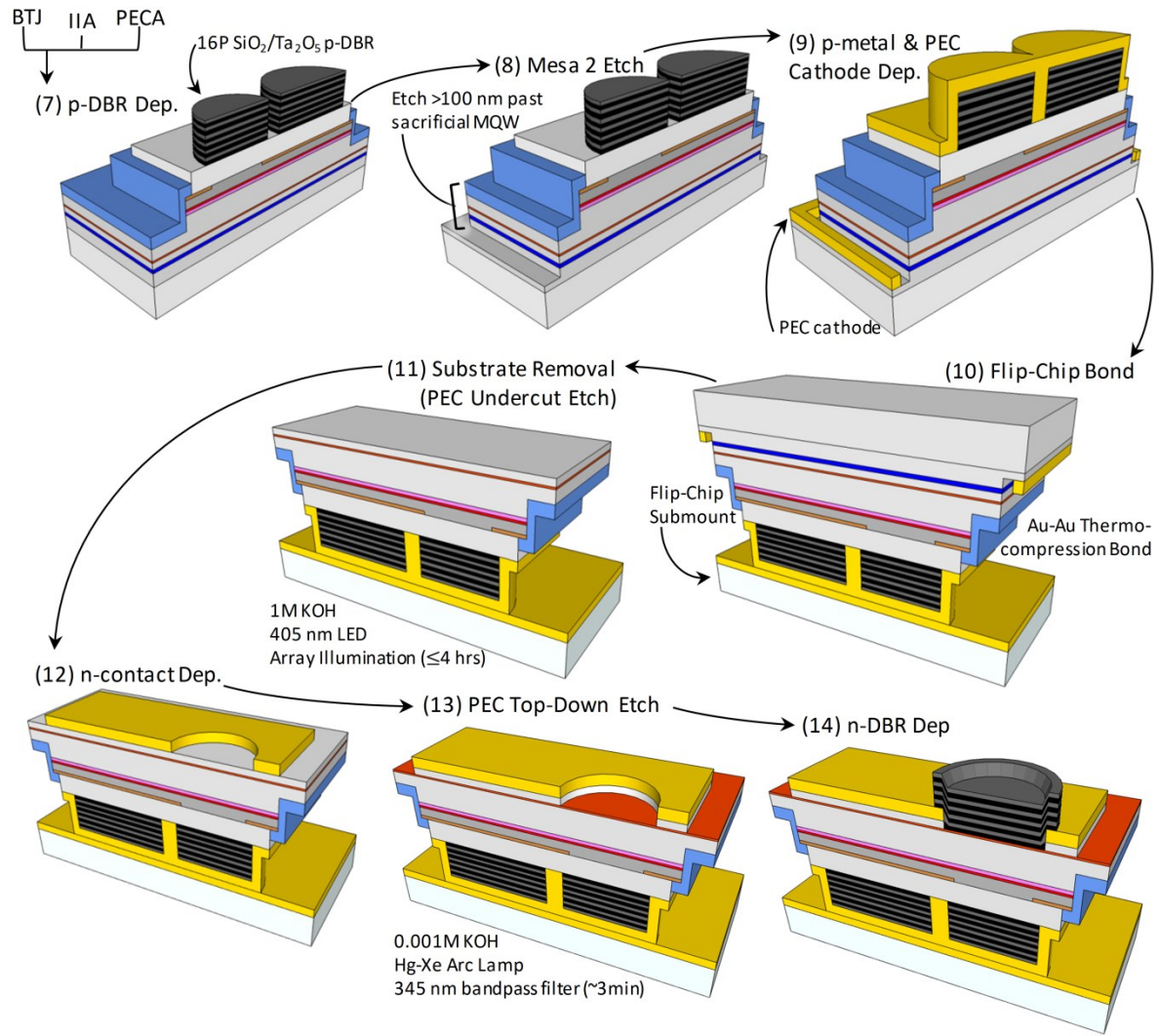
Figure 60 Part 2 of VCSEL process flow schematics. The schematics show the specific structure for the IIA VCSEL design; however the same general steps are applied for PECA and BTJ VCSELs.

the area outside the aperture. Etching to below the p^{++}GaN ensures that the following regrowth of the remaining BTJ layers (Step 6-BTJ) results in a high voltage Schottky contact (i.e. a really bad TJ) outside the aperture. In the IIA and PECA designs, we see a Ti/Au hardmask is used to define the aperture pattern (3-IIA). This is achieved using a standard PR liftoff process. Prior to the metal dep and following the PR development, the samples are immersed in a 1:1 HCl: DI water solution for 30 sec., followed by a dump and rinse in DI water. This ensures good adhesionof the Ti/Au layers, which is particularly

critical for devices with small (4-6 μm) aperture diameters. E-beam deposition is then used to deposit 20 nm Ti, followed by 200 nm Au. In Step (3-PECA) we see that the Ti/Au layer is patterned to not only define the aperture area, but also define a structural support area. This structural support area is necessary to leave room for probing on the n-side of the device after the flip-chip process is completed. It should be noted that the particular design shown here is slightly different than that used in the demonstrated PECA VCSEL,[13] however the concept is the same. The structural design shown in Ref. [13] was far from optimal, as the yield was extremely low due to the fragility of forming a PECA air-gap and the stress introduced during the flip-chip process, as well as general sonication and PR stripping steps. This proposed PECA VCSEL designs would likely result in a higher yield, though the PECA VCSEL is certainly the least structurally stable VCSEL out of all those described here.

Viewing Step (4-IIA) and (4-PECA), we see the particular aperture defining technique. In (4-IIA), the Al ion implantation is performed by Leonard Kroko, Inc., where an Al ion energy of 20 keV, a dose of 10^{15} ions/cm^2, and an incidence angle of 0° (normal incidence) is used. In (4-PECA) we see the formation of the air-gap via selective PEC undercut etching of the active MQW in the areas not covered by the Ti/Au hardmask. Here, the Ti/Au mask simply serves as an opaque layer to block the incident PEC illumination source light. However, it should be noted that a Ti/Au PEC cathode needs to be present in the field of the chip (i.e. off the mesa) in order to replenish the depleted KOH electrolyte. This step uses a low KOH concentration (i.e. 0.1 M KOH) and a 405 nm LED array illumination source (FWHM = 16 nm, ~12 W output power (~65 mW/cm^2)). The demonstration reported in Ref. [13], used an etch time of 30 mins, however this step has not be

thoroughly optimized, and more recent results suggest an etch time as short as 10 mins may be appropriate. It is important to note that using a low KOH concentration is critical for this step in order to minimize the degree of chemical etching during the PECA process. This purely chemical etching can lead to significant roughness, particularly on N-face GaN (Section 3.3.1).

After the aperture is defined in each case, the mask is stripped off (Step (5)). For the BTJ, the PR mask is removed by sonicating in heated (~80 °C) 1165 PR stripper (Microposit remover 1165) for ~5 mins. For the PECA and IIA design, the Ti/Au hardmask is removed in a heated (120 °C) aqua regia bath (3:1 HCl:HNO$_3$). Typically the samples are immersed for 10 mins 2-3 times in new aqua regia solutions each time, for a total stripping time of ~20-30 mins.

Next, the intracavity contact is deposited and patterned on each device (Step (6)). For the BTJ (Step (6-BTJ)) this involves the regrowth of the remaining BTJ cap layers, which may be n-GaN or n-AlGaN. Within the aperture region, the regrowth occurs on top of the n^{++}GaN TJ contact, while outside the aperture region, the regrowth occurs on the etch-damaged p-GaN layer. In the IIA and PECA design, the entire intracavity contact layer is grown or deposited, prior to patterning. It is of note that the BTJ design is not compatible with ITO intracavity contacts, due to the strict limitation of the ITO thickness to ¼-wave (~50 nm), while the PECA and IIA designs are compatible with either a TJ or ITO intracavity contact, though the TJ is arguably the better, but more challenging, option. The intracavity contacts shown in the schematic are more representative of a TJ intracavity contact. In each design, the cap or intracavity contact is deposited on the mesa and in the field. The intracavity contact is then patterned by using a BCl$_3$/Cl$_2$-based dry etch, for III-

nitride layers, or using an MHA (methane-hydrogen-argon) dry etch for ITO. Following the etch, but before the removal of the intracavity contact PR pattern, the SiN_x side-wall layer can be deposited, then lifted-off, yielding a self-aligned sidewall coating layer. This SiN_x layer protects the active MQW from undercut etching during the flip-chip substrate removal via PEC undercut etching (Step (11)). Comparing the SiN_x pattern on the PECA design vs. the IIA design, we see that the dielectric layer in the PECA designs covers a significant portion of the mesa. This is required because the structural support area still contains an active MQW region, thus we must cap this area with dielectric in order to prevent injection into that area. Furthermore, because p-GaN has poor current spreading properties, there will be virtually no leakage between the intracavity contact area (i.e. the aperture area) and the structural support area.

Moving to Figure 60, we see that only the IIA design schematics are shown. This is because all three designs essentially have the same back-end processing requirements, with minor variations in the structural details. At the top of Figure 60, Step (7) shows the p-DBR deposition step. The 16P SiO_2/Ta_2O_5 dielectric p-DBR is deposited using ion-beam deposition (Section 1.4.4.1). Both the n- and p-DBRs use a PR lift-off processes to pattern the samples. In Step (7), we can see the p-DBR layers are patterned over the aperture of the device, as well as the areas that do not receive electrical injection. This is necessary to planarize the mesa for the flip-chip bond (Step (10)). However, one should not cover the entire mesa with the p-DBR layer, as the exposed area of the intracavity contact should be maximized in order to maximize the contact area with the metal contact to the intracavity contact (Step (9)). Furthermore, in order to maximize the heat dissipation in the device, the

metal must be placed as close to the injection area as possible, which is why there is a gap between the two p-DBR coating areas.

Following the p-DBR deposition and patterning, the mesa 2 etch is performed (Step (8)) using an RIE-based dry etch. The field area is etched to > 100 nm past the sacrificial MQW, thereby exposing the sacrificial MQWs side-walls for the PEC undercut etch substrate removal step (Step (11)). It is important to note that the mesa 2 etch should be done after the p-DBR deposition, as the large etch depth can introduce a significant amount of particles. If these particles reside inside the aperture, between the intracavity contact and the p-DBR, they will prevent lasing, but if they sit on top of the p-DBR, they will not affect the optical performance, though they may introduce some structural irregularities. In general, using a chemical detergent, such as Liquinox or Tergitol solution, can significantly reduce the level of particle contamination, while simultaneously helping to keep your glassware clean.

After the p-DBR deposition, the metal contact to the intracavity contact layer is deposited. This contact is also deposited in the field of the sample, where it serves as the PEC cathode, allowing the efficient extraction of electrons back into the KOH solution to replenish the electrolyte and complete the electrochemical circuit (Section 3.3.1). Generally, a Ti/Au contact has been used to contact TJ intracavity contact layers, while a Cr/Ni/Au layer has been used to contact ITO intracavity contacts. Cr is used for adhesion purposes, while the Ni serves as a diffusion barrier. It should be noted that the Ti/Au intracavity contact is likely not ideal and may add some voltage to the device, due to the non-ideal contact resistance between the metal and the TJ, however we have not made attempts to quantify this voltage penalty. Contacts are discussed in more detail in Section 3.6. In Step

(9), we also see the metal layer is conformally coated over the p-DBR. To achieve this conformal coating, an e-beam system with a planetary rotation fixture is used.

The flip-chip bond is shown in Step (10). Here, we see a simple Au-Au thermocompression bond is used. The details of flip-chip bonding are discussed in Section 4.3, however it is of note that the process here uses a very simple graphite fixture, where one simply places the submount and the sample on top of each other and clamps them together with screws. The fixture is then placed in an oven at 200 °C for 2 hrs. More sophisticated tools exist which allow the alignment of patterned submounts to patterned substrates, as well as precise control of the applied pressure and the temperature on the submount and sample itself.

Following the flip-chip bond, the sample is placed in a 1 M KOH solution for $\leq$ 4 hrs, and illuminated through the back-side of the m-plane substrate via a 405 nm LED array (the same as is used for the other PEC etching steps). This LED array provides above band-gap illumination of the sacrificial MQW, resulting in the lateral undercut of this layer. After the PEC undercut completes, the substrate can be lifted off. Ideally, the substrate will simply float off the submount and bonded samples, however sometimes a small amount of force is necessary to separate the substrate. The progress of the PEC undercut etch can be visually analyzed using safety glasses with 405 nm band-pass filters built-in. This filter blocks the illumination source light reflected from the sample, while passing the ~420 nm emission from the photopumped sacrificial MQW. Naturally, this same generally concept could by applied using a micro-PL system to analyze the PEC etching under a microscope.

After substrate removal, the n-contact can be deposited (Step (12)). In the TJ design the metal contact to the intracavity contact can be the same as the n-contact. As suggested,

earlier, we have generally just used a simple Ti/Au n-contact, which is certainly not the optimal contact for n-GaN, but may not add a significant amount of voltage to the device, due to the low operating current of VCSELs. As mentioned previously, keeping this contact area as large as possible can help minimize any added voltage from the contact resistance. This n-contact also serves as the PEC cathode for the top-down PEC etch performed in Step (13).

The top-down PEC etch step (Step (13)) is performed in a 0.001 M KOH solution. The sample is illuminated from the n-side of the device with a Hg-Xe arc lamp in series with a 345 nm bandpass filter. This gives an illumination source excitation energy above the bandgap of the n^{++}GaN contact, but below that of the n-Al$_{0.4}$Ga$_{0.6}$N etch stop layer, resulting in a selective removal of the n^{++}GaN in the exposed areas. The total etch time is ~5 min, however further characterization of this step is recommended. This process is discussed more in Section 3.3.1.

The final step of the process is the n-DBR deposition (Step (14)). Unlike the case of the p-DBR, the n-DBR does not have a defined number of mirror periods for all designs, as different cavity lengths will require different n-DBR mirror periods to achieve an optimal trade-off between the threshold modal gain (threshold current density), and the differential efficiency of the device. Generally speaking though, using 10 to 12 periods is good.

It is important to recognize that the VCSEL process has been evolving with each iteration of the devices, making some of the reported structures appear different. However, the processes shown here likely represent the most optimal iteration of the nonpolar dual dielectric DBR flip-chip VCSEL. The complete process flow procedure can be seen in the Appendix Table 5.

For all lithographic steps in this process, a contact aligner is used. This is in contrast to UCSB EELDs process, where stepper-lithography is used. In most semiconductor devices, a stepper is required if a very fine alignment tolerance (< 1μm) is required. In both the EELD and the VCSEL case though, a 5 μm alignment tolerance is generally acceptable. For the EELDs though, the stepper is also critical to use because it can give very uniform laser stripe patterns. In contrast, the contact aligner can result in wavy patterns on at the edge of PR patterns, which can then lead to rough sidewalls for EELD ridges, inducing a giant scattering loss in the devices. In the VCSEL, there are no long stripes and most of the layers are fairly small circles or squares, thus the contact aligner is well suited for such fabrication. Additionally, in the UCSB Nanofab, the stepper is constantly booked, which can make it problematic to process 10 samples at once. In contrast, the contact aligner does not have a booking schedule and is used by fewer people. Therefore the contact aligner is arguably much more efficient to use for VCSEL processing.

As was mentioned in Section 1.4.5.2, improving the alignment tolerance between the aperture (Figure 59, Step (3)) and the p-DBR (Figure 60, Step (7)) could allow one to reduce the p-DBR diameter, thereby placing the Ti/Au coating closer to the aperture, and thus improve thermal dissipation. This could be achieved by combining the advantages of the contact aligner with the stepper by using the stepper for only the aperture to DBR alignment step, thereby allowing a 1 μm alignment tolerance for that particular layer. That being said, improving the alignment tolerance below 5 μm only marginally improves thermal dissipation for thicker (23λ) cavities. As there are many more critical areas to investigate for improved performance, waiting to use the stepper until other areas are optimized is a good idea.
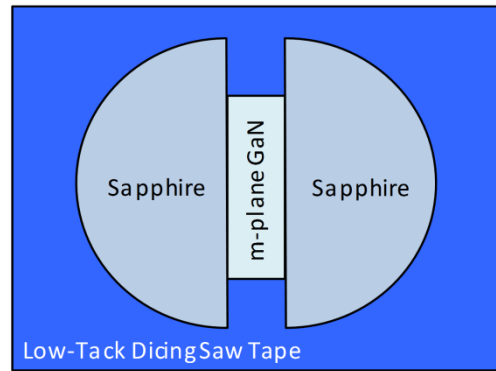
Figure 61 Schematic diagram of sapphire corral used for minimizing edge-bead during PR spinning for m-plane and semipolar GaN substrates.

One of the other notable advantages of a stepper is that it does not require edge-bead removal, as the mask does not come into contact with the sample. In contrast, the contact aligner does require edge-bead removal, which can be problematic as it can introduce particles and create more opportunities for human error (i.e. scratching the PR with tweezers, losing the sample somewhere in the fume hood, etc.). Edge-bead removal is particularly problematic in nonpolar and semipolar bulk-GaN processing because these samples are very small (Figure 65(a)). In order to minimize the edge-bead, we have developed a simple method for using sapphire corrals during the PR spinning process. This concept is shown schematically in Figure 61. By placing the sapphire pieces on each side of the m-plane sample, one can more easily wick away the PR from the edge of the sample, thereby allowing you to only need to remove edge-bead from the short sides of the sample.

3. Nonpolar (m-plane) VCSEL Epitaxy

"Whether you fear it or not, disappointment will come. The beauty is that through disappointment you can gain clarity, and with clarity comes conviction and true originality."

– Conan O'Brien

MOCVD epitaxy in an academic research environment can be a bit of a tedious task. There are often many students growing different structures on the same reactor, which can lead to significant variations from month to month. Furthermore, many students have projects that rely heavily on investigating growth conditions, making the reactors very crowded with users overall. Therefore, it is recommended that graduate students focus on designing experiments that can bring rapid results in 1 growth cycle. Furthermore, because the MOCVD reactors are very crowded, it is generally better to just grow a large series of samples and carry out a full VCSELs process, instead of doing some kind of quicktest. Going through the full VCSELs process for each growth will not only free-up reactor time for projects that are more heavily dependent on analyzing growth conditions, but it will also increase the probability of some growth series being publishable.

The basic motivation for using m-plane for VCSELs and light-emitters generally was described in Section 1.3.4. To summarize, m-plane is advantageous over c-plane for VCSEL due to its higher material gain, lower transparency carrier density, and 100 % polarized stimulated emission characteristics. In this section, we will discuss some of the specific epitaxial growth investigations performed to optimize m-plane VCSELs, while also highlighting some of the critical growth considerations unique to m-plane GaN.

Additionally, we will highlight the details of why m-plane is particularly well suited for flip-chip substrate removal via PEC undercut etching.

3.1. m-Plane Bulk GaN Growth

Prior to going into the specific details of m-plane MOCVD epitaxy for VCSELs, it is important to have some historical perspective. In general, III-nitride devices have been grown on sapphire or SiC substrates. These heteroepitaxial growth methods can produce high quality devices, however homoepitaxial growth of III-nitrides on bulk GaN allows significant reductions in the threading dislocation density, while simultaneously opening up the possibility for epitaxial growth on nonpolar and semipolar orientations. For this, and other reasons,[118] growing bulk GaN boules have been of great interest for many years. The fundamental challenge for growing bulk GaN, compared to other III-V compounds, is the extremely high melting point of GaN (2500 °C)[203] and the high dissociation pressure of N (~45000 atm).[204] Because of these challenges, the earliest reports of bulk-GaN growth used hydride-vapor (or halogen vapor) phase-epitaxy (HVPE) to grow bulk-GaN on sapphire substrates.[205] HVPE, like MOCVD, is a chemical-vapor transport process, thus it does not rely on the growth of bulk GaN from a melt. More recent techniques, such as acidic ammonothermal growth, have shown great promise for growth of large bulk GaN boules, yet HVPE is still the most well established technique and is currently the technique used to manufacture semipolar and nonpolar bulk GaN substrates, such as those used to fabricate the VCSELs discussed here. Specifically, the HVPE m-plane substrates used for these VCSELs are manufactured by Mitsubishi Chemical Corporation (MCC).[206,207] Figure 62 shows some of the HVPE bulk GaN research result from MCC.[206,207] Figure 62(a) shows an HVPE bulk
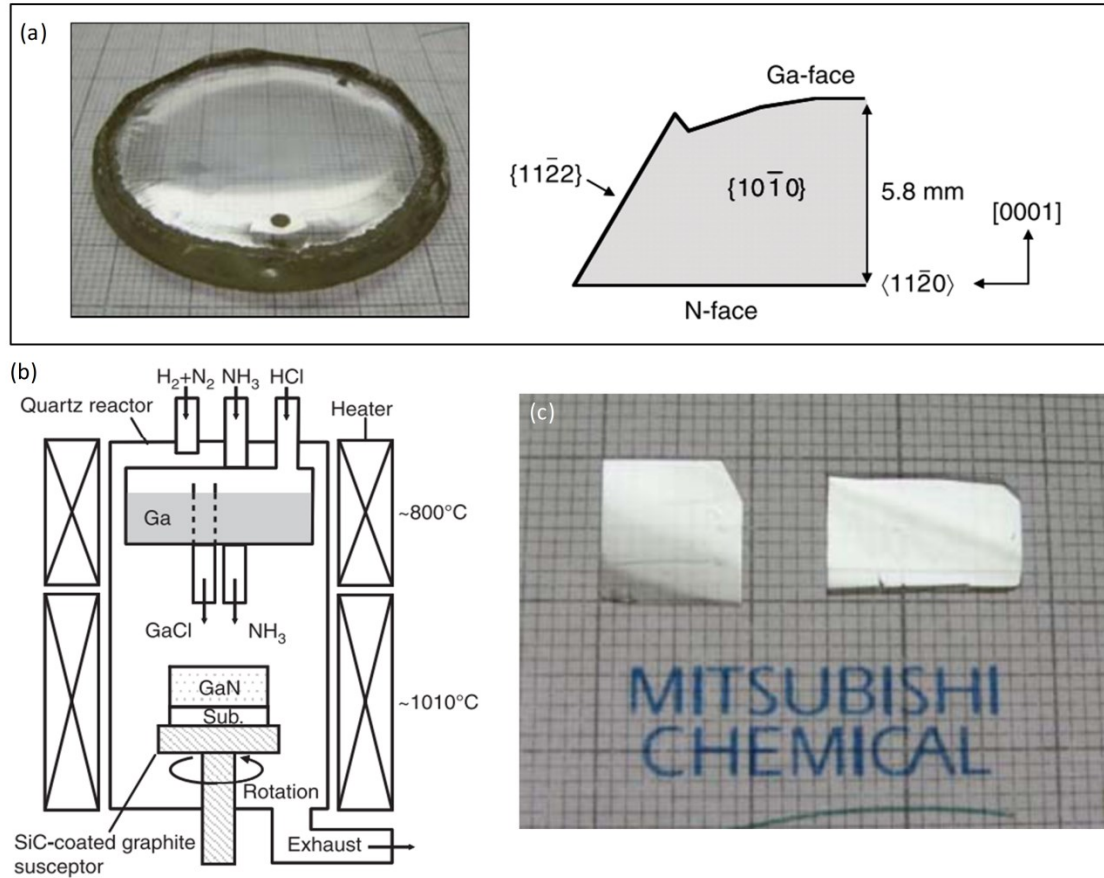
Figure 62 (a) (left) image of an HVPE grown bulk GaN samples from MCC. The growth occurs in the c-direction. (a) (right) schematic cross-section showing the different crystal growth facets. (b) schematic of the HVPE reactor. The chemical-vapor based operation of the reactor can be seen. (c) image of processed m-plane substrates after chemical-mechanical polishing (CMP). The m-plane substrate is made from a cross-section of the c-plane oriented samples, shown in (a).[207]

GaN crystal grown on a sapphire substrate, with an MOCVD grown GaN template. Figure 62(b) shows a schematic of an HVPE reactor, where we can see the different chemical compounds used to grow the bulk GaN. On the right side of Figure 62(a), we can see that HVPE growth yields relatively thin bulk GaN (~6 mm in the [0001] direction). Furthermore, because the preferential growth direction is in the c-direction, and because the bulk layers cannot be grown effectively much thicker than ~6 mm, one cannot achieve a large area m-plane GaN substrate. More specifically, in order to make an m-plane substrate from an HVPE sample, one must essentially make cross-sections of the large diameter c-plane oriented sample, thus the width of the m-plane substrate is equal to the thickness of the
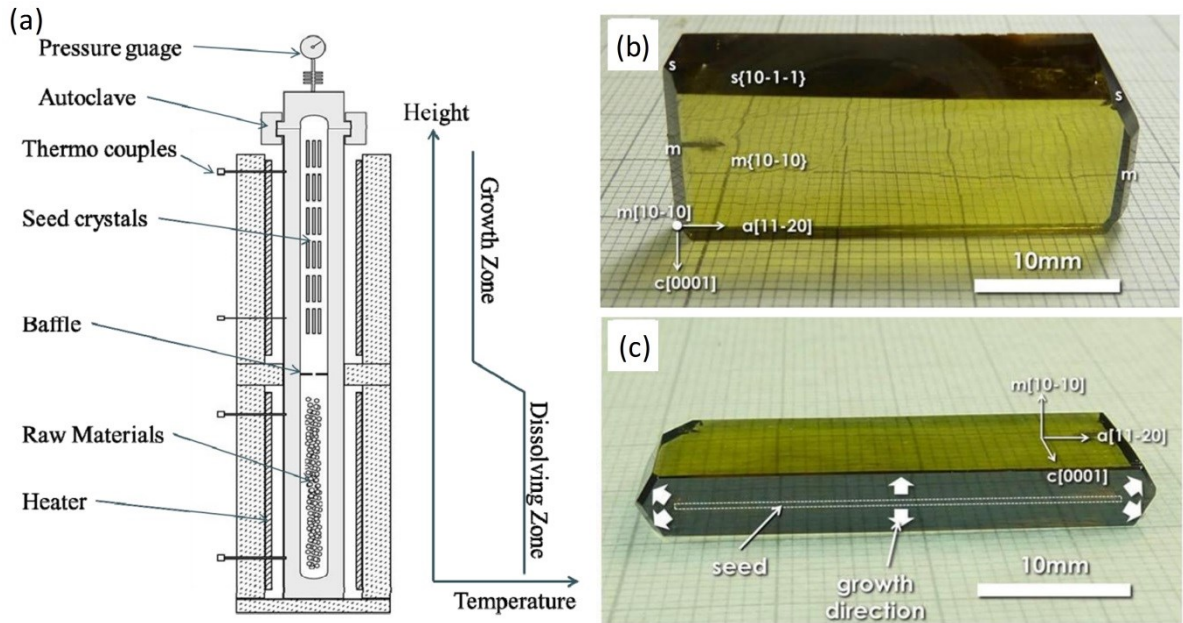
Figure 63 Summary of acidic ammonothermal results from MCC. (a) shows a schematic of MCC's acidic ammonothermal SCAAT[TM] reactor. (b) and (c) show 2 different perspectives of the m-plane bulk GaN crystals grown via acid ammonothermal growth from m-plane bulk GaN seeds.[208]

c-plane oriented growth. This is shown in Figure 62(c), where a set of epi-ready m-plane substrates are shown, after chemical-mechanical polishing (CMP). It is of note that these substrates are ~1/2 the size of the HVPE grown m-plane substrates that MCC now manufactures, which are used for VCSEL growth. An image of the actual m-plane substrates used for growth can be seen in Figure 65(a), which will be discussed in more detail later.

It is important to note that although HVPE grown bulk GaN is currently the standard, acidic ammonothermal shows great promise for m-plane bulk GaN growth,[208] particularly for flip-chip devices. Figure 63 shows a summary of MMC's acidic ammonothermal m-plane bulk GaN growth.[208] In Figure 63(a), we see a schematic of MCC's SCAAT[TM] acidic ammonothermal reactor. Here, we can see that one of the advantages of this technique is that it allows one to co-load many seed crystals, thereby dramatically increasing the yield per growth cycle. Figure 63(b) and (c) show the relatively large m-plane crystal ingots resulting from this growth method. Unfortunately, acidic ammonothermal growth tends to result in

crystals with high impurity content, causing them to have a yellow-tinge and be quite absorptive. For some device designs, this is certainly an issue, however for a flip-chip device, the native GaN substrate is removed during the flip-chip process, thus the transparency of the GaN substrate does not matter. This makes acidic ammonothermal growth particularly of interest for fabricating flip-chip VCSELs, but also any flip-chip LED or EELD.

In all, there is still a great deal of development to be done to make m-plane substrates more of a cost-competitive consideration, compared to sapphire or SiC substrates. Yet, there are many niche applications that can sacrifice cost for performance demands. III-nitride VCSELs, and m-plane nonpolar VCSELs in particular, offer many unique performance properties, compared to EELDs and LEDs, thus VCSELs are particularly well suited for niche applications that can tolerate increased cost for improved performance.

3.2. m-Plane Epitaxy Overview

Beyond the challenges in achieving m-plane bulk GaN substrates, the m-plane epitaxy itself is challenging due to the tendency for irregular growth morphology that depends on the epitaxial method (MBE vs. MOCVD), as well the indium composition (i.e. emission wavelength) in the active region of the device. In the early stages of m-plane epitaxial development, MOCVD epitaxy was performed on nominally on-axis bulk m-plane GaN substrates (i.e. no miscut).[209,210] On-axis m-plane epitaxy results in pyramidal morphological features, generally referred to as pyramidal hillocks, shown in Figure 64.[211] Figure 64(a) and (b) show atomic force microscope (AFM) images of an on-axis m-plane sample after MOCVD epitaxy. (a) shows the standard AFM height-retrace, while (b) shows
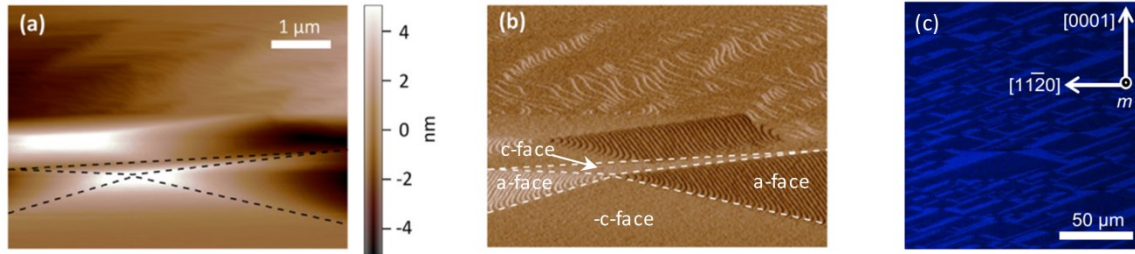
Figure 64 Atomic force microscope (AFM) height retrace (a) and amplitude retrace (b) for MOCVD epitaxial layers grown on a nominally on-axis m-plane substrate.[211] The images show the pyramidal hillocks. (c) shows a fluorescence microscopy (FLM) images of an MOCVD epitaxial growth on an on-axis m-plane substrate, taken with a 450 nm long-pass filter.[212] The different color on the different facets of the pyramidal hillocks indicates a difference in emission wavelength. The epitaxial structure is a single QW LED, where the c-faces are observed to emit at ~424 nm and the a-faces emit at ~465 nm.[212]

the amplitude retrace, which basically applies an artificial light source to the map of the AFM probe tip's z-amplitude values, thereby highlighting to appearance of fine-scale surface morphology, such as the atomic steps along the faces of the pyramidal hillocks. Naturally, a rough surface morphology is not favorable from a scattering loss and QW uniformity perspective, however, as shown in Figure 64(c),[212] the different facets of the pyramidal hillocks also emit at different wavelengths. This is a result of the variation of the band-structure on the difference faces of GaN, discussed in detail in Section 1.3.4. Specifically, the c-faces of the pyramids emit at shorter wavelengths than the a-faces, due to the larger bandgap on c-plane vs. a-plane.

These pyramidal hillocks were discovered to be a result of spiral dislocation propagation in the vicinity of a screw component threading dislocation (TD).[213] To suppress their formation one must engineer the frequency of the step edges passing the screw component TD, to be greater than the angular frequency for spiral growth at the screw component TD. A schematic of this concept can be found in Ref. [213]. This is achieved by tuning the substrate miscut until some critical angle is reached that suppresses the pyramidal hillock formation. Many miscut angles have been investigated,[209–214] leading to the realization that a 1° miscut in the [000$\bar{1}$] (i.e. a -1° miscut) is arguably the optimal miscut
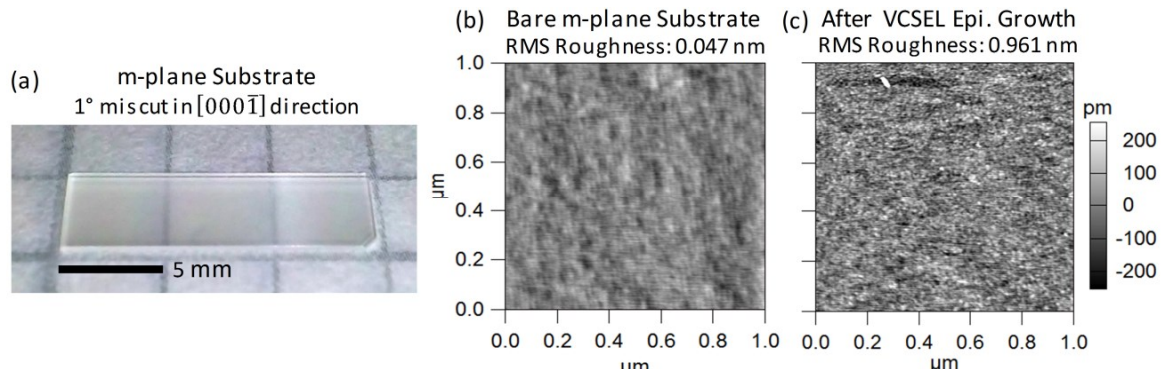
Figure 65 (a) image of a typical m-plane bulk GaN substrate with a 1° miscut in the $[000\bar{1}]$. The substrate is manufactured by MCC. (b) AFM image of the substrate prior to MOCVD epitaxy. (b) AFM image of the substrate following the growth of standard PEC etch compatible VCSEL epi. structure (Section 3.3). The epitaxial growth typically yields an RMS surface roughness of < 1 nm.

for violet emitting devices. Figure 65(a) shows an image of a typical m-plane substrate used for nonpolar flip-chip VCSEL growth and fabrication. The substrate has a nominal miscut of 1° in the $[000\bar{1}]$ direction. Viewing Figure 65(b) and (c) we also see the surface roughness of the substrate before (a), and after (b), epitaxial growth of a standard PEC etch compatible VCSEL epi. structure (Section 3.3). The VCSEL epitaxial growth on the -1° miscut m-plane substrates typically yields a RMS surface roughness of < 1 nm. The highly smooth nature of the growth is also visible in the TEM cross-sections shown in Figure 66.

It is of note that m-plane shows significantly different morphological, miscut, and emission characteristics as the InGaN composition is pushed from violet to blue wavelengths, leading to the development of double miscut substrates for blue emitting m-plane devices.[211,214] Furthermore, because MOCVD and MBE growth operate in different growth regimes, the optimal m-plane miscut is different for the two growth techniques.[215,216]

To conclude, growing on m-plane bulk GaN can introduce a number of unique morphological and emission characteristics not observed on c-plane. Overall, this implies that optimal growth conditions on c-plane do not easily translate to m-plane. Yet, these significant differences also open up new research directions and opportunities for

publication, making m-plane, and non-c-plane devices generally, of great interest from an academic perspective. Beyond academia though, the intrinsic advantages of m-plane, such as higher material gain, lower transparency carrier density, and 100% polarization for nonpolar VCSEL arrays, makes this orientation of particular interest. In the following sections we will discuss the details of the m-plane epitaxial growth for nonpolar VCSELs.

3.3. Epitaxial Structures for PEC Etching Compatibility

The basic MOCVD grown epitaxial structure used in the flip-chip dual dielectric DBR nonpolar VCSELs is shown in Figure 66(a). The optimal active region design (number of QWs) depends on the threshold modal gain for a given VCSEL design, however generally an active region with 3 nm InGaN active QWs (A3 nm) and 1 nm unintentionally doped (UID) GaN barriers (B1 nm) is used in our nonpolar VCSELs, in order to minimize the total thickness of the MQW stack, thereby maximizing the enhancement factor for the VCSEL. In Figure 66(b) we show a TEM cross-section for a 10X MQW, A3 nm, B1 nm VCSEL active
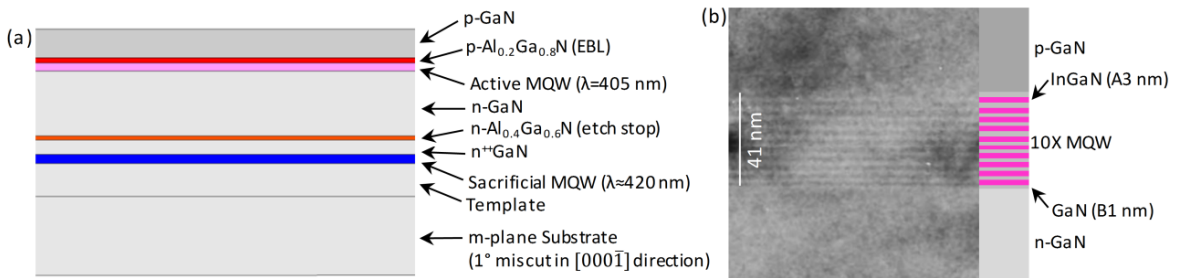
Figure 66 (a) Schematic cross-section of the general MOCVD epitaxial structure for m-plane flip-chip VCSELs. For general compatibility with PEC undercut etching for substrate removal, the n-AlGaN layer is not critical; however it provides additional control over the cavity length and surface roughness on the n-side of a VCSEL. (b) TEM cross-section of a 10X MQW VCSEL active region with 3 nm InGaN active QWs (A3 nm), and 1 nm UID GaN barriers (B1 nm). The total thickness is 41 nm. The cross-section shows each of the QW and barrier thicknesses are roughly equal to the design thickness (A3 nm, B1 nm). (Epi grown by Seunggeun Lee, UCSB and TEM analysis courtesy of Dr. Feng Wu, UCSB).

region. The effect of the number of QWs is discussed in detail in Section 3.4.1. Figure 66(b) is particularly of note because it shows that the real QW and barrier thicknesses are roughly equal to the design thicknesses (A3 nm, B1 nm). In general, the active InGaN QWs have compositions of ~10 % indium, however the actual design parameter is the MQW emission wavelength (405 nm) and not the QW composition itself. The QW composition can be most easily extracted from x-ray diffraction (XRD) measurements, however these measurements require fitting the measured data to a model, and there has been some debate over whether or not some software packages use the correct material parameters for m-plane to generate simulated XRD diffraction spectra.[217] This general issue also applies to measuring AlGaN compositions on m-plane. Another common method for measuring composition is to use secondary-ion mass spectroscopy (SIMS), which can give accurate measurements for thick layers, but has difficulty with thin layers, such as those used for the EBL and QWs. This is a result of the SIMS analysis being performed by essentially creating a crater in the sample and collecting the ions leaving the sample as the surface is bombarded. The crater-like profile of the hole leads to a smearing of interfaces in the measurement. There are some parameters that can be optimized during the SIMS scan that can minimize this smearing, however it is important to recognize that the compositions measured on thin layers are likely averaged over a thicker distance than they are present in the true epitaxial structure. To complicate the XRD or SIMS measured InGaN composition further, it is important to note that many reports show composition fluctuations in the InGaN layers, as well as a physically real smearing of the InGaN/GaN interface.[218–223] This suggests that it is quite possible that the 1 nm GaN barriers used here actually contain some degree of In, though we will generally assume this is not the case for simplicity. Thus, the composition values stated
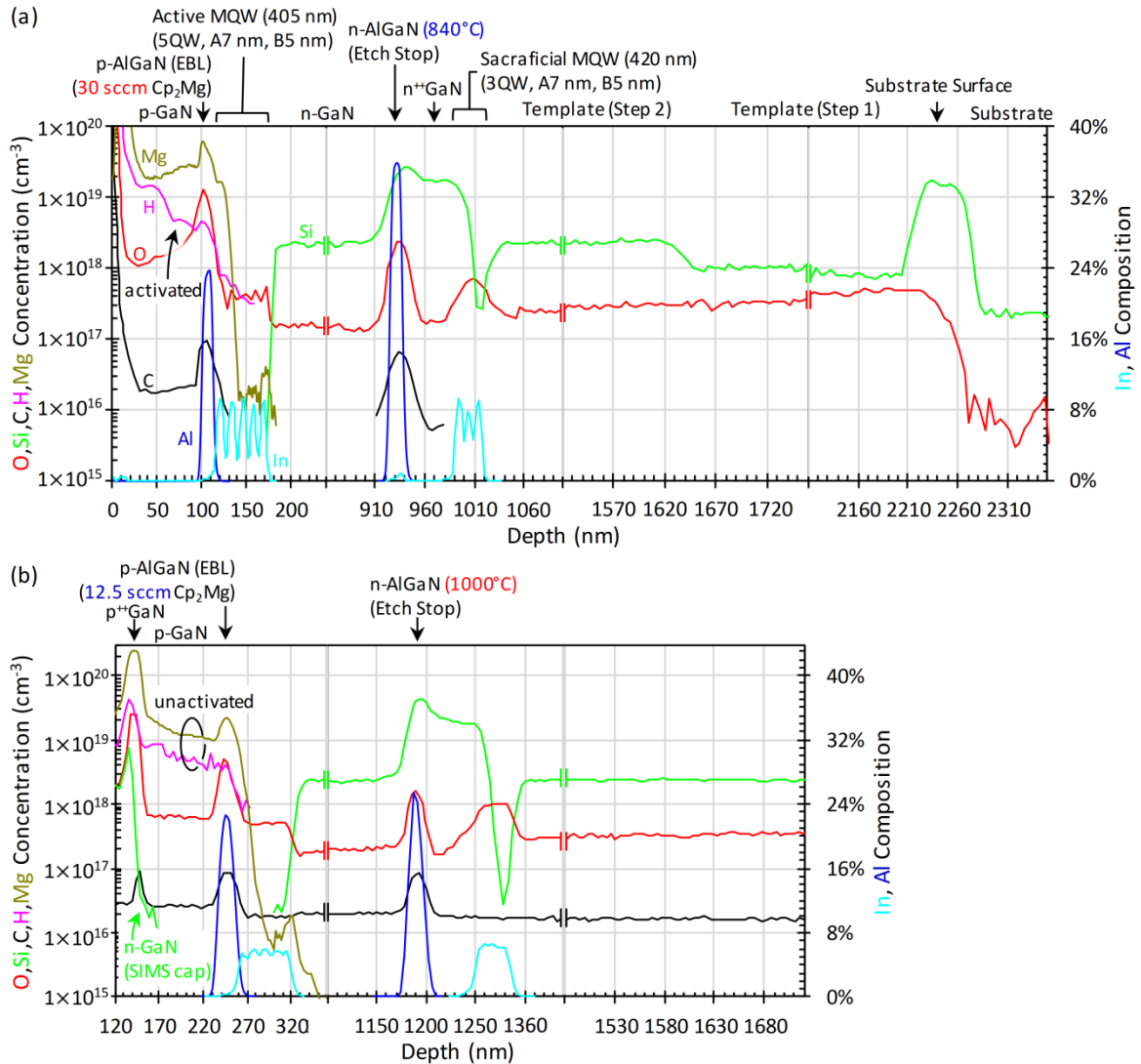
Figure 67 SIMS data taken on ~7λ VCSEL epi. structures. (a) shows the case where the p-GaN layers have been actived at 600 °C for 15 min in air, while (b) shows the case of an unactivated sample which was grown with a n-GaN cap to allow the analysis of the p[++]GaN contact. Each structure also has different p-AlGaN and n-AlGaN growth conditions, which are highlighted on the layer labels. All other layers have the same growth conditions. The plots are segmented into four areas in order to highlight the more relevant areas of the structure. The measured concentrations that were below or equal to the detection limit of the SIMS system have been removed. The details of the optimizations resulting in the more recent VCSEL epi. designs are described in Section 3.3 to Section 3.6. The most recent VCSEL epi. structures[11,12] use active regions with 7QW, A3 nm, B1 nm, and EBL 5nm designs. Also, The EBLs use the growth conditions from (b) (Section 3.4.2), while the n-AlGaN uses the conditions from (a). The template is broken into two separate growth steps for historical reasons and likely has no significant implication for the epi. performance. (The growth recipe ID for (a) is 120901hvSIMS-5QW VCSEL, while (b) is 140515-SIMS_5QW A7B5 VCSEL (JL01)).

should be taken as rough approximation, and one should focus more on the measured

emission wavelengths from a particular layer. Naturally, electrical luminescence (EL) can be

easily used to measure the active region emission wavelengths. However it is also of note

that one can use a He-Cd UV laser to perform photoluminescence (PL) on AlGaN layers in order to measure the relative change in composition (i.e. PL wavelength) between MOCVD growths.

All MOCVD growths reported here were performed at atmospheric pressure with typical V/III ratios (i.e. >3000), and with typical growth temperatures (between 800 °C and 1200 °C). A modified two-flow reactor, similar to that described in Ref. [224], was used for all growths. Ammonia (NH_3) was used as the nitrogen precursor for all layers. For thick n-GaN layers, trimethylgallium (TMG) was used as the Ga precursor, while triethylgallium (TEG) was used for thin n-GaN layers. TMG generally yields higher growth rates (~50 nm/min) than TEG (~5 nm/min), however it also generally results in higher carbon and oxygen impurity concentrations.[225] Trimethylindium (TMI) and trimethylaluminum (TMA) were used as the In and Al precursors in InGaN and AlGaN layers, respectively, with TEG used as the Ga precursor. Bis(cyclopentadienyl)magnesium (Cp_2Mg) and silane (SiH_4) were used as the Mg and Si dopant precursors, respectively. The n-type layers, the QWs, the barriers, and the EBL were all grown with N_2 carrier gas, while the p-GaN layers were grown with H_2 as the carrier gas.

Figure 67 shows SIMS data for early versions of the MOCVD grown VCSEL structures shown schematically in Figure 65(a). All SIMS measurements were performed by Evans Analytical Group (EAG). Observing Figure 67(a) in the direction of growth (n- to p- (right to left on the plot)) we first see the substrate. The HVPE grown, -1° miscut, m-plane substrates from MCC are n-type with a Si concentration of ~2×10^{17} cm^{-3}. The O concertation measured in the substrate is below the detection limit. At the surface of the substrate (i.e. the epi/substrate interface), we see a strong O and Si spike. It is of note that

thermal cleaning of the substrate surface via H_2, which is typically done for growth on sapphire, SiC, or Si substrates, was *not* performed prior to growth. It is possible that such H_2 cleaning could result in faceting of the m-plane substrate, though this was not investigated. Additionally, a low-temperature buffer layer, which is commonly used in III-nitride epitaxy on sapphire, SiC, or Si substrates, is not necessary in growth on bulk GaN, due to the homoepitaxial nature of the growth.

Moving on to the template layer, grown in TMG, the template is roughly 1 μm thick and is broken into a low doped and high doped region. This part of the recipe was simply transferred from older epi. designs and likely has no significant impact on device performance. One could likely reduce the template thickness and remove one of the parts of the template to simplify the recipe and reduce the total growth time.

Following the template, the sacrificial MQW was grown. In all devices, the sacrificial MQW used the same design as C. Holder used in his original nonpolar VCSELs work (3 QW, A7 nm, B5 nm).[16] This layer has never been investigated thoroughly, as it yields satisfactory PEC undercut etching performance. However, the sacrificial MQW design can heavily influence the PEC etching performance, and further optimization of the current design could potentially lead to increased undercut etching rates. Observing the specific In profiles in (a) and (b), we see the measured composition is essentially the same as that of the active MQW. This highlights the previously mentioned limitation of SIMS to accurately resolve thin layers, particularly ones that are deep within the epitaxial stack. Here, the measured indium composition in the three 7 nm QWs is also averaged across four 5 nm GaN barriers, leading to the composition appearing lower than it actually is. Also of note is the difference in resolution between the sacrificial MQW In profiles in (a) and (b),

with (a) more clearly resolving the individual QWs. This is a result of the scan in (a) having the "number of cycles" parameter for the SIMS scan set to 500, while (b) only used 384. Evidently, increasing the number of cycles for the SIMS scan will improve one's ability to resolve thin layers.

The final feature of note in the sacrificial MQW is the spike in the O level. This general increase in the O level is commonly observed in InGaN and AlGaN layers and is likely predominantly a result of the incorporation efficiency of O in the presence of TMA or TMI. However, it is also important to realize that the formation energy for any defect, impurity, or intentionally incorporated dopant, (at thermal equilibrium) depends on the Fermi-level at the surface of a layer during growth.[226–231] During MOCVD growth, the surface is generally not at thermal equilibrium; however this dependence of the formation energy on Fermi-level may still play some role in the incorporation of higher amounts of O in the InGaN layers. In general, the impurity concentration not only depends on the specific precursors used for growth and the Fermi-level of the layer being grown, but also the growth plane itself. There are numerous reports on the difference in impurity uptake on c-plane Ga-face (the standard growth plane) vs. c-plane N-face (a plane of interest for a number of III-nitride electronic devices).[232,233] However, there are also significantly different impurity uptake levels for semipolar and nonpolar planes. In general, the semipolar and nonpolar planes show higher impurity levels than Ga-face c-plane.[234] Some of the implications of this increased impurity concentration for m-plane are discussed in more detail in Section 3.5. Beyond the differences in impurity uptake, there are also significantly different indium incorporation properties on the different planes,[234–237] which we will not go into detail on here.

Viewing the n^{++}GaN layer in Figure 67(a) and (b), we see a Si concentration of ~1.7 $\times$ 10^{19} cm^{-3}. This is the typical doping for the n-contact in the final VCSEL structure. The details of this particular layer will be discussed more in Section 3.6.

After the ~50 nm n^{++}GaN layer is grown, the 15 nm n-AlGaN PEC top-down etch-stop layer is grown. This layer is not required for a general PEC etch compatible structure, and a number of nonpolar VCSELs have been demonstrated without the layer in place,[10] but overall it improves the yield of devices (Section 3.3.1.2). It is of note that the doping in this layer (~2.7 $\times$ 10^{19} cm^{-3}) needs to be higher than the doping of the n^{++}GaN and n-GaN layers, in order to prevent the n-AlGaN from acting as an electron blocking layer. This can be realized by observing band-diagram simulations using SiLENSe, however it is also easily recognized based on a basic understanding of the requirement for the Fermi-level in a structure to be constant, while the relative separation between the Fermi-level and the conduction band and valence band depends on the doping and bandgap of the particular layer. Also of note in this layer is the sharp increase in the carbon and oxygen contamination levels. This is constantly observed for all layers grown in TMA, suggesting it is related to this particular precursor. However, it is also of note that n-AlGaN shows lower contamination levels than p-AlGaN. As mentioned previously, this may be a result of the dependence of the formation energy for a given impurity being a function of the Fermi-level, though it may also be a result of the different contamination levels introduced by using Cp_2Mg vs. SiH_4 precursor. Yet if we observe the contamination level in (a) and (b) we see that the oxygen and carbon impurity level do not depend on growth temperature, which suggests that they are more likely an intrinsic property of the TMA precursor rather than some thermodynamically related effect.

Further comparing the n-AlGaN layer in Figure 67(a) to (b), we see a decrease in the n-AlGaN composition when the temperature is increased from 840 °C to 1000 °C. The SIMS Al concentrations shown are likely lower than the real concentrations in the layers, due the limitation of SIMS to resolve thin layers. However, assuming the designed thickness of 15 nm is equal to the grown layer thickness, one can estimate the real composition by adding the Al content outside the 15 nm thickness range (centered at the peak of the Al spike in the SIMS profile) to the Al content in the 15 nm thickness range. Doing so gives an Al content, x_{Al}, of ~40% for the 840 °C sample and ~32% for the 1000 °C sample. This implies the change in the Al content per °C change in growth temperature, $\Delta x_{Al}/\Delta T_{growth}$ is ~0.05 %/°C.

Following the n-AlGaN growth, the n-GaN layer is grown, which makes up the majority of the cavity. The Si doping of this layer was held at ~2.3 × 10^{18} cm^{-3} for all devices. Yet it is of note that one could potentially benefit from reducing this doping, or using a step-function doping, with the higher doped layer aligned to the nulls of the mode, if the internal loss contributions from the other constituent layers were minimized. This would then reduce the free carrier absorption in the n-GaN layer. On the other hand, from the perspective of current spreading, a higher n-GaN doping would be favored, so there is likely some optimal trade-off point which could potentially be predicted using simulations.

Moving to the MQW active region, we can compare (a) to (b) to gain further insight into the nature of SIMS analysis. In (a) the SIMS "number of cycles" was set to 500, while (b) used 384, resulting in (a) resolving the active region more precisely. In either case though, the true In compositions is likely ~10 %. The final layer of the active region is always a UID GaN barrier, equal to the thickness of the other GaN barriers. Thus the total

active region is composed of *n* QWs and *n + 1* barriers, with *n* being 5 for (a) and (b), but 7 for the most recent VCSELs. The details on the number of QWs in a VCSEL design are discussed in Section 3.4.1.

In both (a) and (b), the active region shows a Mg concentration of $\sim 10^{16}$ cm^{-3}, which is approximately an order of magnitude above the detection limit of the SIMS. Because no Mg is introduced to the system until the p-AlGaN layer is grown, the presence of Mg in the MQW suggests that there is always a finite amount of unintentionally incorporated Mg in the active region. The effect of this relatively small amount of Mg on device performance has not been analyzed in simulations and strong attempts at reducing the Mg contamination to below the SIMS detection limit have not been carried out, thus this is one potential area for improvement of the epitaxial layer, though it is difficult to quantify to what degree such Mg contamination would actually impact performance.

Beyond these near-detection limit levels of Mg in the MQW, we also see a significant amount of Mg present in the QWs nearest to the EBL. It is likely that much of this is simply a result of the tendency for SIMS to smear-out a layers interface, however if we compare the Mg profile directly to the right of the EBL in (a) and (b), we can realized that (a) shows a clear kink before the EBL, while (b) shows a smooth transition of the Mg concentration into the EBL. The difference in the profiles is a result of the p-AlGaN in (a) being grown with a Cp$_2$Mg flow of 30 sccm, while (b) used 12.5 sccm, which is equal to the Cp$_2$Mg flow in the p-GaN layer. The kink in the profile of (a) implies that a significant amount of Mg is back-diffusing into the MQWs, while (b) shows a typical smeared interface profile characteristic of SIMS. This back-diffusion of Mg was found to dramatically reduce the quality of the active region. It is discussed in detail in Section 3.4.2.

Moving to the p-GaN layer, we can note a number of differences between (a) and (b). First, the Mg profile to the left of the EBL is slopes downward for (a), while (b) shows an upward slope towards the surface of the sample. This is a result of the higher Cp_2Mg flow used in the EBL of (a), compared to (b). More specifically, this trend highlights the Mg memory effect, often observed in III-nitrides, where the MOCVD reactor is observed to retain high levels of Mg even after the Cp_2Mg flow is reduced.

Because the p-AlGaN layer and the p-GaN layer in (b) were grown at the same Cp_2Mg flow and temperature, we can also recognize another instance of an AlGaN layer showing higher levels of incorporation for other species in the reactor. This realization allows us to make the general claim that all n- or p-AlGaN layers grown under the same conditions as n- or p-GaN, will show higher dopant concentrations, even if the same SiH_4 or Cp_2Mg flow is used. It appears that using TMA for an AlGaN layer allows the incorporation of ~3X more Mg or Si, compared to a GaN layer, which is generally favorable for proper alignment of the Fermi-level for an EBL or hole-blocking layer (HBL).

The final layer of the MOCVD epi. structure is the 14 nm p^{++}GaN. In (a) we see all measured elements show a spike near the surface (i.e. at the p^{++}GaN layer). This is an artifact of the SIMS scan that always occurs at the surface of a sample. Thus, this particular scan does not show the p^{++}GaN properties. To resolve a surface layer, one must introduce a sacrificial surface layer which will allow the SIMS scan to stabilize before reaching the layer of interest. This is what is done in (b), where an n-GaN SIMS cap was introduced in order to allow the p^{++}GaN layer to be resolved. In (b) we can see the p^{++}GaN has a Mg concentration of 2×10^{21} cm^{-3}. This p-GaN layer was optimized during C. Holder's initial

work on nonpolar VCSELs and has not been modified since. Details on the optimizations can be found in Ref. [16].

Overall, if we compare the layers grown under the same conditions in (a) and (b), we note that (b) shows a much higher carbon contamination level. This is a result of (b) being grown later in the reactor maintenance cycle. The change in background level within a maintenance cycle highlights one of the commonly ignored issues in academic research on devices. Specifically, we do not have as much stringent control over what degree of variation we expect run to run in terms of active region quality, or the optoelectronic quality of each of the constituent epi. layers. This lack of control and predictive understanding of the degree of variation in the epi. quality is important to keep in mind when comparing different laser results, as small variation in performance, such as the J_{th} changing by one or two kA/cm^2, may simply be a result of variation in epi. quality.

Overall a VCSEL structure is more similar to LED than EELD, however a stricter control over the growth rates and thicknesses of each of the layers is required, due to the dependence of the cavity thickness on the cavity (Fabry-Perot) resonance wavelength, and the necessity to align specific layers in the cavity to the peaks and nulls of the mode (Section 1.4.5). It is also of note that the VCSEL does not require a thick p-GaN cladding layer, unlike EELDs, thus the p-GaN absorption does not necessarily dominate the internal loss in VCSEL, as it does in an EELD.

Since the thickness is very important to control in a VCSEL, it is especially important to discuss how one measures the thickness of a nonpolar VCSEL. In c-plane technology, when thickness needs to be controlled precisely, one can use reflectometry to measure the thickness in-situ. On m-plane, such laser-based reflectometry is very difficult

due to the extremely small nature of the substrates, which makes it difficult to have a laser continually focused on the substrate as it rotates. Naturally, engineering such an in-situ reflectometry system specifically designed for small substrates is not impossible, however a much simpler method for measuring thickness is to use XRD to calibrate the growth rates ex-situ. This is what is done for all nonpolar VCSELs, where we typically grew a set of XRD calibration samples two days before the VCSEL epi. is scheduled to be grown. Growing the XRD calibration samples as near to the actual VCSEL epi. growth day as possible minimizes the uncertainty in the true growth rate of the VCSEL epi.. Overall, general observations suggest that the growth rate does not vary dramatically within a maintenance cycle, but that growth rate does vary significantly from maintenance to maintenance.

Beyond the actual run-to-run growth rate variation leading to variations in thickness, it is also important to recognize that the growth rate varies across the sample itself, due to the non-uniform nature of the metal-organic (MO) gas flow around the sample. Figure 68 shows the variation in thickness near the center of a ~1 μm GaN template grown on a sapphire substrate. The thickness was measured ex-situ using a reflectometry-based
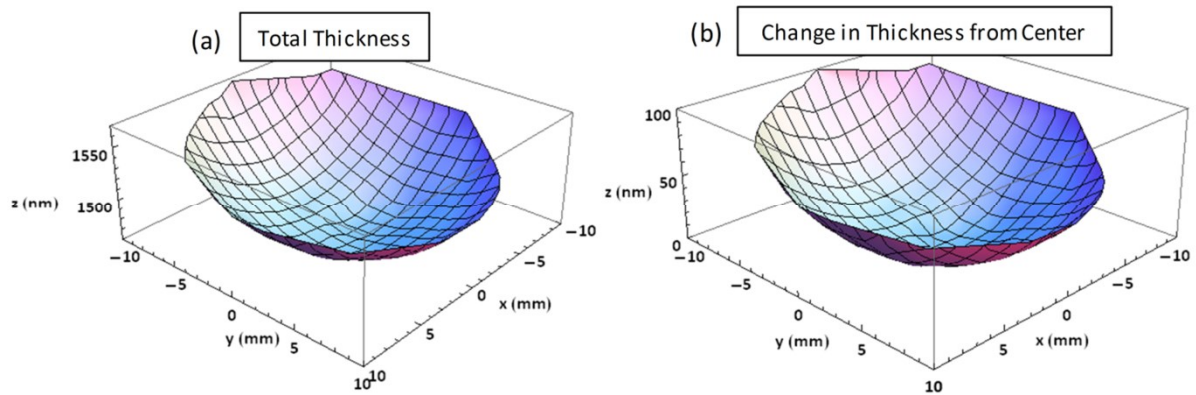
Figure 68 Ex-situ reflectometry based thickness map of a ~1 **μm** n-GaN template grown on sapphire. (a) shows the total thickness, while (b) shows the change in thickness from the center of the wafer. Over a 10 mm radius, the thickness is observed to vary by ≤ 100 nm.

thickness mapper. In Figure 68(b), we can see that over a ~10 mm radius, the thickness varies by ≤ 100 nm. This is a very significant variation, however it is difficult to quantify how this variation actually affects VCSEL performance at this stage, due to lack of statistically relevant LIV data. It is important to note though that such thickness variations have been investigated in other material systems, where one generally observes an increase in the threshold current for devices further from the center of the wafer. This occurs due to the misalignment of the peak gain wavelength and cavity resonance wavelength.[5] Naturally, these results are dependent on the uniformity of growth in a specific reactor, and so such thickness variations are not an intrinsic challenge to III-nitride VCSELs, however it would be illuminating for the field in general if an investigation was carried out analyzing the degree to which thickness non-uniformity affected threshold current density.

The sections to follow will cover the specific experimental and simulation results relevant to the epitaxial design of nonpolar VCSELs. For additional details on general MOCVD growth, please refer to Ref. [238].

3.3.1. PEC Etching

Typically, c-plane oriented flip-chip devices achieve substrate removal using laser lift-off and/or chemical-mechanical polishing (CMP).[171–173,239–246] For the case of VCSELs, such CMP processes can make cavity thickness control difficult, resulting in a misalignment of the cavity resonance wavelength and peak gain wavelength. Beyond the uniformity issues, laser lift-off can also introduce a significant degree of damage to the crystal, which has the potential to increase the contact resistance on the n-side of the device.

One of the primary advantages of m-plane is its suitability for substrate removal via PEC undercut etching. This method of substrate removal is of interest because it is a band-gap selective etching technique that allows one to epitaxially define the point at which the substrate will be removed from the flip-chip bonded epitaxial stack, giving epitaxially defined cavity-length control. The photochemical nature of PEC etching implies it is a low-damage etching technique, which is important to prevent damage-induced increases in the n^{++}GaN contact resistance. Additionally, the non-destructive nature of PEC undercut etching offers the potential for substrate recycling, which could significantly reduce the cost of devices grown on nonpolar and semipolar bulk GaN substrates.

3.3.1.1. PEC Undercut Etch

Figure 69 shows a summary of some of the early work on investigating the PEC undercut etch for the nonpolar VCSEL.[8] In Figure 69(a), we see a schematic of the VCSEL structure following the flip-chip bond to a sapphire submount and prior to the PEC undercut substrate removal step (Step (10) in Figure 60). Here, the PEC undercut etch of the sacrificial MQW (3QW, A7 nm, B5nm, $\lambda \approx 415$ nm) was achieved in a 0.1 M KOH solution under illumination with a 405 nm CW laser with an output power of ~200 mW (~65 mW/cm^2), purchased from DTR's laser shop.[247] This illumination source provides above-bandgap illumination, thereby generating electrons and holes in the sacrificial MQW. The photogenerated electrons are eliminated by a reduction reaction at the Ti/Au cathode on the m-plane GaN substrate (Figure 69(a)), where they replenish the KOH electrolyte. The photogenerated holes diffuse to the mesa edge of the sacrificial MQW where they assisted in the oxidation of Ga atoms.[248,249] This oxide is then dissolved in the electrolyte solution,
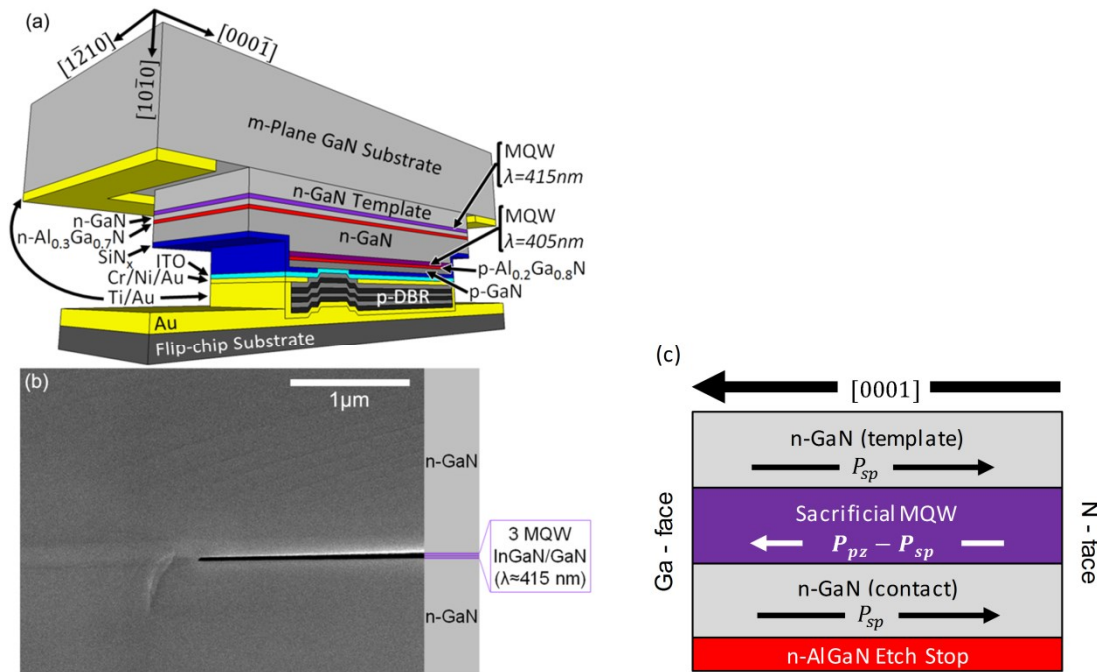
Figure 69 (a) Schematic of a nonpolar VCSEL following flip-chip bond and prior to substrate removal. (b) SEM micrograph demonstrating the highly precise nature of the bandgap selective PEC undercut etching technique. (c) Schematic of the m-plane epitaxial layers near the sacrificial MQW. The direction of the built-in polarization fields (i.e. the spontaneous polarization, P_{sp}, and the piezoelectric polarization, P_{pz}) are shown, along with the Ga-face and N-face on each edge of the structure. The piezoelectric polarization in the sacrificial MQW causes holes to be pushed to the Ga-face, leading to the Ga-face of the MQW etching faster than the N-face.[250]

leading to a lateral undercut etch.[248–251] It is important to recognize that covering the side-walls of the active MQW with dielectric (SiN$_x$) is critical in this step, as the active MQW would likely still absorb a significant amount of light from the illumination source and would thus etch if it were expose to the KOH solution.

Viewing the SEM micrograph in Figure 69(b), we can easily see the highly precise nature of the PEC undercut etch of the sacrificial MQW. The light region above the sacrificial MQW is due to charge build-up during the imaging. Although PEC undercut etching can be achieved on c-plane, it is generally not as precise as we observe it to be on m-plane. This is a result of the built-in polarization fields lying perpendicular to the direction of growth on m-plane, as is shown in Figure 69(c). Generally, the spontaneous polarization in a III-nitride layer results in holes being swept to the N-face, causing the N-face to etch

faster than the Ga-face. However, in the case of a MQW, the strain-induced piezoelectric polarization parallel to the plane of the sacrificial MQWs (Figure 69(c)) sweeps holes to the (0001) face (Ga-face), causing the Ga-face to etch faster than the (000$\bar{1}$) face (N-face).[250] In our initial work on nonpolar VCSELs,[8,14,15] the VCSEL aperture was positioned nearest to the Ga-face to ensure that complete etching occurred in the aperture region, as is shown in the schematic in Figure 69(a), however we have since realized that the completeness of the PEC undercut etch is more of a chip-level effect, rather than a device-to-device effect. More specifically, on a chip with many rows of bonded devices, the PEC undercut etch appears to completely undercut on the outer-most devices on the chip, before moving in towards the devices at the center of the chip, as is discussed in more detail next.

Following this initial investigation of the PEC undercut etch, we sought to gain more insight into the effect of the KOH concentration on etch rate and surface roughness. This was motivated by two questions: (1) could the VCSEL process be simplified by eliminating the top-down PEC etch, if the PEC undercut etch alone gave a highly smooth morphology, and (2) what is the minimum undercut etch time necessary for substrate removal. Question (2) was primarily motivated by the fact that our original samples were simply submerged in the 1 M KOH solution and illuminated overnight (>8 hrs.), which can significantly increase the total processing time, especially when many samples are processed in parallel and all cannot be undercut etched simultaneously (due to the small beam size of the illuminating 405 nm LD). To investigate the PEC undercut etch further, we processed a set of samples up to Step (9) in Figure 60, then cleaved the samples into ~3 mm × 6 mm pieces and carried out the Au-Au flip-chip bond. Each sample was then submerged in various cocentrations of KOH, illuminated with the 405 nm LD, and the undercut etch time was monitored by

viewing the samples through safety glasses with 405 nm long-pass filters integrated into the glasses. These glasses allow one to observe the PL from the sacrificial MQWs, emitting at ~415-420 nm, thereby allowing the visual observation of the chip-level PEC undercut etch progress. Using this method we observed that the PEC undercut etch did not proceed to undercut each sample on the substrate at the same time. Rather, the etch appeared to preferentially occur on the outermost devices of the chip, before gradually moving in towards the center of the chip. This suggests that the KOH solution does not uniformly diffuse through the entire grid structure of the samples when they are submerged. This could be a result of air being trapped in the sample, or perhaps capillary forces. Overall though, this effect implies that the measured undercut etch time actually depends on the size of the substrate.

Figure 70 shows the results of this PEC undercut etch study. Observing Figure 70(a), we see that the sample undercut in 1 M KOH completely undercut in ~2 hrs.. This is significantly shorter than the ~8-10 hr. etch time being used previously. Here the chips were ~1/4 the size of a full m-plane substrate, while most processed VCSELs were fabricated on half-substrates. Consistent with the observation of the chip-level PEC undercut etch propagation, VCSELs fabricated on half-substrates generally showed an undercut etch time of ~4hrs, as the chips were ~2X larger than those used in this study. As the KOH concentration was reduce from 1M to 0.1M, the surface roughness was reduced from ~10 nm RMS to ~1 nm RMS. This highlights the fact that m-plane does indeed show some degree of purely chemical-related roughening, which is commonly observed on the N-face of c-plane GaN, though the degree of the roughening is much less severe than is observed on c-plane. The roughness is observed to linearly decrease with decreasing KOH concentration,
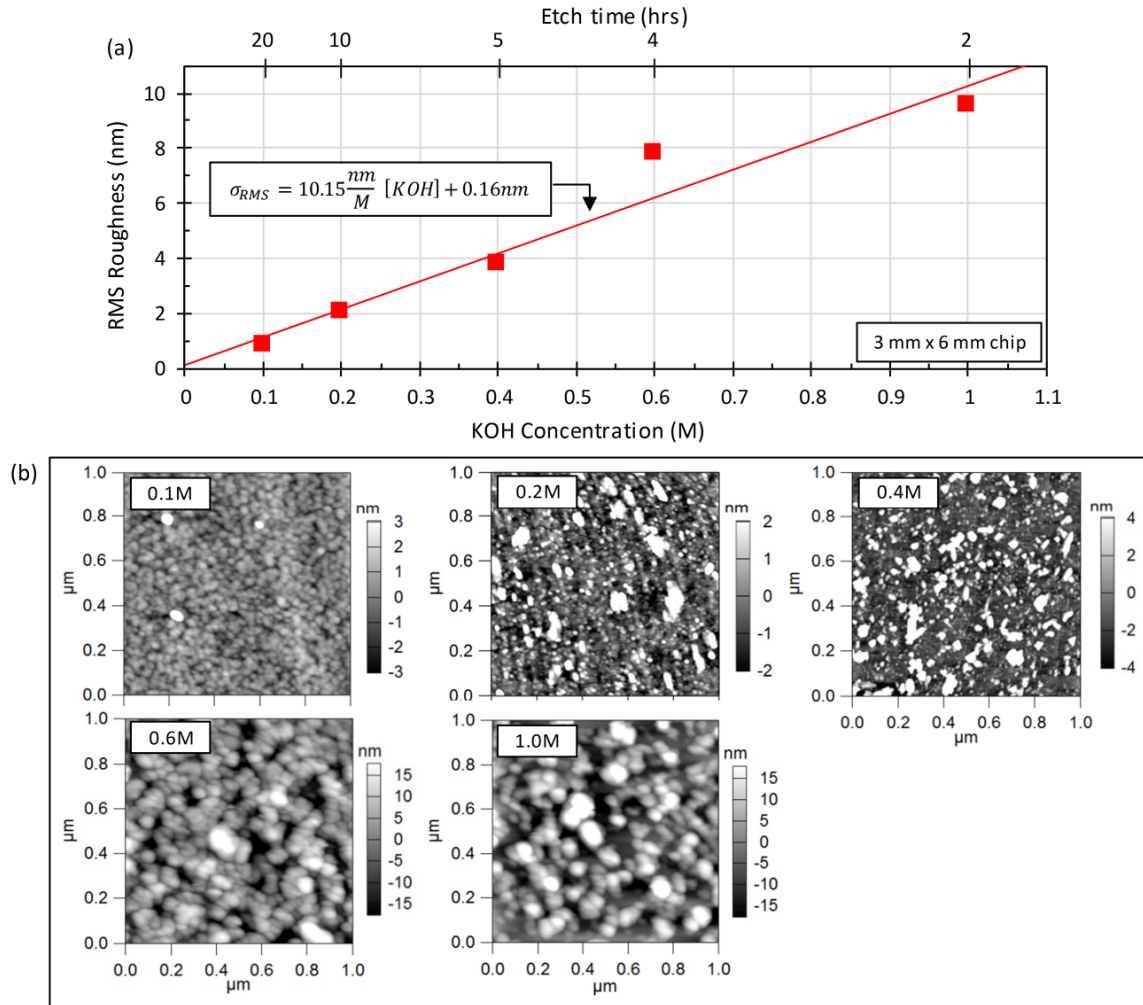
Figure 70 Analysis of PEC undercut etch vs. KOH concentration. (a) shows the RMS roughness vs. KOH concentration and total etch time. Each sample was a partially processed VCSEL on a half-substrate chip (~3 mm × 6 mm m-plane substrate). The total etch time is defined as the time required to lift-off the native m-plane GaN substrate from the flip-chip bonded samples. Generally, the total etch time is osbserved to depend on the chip size, with half-substrate chips (~7 mm × 6 mm) typically taking ~4 hrs to undercut in 1 M KOH, compared to the 2 hr etch time observed here. The RMS roughness was measured via AFM on the flip-chip bonded sample's exposed n[++]GaN surface (Step (11), Figure 60). (b) shows the corresponding AFM micrographs for each of the measured data points in (a).

with a slope of ~10.15 nm RMS roughness per mole KOH in solution. As the 0.1 M surface roughness is on the order of the epitaxial roughness (Figure 65), it is likely that this KOH concentration results in a minimal degree of purely chemical related etching. The corresponding AFM images for each of the surface roughness values in Figure 70(a) can be seen in (b). The highly smooth nature of the 0.1 M undercut suggests that the VCSEL process can indeed be simplified by eliminating the top-down etch. Such a VCSEL was
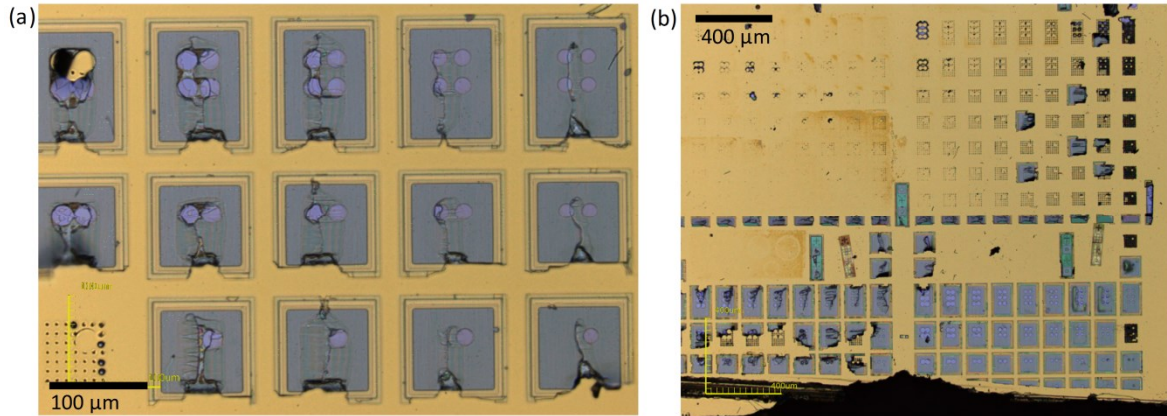
Figure 71 High magnification (a) and low magnification (b) optical microscope images of a VCSEL structure after ~ 40 hrs of undercut etching in a 0.1 M KOH solution with illumination via a 405 nm LD. Many of the samples are observed to show either incomplete undercuts are did not undercut at all, preventing them from being bonded to the Ti/Au coated sapphire submount.

demonstrated in Ref. [10]. However, there are a number of issues with using the 0.1 M KOH

concentration for an undercut etch. First, observing Figure 70(a), we can see that this ¼-

substrate chip took ~20 hrs. to undercut. On the half-substrate chip, from which the device

demonstrated in Ref. [10] came, the etch did not complete even after ~40 hrs. Figure 71 shows

optical microscope images from one such sample, where we can see many of the mesas did

not completely undercut, while some did not undercut at all, preventing them from being

bonded to the Ti/Au coated sapphire submount. While many of the devices failed, the large

number of VCSELs on a chip still allowed many to make it through the process for future

characterization. In general, the degree to which the 0.1 M undercut etch was unsuccessful

varied from sample to sample, but the general conclusion was that using a 1 M undercut

etch, along with a PEC top-down etch, is critical for maximizing the yield of the VCSEL

process. The most recent nonpolar VCSELs have thus used 1 M undercut etches, where a

complete undercut is typically achieved in ~4 hrs. for half-substrate chips (7 mm × 6 mm).

On a related, but less critical note, we should also mention that we have switched

from using the 405 nm LD illumination source to using a 405 nm LED array, purchased

from Weili Optical (Link to Weili Optical Website). It should be noted that the power stated

in the product name is the input power, not the output power of the device. As can be seen, these LED arrays have very high input powers, thus one needs to attach a heat sink to the backplane of the array. We use a ~4 in × 4 in extruded aluminum heatsink from Heatsink USA ([Link to Heatsink USA Website](#)), with thermal paste between the LED array and heatsink to improve heat transfer. The power density of the LED array is was tuned to be approximately equal to that of the LD (~65 mW/cm^2), however the primary advantage of using an LED array is that one can more easily illuminate multiple samples at the same time due to the much larger illumination area of the LED array, compared to the LD. Since we typically process 6-12 chips simultaneously, using such an LED array greatly reduced the total processing time.

We should also note this PEC undercut etch method is potentially applicable to c-plane oriented devices as well. c-plane PEC etching of GaN was first demonstrated by Minsky, et al..[248] In general, etching c-plane oriented III-nitride films often results in rough surfaces with hexagonal pyramidal morphology, particularly on the N-face, which could lead to a significant amount of scattering loss in the case of VCSELs.[252–255] However, a number of groups have achieved fairly smooth surface morphologies,[256–258] suggesting that this substrate removal process could also be used to fabricate c-plane flip-chip VCSELs with the proper optimization.

3.3.1.2. PEC Top-Down Etch

Following the substrate removal via the PEC undercut etch, the n-contact is deposited on the exposed n^{++}GaN surface of the sample (Step (12), Figure 60). This contact not only serves as the n-contact for the device, but also serves as the PEC cathode for the

PEC top-down etch in the following step. As was mentioned previously, a number of VCSELs were successfully fabricated without the PEC top-down etch, and without the n-AlGaN etch-stop in place, however, our earliest demonstrations,[8,14,15] and our latest devices,[11–13] all used the PEC top-down etch process.

A PEC top-down etch process is carried out by submerging the VCSEL in a 0.001 M KOH solution and illuminating with a Hg-Xe arc lamp with a long-pass filter in front of the arc-lamp beam. The essential requirement for the long pass filter is that it must allow light to pass if it has a higher energy than the bandgap of the layer to be removed (i.e. the GaN layer), while stopping light that has an energy great than the stop-etch layer (i.e. the n-AlGaN layer). The Hg-Xe arc lamp itself is a high power density, broad-band source emitting deep into the IR and UV (below 250 nm). To etch the n^{++}GaN ($E_g \approx 3.45$eV) layer in the aperture, an illumination wavelength below ~360 nm is necessary. However, to stop the etch on the n-AlGaN stop-etch layer, the long-pass filter is necessary. The necessary cut-off wavelength of the long-pass filter depends on the composition of the n-AlGaN layer. Typically an n-AlGaN composition of 30-40% was used. $Al_{0.3}Ga_{0.7}N$ has a bandgap of ~3.98 eV, corresponding to a wavelength of ~311 nm, thus any bandpass filter with a cut-off wavelength greater than ~311 nm should theoretically be acceptable for an n-AlGaN layer with a composition of >30% Al. However, long-pass, or band-pass, filters typically do not have a perfect cut-off at the cut-off wavelength, thus it is generally better to separate the band-pass filter cut-off wavelength from the n-AlGaN bandgap wavelength as much as possible. Therefore, more recent devices have switched from using an n-$Al_{0.3}Ga_{0.7}N$ etch-stop with a 320 nm long-pass filter, to using an n-$Al_{0.4}Ga_{0.6}N$ etch-stop with a 345 nm long-pass filter.

In our early investigations of the top-down etch, a test sample was grown with a 15 nm n-$Al_{0.3}Ga_{0.7}N$ layer surrounded by two n-GaN layers. This sample was immersed in 0.001 M KOH and illuminated with the Hg-Xe arc lamp and a 320 nm long-pass filter. Figure 72(a)[8] shows the etch depth vs. etch time, where the etch depth was measured via profilometry. Here, we see that once the etch reached the n-$Al_{0.3}Ga_{0.7}N$ layer it was stopped for ~125 minutes, which corresponded to an n-$Al_{0.3}Ga_{0.7}N$ etch rate of 0.12 nm/min. Comparing this to the n-GaN etch rate of 30.7 nm/min, yields an n-GaN: n-$Al_{0.3}Ga_{0.7}N$ etch selectivity of 255:1. Because AlN is more sensitive to purely chemical etching the GaN, it is likely that the n-AlGaN etching is predominantly a result of purely chemical etching. In Figure 72(b)[8], we see a 10 μm x 10 μm AFM image of the surface of an n-$Al_{0.3}Ga_{0.7}N$ layer after the completion of the PEC top-down etch but before the n-AlGaN was broken through. This image demonstrates the effectiveness of this etch in producing surface roughness's on the order of the epitaxial surface roughness (Figure 65).

Following the completion of this investigation on a test sample, we sought to analyze the surface roughness on a complete VCSEL structure. Prior to characterizing the surface roughness of the top-down etch, we first analyzed the surface morphology of the exposed n^{++}GaN surface after the PEC undercut etch. Figure 72(c) shows the surface roughness of a partially processed VCSEL after the PEC undercut etch in a 0.1 M KOH solution with a 405 nm LD illumination source. In the top image, we see the surface morphology measured on the mesa in the area outside the aperture of the device, while the bottom image shows the AFM image taken inside the aperture. Here, we can see a significant difference in the morphology of the surface inside the aperture vs. outside the aperture. This is likely a result of the area inside the aperture having the p-DBR on the back-side of the device, whereas the
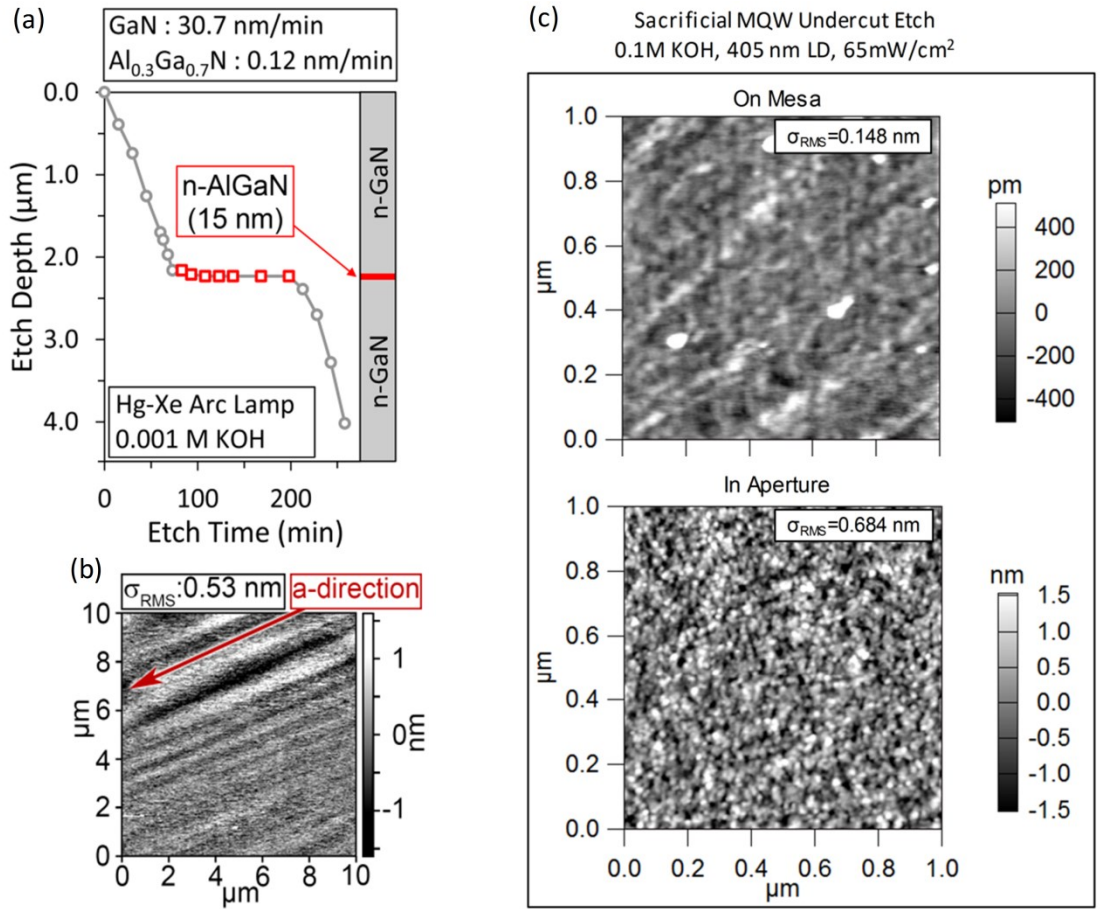
Figure 72 (a) Etch depth vs. etch time measured via profilometry on a test sample with an n-GaN/n-Al$_{0.3}$Ga$_{0.7}$N/n-GaN stack. The sample was etched in 0.001 M KOH under a Hg-Xe arc lamp illumination source, with a 320 nm long-pass filter.[8] The etch is observed to stop on the n-AlGaN layer, until purely chemical etching results in the n-AlGaN layer failing and the PEC etch continuing through the n-GaN layer. (b) shows an AFM image of a test sample after the etch has stopped on the n-AlGaN etch-stop layer. The RMS roughness is on the order of the epitaxial roughness. (c) shows the surface (n^{++}GaN layer) of a VCSEL mesa after it was undercut etched in 0.1 M KOH with a 405 nm LD. The top AFM image was taken on the area of the mesa outside the aperture, while the bottom image was taken on the area of the mesa inside the aperture. We see that the area outside the aperture shows a significantly different morphology than the area inside the aperture, which may be a result of the area inside the aperture having the p-DBR below the illuminated area, while the area outside the aperture has a Ti/Au layer below the illuminated area.

area outside the aperture had a Ti/Au layer before the p-DBR support structure. This Ti/Au layer between the intracavity contact and the p-DBR support structure was used in older designs, however it has now been removed as one can achieve a higher alignment tolerance between the aperture and the p-DBR by eliminating this Ti/Au layer and simply making a metal contact to the intracavity contact using the Ti/Au p-DBR conformal coating layer. Overall though, it is significant to note that the fact that the illuminating light can interact

with the p-DBR on the back-side of the device, rather than simply being absorbed in a Ti/Au contact, appears to lead to a slight increase in the surface roughness of the PEC etched area inside the aperture. This increase is significant, but not catastrophic, though it does imply that one should always characterize the surface roughness within the aperture of the device, which is actually what was done in Figure 70, and was done in the following analysis of the top-down etch.

With this in mind we went on to characterize the surface morphology in the aperture as the top-down etch proceeded through the n^{++}GaN layer to the n-AlGaN etch-stop. As was discussed in the previous section, the surface morphology at the start of the PEC top-down etch depends on the conditions used for the PEC undercut etch. Here, we chose to analyze the two extremes of the top-down etch after an undercut etch in 0.1 M and 1 M KOH. The corresponding AFM images vs. etch time are shown in Figure 73. In Figure 73(a), we see the surface roughness simply stays on the order of the epitaxial roughness, produced by the PEC undercut etch in 0.1M KOH, until the top-down etch breaks through the n-AlGaN layer, leading to an increase in the RMS roughness from ~0.6 nm to ~5 nm. Viewing the sample under an optical microscope (Figure 73(a)), the n-AlGaN stop-etch failure is quite visible. Here, it is of note that the n-AlGaN layer failed faster than it did in the test sample analyzed in Figure 72(a). This may be related to the difference in etching characteristics when the p-DBR is present on the back-side of the device. This p-DBR may lead to some kind of resonant effect that could locally increase the etch rate in that area. Figure 73(b) shows the case of the top-down etch following an undercut etch in 1 M KOH. Here, after 1 min of etching, the surface roughness is observed to increase from ~5 nm to ~9 nm RMS. Following this, the roughness decreases to ~3 nm at 3 mins of etch, then to ~1 nm after 5
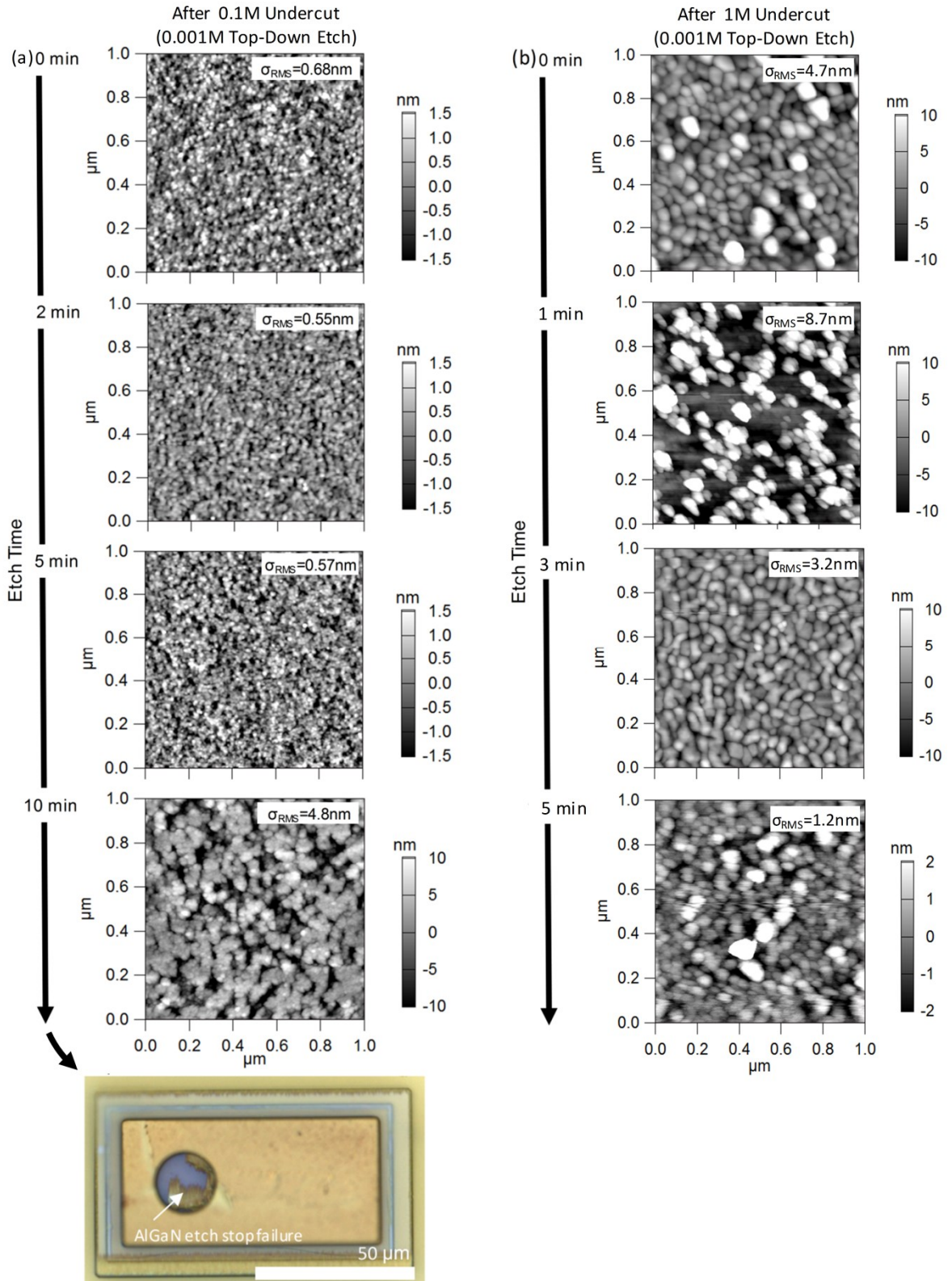
Figure 73 AFM measurements of the surface inside the aperture of a partially processed VCSEL at various times in the PEC top-down etch process. (a) shows the case where the undercut etch was perfomed in 0.1M KOH, while (b) shows the case where the undercut etch was performed in 1M KOH. Both samples used a KOH concentration of 0.001M for the top-down etch.

mins of etching. The fact that the roughness initially increased, then began to decrease towards 1 nm, suggests that the etch rate of the n^{++}GaN layer may vary locally, leading to some areas of the n^{++}GaN layer being completely etched away to the n-AlGaN etch stop, before other areas are completely etched. Overall, this more rigorous analysis led us to use a 5 min top-down etch in the later generations of VCSELs.

In summary, the PEC undercut etch and top-down etch processes display some interesting non-intuitive etching trends, however overall these steps are fairly well optimized for the nonpolar VCSELs. Further reductions in the undercut etch time, could potentially be achieved by varying the sacrificial MQW barrier width, QW width, and number of QWs, as PEC etching efficiency generally depends on these parameters. However, these concerns are rather tangential to the VCSEL process as a whole.

3.4. Active Region Design

With a thorough understanding of the performance and purpose of the sacrificial MWQ and n-AlGaN etch stop layer, we are now ready to consider the active region design for a VCSEL and its implications on device performance. For designing the active region of a VCSEL, one must take into account 3 key parameters: (1) the overlap of the gain with the QWs (i.e. the enhancement factor), (2) the gain vs. current characteristics for a given number of QWs, and (3) the carrier injection efficiency/uniformity of injection for a given number of QWs. In general, consideration (1) implies that for a design with a high number of QWs, one must minimize the total thickness of the QW stack in order to maximize the overlap between the peak intensity of the mode and each layer of the QWs. This is fundamentally why our most recent VCSEL designs use very thin (1 nm) barriers, and

relatively thin (3 nm) QWs for the devices with 7 to 10 QWs. Yet, it is of note that if the barrier width is too small, carriers may not be efficiently confined, leading to a reduction in the radiative recombination efficiency and gain per well. Consideration (2) is arguably the most important to understand, as it is the strongest guide in deciding what number of QWs is ideal for minimizing the threshold current density for a design with a given threshold modal gain. This will be discussed in detail in the next section. Consideration (3) is important to keep in mind because if one uses a very large number of QWs, it is quite possible that carriers will not be injected uniformly into each QW, which can lead to one or more of the QWs simply acting as an absorbing layer, adding to the internal loss in the cavity. This consideration requires a charge transport analysis, which can be carried out using SiLENSe, however there has been a great deal of debate over whether or not SiLENSe's drift diffusion model correctly models carrier transport, so we have not investigated this particular consideration in detail here. Regardless, as will be seen in the next section, minimizing the threshold modal gain will allow one to minimize the number of QWs necessary to achieve a minimal threshold current density. Minimizing the number of QWs would thus minimize the probability that one or more of the wells is not contributing to the gain in the cavity. Minimizing the barrier thickness may also improve the injection uniformity in each of the QWs. The effect of absorbing QWs on c-plane VCSEL performance has been analyzed in Ref. [259], as a motivation for using a tunnel-junction in a cascade MQW VCSEL design, however a similar analysis for an m-plane VCSEL has not been reported. Given that the carrier transport mechanisms are significantly different on c-plane vs. m-plane it is difficult to simply extrapolate c-plane simulation results to m-plane.

3.4.1. Number of QWs

The optimal number of QWs in any laser depends on the threshold modal gain (i.e. total loss) for the particular laser.[3,260–262] This is fundamentally a result of the slope of the gain vs. current curve, for some number of QWs, increasing with an increasing number of QWs, while the transparency current density (i.e the x-intercept of a gain vs. current plot) increases as well. Thus, in order to determine the optimal number of QWs for a given laser, one must first know the gain vs. current trends for a particular QW design. This can be simulated experimentally using software such as SiLENSe, however it is probably more accurate to rely on experimentally measured values. To experimentally measure the gain vs. current trends, one must extract the internal parameters for an EELD using the length-dependent analysis.[3,146,155,263] Because the cavity length of a VCSEL cannot be easily modified on the same chip, this type of analysis is only easily feasible in an EELD. In GaAs-based and InP-based VCSELs research, researchers have fabricated EELDs with similar active regions to that used in a VCSEL, extracted the internal parameters from the EELD, then used the gain vs. current data from the EELD to determine the optimal number of QWs for a given VCSEL design. In the nitrides, particularly m-plane, this type of analysis is difficult due to the inability to form cleaved laser facets on m-plane. This complicates the extraction of the internal parameters for the EELD, as the mirror reflectance then becomes more difficult to accurately predict due to roughness or a tilt of the facets. None the less, such an analysis has been carried out by Farrell et al. on a set of violet emitting m-plane EELDs.[146,155] Using this extracted gain vs. current data, along with our TMM calculated threshold modal gain data, we can achieve a more in-depth understanding of the correct

151

number of QWs for a given VCSEL design. Before going into detail on this analysis, It should be noted that our TMM simulations simply assume the QWs do not contribute any internal loss (i.e. the absorption coefficient in the QWs is equal to $-g_{th}$), which is not completely accurate, but, as always, we are more interested in relative comparison and general guiding principles from simulations, rather than the precision of the numbers themselves.

To approximate the modal gain vs. current density trends for the nonpolar VCSELs, we combined the $g(J)$ data from Ref. [155] with the confinement factor from TMM simulations of 405 nm VCSELs with ~7λ thick cavities and a QW number ranging from 1-10 QWs. Specifically, the modal gain equation used here is stated in Eqn. (7). For convenience we restate it here; the equation has the form $\Gamma g(J) \approx N_w \Gamma_1 g_0 \ln \left[\frac{J + J_s}{N_w J_{tr_1} + J_s} \right]$,[3,146] where N_w is the number of QWs, Γ_1 is the average confinement factor per well (approximated using the 1D TMM simulations), Γ is the total confinement factor, g_0 is the empirical gain coefficient,[155] J_{tr_1} is the transparency current density per well,[155] and J_s is a linearity parameter.[155] We assume the lateral confinement, Γ_{xy}, is equal to 1. Each active region has an A3 nm, B1 nm, EBL5 nm design. Figure 74(a) shows the modal gain vs. current density for ~7λ cavities with different numbers of QWs, overlaid with corresponding threshold modal gain value for ITO VCSELs with different numbers of QWs. Observing the trend in transparency current density, J_{tr} (i.e. the intersection with the x-axis), we see that as the number of QWs increases, the transparency current density increases. This is not surprising since more QWs would require more carriers to reach transparency. Along with the increase in transparency current density, we also see that the slope of the $\Gamma g(J)$ lines increases as the number of QWs increases. This implies that a higher number of QWs is more favorable for cavity designs
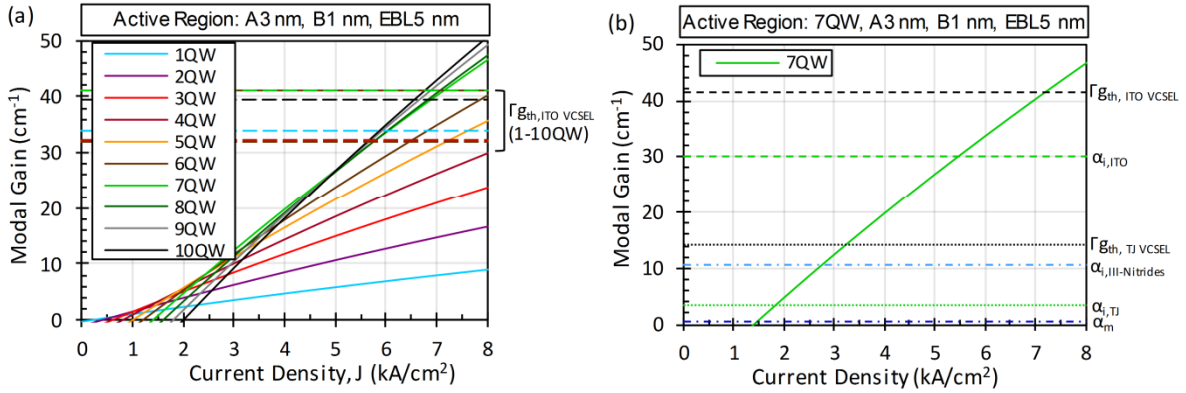
Figure 74 (a) modal gain vs. current density for various number of QWs with active region designs of A3 nm, B1 nm, and EBL5 nm. The confinement factor was calculated using the TMM for ~7λ VCSELs, while the *g(J)* is taken from the experimentally measured values for a violet emitting m-plane EELD.[155] The threshold modal gain, Γg$_{th}$, values (calculated using the TMM) for ~7λ ITO VCSEL designs with different numbers of QWs are shown by the dashed lines, where the color corresponds the number of QWs shown in the key. (b) The modal gain vs. current density for the case of the 7QW design shown in (a). The breakdown of the various sources of loss in a TJ VCSEL vs. an ITO VCSEL are shown as dashed lines. We note the significant reduction in threshold modal gain, and thus a reduction in threshold current density, by moving from an ITO intracavity contact to a TJ intracavity contact.[11]

with a large amount of loss, as it allows one to more easily achieve a low threshold current density. This is fundamentally why we switched from the 5QW design in our original devices,[8,14,15] to the 10QW,[10] then 7QW designs in the more recent reports.[11–13] More specifically, at the time of our early reports, we had very little insight into the fundamental issues in the VCSELs and we did not fully understand why they had such high threshold current densities (~100 kA/cm^2). Overall, there appeared to be some sort of anomalous source of loss in the cavity, which we later attributed to the scattering loss from the SiNx dielectric aperture design, based on the significant improvement in performance resulting from switching to the IIA design. At the time we were basically trying everything we could to try to improve the yield and reduce the threshold current of the devices and increasing the number of QWs appeared to be one of the more obvious design parameters that could allow us to more easily compensate for any anomalous sources of loss in the cavity.

Observing the changes in the threshold modal gain values for different numbers of QWs in TMM simulated ~7λ TJ VCSELs (Figure 74(a)), we can see that changing the

153

number of QWs does not have a very significant impact on the threshold modal gain, particularly in the case of an A3 nm, B1 nm design, since even for the 10QW design, all the QWs overlap with a significant portion of the electric field. Using designs with thicker active QW widths, or thicker barriers would likely lead to more significant changes in the threshold modal gain for different numbers of QWs. Furthermore, incorporating the contribution to the internal loss from absorption in the QWs would also likely lead to a more significant variation in threshold modal gain for different numbers of QWs.

In Figure 74(b), we see the modal gain vs. current density for the 7QW design shown in (a). To gain insight into the various sources of loss in a TJ VCSEL and ITO VCSEL, we have overlain the loss introduced by the DBRs (mirror loss, α_m), intracavity contact ($\alpha_{i,ITO}$ and $\alpha_{i,TJ}$), all other III-nitride layers ($\alpha_{i,\text{III-Nitrides}}$), and the threshold modal gain (Γg_{th}) for each ~7λ design. Comparing the Γg_{th} values for the ITO VCSEL to the TJ VCSEL, we see that using the TJ instead of ITO results in the Γg_{th} being reduced from ~41.6 cm^{-1} to ~14.1 cm^{-1}. Considering the breakdown of the various sources of loss, we see that for the ITO VCSEL the internal loss from the ITO is ~20 cm^{-1} higher than the internal loss from the III-nitride layers. This implies the ITO intracavity contact contributes to ~74 % of the total internal loss. In contrast, the internal loss from the TJ is lower than the internal loss from all other III-nitride layers. Thus, the use of a TJ not only allows us to reduce the threshold current density for a VCSEL with an arbitrary number of QWs, but it also moves us into a regime where there may be a different optimal number of QWs for minimizing the threshold current density, compared to an ITO VCSEL. Reducing the number of QWs is advantageous because, as mentioned previously, increasing the number of QWs implies one must decrease the QW and barrier width in order to achieve a higher enhancement factor. Therefore, a

smaller number of QWs gives one more room to vary the barrier and QW width to optimize the performance. Furthermore, reducing the number of QWs decreases the chance of some poorly populated QWs lead to absorption loss in the device.[259] Finally, for long wavelength III-nitride VCSELs ($\geq$ 450 nm), a lower number of QWs can reduce the likelihood of growth issues, such as relaxation, associated with highly strained InGaN QWs.[264] Overall, these results not only highlight another advantage of using a TJ intracavity contact, but they also highlight the fact that the optimal number of QWs can change depending on the level of loss (threshold modal gain) in the cavity. Indeed, in many GaAs-based EELDs, using a single QW is optimal due to the significantly lower loss levels.[265–267] It should also be noted that in the TJ design, the loss in the cavity is no longer dominated by the loss in the intracavity contact, thus future efforts in minimizing the threshold current density should probably focus on minimizing the other III-nitride layers, possibly by using a step-function doping profile, similar to that used in GaAs-based epitaxial DBRs (Section 1.3.1, Figure 19(a)). However, presently the biggest challenge for efficient nonpolar VCSELs is not the threshold current density, as the initial demonstrations of a TJ VCSEL yielded devices with ~3.5 kA/cm^2,[11] rather it is (1) achieving CW operation, and (2) achieving proper LP mode lasing (i.e. eliminating filamentation) with a robust aperture design.

It is important to mention that our initial investigations of the *g(J)* performance (not shown) for nonpolar VCSELs were carried out using SiLENSe. Overall, the SiLENSe model predicted much steeper gain vs. current density curves and higher transparency current densities, than the experimentally extrapolated *g(J)* data shows. It is difficult to say whether the SiLENSe model is more or less accurate than the experimentally measured data, as Ref. [155] is the only report of experimentally measured internal parameters for nonpolar violet

EELDs, and there may be some variation of the active regions material gain, due to variation in the epi-quality. Yet, the SiLENSe simulations can be useful none-the less as they can be used to investigate the relative effect of the QW and barrier width. To do this, one must have the model give reasonable voltage values. Many of reported that SiLENSe gives a voltage much higher than that of experimentally measured devices. In our simulations, we discovered that using a parabolically graded active region mitigated these unrealistically high voltage results. The study of this effect was reported in Ref. 220. Overall, such a parabolic grading does not seem to be too far from the actual physics distribution of In in III-nitride QWs generally.[218–223] Furthermore, using the quantum potential model (added to version 5.0 of SiLENSe), appeared to further improve the agreement between measured IV curves and modeled IV characteristics. This is not surprising, as the quantum potential model was added in order to account for quantum effects, such as tunneling and quantum confinement of carriers. Additional details on SiLENSe simulations can be found in Refs. [268–270]. Furthermore, we recommend those interested in using SiLENSe read the manuals before building a model, as there are many subtle details and assumptions that the software makes, which are important to be aware of.[270–272]

Beyond these simulation-based analyses of the number of QWs, we also performed some very rudimentary measurements on the unprocessed epi. using the "quicktest" method. This "quicktest method simply involves soldering indium dots onto the top and bottom of the sample, following growth and activation, and performing an EL measurement at 20 mA. Overall, there was never any significant trend observed by changing the number of QWs or changing the QW thickness. We also did some initial testing of InGaN/InGaN QW/barriers designs, but no significant change in LIV performance was observed here either. Overall,

after we solved the Mg-diffusion into the MQW issue, discussed in Section 3.4.2, the violet m-plane epi. was typically yielding some of the highest quicktest powers observed at UCSB for semipolar and nonpolar samples. This implies that any future experimental investigations into the number of QWs, barrier width, QW width, or other active region design parameters, should probably be performed on complete VCSEL structures.

3.4.2. Electron Blocking Layer (EBL)

In general, the EBL has much more significant effects on device performance for c-plane emitters compared to semipolar and nonpolar devices. This is a result of the built-in polarization fields present in the c-direction, leading to significant band bending in each of the layers, which changes much of the nature of the charge transport on c-plane compared to m-plane.[274–277] For c-plane VCSELs, both theoretical[274] and experimental[277] results have shown the strong dependence of lasing performance on EBL design. A study of the effect of EBL design on nonpolar VCSEL performance has not been carried out, however we did perform a number of SiLENSe simulations which essentially suggested that moving from a 15 nm EBL, used in our early demonstrations,[8,14,15] to a 5 nm EBL could improve the injection uniformity for designs with a large number of QWs (> 5QWs). This led us to use a 5 nm EBL in more recent reports,[10–13] however a more rigorous series should be carried out on full VCSEL structures to experimentally analyze the effect of EBL composition and thickness on nonpolar VCSEL performance. Another important point to keep in mind in designing the EBL is the emission wavelength of the device, as devices with longer emission wavelengths (i.e. blue/green) will have deeper QWs (i.e. a larger separation between the conduction band of the GaN barrier and the conduction band of the InGaN active region),

157

leading to stronger confinement of carriers. This then implies that the optimal EBL design also depends on the emission wavelength of the device, as well as the number of QWs in the device.

Beyond these more obvious variations in the EBL design, investigations into optimizing the epitaxial layers performed following the reports in Ref. [8,14,15], did reveal a non-intuitive issue with our EBL. Specifically, following the SIMS analysis shown in Figure 67(a) we realized that there was an unusual kink in the Mg-concentration at the interface of the EBL and the active regions. As mentioned previously, SIMS does not resolve thin layers and interfaces very well, but what makes this interface particularly of note is that the SIMS measured Mg profile does not display the characteristic "tail" typically observed at an interface, but rather shows a kink or bump in the Mg profile at the EBL/MQW interface. This suggests that there was some degree of Mg diffusing back into the QWs. To investigate this effect we grew a series of samples with Cp_2Mg flows in the EBL ranging from 30 sccm (to original Cp_2Mg flow in the EBL), to 0 sccm and analyzed the active region quality using the quicktest method (soldered indium dots on bare epi.). The output power, voltage, FWHM, and peak wavelength measured at 20 mA (~20 A/cm^2) for various samples, with various Cp_2Mg flows in the EBL, is shown in Figure 75. It should be noted that this epi. structure did not actually have the sacrificial MQW in place, as it can convolute the analysis of the active region quality due to the photopumping of the sacrificial MQW ($\lambda \approx 420$ nm) from the active MQW ($\lambda \approx 405$ nm). Originally, C. Holder used 30 sccm Cp_2Mg flow in the EBL because it was ~3× higher than the Cp_2Mg flow in the p-GaN (12.5 sccm), and thus one would expect the Mg doping to be ~3× higher. However, as was mentioned in Section 3.3, growing in the presence of TMA leads to an ~3× increase in impurity and dopant
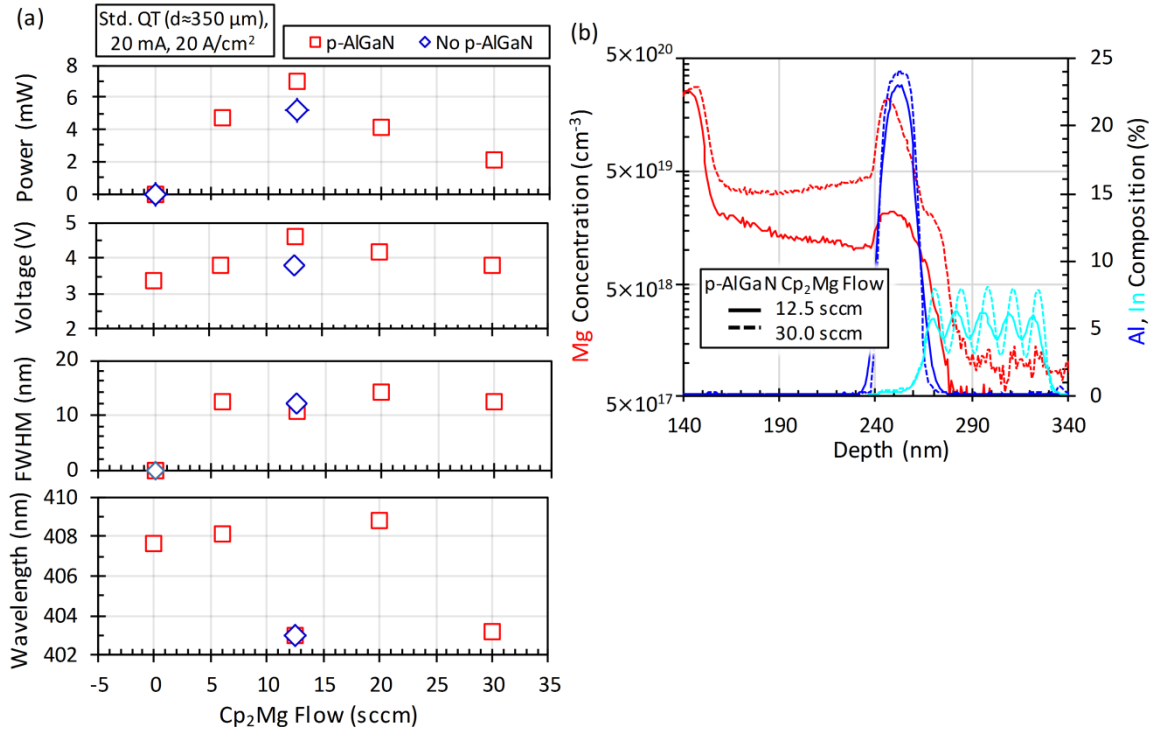
Figure 75 (a) quicktest (soldered indium dot) measurements on VCSEL epi. (with the sacrificial MQW removed) with the EBL grown under various Cp_2Mg flow conditions. 30 sccm corresponds to the original Cp_2Mg flow used in the VCSELs reported in Ref. 8,14,15. The optimal Cp_2Mg flow corresponds to 12.5 sccm, which is equal to the Cp_2Mg flow used in the p-GaN layer. (b) shows the SIMS measured profiles for the structure grown with 30 sccm and 12.5 sccm Cp2Mg flow in the EBL. The 30 sccm Cp_2Mg flow shows the same abnormal kink in the SIMS tail as is observed in Figure 67(a), while the 12.5 sccm sample shows a normal SIMS tail at the EBL/MQW interface, suggesting that no significant diffusion of Mg into the MQW has occurred.

incorporation efficiency (i.e. concentration), compared to just growing a GaN layer. Observing Figure 75, we can see that as the Cp_2Mg flow was reduced from 30 sccm to 12.5 sccm, the quicktest power increased by a factor of $\sim$ 3$\times$. When the p-AlGaN EBL was removed completely, resulting in the p-GaN, grown with 12.5 sccm Cp_2Mg, being next to the MQW active region (i.e. the "no p-AlGaN" data point at 12.5 sccm), the output power was reduced slightly, however it remained above that of the 30 sccm grown sample with the p-AlGaN in place. This highlights the fact that the EBL is indeed playing a significant role in enhancing the active region performance, however the optimal EBL Cp_2Mg flow is 12.5 sccm, not 30 sccm. Viewing the voltage characteristics, we see the voltage only marginally increases from the 30 sccm case to the 12.5 sccm case. To understand the origin of this

improved quicktest power, we performed a SIMS analysis on a sample grown under the 30 sccm condition and the 12.5 sccm condition. The SIMS profiles are shown in Figure 75(b). Here, we see the same abnormal kink in the Mg-concentration tail between the EBL and MQW for the case of 30 sccm, which we also observe in Figure 67(a). In contrast, under the 12.5 sccm condition, the Mg concentration in the EBL shows a characteristics SIMS tail at the interface, suggesting that no significant diffusion of Mg into the MQW has occurred. We also note the decrease in the EBL Mg concentration, which may be why we observe a slight voltage increase when going from the 30 sccm condition to the 12.5 sccm condition.

Following the optimization of the EBL doping level, we also carried out an investigation of the optimal thickness of the last UID GaN barrier on the p-side of the device. However, no significant change in the quicktest characteristics was observed, so we continued to use the simplest design, where the last GaN barrier thickness is equal to the thickness of the other GaN barriers (i.e. 1 nm in the most recent active region designs). Overall, optimizing the EBL thickness was one of the most significant improvements we made to the epitaxial design from our original VCSEL demonstrations in Ref. 8,14,15.

3.5. Doping

As was shown in Section 3.4.1, the doping of the various III-nitrides layers contributes a relatively small percentage to the total internal loss of a violet emitting VCSEL with an ITO intracavity contact. For this reason, optimizing the doping in the structures was not really a critical point of interest until quite recently when the TJ VCSEL was demonstrated.[11] In future designs, one could potentially minimize the internal loss in the VCSEL by using a modulated doping profile, or by simply reducing the doping
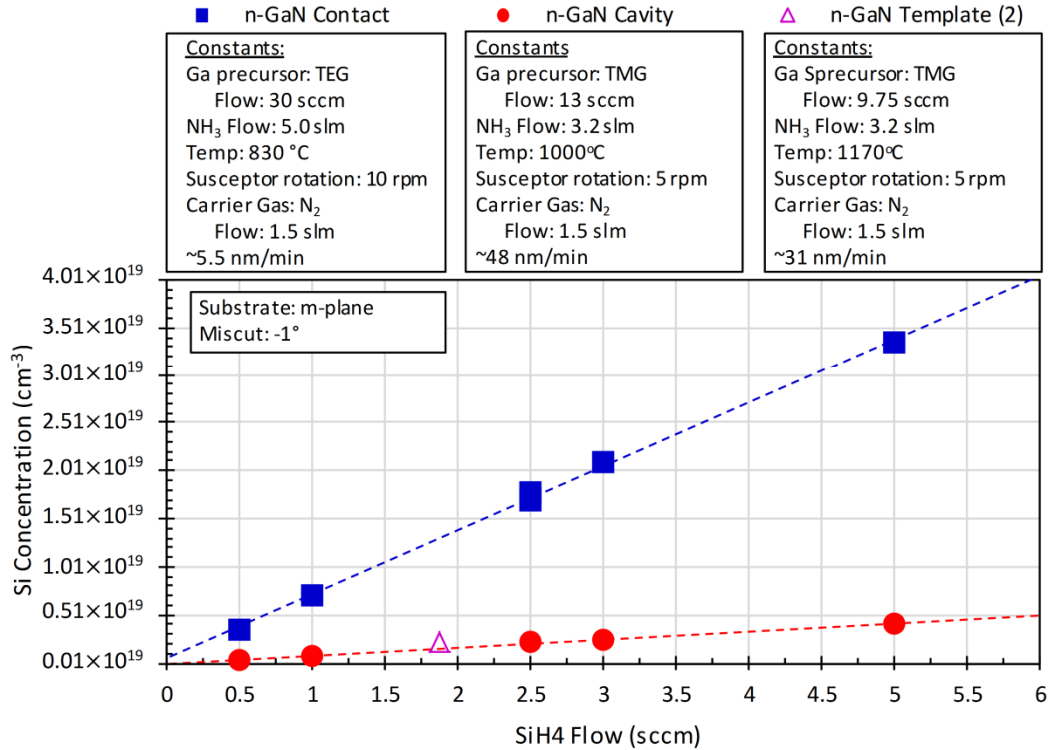
Figure 76 SIMS measured Si concentration vs. SiH$_4$ flow in n-GaN layers grown in TEG and TMG. The constants of the various growth conditions, and the relevant layer in the cavity corresponding to each condition, are shown above the plot. In general, growing in TEG results in a higher Si concentration, but a lower growth rate (~5 nm/min), while growing in TMG results in a lower Si concentration, but a faster growth rate (~50 nm/min).

concentration until an optimal trade-off between the increased voltage and the reduced internal loss were reached. Regardless, have an understanding of Si or Mg concentration vs. SiH$_4$ or Cp$_2$Mg flow in TEG and TMG growth conditions can be useful. We have not characterized the Mg concentration vs. Cp$_2$Mg flow, however Figure 76 shows the SIMS measured Si concentration vs. SiH$_4$ flow in n-GaN layers grown with TMG and TEG as the Ga precursor. These measurements were taken from a single epi. structure specifically designed for this analysis (i.e. not a bunch of different complete VCSEL epi. growths). Above the plot we see the constants for the various layers. Overall, we see that growing in TEG gives a much higher dopant level, but much slower growth rate than growing in TMG. This is why TEG growths are more appropriate for highly doped contact layers. We also use TEG for the InGaN/GaN active region growths, due to its lower impurity incorporation

levels than TMG, as well as it's slower growth rate. Viewing the trend for the TMG doping, we can see the doping has a weak dependence on SiH4 flow. Furthermore, comparing the doping levels from the n-GaN cavity growth conditions (TMG, 1000 °C), to the doping level observed in the n-GaN template (TMG, 1170 °C), we see that changing the growth temperature has little effect on the Si concentration as well. Thus for any highly doped n-GaN layer, it is better to use TEG.

3.6. p^{++}GaN & n^{++}GaN Contacts

Much of the initial work on optimizing the p^{++}GaN contacts for the VCSEL epi. was done by C. Holder. Some of these optimizations are reported in his thesis.[16] Following his developments, a number of quicktest-based analyses were carried out, briefly investigating the potential for using a p^{++}InGaN contact,[278–280] or testing growing the p^{++}GaN in N$_2$ instead of H$_2$, however neither of these yielded significant changes in the IV characteristics measured via quicktest. That being said, quicktest is really only appropriate for analyzing large-scale changes in epi-quality, and it may very well be the case that these types of changes to the p-contact only result in small-scale changes, which must be observed in a complete VCSEL structure, or using the CTLM method.

Additionally, little optimization of the n^{++}GaN contact has been carried out, as the n^{++}GaN Si doping level of ~2.5×10^{19} cm^{-3} is already quite high. However, it would be useful to confirm whether or not this doping level is sufficient to yield Ohmic contacts.

In terms of the optimal metallic contacts to the n++GaN layer (on the n-side or in the case of the TJ being used on the p-side), we have chosen to use the simplest metal stack composed of ~20 nm Ti and ≥ 500 nm Au. There are certainly more optimal metal stacks

that could be used to reduce the contact resistance. A review of nonalloyed and alloyed ohmic contacts to n-GaN can be found in Ref. [281,282]. Lowering the contact resistance is significant because it can lower the operating voltage of the device, thereby lowering the input power of the device, and reducing the amount of internal heating generated under CW operation.

Overall, the more recent III-nitride VCSELs have had fairly good IV characteristics (i.e. low turn-on voltage and low differential resistance),[10–13] suggesting that the contacts and other sources of resistance, such as heterobarriers, are not significantly limiting device performance. Comparing the ITO VCSEL design to the TJ VCSEL design,[11,12] it is evident that the largest source of the voltage increase in the TJ VCSEL is the p^{++}GaN/TJ contact itself, the nature of which is not well understood at this time.

Beyond the more obvious epitaxially related contact issues, we did encounter a number of processing related issues that resulted in significant increases in the voltage of the devices. One issue was p-GaN plasma damage caused by the IBD deposition of the DBR layers, which will be discussed here, while the other was an anomalous voltage increased cause by performing the flip-chip bond at 300 °C, which is discussed in Section 4.3. p-GaN plasma damage, or p-GaN passivation, refers to the damaging of the p-GaN contact upon exposure to high energy plasmas. This is commonly observed in III-nitrides research generally and is the primary reason why metal contacts and transparent conductive oxide (TCO) layers, such as ITO, are generally deposited using e-beam deposition, rather than sputtering, or other plasma-based deposition techniques. In the literature, p-GaN plasma damage has been investigated in Refs. [283–286]. The primary origin of the "damage" is the creation of nitrogen vacancies, which are n-type in nature, which results in compensation at

the p^{++}GaN surface. This is why n-contacts do not suffer from catastrophic plasma damage. Actually, many reports suggest that one can improve an n-contact by exposing the n-GaN to plasma.

In the case of the nonpolar VCSEL design, the DBR layers are deposited using IBD. Though the intracavity contact sits between the DBR and the p^{++}GaN layer, in the case of an ITO design, the intracavity contact is quite thin (1/4-wave (~50 nm)), thus it is possible that high energy ions from the DBR deposition may reach the ITO/p^{++}GaN interface. Even if this interface is not reached, it is possible that the ions may damage the ITO itself, causing the spreading resistance to increase. To investigate this effect, we carried out a series of IV measurements on partially processed VCSELs before the p-DBR deposition and after the p-DBR deposition, where the DBR was deposited under various ion beam powers. The results of this study are shown in Figure 77. Viewing Figure 77(a), we see the variation in deposition rate of the Ta$_2$O$_5$ DBR layer, as a function of the deposition (depo.) beam and assist beam power. The SiO$_2$ layers are deposited under the same beam conditions, but with
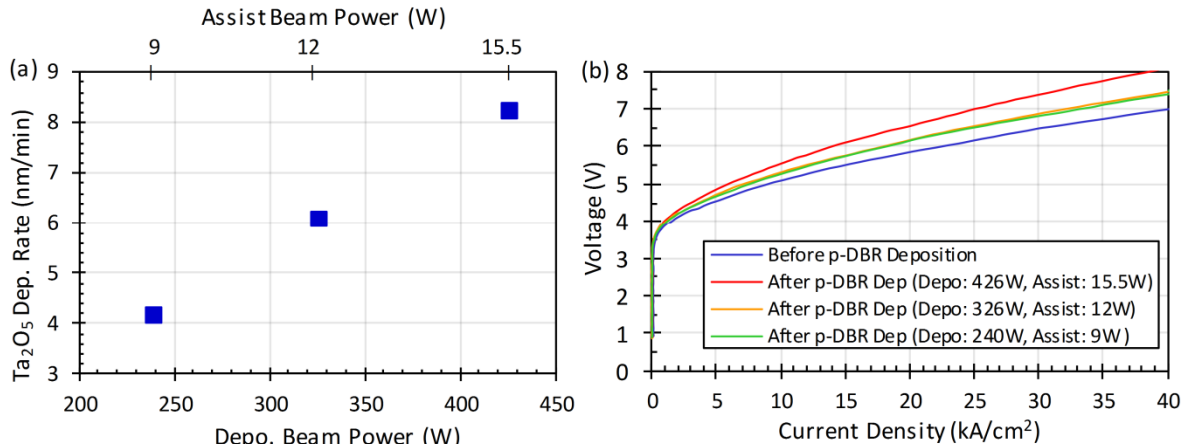
Figure 77 Results from the optimization of p-GaN plasma damage occurring from the DBR deposition. (a) shows the Ta$_2$O$_5$ deposition rate, measured via ellipsometry, vs. the deposition (depo.) beam power and the assist beam power in the IBD system. (b) shows the IV measurements on 20 μm aperture diameter partially processed VCSELs, measured before and after the p-DBR deposition under ion beam powers. Reducing the beam power from the original intensity (Depo: 426 W, Assist: 15.5 W), reduces the degree of plasma damage, however the increase in voltage resulting from the DBR deposition step cannot be completely elliminated.

a Si target in place. The original beam powers, used to fabricated the DBRs in our early devices,[8,14–16] corresponds to the highest power (Depo: 426 W, Assist: 15.5 W). Observing the IV characteristics of 20 µm aperture diameter partially processed IIA VCSELs before and after the p-DBR deposition under the various beam power conditions, Figure 77(b), we see that using the original high power deposition conditions results in a significant increase in the differential resistance of the device. Reducing the beam voltage and current by ¾, results in the deposition rate reducing by ~3/4th (Figure 77(a)). This then reduces the degree of voltage increase induced by the DBR deposition, however reducing the beam power further shows no significant change in the IV characteristics (Figure 77(b)). This implies that the DBR deposition always induces some small degree of ion damage, however it can be minimized. It is important to note that all of this analysis was done on IIA VCSELs with ~50 nm ITO intracavity contacts. Because the n-GaN TJ intracavity contacts are much thicker (> 100 nm) and because plasma damage actually creates n-type N-vacancies, it is quite possible that this effect is not as much of a concern in TJ VCSELs, though no experimental analysis was carried out.

In summary, the current contacts on the VCSELs are of a fairly high quality, however there is room for some minor improvements which could help reduce the input power of the devices and improve the CW performance overall.

4. Optimizing Structural Design

"Being right might be gratifying, but in the end it is static, a mere statement. Being wrong is hard and humbling, and sometimes even dangerous, but in the end it is a journey and a story...To fuck up is to find adventure."

– Kathryn Schulz

Now that we have an understanding of the general concepts and experimental investigations relevant to the epitaxial structure, we can move to higher level device design parameters. Overall, the rapid pace of the nonpolar VCSELs project has been a result of the ability to test a number of different device designs by processing many devices in parallel. The results presented in the following section are essentially what are reported in our more recent nonpolar VCSEL papers. Due to the rapid pace of experimental progress, and the comparably slow peer-review process for publications, the order in which our latest papers were published does not match the order in which the experimental results were obtained. Specifically, the smooth e-beam deposited ITO results from Ref. 9 were obtained prior to the IIA VCSEL demonstration reported in Ref. 10. These demonstrations were then followed by investigations into the aperture dependence of lasing performance on IIA VCSELs for ITO intracavity contacts, discussed in this section. In parallel with this analysis, we also demonstrated 100% polarized emission from a nonpolar VCSEL array, which is also
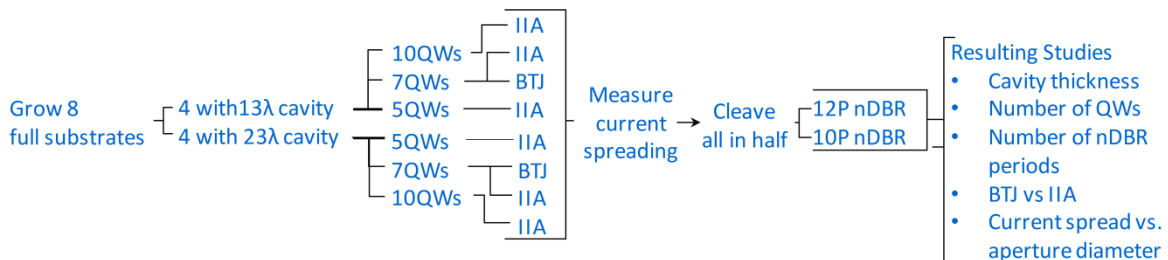
Figure 78 Schematic representation of the design of experiment (DOE) in process at the time of this writing.

described in this section. However, before either the aperture diameter dependence study or the 100% polarized VCSEL array demonstration could be published, we achieved breakthrough results using the n-GaN TJ intracavity contact design on a IIA VCSEL, reported in Ref. 11,12. The devices from the TJ VCSEL study were processed in parallel with a chip to test the PECA design (with an ITO intracavity contact). This PECA VCSEL also showed very interesting emission characteristics and overall improved output power compared to the IIA design, resulting in the demonstration reported in Ref. 13. Though these results were interesting, the fragility of the PECA process led us to decide to abandon this particular design, in favor of making other advancements and characterizations using devices with less fragile aperture designs. The final VCSEL study that was planned before I left UCSB is summarized in the design of experiment (DOE) schematic shown in Figure 78. Here, we see the DOE involved a parallel processing round of samples that would allow us to analyze 13λ and 23λ IIA+TJ VCSEL cavities (all previous VCSELs had ~7λ cavities), the aperture dependence of the lasing characteristics (i.e. the current spreading vs. aperture diameter), the effect of different numbers of n-DBR mirror periods on different cavity lengths, as well as the effect of different numbers of QWs on each of the these cavities. It is important to note that one must initially analyze the current spreading before the n-DBR deposition, as having the n-DBR in place convolutes the spontaneous emission intensity profile across the aperture, which is arguably the simplest way to analyze the current spreading in the device. It should be highlighted that an optimization of the number of n-DBR periods is critical for designs with different cavity thicknesses, as a longer cavity allows one to reduce the number of n-DBR mirror periods and maintain a low mirror loss, but increase the fraction of light emitted from the top-side of the device, allowing a higher

output power and differential efficiency. This DOE would also allow us to test our first attempt at a BTJ VCSEL, with simple n^{++}GaN BTJ capped with a n-GaN regrown current spreading layer, as is demonstrated on a micro-LED reported in Ref. 287. Here, it should be noted that using a BTJ design with an n-AlGaN cap, instead of n-GaN, would result in the BTJ design having some degree of index guiding, which would be favorable for optical confinement. The following section will highlight the previous experimental results leading up to the DOE proposed in Figure 78.

4.1. Intracavity Contacts

As was shown in Section 1.4.5.2 and Section 3.4.1, the intracavity contact can have critical implications for the thermal performance as well as optical performance (i.e. threshold modal gain), which can directly impact the optimal number of QWs for a VCSEL. Historically speaking, ITO has been the most common intracavity contact used for III-nitride VCSELs, however a number of groups have attempted to use a III-nitride TJ intracavity contact,[288] and recently we have demonstrated a VCSEL with such a TJ.[11,12] This section will focus on the development of the ITO and TJ intracavity contacts used in all the newer generations of nonpolar VCSELs reported in Ref. 10–13. The ITO intracavity contact development is also reported in Ref. 9.

4.1.1. Tin-Doped Indium Oxide (ITO)

In the first generation of nonpolar VCSELs,[8,14–16] electron-cyclotron resonance (ECR) sputtering was used to deposit highly smooth, transparent, and conductive ~50 nm ITO

intracavity contacts. This deposition was carried out by MES AFTY Corporation, a subsidiary company of Mitsui Engineering & Ship building Co., who report on their ECR sputter system in Ref. 289. In the end, we did not decide to purchase the tool, so we needed an alternative method for depositing ITO. Furthermore, sending the samples to MES AFTY in Japan added ~1 month to the total processing time, so it was not an ideal situation regardless.

Considering the deposition techniques used by other researchers in the field of III-nitride VCSELs, we can recognize that nearly every published III-nitride VCSEL has employed ITO deposited by companies, including MES AFTY Co.,[14] Nichia Co.,[171–173] Canon Co.,[131–133,290] and Evatec Co..[166] Of these, only the MES AFTY ITO deposition technique is identified as ECR sputtering,[289] however it is likely that all are using a remote plasma[289,291] or an ion assisted e-beam deposition technique.[292] Overall, this is a result of the necessity for ITO intracavity contacts to be highly smooth, transparent, and conductive.[9] The roughness is critical to minimize in order to minimize the scattering loss, while the transparency needs to be maximized to minimize the absorption loss from the ITO contacts. Finally, the conductivity needs to be maximized to maximize the current spreading uniformity in the aperture of the device. Beyond the morphological and optoelectronic requirements for the ITO films, one must also avoid p-GaN plasma damage, thus remote plasma, such as ECR sputtering, or physical vapor deposition techniques, such as e-beam deposition, are necessary for ITO deposition on III-nitride VCSELs.[283–285,293] While the more advanced remote plasma techniques do yield high quality ITO films with low surface roughness, without damaging p-GaN, they are relatively complex and expensive. Thus, a method for achieving high quality ITO using a conventional e-beam is important for

reducing the cost and complexity of III-nitride VCSELs research. Furthermore, other devices, such as OLEDs, III-nitride LEDs, or EELDs also benefit from depositing ITO using e-beam evaporation, rather than sputtering. Yet in these more typical devices, the requirement for low surface roughness is not as strict as it is in the case of VCSELs. More specifically, for LEDs, surface roughness enhances the extraction efficiency, thus improving device performance.[294–297] For EELDs, the transverse mode does not reach the surface of the ITO (if the device is properly designed), thus the surface roughness is not important. In contrast, for VCSELs, the axial mode does not decay until passing the ITO intracavity contact into the p-DBR. If the p-DBR is deposited using a conformal deposition technique, such as the IBD process used here, any surface roughness in the ITO can potentially be propagated into the p-DBR, introducing scattering loss at every interface. The natural roughness of the p-DBR layers alone may also contribute to a significant amount of scattering loss if a high quality sputtering system is not used.

4.1.2. Scattering Loss from ITO Surface Roughness

The dependence of mirror reflectance and scattering loss on surface roughness was investigated several decades ago for infrared and microwave mirrors, using scalar models[298] and vector models.[299–306] In Ref. 9 we built on these models and simulated how the surface roughness from ITO would affect III-nitride VCSEL performance. The main results from this theoretical investigation are shown in Figure 79, where we see the effect of ITO RMS roughness on scattering loss, threshold current density, and top-side differential efficiency. The details of the modeled 405 nm VCSEL can be found in Ref. 9, here we simply highlight
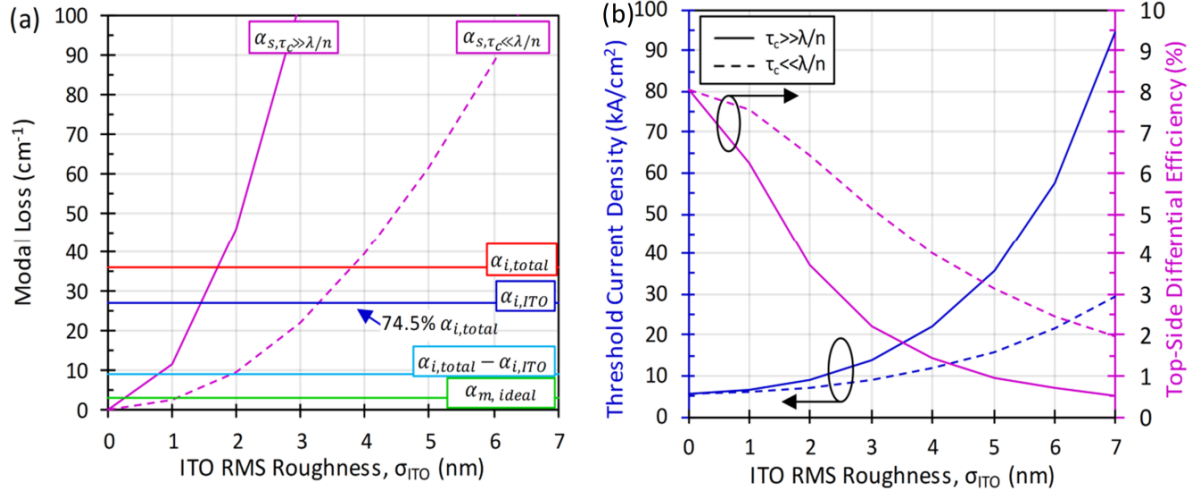
Figure 79 (a) shows a breakdown of the various sources of modal loss a simulated ~7λ 405 nm VCSEL.[9] The scattering loss, α_s, for the case of the correlation length, τ_c,(proportional to the average spacing between roughness features) is smaller than the interacting wavelength, λ, normalized to the refractive index, n, of the ITO layer, $\tau_c \ll \lambda/n$ is shown. Also shown is the scattering loss for the opposite case, where $\tau_c \gg \lambda/n$. $\alpha_{i,ITO}$ is the internal loss in the ¼-wave ITO layer, assuming an absorption coefficient of 2000 cm[-1] (Figure 42). (b) Threshold current density, J_{th} and top-side differential efficiency, $\eta_{d,top}$, vs. ITO RMS roughness, for the 7λ ITO VCSEL. The threshold current density is determined using the $J(g)$ characteristics measured on violet emitting EELDs from Ref. 155. The active region of the simulated VCSEL here used a 3QW, A8 nm, B1 nm, EBL 5 nm design, as the EELDs in Ref. 155 also had 3QWs with A8 nm. The top-side differential efficiency is calculated using Eqn. (4), assuming an injection efficiency of 100 %.

that it had a ~7λ cavity with an active region design consisting of 3QW, A8 nm, B1 nm, and

EBL 5nm. This was the same number of QWs and QW width (A), used in R. M. Farrell, et.

al's nonpolar violet emitting EELDs, from which the $J(g)$ trend, used to simulate the

VCSELs threshold current density vs. ITO RMS roughness in Figure 79(b), was extracted.

Figure 79(a) shows a breakdown of the various sources of modal loss present in the

simulated ITO VCSEL. Here, we see two different extremes for the scattering loss, one

where the correlation length, τ_c, which is proportional to the average spacing between

roughness features, is smaller than the interacting wavelength, λ, normalized to the

refractive index, n, of the ITO layer, $\tau_c \ll \lambda/n$, and one where the correlation length is

much greater than the wavelength normalized by the index, $\tau_c \gg \lambda/n$. The correlation

length can analyzed by measuring the autocovariance, $G(\tau)$, of a film after performing an

AFM scan. The measured autocovariance data can then be fit with a Gaussian function of the form

$$(33) \quad G(\tau) = \sigma^2 exp[-(\tau/\tau_c)^2],$$

where τ is the autocorrelation distance.[307] The autocovariance is essentially a measure of the variations in the amplitude and period of a film's surface features, yielding the average correlation between two points separated by a distance τ.[308] The distance at which the autocovariance function equals $1/e$ of its initial value is defined as the correlation length, τ_c.[308] A more complicated analysis of the correlation length involves representing the autocovariance function as the sum of a Gaussian and exponential term.[306,309,310] This results in a term for the long-range correlation length, as well as the short-range correlation length, which can describe surfaces with small surface features overlain on larger hillocks. This greatly complicates the general analysis and thus we do not employ such a method. To measure the specific correlation length for the ¼-wave ITO films used in our devices, AFM measurements were carried out on a number of e-beam deposited ITO films with RMS roughness's ranging from ~0.6 nm to ~4 nm. The autocovariance of the surface was then analyzed using Gwydion 2.36,[311] and the data was fit using Eqn. (4). The average correlation length was ~25±6 nm. For the nonpolar violet VCSELs considered here, λ/n is ~405 nm / 2, which suggests that we nearer to the regime where $\tau_c \ll \lambda/n$. Viewing Figure 79(a), we see that the scattering loss, α_s, has a weaker dependence on the ITO RMS roughness for $\tau_c \ll \lambda/n$, compared to $\tau_c \gg \lambda/n$. This implies that having > 1 nm RMS roughness is less catastrophic in our case, however surfaces have long-range and short-range correlation lengths,[306,309,310] and the measured correlation length (25 nm) and wavelength of interest (405 nm/~2) do not strictly satisfy the condition $\tau_c \ll \lambda/n$, thus the true scattering loss

value will likely sit somewhere between the case of $\tau_c \gg \lambda/n$ and $\tau_c \ll \lambda/n$. The case of $\tau_c \ll \lambda/n$ and $\tau_c \gg \lambda/n$ thus give the upper and lower bounds of the potential scattering loss induced by ITO surface roughness.

It is of note that the large absorption coefficient of the ITO layer (2000 cm^{-1}) at 405 nm leads to a high internal loss, which lowers the fraction of the total modal loss contributed by the scattering loss. As longer wavelength VCSELs would operate further from the ITO absorption edge, where the ITO absorption would be dominated by free carrier absorption, typically much less than band-edge absorption,[312,313] the scattering loss would contribute to a larger percentage of the total cavity loss.

Viewing the simulated threshold current density and differential efficiency trends in Figure 79(b), we see that for both cases ($\tau_c \gg \lambda/n$ and $\tau_c \ll \lambda/n$), having < 1 nm RMS roughness for the ITO intracavity contact, minimizes the threshold current density and maximizes the differential efficiency. For $\tau_c \gg \lambda/n$, having > 2 nm RMS roughness will yield a threshold current density > 10 kA/cm^2, essentially preventing CW operation. For $\tau_c \ll \lambda/n$, having > 3 nm RMS roughness will yield > 10 kA/cm^2, thus the effect of scattering loss is not as catastrophic, as was observed previously. Comparing the J_{th} and $\eta_{d,top}$ trends, shown in Fig. 3(c), we see that for low roughness values, the scattering loss has a more significant effect on $\eta_{d,top}$ than on J_{th}. Specifically, for a 1 nm RMS roughness there is an approximately 6 to 23 % reduction in the differential efficiency, while there is an approximately 6 to 12 % increase in the threshold current density. The stronger dependence of differential efficiency on scattering loss, for low roughness values, is a result of the differential efficiency being directly (inversely) proportional to the scattering loss (Eqn. (4)), while the threshold current density, is related to the scattering loss through Eqn. (7), where

the scattering loss is wrapped inside the threshold modal gain term, and is overall less directly related to the threshold current density than the differential efficiency.[3,155] In summary, Figure 79 demonstrates that in the case of $\tau_c \gg \lambda/n$ and $\tau_c \ll \lambda/n$, having < 1 nm RMS roughness for the ITO layer is essential for maximizing the differential efficiency, output power, and minimizing the threshold current density.

4.1.3. Optimization of Smooth e-beam ITO

In general, e-beam deposited ITO films typically have an RMS roughness on the order of 0.5-6 nm, a transparency of ~80 % at 405 nm, a resistivity slightly higher than those achieved using sputtering techniques (10^{-3}-10^{-4} Ω-cm), and p-GaN contact resistances lower than those reported for many sputtered contacts (10^{-2}-10^{-3} Ω-cm^2).[290,314–327] As observed in our e-beam ITO deposition analysis to follow, when ITO is deposited at room temperature, the films are typically smooth with $\leq$ 1 nm RMS roughness, however they exhibit poor optoelectronic properties, which would lead to large absorption losses and poor current spreading in the aperture of a VCSEL.[323–325,327] There are many reports on improving the optoelectronic properties of e-beam deposited ITO films by varying the post deposition annealing conditions, however this generally results in increasing the RMS roughness to > 1 nm, making such post-deposition annealing processes inappropriate for VCSELs.[315–320,323,324,326,327] This is consistent with what C. O. Holder observed in his e-beam deposited ITO investigations, where he also observed large agglomerates forming in the center of the aperture upon anneal ITO films deposited at room-temperature.[16]

Because we no longer had the option of using MES AFTY's ECR sputtered ITO, and because we had recently built an e-beam deposition system with in-situ heating, we sought

to carry out a rigorous analysis of the e-beam ITO deposition parameters to achieve films with < 1 nm RMS roughness, with a high transparency and conductivity. The e-beam chamber (e-beam #2 in UCSB's Nanofab) was a standard bell jar chamber. In_2O_3/SnO_2 (90/10 wt. %) source material purchased from Kurt J. Lesker (Part No. EVMITO40) was used as the evaporation source. The source-substrate distance was ~29 cm. Substrate heating was achieved using a custom built resistive heater wired to a Variac AC controller. The maximum heater temperature was ~285 ^{o}C. The heat-up and cool-down rate was 5 V/5 min on the Variac AC controller. Samples were held using metal clips and the temperature was measured using a thermocouple inserted into the metal chuck between the heating block and the substrate. The chamber was evacuated to $< 3 \times 10^{-6}$ Torr before introducing O_2. The chamber pressure was controlled by the oxygen flow. Following the deposition, the O_2 flow and chamber pressure were held constant until < 100 ^{o}C, then the samples were unloaded in atmosphere. The deposition rate was monitored in-situ using a quartz crystal monitor (QCM) and ex-situ thickness measurements were made using a J. Woollam M-2000 DI Variable Angle Spectroscopic Ellipsometer. We also measured some test samples using confocal microscopy and stylus profilometry to confirm the deposition rate measured by the QCM. The ellipsometer measured thickness was used to calculate the resistivity from the 4-point probe measured sheet resistance, discussed in detail below. Prior to deposition, each sample was dipped in 1:1 $HCl:H_2O$ solution for 30 sec., rinsed in DI water, and dried with N_2.

The ITO ellipsometer measurements were carried out at angles of 55°, 65°, and 75°, over a spectral range of 270 nm to 1000 nm. CompleteEASE software from J. Woollam was used to analyze the measured psi, Ψ, and delta, Δ, vs. wavelength information. The ellipsometer model consisted of a Si substrate and a generic oscillator (Tauc-Lorentz) layer

representing the modeled ITO film. This yields a 5 parameter fit. The mean-square-error (MSE) over the measured spectral range was generally < 10. The MSE was calculated using the weighted N, C, and S model describe in the CompleteEASE user manual,[328] where an MSE of ~1 implies an ideal fit. We also tested a number of more complicated models, which accounted for surface roughness, a gradients in refractive index through the ITO films, and the presence of Drude-oscillator characteristics,[328] were also tested. While these models did yield slightly different refractive index dispersion profiles, there was little variation in the measured thickness, compared to the simplified Tauc-Lorentz oscillator model. Also, these additional layers of complication did not significantly reduced the MSE, thus we chose to use the more simplified model.[328]

For each test of different deposition conditions, three substrates were co-loaded: (1) double-side polished (DSP) sapphire, (2) (100) polished Si, and (3) m-plane GaN LEDs (~405 nm emission) with epitaxial structures similar to those used in the older nonpolar VCSELs,[8,14,15] but without the sacrificial MQW. A CDE ResMap 4-point probe was used to measure the ρ and R_s on the ITO/DSP sapphire samples. It is of note that one should not measure the 4-point probe resistivity on ITO/Si samples, as the conductivity of the Si substrate will convolute the calculated resistivity of the ITO film. However, performing the ellipsometer measurements on ITO/Si samples is favorable, because it avoids the presence of back-side substrate reflections which would be seen in the case of ellipsometer measurements on ITO/sapphire samples. A Carry 500 Spectrophotometer was used to measure the transparency on the ITO/DSP sapphire samples, after normalizing to a bare DSP sapphire substrate. An Asylum MFP-3D Atomic-Force Microscope (AFM) (< 50 pm noise floor), equipped with an AppNano Forta (single crystal silicon) AFM probe, was used

to measure the surface morphology on the ITO/LED samples. This was the same AFM system also used for all other AFM measurements reported in this thesis. Following the AFM measurements, 40 μm radius ITO contacts were etched using an MHA etch on the ITO/LED samples. Pd/Au (10/200 nm) p-contacts and blanket Ti /Au (10/200 nm) backside n-contacts were then deposited via e-beam evaporation. Pulsed IV measurements were made at 1% duty cycle (1 μs pulse width) and the voltage at 1 kA/cm^2 was recorded to give an idea of the relative contact resistance for the different ITO films.

4.1.3.1. ITO Deposition Temperature Series

To analyze the dependence of the ITO film properties on the deposition temperature, 18 nm ITO films were deposited at 30 sccm O$_2$ flow (~0.27 mTorr), at a rate of 0.15 Å/sec, over a range of temperatures from 45 ^{o}C to 250 ^{o}C. Figure 80 summarizes the results the temperature series. Viewing Figure 80(d), we see that at 45 ^{o}C and 96 ^{o}C, the films appear to be amorphous with periodically spaced large crystalline clusters. This is in agreement with the literature, where a crystallization temperature of ~150 ^{o}C (close to the melting point of In metal (157 ^{o}C)) is commonly reported.[320,329,330] Additionally, the TEM analyses reported in Ref. 331 and x-ray diffraction measurements reported in Ref. 330 on a similar temperature series, show that low temperature ITO films are amorphous with periodic crystalline island regions. Excluding the large crystalline clusters from the RMS roughness analysis, indicates that the amorphous regions on the films deposited at 45 ^{o}C and 96 ^{o}C have an RMS roughness of < 0.5 nm. Figure 80(e) shows the RMS roughness with the large crystalline clusters included in the measurement (i.e. a full area RMS roughness measurement), where one can see the crystalline clusters cause the RMS roughness to be > 1 nm for the 45 ^{o}C
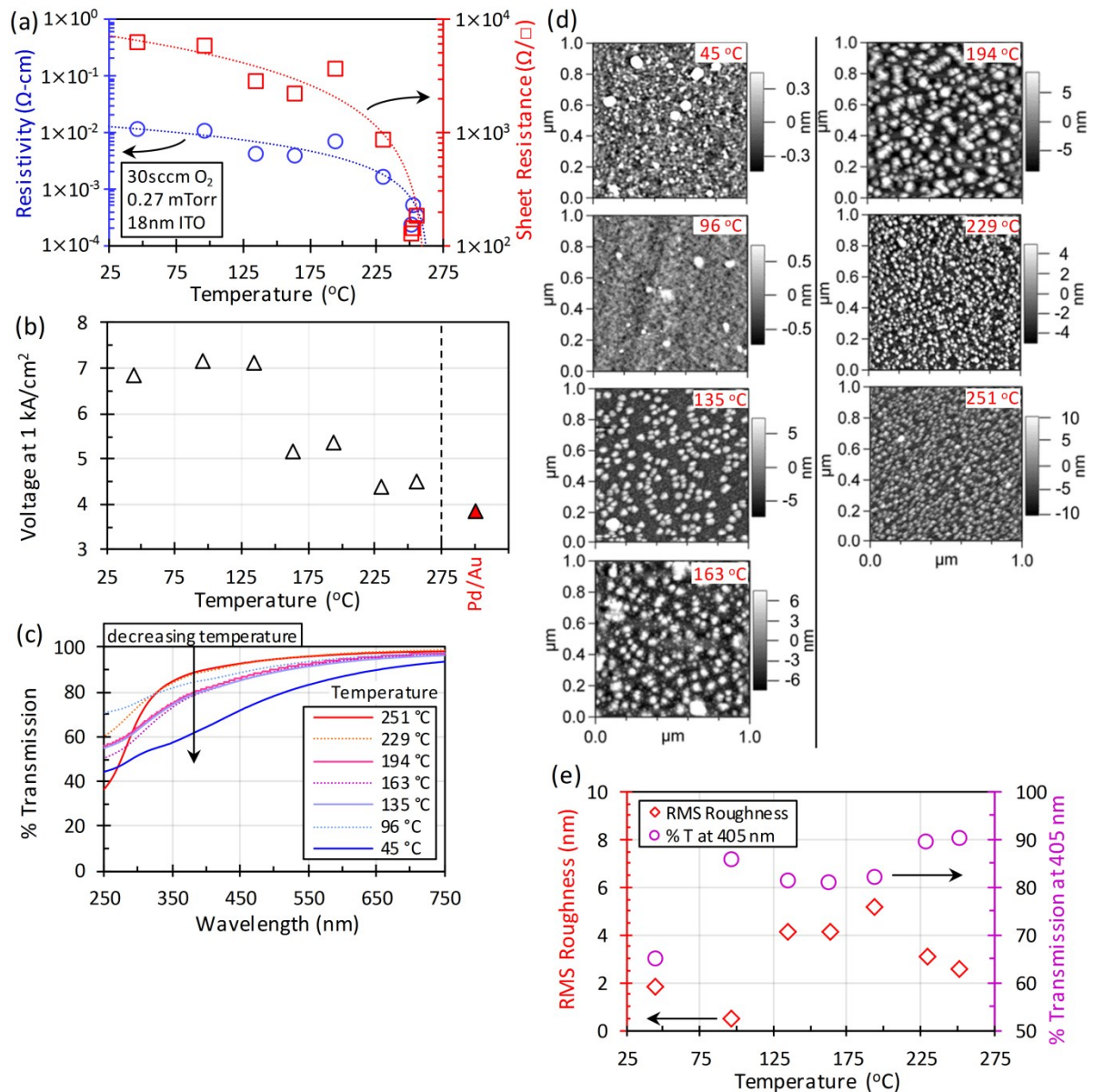
Figure 80 The temperature dependence of 18 nm ITO films deposited at 30 sccm O_2 flow (0.27 mTorr). (a) Resistivity and sheet resistance vs. temperature measured on ITO/DSP sapphire samples. (b) Voltage at 1 kA/cm^2 measured on ITO/LED samples. The voltage at 1 kA/cm^2 for Pd/Au contacts is shown for comparison. (c) % transmission for the ITO/DSP sapphire samples. (d) AFM images on the ITO/LED samples. (e) RMS roughness, corresponding to the AFM images shown in (d), and the % transmission at 405 nm, taken from the measurements shown in (c), vs. substrate temperature.

film. This particular case highlights an important consideration in AFM analysis generally, where one must be careful to draw a significant conclusion from an RMS value alone, without knowing what the actual morphology looks like. Viewing Figure 80(a) and (b), we can see that the dominant amorphous nature of these low-temperature films leads to a high

resistivity and voltage at 1 kA/cm^2 of ~1×10^{-2} Ω-cm and ~7 V. Beyond the actual crystallinity and the Sn concentration of the films influencing resistivity, Habermeir[332] has suggested that increasing the deposition temperature may also increase the oxygen vacancy concentration, thereby contributing to the reduction in the resistivity observed with increasing temperature in Figure 80(a). Additionally, hydrogen interstitials have recently been shown to act as donors in indium oxide.[333–337] Considering the temperature effects on transparency, shown in Figure 80(c), we note that the transparency increases with temperature from 45 °C to 96 °C. This can be attributed to a marginal increase in the crystallinity of the ITO film. At 135 °C the onset of crystallization is evident, with a high density of grains surrounded by amorphous regions, as seen in Figure 80(d). At this temperature, the nucleation of grains leads to an increase of the surface roughness to ~3.5 nm (Figure 80(e)). As the temperature is increased further to 163 °C and 194 °C, the grain size increases and the amorphous regions are no longer visible (Figure 80(d)). At 194 °C, with the largest grains seen in the series, the RMS roughness is ~5.5 nm (Figure 80(e)). Above 194 °C the grain size and RMS roughness begins to decrease. This trend in the grain size vs. temperature is counterintuitive to traditional models of grain growth vs. temperature.[338] The reason for this is that ITO initially grows in an amorphous state and crystallizes as thickness increases, regardless of the substrate temperature.[330,331] As temperature increases the density of crystalline nucleation sites embedded in the amorphous region increases, and the thickness at which the crystallites begin to form decreases.[330,331] This implies that at intermediate temperatures, (i.e. 163 °C and 195 °C), there is a relatively low density of nucleation sites when the films are very thin, which allows the formation of larger grains as films grow thicker. However, at high temperatures (i.e. ≥ 229 °C), there is a

high density of nucleation sites when the films are very thin, resulting in smaller, more uniform grains when the final thickness of 18 nm is reached. By ~250 ^{o}C, the film morphology is homogeneous, with an RMS roughness of ~2.5 nm. Muranka, et al.[331] report a saturation of the grain size at >300 ^{o}C, which implies that the trend of reducing grain size and RMS roughness, observed in this study, would not be likely to continue at higher temperatures.

Considering the temperature dependence of the electrical characteristics of the films in more detail, we can see a linear decrease of the resistivity, sheet resistance (Figure 80(a)), and voltage at 1 kA/cm^2 Figure 80(b)), with increasing temperature. This results in a resistivity of ~2 × 10^{-4} Ω-cm and a voltage at 1 kA/cm^2 (~50 mA) of ~4.5 V, which is ~0.5 V greater than the voltage measured on the LEDs with the Pd/Au. Because Sn does not contribute carriers (i.e. it acts as a neutral impurity) when ITO is amorphous,[339] the relative change in sheet resistivity corresponds to the relative reduction in the amorphous area of the films with increasing temperature. Assuming the differential resistance of the measured LEDs is dominated by the contact resistance, we estimate a specific contact resistivity of ~7.8 × 10^{-4} Ω-cm^2 for the Pd/Au contact, and ~1.3 × 10^{-3} Ω-cm^2 for the ITO contacts deposited at 251 ^{o}C, operating at 4.41 V at 1 kA/cm^2. This ITO/p-GaN specific contact resistivity is lower than many values reported in the literature.[290,314,317–319] Additionally, these values are an likely an upper bound on the true contact resistivity, as any additional sources of resistance, such as those resulting from band-offsets in the epitaxial layers, would lower the contribution of the contact to the measured voltage of the device, thereby lowering the calculated contact resistivity.

Viewing Figure 80(c) and (e), we see that the ITO film deposited at a low temperature (45 ^{o}C) shows a low transparency. As the temperature is increased to 96 ^{o}C and 194 ^{o}C, the transmission spectrum seen in Figure 80(c) remains relatively unchanged. As was previously mentioned, this temperature range is around the reported crystallization temperature of 150 ^{o}C, suggesting that complete crystallization does not occur until > 194 ^{o}C, which is in agreement with the AFM images of Figure 80(d), all of which show a gradually increasing area of crystalline regions surrounded by a decreasing area of amorphous regions, with increasing temperature. At 229 ^{o}C, the transparency is observed to increase significantly, yet a short wavelength transmission tail, observed in all the films with amorphous regions, is still present. At 251 ^{o}C a sharp absorption edge is observed in the transmission spectrum, indicating that the film is fully crystalized.

In summary, as temperature increased the resistivity linearly decreased, the voltage at 1 kA/cm^2 decreased to near the value of Pd/Au contacts, and the transparency increased until saturating at ~90 % at 405 nm. Additionally, the RMS roughness is observed to increase up to a value of ~5 nm at ~200 ^{o}C, then decrease as the temperature is increased further. Though the high temperature films shown high quality optoelectronic characteristics, they do not have < 1 nm RMS roughness, thus they are not ideal for a VCSEL.

4.1.3.2. ITO Deposition O$_2$ Flow Series

Following the temperature series, we carried out an analysis investigating the effect of oxygen flow and pressure on the morphological and optoelectronic properties of ITO. Here, the deposited films were ~35 nm thick and they were deposited at 250 ^{o}C, at a rate of

0.15 Å/sec, for oxygen flows ranging from 30 sccm to 1 sccm. This corresponds to a range of pressures from 0.27 to 0.015 mTorr. The results of this series are summarized in Figure 81. Viewing Figure 81(a), (b), and (d), we see the resistivity and transparency remained relatively constant when the O_2 flow was decreased from 30 sccm (0.27 mTorr) to 10 sccm (0.12 mTorr). At 1 sccm O_2 flow (0.015 mTorr), Figure 81(a) shows the resistivity increased by a factor of 3. In Figure 81(b) we see the transparency also increased from ~90 % at 405 nm for O_2 flows in the range of 10-30 sccm, to ~95 % at 405 nm. This is likely a result of the reduction in the free carrier abosrption.[322] Viewing Figure 81(d), we note that the RMS roughness steadily increased from ~4 nm at 30 sccm O_2 to ~32 nm at 1 sccm O_2 flow. This RMS roughness value (32 nm) is, to our knowledge the highest reported for ITO and could
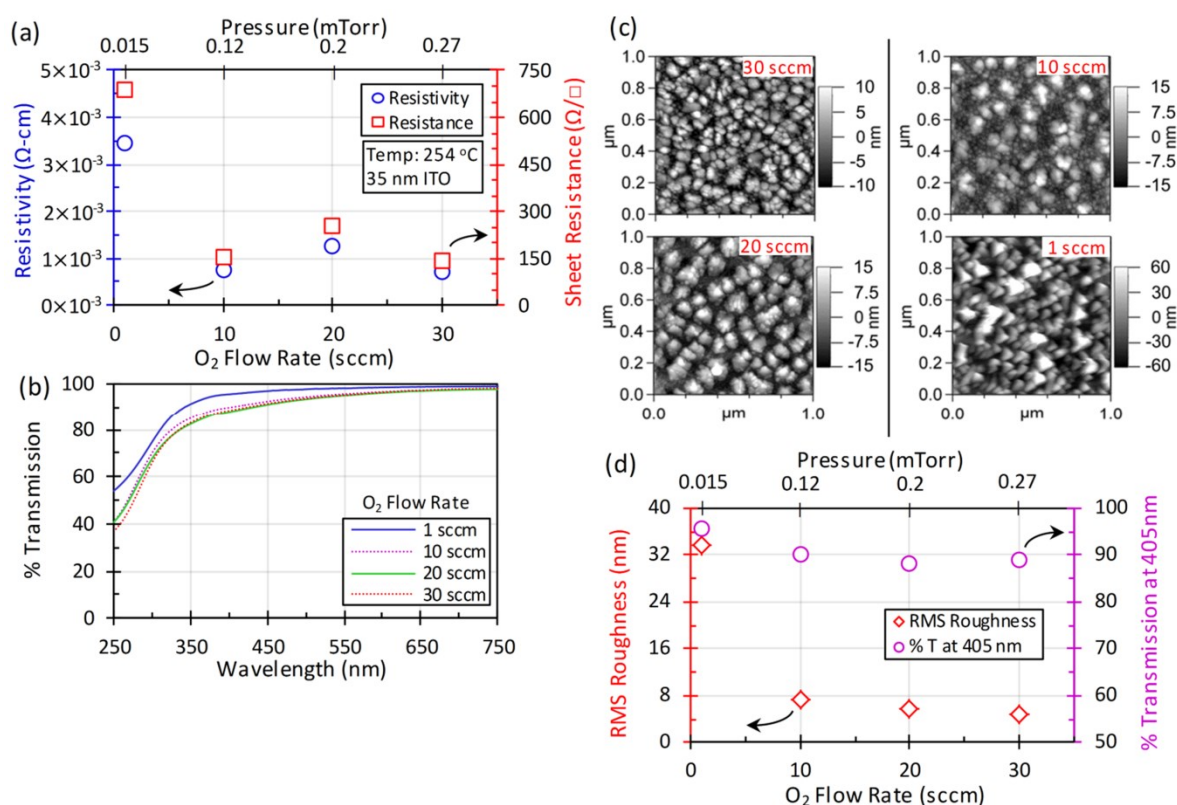
Figure 81 The dependence of 35 nm ITO films deposited at 250 °C on O_2 flow and pressure dependence. (a) shows the resistivity and sheet resistance vs. O_2 flow and pressure. The 4-pt probe measurements were performed on ITO/DSP sapphire samples. (b) shows the % transmission for the ITO/DSP sapphire samples. (c) shows AFM scans of the ITO/LED samples. (d) shows the RMS roughness, corresponding to the AFM images in (c), and the % transmission at 405 nm, from the spectrometer measurements in (b), vs. O_2 flow and pressure.

be useful for LED applications, where a rough surface can improve extraction. Overall, the trend of RMS roughness vs. O_2 flow and pressure shows that the ITO roughness cannot be reduced to < 1 nm RMS, simply by varying the O_2 flow and pressure, at temperatures that yield highly transparent and conductive films.

Considering the physical origin of the observed trend in the ITO properties as a function of O_2 flow, we can hypothesize that the slight increase in resistivity with decreasing O_2 pressure is due to a small increase in the carrier concentration, outweighed by a large decrease in the mobility.[322,340,341] This effect can be attributed to the increased oxygen vacancy concentration as the O_2 pressure is decreased.[322,340,341] It is of note that the dependence of resistivity on O_2 flow and pressure generally shows a convex parabolic trend, therefore it is possible that if we were able to increase the O_2 pressure further, without shutting down the e-beam, the resistivity would be seen to increase again, due to the oversaturation of oxygen, leading to the formation of defects and structural imperfections.[322,340–343] Additionally, it is important to realize that the optimal O_2 pressure is dependent on deposition temperature.[322]

Because the films deposited at low O_2 flow are extremely rough, highly transparent (95 % at 405 nm), fairly conductive ($\rho\sim3.5 \times 10^{-3}$ Ω-cm), we believe depositing ITO under low O_2 flow and pressure conditions may be optimal for LED applications, as the increased roughness and transparency would improve light extraction. It is important to note that we did not measure the voltage at 1 kA/cm^2 for the O_2 flow series, however based on the temperature series results, it is likely that the ITO deposited at 1 sccm O_2 flow would only experience a marginal increase in voltage, compared to the lower resistivity samples. Furthermore, comparing the 35 nm film deposited at 30 sccm O_2 and 250 °C, in Figure 81,

to the 18 nm film deposited under the same conditions for the temperature series, shown in Figure 80, we that RMS roughness and grain size are increasing with film thickness, which is consistent with the general observations of ITO crystallization.

4.1.3.3. Multi-Layer ITO Deposition Series

Our primary goal of the deposition temperature series and O_2 flow series was to determine if ITO films with a high transparency and conductivity could be achieved while simultaneously maintaining a low surface roughness of < 1 nm RMS, in order to mitigate scattering losses in the VCSELs. As Figure 80 and Figure 81 show, this cannot be achieved by varying the deposition temperature or O_2 flow alone. Yet, based on the temperature and O_2 flow dependence of the RMS roughness, and the knowledge that very thin films (< 10 nm) deposited at low temperatures (≤100 ^{o}C) tend to exhibit partially or completely amorphous, very smooth surfaces, without a high density of crystalline nucleation sites,[330,331] we can hypothesize that a two-step temperature growth scheme, consisting of a thin layer of ITO grown at a low temperature (LT) of ~100 ^{o}C, followed by a thicker high temperature (HT) ITO layer, grown at ≥ 250 ^{o}C, could promote the growth of large ITO grains with < 1 nm RMS surface roughness, as was observed in the low temperature films (Figure 80), while maintaining the good optoelectronic properties of the high temperature films.

To determine the optimal LT layer thickness, a series of multi-layer ITO films were deposited at 30 sccm O_2 (0.27 mTorr), at a rate of 0.15 A/sec. Each multi-layer film consisted of an LT (100 ^{o}C) layer, followed by a HT (285 ^{o}C) layer. The total thickness was held constant at ~38 nm, while the LT layer thickness was varied from 0.7 nm to 5.5 nm. 38
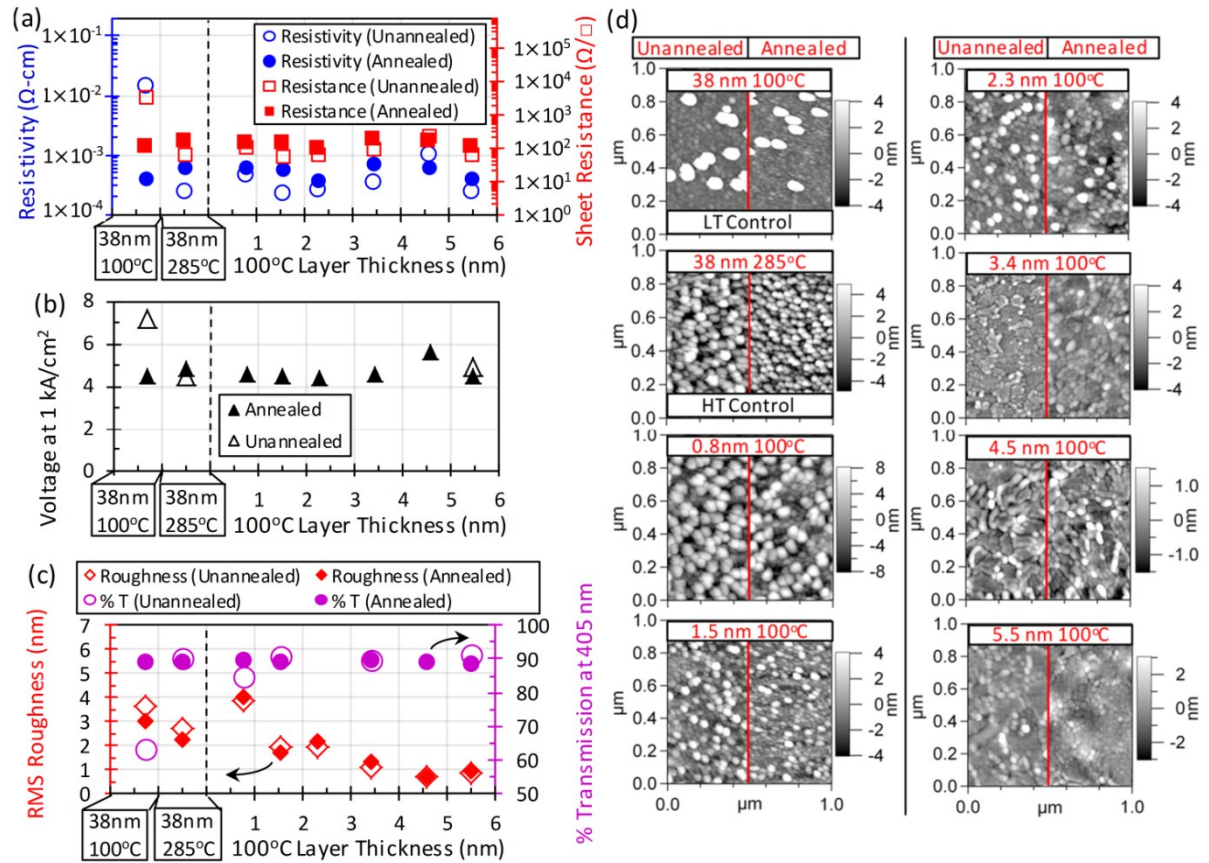
Figure 82 Summary of the dependence of multi-layer (low temp. (LT) + high temp. (HT)) ITO film properties on the LT layer thickness. The LT layer is deposited at 100 °C, while the HT layer is deposited at 285 °C. The total LT+HT layer thickness is held constant at 38 nm. The O_2 flow was 30 sccm (0.27 mTorr). Data is also shown for samples annealed in an N_2 and O_2 ambient at 600 °C, at atmospheric pressure, following the deposition. (a) The resistivity and sheet resistance vs. LT layer thickness, measured on the ITO/DSP sapphire samples. (b) Voltage at 1 kA/cm^2 vs. LT layer thickness, measured on the ITO/m-plane LED samples. (c) The RMS roughness and % transmission at 405 nm vs. the LT layer thickness. In (a), (b), and (c), The LT and HT single-layer control samples are shown on the left side of the plot. In (c), the missing data points are due to the samples being lost before the measurement. (d) AFM images of the ITO/LED samples before and after annealing for the various LT layer thicknesses

nm thick single-layer LT and HT control samples were also deposited. . Figure 82 shows the results of this multi-layer ITO series. For each sample, the resistivity, transparency, and morphology was analyzed before and after ex-situ annealing in an AET Thermal RX Rapid Thermal Annealer (RTA) at 600 °C for 10 min under atmospheric pressure with 6 slm N_2 flow and 1.5 slm O_2 flow. Figure 82(a) shows the sheet resistance and resistivity for each of the samples. Consistent with the temperature series results (Figure 81), the unannealed LT control sample has a high resistivity of 10^{-2} Ω-cm. After annealing, the resistivity was

reduced to the value of the HT control sample and the multi-layer samples. Also of note is the fact that annealing the HT control sample and the multi-layer samples resulted in a small *increase* in the resistivity. Moving to thicker LT layers, we see little change in the resistivity.

Considering the literature, we note that amorphous ITO films deposited at low temperatures generally show a decrease in resistivity upon annealing, due to a large increase in carrier concentration, and a small decrease in mobility, resulting from annealing induced crystallization.[320,329] In contrast, crystalline ITO films are much more sensitive to the annealing temperature, tending toward a slight decrease in resistivity at moderate annealing temperatures (< 300 °C) [329,344] and an increase in resistivity at high annealing temperatures (> 350 °C).[344,345] This is due to the mobility continually decreasing upon annealing as-deposited crystalline films, while the carrier concentration initially increases up to annealing temperatures of ~350 °C, then rapidly decreases above this temperature.[329,344,345] The increase in carrier concentration after annealing at low temperatures is attributed to a marginal increase in crystal quality, while the decrease in carrier concentration at high temperatures is attributed to the segregation of Sn at grain boundaries[329] and/or the reduction in oxygen vacancy concentration and the formation of SnO_x complexes when annealing is performed in the presence of oxygen.[344,345]

Figure 82(b) shows the voltage at 1 kA/cm^2 measured on the ITO/LED samples. The data points for the unannealed samples, shown in Figure 82(b), are from a second set of samples. Overall, the trends are similar to those observed for the resistivity analysis (Figure 82(a)). Specifically, the LT control sample shows an improved voltage upon annealing, while the multi-layer films and the HT control samples show no significant change in the

voltage, suggesting that the contact resistance is not improved by annealing as-deposited crystalline ITO films. Assuming the contact resistance dominates the differential resistance for the 405 nm LED, we approximate the annealed and unannealed 5.5 nm LT layer thickness sample, operating at 4.45 V at 1 kA/cm^2 (~50 mA), to have a specific contact resistivity of ~1.4×10^{-3} Ω-cm^2.

Figure 82(d) shows the AFM images taken on the series of samples before and after annealing. As can be seen, annealing the samples did not result in a drastic change in grain size, though some minor change in morphology can be seen. Comparing the LT control sample to the multi-layer films, we see that the multi-layer films do not exhibit the large crystalline clusters surrounded by amorphous regions, as seen in single-layer films deposited at 100 ^{o}C. This suggests that the initial LT layer crystallizes upon heating the sample to 285 ^{o}C in the chamber. This is supported by annealing experiments reported in the literature[331] which show crystallization of 55 nm amorphous films upon annealing at 300 ^{o}C. We hypothesize that by depositing a thin LT layer, we form a small number of nucleation sites in the LT layer. Upon heating, large grains are able to grow due to the small number of nucleation sites, characteristic of thin LT ITO films generally.[330,331] Once these large grains are formed the high temperature deposited ITO easily crystalizes, rather than forming an initially amorphous layer with many nucleation sites. This results in the formation of large primary grains which grow vertically by consuming the smaller secondary nucleated grains sitting on top of the larger grains. In agreement with this hypothesis, the AFM images shown in Figure 82(d) for the multi-layer films with LT layers between 3.4 – 5.5 nm show a morphology that appears to consist of large primary grains covered with smaller secondary grains.

Figure 82(c) shows the RMS roughness and transmission at 405 nm for the multi-layer ITO films series. As the LT layer thickness increases the RMS roughness gradually drops from 4 nm RMS to < 1 nm RMS for a LT layer thickness of ~ 4.5 and 5.5 nm. Observing the transparency trend shown in Figure 82(c), we note that the thin LT layer has no significant effect on the transparency. The transparency remains on the order of the HT control sample, regardless of the LT layer thickness. Comparing the unannealed and annealed data points in Figure 82(c), it is apparent that the RMS roughness does not change upon annealing. Furthermore, for the HT control sample and the multi-layer films, the transparency does not change significantly upon annealing. However, the LT control sample does show a significant improvement upon annealing, as is expected from amorphous ITO films which crystallize upon annealing.

In the final multi-layer ITO films used in the VCSELs,[10–12] we simplified the LT+HT structures so that the LT layer was deposited at room temperature and the HT layer was deposited at ~400 °C. As our original substrate heater could only reach ~285 °C maximum temperature, this final iteration of the multi-layer ITO film used a commercial heater from

(a) **Multi-layer ITO parameters**

O$_2$ Flow Rate (sccm)	30
Pressure (mTorr)	0.27
Deposition Rate (Å/s)	0.2
25 °C Layer Thickness (nm)	4.4
400 °C Layer Thickness (nm)	39.8
ρ_s (Ω-cm) (UnAnnealed)	5.7E-04
% Transmission at 405 nm	86
Full Area σ_{RMS} (nm)	0.282
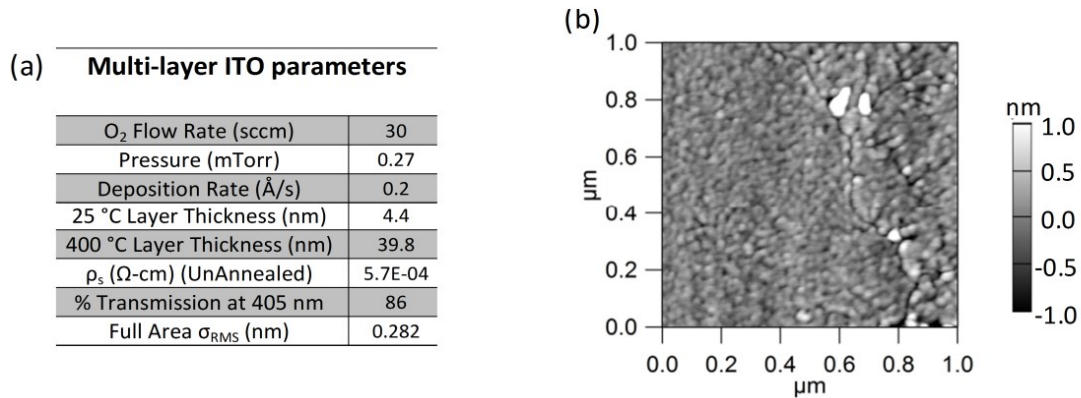
Figure 83 (a) table summarizing the deposition parameters, typical optoelectronic properties, and typical RMS surface roughness for the final multi-layer ITO films used the later generations of nonpolar VCSELs with ITO intracavity contacts.[10–12] (b) AFM image showing the highly smooth nature of the ITO film. The correlation length (avg. spacing between roughness features) is 24.5 nm and the RMS roughness is 0.282 nm.

Heatwave Labs, Inc.. Figure 83 shows a summary of the optoelectronic and morphological characteristics for a representative ITO film used on the recent nonpolar VCSELs with ITO intracavity contacts. In Figure 83(b) we see that the generality of the multi-layer deposition hypothesis is confirmed, as we observe that the primary grain size increased, due to the reduced number of nucleation sites for the LT layer deposited at room-temperature. Furthermore, the optoelectronic properties of this film, stated in Figure 83(a), are equivalent to that of the single-layer HT films.

With this development of the ITO films, we successfully overcame one of the most significant limiting factors in our nonpolar VCSELs fabrication, the difficulty of depositing highly smooth, transparent, and conductive ITO films with a deposition technique (e-beam deposition) that avoids p-GaN plasma damage. Though these films were quite transparent, they still show large absorption coefficient values at 405 nm (~2000 cm^{-1}, Figure 42), due to this wavelength being near to the absorption edge for ITO's bandgap. As was highlighted in Section 3.4.1, this implies that the total internal loss in the violet VCSELs is dominated by the internal loss in the ITO, thus a more transparent intracavity contact was desirable, however such a contact was not available until E. C. Young began investigating MBE grown III-nitride TJs for research projects outside the VCSELs project. Prior to testing these TJs on a device though, we obtained a number of interesting VCSEL results using ITO intracavity contacts and different aperture designs, which are discussed in Section 4.2. Before moving to the discussion of different aperture designs though, we will summarize the initial investigations on the III-nitride TJ intracavity contacts and highlight some potential paths forward for these more recent and more promising intracavity contacts.

4.1.4. III-Nitride Tunnel Junctions (TJs)

III-nitride LEDs with TJ current spreading layers have been reported, and a number of attempts have been made to fabricate III-nitride VCSELs with TJ intracavity contacts, though no lasing was achieved.[288,346–352] Thus, our TJ VCSELs, reported in Refs. 11,12, were the first demonstration of III-nitride TJ intracavity contacts. Though the TJ is an obvious choice for an intracavity contact in a VCSEL, as it has been used in InP-based VCSELs, the 1st generation of III-nitride VCSELs[8,10,14,131–133,171–173,175,177] did not use a TJ because MOCVD grown III-nitride TJs have been shown to have highly resistive contacts.[288,346–349] This is a result of hydrogen repassivation of p-GaN during the MOCVD n-GaN TJ growth, and the intrinsic doping limits of MOCVD grown n-GaN.[353] Additionally, the growth of this n-GaN layer after the p-GaN growth prevents Mg activation, as H does not easily diffuse through n-GaN.[354] Previous reports of TJs in LEDs and resonant-cavity (RC) LEDs, which are generally just failed VCSELs, show an increase in the turn-on voltage and differential resistance, compared to conventional ITO-based current spreading layers. More recently, TJs grown on c-plane GaN have used a thin AlN layer,[355] InGaN layer,[350,351] or GdN nanoislands[352] between the n^{++}GaN and p^{++}GaN layers to reduce the tunneling barrier. These more recent TJs are also grown using MBE, which reduces the potential for hydrogen repassivation and allows activation of p-GaN before regrowth and/or during MBE p-GaN growth. On nonpolar or semipolar planes, the effects of the intrinsic polarization present on c-plane will not be seen by the junction, thus only the InGaN or GdN layers would be expected to enhance performance. For *violet* VCSELs in particular, using an InGaN contact layer is not a good idea, as the layer would probably have an indium composition near to that of the active QWs of the VCSEL, leading to significant absorption

loss. Naturally, aligning a null of the mode to the InGaN contact would minimize this absorption loss contribution, as it does for the ITO intracavity contact, but if one can achieve a good electrical contact without this layer, then that is a more ideal situation.

In our TJ intracavity contacts,[11,12] we use ammonia MBE with solid source effusion cells for Ga and Si, to regrow an n-GaN TJ on the MOCVD growth nonpolar VCSEL epi. structure. Like MOCVD, ammonia MBE uses thermally cracked NH_3 as the precursor for nitrogen in GaN growth. In contrast to MOCVD though, the hydrogen levels present during ammonia MBE growth are much lower ($\sim 10^{-6}$ Torr) and the regrowth does not result in hydrogen passivation of the MOCVD grown p-GaN layers.

The general process for incorporating the TJ into the VCSEL can be seen in Figure 59, where we can see that the TJ can be incorporated into the three primary aperture designs considered in this thesis: the IIA, the PECA, and the BTJ aperture. In our initial test of the TJ, we simply used the IIA design, as it was the only aperture design that was previously tested at that time. The specific processing steps for the IIA+TJ design are stated below, however it is important to note that at the time of this writing, we had a number of samples in-process for testing the BTJ aperture design as well (Figure 78). As is shown in Figure 59, prior to growth of the TJ, the MOCVD p-GaN must be activated. This step is then followed by a mesa etch and the deposition of a Ti/Au hardmask to define the IIA.[10] Following the Al ion implant by Leonard Kroko, the Ti/Au hardmask is removed in aqua regia and a DI water rinse is performed. Next, the samples are prepped for the TJ growth using an acetone, isopropanol (IPA) solvent clean, prior to loading into the MBE, and baking at 400 °C for one hour. The TJ regrowth reported in Ref. 11,12, was performed at 750 °C, as measured by pyrometry. The Ga flux during growth was $\sim 10^{-7}$ Torr with an NH_3 flow rate of 200 sccm.

The presence of a streaky reflection high energy electron diffraction (RHEED) pattern during growth indicated smooth, 2D regrowth of the TJ. For the initial demonstration, the TJ consisted of an n^{++}GaN (39.6 nm)/ n-GaN (39.6 nm)/ n^{++}GaN (39.6 nm)/ n-GaN (22.1 nm) stack (~141 nm total thickness) with the n^{++}GaN layers having a Si concentration of 1.1×10^{20} cm^{-3} and the n-GaN layers having a concentration of 1×10^{19} cm^{-3}, while the MOCVD grown p^{++}GaN (14 nm) had a Mg concentration of ~2.5×10^{20} cm^{-3}. The step-function doping was originally used in an attempt to reduce the free carrier absorption in the TJ by aligning the n^{++}GaN layers to nulls in the mode. However, more recent designs have eliminated this step-function doping, in favor of simply using the n^{++}GaN layers at the start and finish of the TJ (i.e. at the p-GaN contact and at the TJ metal contact interfaces), and a lower doped n-GaN region for the majority of the TJs thickness. The resistivity and carrier concentrations of the n^{++}GaN and n-GaN films has been measured via the Hall method on a set of test samples, where the n++GaN was found to have a resistivity of ~4×10^{-4} Ω-cm, while the n-GaN has a resistivity of ~4.4×10^{-3} Ω-cm.

In a TJ contact the p-GaN, a contact is essentially formed in the same way as it does in an ITO contact to p-GaN. In both the TJ and the ITO intracavity contact, the majority carriers are n-type. To achieve an *effectively* Ohmic contact, one simply needs to dope the n-type contact to p-GaN extremely high, thereby minimizes the depletion width at the p-n junction. This then allows electrons to tunnel across the depletion region of the junction, recombining with holes, thereby yielding charge transport across the junction. It is important to recognize that all p-type contacts are technically Schottky diodes, as there is no metal, transparent conductive oxide (TCO), or semiconductor generally, with a work function large enough to match the work function of p-GaN (i.e. the separation between the vacuum level

and the Fermi-level). In the case of metals, the Fermi-level energy is equal to the conduction band energy, however TCOs are actually just highly (degenerately) doped semiconductors. Thus a TCO contact to p-GaN is technically a TJ, though the term TJ generally refers to a highly doped n-type contact epitaxially grown using a material in the same class (i.e. III-V compounds) as the p-type material that the contact is being made to. In both the TCO and the TJ case, a Schottky diode is formed at the p-n contact junction. By doping the p- and n-type material extremely high, the junction width is minimized until carriers can easily tunnel across the junction, *effectively* forming an Ohmic contact. We highlight the term "effectively", because a truly Ohmic contact refers to a contact in which the work function of the metal making the contact is equal to the work function of the semiconductor to which the contact is being made. A more comprehensive discussion on different current flow mechanisms in different types of contacts can be found in Ref. 356.

To investigate the expected performance of the TJ contacts on the VCSELs, we simulated the TJ/p-GaN junction band structure in SiLENSe. The results of the simulations
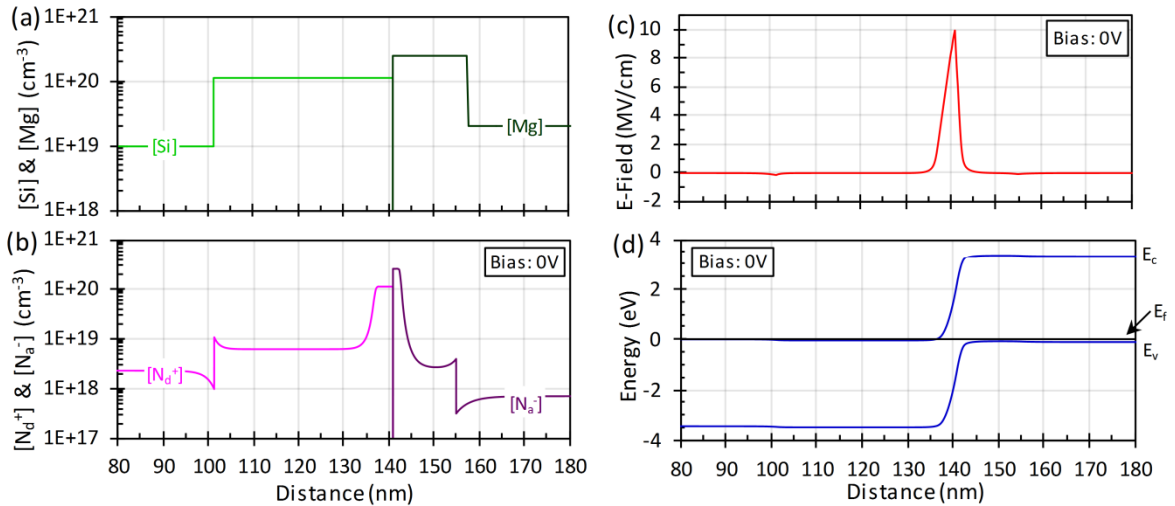
Figure 84 SiLENSe simulations of the TJ employed in TJ VCSELs reported in Ref. 11,12. (a) shows the dopant concentrations for the n-GaN, n^{++}GaN, p^{++}GaN, and p-GaN layers. (b) shows the corresponding ionized donor and acceptor concentrations, assuming a donor ionization energy of 5 meV and an acceptor ionization energy of 165 meV. (c) Electric field vs. position. (d) Band diagram of the TJ contact. The total depletion width is ~7.95 nm, with 6.25 nm of depletion on the n-side.

are shown in Figure 84. Viewing Figure 84(c), we can see that the depletion width is predicted to be ~7.95 nm, with 6.25 nm of depletion on the n-side. This is a large depletion width for a TJ, suggesting that tunneling would not occur in such a junction. However, because the actual TJ VCSEL devices show a fairly small voltage increase (~1.5 V) and no change in the differential resistance compared to the ITO sample processed in parallel (Figure 86), it is plausible that regrowth interface or defect states assist in carrier transport across the junction.[357–359] Also, the SiLENSe simulations predict the electric field at the junction to be two times larger than the breakdown field for GaN (5 MV/cm),[360] which may play some role in the tunneling process. More in-depth experimental investigations of the nature of the charge transport in the MBE-MOCVD hybrid TJs are currently being carried out, led by E. C. Young and B. P. Yonkee. E. C. Young, a staff scientist at UCSB, carried out all TJ growths reported here, as she is an expert in MBE growth. A recent series carried out by B. P. Yonkee and E. C. Young, showed that avoiding the use of cleaning methods that remove native surface oxidation, such as HF solutions, is beneficial, as a high oxygen spike at the TJ/p-GaN interface may be favorable for charge transport. Furthermore, B. P. Yonkee has observed a burn-in effect on TJ contacts for LEDs. Overall, the nature of the TJ charge transport is not well understood at the moment, but it seems quite likely that the electrical performance can be improved to reduce the voltage penalty associated with using a TJ intracavity contact vs. an ITO intracavity contact.

Prior to our original TJ VCSEL demonstration,[11,12] we carried out TMM simulations of ~7λ ITO VCSELs and TJ VCSELs. This allowed us to analyze the potential optical advantages introduced by using a TJ vs. ITO intracavity contact. The longitudinal mode profile and refractive index profile for the two devices is shown in Figure 85. Figure 85(a)
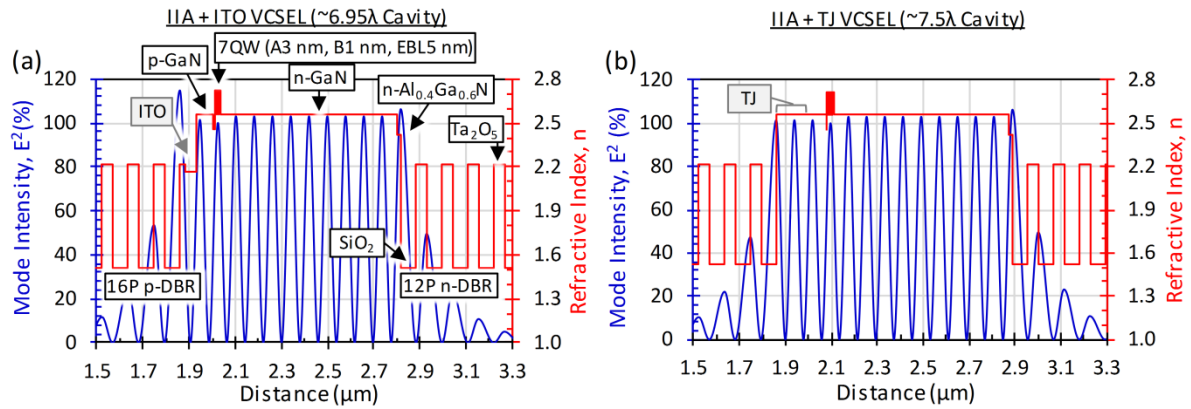
Figure 85 longitudnal mode profile and refractive index profile vs. distance in the central part of the ~7λ VCSELs with 7QW, A3 nm, B1nm, and EBL5 nm designs. (a) shows the VCSEL with an ITO intracavity contact. (b) shows the similar device with a III-nitride tunnel junction (TJ) intracavity contact. In (a), the ¼-wave (46.7 nm) ITO layer is aligned to a null of the mode using the $1/8^{th}$-wave Ta_2O_5 spacer to the left of the ITO. This minimizes the internal loss contribution from the ITO layer. In (b), the TJ layer is composed of alternating layers of highly doped n^{++}GaN and lower doped n-GaN, with the highly doped layers aligned to the nulls in the mode. The total TJ thickness is ~141 nm.

shows the VCSEL with an ITO intracavity contact, while Figure 85(b) shows the TJ intracavity contact. Both structures have 16P p-DBRs and 12P n-DBRs. The effective cavity length is ~6.95λ for the ITO VCSEL and ~7.5λ for the TJ VCSEL, with the structures being designed for 405 nm emission. A detailed table stating the layer thicknesses, assumed absorption coefficients, and the refractive indices for each of the layers in the model can be found in Ref. 11. Using this simulations we calculated the loss introduced by the DBRs (mirror loss, α_m), the intracavity contacts ($\alpha_{i,ITO}$ and $\alpha_{i,TJ}$), all other III-nitride layers ($\alpha_{i,III-nitrides}$), and the threshold modal gain (Γg_{th}). The threshold current density for each of the structures was then calculated using the method described in Section 3.4.1. The results from this simulation can be seen in Section 3.4.1, Figure 74(b), where the modal gain vs. current density for the 7QW, overlaid with the breakdown of the sources of loss in the ITO and TJ VCSELs. In Section 3.4.1, we highlighted the number of QW design implications resulting from the use of a TJ intracavity contact. Here, we will compare the breakdown of the sources of loss in more detail. Starting by considering the threshold modal gain values,

we can see that replacing the ITO with the TJ reduces our Γg_{th} from ~41.6 cm^{-1} to ~14.1 cm^{-1}. Viewing the breakdown of the sources of loss more closely, we see that for the ITO VCSEL the internal loss from the ITO is ~20 cm^{-1} higher than the internal loss from the III-nitride layers, implying that the intracavity contact contributes to ~74 % of the total internal loss. In contrast, the internal loss from the TJ is lower than the internal loss from all other III-nitride layers. Overall, this reduces the simulated threshold current density from ~7.2 kA/cm^2 for the ITO VCSEL, to ~3.2 kA/cm^2 for the TJ VCSEL. It is interesting to note that these values are actually in good agreement with the J_{th} values for the final ITO and TJ VCSELs processed in this study (Figure 86), where we see a J_{th} of ~3.5 kA/cm^2 for the TJ VCSELs and ~8 kA/cm^2 for the ITO VCSEL.

Beyond the improvements in Jth that a TJ design offers, we also expect a large improvement in differential efficiency. Using Eqn. (4), where the fraction of light-emitted out the top-side of the device is calculated to be 99.989 % (Eqn. (6)), and assuming an injection efficiency of 65 %, we calculate the TJ VCSEL to have a top-side differential efficiency ($\eta_{d,top}$) of ~3 %, whereas the ITO VCSEL has an $\eta_{d,top}$ of ~1.1 %. These values are actually much greater than what is observed experimentally, which may be a result of the filamentary lasing in the aperture, poor current spreading in the aperture, or weak modal confinement from the IIA design.

The previous discussion on the advantages of TJs has focused on the particular case of violet (405 nm) VCSELs, however because III-nitrides could be used to fabricate UV, blue, or green VCSELs, it is also important to consider the TJ advantages for these wavelengths as well. Observing the ITO absorption spectrum in Figure 42(e) it is easily recognized that devices emitting in the UV regime (< 390 nm) will suffer from

catastrophically high ITO absorption losses, make a III-nitride (n-AlGaN) TJ critical to achieving efficient UV VCSEL. For devices emitting in the blue (450 nm) or green (525 nm) regime, the advantages of the TJ are less obvious due to the significantly lower absorption loss for ITO (Figure 42(e)). Furthermore, the longer emission wavelength and lower refractive index implies that the physical thickness of the ¼-wave ITO layer is greater than that of ITO in violet VCSELs, making the spreading resistance of the intracavity contact lower for blue and green VCSELs. However, although these longer wavelengths do not suffer from the same degree of ITO absorption loss as violet VCSELs, the ITO thickness is still limited to a ¼-wave thickness. In contrast, using a TJ gives much more leverage over device design, while simultaneously reducing the internal loss, as one can grow a very thick TJ without introducing catastrophically high levels of loss. This is essentially due to the majority of the TJ layer being composed of relatively low doped n-GaN, which has lower absorption than p-GaN and ITO. Considering that the electrical resistivity of the TJ layer is an order of magnitude lower than that of ITO, using a thicker TJ is also advantageous for reducing the spreading resistance across the aperture. In our initial demonstration of a TJ VCSEL, the sheet resistance of the TJ intracavity contact is likely somewhat larger than that of the ITO intracavity contact, however in our next generation of devices (Figure 78) we plan to more than double the TJ thickness in an effort to improve the current spreading.

Beyond these electrical benefits of using a TJ, we may also achieve significant thermal improvements, particularly in the case of dual dielectric DBR VCSELs. In Section 1.4.4.3 and Section 1.4.5.2, we discussed some simple thermal models that compared the thermal performance of ITO VCSELs, TJ VCSELs, and TJ VCSELs with different cavity thicknesses. In Figure 48 the ~7λ TJ VCSEL was shown to dissipate heat slightly more

effectively than the ~7λ ITO VCSEL. However, the most significant improvement in thermal dissipation was achieved by increasing the cavity thickness from a 7λ cavity, to a 23λ cavity, as is shown in Figure 53. This implies that maximizing the total thickness of the p-GaN and intracavity contact layer will minimize the lateral thermal spreading resistance. In the case of an ITO VCSEL, one should increase the p-GaN thickness to improve heat dissipation. Unfortunately, this has the trade-off of significantly increasing the loss due to p-GaN's notoriously high absorption coefficient, compared to n-GaN.[147,161,162] In the case of the TJ, one can maintain a thin p-GaN layer, while increasing the TJ n-GaN thickness to improve thermal dissipation.

Finally, TJs are also advantageous because they open the door for some new VCSEL designs. The BTJ design has been discussed throughout this thesis, however TJs also allow the fabrication of bipolar cascade (BC) III-nitride VCSELs, which could lead to significant improvements in III-nitride VCSEL output powers.[259,361–363]

In first experimental investigation of the TJ VCSEL, reported in Ref. 11, we compared an IIA+ITO VCSEL and an IIA+TJ VCSEL with active region designs of 7QWs, A3 nm, B1 nm, and EBL5 nm for each design. As mentioned previously, a higher number of QWs may be more optimal for ITO VCSELs, due to the higher loss, however using the same number of QWs for this study allowed us to eliminate any device performance changes resulting from using different active region designs. Previous ITO VCSELs we processed had 10QW designs, however the 7QW ITO VCSELs processed in this study actually turned out to be the best performing ITO VCSELs we had achieved to that date, which could be a result of the 10QW design being unable to effectively populate all the QWs, though a more systematic study is necessary to determine the validity of this statement. Figure 86 shows
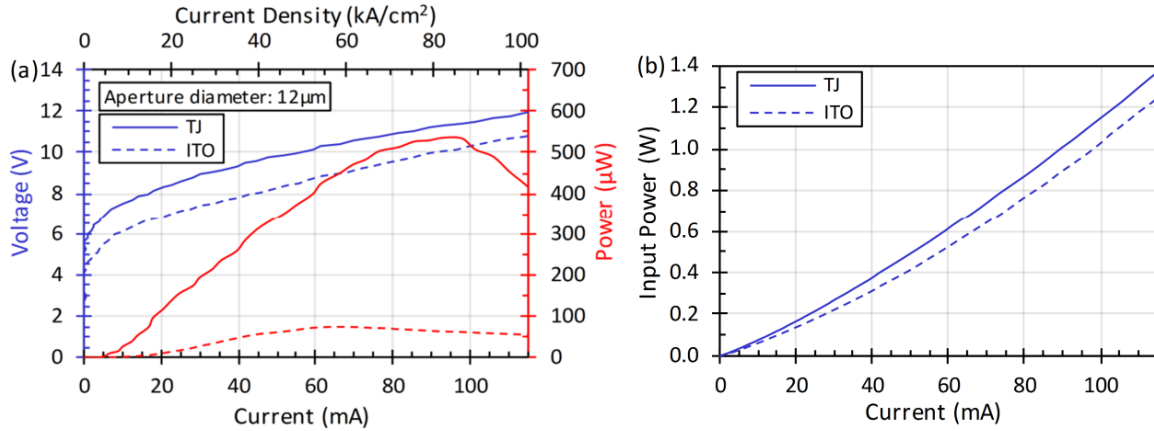
Figure 86 LIV and LJV characteristics of the ~7λ TJ VCSEL and ITO VCSEL with 12 μm aperture diameters measured under pulsed operation (0.3% duty cycle, 100ns pulse width). The ITO VCSEL shows a threshold current of ~9 mA (8 kA/cm^2), while the TJ VCSEL shows a threshold current of ~4 mA (3.5 kA/cm^2). The TJ VCSEL shows significantly higher differential efficiency due to the large reduction in internal loss, however the TJ results in an ~1.5 V increase in the forward voltage.

the LIV characteristics for the IIA TJ and ITO VCSELs measured under pulsed operation (0.3% duty cycle, 100 ns pulse width) at room temperature. Viewing Figure 86(a), We see a ~1.5 V increase in the voltage going from the ITO VCSEL to the TJ VCSEL. Comparing the differential resistance (R_d) for each device, we see that the TJ does not add any series resistance to the device (R_d = 37 Ω), which is in contrast to what is observed in the literature.[288,346–352] Viewing Figure 86(b), we see the input power vs. current for the 12 μm aperture diameter devices. This figure more clearly shows that slightly above threshold for both device (20 mA), there is little difference in the input power for the ITO VCSEL and the TJ VCSEL. At higher currents, the input power of the TJ VCSEL diverges from that of the ITO VCSEL, but overall the difference remains relatively small.

Considering the threshold current density of the two devices (Figure 86(a)) we see that the J_{th} is reduced from 8 kA/cm^2 (9 mA) for the ITO VCSEL to 3.5 kA/cm^2 (4 mA) for the TJ VCSEL. The TJ VCSEL shows a differential efficiency of 0.262 %, while the ITO VCSEL has a differential efficiency of 0.062 %. Both of these values are much lower than what is predicted by simulations, however this is commonly observed in III-nitride

199

VCSELs.[8,10,14,131–133,172,173,175,177] It is likely that this large discrepancy in the differential efficiency is due to the filamentary nature of the lasing in the aperture, non-uniform current spreading, and/or weak modal confinement in the IIA design.

The emission spectra for the two devices, as a function of current density, are shown in Figure 87. The lasing wavelength is seen to be 410 and 417 nm for the ITO and TJ VCSEL, respectively. Both devices were initially designed for lasing at 405 nm, however during the fabrication we wanted to test a method for tuning the cavity resonance wavelength by analyzing the resonance wavelength in the spontaneous emission prior to depositing the n-DBR, then adding a Ta_2O_5 spacer to the n-DBR to shift the resonance wavelength if the spontaneous emission spectrum showed it to be too short. Unfortunately, we forgot to account for the effective penetration in the n-DBR adding to the cavity length
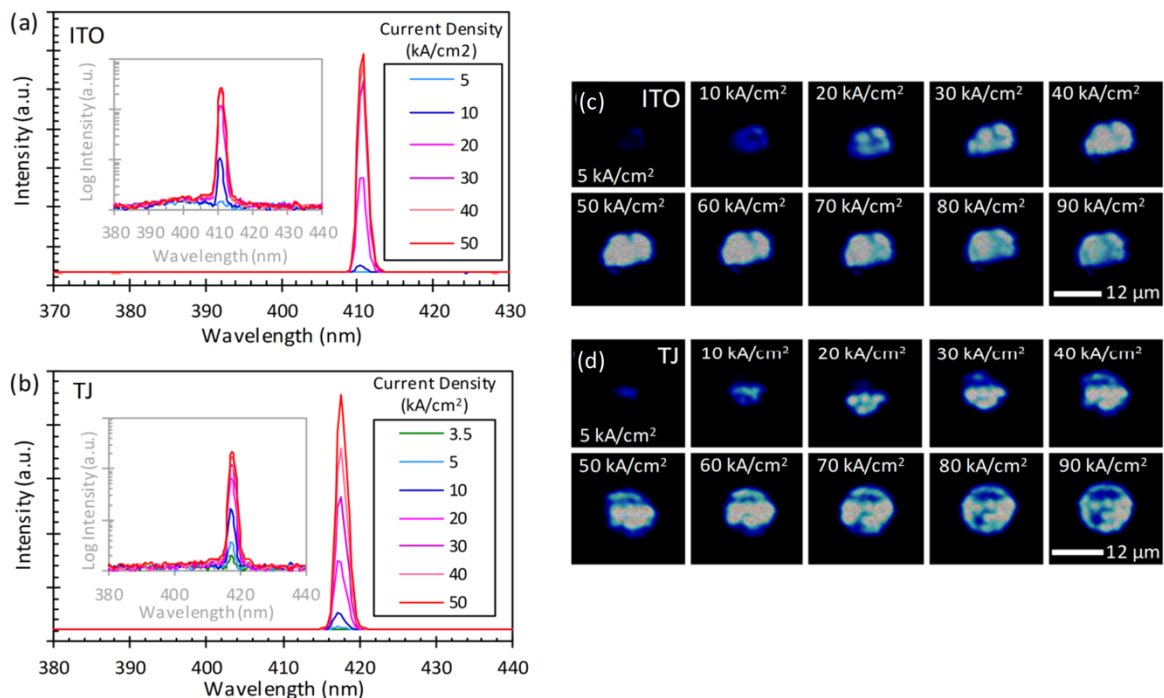
Figure 87 (a) and (b) show the emission spectrum vs. current density for the IIA+ITO VCSEL and the IIA+TJ VCSEL, respectively. The devices were designed for 405 nm emission, but a Ta_2O_5 layer was added to the start of the n-DBR, shifting the cavity resonance to longer wavelengths. (c) and (d) show the near-field emission profiles, imaged with a CCD optical microscope camera, for the ITO VCSEL and TJ VCSEL, respectively. Both devices show filamentary lasing in the aperture.

once the n-DBR is in place. This led us to believe that the cavity thickness would be shorter than it actually would be in the final device, causing us to incorporate an unnecessarily thick Ta_2O_5 spacer at the start of the n-DBR, which then resulted in the resonance wavelength being shifted away from 405 nm. In general, we have referred to this as an "accidental" or "unintentionally" incorporation of a Ta_2O_5 spacer layer, because of the somewhat tangential discussion necessary to describe why the Ta_2O_5 spacer layer itself was not actually accidentally incorporated, but that the layer was accidentally made too thick. In general, this method for analyzing the cavity resonance wavelength prior to the n-DBR deposition is certainly feasible; however one must be careful to account for the added effective penetration depth once the n-DBR is in place. This particular method of shifting the cavity resonance wavelength could be useful for analyzing the optimal gain offset parameter by processing a series of samples with the same peak gain wavelength, then using the Ta_2O_5 spacer on the n-side of the device to shift the cavity resonance wavelength slightly for each VCSEL. On a related note, in Figure 87(a) and (b), we can imagine that this shift of the cavity resonance wavelength may have also led to a misalignment of the peak gain and the cavity resonance wavelengths, which can lead to an increase in the threshold current density. That being said though, a systematic experimental study investigating the optimal gain offset parameter has not been carried out, so perhaps the gain offset in these devices was actually beneficial. Both devices show a spectrometer resolution limited FWHM of ~2 nm and a slight increase in the peak wavelength with increasing current (~0.005 nm/mA).

In Figure 87(c) and (d) we see optical microscope (near-field) images of the ITO and TJ VCSEL, taken as a function of current density for both devices. The ITO VCSEL (Figure 87(c)) and the TJ VCSEL (Figure 87(b)) both display filamentary lasing. This filamentation

results in large areas of the aperture not contributing to the stimulated output power. The origin of this filamentation is not well understood, however in our report on the demonstration of an IIA VCSEL,[10] we eliminated a number of potential sources, suggesting that it may be a result of non-uniform current spreading, contact resistance, absorption loss, and lateral index fluctuations. In the case of the ITO VCSEL, the polycrystalline nature of the ITO was proposed to be a possible cause of a spatially varying absorption loss,[10] leading to filamentation. However, here we see filamentation in the ITO VCSEL *and* the TJ VCSEL, where the TJ VCSEL is epitaxially grown, and thus the filamentation is not likely to be a result of spatial variations in the intracavity contact absorption loss. Related to this is the consideration of variations in contact resistance and current spreading (local current density) across the aperture. The polycrystalline nature of ITO contacts makes it possible for the contact resistance to vary from grain to grain. Additionally, recent investigations on the MBE regrown TJs employed here have shown large variations in the emission intensity across large area LEDs employing such TJs. Thus, for the ITO and TJ intracavity contacts, local variations in the contact resistance may play an important role in filamentation. With a variation in contact resistance, one would expect a local variation in current density and heating, inducing a change in the local refractive index and loss, which may then induce filamentary lasing. In early reports on GaAs-based lasers, filamentary lasing was also observed, which was predominantly attributed to local built-in gain (loss) and refractive index variations.[364] Considering our more recent results on an ITO VCSEL with a PECA design,[13] it is evident that one can suppress the filamentation effect by using an aperture design that provides a large core-cladding index contrast, making the laser effectively index guided, rather than gain guided, as it is in the case of the IIA design. This implies that we

now have an effective way to engineer around the filamentation effect, however the actual cause and nature of the filamentation is still unknown and more rigorous investigations into this phenomenon are necessary to fully understand its origin.

Evidently, TJs are the best intracavity contact for any III-nitride VCSEL. However, thus far we have only investigated $\sim 7\lambda$ VCSELs with ~ 141 nm TJs. As was shown in Section 1.4.5, using a 23λ cavity design may be the key to enabling CW nonpolar VCSELs. In Figure 78 we showed a DOE that involved testing 23λ TJ VCSELs with ~ 1642 nm TJs. At the time of this writing, these samples were in-process, however we have observed some interesting potentially challenges presented by moving from a thin MBE growth TJ to a thick TJ. Specifically, in Figure 88(a), we see a confocal microscope image (take in laser scanning mode) of the 23λ TJ VCSEL before (left) and after (right) growth of the ~ 1642 nm TJ. We see a significant change in the surface morphology upon growth of the TJ. Measuring this surface under AFM (Figure 88(b)), shows that the TJ has a morphology composed of crystallographically oriented striations. Fortunately, these striations are
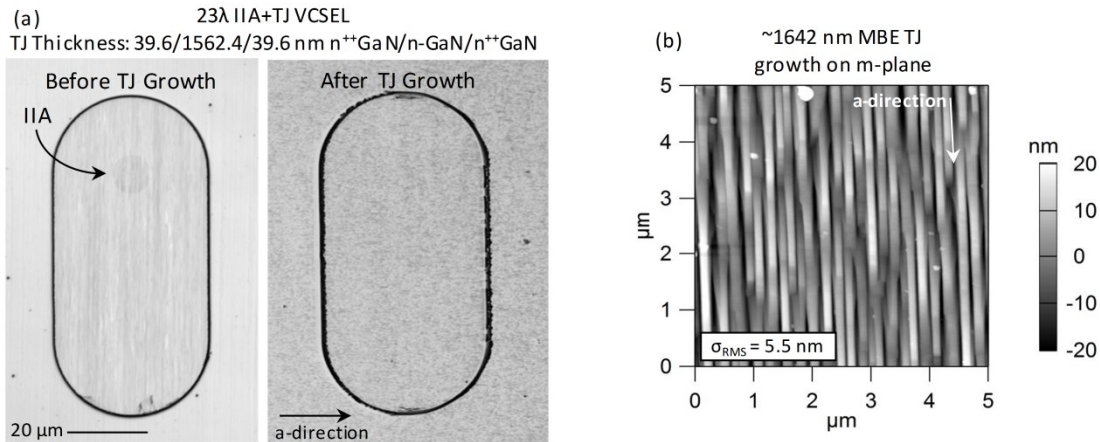
Figure 88 (a) confocal microscope images of a partially processed 23λ IIA+TJ VCSEL before the TJ growth (left) and after the TJ growth (right). The thick TJ (~ 1642 nm) can be seen to introduce significant roughness to to the surface. (b) shows an AFM image taken on the mesa after the TJ growth. The crystallographically oriented striations are a result of the optimal m-plane miscut being different for MBE and MOCVD growth. These striations were not observed on the thinner (~ 141 nm) TJs.

oriented parallel to the a-direction, which is the same direction of polarization on m-plane, thus they may not introduce catastrophic levels of scattering loss. These striations are a result of the difference in growth regimes for MOCVD vs. MBE, which results in a difference in the optimal miscut for m-plane substrates for MBE growth vs. MOCVD growth.[215,216] This phenomenon has not been studied in great detail, and is certainly an interesting area for future research.

In summary, we analyzed some of the growth challenges to achieving III-nitride TJ intracavity contacts, prior to delving into the details of why TJs are advantageous to ITO intracavity contacts. Specifically, we highlighted the improvements in current spreading, threshold modal gain, threshold current density, differential efficiency, and thermal dissipation, offered by a TJ design. It is apparent that TJs are the ideal intracavity contact for III-nitride VCSELs, but there is still a great deal of work necessary to determine the optimal growth procedure and TJ thickness (i.e. cavity thickness) for achieving efficient CW operation of III-nitride VCSELs.

4.2. Aperture Design & Diameter

The final critical parameter in a VCSEL is the aperture design and the aperture diameter. In Figure 59 we outlined the basic process steps for 3 different kinds of aperture designs: (1) the ion implanted aperture (IIA), (2) the photoelectrochemical (air-gap) aperture (PECA), and (3) the buried tunnel junction (BTJ) aperture. In this section we will go into more detail on the development of these different kinds of apertures. Historically speaking, the original VCSELs from our group used dielectric (SiN_x) apertures.[8,14,15] These demonstrations were followed by the development of the IIA,[10] which was used to

demonstrate the first TJ VCSEL.[11,12] In parallel with the first IIA+TJ VCSEL samples, we also processed the first PECA+ITO VCSEL samples, reported in Ref. 13. Finally, motivated by the BTJ micro-LED, reported in Ref. 287, and by the IIA+TJ VCSELs excellent performance, we began processing a set of BTJ VCSELs, which were still in process at the time of this writing. These BTJs simply use an n++GaN contact and an n-GaN regrowth layer, however, we now believe that using an n++GaN contact with an n-AlGaN regrowth layer could possibly yield the best possible aperture design for III-nitride VCSELs generally. This is because forming a BTJ with an n-AlGaN regrowth layer would allow one to introduce a core-cladding index contrast to the device, assisting in index-guided lasing, while simultaneously overcoming the structural complications involved in using an air-gap aperture. In the section to follow, we will go through the details on the developments of the IIA, PECA, and BTJ aperture, while simultaneously analyzing some of the preliminary studies investigating the lasing performance vs. aperture diameter and number of n-DBR mirror periods

4.2.1. The Ion Implanted Aperture (IIA)

In III-nitride VCSELs, four methods have been demonstrated for defining the aperture: (1) using a dielectric (SiN_x[8,14,15] or SiO_2[132,171–173,175,179,277]), (2) using p-GaN passivation,[180] (3) using ion implantation (Al[10–12] or B[174,180]), and (4) forming air-gap aperture using PEC etching.[13] The earliest experimental reports on III-nitride VCSELs generally used the dielectric aperture design, due to its simplicity. However, simulations from a number of groups have shown that the standard dielectric aperture suffers from poor lateral confinement and may actually introduce additional loss to the mode.[200,201,365] In Refs.
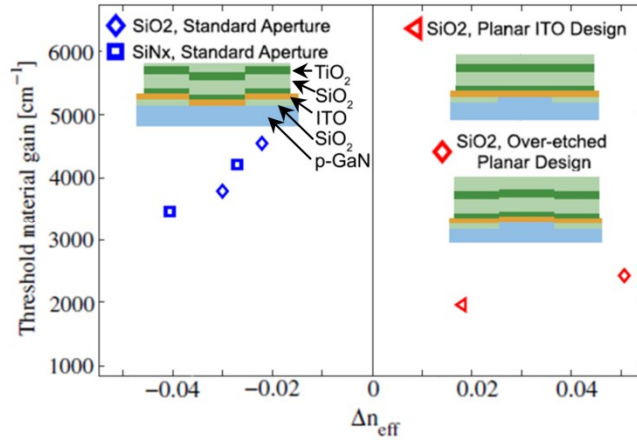
Figure 89 Simulations of the threshold material gain vs. effective index contrast, Δn_{eff}, for different aperture designs. The left side of the plot, where $\Delta n_{eff} < 1$, shows the case of a standard dielectric aperture, while the right side shows a planar ITO design. In these simulations, the planar ITO design is formed by etching into the p-GaN outside the aperture, prior to depositing the dielectric layer.[200]

198 and 199 in particular, the authors show that by switching from a dielectric aperture design with a step (resulting from the dielectric layer) from outside to inside the aperture, to a configuration with a planar ITO design (i.e. no step from within the aperture to outside the aperture) can reduce the threshold modal gain. These results are summarized in Figure 89,[200] where we can see reduction in the threshold material gain by moving from a standard dielectric aperture design, where there is a step in the ITO layer at the aperture (due to the dielectric layer), to a planar ITO design. In this particular report, the authors chose to simulate the case of a planar ITO design being achieved by etching into the p-GaN layer outside the aperture, then depositing a dielectric layer of the same thickness as the etch depth, prior to depositing the ITO intracavity contact. This illuminates the importance of a planar ITO design, however, processing a sample in this way can be challenging, as the etch into the p-GaN could damage the p-GaN within the aperture itself, particularly in the areas around the edge of the aperture, and it could also creat rough sidewalls at the edge of the aperture, which could then lead to scattering loss. For this reason, we sought to develop an alternative method for obtaining a planar ITO design. In Ref. 166, G. Cosendey, et al. used

p-GaN passivation (i.e. exposed the p-GaN outside the aperture to RIE plamsa) to define the aperture, thus we attempted to reproduce these results at UCSB. In our original VCSELs, the devices reached threshold at ~10V, thus we decided that producing a p-GaN passivated layer with a Schottky-diode breakdown voltage of ≥ 20 V, would provide sufficient insulation to prevent any leakage through the passivated area. An extensive optimization of the p-GaN passivation parameters was carried out using an RIE and ICP tool, however none of the tested conditions prooved to yield sufficient insulation. Furthermore, the p-GaN damage was observed to be healed during the flip-chip bond process, making such an aperture design particularly problematic for flip-chip devices. Thus, we moved on to try using Al ion implantation to form the aperture and simultaneously achieve a planar ITO design.

Al ion implantation has been employed in c-plane resonant cavity LEDs[366,367] and current aperture vertical electron transistors (CAVETs).[368] Recently, boron ion (B[++]) implantation has also been used to define the aperture for c-plane VCSELs.[174,180] To gain insight into the expected Al ion implant depth, we performed Stopping Range of Ions in Matter (SRIM) simulations, the results of which are shown in Figure 90(a). Based on these simulations, we chose to initially test defining the aperture using ion energies of 45-60 keV. The implantation was performed by Leonard Kroko, Inc.. Unfortunately, these high energies resulted in a >1 V increase in the turn-on voltage, or prevented turn-on entirely, for the partially processed VCSELs tested. This is in contrast to the simulations, which predict a lateral straggle of ≤ 50 nm. The increased straggle length, observed experimentally, could be due to enhanced lateral straggle along the core of the c-axis, which lies perpendicular to the implant plane. However, more recent studies by S. G. Lee suggest that even the longitudinal (vertical) projected range and/or straggle is much greater than what is predicted
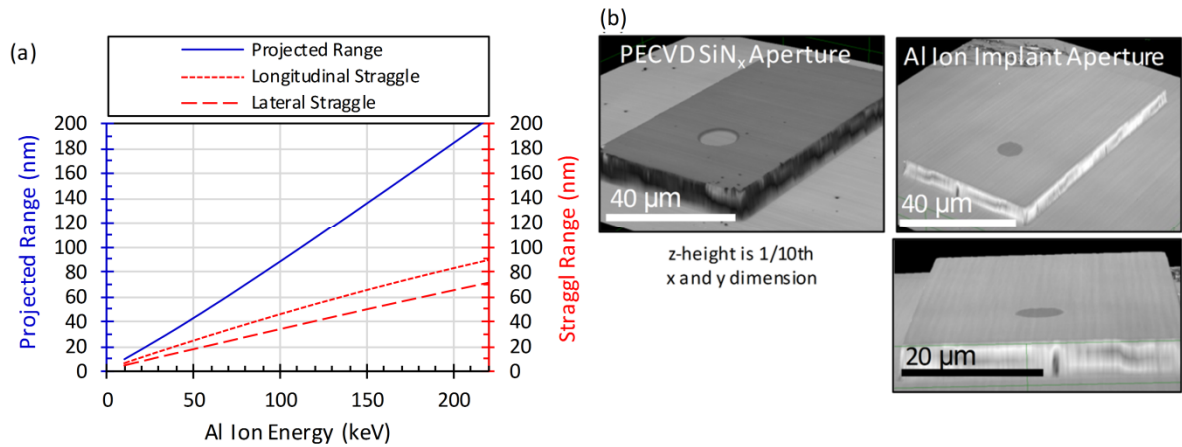
Figure 90 (a) SRIM simulation results of the projected range and straggle range for Al ion implanted ions in GaN. The Al ion dose is ~10^{15} cm^{-2} and the implant is performed with a normal incidence angle. The projected range refers to the depth at which the implanted ion concentration peaks, while the straggle refers to the approximate distance past the projected range that ions are implanted to. (b) shows confocal miscrope images (laser scanning mode) of the standard PECVD SIN$_x$ aperture (left) and the Al ion implanted aperture (right). The Al ion implanted aperture is yields a planar surface, allowing for a planar ITO design.

by SRIM simulations. Following these initial failed tests, a series of samples were processed

with 10, 20, and 30 keV Al ion implantation energies. The ion dose was 10^{15}cm^{-2}, and the

implant was performed at normal incidence. In parallel with these samples, we also

processed a sample with a standard SiNx aperture, deposited using plasma-enhanced-

chemical-vapor deposition (PECVD). Figure 90(b) shows scanning confocal microscope

images of the PECVD SiN$_x$ aperture sample and the ion implant aperture sample (20 keV)

after the aperture is formed. Here, we can see that the ion implant does indeed result ion no

height change at the edge of the aperture, allowing for a planar ITO design. Following the

deposition of the ITO intracavity contact, Cr/Ni/Au p-pad, and a Ti/Au blanket backside n-

contact, we measured the IV characteristics on a number of 10 μm aperture diameter

devices. The results are shown in Figure 91(a), where we compare the PECVD SiN$_x$ aperture

(used previously)[8,14] to the ion implanted aperture on partially processed VCSELs (prior to

the p-DBR deposition and flip-chip bond). The SiN$_x$ aperture shows a ~1 V increase in

voltage. This is a result of plasma damage to p-GaN caused by the PECVD process.[166,283–]
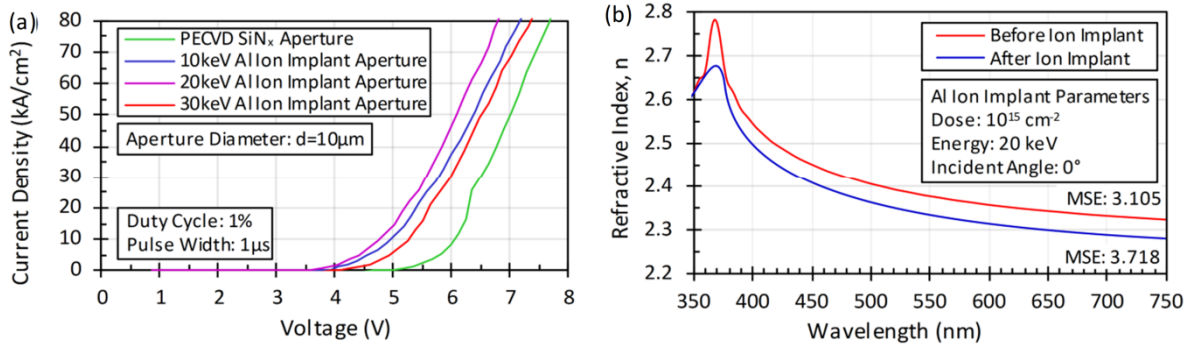
Figure 91 (a) IV characteristics measured on half-processed VCSELs (after ITO p-pad deposition), comparing a SiN$_x$ aperture to an IIA formed using various Al ion energies. The implant was performed at normal incidence with an Al ion dose of 10^{15}cm^{-2}. The SiN$_x$ aperture shows the highest turn-on voltage. (b) Refractive index of a free-standing m-plane GaN substrate, measured using ellipsometry, before and after ion implantation. Both measurements show a low mean-square error (MSE). The implant decreases the refractive index.

[285,293] The IV characteristics of apertures defined by 10, 20, and 30 keV implants show no clear trend, thus a 20 keV implant was chosen to reduce the potential for carrier leakage, while simultaneously decreasing the chance of lateral straggle.

Following the analysis of the IV characteristics, we sought to analyze the optical properties of the IIAs. To do this, we performed an ellipsometry measurement on a bare m-plane substrate before and after Al ion implantation at 20 keV. The results are shown in Figure 91(b). Here, we see the refractive index decreased upon implantation, which is generally favorable for providing optical confinement in the aperture. At 405 nm, there is a ~2% reduction in the index. Assuming the implantation reduces p^{++}GaN index from 2.557 to 2.510, we calculate an effective index within the aperture (avg. core index) of 2.35 and an effective index outside the aperture (avg. cladding index) of 2.349. Using FIMMWAVE,[192] we simulate the lateral confinement for the LP_{01} mode as a function of aperture diameter, as is shown in Figure 92(a). This simulation uses a simple 2D core-cladding model, as would be used to simulate an optical fiber. In Figure 92(a), the lateral confinement factor (Γ_{xy}) drops below 90 % when the aperture diameter is reduced to < 6 μm. For the case of a 12 μm aperture, the lateral confinement factor is 98 %. To analyze the modal confinement for

209
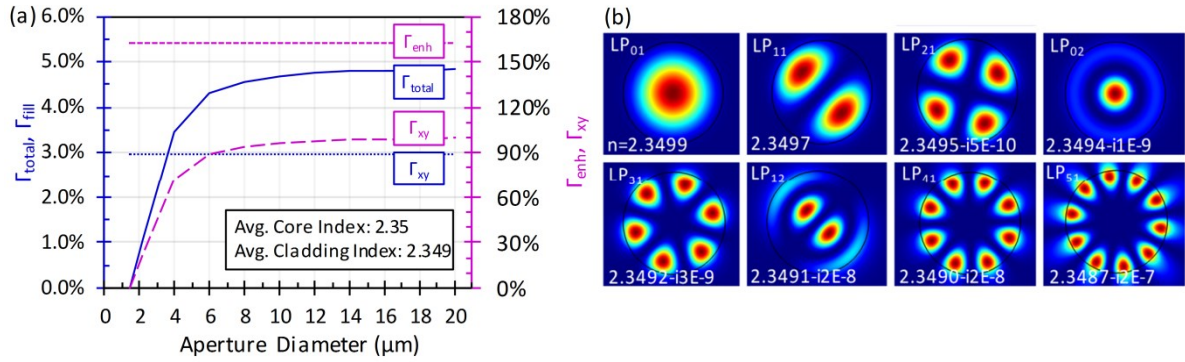
Figure 92 (a) Simulated total confinement factor (Γ_{total}), fill factor (Γ_{fill}), enhancement factor (Γ_{enh}), and lateral confinement factor (Γ_{xy}) vs. aperture diameter for a ~7λ 405 nm IIA+ITO VCSEL. The enhancement factor and fill factor are calculated using a 1D TMM model, while the lateral confinement factor was calculated using FIMMWAVE for the LP_{01} (fundamental) mode. The small core-cladding index contrast results in weak confinement of the LP_{01} mode for devices with < 10 μm aperture diameters. (b) 2D COMSOL simulation of the variation LP modes effectively confined in an 12 μm IIA VCSEL. The imaginary component of the mode index implies that the mode is leaking out of the core region (i.e. that particular mode has a low confinement factor). The simulation uses the "Electromagnetic Waves, Frequency Domain" physics module.

different LP_{lm} modes, we used a 2D COMSOL simulation using the "Electromagnetic Waves, Frequency Domain" physics module. We simulated the case of a 12 μm aperture. Figure 92(b) shows the various LP mode profiles that are reasonably confined to the cavity. The mode index for each mode is shown. As can be seen, only the LP_{01} and LP_{11} mode have a purely real index. Beyond the second LP mode, the modes have an increasingly large imaginary index, implying that they are not completely confined to the core of the cavity. This weak confinement of higher order modes is likely why the IIA VCSELs show a rollover even when they are driven with extremely short pulse widths (100 ns). More specifically, in many of the IIA VCSELs, one can see multiple kinks in the output power above threshold. Each kink indicates the switching to and/or turning-on of a higher order LP mode (Figure 57). In the 12 μm aperture diameter IIA+ITO VCSEL in Figure 99, in particular, one can see a kink at ~35 kA/cm^2, which is likely a result of the switching from the LP_{01} mode to the LP_{11} mode. At ~65 kA/cm^2, the output power begins to roll-over,
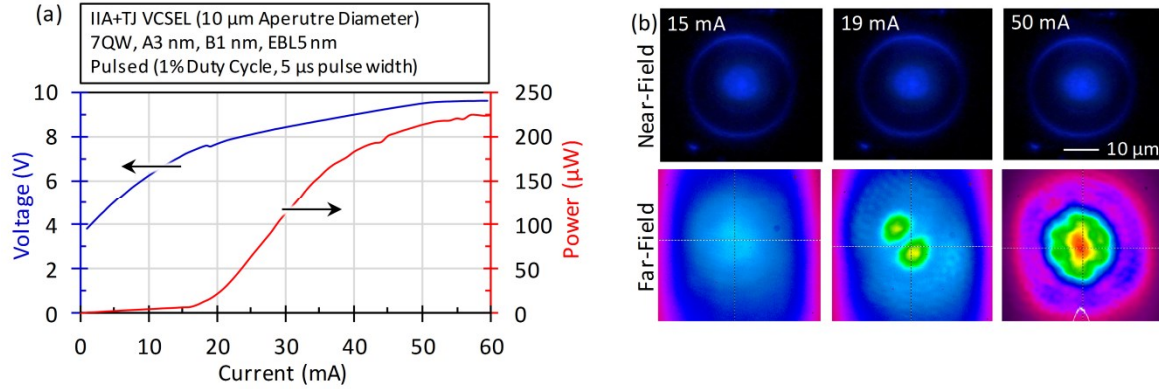
Figure 93 (a) LIV data from a 10 μm aperture diameter IIA+TJ VCSEL (7QW, A3 nm, B1 nm, EBL5 nm) driven under pulsed operation. Measurements were taken at 15 °C. The device was on the same chip as those reported in Refs. 11,12. (b) near-field and far-field profiles of the IIA+TJ VCSEL driven at 15 mA, 19 mA, and 50 mA. Each near-field profile, taken through microscope lens coupled to a CCD camera, shows a relatively small degree of filamentary lasing commonly observed in III-nitride VCSELs. In contrast, the far-field image, captured by placing a beam-profiler (large-area CCD) directly over the VCSEL, shows distinct mode profiles, with the LP_{11} mode being clearly visible at 19 mA. The 50 mA far-field profile appears to show multiple LP modes lasing simultaneously. The discrepancy between the near-field and far-field profiles is not well understood at this time. This device was also used to perform the first modulation bandwidth measurement on a III-nitride VCSEL. These results can be seen in Figure 11.

implying that the next highest order mode (LP_{21}) does not turn-on, which is not surprising because it has an imaginary mode index in the COMSOL simulations (Figure 92(b)). Furthermore, this rollover is likely not a result of heating because this device was measured under pulsed operation with a 0.03 % duty cycle and a 300 ns pulse width. It is relevant to this discussion to mention that all IIA VCSELs fabricated by our group have shown near-field emission profiles that are filamentary in nature. However, we recently analyzed the far-field profile of an IIA+TJ VCSEL and observed a well-defined LP mode. Figure 93 shows the LIV, near-field, and far-field profiles for this 10 μm aperture diameter device. Viewing Figure 93(b), we can see that at 19 mA, the far-field profile clearly shows the LP_{11} mode, but no clear mode profile can be seen in the near-field profile. Viewing the 50 mA far-field profile, it is apparent that multiple LP modes are lasing simultaneously, with the LP_{31} mode possibly being the highest order mode in the device. The reason for this large discrepancy in the near-field profile and the far-field profile is currently under investigation. Regardless

though, the results highlight the importance of measuring both the near-field and far-field profiles in III-nitride VCSELs.

Following the optimization of the IIA conditions, we fabricated a complete nonpolar VCSEL with a ~7λ cavity and an ITO intracavity contact. The results from one of the first IIA+ITO VCSELs we successfully fabricated are summarized in Figure 94, where the VCSEL geometry is schematically shown in (a), the cavity and refractive index profiles are shown in (b), the LIV characteristics are shown in (c), and the emission spectrum is shown in (d). Comparing Figure 94(a) to the VCSEL schematic shown in the process flows
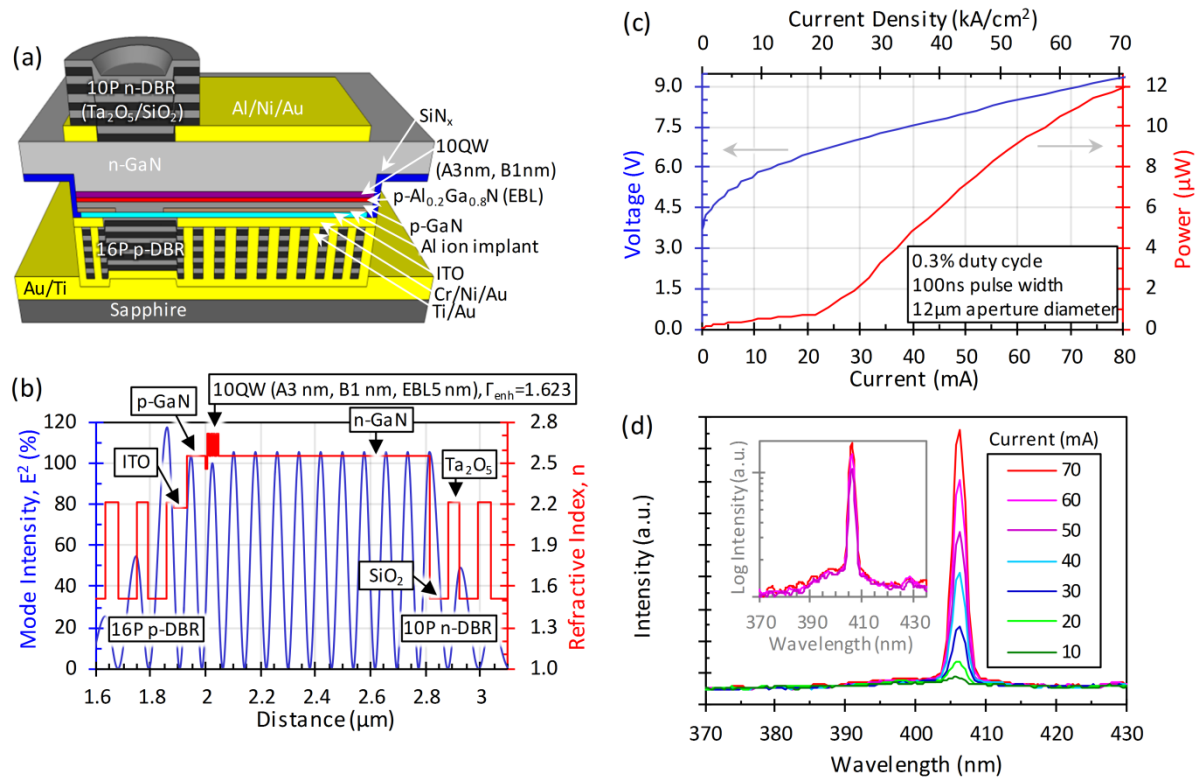
Figure 94 (a) Schematic of one of the first IIA+ITO VCSELs. The aperture is defined by the Al ion implant into the p-GaN layer, allowing for a planar ITO design, as shown in the schematic. (b) mode intensity, E^2, (normalized to the peak in the active region) and refractive index profile of the 10QW, A3 nm, B1 nm, EBL 5nm, 6.95λ cavity thickness (single longitudinal mode) VCSEL. The ¼-wave ITO layer is aligned to a null of the mode using the 1/8-wave Ta_2O_5 spacer at the start of the p-DBR. The enhancement factor, Γ_{enh}, is 1.623. (c) LIV characteristics measured on the 12 μm aperture diameter VCSEL at a duty cycle of 0.3% (100 ns pulse width). The threshold current is ~18 mA (~16 kA/cm^2). (d) Emission spectrum as a function of current. The lasing wavelength is ~406 nm, with a cavity resonance mode spacing of ~22 nm, leading to single longitudinal mode emission. Measurements (not shown) confirmed the emission has a polarization ratio of 100 %.

212

described in Figure 59 and Figure 60, we can see that this version of the VCSEL had a Cr/Ni/Au contact deposited onto the ITO, followed by the p-DBR, which was then coated in Ti/Au. In our newer design, shown in Figure 59 and Figure 60, we eliminated this metal layer between the ITO and the p-DBR outside the aperture, in order to reduce the distance between the edge of the aperture and the edge of the p-DBR, in order to improve heat dissipation, while simultaneously reducing the processing time by eliminating several of the processing steps. Furthermore, we have eliminated the pillar-like p-DBR support structure outside the aperture (Figure 94(a)), in favor of a simpler monolithic p-DBR block, as our thermal simulations show that heat is effectively dissipated through the metal pillar/ring nearest to the aperture. The other notable design difference for this particular device is that it did not use the n-AlGaN PEC top-down etch-stop layer, as this sample was used to perform some of the analysis discussed in Section 3.3.1.1.

Viewing the LIV (Figure 94(b)) for the completed VCSEL employing a 20 keV Al ion implant and the multi-layer ITO film shown in Figure 83, we see the stimulated emission overcomes the spontaneous emission at ~20 mA. Extrapolating the stimulated emission LI trend back to the x-intercept, gives a threshold current (voltage) of ~18 mA (6.4 V), corresponding to a threshold current density of ~16 kA/cm^2 for the 12 μm aperture diameter VCSEL. At 80 mA the output power is ~12 μW. Considering the emission spectrum vs. current, shown in Figure 94(c), we see single longitudinal mode lasing at a wavelength of 406 nm, with a spectrometer resolution limited FWHM of ~2 nm at 70 mA. The log-scale plot of the emission spectrum in the inset of Figure 94(c) makes it easier to see the second resonance wavelength at ~427 nm. This implies the cavity resonance wavelength spacing is ~22 nm. This VCSEL was also measured to have a 100 % polarization ratio, as reported in

one of our initial reports on nonpolar VCSELs.[8] Comparing this device to our first generation nonpolar VCSELs, which employed a SiN_x aperture, we see a ~5X reduction in J_{th}, which is likely due to the use of the ion implanted aperture. Furthermore, the overall yield of these devices is markedly higher than we observed previously, though we still see a large variation in the J_{th} across a single chip. Despite the significant improvement in J_{th}, the differential efficiency was not improved. However, further iterations and optimizations of the IIA+ITO VCSEL design resulted in significant improvements in both threshold current density, with the final ITO VCSELs processed, prior to switching to the TJ VCSEL design, having a threshold current density of ~7 kA/cm^2 and a peak power of ~80 μW.

Prior to moving on to the more recent developments in the IIA+ITO VCSELs, it is important to consider the near-field emission profile for the VCSEL shown in Figure 94. Figure 95 shows optical microscope images, taken with a CCD camera, of the device as a function of current. The images were taken under low gain settings to avoid saturating the camera when the device was well above threshold. As is commonly observed in III-nitride VCSELs, the lasing is spatially non-uniform. As the current is increased the integrated spatial lasing area increases. This is not surprising, as higher order LP modes are expected to turn-on as the current is increased; however the observed spatial distribution of the lasing does not follow any clear predicted LP mode profile. The irregular nature of the lasing in the aperture suggests that filamentation is occurring.[364,369–371] Unfortunately, the primary cause
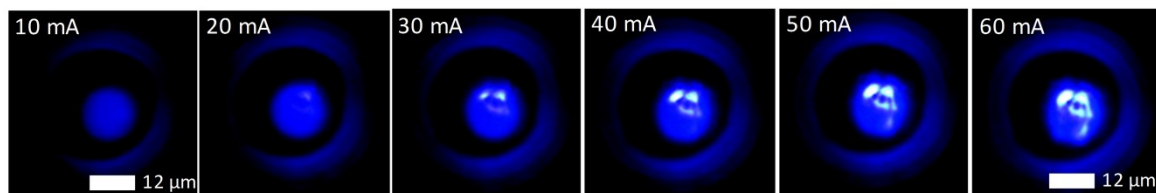
Figure 95 Optical microscope images, taken with a CCD camera, of the VCSEL aperture as a function of current. All images were taken with a low gain to prevent saturation at high currents. The lasing is seen to be non-uniform across the current aperture due to filamentation.

of filamentation is still unknown, however the original proposed causes included inhomogeneity in material composition, surface morphology, local cavity length, current spreading, or lateral index fluctuations.[8,171] Furthermore, in Ref. 10, we suggested that the polycrystalline nature of the ITO contact could introduce inhomogeneities in absorption loss across the aperture, inducing filamentation, however this was later refuted by the TJ VCSEL results.[11] Considering the length scale of experimentally measured indium fluctuations[220,234,372] it is unlikely that this is the cause of the non-uniformity in 405 nm VCSELs, though it may play a strong role at longer wavelengths. Next, given that the epitaxial growth and ITO employed in this device have < 1 nm RMS roughness, it is unlikely that rough surface morphology on the p-side of the device is resulting in the non-uniformity. The n-side morphology can be quite rough if the PEC etch conditions are not optimized properly (Section 3.3.1, however this particular device showed <1 nm RMS roughness after PEC etching, suggesting the n-side morphology is not an issue here either. Finally, given that multiple devices across the entire chip lased at approximately the same wavelength, long-range cavity length variations are probably not significant. Thus, we believe the filamentation is predominately a result of non-uniform current spreading, contact resistance, and/or lateral index fluctuations.

4.2.1.1. Optimization of Number of n-DBR Mirror Periods for 7λ IIA+ITO VCSELs

With the significant improvement in threshold current density and yield resulting from our IIA design demonstration discussed in the last section, we were in a better position to investigate the other parameters relevant to VCSEL operation. One of the simplest series

that can be performed on VCSELs is to test the effect of the number of n-DBRs, as the n-DBR deposition is the last step of the process and the number of DBR periods is very easily varied. The effect of the number of n-DBR mirror periods can be easily analyzed using the fundamental laser equations discussed in Section 1.4.2. To approximate how the mirror loss varies with the number of n-DBR mirror periods we use the TMM to calculate the mode in the cavity of a ~7λ ITO VCSEL with a 10QW, A3 nm, B1 nm, EBL5 nm design. It is particularly important to realize that this optimization was meant for 7λ cavities, as changing the cavity length itself affects the mirror loss, and thus a different cavity length will have a different optimal number of n-DBR mirror periods. Figure 96 shows the mirror loss (Figure 96(a)), threshold modal gain (Figure 96(b)), and top-side differential efficiency (Figure 96(b)) vs. the number of n-DBR mirror periods. In calculating the differential efficiency, we assume an injection efficiency, η_i, of 65 %.[155] In our original IIA demonstration[10] and the early generation of VCSELs with SiN$_x$ apertures,[8,14,15] we used a 10P n-DBR mirror, giving a mirror loss of ~3 cm^{-1}. As the number of n-DBR periods increases above 10P, the mirror loss begins to level out at a value of ~0.3 cm^{-1} (Figure 96(a)). The threshold modal gain, Γg_{th}, follows a similar trend, reaching a minimum of ~12.5 cm^{-1} (Figure 96(b)). Here,
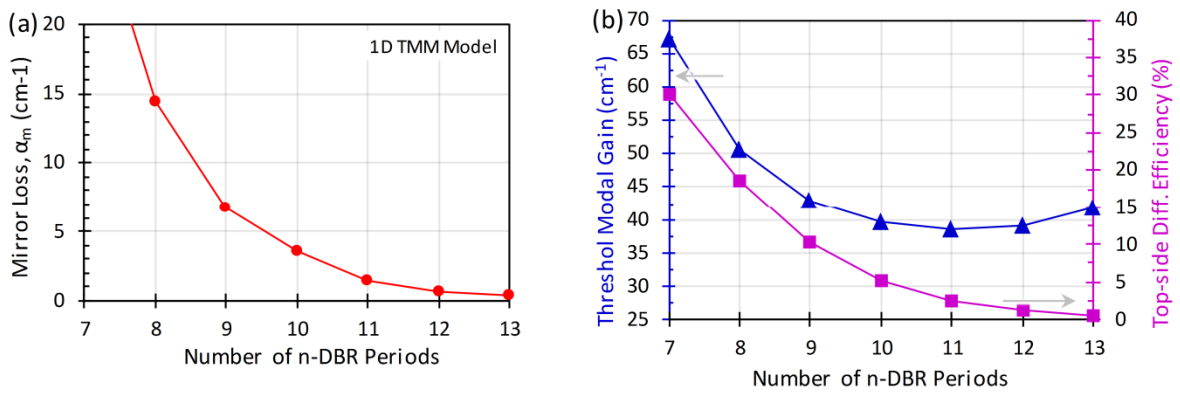
Figure 96 Simulated mirror loss vs. number of n-DBR mirror periods, where the n-DBR is composed of SiO$_2$/Ta$_2$O$_5$ ¼-wave layers. The Ta$_2$O$_5$ and SiO$_2$ layers are assumed to be lossless with refractive indices of 2.22 and 1.516, respectively.

a slight increase in Γg_{th} occurs from 11P to 13P, due to a small increase in the modal overlap with the highly absorbing ITO layer (the ITO absorption coefficient is ~2000 cm$^-$ ^{1}).[10] Finally, with increasing n-DBR mirror periods, the differential efficiency decreases from ~18 % with an 8P n-DBR, to ~1 % with a 12 P n-DBR, due to the decrease in the mirror loss.

To compare the simulated results to experimental results, a series of VCSELs were processed with 8, 10, and 12P n-DBRs. The VCSEL geometries were similar to that shown in Figure 94(a), however the samples were flip-chip bonded to a Cu block instead of a sapphire submount. All LIV measurements were done under pulsed operation at 0.3% duty cycle (100 ns pulse width). Figure 97 shows the threshold current density, J_{th}, (Figure 97(a)) and top-side differential efficiency (Figure 97(b)), as a function of the number of n-DBR mirror periods for devices with aperture diameters ranging from 6-20 μm. The aperture diameter dependence is discussed in Section 4.2.1.2. Each chip contained over 100 processed devices, which were all tested, though only the devices that lased are reported. As the number of n-DBR mirror periods increases from 8 to 12P we see a decrease in the minimum threshold current density ($J_{th,min}$), an increase in the top-side differential efficiency
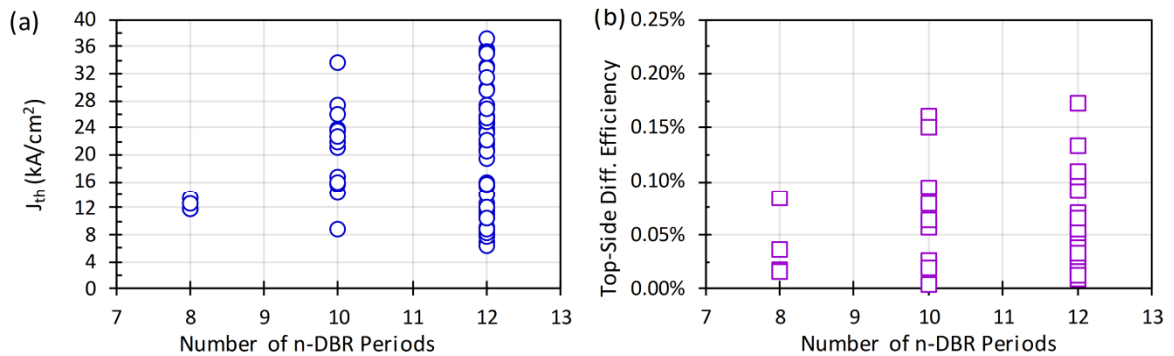
Figure 97 (a) Threshold current density (J_{th}) and (b) top-side differential efficiency ($\eta_{d,top}$) vs. number of n-DBR periods measured on 7λ IIA+ITO VCSELs with apertures ranging from 6-20μm. The number of lasing devices/chip decreases as the number of n-DBR periods decreases, while the minimum J_{th} decreases and the maximum $\eta_{d,top}$ increases as the number of n-DBR mirror periods increases.

($\eta_{d,top}$), along with an increase in the overall yield. For the 8P n-DBR case we see a $J_{th,min}$ of ~12 kA/cm^2 with a yield of 5 VCSELs/chip. Increasing the number of n-DBR mirror periods to 10P, the $J_{th,min}$ reduces to ~9 kA/cm^2 and the yield increases to 12 VCSELs/chip. Finally, with a 12P n-DBR we achieve $J_{th,min}$ of ~6.5 kA/cm^2 and a yield of over 50 VCSELs/chip. The cause of the large variation in J_{th} is related to the variation in aperture diameter, which leads to changes in the lateral confinement factor, current spreading, and the degree of filamentation. The details of this are discussed in the next section. Overall, the trend in reducing J_{th} with increasing number of n-DBR mirror periods observed experimentally agrees with the simulations showing a reduced threshold modal gain with increasing number of mirror periods (Figure 96(a)), however this is not the case for the trend of differential efficiency. In the experimental results (Figure 97(b)) we see the top-side differential efficiency generally increases as the number of n-DBR periods increases, as is expected for all lasers. This is in contrast to the trend expected from Eqn. (4) and the simulated results shown in Figure 96(b). This effect is a result of the anomalous filamentation observed in all samples. Viewing the near-field emission profile via optical microscopy we observe the degree of filamentation generally decreases as the number of n-DBR mirror periods increases. This suggests that the filamentation is a result of spatial variation in the cavity loss or gain across the aperture. By increasing the number of n-DBR mirror periods we lower the threshold modal gain, thereby lowering the average cavity loss across the aperture, resulting in a decrease in the degree of filamentation and an increase in the differential efficiency. It is likely that once the exact cause of filamentation is understood and under control one could improve the differential efficiency by increasing the mirror loss, however

the immature nature of the field makes achieving a reliable process with high yield arguably more important for understand the unique operating characteristics of III-nitride VCSELs.

4.2.1.2. Aperture Diameter Dependence of 7λ IIA+ITO VCSEL Lasing

Following the analysis of the effect of the number of n-DBR mirror periods we analyzed the effect of the aperture diameter for the each sample. Figure 98(a) shows the threshold current density vs. aperture diameter for the 8P, 10P, and 12P n-DBR samples, while Figure 98(b) shows the top-side differential efficiency vs. aperture diameter for the 12P n-DBR sample. Figure 99 shows the LIV and LJV curves for the best performing devices of each aperture diameter on the 12P n-DBR 7λ IIA+ITO VCSEL. Figure 100 shows optical microscope images of the near-field emission for the devices shown in Figure 99.

First, consider Figure 98(a). Here, the threshold current density is seen to decrease as the aperture diameter is increased from 6 to 10 µm, then increase again from 10 to 20 µm.
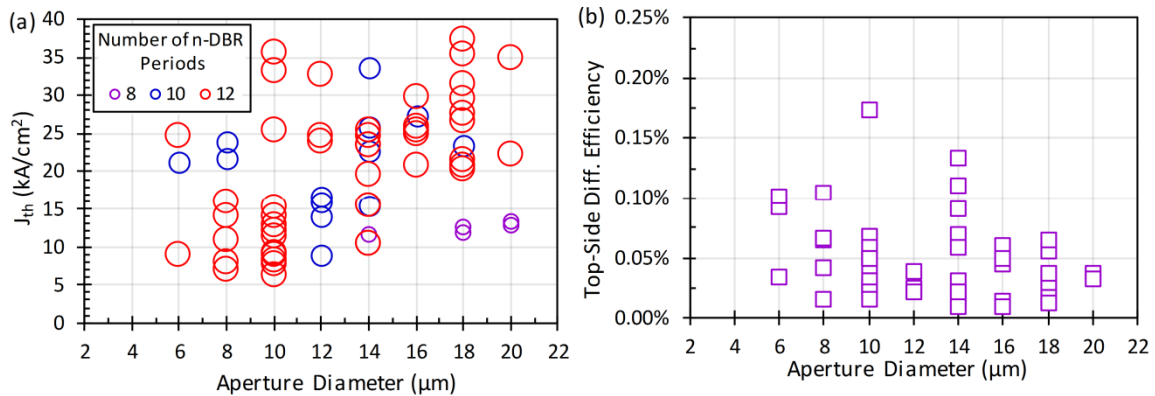
Figure 98 Threshold current density (J_{th}) vs. aperture diameter for 405 nm IIA+ITO VCSELs with 8, 10 and 12P n-DBRs. The J_{th} is seen to increase as the aperture diameter increases from 10 µm, due to reduced current spreading efficiency, while J_{th} increases as the diameter decreases from 10 µm due to the reduced confinement factor (Figure 92).
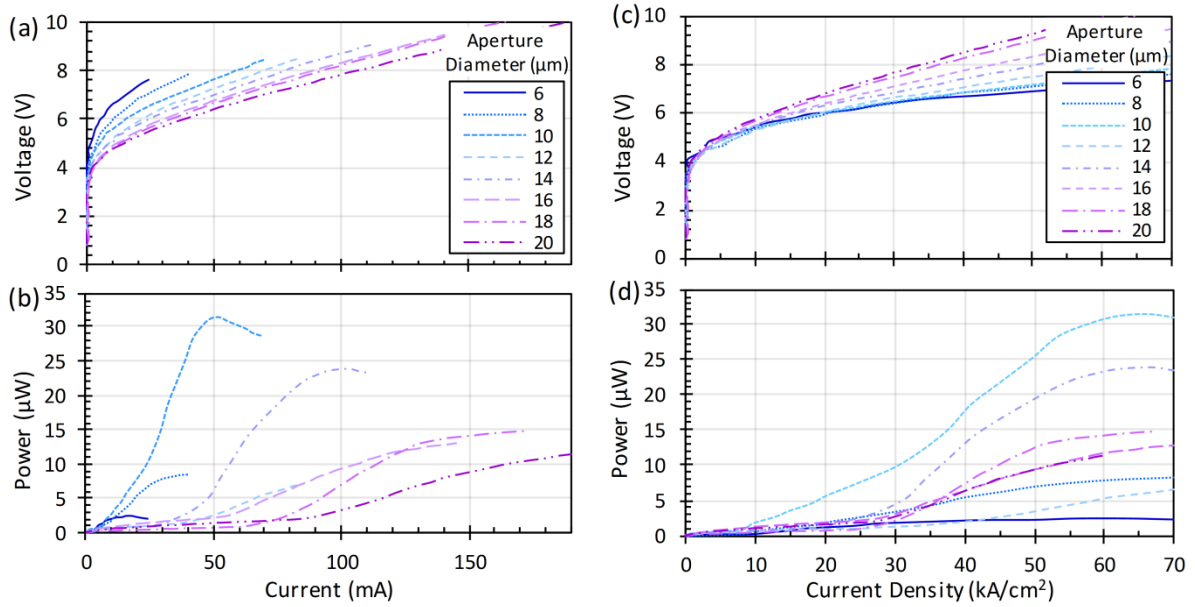
Figure 99 (a) voltage and (b) output power vs. current for the lowest J_{th} VCSELs with aperture diameters ranging from 6-20 μm. The corresponding plots of voltage and output power vs. current density are shown in (c) and (d). For a given *current*, smaller aperture diameter devices operate at higher voltages, but for a given *current density* they operate at a lower voltage. The 10 μm aperture diameter device shows the highest output power.

There are two important aperture diameter dependent characteristics to be considered here, (1) the lateral confinement vs. aperture diameter, and (2) the current spreading vs. aperture diameter. As is shown in Figure 91(b), defining the aperture using Al ion implantation results in a small (~2 %) decrease in the refractive index of the implanted layer.[10] This leads to the lateral confinement factor (Γ_{xy}) vs. aperture diameter trend shown in Figure 92(a). For aperture diameters less than 10 μm, the lateral confinement factor begins to drop dramatically, resulting in a decrease in the total confinement. This correlates to the experimentally observed 6-10 μm aperture diameter threshold current density trend (Figure 98(a)). Specifically, as the lateral confinement decreases the mode becomes less confined to the aperture of the VCSEL. This implies that the active region must be pumped harder in order to achieve the higher material gain necessary offset the lower confinement factor, and thereby reach the threshold modal gain. This higher material gain required implies a higher
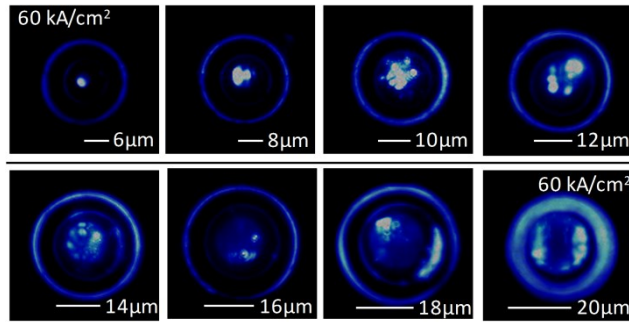
Figure 100 Optial microscope images of the devices shown in Figure 98 and Figure 99 operating at 60 kA/cm². Filamentation is evident in each case, however devices with ≤ 12 μm aperture diameters show the most uniformity of emission in the aperture. Above 12 μm aperture diameters the lasing occurs predominantly at the edge of the apertures where poor current spreading efficiency results in the highest localized current density being at the edge of the aperture. The 20 μm device shows brighter areas outside the aperture, relative to the other devices, as a result of the n-DBR pattern only being 5 μm larger than the aperture diameter, rather than 10 μm, as was the case for all other aperture diameters.

threshold current density, resulting in the observed increase in threshold current density as the aperture diameter decreases from 10 to 6 μm (Figure 99(a)). It is of note that devices with 4 μm apertures were also processed on this same chip, however none of these devices lased due to poor lateral confinement.

For aperture diameters greater than 10 μm, the confinement factor for the fundamental mode is relatively constant (Figure 92(a)) and thus has very little influence on the observed increase in the threshold current density from 10 μm to 20 μm devices. To understand why this increase in threshold current density is observed, we must consider how current spreading varies with aperture diameter. Current spreading can be analyzed in two ways (1) viewing the emission intensity across the aperture, or (2) modeling the current spreading profile across the aperture. In a fully processed VCSEL using method (1) is difficult because the high reflectivity mirror on the top-side of the device prevents much of the spontaneously emitted light from escaping the cavity. Furthermore, the filamentary nature of the lasing light convolutes the current spreading analysis (Figure 100). However, even if the devices were not filamentary in nature, well defined *LP* modes do not have emission intensity profiles that perfectly correlate with current distributions in the aperture

(Figure 92(b)). Choosing to model the current spreading profile based on IV measurements can be difficult because it requires making many assumptions about the various sources of resistance (such as contact resistance, or hetero-barriers) and the nature of their equivalent circuit element IV characteristics. If the device of interest follows the diode equation with an ideality factor between 1-2, one can be reasonably certain that the modeling current profile in the structure corresponds to the true current distribution in the device. However, such ideal devices are rarely found in research-grade material. Finally, in the VCSEL structure, current spreading occurs on the p-side (through the ITO or TJ intracavity contact) as well as on the n-side (predominantly through the n-GaN cavity layer), implying that one must develop a model that couples the current spreading on the n-side to the current spreading on the p-side of the device, in a similar manner to what is done for ambipolar diffusion. In collaboration with M. Piccardo at Ecole Polytechnique, we began developing such a model building on the work by Joyce and Wemple.[373] Using a modified Joyce and Wemple model developed by M. Piccardo, we fit the IV and JV vs. aperture diameter data shown in Figure 99(a) and (c) and analyzed the normalized current density vs. normalized radial distance at 60 kA/cm^2. Unfortunately, fitting these IV characteristics yielded diode equations with unrealistically large ideality factors (15-20), suggesting that there were some significant equivalent circuit elements not accounted for in the models. This implies that the quantitative validity of the models needs to be confirmed by analyzing the spontaneous emission distribution in the aperture prior to the n-DBR deposition, which was not done on this particular sample set. None the less, the preliminary results from the models highlight some important properties that should be considered for III-nitride VCSELs, and the general results do correlate well with the observed lasing performance vs. aperture diameter trends.
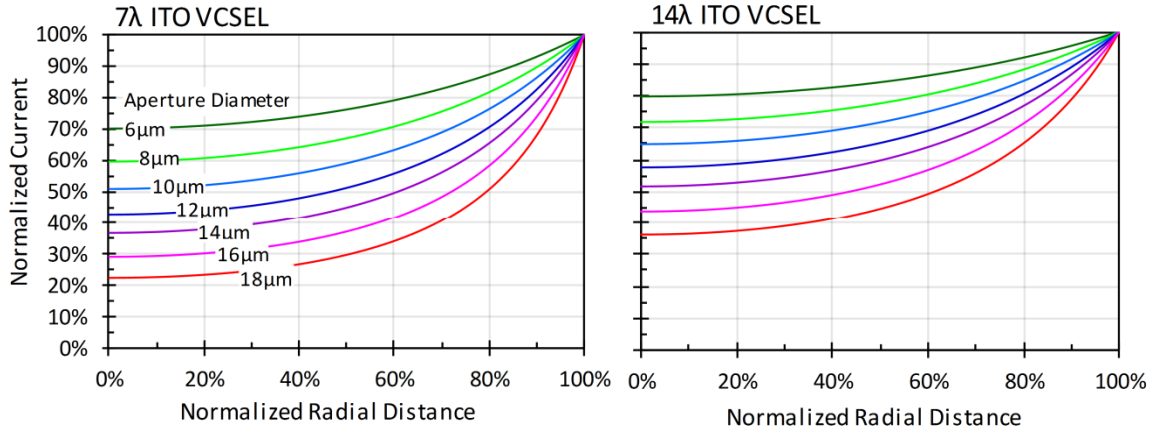
Figure 101 Preliminary simulation results analyzing the current spreading in a 7λ ITO VCSEL (left) and 14λ ITO VCSEL (right). The normalized current in the aperture is plotted vs. normalized radial distance, assuming each device is operating at a total injection current density of 60 kA/cm^2. The results show significant variations in current spreading between devices with different aperture diameters and different cavity lengths, however because the models were based purely on IV curves that showed unrealistically large ideality factors (15-20), the quantitative validity of the models is not clear at this time. Data analyzing the spontaneous emission intensity in the aperture, prior to the n-DBR deposition, is necessary to confirm whether or not the model is showing the precise current distributions in the aperture. Regardless though, the relative trend of the current spreading between aperture diameters and cavity lengths is an important consideration for VCSEL designs and agrees well with the general observations of on lasing characteristics vs. aperture diameter.

Figure 101 shows some preliminary results from these analysis, where the plot on the left shows the normalized current vs. normalized radial distance for a 7λ cavity, while the plot on the right shows the case of a 14λ cavity. Here we can see that with increasing aperture diameter, the current spreading efficiency continually decreases. This decreasing spreading efficiency with increasing current implies that one must inject a higher current into the edge of large aperture diameter devices in order to achieve the same current density seen in the center of a smaller aperture diameter device. This would then lead to an increase in the measured threshold current density, as seen Figure 98(a) for devices with aperture diameters ranging from 10 to 20 μms. Furthermore, we would expect this reduced current spreading efficiency to result in lasing being localized to the edge of large aperture diameter devices, where the current density is the highest. This is in agreement with the optical microscope images of the near-field pattern measured at 60 kA/cm^2, shown in Figure 100. It is of note that filamentary lasing is also observed, however it appears that the filamentation effect is

overlain with the non-uniform current distribution. Specifically, we see for aperture diameters from 6 to 10 μm, the stimulated emission occurs across the entire aperture, with filamentary lasing spots distributed randomly. Above 10 μm the lasing becomes increasingly localized to the edge of the aperture where the current is highest. For the 18 μm and 20μm device, the lasing occurs only at the very edge of the aperture due to the very weak current spreading efficiency. In further support of this conclusion, Figure 102 shows optical microscope images taken prior to the n-DBR deposition on the same chip that the VCSEL reported in Ref. 10 came from. Unfortunately, we did not record the drive current at which these images were taken, making a more quantitative analysis of the current spreading difficult. Furthermore, the number of lasing devices on this original IIA+ITO VCSEL was considerably lower than the yield from the chips fabricated for the number of n-DBR mirror periods and aperture diameter effect analysis. Regardless, viewing the spontaneous emission profiles in Figure 102, we can see that as the aperture diameter increases from 4 μm to 10 μm, the peak emission intensity remains relatively localized to the center of the aperture.
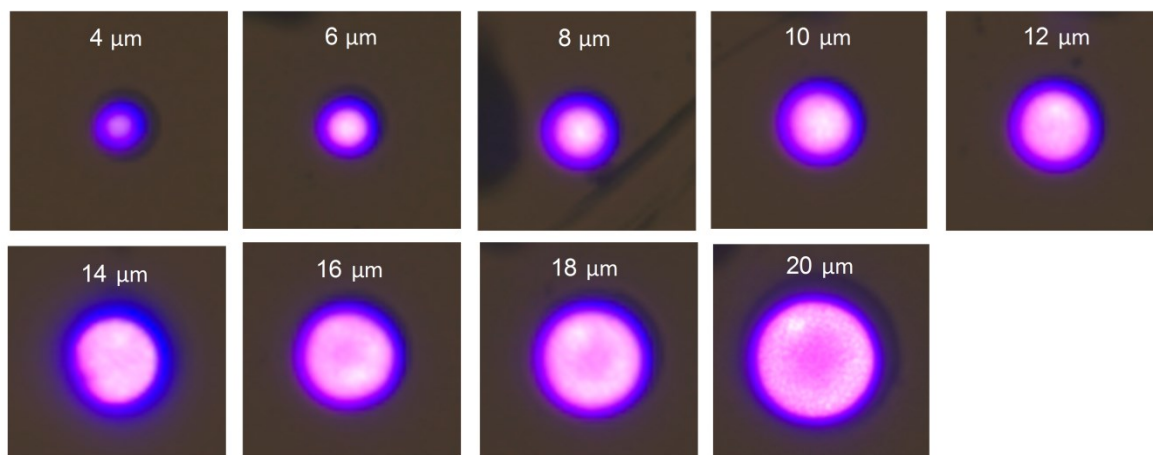
Figure 102 Optical microscope images of the spontaneous emission distribution in partially processed VCSELs, measured prior to the n-DBR deposition. These samples were from the same chip as the VCSEL reported in Ref. 10. Unfortunately, the drive current was not recorded for each of the images, making a more quantitative analysis of the current spreading distribution difficult, however one can easily see that as the aperture diameter is increased from 12 μm to 20 μm, the emission becomes increasingly localized to the edge of the aperture, indicating non-uniform current spreading.

Moving from 12 μm to 20 μm apertures, the emission begins to become increasingly localized to the edge of the aperture, suggesting that highly non-uniform current spreading is occurring in devices with large aperture diameters (> 14 μm). For ITO VCSELs, the only effective way to improve the current spreading is to increase the n-GaN thickness. The plot on the right hand side of Figure 101 shows the primary simulation results for a 14λ ITO VCSEL, where we can see the current spreading efficiency is significantly improved. However, because an ITO VCSEL cannot improve the current spreading on the p-side of the device, due to the restriction of the ITO being ¼-wave thick, we are very restricted in the design options to improving the current spreading. This highlights another advantage of the TJ VCSEL, which was briefly discussed in Section 4.1.4. In the TJ VCSEL design we can improve the current spreading on both the n-side and p-side of the device by increasing the n-GaN cavity thickness, as well as the TJ thickness. Because single longitudinal mode operation can still be easily achieved with a 23λ cavity, it is likely that using a 23λ cavity will yield the best current spreading and thermal dissipation efficiency for dual dielectric DBR VCSELs. In the DOE outlined in Figure 78, we show our plans to measure the current spreading efficiency on 13λ and 23λ IIA+TJ VCSELs, which will hopefully allow us to develop a more quantitative model for describing the current spreading in III-nitride dual dielectric DBR VCSELs.

Moving back to Figure 98 and considering the differential efficiency vs. aperture diameter for the 12P n-DBR sample (Figure 98(b)), we see that the differential efficiency generally decreases with increase aperture diameter across the entire 6 to 20 μm range. This highlights the secondary effect of the overlay between the filamentary lasing and current spreading efficiency. In all devices some degree of filamentation is observed, however as the

aperture diameter increases from 6 to 20 µm the filamentary lasing effect becomes overlaid with the reducing current spreading efficiency, resulting in a gradual reduction of the total lasing area in the aperture, and thus a reduction in the differential efficiency with increasing aperture diameter. Generally speaking one would expect large aperture diameter devices to result in higher output power, however, as can be seen, this false expectation is based on the assumption that the III-nitride VCSEL has efficient current spreading for all aperture diameters.

For many applications achieving a minimum total input power is desirable, thus one should not only consider the J_{th} and I_{th}, but also the V_{th} and the differential resistance vs. aperture diameter. Using the IV data from all the 12P n-DBR VCSELs shown in Figure 97, we measured the average differential resistance vs. aperture diameter, shown in Figure 103(a) and (b). Observing Figure 103 and Figure 99(a), we see that as the aperture diameter increases, the differential resistance decreases from ~75 Ω for a 6 µm aperture, to ~25 Ω for an 18 and 20 µm aperture. This implies that for a given operating current, a smaller aperture diameter device will operate at a higher voltage (i.e. higher input power and more self-heating). Comparing the trend in terms of current density (Figure 99(c)), we see that for a given current density a smaller aperture diameter device will operate at a lower voltage.
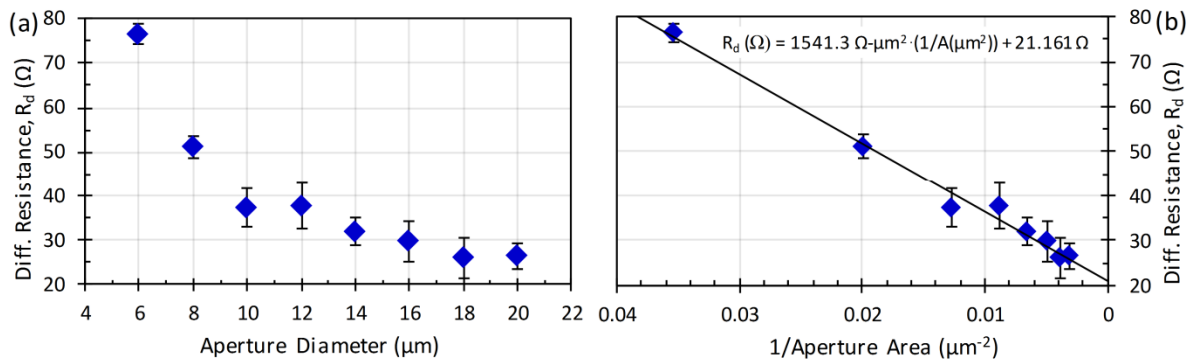
Figure 103 (a) Differential resistance vs. aperture diameter and (b) 1/aperture area for all 12P n-DBR VCSELs shown in Figure 97.The differential resistance decreases as the aperture diameter increases. For an infinitely large aperture area (y-axis intercept on plot (b)) we find a differential resistance of 21.161 Ω.

Understanding these effects is critical because when we consider the effect of lateral confinement as a function of aperture diameter (Figure 92(a)), along with the differential resistance trends (Figure 103), we can realize that once the lateral confinement begins to drop off for small aperture diameter devices, there is no longer any advantage to using a small aperture diameter device, as it would then have a higher threshold voltage for a marginal or non-existent improvement in threshold current. Considering Figure 99(a) and (b), we see that this is indeed the case for devices with 6, 8, and 10 µm apertures. Specifically, each device has essentially the same threshold current, however the 10 µm device has the lowest threshold voltage, meaning it operates with the lowest input power. For larger aperture diameters, one runs into issues with current spreading, as mentioned previously.

In summary, by optimizing the number of n-DBR mirror periods and analyzing the aperture dependence of the lasing characteristics for 7λ IIA+ITO VCSELs, we were able to not only improve the overall performance of our IIA+ITO VCSELs, but also realize some of the fundamental limitations of our device design. The issues with current spreading illuminated the necessity for using a thick cavity to improve current spreading in large aperture devices, while the issues with weak index contrast between the core and cladding in the IIA design highlighted the importance of developing new lateral confinement methods with stronger index contrast to achieve efficient lasing in VCSELs with small aperture diameters. To overcome the lateral confinement issue, we developed the PECA design. However, before going into the details on the PECA VCSEL demonstration and the challenges with using such an aperture design, we will highlight some of the other results obtained using the IIA design, including 100% polarization locked VCSEL arrays, as well as

the demonstration of IIA+TJ VCSELs and some of the aperture diameter dependent trends observed on those samples.

4.2.1.3. 100 % Polarization Locked IIA+ITO VCSEL Arrays

III-nitride VCSELs grown on c-plane substrates have been shown to have emission with a polarization ratio of ~ 80%,[132] however because of the isotropic nature of the transition matrix elements on c-plane, one would expect an array of c-plane VCSELs to have an average of 0% polarization.[15] In contrast, each m-plane VCSEL in an m-plane VCSEL array has a polarization defined by the anisotropic nature of the transmission matrix elements (i.e. gain) on m-plane, as was discussed in Section 1.3.4.2. In our original demonstration of a nonpolar VCSEL,[14] emission with a polarization ratio of 100% was not observed because the polarization was measured using a linear polarizer in front of a photodetector (i.e. the output power vs. polarizer angle was measured). This resulted in spontaneous emission being collected with the stimulated emission. The spontaneous emission on m-plane is polarized predominantly in the a-direction, however transitions from the B1 valence subband also contribute to the total spontaneous emission output power,
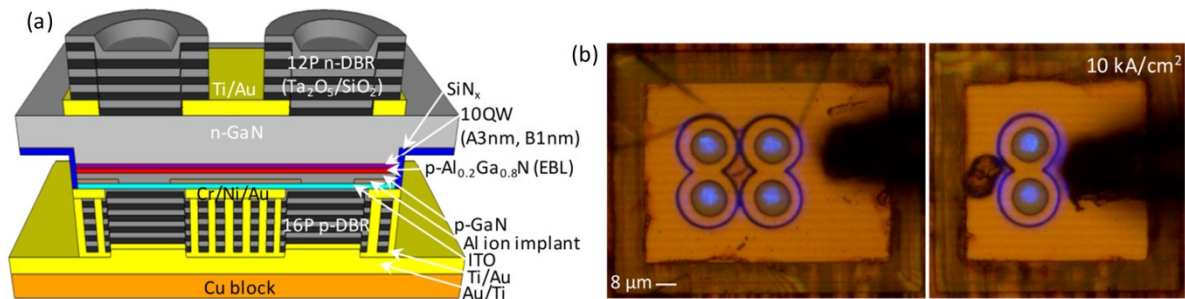
Figure 104 Schematic cross-section of the VCSEL array design. The arrays employ an IIA+ITO design and are flip-chip bonded to a Cu block. The devices have an ~7λ cavity thickness, with a 10QW, A3 nm, B1 nm and ELB5 nm active region design.

leading to a polarization ratio of < 100 %. In Ref. 8, we measured the polarization using a linear polarizer and a fiber optic, allowing us to analyze the polarization of the stimulated emission alone. This yielded a polarization ratio of 100 %, with the emission polarized parallel to the a-direction. Following the investigations on the number of n-DBR mirror periods and aperture diameter effects, discussed in the previous section, we went on to experimentally prove that an m-plane VCSEL array would have a total polarization of 100 %. Figure 104(a) shows a schematic cross-section of the m-plane VCSEL array with an IIA+ITO design. These devices were patterned on the same chip as the 12P IIA+ITO
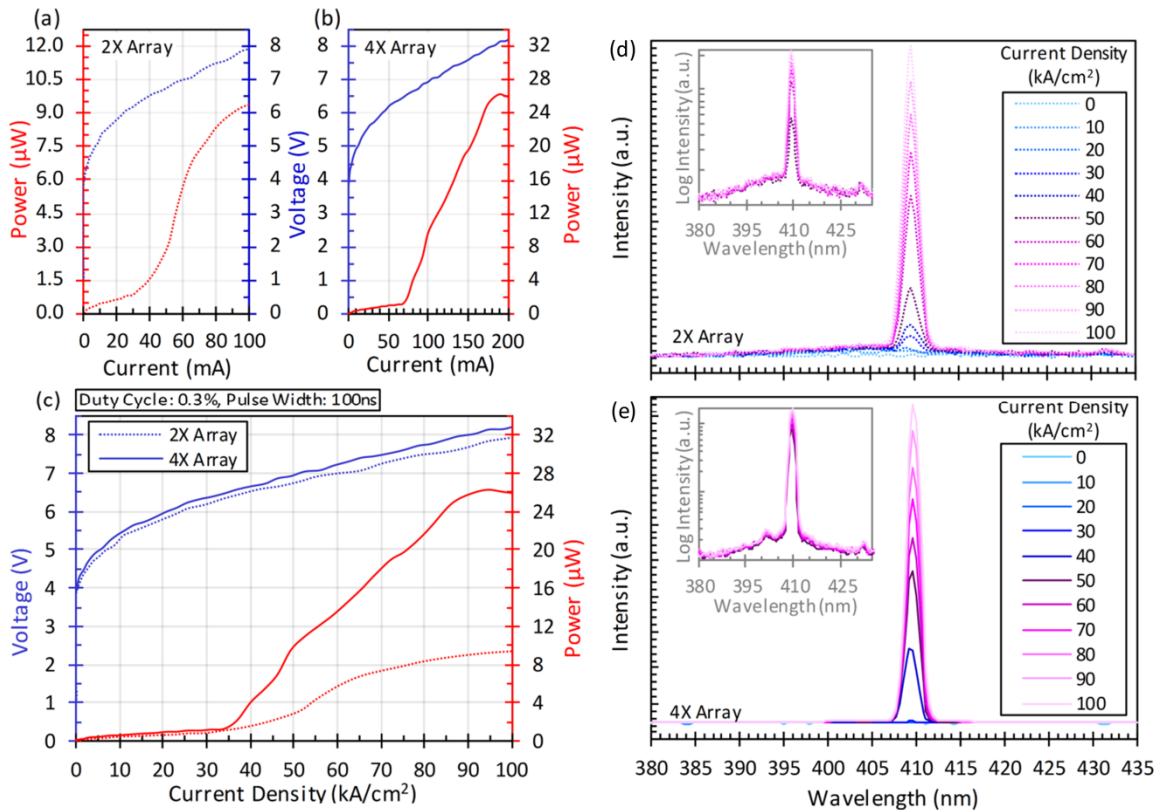
Figure 105 LIV characteristics for the 2X (a) and 4X (b) VCSEL arrays with 8 μm aperture diameter devices. (c) shows the LJV characteristics for each device. The threshold current (current density) for the 2X array is ~25 mA (~25 kA/cm^2), and ~70 mA (~35 kA/cm^2) for the 4X array. The emission spectrum vs. current density for the 2X array and the 4X array are shown in (d) and (e) respectively. The insets show the 50 – 100 kA/cm^2 spectra plotted on a log scale. The lasing wavelengths are ~410 nm. The log scale shows single longitudinal mode emission, with a mode spacing of ~21 nm. The peak spontaneous emission wavelength was measured to be ~405 nm.

VCSELs discussed in the previous section. Figure 104(b) shows optical microscope images of the 8 μm aperture diameter VCSEL arrays discussed here. A number of arrays on the chip were tested, however many did not show lasing in all the VCSELs in the array. Figure 105(a), (b), and (c) show the LIV curves for the 4× and 2× VCSEL arrays being considered here. Both arrays show approximately the same threshold current density per VCSEL (~35 kA/cm^2). Comparing the peak powers, we see that going from the 2× array to the 4× array the total output power increases from ~9 μW to ~26 μW, implying output power per VCSEL varies from array to array and device to device. This is a result of the filamentary lasing in
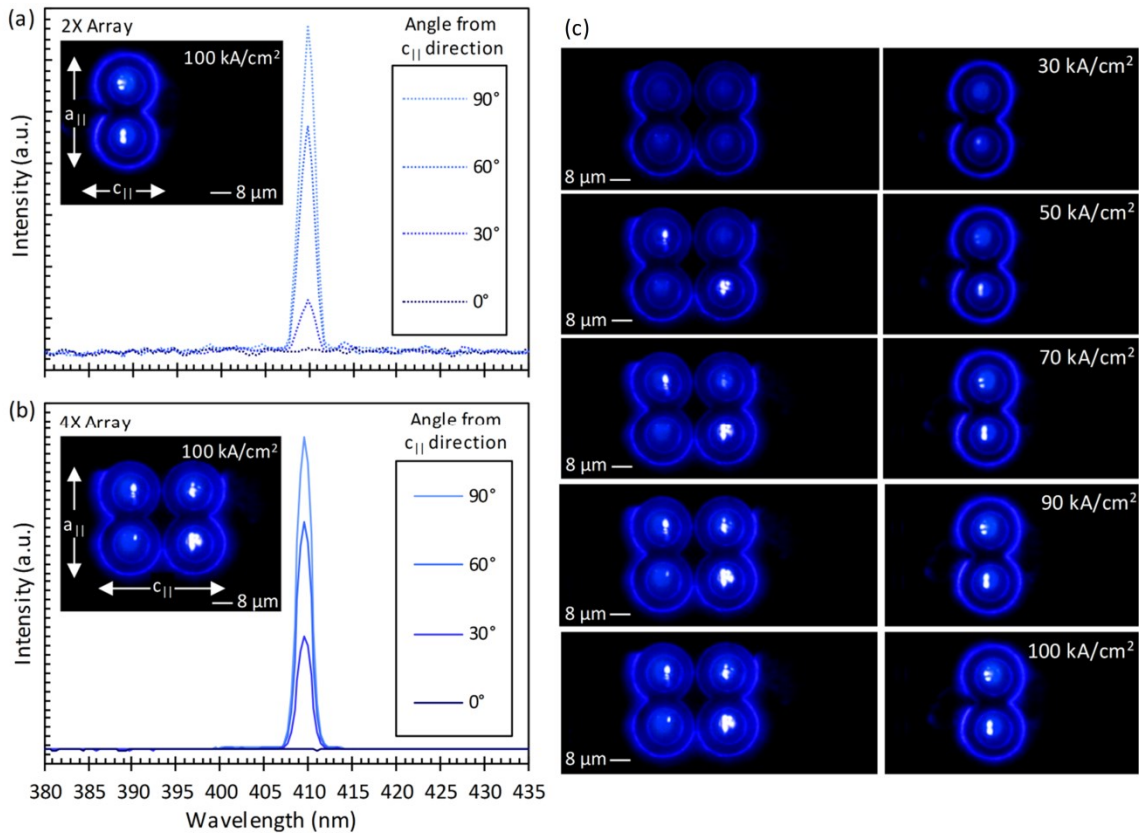
Figure 106 (a) and (b) show the emission spectra as a function of linear polarizer angle relative to the c|| direction for the 2× and 4× array, respectively. The devices were measured at 100 kA/cm^2. The insets show optical microscope images of the arrays, with each individual VCSEL showing varying degrees of filamentation. The a|| and c|| directions are labeled. Both arrays are measured to have a polarization ratio of 100 %, due to the intrinsic nature of the anisotropic gain on m-plane leading to 100 % polarized emission for each individual m-plane VCSEL.[8] (c) shows the near-field optical microscope images as a function of current density, fo the 4× array (left) and 2× array (right). In each array, many of the VCSELs show different threshold currents.

230

the aperture, shown in the optical microscope images in Figure 106(c). The emission spectra at various current densities can be seen in Figure 105(c), where we see each array lases at ~410 nm, and has a resonance wavelength spacing of ~21 nm. The emission spectra vs. linear polarizer angle for each device (operating at 100 kA/cm^2) is shown in Figure 106(a) and (b). As can be seen, each array shows a polarization ratio of 100%, with the emission being polarization locked in the a|| direction. This experimentally demonstrates 100% polarized emission from m-plane VCSEL arrays. This highly polarized emission can be advantageous in many of the applications discussed in the introduction. Viewing Figure 106(c), we can see that it is critical to observe the near-field emission profiles before doing the polarization measurement as many of the devices in the array do not have the same threshold current.

4.2.1.4. Comparison of 7λ 7QW IIA+ITO VCSEL to 7QW IIA+TJ VCSEL

Following the analysis of the polarization from nonpolar VCSEL arrays, we went on to perform a parallel test of the potential for TJ intracavity contacts, a PEC etched air-gap aperture (PECA) VCSEL, and the effect of the number of QWs on lasing performance. Unfortunately, the new design we were testing resulted in a significant reduction in yield, due to cracking after the flip-chip bond (discussed in Section 4.3). This resulted in many of the chips in the number of QWs study having no lasing devices. Fortunately a number of the devices on the 7QW IIA+ITO and IIA+TJ VCSEL chips made it through the process, allowing for the direct comparison of the ITO design to the TJ design, as discussed in Section 4.1.4. Here we will discuss more of the device results from these chips, going into
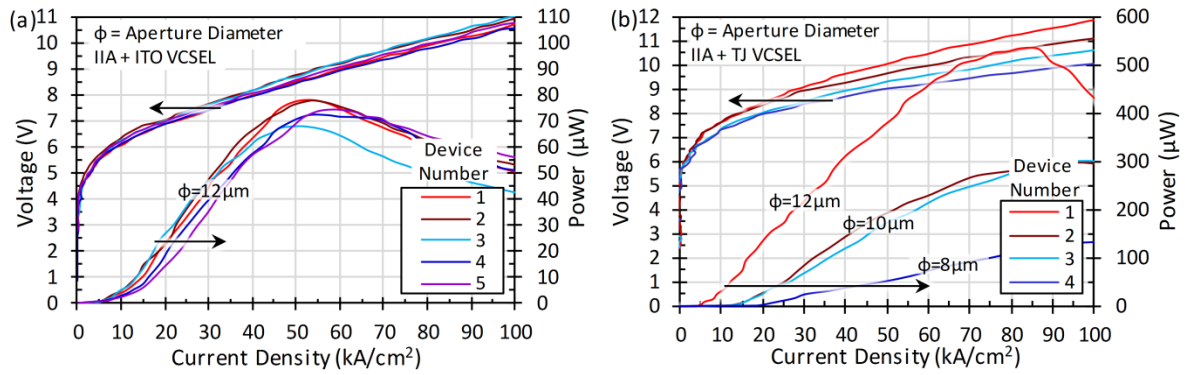
Figure 107 LIV characteristics for the 7QW 7λ IIA VCSELs. (a) shows the IIA+ITO VCSELs, while (b) shows the IIA+TJ VCSELs (~141 nm TJ thickness). All measurements were made under pulsed operation with a duty cycle of 0.3% (100 ns pulse width). Device 5 of the IIA+ITO VCSEL and device 1 of the IIA+TJ VCSEL correspond to those shown in Figure 86 and reported in Ref. 11.

detail on the improved ITO VCSEL performance by using 7QWs instead of 10, and the TJ VCSEL vs. aperture diameter trends. The other notable difference on these more recent 7QW samples is that they used the n-AlGaN etch-stop layer, which had been left out of some of the previous samples in order to test the feasibility of eliminating the top-down PEC etch step (Section 3.3.1.2).

Figure 107(a) shows several LIV curves for the 7QW ~7λ IIA+ITO VCSELs processed in parallel with the similar IIA+TJ VCSELs, for which the LIV curves are shown in Figure 107(b). All measurements were taken under pulsed operation with a duty cycle of 0.3% and a 100 ns pulse width. Beyond the TJ VCSELs evident improvement in LIV characteristics under pulsed operation, it is also of note that TJ VCSELs continued to lase under higher pulse widths (10's of μs), while the ITO VCSELs only showed spontaneous emission, due the misalignment of the peak gain and peak cavity mode wavelength (i.e. gain offset parameter) caused by internal heating. This is in agreement with the improvement in lateral heat dissipation expected from using a TJ (Figure 48). Considering the specific performance characteristics of the devices, we see, in Figure 107, that the 7QW IIA+ITO VCSELs with aperture diameters (φ) of 12 μm consistently give ~7 kA/cm^2 (7.9 mA)

threshold current densities, with variable peak output powers around 70-80 μW at ~50-55 kA/cm^2. These output powers are more than 2× greater than the peak powers achieved in the best performing 10QW IIA+ITO VCSELs (Figure 99), suggesting that the 10QW design may suffer from non-uniform injection into some of the QWs, leading to additional internal absorption losses from the poorly populated QWs. The threshold voltage is ~5.5 V and the operating voltage increases to ~8.5 V at 50 kA/cm^2 (56.5 mA). Device 5 corresponds to the ITO VCSEL reported in Ref. 11 and shown in Figure 86. The most direct comparison between the ITO VCSELs and the TJ VCSELs is realized by comparing the LJV curve for the 12 μm aperture diameter TJ VCSEL (device 1) shown in Figure 107(b). This was also the TJ VCSEL analyzed in Ref. 11 and Section 4.1.4. Unfortunately, this was the only 12 μm aperture diameter device to make it through the process, preventing a more statistically relevant comparison. Regardless, viewing the LIV curves for this device, we see the TJ VCSEL shows a marginal improvement in threshold current density, lasing at ~3.5 kA/cm^2. This threshold is also confirmed in the spectral analysis shown in Figure 87(a) and (b). The threshold voltage is seen to increase to ~6.5 V, highlighting the non-optimized nature of the TJ contact resistance. On device 1 of the TJ VCSELs, we observe a significant improvement in differential efficiency and peak output power compared to the ITO VCSELs. Specifically, the 12 μm aperture diameter TJ VCSEL shows a peak power of ~550 μW at ~85 kA/cm^2. At 50 kA/cm^2 the power is ~475 μW and the voltage is ~10 V. Considering the other TJ VCSEL devices with 8 and 10 μm aperture diameters, we see the threshold current density significantly increases with decreasing aperture diameter. This is in agreement with our previous studies on the aperture diameter dependence of the threshold current density on IIA+ITO VCSELs, discussed in Section 4.2.1.2. Despite the significant increase in threshold

current density with decreasing aperture diameter for the IIA+TJ VCSELs, even the poorest performing TJ VCSEL, with an 8 μm aperture diameter, still achieves a higher peak output power than any of the ITO VCSELs. Overall, the results described here and in Section 4.1.4 demonstrate the great potential for TJ VCSELs, yet there is still a great deal of research necessary to achieve the optimal performance for III-nitride TJ VCSELs

Although the first demonstration of a III-nitride TJ VCSEL[11] simply built on our previously established IIA design, it is of note that the buried TJ (BTJ) method may be a more promising approach. A number of groups have shown effective electrical confinement using a BTJ on III-nitride micro-LEDs.[287,374] However, these TJ intracavity contacts have simply used a patterned n^{++}GaN contact to p-GaN, followed by an n-GaN regrowth current-spreading layer, forming the completed BTJ. This particular kind of BTJ design is currently being processed for a nonpolar VCSEL, as outlined in the DOE shown in Figure 78, however additional improvements could be realized by replacing the n-GaN regrowth layer with an n-AlGaN layer. This could potentially yield effective optical and electrical confinement from the BTJ, though the precise degree of the confinement would depend on the n-AlGaN composition, and the depth of the etch through the n^{++}GaN/p^{++}GaN contact. As was mentioned in Section 1.3.2, InP-based VCSELs have had great success using the BTJ design, where there the BTJ is formed with n^{++}InGaAs as the p^{++}InGa(Al)As contact, followed by a lower index n-InP regrowth layer.[4] The n++GaN/n-AlGaN BTJ would be the III-nitride parallel to the InP-based VCSEL BTJ. Beyond the BTJs favorable confinement characteristics, and its structural stability (compared to the PECA design), using a BTJ with a thick n-AlGaN current spreading layer is likely the optimal intracavity contact design for UV VCSELs operating near the band-gap of GaN.

Though the BTJ design is promising, this option for designing an aperture was not available until the IIA+TJ VCSEL was demonstrated. Another alternative to confinement for ITO and TJ VCSELs is to form an air-gap aperture using PEC undercut etching. This PECA design, discussed in detail next, defines the aperture at the active region, rather than near the p-side surface, thus it could potentially be combined with a BTJ design. In the case of an ITO VCSEL though, the PECA design is likely one of the simplest and most effective ways to achieve a large core-cladding index confinement.

4.2.2. Photoelectrochemically etched Aperture (PECA) VCSEL

In general, when we compare GaAs-based, InP-based, and GaN-based VCSELs, one of the most notable differences between the systems is the way in which the aperture is defined. As was discussed in Section 1.3, GaAs-based VCSELs generally have their aperture defined using the native-oxide aperture. This aperture is formed by hydrolyzing the sidewalls of AlGaAs or AlAs layers in a steam atmosphere furnace at ~400 – 500 °C, to yield lateral oxidation in the form of Al_xO_y.[4,79,80] In InP-based VCSELs, lateral oxidation is not easily achieved, thus the aperture is often formed using a BTJ, or a selective undercut etch close to the active region to form an air-gap aperture.[4,91–93] This air-gap aperture is fabricated by selectively etching InAlAs or AlGaInAs in a solution of citric acid and hydrogen peroxide.[92,93] In III-nitride VCSELs, the dielectric aperture the IIA design have been most commonly used. However the dielectric aperture has been used with a large variation in the degree of success. Theoretical analysis, discussed in Section 4.2.1, suggests that using the standard dielectric aperture design can lead to significant amounts of

diffraction loss,[200,201] which correlates well with some reported experimental results.[8,10,14] Previously, we discussed how the IIA design resulted in a reduction in threshold current density, compared to a standard SiN_x aperture,[8,10,14] however the index contrast between the implanted region and the inner aperture is very small, restricting the ion implanted aperture to fairly large diameter devices (Figure 92(a)). Additionally, even if the lateral confinement for the LP_{01} mode is near to 1, the weak index contrast in the IIA design makes it difficult to effectively confine higher order modes which turn on at higher currents (Figure 92(a), Figure 57). Developing GaN-based VCSELs with aperture designs similar to those used in GaAs-based and InP-based VCSELs would be beneficial, however lateral oxidation and selective undercut wet etching is not easily achieved in the III-nitrides,[249] and the BTJ design was not an option until recently.[11,12] Yet, a number of non-VCSEL III-nitride devices have utilized PEC undercut etching to form an electrical and/or electro-optical aperture.[8,10,11,14] This photoelectrochemical aperture (PECA) was initially demonstrated on optically pumped microdisk lasers.[138,375,376] A PECA was also used to confine current in a III-nitride current aperture vertical electron transistor (CAVETs).[377,378] These studies, and the majority of work investigating PEC etching, have been carried out on epitaxialy layers grown on c-plane GaN,[252,254,256,257,379] which has significantly different etching behavior than m-plane GaN epitaxial layers (Section 3.3.1).[8,250,251] More recently, a III-nitride edge-emitting laser has also been fabricated using the PECA technique.[151,380] Also, the basic mechanism of the PEC undercut etch has been used to form air-gap DBRs.[156–158]

To investigate the PECA in a VCSEL, we processed a series of devices in parallel with the samples demonstrating the use of a TJ intracavity contact.[11,12] Here, the PECA VCSELs had ~7λ cavities, ITO intracavity contacts, and 7QW, A3 nm, B1 nm, EBL5 nm

active region designs. Figure 108(a) shows a schematic of the device immediately after the PEC aperture (PECA) is defined, and after the fabrication process is complete. The fabrication procedure was generally similar to that described in Section 2. Specifically, following epitaxial growth and p-GaN activation, a dry etch was performed to define a mesa with an etch depth below the active MQW and above the sacrificial MQW. Next, a Ti/Au mask was patterned, defining the PECA pattern. This Ti/Au layer also served as a protective layer for the structural support ring surround the core of the device, while simultaneously acting as the PEC cathode in the areas in contact with the n-GaN. The support ring, seen in Figure 108(a) and (b), is necessary because one must make the mesa area large enough for probing the n-contact, however it is also important to reduce the lateral etch distance for the PECA, in order to minimize the structural weakness created when the PECA air-gap is formed. It is of note that sonicating these devices causes catastrophic damage to the majority
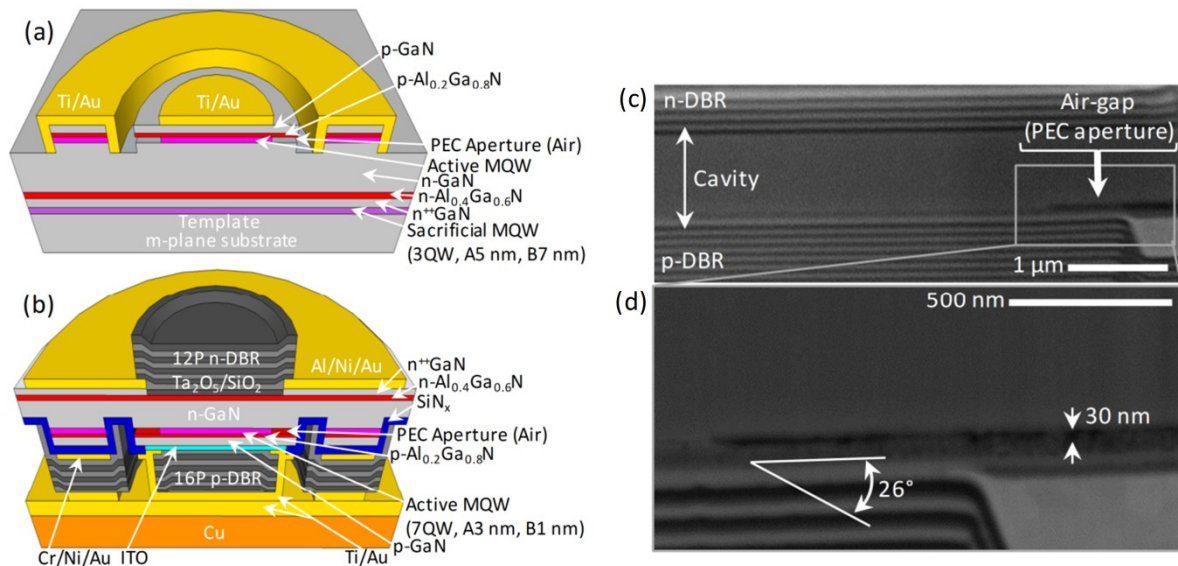
Figure 108 (a) Schematic of a partially processed VCSEL, immediately after the PEC aperture (PECA) is defined. (b) Schematic of a completed PECA VCSEL. (c) and (d) show SEM micrographs of a PECA VCSEL cross-section made using a focused ion beam (FIB). (c) shows a zoomed-out view, giving perspective on the position of the DBRs, cavity, and air-gap PEC aperture. (d) shows a zoomed-in view of the PEC aperture, where the air-gap is seen to be ~30 nm thick (roughly the thickness of the MQW) and the aperture appears to end in an angled etch.

of devices on a chip. Furthermore, using a support ring, instead of a support pillar, or many support pillars, is not recommended for future designs, as it leads to cracking of the n-GaN layer following the flip-chip bond, as is discussed in Section 4.3. Following the Ti/Au deposition, the sample was submerged in 0.1 M KOH and illuminated with a 405 nm LED array (FWHM = 16 nm, ~12 W output power (~65 mW/cm^2)) for 30 minutes, yielding the PECA via undercut etching of the active MQW not protected by the opaque Ti/Au mask. The 0.1 M KOH concentration was chosen in order to minimize the degree of purely chemical roughening on the sidewall of the aperture, however the 30 min etch time was chosen based on a the apparent progression or completeness of the undercut etch, as viewed through an optical microscope. Interestingly, the apparent progression of the undercut etch does not look as clear as one would assume. Specifically, in Figure 109, we can see an optical microscope image and SEM images taken after the Ti/Au hardmask removal
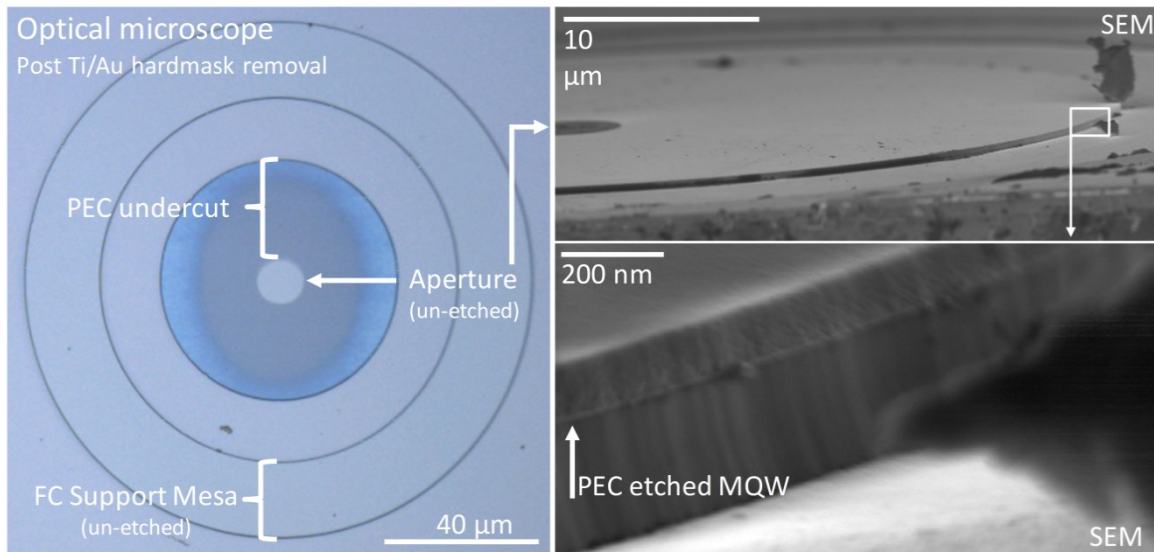
Figure 109 Optical microscope image (left) and SEM images (right) of the PECA following the Ti/Au hardmask removal in aqua regia. In the optical microscope image we can see the flip-chip (FC) support ring, where no etching has occurred. Within the support ring we can see the area where the PEC undercut etch has taken place. In this region, we see there is an oval shaped light blue and dark grey region. It is likely that this contrast is a result of the outer region being over etched by purely chemical processes. The SEM images here show that the etch is visible at the edge of the inner mesa, while the SEM images of the FIB cross-section, shown in Figure 108, confirm that the etch proceeded to the aperture region defined by the Ti/Au mask.

following the 30 min PECA etch. Observing the PEC undercut region, we can see a color contrast is visible, which is likely a result of the two different regions having different thicknesses. However, when we were testing the etch, we began observing the etch after 10 mins, with the Ti/Au mask still in place, and we observed this contrast in the two regions and concluded that it implied the etch was not complete. After another 20 mins without a dramatic change in the appearance of the dark grey region, we decided to stop and strip the Ti/Au mask, yielding the image shown in Figure 109. Thus it is likely that an etch time of < 10 min is sufficient to define the PECA, though a more thorough etching series is necessary. It is possible that as the etch proceeds, the KOH gets depleted, lowering the effect concentration as the etch proceeds toward the edge of the Ti/Au aperture pattern. This would imply that the outer regions are exposed to a higher degree of purely chemical etching effects, which may then cause them to become over etched, leading to their significantly different appearance. The oval shape of light blue/dark grey interface region is a result of the anisotropic PEC etch rate in m-plane QWs, where the a-planes etch slower than the c-planes, and the Ga-face on the c-plane etches slightly faster than the N-face, in m-plane MQWs, due to the piezoelectric polarization in the plane of the m-plane MQWs (Section 3.3.1.1). Regardless, it is apparent that once the etch reaches the edge of the opaque Ti/Au hardmask defining the aperture, photo-generated holes are no longer available to continue the PEC etch process, preventing further etching below the Ti/Au hardmask. That being said though, leaving the sample in KOH longer than is necessary is not recommended as it can lead to purely chemical etching, increasing the probability of the aperture sidewall being rough. After the PECA was defined, and the Ti/Au mask was removed in aqua regia, the remainder

of the device was processed using methods described in Section 2. A schematic cross-section of the completed device is shown in Figure 108(b).

Following fabrication, a focused-ion beam cross-sectional analysis was carried out on one of the VCSELs on the chip. Figure 108(c) and (d) show SEM images taken after forming the cross-section. The PECA is clearly visible, with an air-gap thickness of ~30 nm. This thickness is approximately equal to the active MQW total thickness (7QW, A3 nm, B1 nm), demonstrating the precise nature of this undercut etch technique. Observing the region where the lateral etch stops, we see a slight slope to the edge of the aperture (~26 °). This tapering suggests the Ti/Au mask does not yield a perfect etch selectivity between the areas illuminated during the PEC etch, and the areas covered with the opaque Ti/Au mask. This is likely a result of scattered light at the Ti/Au mask edge. In general, tapered apertures can be beneficial, as demonstrated on GaAs-based VCSELs with tapered oxide apertures,[149] however the specific effects of such tapering depend on the position of the aperture relative to the longitudinal mode peaks and nulls in the cavity, the aperture diameter, and the slope of the tapering. More analysis is necessary to determine the degree to which the tapering observed here effects VCSEL performance.

To analyze the optical confinement properties of the PECA design, we first calculated the effective mode index in the core (within the aperture) and cladding (outside the aperture) in the longitudinal direction, using the 1D TMM. Assuming the cladding region has an air-gap where the active MQW would be, we calculate a core-cladding effective index step, Δn_{eff}, of 0.049 (2.344 - 2.295). For the case of an IIA, Δn_{eff} is predicted to be ~0.001 (Section 4.2.1).[10,11] In InP-based air-gap aperture VCSELs, Δn_{eff} is ~0.4, which is similar to the Δn_{eff} in GaAs-based VCSELs with oxide apertures.[91,93] In

general, increasing Δn_{eff} improves modal confinement, but can also lead to increased scattering loss caused by the aperture.[91] Furthermore, a larger core-cladding index contrast allows higher order modes to be more easily supported in a fiber or VCSEL, due to the increase in the normalize frequency, V (Section 1.4.6).[4,7] Viewing the FIMMWAVE simulated lateral confinement for the LP_{01} mode vs. aperture diameter, shown in Figure 110, we can see that the PECA design significantly improves the lateral confinement for devices with smaller aperture diameters, compared to the IIA design. Specifically, in the IIA design, we saw that the lateral confinement began to drop off when the aperture diameter was reduced to < 10 µm (Figure 92(a)). In contrast, for the PECA design, the lateral confinement does not drop off until < 2 µm, suggesting that the PECA design is particularly useful if one requires VCSELs with very small aperture diameters. These kinds of VCSELs would generally be useful in low-power sensor applications. Unfortunately, due to the low-yield of the PECA VCSELs in this first round of processing, we were unable to experimentally analyze the lasing performance vs. aperture diameter.
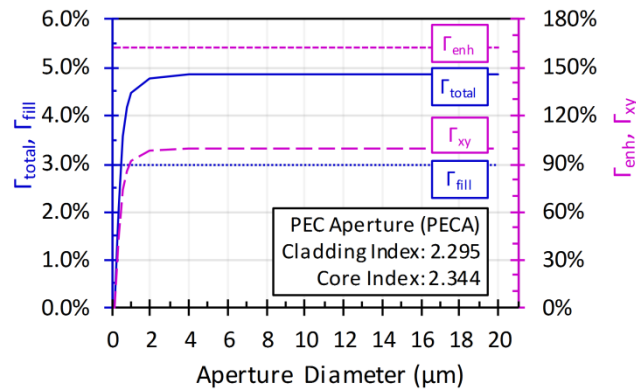
Figure 110 (a) Simulated total confinement factor (Γ_{total}), fill factor (Γ_{fill}), enhancement factor (Γ_{enh}), and lateral confinement factor (Γ_{xy}) vs. aperture diameter for a ~7λ, 7QW, 405 nm PECA+ITO VCSEL. The enhancement factor and fill factor are calculated using a 1D TMM model. The lateral confinement factor is calculated using FIMMWAVE for the LP_{01} mode. The small core-cladding index contrast results in weak confinement of the LP_{01} mode for devices with < 2µm aperture diameters.

Following the determination of the core-cladding index contrast and the analysis of the lateral confinement vs. aperture diameter, we carried out a 2D simulation in COMSOL's "Electromagnetic Waves, Frequency Domain" physics module, to calculate the LP mode profiles for a 12 μm aperture diameter VCSEL. The boundaries of the core-cladding simulation were assumed to be perfect electrical conductors. The basic 2D geometry of the COMSOL model can be seen in **Figure 111**(a). Unlike in the case of the IIA design, where only ~8 LP modes are expected to be confined, with many of the higher order ones being very weakly confined, the PECA design is expected to have many more confined modes. Specifically, using the first-order approximation for the number of confined modes in a core-cladding structure (Eqn. (29)), we find the PECA design is expected to have ~984 confined modes (the normalized frequency is $V \approx 44.38$). Naturally, displaying the mode profile for all of these potential modes is a bit ridiculous here, though one can easily perform the COMSOL simulation to view the mode profiles for the very high order modes. Here, we
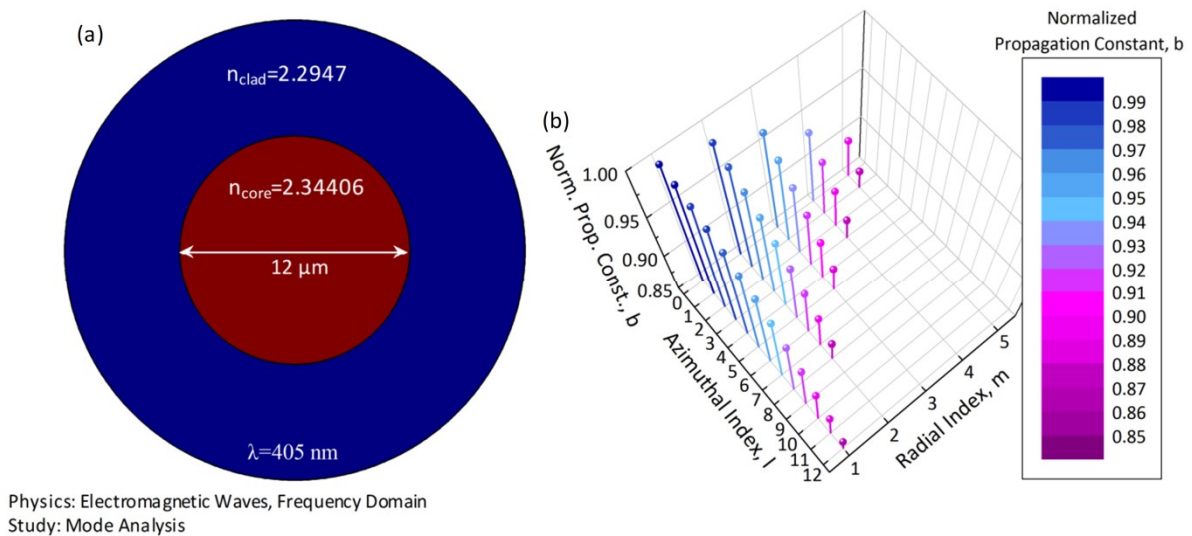
Figure 111 (a) 2D geometry of the core-cladding LP mode simulation carried out using COMSOL. (b) COMSOL results showing the normalized propagation constant, b, for each mode, as a function of the particular modes azimuthal modal index, l, and radial modal index, m. The higher the normalized propogation constant for a given mode, the lower the order of that mode (i.e. the LP_{01} mode is the lowest order (fundamental) mode).

will simply analyze the LP modes of a lower order than that observed experimentally in the actual PECA VCSEL (Figure 114(b)), discussed in more detail later.

The COMSOL simulation results can be seen in Figure 111(b) and Figure 112. In Figure 111(b), we see the normalized propagation constant for each of the modes, as a function of the modes azimuthal and radial index. This plot basically defines the order of the modes, with the higher order modes having a lower propagation constant, while the lower order modes have a higher propagation constant. The order of the mode can also be identified in plots of the normalized propagation constant vs. normalized frequency, such as that shown in Figure 55. Figure 112 show the actual LP modes profiles (E^2-fields), organized according to their radial modal index, l, and azimuthal modal index, m ($LP_{l,m}$). Viewing the different mode profiles, we can see that as the azimuthal index increases, the mode becomes more predominantly localized to the edge of the aperture. This is particularly important because, as has was discussed in Section 4.2.1.2, the current spreading can be highly non-uniform across the aperture, leading to the edge of the aperture having a higher
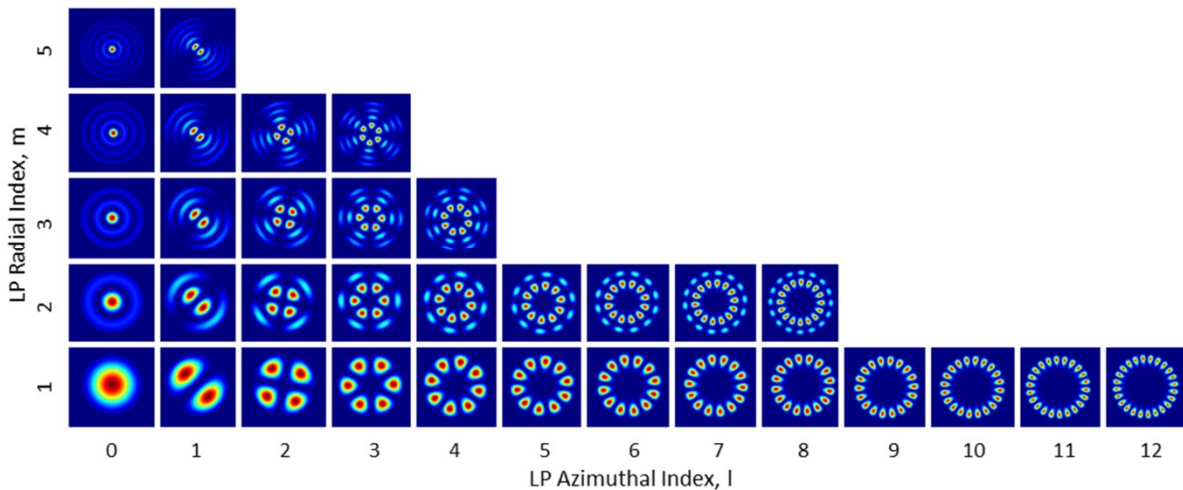
Figure 112 Simulated linearly polarized ($LP_{l,m}$) mode profiles as a function of the radial modal index, *m*, and azimuthal modal index, *l*. The modes shown correspond to those with normalized propogation constants greater than the experimentall observed mode, $LP_{12,1}$. The simulations were carried out using COMSOL's "Electromagnetic Waves, Frequency Domain" module.

injected current, and thus higher gain, than the center of the aperture. This particular effect is likely the predominant cause of the unique lasing characteristics observed in the PECA VCSEL, discussed in detail next. Overall though, comparing the confinement of high order LP modes in the IIA design (Figure 92(b)) to the PECA design, it is clear that the PECA's core-cladding index contrast is sufficient to prevent leaky modes from occurring.

In Figure 113(a) we see the LIV characteristics of a 7λ, 7QW, 12 μm aperture diameter PECA+ITO VCSEL, along with the LIV data from a 12 μm aperture diameter IIA+ITO VCSEL. This IIA+ITO VCSEL was processed in parallel with the PECA VCSEL and was also considered previously when we compared the ITO intracavity contact to the TJ intracavity contact (Section 4.1.4 and 4.2.1.4). Observing the lasing performance of the PECA VCSEL, we see a threshold current of ~25 mA (~22.1 kA/cm^2), with a peak output power of 180 μW at ~100 kA/cm^2, and a top-side differential efficiency, $\eta_{d,top}$, of ~0.07%. The differential resistance is ~42.82 Ω. The device was measured under pulsed operation (0.3% duty cycle, 100 ns pulse width). Figure 113(b) shows the emission spectrum vs. current density for the PECA VCSEL, where the single longitudinal mode lasing wavelength
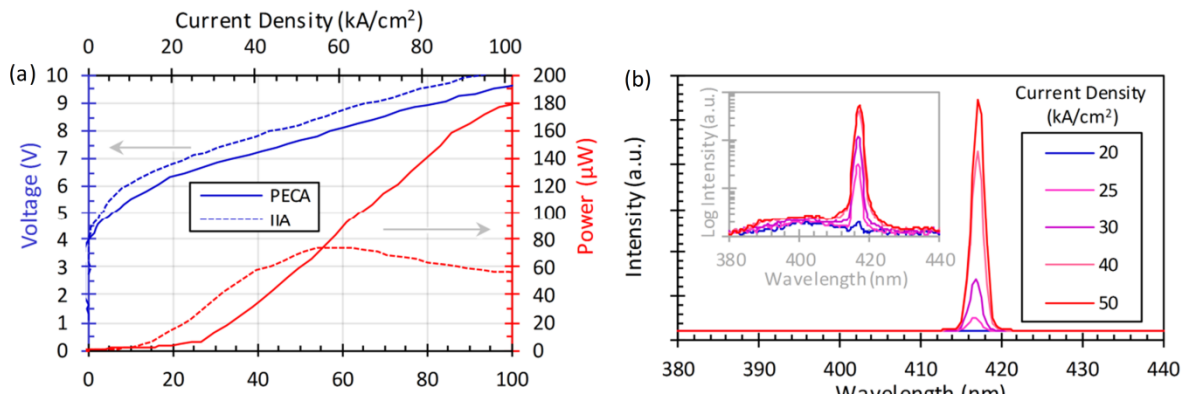
Figure 113 (a) Pulsed LIV characteristics of a PECA+ITO VCSEL and an IIA+ITO VCSEL with 12μm aperture diameters, ~7λ cavities, and 7QW, A3 nm, B1 nm, EBL5 nm active region designs. The threshold current of the PECA VCSEL is ~25 mA (22 kA/cm^2) (b) Emission sprectrum vs. current density for the PECA VCSEL. The lasing wavelength (~417 nm) is offset from the peak spontaneous emission wavelength (~405 nm), due to the accidental incorporation of a Ta$_2$O$_5$ spacer at the start of the n-DBR deposition.

is observed to be ~417 nm, with a spectrometer resolution limited FWHM of ~2 nm. The FWHM and peak wavelength vs. current density can be seen in Figure 114(a), where the lasing wavelength is shown to shift to longer wavelengths with increasing current at a rate of ~0.01 nm per kA/cm^2 injected. Assuming a group index, n_g, of ~3.3,[381] the mode spacing, $d\lambda$, is calculated to be ~21 nm (Eqn. (28)),[3] which is in good agreement with the longitudinal mode spacing observed in the other 7λ nonpolar VCSELs. Moving back to Figure 113(b) and viewing the log-intensity plot in the inset, we see the spontaneous emission peak at ~405 nm. This misalignment between the approximate peak gain wavelength and cavity resonance wavelength was caused by the unintentional incorporation of a Ta$_2$O$_5$ spacer layer at the start of the n-DBR deposition (discussed previously in Section 4.1.4). Such gain offsets have been used advantageously in InP- and GaAs-based VCSELs, however a comprehensive study on the proper gain offset for enhancing the performance of violet GaN-based VCSEL with a PECA design has not been reported. It is of note that simulations of violet c-plane VCSELs, with SiN$_x$ apertures, and hybrid DBR designs, have been reported,[197] which show that the optimal gain offset is dependent on the aperture diameter, lasing linearly-polarized (LP) mode, as well as cavity length. Comparing the PECA+ITO VCSEL to the IIA+ITO VCSEL, we see that the IIA VCSEL has a lower J_{th} (~8 kA/cm^2), however only reaches a peak power of ~80 μW at ~60 kA/cm^2 ($\eta_{d,top} \approx 0.06\%$). It is possible that the difference in $J_{th,}$, but similarity in $\eta_{d,top}$, is a result of a difference in the transparency current density, which would not be unexpected as the two devices have different lasing wavelengths (~410 vs. ~417 nm). The difference in the peak power is likely a result of the IIA design being unable to effectively confine higher order modes that turn on at higher currents. Overall though, more work is necessary to develop a complete
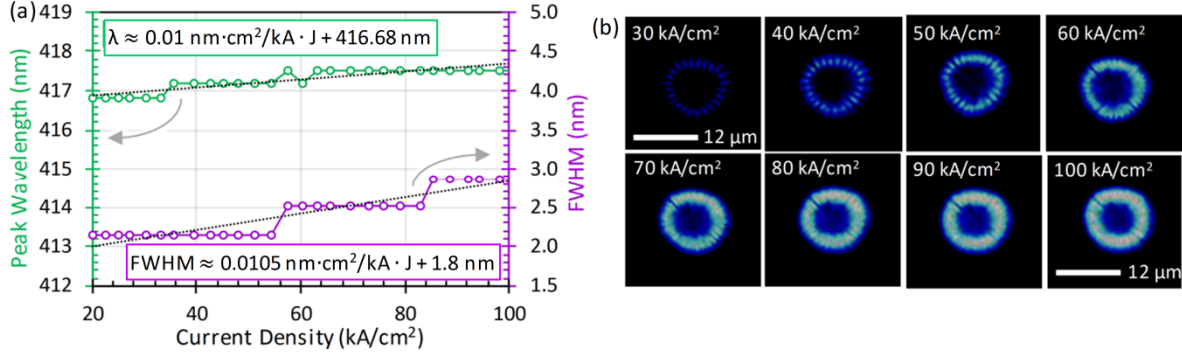
Figure 114 (a) peak lasing wavelength and FWHM (limited by the spectrometer resolution) vs. injected current density. The FWHM and peak wavelength increase with increasing current. (b) near-field emission intensity imaged using optical microscopy at various current densities. The emission profile shows 24 lobes located near the edge of the aperture. This mode profile corresponds to the $LP_{12,1}$ mode.

understanding of the differences and similarities in device performance of IIA and PECA VCSELs, as both devices show significantly different near-field mode profiles, discussed in detail next.

Prior to this report, all VCSELs fabricated by our group have shown filamentary lasing in the aperture.[8,10,11,14] This includes VCSELs with SiN_x apertures,[8,14] and the more recent VCSELs with IIA+ITO and IIA+TJ designs.[10,11] Filamentation has also been observed by other groups researching III-nitride VCSELs.[131–133,137,166,173,175,179] In some publications, the degree of filamentation is difficult to determine due to the imaging camera being over saturated when the image was taken.[171–173] It is of note that the dielectric aperture VCSEL reported by S. Izumi, et. al, appears to have a well-defined mode profile.[174] In comparison to the filamentary lasing observed in our dielectric aperture and IIA designs, the PECA VCSEL near-field emission profile, shown in Figure 114(b), shows a clearly defined single LP mode, meaning the PECA is a single longitudinal and lateral mode device. This suggests that a method for eliminating filamentation is to use a design with a high core-cladding refractive index contrast. Observing Figure 114(b), we see no evidence of higher order modes turning on as the current is increased. Comparing the experimentally observed mode profile, seen in Figure 114(b), to the COMSOL simulations of the mode profiles,

shown in Figure 112, we see that the PECA VCSEL shows $LP_{12,1}$ lasing. A more direct and easily visible comparison can be seen in Figure 115(a). Because this is a high-order mode, one would expect to see the low-order modes lasing as well. If we consider the fact that the n-GaN and ITO layers are fairly thin (~760 nm, and ~47 nm, respectively), we can realize that this device would be expected to have a significant current spreading resistance on the n-side and p-side (ITO). Assuming an n-GaN mobility of 200 cm^2/V-s and a carrier concentration of 2.5×10^{18} cm^{-3}, we estimate the resistivity to be 1.25×10^{-2} Ω-cm, giving a sheet resistance of ~160 Ω. For ITO, the resistivity is ~5×10^{-4} Ω-cm,[9,10] giving a sheet resistance of ~100 Ω. The large spreading resistance on the p- and n-side of the device suggests that the edge of the aperture may receive significantly more injected current than the center of the aperture. Because the high order $LP_{12,1}$ mode has its peak intensity near the aperture edge, while lower order modes have peak intensities nearer to the center of the aperture, one would expect the high-order modes to reach threshold before the low-order modes, due to the non-uniform current spreading. This hypothesis is conceptually shown in
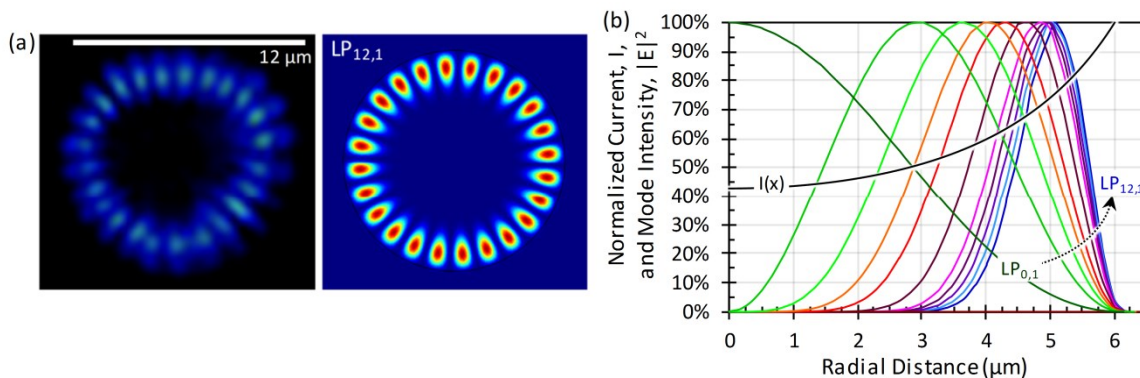
Figure 115 (a) direct comparison of the $LP_{12,1}$ lasing profile observed experimentally in the 12 μm aperture diameter VCSEL (left) and the equivalent COMSOL simulated mode profile (right). The profiles are also shown in Figure 112 and Figure 114(b). (b) Shows the concept of how the various LP mode profiles could be overlapping with the current distribution in the aperture. The injection current profile is based on the preliminary current spreading model results described in Section 4.2.1.2. This figure should only be taken to *conceptually* represent the possible phenomena leading to the single higher-order mode lasing observed in the PECA.

Figure 115, where we have overlain the current spreading profile from *preliminary* simulations, discussed in Section 4.2.1.2, with the cross-sections of the $LP_{l,l}$ mode profiles from the COMSOL simulations. Overall, this analysis is in agreement with the simulation reports from Ref. 197, where non-uniform current spreading in large aperture VCSELs results in higher order LP modes being favored. The researchers also show that longer cavity lengths generally result in a decrease in the order of the primary lasing LP mode and that the aperture diameter, as well as gain offset, can heavily influence mode selection.[197] It is possible that modes higher than the $LP_{12,1}$ mode are not observed because of a higher degree of scattering loss.[91] Thus, it seems likely that the single lateral mode emission results from a balance of non-uniform current spreading, causing lower order modes to be suppressed, and aperture induced scattering loss, which suppresses higher order modes. Overall, the PECA VCSEL results and the IIA VCSEL results suggest that the filamentary lasing observed in the IIA design is a result of gain guiding dominating the mode profile behavior, rather than index guiding, which dominates in the PECA case. It is of note that future PECA VCSELs with TJ intracavity contacts could show further improved performance over these PECA+ITO VCSELs.

In conclusion, these results demonstrate the effectiveness of the PECA air-gap design for providing strong core-cladding index guiding, however more data is necessary to analyze the performance of this particular aperture design. One specific avenue of research which would yield extremely illuminating results would be to analyze the dependence of mode behavior on aperture diameter, similar to what is done in the theoretical simulations shown in Figure 58.[197] That being said, the PECA VCSEL is arguably the most difficult VCSEL design to fabricate due to the weak nature of the PECA air-gap. There are certainly

design methods that could improve the stability of the device, compared to the original demonstration shown here, such as the one outlined in Figure 59. Furthermore, one could potentially introduce a BCB layer, or some other kind of filler, following the formation of the air-gap, which may improve the strength of the structure. Overall though, it seems likely that if the BTJ design (with n^{++}GaN/n-AlGaN/n^{++}GaN) yields strong lateral confinement, then this aperture design will likely be chosen as the most applicable aperture design for industry-grade III-nitride VCSELs, due to its comparatively simple processing and improved structural stability.

4.3. Flip-Chip Submounts & Bonding

In this final section we will discuss in more detail the developments in the flip-chip submount selection and the bonding processed that occurred between the original nonpolar VCSEL demonstrations,[8,14,15] and our latest IIA+TJ and PECA+ITO VCSELs results.[11–13] Overall, the topic of flip-chip bonding gets very little discussion, as the final VCSEL results are much more interesting, however the flip-chip bonding process represented one of the major road-blocks to achieving improved yield and reduce operating voltage in the ITO intracavity contact VCSELs.

In general, the most common types of flip-chip bonding are thermal compression bonding and wafer fusion/bonding. Wafer fusion has been popularly employed in InP-based devices,[86,87,382–384] however a number of III-nitride based devices have also been fabricated using wafer fusion.[385,386] In III-nitride VCSELs, there are certainly some interesting design options that could be explored using wafer-fusion, however thermal compression bonding is generally much simpler than wafer fusion, as it uses metal-to-metal bonding, which greatly

reduces the chance of traps or poorly conducting bond interfaces. The Au-Au compression bond, used in all reported nonpolar VCSELs, is by far the simplest bond and results in a fairly strong bond, however the Au-Sn eutectic bond offers a much greater bond strength, though it is more costly and complicated. Another common bond is the indium bump bond. This is a very weak bond, but it is often used in pick-and-place processes in the semiconductor industry. Overall, the issues observed in the VCSEL bonding process have never been related to the strength of the actual metal-metal bonding interface, thus the Au-Au bonding process is the ideal option for research grade devices.

In our initial processing designs, used to fabricate the VCSELs reported in Refs. 8,14,15, the Au-Au thermocompression bond was carried out at 300 °C for 2 hrs. in an air ambient. A Ti/Au sapphire substrate was used as the submount. In the initial test of the IIA VCSEL, the final devices had extremely high operating voltages, which prevented them from lasing. With this observation, we went back and measured the IV characteristics of the devices at the various stages of the process. Our initial belief was that the IBD conditions were resulting in p-GaN plasma damage, thus the IBD deposition power was optimized, as was discussed in Section 3.6 (Figure 77). Yet the IBD damage did not completely account for the dramatic increase in voltage observed in the final devices. Measuring the IV characteristics before and after the flip-chip bond at 300 °C revealed that this step was leading to catastrophic voltage damage. To solve this issue, we carried out a series analyzing the effect of different bonding conditions on the IV characteristics of partially processed VCSELs. The results from this study are summarized in Figure 116. Comparing Figure 116(a) to (b) and (c), we can see that by capping the ITO layer with the dielectric p-DBR, the effect of the flip-chip bonding conditions on the IV characteristics is changed.
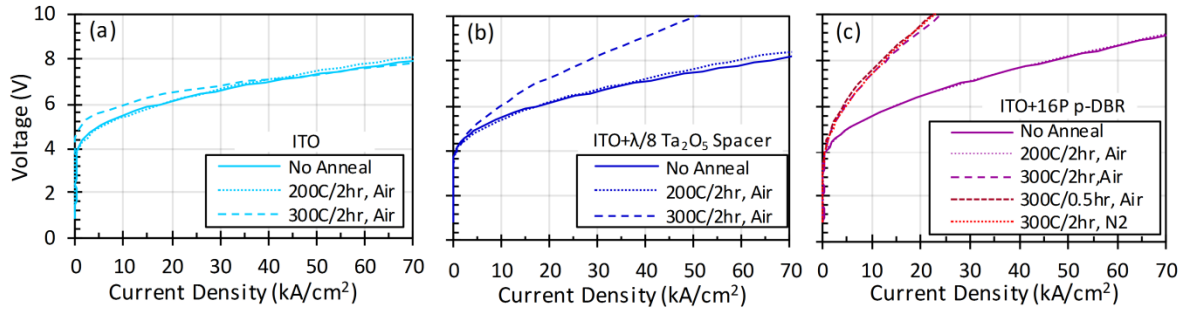
Figure 116 Summary of the optimization of Au-Au thermocompression flip-chip bonding conditions. (a) shows IV curves from samples processed up to the ITO deposition and etch step, which have been exposed to the following annealing conditions: no annealing, annealing at 200 °C for 2hrs in air, and annealing at 300 °C for 2 hrs in Air. No catastrophic increase in voltage is observed. (b) shows the similar experiment to (a), but now the sample has been coated with the $1/8^{th}$-wave Ta_2O_5 spacer layer prior to being exposed to the various annealing conditions. Annealing at 200 °C for 2 hrs shows no significant change in IV curves, while annealing at 300 °C results in a dramatic increase in the series resistance of the device. (c) shows the case where the full p-DBR has been deposited and the sample has been tested after no annealing, and annealing at 200 °C for 2 hrs in air, 300 °C for 2 hrs in air, 300 °C for 30 mins in air, and 300 °C for 2 hrs in N_2. The IV curve of the sample annealed at 200 °C for 2 hrs in air is essentially identical to that of the unannealed sample's IV curve. The fact that reducing the 300 °C annealing time does not reduce the degree of voltage damage implies that the process resulting in the voltage increase is likely thermally activated and not kinetically limited. Furthermore, the 300 °C anneal in N_2 shows catastrophic voltage increase, implying that possible impurity incorporation from performing the anneal in air is not a cause of the voltage damage.

Furthermore, going from only the thin $1/8^{th}$-wave Ta_2O_5 spacer layer as the cap, to the full p-DBR, leads to an increase in the voltage damage occurring when the samples are annealed (bonded) at 300 °C. This suggests that there is either an impurity in the dielectric layer that diffuses into the ITO/p-GaN upon bonding at 300 °C, or that by having the dielectric layer we effectively block some impurity in the ITO from diffusing out into air. A SIMS analysis on these samples was carried out, however because it is very difficult to resolve interfaces in SIMS, and because it is even more difficult to accurately analyze a stack of dielectric, ITO, and III-nitride materials simultaneously, no conclusive source of the voltage damage was identified. Regardless, in Figure 116(b) and (c), we can see that this unusual IV damage can be mitigated by moving from doing the bond at 300 °C to bonding at 200 °C. In Figure 116(c) we can also gain more insight into the nature of this IV damage by observing that performing the 300 °C bond for 30 mins, instead of 2 hrs., still results in the same degree of IV damage. The fact that changing the annealing time does not change the degree of

251

damage, while reducing the temperature completely mitigates it, implies that the IV damage process is not a kinetically limited process, but is rather a thermodynamic process that has some activation energy between 200 °C and 300 °C. Furthermore, Figure 116(c) shows that performing the 300 °C anneal in a nitrogen ambient, instead of air, yields that same catastrophic increase in voltage, thus the IV damage process is not related to the atmospheric conditions of the furnace in which the bonding is performed. Based on these results, we modified the standard VCSEL process flow to have the flip-chip bond performed at 200 °C for 2 hrs., in an air ambient. This is the process that was used on all reported nonpolar VCSELs following the early demonstrations reported in Ref. 8,14,15.

Beyond the actual flip-chip bonding conditions, we have also carried out a number of investigations on different flip-chip submounts. In general, in selecting a submount for a nonpolar VCSEL, one must take into account 3 primary factors: (1) the thermal conductivity of the submount, (2) the thermal expansion coefficient of the submount, (3) the chemical stability of the submount in KOH. Some other secondary factors to keep in mind when choosing a submount are the surface roughness, thickness of the submount, and cost/wafer or sheet. Table 4 summarizes the characteristics of the primary submounts of interest for III-nitride flip-chip devices. Some other submounts not listed here, which are generally of intrest for flip-chip devices, include Ga_2O_3, ZnO, AlN, and boron nitride (BN) wafers, however all of these react strongly with KOH so they cannot be used in our substrate removal process. Table 4 shows the various substrate that have been tested for the nonpolar VCSEL process. In all iterations of the VCSEL process, the submount is coated in Ti/Au (10/ 500 nm). In the older reports on nonpolar VCSELs,[8,10,14,15] a sapphire substrate was used as the submount due to the large inventory of such substrates at UCSB, its low cost,

Table 4 Summary of typical material properties for different flip-chip submounts. The values quoted are for near-room temperature. The KOH stability assumes low KOH concentrations ($\leq$ 1M) and room temperature conditions. Values are mostly taken from NSM Archive and MTI Corp. data sheets. The success or failure of the tested submounts in the nonpolar VCSEL process is indicated by a check-mark or x-mark.

Submount	Thermal Conductivity, κ_L (W/Kcm)	Thermal Expansion Coeff., α_T (°C^{-1})	KOH Stable	Thickness	Surface Roughness	Cost	Tested
Sapphire	0.25	8×10^{-6}	Yes	~0.3 mm	<1 nm	$$	Yes (✓)
GaN	1.30	$\alpha_c=4\times10^{-6}$ $\alpha_a=6\times10^{-6}$	Yes	~0.3 mm	<1 nm	$$$	Yes (✓)
SiC	3.6	4×10^{-6}	Yes	~0.3 mm	<1 nm	$$$ $	Yes (✗)
Si	1.48	3×10^{-6}	Yes	~0.5 mm	<1 nm	$	Yes (✗)
Cu	3.85	17×10^{-6}	Yes	$\geq$0.6 mm	<50 μm	$	Yes (✓)
Al (mirror)	2.05	22×10^{-6}	No	$\geq$0.8 mm	<10 μm	$	Yes (✗)
BeO	3.3	8×10^{-4}	Yes	~0.5 mm	<50 μm	$	No
Graphite	$\kappa_{L,AB}=4.0$ $\kappa_{L,C}=0.04$	$\alpha_{AB}=0.5\times10^{-6}$ $\alpha_C=6.5\times10^{-6}$	Yes	~0.5 mm	<1 nm	$$	No
Diamond on Si	22	1.0×10^{-6}	Yes	~0.5 mm	<1 nm	$$$ $	No

And its stability in KOH. Unfortunately, sapphire has a terrible thermal conductivity (~0.25 W/Kcm), thus it is not an ideal candidate for a CW VCSEL. As was shown in Section 1.4.4.3 and 1.4.5.2, the largest barrier to efficient thermal dissipation in a dual dielectric DBR flip-chip VCSEL is actually the dielectric DBR itself, thus the submounts thermal conductivity is more of a second-order concern that becomes critical once the thermal dissipation efficiency around the p-DBR has been maximized. As we have discussed, increasing the cavity thickness from 7λ to 23λ will likely lead to efficient thermal dissipation around the p-DBR, making the submount the next critical layer for dissipating heat. Motivated by this fact we have tested a number of submount alternatives to sapphire.

In C. Holders optimization of the VCSEL process, he tested GaN and Si substrates. The GaN worked effectively, however it is not an ideal option due to the expensive nature of bulk GaN. C. Holder observed that samples bonded to Si substrates (at 300 °C for 3 hrs. in air) cracked, leading to this option being abandoned. It is of note that the Nichia VCSELs

are bonded to Si substrates, though these reports are extremely vague about any of the actual device design or processing details.[171–173] It is likely that the Nichia bonding process is much more sophisticated than our current bonding process, which simply uses a graphite fixture with screws in place to clamp the chip and submount together.

Following C. Holders work,[16] we went on to test SiC and Cu substrates. Optical microscope images taken after the flip-chip bond and substrate removal process for samples bonded to SiC, sapphire, and Cu submounts are shown in Figure 117. Here, we can see that bonding to SiC resulted in cracking around the aperture area. Around the time of this test, B. P. Yonkee also tested a flip-chip bond to SiC of an LED sample with a metallic mirror and observed no cracking. Based on this result, and the general observations from many other samples, it appears that the cracking in the VCSELs is predominantly a result of the strain induced by the dielectric DBR. This is not very surprising because the DBR layers themselves have an order of magnitude lower thermal expansion coefficient than the III-nitride layers alone, which would introduce significant stress to the structure upon heating and cooling the sample for the flip-chip bond. Moving from the 300 °C bonding conditions to the 200 °C bonding conditions did reduce the degree of cracking observed in samples bonded to SiC, however the large aperture diameter devices in particular continued to show
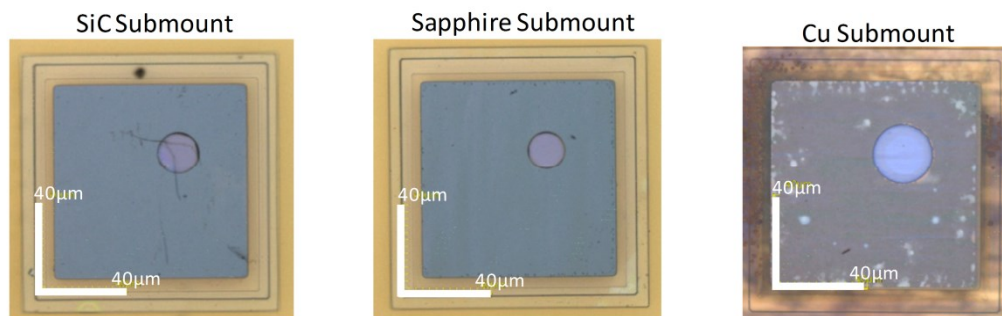
Figure 117 Optical microscope images taken after the flip-chip bond and substrate removal process for samples bonded to SiC, sapphire, and Cu submounts. The sample bonded to SiC shows cracking near the aperture.

cracking, thus SiC was eliminated as a possible submount.

As can be seen in Figure 117, the sample bonded to Cu does not show cracking, however using Cu introduces a number of complications of its own. In our first test of Cu substrates, we simply used unpolished Cu blocks and used e-beam deposition to put down the Ti/Au coating, prior to flip-chip bonding. Upon substrate removal, the bond was observed to fail at the Cu/(Ti/Au) interface, as is shown in Figure 118(a). Though this failure of the bond reduced the yield, a number of VCSELs still made it through the process for testing. We hypothesized that the failed bond could be due to two causes: (1) the extremely rough nature of the Cu block surface, and (2) the formation of a copper oxide layer prior to the deposition of the Ti/Au. We decided to attempt to solve both these issues simultaneously, thus in our next iteration of the process we first mechanically polished the Cu submounts, prior to sputtering down the Ti/Au layers, after an in-situ Ar plasma clean. While the plasma clean and Ti/Au sputtering eliminated the failed bond issue, the polishing introduced another complication. Specifically, because the polishing was performed using a
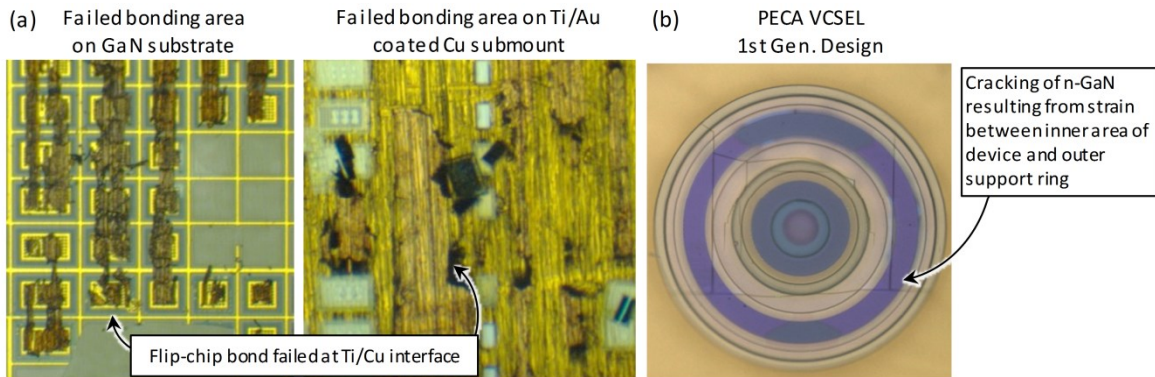
Figure 118 (a) optical microscope images following the substrate removal process on samples bonded to Cu blocks with e-beam deposited Ti/Au coatings. The image on the left shows the samples on the original m-plane GaN substrate which failed to bond to the Ti/Au layer peeling off the Cu submount, while the image on the right shows an area on the Cu submount where the Ti/Au layer has peeled off. (b) optical microscope image of a VCSEL geometry with a circular support ring, used in the devices reported in Ref. 11–13. A cross-sectional schematic of this basic design can be found in the discussion on the PECA (Figure 108). The strain in the n-GaN layer, created by the dielectric layers in the center of the device, and the dielectric layers in the support ring, led to cracking of the devices.

felt pad and a fine grit slurry, the outer edges of the Cu submounts polished more than the inner area, due to the build-up of slurry at the edges, resulting in a hill-like shape across the surface of the Cu submounts. This hill-like shape then prevented many of the VCSELs from bonding to the substrate, reducing the yield of the process. It is possible that the poor adhesion was not related to the surface roughness of the original Cu submounts, thus one could potentially achieve a high yield using unpolished Cu submounts with Ti/Au sputtered coatings, however we have not tried this yet.

It should be noted that beyond the bonding issues, the other problem we encountered when using Cu submounts was that the thickness of the blocks was only slightly less than the separation between the lithography mask and the contact aligner chuck, making it extremely difficult to properly align the n-DBR and the n-contacts following the flip-chip bond and substrate removal. This particular issue was easily overcome by reducing the Cu submount thickness in the next processing iteration, however it is an important general consideration if one is considering using metallic submounts, as they tend to be much thicker than the dielectric- or semiconductor-based submounts. It

In an attempt to overcome the issues with the Cu submounts, we decided to test Al submounts, as they can be purchased with a mirror-like surface finish. However, Al is highly susceptible to KOH etching, thus we attempted to coat the entire top and bottom surface with Ti/Au prior to submerging the sample in KOH. Unfortunately, the Ti/Au layer was not sufficient to protect the Al, and severe bubbling and etching of the Al submount occurred, which led to delamination of the Ti/Au layers, exposing more Al for etching. Thus, Al submounts were also abandoned as an option.

After looking into the potential options for submounts more, we determined that BeO was an ideal candidate for a submount. BeO is commonly used in the semiconductor industry due to its high thermal conductivity and electrical resistivity. Having a submount that is thermally conductive and electrically insulating can be favorable if one wishes to design a patterned flip-chip submount. For basic nonpolar VCSELs research, BeO is advantageous due to its high thermal conductivity, low cost, and chemical stability in KOH. It is of note that BeO has a very low thermal expansion coefficient (Table 4), however it is not clear how this would impact the bonded VCSELs. As of this writing, BeO was being evaluated in the DOE outlined in Figure 78. Beyond BeO, some other substrates of interest are graphite and diamond coated Si. Graphite substrates are inexpensive, however the thermal conductivity is anisotropic and is only high in the AB crystal plane. Diamond on Si also has a high thermal conductivity, however these substrates are extremely expensive.

In summary, the optimal submount for the nonpolar VCSEL process has yet to be identified. As mentioned previously, unpolished Cu submounts with sputtered Ti/Au coatings could give the high yield results desired, however the fact that BeO is thermally conductive while electrically insulating makes it a more interesting candidate as it opens up to potential for more advance VCSEL flip-chip designs. Specifically, if it was not necessary to probe the top-mesa of the VCSEL, one could dramatically reduce the mesa size of the device. This could be achieved by having a patterned BeO submount and performing an aligned flip-chip bond so that both the n-contacts and p-contacts were bonded to the submount, so that one would simply probe the submount alone, and not the actual VCSEL structure. This would also make it easier to integrate wire bonding into the VCSEL structure, allowing one to completely package a VCSEL or a VCSEL array.

5. Conclusions & Future Directions

"Follow your heart, but take your brain with you"

– Alfred Adler

"Your time is limited, don't waste it living someone else's life. Don't be trapped by dogma, which is living the result of other people's thinking. Don't let the noise of other opinions drown your own inner voice. And most important, have the courage to follow your heart and intuition, they somehow already know what you truly want to become. Everything else is secondary"

– Steve Jobs

In our early work on III-nitride VCSELs, C. Holder made significant advancements in developing the basic nonpolar VCSEL process flow and epitaxial design, resulting in the successful demonstration of the first nonpolar VCSEL. Yet at that time we struggled to reproduce the results and the critical parameters limiting performance were not clear. Now, with the rapid progress made in optimizing the epitaxial structure and process flow, along with the highly parallel testing of multiple aperture designs, we can more clearly see the path forward, and it is simply a matter of making the samples and doing the measurements. It seems that the greatest barriers to achieving efficient III-nitride VCSEL performance are now clearly identified and can be overcome through dedicated research. Naturally, there are many alterations to device design that can be studied, but there are also many fundamental performance properties of III-nitride VCSELs that can now be studied due to the improved yield of the IIA process overall. Below, we list a number of potential research fronts that could help improve the scientific understanding of III-nitride VCSEL performance and operating principles.

- **Future Directions**

- n^{++}GaN/n-AlGaN/n^{++}GaN BTJ VCSEL
  - Measure BTJ leakage by varying BTJ diameter from 20 µm to 0 µm and test IV.[4]
- CW lasing of nonpolar VCSELs
- High power VCSEL arrays with 100 % polarization
- RF modulation characteristics of VCSELs and VCSEL arrays (in collaboration with KAUST)
- Lasing vs. position on wafer
- Analysis of far-field vs. near-field emission profiles
- Epitaxial optimization of…
  - Barrier thickness
  - QW thickness
  - Number of QWs
  - EBL thickness
  - Modulated doping profile
  - p^{++}GaN/n^{++}GaN TJ contact (increase p- and n- doping)
- Optimization of gain offset parameter for room temperature or high temperature operation
- Test graphite as alternative to BeO (toxic), boron nitride (etches in KOH), AlN (etches in KOH)).
- Cascade QW VCSELs.[259,361–363]
- Develop a robust PECA VCSEL design
- Test a QW intermixed aperture (in collaboration with KAUST)
- Demonstrate substrate recycling with VCSELs using PEC undercut process

Many of these future directions have been stated throughout this thesis, however, in each section, I have also made an effort to include the less noteable research fronts that would help illuminate the areas we have only begun to explore over the last several years. Perhaps it is overly optimistic of me, but it does seem that we are currently witnessing the dawn of the III-nitride VCSEL. With the breakthroughs we have described in this thesis, as

well as the recent III-nitride VCSEL results from Sony[174,180] and NCTU[277], it is apparent that the age of researchers struggling to achieve lasing in III-nitride VCSELs is over. With the threshold current densities now being at reasonable levels, the door is open to explore more design schemes in III-nitride VCSELs. Through this research III-nitride VCSELs will be brought nearer to commercialization, bringing them one step closer to directly improving the quality of life for humanity as a whole.

Appendix

"Knowledge may give weight, but accomplishments give luster, and many more people see than weigh."

– Lord C. Field

"We don't get a chance to do that many things, and everyone should be really excellent. Because this is our life. Life is brief, and then you die, you know? And we've all chosen to do this with our lives. So it better be damn good. It better be worth it."

– Steve Jobs

A1. A Note to Graduate Students

Whether you like it or not, your success as a graduate student will be largely measured by your *number* of publications. I emphasize number because many publications are simply "letters" while others are full length papers, and sadly you will look better if you write 4 short letters than if you write 2 full length papers. Furthermore, I have found that full length papers end up requiring you to spend a lot more time hashing out little details here and there, when you could be working on your next breakthrough experiment. Regardless, in whatever you do, always keep in mind that your success and your performance as a graduate student is measured in publications. If you have multiple options, always choose the one that has the highest potential for publication. Realizing that publications are your measure of success will motivate you to frame your research in terms of publishable stories. It will also help you improve the quality of your data collection, as it will encourage you to take the time to collect publishable data, instead of partial data that gets the point across to you or your team, but would not stand up to a peer review. Often time's graduate students think that

their success is measured by the number of results they generate or the amount of time they spend in the lab, but if you do not publish those results then only the people in your group will really recognize you as a hard working person. From a more humanitarian perspective, humanity will only really remember your contribution if you publish, and the purpose of science and engineering is truly to advance humanity as a whole.

A2. Making Figures

Most of the figures presented in this thesis were made using Microsoft Excel with "Daniel's XL Toolbox", a free plugin available online. Figures with 3D schematics were made using SketchUp, while the labels and arrows were arranged in Excel, prior to exporting the completed figure using Daniels XL Toolbox. Though there are many other plotting software available other than Excel, such as OriginPro, it does seem to be the most capable of integrating rapid data analysis and versatile plotting/figure making. That being said, it does not have as many plot types as origin, including polar plots and 3D plots, and it is also lacking in its curve-fitting ability and the availability of different trend-line formulas, thus being able to use OriginPro is very useful. Without the Daniel's XL Toolbox plugin installed, Excel is virtually useless because it cannot export high quality (600 dpi) images easily. However, with this plugin, one can easily design figures with the true print-ready font size and dimensions and export 600 dpi images of the figures. In general, I design figures to have 10 pt. axes labels, 9 pt. axes numbers, and 8 pt. legend font. I generally use 1 pt. line widths for plot lines. It is also a good idea to imagine how you can make a plot as informative as possible. Specifically, try to think of ways to add information to a plot so that an experienced reader in the field may glance at the plot and see all the critical information

they need to fully consider the result. Naturally, you do not want to make the plot over crowded though, because that can make analyzing the data confusing, so it is a bit of a balancing act. Besides making a single plot, Daniels XL Toolbox also makes it very easy to make figures from multiple plots (i.e. Figure (a), (b), (c), etc.) directly in Excel. This makes the whole process much faster and simpler than importing figures into unnecessarily advanced image editing software, such as Photoshop, which is what most researchers do. Finally, keep in mind, figures matter. Make a figure that is appealing to look at and people will find it more enjoyable to read about your work. More importantly though, if you make an excellent figure, it will be something that you are proud of, and you shouldn't waste your time doing things you're not proud of. Happy figure making!

A3. Data Collection & Analysis

A3.1. LabView

Often times the complexity involved in characterizing a device is not discussed. Yet characterization is essential for rapidly acquiring and analyzing data. More specifically, automating characterization is an essential skill to have. There are so many little stupid things in life that people just do repetitively over and over again because they are habit. They think, "oh this is just the way things are" until someone comes along and automates or eliminates the little trivial task and saves humanity lifetimes of hours wasted doing some kind of triviality. This is how I think of characterization. I have seen countless people spend hours and hours doing IV measurements by hand, writing down each point by hand, or taking a measurement a billion times and sitting at their desk a billion times and selecting all

the cells and rows to plot the data. Just stop it! There is a better way! Go spend a day learning LabView and you will save yourself and so many other people hours of time, more importantly, you will save them hours of their life! Go save lives! Learn LabView! I learned LabView simply by watching the first 5 tutorials here: Link to LabView Tutorials on YouTube. After watching these tutorials I just started building programs and learned the rest on the go.

A3.2. Excel Macros & Visual Basic

Although you can build LabView programs to automatically plot and analyze the data you collected (also using LabView), sometimes other users of your programs will want the data in a simple .csv file, instead of a pre-formatted Excel file. Because of this, it is also very useful to learn Excel Macros, as you can then build custom codes to compile .csv or .txt files and automatically plot the data. Basically any repetitive task you are doing in Excel can be automated using Macros, so it is a great skill to have and it is very easy to learn. I don't have any particular tutorials I recommend, but you can find tons of advice online and tons of YouTube tutorials to get you started. Also there are many codes that people post online that you can easily modify for your own purposes.

A4. Process Flow

The nonpolar VCSELs process is still a work in progress. Currently, much of the process is defined, however there are certainly many areas that could be modified to improve the general processing procedure, increase yield, or reduce processing time. The

specific process below is the last draft of the VCSEL process flow I developed before graduating.

Table 5

160203 VCSEL Process Flow - IIA,PECA,BTJ+TJ or ITO		
Authors: John Leonard		
General Prep	Flip-chip substrate Prep	See end of process follower
	PR Bench	Prep PRs and check expiration date
		SPR220-3.0
		SPR220-7.0
		nLOF2020
		nLOF2035
Calibration (Day 1)	MOCVD	Grow xrd and emission wavelength calibrations for all relevant layers in the device
Calibration (Day 2)	XRD	Analyze XRD calibration samples using ~35 min 2-theta/omega scans (6-8hrs XRD time)
		Fit the XRD data by simulating the structure and adjusting the parameters by hand, until a good fit is obtained (do not simply fit the thickness fringes)
	Quicktest	Deposit 80 um diameter Pd/Au p-contacts using old CTLM mask and measure LIVS on the emission wavelength calibration sample, using 4-pt probe method
	Computer	Adjust the growth times and QW temperatures on the layers of interest in all the recipes. $\lambda_{EL}>\lambda_{FP}$ is not desirable (i.e. $\lambda_{EL}<\lambda_{FP}$ or $\lambda_{EL}=\lambda_{FP}$ is preferred). $\lambda_{sacrificial}>405$nm is required for PEC etching. $\lambda_{sacrificial}>420$nm is required for observation under Fluorescence microscope
Growth (Day 3)	MOCVD	Grow the desired VCSEL Series
Begin Processing (Day 4)	Furnace	600C, Air, 15min
	Quicktest	Solder In dots onto corners only. Do not press through shadow mask, it will leave residue. Measure Quicktest data for the VCSELs. Save all spectrum and IV data. Regrow if power or voltage is bad
Remove Indium	Acid Bench	3:1 HCl:HNO3 Aqua Regia, 3x 10min, mix new batch each iteration, wait 5min for boiling, 120C on hotplate. End with DI+Tergitol clean, N2 dry
Mesa 1 Litho	Solvent Bench	Sonicate on high: 2min Ace, 2min Iso, 3x 30s DI+Tergitol Dump&Rinse, N2 dry **UV VCSEL: Spray with pipette (no sonicate)**
	PR Bench	Dehydration bake, 2min 110°C, let cool 30sec
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **SPR220-3.0** Program 5 (3000rpm 30s)
		edge-bead removal from short edges

		Soft bake, 115°C 90s
	Contact Aligner	Expose **"Mesa 1"**, 7.5mW/cm^2, **25s,** No Filter, Black chuck, **Hard contact**
	Develop Bench	**Post exposure bake 115°C 60s**
		Develop in AZ300MIF **60s**
		30 sec DI rinse flowing, N$_2$ dry
	Microscope	Inspect, develop more if necessary
	PEII	O2 plasma descum, 300 mT, 100 W, 30sec
Mesa 1 Etch	RIE5	Load bare carrier wafer
		Standard O$_2$, BCl$_3$/Cl$_2$ preclean (Dan_01 (~10min pump down, 10min O$_2$ clean))
		Load samples onto carrier wafer, no oil
		Dan_05 (120 nm/min) (etch past active QW but not past sacrificial QW) BCL$_3$ (10sccm, 10mT, 100W, 2min), Cl$_2$ (10sccm, 5mT, 200W, 2.5 min)
	Solvent Bench	Preheat 1165 Stripper for 10 min, 80 C
		Sonicate on High 1165 at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry **UV VCSEL:** Treat in 1165 at 80C for 5min. Brush using swab soaked in DI+Tergitol for 1min. Repeat 1165 and swab step. Rinse 3x 30s DI+Tergitol Dump, N2 dry
BTJ Only: Grow n++GaN Layer	**BTJ: MBE**	Give samples to Erin Young for growth of first n++GaN layer only. Model the structure in VERTICAL to get correct thickness
		After regrowth, remove indium using standard aqua regia process
BTJ Only: BTJ Aperture Litho	Solvent Bench	Sonicate on low: 2min Ace, 2min Iso, 3x 30s DI+Tergitol Dump&Rinse, N2 dry **UV VCSEL: Spray with pipette (no sonicate)**
	PR Bench	Dehydration bake, 2min 110°C, let cool 30sec
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **SPR220-3.0** Program 5 (3000rpm 30s)
		edge-bead removal from short edges
		Soft bake, 115°C 90s
	Contact Aligner	Expose **"Aperture"**, 7.5mW/cm^2, **25s,** No Filter, Black chuck, **Hard contact**
	Develop Bench	**Post exposure bake 115°C 60s**
		Develop in AZ300MIF **60s**
		30 sec DI rinse flowing, N$_2$ dry
	Microscope	Inspect, develop more if necessary
	PEII	O2 plasma descum, 300 mT, 100 W, 30sec
BTJ Only: BTJ Aperture Etch	RIE5	Load bare carrier wafer
		Standard O$_2$, BCl$_3$/Cl$_2$ preclean (Dan_01 (~10min pump down, 10min O$_2$ clean))
		Load samples onto carrier wafer, no oil

		Dan_05 (120 nm/min) (etch through n++GaN & p++GaN to ~1/2 p-GaN thickness) BCL_3 (10sccm, 10mT, 100W, 2min), Cl_2 (10sccm, 5mT, 200W, 2.5 min)
	Solvent Bench	Preheat 1165 Stripper for 10 min, 80 C
		Sonicate on low 1165 at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry **UV VCSEL:** Treat in 1165 at 80C for 5min. Brush using swab soaked in DI+Tergitol for 1min. Repeat 1165 and swab step. Rinse 3x 30s DI+Tergitol Dump, N2 dry
IIA & PECA Only: Aperture hardmask Litho	Solvent Bench	Sonicate on low: 3min Ace, 3min Iso, 3x 30s DI+Tergitol Dump&Rinse, N_2 dry **UV VCSEL: Spray with pipette (no sonicate)**
	PR Bench	Dehydration bake, 2min 110°C, let cool 30sec
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **nLOF2020** Program 5 (3000rpm 30s)
		edge-bead removal from short edges
		Soft bake, 110°C 90s
		Expose **"Aperture"**, **10s**,7.5mW/cm^2, No Filter, Black chuck, **Hard contact**
		Post exposure bake 110°C 60s
		Develop in AZ300-MIF **50s**
		2min DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
	UV Ozone	20min (~6A/min)
IIA & PECA Only: Aperture Hardmask Dep	Acid Bench	**1:1 HCl:DI 30s, 3x 30s DI Dump&Rinse, N2 Dry**
	Ebeam 4	Deposit Ti/Au 200A (1A/s)/ 2000A (1A/s→100A,3A/sec→500A, 6A/sec→2000A)
	Solvent Bench	Preheat 1165 Stripper for 10 min, 80 C
		Sonicate on Low 1165 at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry **PECA or UV VCSEL:** Treat in 1165 at 80C for 5min. Brush using swab soaked in DI+Tergitol for 1min. Repeat 1165 and swab step. Rinse 3x 30s DI+Tergitol Dump, N2 dry
	Microscope	Inspect, liftoff more if necessary
PECA Only: Define Aperture	Packaging Lab	PEC etch to undercut exposed active region area 405 nm LED Array, 3.5A (35V?), (~12 W output power, ~65 mW/cm^2), FWHM = 16 nm. **0.1M KOH? (recommend testing, lower may be better)** **30 mins? (recommend testing, less time may be sufficient)**
	Microscope	Inspect, etch more if necessary
IIA Only: Define Aperture	Leonard Kroko, Inc.	Ship samples to Leonard Kroko
		wafer size: ~1cm^2
		Ion: Al, Dose: 10^{15} ions/cm^2, Energy: 20 keV, Normal incidence
		~3-4 day turn-around

267

	Acid Bench	3:1 HCl:HN03 Aqua Regia, 3x 10min, mix new batch each iteration, wait 5min for boiling, 120°C on hotplate. End with DI+Tergitol clean, N2 dry
	3D Microscope	Inspect, strip more if necessary
Intracavity Contact Dep	**ITO:** E-beam 2	Coload DSP sapphire and Si samples. Deposit heated substrate multi-layer ITO (Crucible 3, Film 2, Tooling Factor 79.8, 30sccm O2 (0.28mTorr), Predep at 1A/sec for 1 min, Dep at 0.1A/sec, Frequency 7/7, 5nm(50C(100sp)), 45nm(400C(850sp)), Cool in O2 till T<150C. This should yield ~46.6nm ITO, as measured by ellipsometry.
	ITO: 4-pt Probe (optional)	Measure DSP Sapphire and Si samples
	ITO: Ellipsometer (optional)	Measure Si Sample using model: 140526_50nm ITO-Si_NoneGradedIndex_2.2_All Fits On. Save Model Table, Psi & Delta vs Wavelength, and Index dispersion Data. Note optical thickness and correct Ta2O5 1/8th wave layer to compensate for any cavity thickness offset
	ITO: Carry 500 (optional)	Measure DSP sapphire sample
	IIA+TJ or BTJ:	Give samples and structure to Erin Young for TJ growth. For BTJ, regrow the remaining current spreading layer (n-GaN or n-AlGaN) and the metal contact layer (n++GaN) Model the structure in VERTICAL to get correct thickness
		After regrowth, remove indium using standard aqua regia process
	TJ, BTJ, or ITO: AFM (optional)	Measure intracavity contact RMS roughness (1um x 1um scan)
Intracavity Contact Etch Litho	Solvent Bench	Sonicate on low: 3min Ace, 3min Iso, 3x 30s DI+Tergitol Dump&Rinse, N$_2$ dry **PECA or UV VCSEL: Spray with pipette (no sonicate)**
	PR Bench	Dehydration bake, 2min 110°C, let cool 1min
		Spin **LOL 2000**, 2 krpm, 10 krpm/s, 30s (~250 nm thick)
		Edge Bead removal, Clean backside with EBR 100
		Softbake, 170 °C, 5min, let cool 2 min
		Spin **SPR220-3.0** Program 5 (3000rpm 30s)
		edge-bead removal from short edges
		Soft bake, 115C 90s
		Expose "**Intracavity-Dielectric**", **25s**,7.5mW/cm2, No Filter, Black chuck, hard contact
		Post exposure bake 115°C 60s
		Develop in AZ300-MIF 60s+10s undercut
		2min DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
	PEII	O2 plasma descum, 300 mT, 100 W, 30sec
ITO or TJ Etch	**ITO: RIE 2**	Standard O$_2$ preclean (20sccm, 125mTorr, **500V**, 20min)
		Standard MHA precoat (pump down from O$_2$ clean, check MHA set-pts. (4/20/10 sccm, 75mTorr, **500V**, 20min)

		Load samples
		MHA etch (4/20/10sccm, 75mTorr, **350V**, 5min)
		O$_2$ clean (20sccm, 125mTorr, **350V**, 10min)
	IIA+TJ & BTJ: RIE5	Load bare carrier wafer
		Standard O$_2$, BCl$_3$/Cl$_2$ preclean (Dan_01 (~10min pump down, 10min O$_2$ clean))
		Load samples onto carrier wafer, no oil
		Dan_05 (120 nm/min) (IIA+TJ: Etch through p++GaN. BTJ: Etch >10 nm past regrown current spreading layer (n-GaN or n-AlGaN/n++GaN))BCL$_3$ (10sccm, 10mT, 100W, 2min), Cl$_2$ (10sccm, 5mT, 200W, 2.5 min)
SiNx Sidewall Dep	IBD	(Optional) Calibrate SiNx Dep with 40◦ angle
		Dep >=250 nm SiNx with 40◦ angle (side-wall is ~3/4 as thick as planar dep), with Si test wafer co-loaded (~1hr)
	Ellipsometer	Check SiNx thickness of Si test wafer
	Solvent Bench	Preheat 1165 Stripper for 10 min, 80 C
		Sonicate on Low 1165 at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry
		PECA or UV VCSEL: Treat in 1165 at 80C for 5min. Brush using swab soaked in DI+Tergitol for 1min. Repeat 1165 and swab step. Rinse 3x 30s DI+Tergitol Dump, N2 dry
	3D Microscope	Inspect, strip more if necessary
p-DBR Litho	Solvent Bench	Sonicate on low: 3min Ace, 3min Iso, 3x 30s DI+Tergitol Dump&Rinse, N$_2$ dry **PECA or UV VCSEL: Spray with pipette (no sonicate)**
	PR Bench	Dehydration bake, 2min 110°C, let cool 1min
		Spin **LOL 2000**, 2 krpm, 10 krpm/s, 30s (~250 nm thick)
		Softbake, 170 °C, 5min, let cool 2 min
		Spin **nLOF2035** Program 5 (3000rpm 30s)
		edge-bead removal from short edges
		Softbake, 110°C 90s
	Contact Aligner	Expose **"p-DBR"**, 7.5mW/cm2, **10s**, No Filter, Black chuck, **Hard contact**
	PR Bench	**Post exposure bake 110C 60s**
	Develop Bench	Develop in AZ300MIF **50s+10s** undercut
		2min DI rinse flowing, N$_2$ dry
	Microscope	Inspect, develop more if necessary
	UV Ozone	20min (~6A/min)
p-DBR Dep	IBD	Calibration Sample(s), Ellipsometer/Filmetrics, **(UV VCSEL: Carry 500)**
		Deposit 16 periods SiO$_2$/Ta$_2$O$_5$, **beginning with Ta$_2$O$_5$ spacer if ITO design used. Do not use spacer if TJ design used for >=405 nm VCSELs** (Optical thickness of spacer = 3/8 - ITO optical Thickness). Co-load a DSP sapphire 1/4 wafer
	Carry 500	Measure and Model reflectance on SSP sapphire sample
	Solvent	Preheat 1165 Stripper for 10min, 80°C

	Bench	Sonicate on Low 1165 at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry **PECA or UV VCSEL:** Treat in 1165 at 80C for 5min. Brush using swab soaked in DI+Tergitol for 1min. Repeat 1165 and swab step. Rinse 3x 30s DI+Tergitol Dump, N2 dry
	3D Microscope	Inspect, liftoff more if necessary
Mesa2 Etch Litho	Solvent Bench	Sonicate on low: 3min Ace, 3min Iso, 3x 30s DI+Tergitol Dump&Rinse, N_2 dry **PECA or UV VCSEL: Spray with pipette (no sonicate)**
	PR Bench	pre-heat hot-plate to 50C
		Dehydration Bake, 2min 110°C, let cool 1min
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **SPR 220-7.0** Program 5 (3000rpm 30s) (~7µm)
		edge-bead removal from short edges
		Soft bake, 115C 120s
	Contact Aligner	Expose **"Mesa2",** 7.5mW/cm2, No Filter, Black chuck, **Hard contact, 60s**
	PR Bench	**wait 20min before bake. Bake 50C 60s, 115C 60s**
	Develop Bench	Develop in AZ300-MIF, **70s**
		2min DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
	PEII	O2 plasma descum, 300 mT, 100 W, 30sec
Mesa2 Etch	RIE5	Load bare carrier wafer
		Standard O_2 preclean (Dan_01 (~20min pump down, 10min O_2 clean, BCl$_3$ Coat))
		Load samples onto carrier wafer, no oil
		BCL$_3$ (10sccm, 10mT, 100W, 2min), Cl2 (10sccm, 5mT, 200W) **single-mode or multi-mode: Dan_05 (3,000 nm/25 min)**
		Soak sample in DI for 2min, N_2 dry
	Solvent Bench	Preheat 1165 Stripper for 10min, 80C
		Sonicate on Low 1165 at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry **PECA or UV VCSEL:** Treat in 1165 at 80C for 5min. Brush using swab soaked in DI+Tergitol for 1min. Repeat 1165 and swab step. Rinse 3x 30s DI+Tergitol Dump, N2 dry
	3D Microscope	Inspect, strip more if necessary.
Intracavity contact metal and PEC cathode Litho	Solvent Bench	Spray with pipette (no sonicate) 2min Ace, 2min Iso, 3x 30s DI+Tergitol Dump&Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110°C, let cool 1min
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **nLOF2020** Program 5 (3000rpm 30s)
		Scrape off edge-bead from short edges
		Softbake, 110C 90s
	Contact Aligner	Expose **"Intracavity Metal, PEC Cathode"**, 7.5mW/cm2, **10s**, No Filter, Black chuck, **Hard contact**
	PR Bench	**Post exposure bake 110C 60s**
	Develop	Develop in AZ300MIF **50s**

	Bench	2min DI rinse flowing, N_2 dry
	Microscope	Inspect, develop more if necessary
	PEII	O2 plasma descum, 300 mT, 100 W, 30sec
Intracavity Contact metal and PEC cathode Dep	**IIA+TJ & BTJ Only:** Acid Bench	1:1 HCl:DI 30s, 3x 30s DI Dump&Rinse, N2 Dry
	ITO: Ebeam 4	**ITO:** Deposit Cr/Ni/Au 250A/200A/10,000A, **planetary angle&rotate.**
	IIA+TJ & BTJ: Ebeam 4 or Sputter 4	**Ebeam 4:** Deposit Ti/Au (200A/10,000A) **planetary angle&rotate.** **Sputter 4:** Load samples using clips (Optional, load flip-chip substrates as well) Adjust Ti and Au gun angle to "20" Run J_Leonard Ti-Au Dep (Ar plasma clean, Ti (10nm), Au (500nm))
	Solvent Bench	Preheat 1165 Stripper for 10min, 80C
		Sonicate on Low 1165 at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry
		PECA or UV VCSEL: Treat in 1165 at 80C for 5min. Brush using swab soaked in DI+Tergitol for 1min. Repeat 1165 and swab step. Rinse 3x 30s DI+Tergitol Dump, N2 dry
	3D microscope	Inspect, liftoff more if necessary
Flip-chip Substrate Only: Metal Dep	Acid Bench	**1:1 HCl:DI 30s, 3x 30s DI Dump&Rinse, N2 Dry**
	Sputter 4	Load flip-chip substrates on double side sticky tape
		Adjust Ti and Au gun angle to "20"
		Run J_Leonard Ti-Au Dep (Ar plasma clean, Ti (10nm), Au (500nm))
Flip-Chip Thermo-compression Bond	Scribing bench	Cleave off the areas of chip where edge bead removal occurred (scribe the backside then nick the edge of the chip)
		Label back of flip-chip substrates
	Acid Bench	Basic Piranha clean (1:1:1 NH4OH:H2O2:H2O). 80C. 5 min warm-up. Clean flip-chip substrates and samples for 10 min
	PEII	O2 plasma descum, 300 mT, 100 W, 30sec
	Litho Bay Furnace	Load Samples in graphite fixtures. Clamp finger tight + 1/8 turn Bond at 200 C/2 hrs.
PEC Lift-off	Packaging Lab	PEC etch to remove substrate 405 nm LED Array, 3.5A (35V?), (~12 W output power, ~65 mW/cm^2), FWHM = 16 nm. 1M KOH ~4 hrs
	Microscope	Inspect, etch more if necessary
n-contact litho	Solvent Bench	Spray with pipette (no sonicate) 2min Ace, 2min Iso, 3x 30s DI+Tergitol Dump&Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110°C, let cool 1min
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **nLOF2020** Program 5 (3000rpm 30s)

		Scrape off edge-bead from short edges
		Softbake, 110C 90s
	Contact Aligner	Expose "**n-contact**", 7.5mW/cm2, **10s**, No Filter, Black chuck, **Hard contact**
	PR Bench	**Post exposure bake 110C 60s**
	Develop Bench	Develop in AZ300MIF **50s**
		2min DI rinse flowing, N_2 dry
	Microscope	Inspect, develop more if necessary
	PEII	O2 plasma descum, 300 mT, 100 W, 30sec
n-contact Dep	**Sputter 4**	Load samples using clips
		Adjust Ti and Au gun angle to "20"
		Run J_Leonard Ti-Au Dep (Ar plasma clean, Ti (10nm), Au (500nm))
	Solvent Bench	Preheat 1165 Stripper for 10min, 80C
		Treat in 1165 at 80C for 5min. Brush using swab soaked in DI+Tergitol for 1min. Repeat 1165 and swab step. Rinse 3x 30s DI+Tergitol Dump, N2 dry
	3D microscope	Inspect, liftoff more if necessary
	AFM (optional)	Measure RMS roughness in the aperture
PEC Stop-etch	Packaging Lab	PEC etch to AlGaN stop-layer Hg-Xe Arc Lamp, **345nm long-pass filter** 0.001M KOH 3min (~50nm/min) **This step is still under optimization**
	3D Microscope	Inspect
	AFM (optional)	Measure RMS roughness in the aperture
Cavity Resonance Check	Laser Testing Station	Run Spectra vs. IV program up to 70-100 kA/cm2 on each corner and middle of device
		Check cavity resonance
	Vertical	If resonance is off, model in vertical adding a Ta2O5 n-side spacer to re-align the resonance with the peak gain. **Make sure you do the vertical simulation without the n-DBR as well, since this layer will increase the cavity length**
n-DBR Litho	Solvent Bench	Spray with pipette (no sonicate) 2min Ace, 2min Iso, 3x 30s DI+Tergitol Dump&Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110C, let cool 1min
		Spin **LOL 2000**, 2 krpm, 10 krpm/s, 30s (~250 nm thick)
		Edge Bead removal, Clean backside with EBR 100
		Softbake, 170 °C, 5min, let cool 2 min
		Spin **nLOF2035** Program 5 (3000rpm 30s)
		Edge Bead removal, Clean backside with EBR 100
		Softbake, 110C 90s
	Contact Aligner	Expose "N-DBR", 7.5mW/cm2, **10s**, No Filter, Black chuck, hard contact.

	PR Bench	**Post exposure bake 110°C 60s**
	Develop Bench	Develop in AZ300MIF **50s**
		2min DI rinse flowing, N_2 dry
	Microscope	Inspect, develop more if necessary
	UV Ozone	20min (~6A/min)
DBR Dep	IBD	Calibration Sample(s), Ellipsometer/Filmetrics **(UV VCSEL: Carry 500)**
		Deposit 12 periods SiO_2/Ta_2O_5 n-DBR on VCSEL and DSP sapphire 1/4 wafer
DBR Liftoff	Solvent Bench	Preheat 1165 Stripper for 10min, 80°C
		Treat in 1165 at 80C for 5min. Brush using swab soaked in DI+Tergitol for 1min. Repeat 1165 and swab step. Rinse 3x 30s DI+Tergitol Dump, N2 dry
	3D Microscope	Inspect, liftoff more if necessary
	Solvent Bench	no ultrasonic: 3min Ace, 3min Iso, 3x 30s DI+Tergitol Dump&Rinse, N2 dry
LIV Test		Congrats, you made a VCSEL!

References

[1]   Iga, K., "Surface-Emitting Laser — Its Birth and Generation of New Optoelectronics Field," IEEE J. Sel. Top. Quantum Electron. **6**(6), 1201–1215 (2000).

[2]   Iga, K., "Vertical-cavity surface-emitting laser: Its conception and evolution," Jpn. J. Appl. Phys. **47**, 1–10 (2008).

[3]   Coldren, L. A., Corzine, S. W.., Mašanović, M. L., Diode Lasers and Photonic Integrated Circuits, John Wiley & Sons, Inc., Hoboken, NJ, USA (2012).

[4]   Michalzik, R., VCSELs: Fundamental, Technology and Applications of Vertical-Cavity Surface-Emitting Lasers, 1st ed., Springer Berlin Heidelberg, Heidelberg (2013).

[5]   Wilmsen, C. W., Temkin, H.., Coldren, L. A., Vertical-Cavity Surface-Emitting Lasers: Design, Fabrication, Characterization, and Applications, Cambridge University Press, New York (2001).

[6]   Piprek, J., Semiconductor Optoelectronic Devices: Introduction to Physics and Simulation, Elsevier, San Diego (2003).

[7]   G. P. Agrawal., Fiber-Optic Communication Systems (4th Ed.), 4th ed., John Wiley & Sons, Inc. (2010).

[8]   Holder, C. O., Leonard, J. T., Farrell, R. M., Cohen, D. A., Yonkee, B., Speck, J. S., DenBaars, S. P., Nakamura, S.., Feezell, D. F., "Nonpolar III-nitride vertical-cavity surface emitting lasers with a polarization ratio of 100% fabricated using photoelectrochemical etching," Appl. Phys. Lett. **105**(3), 031111 (2014).

[9]   Leonard, J. T., Cohen, D. A., Yonkee, B. P., Farrell, R. M., Denbaars, S. P., Speck, J. S.., Nakamura, S., "Smooth e-beam-deposited tin-doped indium oxide for III-nitride vertical-cavity surface-emitting laser intracavity contacts," J. Appl. Phys. **118**(14), 145304 (2015).

[10]   Leonard, J. T., Cohen, D. A., Yonkee, B. P., Farrell, R. M., Margalith, T., Lee, S., DenBaars, S. P., Speck, J. S.., Nakamura, S., "Nonpolar III-Nitride Vertical-Cavity Surface-Emitting Lasers Incorporating an Ion Implanted Aperture," Appl. Phys. Lett. **107**, 011102 (2015).

[11]   Leonard, J. T., Young, E. C., Yonkee, B. P., Cohen, D. a., Margalith, T., DenBaars, S. P., Speck, J. S.., Nakamura, S., "Demonstration of a III-nitride vertical-cavity surface-emitting laser with a III-nitride tunnel junction intracavity contact," Appl. Phys. Lett. **107**(9), 091105 (2015).

[12]   Leonard, J. T., Young, E. C., Yonkee, B. P., Cohen, D. A., Shen, C., Margalith, T., Ng, T. K., DenBaars, S. P., Ooi, B. S., et al., "Comparison of Nonpolar III-nitride

Vertical-Cavity Surface-Emitting Lasers with Tunnel Junction and ITO Intracavity Contacts," Proc. SPIE Gall. Nitride Mater. Devices XI (2016).

[13] Leonard, J. T., Yonkee, B. P., Cohen, D. A., Megalini, L., Lee, S., Speck, J. S., DenBaars, S. P.., Nakamura, S., "Nonpolar III-Nitride Vertical-Cavity Surface-Emitting Laser with a Photoelectrochemically Etched Air-Gap Aperture," Appl. Phys. Lett. **108**, 031111 (2016).

[14] Holder, C. O., Speck, J. S., DenBaars, S. P., Nakamura, S.., Feezell, D., "Demonstration of Nonpolar GaN-Based Vertical-Cavity Surface-Emitting Lasers," Appl. Phys. Express **5**(9), 092104 (2012).

[15] Holder, C., Feezell, D., Speck, J. S., DenBaars, S. P.., Nakamura, S., "Demonstration of nonpolar GaN-based vertical-cavity surface-emitting lasers," Proc. SPIE Vertical-Cavity Surface-Emitting Lasers XVII **8639**, 863906 (2013).

[16] Holder, C. O., "Nonpolar GaN-based VCSELs," Thesis(September), University of California, Santa Barbara (2013).

[17] Johnson, R. H.., Kuchta, D. M., "30 Gb/s Directly Modulated 850 nm Datacom VCSELs," IEEE Conf. Lasers Electro-Optics/Quantum Electron. Laser Sci. CLEO/QELS(May), 28–30, San Jose, CA (2008).

[18] Blokhin, S. A., Lott, J. A., Mutig, A., Fiol, G., Ledentsov, N. N., Maximov, M. V., Nadtochiy, A. M., Shchukin, V. a.., Bimberg, D., "Oxide-confined 850 nm VCSELs operating at bit rates up to 40 Gbit/s," Electron. Lett. **45**(10), 501 (2009).

[19] Lear, K. L.., Al-Omari, A. N., "Progress and issues for high speed vertical cavity surface emitting lasers," Proc. SPIE Vertical-Cavity Surface-Emitting Lasers XI **6484**, 64840J – 1–12 (2007).

[20] Lear, K. L., Hietala, V. M., Hou, H. Q., Ochiai, M., Banas, J. J., Hammons, B. E., Zolper, J. C.., Kilcoyne, S. P., "Small and Large Signal Modulation of 850 nm Oxide-Confined Vertical Cavity Surface Emitting Lasers," Adv. Vert. Cavity Surf. Emit. Lasers Ser. OSA Trends Opt. Photonics **15**, 69–74 (1997).

[21] Jewell, J., Graham, L., Crom, M., Maranowski, K., Smith, J.., Fanning, T., "1310nm VCSEL in 1-10Gb/s commercial applications," Proc. SPIE Vertical-Cavity Surface-Emitting Lasers X **6132**, 613204–613204 – 9 (2006).

[22] Doany, F. E., Schow, C. L., Baks, C. W., Kuchta, D. M., Pepeljugoski, P., Schares, L., Budd, R., Libsch, F., Dangel, R., et al., "160 Gb/s bidirectional polymer-waveguide board-level optical interconnects using CMOS-cased transceivers," IEEE Trans. Adv. Packag. **32**(2), 345–359 (2009).

[23] Giaretta, G., White, W., Wegmuller, M.., Onishi, T., "High-speed (11 Gbit/s) data transmission using perfluorinated graded-index polymer optical fibers for short interconnects (<100 m)," IEEE Photonics Technol. Lett. **12**(3), 347–349 (2000).

[24] Eben, K.., Polishuk, P., "Present State-of-the-art of Plastic Optical Fiber (POF) Components and Systems," Brighton, MA (2004).

[25] Johnson, K., Hibbs-Brenner, M., Hogan, W.., Dummer, M., "Advances in red VCSEL

technology," Adv. Opt. Technol. **2012** (2012).

[26]   Larsson, A., "Advances in VCSELs for communication and sensing," IEEE J. Sel. Top. Quantum Electron. **17**(6), 1552–1567 (2011).

[27]   Rudd, M. J., "A laser Doppler velocimeter employing the laser as a mixer-oscillator," J. Phys. E. **1**(7), 723–726 (1968).

[28]   Pruijmboom, A., Schemmann, M., Hellmig, J., Schutte, J., Moench, H.., Pankert, J., "VCSEL-based miniature laser-Doppler interferometer," Proc. SPIE Vertical-Cavity Surface-Emitting Lasers XII **6908**, 69080I – 69080I – 7 (2008).

[29]   Grabherr, M., Gerlach, P., King, R.., Jager, R., "Integrated photodiodes complement the VCSEL platform," Proc. SPIE Vertical-Cavity Surface-Emitting Lasers XIII **7229**, 72290E – 72290E – 9 (2009).

[30]   Raoul, X., Bosch, T., Plantier, G.., Servagent, N., "A double-laser diode onboard sensor for velocity measurements," IEEE Trans. Instrum. Meas. **53**(1), 95–101 (2004).

[31]   Mul, F. F., Koelink, M. H., Weijers, a L., Greve, J., Aarnoudse, J. G., Graaff, R.., Dassel, a C., "Self-mixing laser-Doppler velocimetry of liquid flow and of blood perfusion in tissue.," Appl. Opt. **31**(27), 5844–5851 (1992).

[32]   Shinohara, S., Yoshida, H., Ikeda, H., Nishide, K. I.., Sumi, M., "Compact and high-precision range finder with wide dynamic range and its application," IEEE Trans. Instrum. Meas. **41**(1), 40–44 (1992).

[33]   Lutwak, R., Rashed, A., Varghese, M., Tepolt, G., Leblanc, J., Mescher, M., Stark, C., Serkland, D. K., Geib, K. M., et al., "The Chip-Scale Atomic Clock – Prototype Evaluation," 39th Annu. Precise Time Time Interval Meet., 269–290, The Institute of Navigation (ION) (2007).

[34]   Serkland, D. K., Geib, K. M., Peake, G. M., Lutwak, R., Rashed, A., Varghese, M., Tepolt, G.., Prouty, M., "VCSELs for Atomic Sensors," Proc. SPIE **6484**(505), 648406–1 – 10 (2007).

[35]   National Aeronautics and Space Administration (NASA)., "NASA's Journey to Mars: Pioneering Next Steps in Space Exploration," Washington, DC (2015).

[36]   Mukoyama, N., Otoma, H., Sakurai, J., Ueki, N.., Nakayama, H., "VCSEL array-based light exposure system for laser printing," Proc. SPIE **6908**, 69080H – 69080H – 11 (2008).

[37]   Wallace, J., "Photonics Products: High-power Laser-Diode Arrays: Diode arrays are compact, high-power light dynamos," Laser Focus World **51**(01), 75–80 (2015).

[38]   Pruijmboom, A., "High-Power VCSEL arrays make ideal industrial heating systems," Laser Focus World **50**(12), 21–26 (2014).

[39]   Moench, H., Conrads, R., Deppe, C., Derra, G., Gronenborn, S., Gu, X., Heusler, G., Kolb, J., Miller, M., et al., "High-power VCSEL systems and applications," Proc. SPIE High-Power Diode Laser Technol. Appl. XIII **9348**, 93480W – 1 (2015).

[40] Monch, H.., Derra, G., "High Power VCSEL Systems," Laser Tech. J. **2**, 43–47 (2014).

[41] Haas, H., "Wireless data from every light bulb," TED Glob. 2011, 2011, <https://www.ted.com/talks/harald_haas_wireless_data_from_every_light_bulb?language=en>.

[42] Suganya, U.., Subhalakshmipriya, C., "Li-Fi (Light Fidelity) Technology," Int. J. Res. Comput. Appl. Robot. **3**(1), 26–32 (2015).

[43] Gottumukkala, S.., Pasupuleti, K., "Li-Fi (Light Fidelity)-The Future Technology in Wireless Communication," Discov. Int. Dly. J. **28**(103), 29–33 (2015).

[44] Takai, I., Harada, T., Andoh, M., Yasutomi, K., Kagawa, K.., Kawahito, S., "Optical Vehicle-to-Vehicle Communication System Using LED Transmitter and Camera Receiver," IEEE Photonics J. **6**(5), 1–14 (2014).

[45] Austen, K., "The Trouble with Wearables," Nature **525**, 22–24 (2015).

[46] Shi, J., Sheu, J., Wang, C., Chen, C., Hsieh, C., Chyi, J.., Lai, W., "Linear Cascade Arrays of GaN-Based Green Light-Emitting Diodes for High-Speed and High-Power Performance," IEEE Photonics Technol. Lett. **19**(18), 1368–1370 (2007).

[47] McKendry, J. J. D., Massoubre, D., Zhang, S., Rae, B. R., Green, R. P., Gu, E., Henderson, R. K., Kelly, a. E.., Dawson, M. D., "Visible-Light Communications Using a CMOS-Controlled Micro-Light- Emitting-Diode Array," J. Light. Technol. **30**(1), 61–67 (2012).

[48] McKendry, J. J. D., Green, R. P., Kelly, A. E., Gong, Z. G. Z., Guilhabert, B., Massoubre, D., Gu, E.., Dawson, M. D., "High-Speed Visible Light Communications Using Individual Pixels in a Micro Light-Emitting Diode Array," IEEE Photonics Technol. Lett. **22**(18), 1346–1348 (2010).

[49] Lee, C., Shen, C., Oubei, H. M., Cantore, M., Janjua, B., Ng, T. K., Farrell, R. M., El-Desouki, M. M., Speck, J. S., et al., "2 Gbit/s data transmission from an unfiltered laser-based phosphor-converted white lighting communication system," Opt. Express **23**(23), 29779 (2015).

[50] Lee, C., Zhang, C., Cantore, M., Farrell, R. M., Oh, S. H., Margalith, T., Speck, J. S., Nakamura, S., Bowers, J. E., et al., "4 Gbps direct modulation of 450 nm GaN laser for high-speed visible light communication," Opt. Express **23**(12), 16232 (2015).

[51] Dimitrov, S.., Haas, H., Principles of LED Light Communications: Towards Networked Li-Fi, Cambridge University Press, West Nyack, NY, USA (2015).

[52] Arnon, S., Visible Light Communication, Cambridge University Press, Cambridge, UK (2015).

[53] Poher, V., Grossman, N., Kennedy, G. T., Nikolic, K., Zhang, H. X., Gong, Z., Drakakis, E. M., Gu, E., Dawson, M. D., et al., "Micro-LED arrays: a tool for two-dimensional neuron stimulation," J. Phys. D. Appl. Phys. **41**, 094014 (2008).

[54] Chhajed, S., Xi, Y., Li, Y. L., Gessmann, T.., Schubert, E. F., "Influence of junction

temperature on chromaticity and color-rendering properties of trichromatic white-light sources based on light-emitting diodes," J. Appl. Phys. **97**(2005), 1–8 (2005).

[55]   Chow, W. W.., Crawford, M. H., "Analysis of lasers as a solution to efficiency droop in solid-state lighting," Appl. Phys. Lett. **107**(14), 141107 (2015).

[56]   Wierer, J. J.., Tsao, J. Y., "Advantages of III-nitride laser diodes in solid-state lighting," Phys. Status Solidi **212**(5), 980–985 (2015).

[57]   Pourhashemi, A., Farrell, R. M., Hardy, M. T., Hsu, P. S., Kelchner, K. M., Speck, J. S., Denbaars, S. P.., Nakamura, S., "Pulsed high-power AlGaN-cladding-free blue laser diodes on semipolar," Appl. Phys. Lett. **151112**(2013), 2–6 (2014).

[58]   Denault, K. A., Cantore, M., Nakamura, S., DenBaars, S. P.., Seshadri, R., "Efficient and stable laser-driven white lighting," AIP Adv. **3**(7), 072107 (2013).

[59]   Neumann, A., Wierer, J. J., Davis, W., Ohno, Y., Brueck, S. R. J.., Tsao, J. Y., "Four-color laser white illuminant demonstrating high color-rendering quality.," Opt. Express **19**(S4), A982–A990 (2011).

[60]   Hainich, R. R.., Bimber, O., Displays, Fundamentals & Applications, CRC Press LLC, Boca Raton, FA (2011).

[61]   Thompson, A. C., Stoddart, P. R.., Jansen, E. D., "Optical Stimulation of Neurons," Curr. Mol. Imaging **3**, 162–177 (2014).

[62]   Anan, T., Yamada, M., Nishi, N., Kurihara, K., Tokutome, K., Kamei, A.., Sugou, S., "Continuous-wave operation of 1.30 μm GaAsSb/GaAs VCSELs," Electron. Lett. **37**(9), 566–567 (2001).

[63]   Kilper, D. C., Quochi, F., Cunningham, J. E.., Dinu, M., "High-Speed Dynamics of GaAsSb Vertical-Cavity Lasers," 438–440 (2002).

[64]   Dowd, P., Johnson, S. R., Feld, S. A., Adamcyk, M., Chaparro, S. A., Joseph, J., Hilgers, K., Horning, M. P., Shiralagi, K., et al., "Long wavelength GaAsP/GaAs/GaAsSb VCSELs on GaAs substrates for communications applications," Electron. Lett. **39**(13), 987–988 (2003).

[65]   Kondow, M., Uomi, K., Niwa, A., Kitatani, T., Watahiki, S.., Yazawa, Y., "GaInNAs: A novel material for long-wavelength-range laser diodes with excellent high-temperature performance," Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap. **35**(2 SUPPL. B), 1273–1275 (1996).

[66]   Jiang, J.., Zhang, Y., "Room Temperature Continuous wave InGaAsN quantum well vertical-cavity lasers emitting at 1.3 um," Electron. Lett. **36**(16), 1388–1390 (2000).

[67]   Borchert, B., Egorov, A. Y., Illek, S., Komainda, M.., Riechert, H., "1.29 um GalnNAs multiple quantum-well ridge-waveguide laser diodes with improved performance," Electron. Lett. **35**(25), 2204–2206 (1999).

[68]   Wistey, M. A., Bank, S. R., Bae, H. P., Yuen, H. B., Pickett, E. R., Goddard, L. L.., Harris, J. S., "GaInNAsSb/GaAs vertical cavity surface emitting lasers at 1534 nm," Electron. Lett. **42**(5), 282–283 (2006).

[69] Nishiyama, N., Arai, M., Shinada, S., Azuchi, M., Miyamoto, T., Koyama, F.., Iga, K., "Highly strained GaInAs-GaAs quantum-well vertical-cavity surface-emitting laser on GaAs (311)B substrate for stable polarization operation," Ieee J. Sel. Top. Quantum Electron. **7**(2), 242–248 (2001).

[70] Asplund, C., Sundgren, P., Mogg, S., Hammar, M., Christiansson, U., Oscarsson, V., Runnstrm, C., Odling, E.., Malmquist, J., "1260 nm InGaAs vertical-cavity lasers," Electron. Lett. **38**(13), 1–2 (2002).

[71] Kuo, H. C., Chang, Y. H., Yao, H. H., Chang, Y. A., Lai, F. I., Tsai, M. Y.., Wang, S. C., "High-speed modulation of InGaAs : Sb-GaAs-GaAsP quantum-well vertical-cavity surface-emitting lasers with 1.27-mu m emission wavelength," Ieee Photonics Technol. Lett. **17**(3), 528–530 (2005).

[72] von Würtemberg, R. M., Sundgren, P., Berggren, J., Hammar, M., Ghisoni, M., Ödling, E., Oscarsson, V.., Malmquist, J., "1.3 µm InGaAs vertical-cavity surface-emitting lasers with mode filter for single mode operation," Appl. Phys. Lett. **85**(21), 4851 (2004).

[73] Pougeoise, E., Gilet, P., Grosse, P., Poncet, S., Chelnokov, A., Gerard, J. M., Bourgeois, G., Stevens, R., Hamelin, R., et al., "Strained InGaAs quantum well vertical cavity surface emitting lasers emitting at 1.3 um," Electron. Lett. **42**(10), 1437–1439 (2006).

[74] Mirin, R. P., Ibbetson, J. P., Nishi, K., Gossard, A. C.., Bowers, J. E., "1.3 µm photoluminescence from InGaAs quantum dots on GaAs," Appl. Phys. Lett. **67**(25), 3795 (1995).

[75] Lott, J. A., Ledentsov, N. N., Ustinov, V. M., Maleev, N. A., Zhukov, A. E., Kovsh, A. R., Maximov, M. V., Volovik, B. V., Alferov, Z. I., et al., "InAs-InGaAs quantum dot VCSELs on GaAs substrates emitting at 1.3 mu m," Electron. Lett. **36**(16), 1384–1385 (2000).

[76] Uenohara, H., Tateno, K., Kagawa, T.., Ohiso, Y., "Polarization-Controlled 850-nm-Wavelength Vertical-Cavity Surface-Emitting Lasers Grown on (311)B Substrates by Metal-Organic Chemical Vapor Deposition," IEEE J. Sel. Top. Quantum Electron. **5**(3), 537–545 (1999).

[77] Lear, K. L.., Schneider, R. P., "Uniparabolic mirror grading for vertical cavity surface emitting lasers," Appl. Phys. Lett. **68**(5), 605–607 (1996).

[78] Hietala, V. M., Lear, K. L., Armendariz, M. G., Tigges, C. P., Hou, H. Q.., Zolper, J. C., "Electrical Characterization and Application of Very High Speed Vertical Cavity Surface Emitting Lasers (VCSELs)," IEEE MTT-S Int. Microw. Symp. Dig., 355–358 (1997).

[79] Huffaker, D. L., Deppe, D. G., Kumar, K.., Rogers, T. J., "Native-oxide defined ring contact for low threshold vertical-cavity lasers," Appl. Phys. Lett. **65**(1), 97–99 (1994).

[80] Choquette, K. D., Schneider, R. P., Crawford, M. H., Geib, K. M.., Figiel, J. J., "Continuous wave operation of 640-660nm selectively oxidised AlGaInP vertical-

cavity lasers," Electron. Lett. **31**(14), 1145–1146 (1995).

[81] Hegblom, E. R., Thibeault, B. J., Naone, R. L.., Coldren, L. A., "Vertical cavity lasers with tapered oxide apertures for low scattering loss," Electron. Lett. **33**(10), 869–871 (1997).

[82] Lear, K. L., Choquette, K. D., Schneider, R. P., Kilcoyne, S. P.., Geib, K. M., "Selectively oxidised vertical cavity surface emitting lasers with 50% power conversion efficiency," Electron. Lett. **31**(3), 208–209 (1995).

[83] Weigl, B., Grabherr, M., Jung, C., Jäger, R., Reiner, G., Michalzik, R., Sowada, D.., Ebeling, K. J., "High-performance oxide-confined GaAs VCSEL's," IEEE J. Sel. Top. Quantum Electron. **3**(2), 409–415 (1997).

[84] Seurin, J.-F., Ghosh, C. L., Khalfin, V., Miglo, A., Xu, G., J.D.Wynn., Pradhan, P.., D'Asaro, L. A., "High-power high-efficiency 2D VCSEL arrays," Proc. SPIE Vertical-Cavity Surface-Emitting Lasers XII **6908**(609), 1–14 (2008).

[85] Adachi, S., Physical Properties of III-V Compounds (1992).

[86] Babic, D. I., Streubel, K., Mirin, R. P., Margalit, N. M., Bowers, J. E., Hu, E. L., Mars, D. E., Yang, L.., Carey, K., "Room-temperature performance of double-fused 1.54 um Vertical-Cavity Lasers," Eighth Int. Conf. Indium Phosphide Relat. Mater. (1996).

[87] Black, A., Hawkins, A. R., Margalit, N. M., Babi, D. I., Holmes, A. L., Chang, Y., Abraham, P., Bowers, J. E.., Hu, E. L., "Wafer Fusion : Materials Issues and Device Results," IEEE J. Sel. Top. Quantum Electron. **3**(3), 943–951 (1997).

[88] Syrbu, A., Mereuta, A., Iakovlev, V., Caliman, A., Royo, P.., Kapon, E., "10 Gbps VCSELs with High Single Mode Output in 1310nm and 1550 nm Wavelength Bands," IEEE Conf. Opt. Fiber Commun.(1), 25–27 (2008).

[89] Adachi, S., "Lattice thermal resistivity of III – V compound alloys," J. Appl. Phys. **54**(1983), 1844 (2007).

[90] Tuttle, G., Kavanaugh, J.., Mccalmont, S., "(Al, Ga)Sb Long-Wavelength Distributed Bragg Reflectors," IEEE Photonics Technol. Lett. **5**(12), 1376–1379 (1993).

[91] Feezell, D., Buell, D. A., Lofgreen, D., Mehta, M.., Coldren, L. A., "Optical design of InAlGaAs low-loss tunnel-junction apertures for long-wavelength vertical-cavity lasers," IEEE J. Quantum Electron. **42**(5), 494–499 (2006).

[92] Reddy, M. H. M., Feezell, D., Asano, T., Buell, D. A., Huntington, A. S., Koda, R.., Coldren, L. A., "Selectively etched tunnel junction for lateral current and optical confinement in InP-based vertical cavity lasers," J. Electron. Mater. **33**(2), 118–122 (2004).

[93] Feezell, D., Buell, D. A.., Coldren, L. A., "InP-Based 1.3-1.6-um VCSELs with Selectively Etched Tunnel-Junction Aperture on a Wavelength Flexible Platform," IEEE Photonics Technol. Lett. **17**(10), 2017–2019 (2005).

[94] Vanderwater, D. a., Tan, I. H., Höfler, G. E., Defevere, D. C.., Kish, F. a., "High-

brightness AlGaInP light emitting diodes," Proc. IEEE **85**(11), 1752–1763 (1997).

[95] Kish, F. A.., Fletcher, R. M., "AlGaInP Light-Emitting Diodes," Semicond. Semimetals **48**, 149–226 (1997).

[96] Prins, A. D., Sly, J. L., Meney, A. T., Dunstan, D. J., O'Reilly, E. P., Adams, A. R.., Valster, A., "High Pressure Determination of AlGaInP Band Structure," J. Phys. Chem. Solids **56**(3), 349–352 (1995).

[97] Lin, J.-F., Jou, M.-J., Chen, C.-Y.., Lee, B.-J., "Effect of substrate misorientation on the optical properties and hole concentration of Ga0.5In0.5P and (A10.5Ga0.5)0.5In0.5P grown by low pressure metalorganic vapor phase epitaxy," J. Cryst. Growth **124**, 415–419 (1992).

[98] Liu, Q., Frost, W.., Tegude, F. J., "Investigation of growth temperature dependent GaInP ordering in different crystal planes using X-ray diffraction and photoluminescence," Mater. Sci. Eng. B **44**, 91–95 (1997).

[99] Dong, J., Chua, S., Wang, Y.., Yuan, H., "Substrate orientation dependence of In composition of AlGaInP epilayers grown by MOCVD," J. Cryst. Growth **269**, 408–412 (2004).

[100] Zhou, P., Cheng, J., Schaus, C. F., Sun, S. Z., Zheng, K., Armour, E., Hains, C., Hsin, W., Myers, D. R., et al., "Low series resistance high-efficiency GaAs/AlGaAs vertical-cavity surface emitting lasers with continuously graded mirrors grown by MOCVD," IEEE Photonics Technol. Lett. **3**(7), 591–593 (1991).

[101] Nakarmi, M. L., Nepal, N., Lin, J. Y.., Jiang, H. X., "Photoluminescence studies of impurity transitions in Mg-doped AlGaN alloys," Appl. Phys. Lett. **94**(9), 091903 (2009).

[102] Cunningham, B. T., Guido, L. J., Baker, J. E., Jr., J. S. M., Jr., N. H.., Stillman, G. E., "Carbon diffusion in undoped, n-type, and p-type GaAs," Appl. Phys. Lett. **55**, 687–689 (1989).

[103] Dingle, R., Shaklee, K. L., Leheny, R. F.., Zetterstrom, R. B., "Stimulated Emission and Laser Action in Gallium Nitride," Appl. Phys. Lett. **5**(19), 5–7 (1971).

[104] Nakamura, S., Mukai, T.., Senoh, M., "High-Power GaN P-N Junction Blue-Light-Emitting Diodes," Jpn. J. Appl. Phys. **30**, L1998 (1991).

[105] Nakamura, S., "GaN Growth Using GaN Buffer Layer," Jpn. J. Appl. Phys. **30**(Part 2, No. 10A), L1705–L1707 (1991).

[106] Nakamura, S., Iwasa, N., Senoh, M.., Mukai, T., "Hole Compensation Mechanism of P-Type GaN Films," Jpn. J. Appl. Phys. **31**(5R), 1258 (1992).

[107] Nakamura, S., "InGaN-based violet laser diodes," Semicond. Sci. Technol. **14**(6), 0 (1999).

[108] Nakamura, S., Senoh, M., Nagahama, S., Iwasa, N., Yamada, T., Matsushita, T., Kiyoku, H.., Sugimoto, Y., "InGaN-Based Multi-Quantum-Well-Structure Laser Diodes," Jpn. J. Appl. Phys. **35**(Part 2, No. 1B), L74–L76 (1996).

[109] Nakamura, S., Senoh, M.., Mukai, T., "P-GaN/N-InGaN/N-GaN Double-Heterostructure Blue-Light-Emitting Diodes," Jpn. J. Appl. Phys. **32**, 8–11 (1993).

[110] Nakamura, S.., Mukai, T., "High-Quality InGaN Films Grown on GaN Films," Jpn. J. Appl. Phys. **31**(10B), L1457–L1459 (1992).

[111] Nakamura, S., Mukai, T., Senoh, M.., Iwasa, N., "Thermal Annealing Effects on P-Type Mg-Doped GaN Films," Jpn. J. Appl. Phys. **31**(2B), L139 (1992).

[112] Nakamura, S.., Fasol, G., The Blue Laser Diode: GaN Based Light Emitters and Lasers, Springer-Verlag, Heidelberg, Germany (2007).

[113] Lester, S. D., Ponce, F. a., Craford, M. G.., Steigerwald, D. a., "High dislocation densities in high efficiency GaN-based light-emitting diodes," Appl. Phys. Lett. **66**(10), 1249–1251 (1995).

[114] Karpov, S. Y.., Makarov, Y. N., "Dislocation effect on light emission efficiency in gallium nitride," Appl. Phys. Lett. **81**(25), 4721 (2002).

[115] Chichibu, S., Azuhata, T., Sota, T.., Nakamura, S., "Recombination of Localized Excitons in InGaN Single- and Multiquantum-Well Structures," MRS Proc. **449**, 14–17 (1996).

[116] Narukawa, Y., Kawakami, Y., Fujita, S., Fujita, S.., Nakamura, S., "Recombination dynamics of localized excitons in In0.20Ga0.80N-In0.05Ga0.95N multiple quantum wells," Phys. Rev. B **55**(4), R1938–R1941 (1997).

[117] Schubert, E. F., Light-Emitting Diodes, 2nd Ed., Cambridge University Press, Cambridge, UK (2006).

[118] Amano, H., "Progress and Prospect of the Growth of Wide-Band-Gap Group III Nitrides: Development of the Growth Method for Single-Crystal Bulk GaN," Jpn. J. Appl. Phys. **52**, 050001 (2013).

[119] Seong, T.-Y., Han, J., Amano, H., Morkoc, H., Keraly, C. L., Kuritzky, L., Cochet, M., Weisbuch, C., Seong, T.-Y., et al., III-Nitride Based Light Emitting Diodes and Applications, T.-Y. Seong, J. Han, H. Amano, and H. Morkoc, Eds., Springer Netherlands, Dordrecht (2013).

[120] Bernardini, F.., Fiorentini, V., "Spontaneous versus Piezoelectric Polarization in III-V Nitrides: Conceptual Aspects and Practical Consequences," Phys. Status Solidi **216**(1), 391–398 (1999).

[121] Feezell, D. F., Speck, J. S., Denbaars, S. P.., Nakamura, S., "Semipolar 20-2-1 InGaN/GaN Light-Emitting Diodes for High-Efficiency Solid-State Lighting," J. Disp. Technol. **9**(4), 190–198 (2013).

[122] Park, S.-H., "Crystal Orientation Effects on Many-Body Optical Gain of Wurtzite InGaN/GaN Quantum Well Lasers," Jpn. J. Appl. Phys. **42**(Part 2, No. 2B), L170–L172 (2003).

[123] Park, S.-H., Ahn, D.., Chuang, S.-L., "Electronic and Optical Properties of a - and m - Plane Wurtzite InGaN-GaN Quantum Wells," IEEE J. Quantum Electron. **43**(12),

1175–1182 (2007).

[124] Scheibenzuber, W., Schwarz, U., Veprek, R., Witzigmann, B.., Hangleiter, A., "Calculation of optical eigenmodes and gain in semipolar and nonpolar InGaN/GaN laser diodes," Phys. Rev. B **80**(11), 115320 (2009).

[125] Li, Z. Q., Li, Z. M. S.., Piprek, J., "Simulations of laser diodes with nonpolar InGaN multi-quantum-wells," Phys. Status Solidi **7**(7-8), 2259–2261 (2010).

[126] Scheibenzuber, W. G.., Schwarz, U. T., "Polarization switching of the optical gain in semipolar InGaN quantum wells," Phys. Status Solidi **248**(3), 647–651 (2011).

[127] Schade, L., Schwarz, U. T., Wernicke, T., Weyers, M.., Kneissl, M., "Impact of band structure and transition matrix elements on polarization properties of the photoluminescence of semipolar and nonpolar InGaN quantum wells," Phys. Status Solidi **248**(3), 638–646 (2011).

[128] Melo, T., Hu, Y.-L., Weisbuch, C., Schmidt, M. C., David, A., Ellis, B., Poblenz, C., Lin, Y.-D., Krames, M. R., et al., "Gain comparison in polar and nonpolar/semipolar gallium-nitride-based laser diodes," Semicond. Sci. Technol. **27**(2), 024015 (2012).

[129] Park, S.-H., "Piezoelectric and Spontaneous Polarization Effects on Many-Body Optical Gain of Wurtzite InGaN/GaN Quantum Well with Arbitrary Crystal Orientation," Jpn. J. Appl. Phys. **42**(Part 1, No. 8), 5052–5055 (2003).

[130] Park, S.-H., "Crystal orientation effects on electronic properties of wurtzite InGaN/GaN quantum wells," J. Appl. Phys. **91**(12), 9904 (2002).

[131] Lu, T.-C., Chen, S.-W., Wu, T.-T., Tu, P.-M., Chen, C.-K., Chen, C.-H., Li, Z.-Y., Kuo, H.-C.., Wang, S.-C., "Continuous wave operation of current injected GaN vertical cavity surface emitting lasers at room temperature," Appl. Phys. Lett. **97**(7), 071114 (2010).

[132] Lu, T.-C., Chen, J.-R., Chen, S.-W., Kuo, H.-C., Kuo, C.-C., Lee, C.-C.., Wang, S.-C., "Development of GaN-Based Vertical-Cavity Surface-Emitting Lasers," IEEE J. Sel. Top. Quantum Electron. **15**(3), 850–860 (2009).

[133] Lu, T.-C., Kao, C.-C., Kuo, H.-C., Huang, G.-S.., Wang, S.-C., "CW lasing of current injection blue GaN-based vertical cavity surface emitting laser," Appl. Phys. Lett. **92**(14), 141102 (2008).

[134] Tropper, A. C., Foreman, H. D., Garnache, A., Wilcox, K. G.., Hoogland, S. H., "Vertical-external-cavity semiconductor lasers," J. Phys. D. Appl. Phys. **37**(9), R75–R85 (2004).

[135] Zhang, Y., Zhang, X., Li, K. H., Cheung, Y. F., Feng, C.., Choi, H. W., "Advances in III-nitride semiconductor microdisk lasers," Phys. Status Solidi **212**(5), 960–973 (2015).

[136] Nosich, A. I., Smotrova, E. I., Boriskina, S. V., Benson, T. M.., Sewell, P., "Trends in microdisk laser research and linear optical modelling," Opt. Quantum Electron. **39**(2007), 1253–1272 (2007).

[137] Liu, W.-J., Hu, X.-L., Ying, L.-Y., Zhang, J.-Y.., Zhang, B.-P., "Room temperature continuous wave lasing of electrically injected GaN-based vertical cavity surface emitting lasers," Appl. Phys. Lett. **104**(25), 251116 (2014).

[138] Tamboli, A. C., Haberer, E. D., Sharma, R., Lee, K. H., Nakamura, S.., Hu, E. L., "Room-temperature continuous-wave lasing in GaN/InGaN microdisks," Nat. Photonics **1**(1), 61–64 (2007).

[139] Wang, R. P.., Dumitrescu, M. M., "Optical modes in semiconductor microdisk lasers," IEEE J. Quantum Electron. **34**(1997), 1933–1937 (1998).

[140] Deng, Q., Deng, H.., Deppe, D. G., "Radiation fields from whispering-gallery modes of oxide-confined vertical-cavity surface-emitting lasers.," Opt. Lett. **22**(7), 463–465 (1997).

[141] Liu, Y., Zhang, J., Jia, Z., Yao, D., Liu, F., Zhai, S., Zhuo, N.., Wang, Z., "Top Grating, Surface-Emitting DFB Quantum Cascade Lasers in Continuous-Wave Operation," IEEE Photonics Technol. Lett. **27**(17), 1829–1832 (2015).

[142] Kanskar, M., Cai, J., Kedlaya, D., Olson, D., Xiao, Y., Klos, T., Martin, M., Galstad, C.., Macomber, S. H., "High Brightness 975 nm Surface-emitting Distributed Feedback Laser & Arrays," Proc. SPIE 7686, Laser Technol. Def. Secur. VI **7686**, 76860J – 76860J – 7 (2010).

[143] Schrenk, W., Finger, N., Gianordoli, S., Hvozdara, L., Strasser, G.., Gornik, E., "Surface-emitting distributed feedback quantum-cascade lasers," Appl. Phys. Lett. **77**(14), 2086 (2000).

[144] Klein, T., Klembt, S., Kozlovsky, V. I., Zheng, A., Tiberi, M. D., Kruse, C., Klein, T., Klembt, S., Kozlovsky, V. I., et al., "High-power green and blue electron-beam pumped surface-emitting lasers using dielectric and epitaxial distributed Bragg reflectors High-power green and blue electron-beam pumped surface-emitting lasers using dielectric and epitaxial distributed Bragg refl," J. Appl. Phys. **113106**, 113106 (2015).

[145] Iga, K., Koyama, F.., Kinoshita, S., "Surface emitting semiconductor lasers," IEEE J. Quantum Electron. **24**(9), 1845–1855 (1988).

[146] Farrell, R. M., "Growth, Fabrication, and Characterization of Continuous-Wave AlGaN-Cladding-Free m-plane InGaN/GaN Laser Diodes," University of California, Santa Barbara (2010).

[147] Kioupakis, E., Rinke, P., Schleife, A., Bechstedt, F.., Van De Walle, C. G., "Free-carrier absorption in nitrides from first principles," Phys. Rev. B - Condens. Matter Mater. Phys. **81**(24), 241201(R) (2010).

[148] Hegblom, E. R., Babic, D. I., Thibeault, B. J.., Coldren, L. A., "Estimation of scattering losses in dielectrically apertured vertical cavity lasers," 1757–1759 (1996).

[149] Hegblom, E. R., Babic, D. I., Thibeault, B. J.., Coldren, L. A., "Scattering Losses from Dielectric Apertures in Vertical-Cavity Lasers," IEEE J. Sel. Top. Quantum Electron. **3**(2), 379–389 (1997).

[150] Stocker, D. A., Schubert, E. F., Grieshaber, W., Boutros, K. S.., Redwing, J. M., "Facet roughness analysis for InGaN/GaN lasers with cleaved facets," Appl. Phys. Lett. **73**(14), 1925–1927 (1998).

[151] Megalini, L., Becerra, D. L., Farrell, R. M., Pourhashemi, A., Speck, J. S., Nakamura, S., Denbaars, S. P.., Cohen, D. A., "Continuous-wave operation of a (20-2-1) InGaN laser diode with a photoelectrochemically etched current aperture," Appl. Phys. Express **8**, 042701–1 – 4 (2015).

[152] Toor, F., Sivco, D. L., Liu, H. E.., Gmachl, C. F., "Effect of waveguide sidewall roughness on the threshold current density and slope efficiency of quantum cascade lasers," Appl. Phys. Lett. **93**(2008), 93–95 (2008).

[153] Lee, K. K., Lim, D. R., Luan, H.-C., Agarwal, A., Foresi, J.., Kimerling, L. C., "Effect of size and roughness on light transmission in a Si/SiO[sub 2] waveguide: Experiments and model," Appl. Phys. Lett. **77**(11), 1617 (2000).

[154] Zhang, Z. Y., Luxmoore, I. J., Jin, C. Y., Liu, H. Y., Jiang, Q., Groom, K. M., Childs, D. T., Hopkinson, M., Cullis, A. G., et al., "Effect of facet angle on effective facet reflectivity and operating characteristics of quantum dot edge emitting lasers and superluminescent light-emitting diodes," Appl. Phys. Lett. **91**(2007), 081112 (2007).

[155] Farrell, R. M., Haeger, D. A., Hsu, P. S., Fujito, K., Feezell, D. F., Denbaars, S. P., Speck, J. S.., Nakamura, S., "Determination of internal parameters for AlGaN-cladding-free m -plane InGaN / GaN laser diodes," Appl. Phys. Lett. **99**, 171115 (2011).

[156] Tao, R., Arita, M., Kako, S.., Arakawa, Y., "Fabrication and optical properties of non-polar III-nitride air-gap distributed Bragg reflector microcavities," Appl. Phys. Lett. **103**(20), 201118 (2013).

[157] Sharma, R., Haberer, E. D., Meier, C., Hu, E. L.., Nakamura, S., "Vertically oriented GaN-based air-gap distributed Bragg reflector structure fabricated using band-gap-selective photoelectrochemical etching," Appl. Phys. Lett. **87**(5), 051107 (2005).

[158] Tao, R., Arita, M., Kako, S., Kamide, K.., Arakawa, Y., "Strong coupling in non-polar GaN/AlGaN microcavities with air-gap/III-nitride distributed Bragg reflectors," Appl. Phys. Lett. **107**(10), 101102 (2015).

[159] Lin, C. K., Bour, D. P., Zhu, J., Perez, W. H., Leary, M. H., Tandon, A., Corzine, S. W.., Tan, M. R. T., "High Temperature Continuous-Wave Operation of 1.3- and 1.55-um VCSELs With InP/Air-Gap DBRs," IEEE J. Sel. Top. Quantum Electron. **9**(5), 1415–1421 (2003).

[160] Maier, M., Kaufmann, U., Schlotter, P., Obloh, H.., Ko, K., "Hole conductivity and compensation in epitaxial GaN:Mg layers," 867–872 (2000).

[161] Sizov, D., Bhat, R.., Zah, C. E., "Optical absorption of Mg-doped layers and InGaN quantum wells on c-plane and semipolar GaN structures," J. Appl. Phys. **113**, 203108 (2013).

[162] Kioupakis, E., Rinke, P.., Van de Walle, C. G., "Determination of Internal Loss in

Nitride Lasers from First Principles," Appl. Phys. Express **3**(8), 082101 (2010).

[163] Eiting, C. J., Grudowski, P. a.., Dupuis, R. D., "Growth of low resistivity p-type GaN by metal organic chemical vapour deposition," Electron. Lett. **33**(23), 1987 (1997).

[164] Götz, W., Johnson, N. M., Walker, J., Bour, D. P.., Street, R. a., "Activation of acceptors in Mg-doped GaN grown by metalorganic chemical vapor deposition," Appl. Phys. Lett. **68**(5), 667 (1996).

[165] Huang, G. S., Lu, T. C., Yao, H. H., Kuo, H. C., Wang, S. C., Lin, C. W.., Chang, L., "Crack-free GaN/AlN distributed Bragg reflectors incorporated with GaN/AlN superlattices grown by metalorganic chemical vapor deposition," Appl. Phys. Lett. **88**(2006), 5–7 (2006).

[166] Cosendey, G., Castiglia, A., Rossbach, G., Carlin, J.-F.., Grandjean, N., "Blue monolithic AlInN-based vertical cavity surface emitting laser diode on free-standing GaN substrate," Appl. Phys. Lett. **101**(15), 151113 (2012).

[167] Carlin, J.-F.., Ilegems, M., "High-quality AlInN for high index contrast Bragg mirrors lattice matched to GaN," Appl. Phys. Lett. **83**(4), 668 (2003).

[168] Feltin, E., Christmann, G., Dorsaz, J., Castiglia, A., Carlin, J., Butte, R., Grandjean, N., Christopoulos, S., Baldassarri, G., et al., "Blue lasing at room temperature in an optically pumped lattice-matched AlInN/GaN VCSEL structure," Electron. Lett. **43**(17), 16–17 (2007).

[169] Feltin, E., Butte, R., Carlin, J., Dorsaz, J., Grandjean, N.., Ilegems, M., "Lattice-matched distributed Bragg reflectors for nitride-based vertical cavity surface emitting lasers," Electron. Lett. **41**(2), 4–5 (2005).

[170] Waldrip, K. E., Han, J., Figiel, J. J., Zhou, H., Makarona, E.., Nurmikko, A. V., "Stress engineering during metalorganic chemical vapor deposition of AlGaN/GaN distributed Bragg reflectors," Appl. Phys. Lett. **78**(21), 3205 (2001).

[171] Kasahara, D., Morita, D., Kosugi, T., Nakagawa, K., Kawamata, J., Higuchi, Y., Matsumura, H.., Mukai, T., "Demonstration of Blue and Green GaN-Based Vertical-Cavity Surface-Emitting Lasers by Current Injection at Room Temperature," Appl. Phys. Express **4**(7), 072103 (2011).

[172] Omae, K., Higuchi, Y., Nakagawa, K., Matsumura, H.., Mukai, T., "Improvement in Lasing Characteristics of GaN-based Vertical-Cavity Surface-Emitting Lasers Fabricated Using a GaN Substrate," Appl. Phys. Express **2**, 052101 (2009).

[173] Higuchi, Y., Omae, K., Matsumura, H.., Mukai, T., "Room-Temperature CW Lasing of a GaN-Based Vertical-Cavity Surface-Emitting Laser by Current Injection," Appl. Phys. Express **1**, 121102 (2008).

[174] Izumi, S., Fuutagawa, N., Hamaguchi, T., Murayama, M., Kuramoto, M.., Narui, H., "Room-temperature continuous-wave operation of GaN-based vertical-cavity surface-emitting lasers fabricated using epitaxial lateral overgrowth," Appl. Phys. Express **8**, 062702 (2015).

[175] Onishi, T., Imafuji, O., Nagamatsu, K., Kawaguchi, M., Yamanaka, K.., Takigawa,

S., "Continuous Wave Operation of GaN Vertical Cavity Surface Emitting Lasers at Room Temperature," IEEE J. Quantum Electron. **48**(9), 1107–1112 (2012).

[176] Osinski, M.., Nakwaski, M., "Effective Thermal Conductivity Analysis of 1.55um InGaAsP/InP Vertical-Cavity Top-Surface-Emitting Microlasers," Electron. Lett. **29**(11), 1015 (1993).

[177] Lu, T.-C., Wu, T.-T., Chen, S.-W., Tu, P.-M., Li, Z.-Y., Chen, C.-K., Chen, C.-H., Kuo, H.-C., Wang, S.-C., et al., "Characteristics of Current-Injected GaN-Based Vertical-Cavity Surface Emitting Lasers," IEEE J. Sel. Top. Quantum Electron. **17**(6), 1594–1602 (2011).

[178] Kao, C.-C., Lu, T. C., Huang, H. W., Chu, J. T., Peng, Y. C., Yao, H. H., Tsai, J. Y., Kao, T. T., Kuo, H. C., et al., "The Lasing Characteristics of GaN-Based Vertical-Cavity Surface-Emitting Laser With AlN-GaN and Ta2O5-SiO2 Distributed Bragg Reflectors," IEEE Photonics Technol. Lett. **18**(7), 877–879 (2006).

[179] Kawaguchi, M., Imafuji, O., Nagamatsu, K., Yamanaka, K., Takigawa, S.., Katayama, T., "Design and lasing characteristics of GaN vertical elongated cavity surface emitting lasers," SPIE Photonics West 2014-OPTO Optoelectron. Devices Mater. **8986**, 89861K – 1 (2014).

[180] Hamaguchi, T., Fuutagawa, N., Izumi, S., Murayama, M.., Narui, H., "Milliwatt-class GaN-based blue vertical-cavity surface-emitting lasers fabricated by epitaxial lateral overgrowth," Phys. Status Solidi **7**, 1–7 (2016).

[181] Nakwaski, W.., Sarzała, R. P., "Transverse modes in gain-guided vertical-cavity surface-emitting lasers," 63–69 (1998).

[182] Zhao, Y.., Mcinemey, J. G., "Transverse-Mode Control of Vertical-Cavity Surface-Emitting Lasers," IEEE J. Quantum Electron. **32**(11), 1950–1958 (1996).

[183] Redaelli, L., Wenzel, H., Piprek, J., Weig, T., Einfeldt, S., Martens, M., Lükens, G., Schwarz, U. T.., Kneissl, M., "Index-Antiguiding in Narrow-Ridge GaN-Based Laser Diodes Investigated by Measurements of the Current-Dependent Gain and Index Spectra and by Self-Consistent Simulation," IEEE J. Quantum Electron. **51**(8), 2000506 (2015).

[184] Scheibenzuber, W. G., Schwarz, U. T., Lermer, T., Lutgen, S.., Strauss, U., "Antiguiding factor of GaN-based laser diodes from UV to green," Appl. Phys. Lett. **97**(2), 021102 (2010).

[185] Tisch, U., Meyler, B., Katz, O., Finkman, E.., Salzman, J., "Dependence of the refractive index of Al[sub x]Ga[sub 1−x]N on temperature and composition at elevated temperatures," J. Appl. Phys. **89**(5), 2676 (2001).

[186] Smolyakov, G. A.., Osi, M., "Analysis of Lateral-Mode Confinement in VCSELs With Ring Metal Apertures," J. Light. Technol. **23**(12), 4278–4286 (2005).

[187] Chen, C. C., Liaw, S. J.., Yang, Y. J., "Stable Single-Mode Operation of an 850-nm VCSEL with a Higher Order Mode Absorber Formed by Shallow Zn Diffusion," IEEE Photonics Technol. Lett. **13**(4), 266–268 (2001).

[188] Shi, J., Yang, L.-C., Chen, C.-C., Wu, Y.-S., Guol, S.-H.., Yang, Y.-J., "Minimization of Damping in the Electrooptic Frequency Response of High-Speed Zn-Diffusion Single-Mode Vertical-Cavity Surface-Emitting Lasers," IEEE Photonics Technol. Lett. **19**(24), 2057–2059 (2007).

[189] Iizuka, K., Elements of Photonics, Volume II: For Fiber and Integrated Optics, John Wiley & Sons, Inc., New York, NY (2002).

[190] Gómez-Castellanos, I.., Rodríguez-Dagnino, R. M., "Intensity distributions and cutoff frequencies of linearly polarized modes for a step-index elliptical optical fiber," Opt. Eng. **46**(4), 045003 (2007).

[191] Nyakas, P., Varga, G., Karpati, T., Veszpremi, T., Zsombok, G., Puskas, Z.., Hashizume, N., "Optical simulation of vertical-cavity surface-emitting lasers with noncylindrical oxide confinement," Conf. Lasers Electro-Optics Eur. - Tech. Dig. **250**, 201 (2003).

[192] "Fimmwave.", Phot. Des. Ltd., 2015, <http://www.photond.com/products/fimmwave.htm> (1 January 2015).

[193] Gustavsson, J. S., Vukusic, J. A., Bengtsson, J.., Larsson, A., "A Comprehensive Model for the Modal Dynamics of Vertical-Cavity Surface-Emitting Lasers," IEEE J. Quantum Electron. **38**(2), 203–212 (2002).

[194] Sarzała, R., Czyszanowski, T., Wasiak, M., Dems, M., Piskorski, L., Nakwaski, W.., Panajotov, K., "Numerical self-consistent analysis of VCSELs," Adv. Opt. Technol. **2012** (2012).

[195] Hadley, G. R., Warren, M. E., Choquette, K. D., Scott, J. W.., Corzine, S. W., "Comprehensive Numerical Modeling of Vertical- Cavity Surface-Emitting Lasers," IEEE J. Quantum Electron. **32**(4), 607–616 (1996).

[196] Smolyakoit, G. A., Smagleya, V. A., Nakwash, W., Eliseev, P. G.., Osiñski, M., "Design of InGaN/GaN/AlGaN VCSELs using the effective frequency method," SPIE Conf. Phys. Simul. Optoelectron. Devices Vii **3625**(January), 324–335 (1999).

[197] Marciniak, M., Śpiewak, P., Wieckowska, M.., Sarzala, R. P., "Mody poprzeczne w azotkowym laserze typu VCSEL," Przegląd Elektrotechniczny **1**(9), 127–131 (2015).

[198] Petrolati, E.., Di Carlo, A., "Enhancement of carrier focusing GaN based vertical cavity surface emitting lasers and polariton lasers," Appl. Phys. Lett. **94**(9), 091105 (2009).

[199] Nakwaski, W.., Mac, P., "Transverse-mode selectivity in possible nitride vertical-cavity surface-emitting lasers," Opt. Quantum Electron. **35**, 1037–1054 (2003).

[200] Hashemi, E., Gustavsson, J., Bengtsson, J., Stattin, M., Cosendey, G., Grandjean, N.., Haglund, A., "Engineering the Lateral Optical Guiding in Gallium Nitride-Based Vertical-Cavity Surface-Emitting Laser Cavities to Reach the Lowest Threshold Gain," Jpn. J. Appl. Phys. **52**, 08JG04 (2013).

[201] Hashemi, E., Bengtsson, J., Gustavsson, J., Stattin, M., Cosendey, G., Grandjean, N.., Haglund, A., "Analysis of structurally sensitive loss in GaN-based VCSEL cavities

and its effect on modal discrimination.," Opt. Express **22**(1), 411–426 (2014).

[202] Huang, S., Lai, Y., Ho, T., Lu, T.., Wang, S., "Study on Confinement Scheme of GaN-based Vertical- Cavity Surface-Emitting Lasers," 4–5.

[203] Soediono, B., "Quantum Dielectric Theory of Electronegativity in Covalent Systems. III. Pressure-Temperature Phase Diagrams, Heats of Mixing, and Distribution Coefficients," J. Chem. Inf. Model. **7**(4), 1479–1507 (1973).

[204] Karpiński, J., Jun, J.., Porowski, S., "Equilibrium pressure of N2 over GaN and high pressure solution growth of GaN," J. Cryst. Growth **66**(1), 1–10 (1984).

[205] Maruska, H. P.., Tietjen, J. J., "The preparation and properties of vapor-deposited single-crystal-line GaN," Appl. Phys. Lett. **15**(10), 327–329 (1969).

[206] Fujito, K., Kiyomi, K., Mochizuki, T., Oota, H., Namita, H., Nagao, S.., Fujimura, I., "High-quality nonpolar m-plane GaN substrates grown by HVPE," Phys. Status Solidi Appl. Mater. Sci. **205**(5), 1056–1059 (2008).

[207] Fujito, K., Kubo, S.., Fujimura, I., "Development of Bulk GaN Crystals and Nonpolar / Semipolar Substrates by HVPE," MRS Bull. **34**(May), 313–316 (2009).

[208] Mikawa, Y., Ishinabe, T., Kawabata, S., Mochizuki, T., Kojima, A., Kagamitani, Y.., Fujisawa, H., "Ammonothermal growth of polar and non-polar bulk GaN crystal," Proc. SPIE **9363**, 936302 (2015).

[209] Hirai, A., Jia, Z., Schmidt, M. C., Farrell, R. M., DenBaars, S. P., Nakamura, S., Speck, J. S., Fujito, K., "Formation and reduction of pyramidal hillocks on m-plane {1100} GaN," Appl. Phys. Lett. **91**(19), 191906 (2007).

[210] Yamada, H., Iso, K., Saito, M., Fujito, K., DenBaars, S. P., Speck, J. S.., Nakamura, S., "Impact of substrate miscut on the characteristic of m-plane InGaN/GaN light emitting diodes," Japanese J. Appl. Physics, Part 2 Lett. **46**, 2–5 (2007).

[211] Kelchner, K. M., Kuritzky, L. Y., Nakamura, S., DenBaars, S. P.., Speck, J. S., "Stable vicinal step orientations in m-plane GaN," J. Cryst. Growth **411**, 56–62, Elsevier (2015).

[212] Kelchner, K. M., Kuritzky, L. Y., Fujito, K., Nakamura, S., Denbaars, S. P.., Speck, J. S., "Emission characteristics of single InGaN quantum wells on misoriented nonpolar m-plane bulk GaN substrates," J. Cryst. Growth **382**, 80–86, Elsevier (2013).

[213] Farrell, R. M., Haeger, D. A., Chen, X., Gallinat, C. S., Davis, R. W., Cornish, M., Fujito, K., Keller, S., DenBaars, S. P., et al., "Origin of pyramidal hillocks on GaN thin films grown on free-standing m-plane GaN substrates," Appl. Phys. Lett. **96**(23), 231907 (2010).

[214] Kuritzky, L. Y., Myers, D. J., Nedy, J., Kelchner, K. M., Nakamura, S., Denbaars, S. P., Weisbuch, C.., Speck, J. S., "Electroluminescence characteristics of blue InGaN quantum wells on m-plane GaN 'double miscut' substrates," Appl. Phys. Express **8**, 061002 (2015).

[215] Shao, J., Edmunds, C.., Gardner, G. C., "Surface morphology evolution of m-plane

(11-00) GaN during molecular beam epitaxy growth : Impact of Ga / N ratio , miscut direction , and growth temperature," J. Appl. Phys. **114**, 023508 (2013).

[216] Sawicka, M., Turski, H., Siekacz, M., Smalc-Koziorowska, J., Kryśko, M., Dzięcielewski, I., Grzegory, I.., Skierbiszewski, C., "Step-flow anisotropy of the m-plane GaN (1$\bar{1}$00) grown under nitrogen-rich conditions by plasma-assisted molecular beam epitaxy," Phys. Rev. B - Condens. Matter Mater. Phys. **83**(24), 1–8 (2011).

[217] Yam, F. K.., Hassan, Z., "InGaN: An overview of the growth kinetics, physical properties and emission mechanisms," Superlattices Microstruct. **43**(1), 1–23 (2008).

[218] Massabuau, F. C.-P., Davies, M. J., Blenkhorn, W. E., Hammersley, S., Kappers, M. J., Humphreys, C. J., Dawson, P.., Oliver, R. a., "Investigation of unintentional indium incorporation into GaN barriers of InGaN/GaN quantum well structures," Phys. Status Solidi, n/a – n/a (2014).

[219] Shivaraman, R., Kawaguchi, Y., Tanaka, S., DenBaars, S. P., Nakamura, S.., Speck, J. S., "Comparative analysis of 2021 and 2021 semipolar GaN light emitting diodes using atom probe tomography," Appl. Phys. Lett. **102**(25), 251104 (2013).

[220] Jeong, M. S., Kim, J. Y., Kim, Y. W., White, J. O., Suh, E. K., Hong, C. H.., Lee, H. J., "Spatially resolved photoluminescence in Ingan/gan quantum wells by near-field scanning optical microscopy," Appl. Phys. Lett. **79**(2001), 976–978 (2001).

[221] Galtrey, M. J., Oliver, R. a., Kappers, M. J., Humphreys, C. J., Stokes, D. J., Clifton, P. H.., Cerezo, A., "Three-dimensional atom probe studies of an InxGa 1-xN/GaN multiple quantum well structure: Assessment of possible indium clustering," Appl. Phys. Lett. **90**(6), 28–31 (2007).

[222] Wu, Y., Wu, C., Li, C., Browne, D. A.., Speck, J. S., "Study of Percolation Transport in the InGaN / AlGaN LEDs with Random Alloy Fluctuation," Converence on Lasers and Electro-Optics (CLEO) (2015).

[223] Browne, D. a., Mazumder, B., Wu, Y.-R.., Speck, J. S., "Electron transport in unipolar InGaN/GaN multiple quantum well structures grown by NH3 molecular beam epitaxy," J. Appl. Phys. **117**(18), 185703 (2015).

[224] Nakamura, S., Harada, Y.., Seno, M., "Novel metalorganic chemical vapor deposition system for GaN growth," Appl. Phys. Lett. **58**(18), 2021–2023 (1991).

[225] Saxler, a., Walker, D., Kung, P., Zhang, X., Razeghi, M., Solomon, J., Mitchel, W. C.., Vydyanath, H. R., "Comparison of trimethylgallium and triethylgallium for the growth of GaN," Appl. Phys. Lett. **71**(22), 3272 (1997).

[226] Neugebauer, J.., Walle, C. G. Van de., "Hydrogen in GaN: Novel Aspects of a Common Impurity," Phys. Rev. Lett. **75**(24), 4452 (1995).

[227] Neugebauer, J.., Van de Walle, C., "Role of hydrogen in doping of GaN," Appl. Phys. Lett. **68**(November 1995), 1829–1831 (1996).

[228] Van de Walle, C. G., Stampfl, C.., Neugebauer, J., "Theory of doping and defects in III–V nitrides," J. Cryst. Growth **189-190**, 505–510 (1998).

[229] Van de Walle, C. G., Neugebauer, J., Stampfl, C., McCluskey, M. D.., Johnson, N. M., "Defects and Defect Reactions in Semiconductor Nitrides," Acta Phys. Pol. A **96**(5), 613–627 (1999).

[230] Stampfl, C.., Van de Walle, C., "Theoretical investigation of native defects, impurities, and complexes in aluminum nitride," Phys. Rev. B **65**, 1–10 (2002).

[231] Van de Walle, C. G.., Neugebauer, J., "First-principles calculations for defects and impurities: Applications to III-nitrides," J. Appl. Phys. **95**(8), 3851 (2004).

[232] Sumiya, M., Yoshimura, K., Ohtsuka, K.., Fuke, S., "Dependence of impurity incorporation on the polar direction of GaN film growth," Appl. Phys. Lett. **76**(15), 2098 (2000).

[233] Fichtenbaum, N. a., Mates, T. E., Keller, S., DenBaars, S. P.., Mishra, U. K., "Impurity incorporation in heteroepitaxial N-face and Ga-face GaN films grown by metalorganic chemical vapor deposition," J. Cryst. Growth **310**(6), 1124–1131 (2008).

[234] Browne, D. A., Young, E. C., Lang, J. R., Hurni, C. A.., Speck, J. S., "Indium and impurity incorporation in InGaN films on polar, nonpolar, and semipolar GaN orientations grown by ammonia molecular beam epitaxy," J. Vac. Sci. Technol. A Vacuum, Surfaces, Film. **30**(2012), 041513 (2012).

[235] Zhao, Y.., Huang, C., "High indium uptake and high polarization ratio for group-iii nitride optoelectronic devices fabricated on a semipolar (20-2-1) plane of a gallium nitride substrate," WO2012149531 A2, EP2702618A2, US20120273796, Google Patents, United States of America (2012).

[236] Wernicke, T., Schade, L., Netzel, C., Rass, J., Hoffmann, V., Ploch, S., Knauer, A., Weyers, M., Schwarz, U., et al., "Indium incorporation and emission wavelength of polar, nonpolar and semipolar InGaN quantum wells," Semicond. Sci. Technol. **27**(2), 024014 (2012).

[237] Dinh, D. V., Pristovsek, M.., Kneissl, M., "MOVPE growth and indium incorporation of polar, semipolar (112¯2) and (202¯1) InGaN," Phys. Status Solidi **6**, n/a – n/a (2015).

[238] Stringfellow, B. G., Organometallic Vapor-Phase Epitaxy: Theory and Practice, 2nd Editio, Academic Press, San Diego, California (1999).

[239] Wang, S.-C., Lu, T.-C., Kao, C.-C., Chu, J.-T., Huang, G.-S., Kuo, H.-C., Chen, S.-W., Kao, T.-T., Chen, J.-R., et al., "Optically Pumped GaN-based Vertical Cavity Surface Emitting Lasers: Technology and Characteristics," Jpn. J. Appl. Phys. **46**(8B), 5397–5407 (2007).

[240] Chu, C.-F., "Study of GaN light-emitting diodes fabricated by laser lift-off technique," J. Appl. Phys. **95**(8), 3916 (2004).

[241] Iida, D., Kawai, S., Ema, N., Tsuchiya, T., Iwaya, M., Takeuchi, T., Kamiyama, S.., Akasaki, I., "Laser lift-off technique for freestanding GaN substrate using an In droplet formed by thermal decomposition of GaInN and its application to light-

emitting diodes," Appl. Phys. Lett. **105**(7), 072101 (2014).

[242] Tan, B. S., Yuan, S.., Kang, X. J., "Performance enhancement of InGaN light-emitting diodes by laser lift-off and transfer from sapphire to copper substrate," Appl. Phys. Lett. **84**(15), 2757 (2004).

[243] Wong, W. S., Sands, T., Cheung, N. W., Kneissl, M., Bour, D. P., Mei, P., Romano, L. T.., Johnson, N. M., "Fabrication of thin-film InGaN light-emitting diode membranes by laser lift-off," Appl. Phys. Lett. **75**(10), 1360 (1999).

[244] Lee, Y. J., Lin, P. C., Lu, T. C., Kuo, H. C.., Wang, S. C., "Dichromatic InGaN-based white light emitting diodes by using laser lift-off and wafer-bonding schemes," Appl. Phys. Lett. **90**(16), 161115 (2007).

[245] Wuu, D.-S., Hsu, S.-C., Huang, S.-H., Wu, C.-C., Lee, C.-E.., Horng, R.-H., "GaN/Mirror/Si Light-Emitting Diodes for Vertical Current Injection by Laser Lift-Off and Wafer Bonding Techniques," Jpn. J. Appl. Phys. **43**(8A), 5239–5242 (2004).

[246] Chu, J.-T., Lu, T., Yao, H.-H., Kao, C.-C., Liang, W.-D., Tsai, J.-Y., Kuo, H.., Wang, S.-C., "Room-Temperature Operation of Optically Pumped Blue-Violet GaN-Based Vertical-Cavity Surface-Emitting Lasers Fabricated by Laser Lift-Off," Jpn. J. Appl. Phys. **45**(4A), 2556–2560 (2006).

[247] DTRLPF@gmail.com., "DTR's Laser Shop," <https://sites.google.com/site/dtrlpf/home> (1 January 2016).

[248] Minsky, M. S., White, M.., Hu, E. L., "Room-temperature photoenhanced wet etching of GaN," Appl. Phys. Lett. **68**(11), 1531 (1996).

[249] Zhuang, D.., Edgar, J. H., "Wet etching of GaN, AlN, and SiC: a review," Mater. Sci. Eng. R **48**(1), 1–46 (2005).

[250] Tamboli, A. C., Schmidt, M. C., Hirai, A., DenBaars, S. P.., Hu, E. L., "Photoelectrochemical Undercut Etching of m-Plane GaN for Microdisk Applications," J. Electrochem. Soc. **156**(10), H767 (2009).

[251] Tamboli, A. C., Schmidt, M. C., Rajan, S., Speck, J. S., Mishra, U. K., DenBaars, S. P.., Hu, E. L., "Smooth Top-Down Photoelectrochemical Etching of m-Plane GaN," J. Electrochem. Soc. **156**(1), H47 (2009).

[252] Stonas, A. R., Margalith, T., DenBaars, S. P., Coldren, L. A.., Hu, E. L., "Development of selective lateral photoelectrochemical etching of InGaN/GaN for lift-off applications," Appl. Phys. Lett. **78**(13), 1945 (2001).

[253] Yang, B.., Fay, P., "Etch rate and surface morphology control in photoelectrochemical etching of GaN," J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. **22**(4), 1750 (2004).

[254] Stonas, A. R., Kozodoy, P., Marchand, H., Fini, P., DenBaars, S. P., Mishra, U. K.., Hu, E. L., "Backside-illuminated photoelectrochemical etching for the fabrication of deeply undercut GaN structures," Appl. Phys. Lett. **77**(16), 2610 (2000).

[255] Jung, Y., Baik, K. H., Ren, F., Pearton, S. J.., Kim, J., "Effects of

Photoelectrochemical Etching of N-Polar and Ga-Polar Gallium Nitride on Sapphire Substrates," J. Electrochem. Soc. **157**(6), H676 (2010).

[256] Trichas, E., Kayambaki, M., Iliopoulos, E., Pelekanos, N. T.., Savvidis, P. G., "Resonantly enhanced selective photochemical etching of GaN," Appl. Phys. Lett. **94**(17), 173505 (2009).

[257] Trichas, E., Xenogianni, C., Kayambaki, M., Tsotsis, P., Iliopoulos, E., Pelekanos, N. T.., Savvidis, P. G., "Selective photochemical etching of GaN films and laser lift-off for microcavity fabrication," Phys. Status Solidi **205**(11), 2509–2512 (2008).

[258] Youtsey, C., Adesida, I., Romano, L. T.., Bulman, G., "Smooth n-type GaN surfaces by photoenhanced wet etching," Appl. Phys. Lett. **72**(5), 560 (1998).

[259] Piprek, J., "GaN-based vertical-cavity laser performance improvements using tunnel-junction-cascaded active regions," Appl. Phys. Lett. **105**, 011116 (2014).

[260] Zandi, A., Jasim, F. Z., Hassan, Z., Hassan, H. A., Yahya, a. K.., Alam, S., "Single and Double Quantum Well Effects on GaN-Based VCSELs Performance," 101–104 (2010).

[261] Electronics, Q., Publishers, K. A.., Engineering, C., "Thermal aspects of designing CW-operated nitride VCSELs" (1999).

[262] Zhao, H., Arif, R. a., Ee, Y. K.., Tansu, N., "Self-consistent analysis of strain-compensated InGaN-AlGaN quantum wells for lasers and light-emitting diodes," IEEE J. Quantum Electron. **45**(1), 66–78 (2009).

[263] Ryu, H. Y., Ha, K. H., Son, J. K., Lee, S. N., Paek, H. S., Jang, T., Sung, Y. J., Kim, K. S., Kim, H. K., et al., "Determination of internal parameters in blue InGaN laser diodes by the measurement of cavity-length dependent characteristics," Appl. Phys. Lett. **93**(1), 011105 (2008).

[264] Shan Hsu, P., Hardy, M. T., Young, E. C., Romanov, A. E., DenBaars, S. P., Nakamura, S.., Speck, J. S., "Stress relaxation and critical thickness for misfit dislocation formation in (1010) and (3031) InGaN/GaN heteroepitaxy," Appl. Phys. Lett. **100**(17), 171917 (2012).

[265] Shimada, N., Ohno, A., Abe, S., Miyashita, M.., Yagi, T., "High-Power 625-nm AlGaInP Laser Diode," IEEE J. Sel. Top. Quantum Electron. **17**(6), 1723–1726 (2011).

[266] Michel, N., Lecomte, M., Parillaud, O., Calligaro, M., Nagle, J.., Krakowski, M., "Optimization of the wall-plug efficiency of Al-free active region diode lasers at 975 nm," Semicond. Lasers Laser Dyn. III **6997**(0), K. P. Panajotov, M. Sciamanna, A. A. Valle, and R. Michalzik, Eds., 69971W – 69971W – 8 (2008).

[267] Crump, P., Dong, W., Grimshaw, M., Wang, J., Patterson, S., Wise, D., DeFranza, M., Elim, S., Zhang, S., et al., "100-W+ Diode Laser Bars Show >71% Power Conversion From 790-nm to 1000-nm and Have Clear Route to >85%," High-Power Diode Laser Technol. Appl. V **6456**, M. S. Zediker, Ed., 64560M – 64560M – 11 (2007).

[268] Karpov, S. Y., "Modeling of III-nitride light-emitting diodes: progress, problems, and perspectives," 79391C – 79391C – 12 (2011).

[269] Bulashevich, K. a., Khokhlev, O. V., Evstratov, I. Y.., Karpov, S. Y., "Simulation of light-emitting diodes for new physics understanding device design," K. P. Streubel, H. Jeon, L.-W. Tu, and N. Linder, Eds., 827819–827819 – 12 (2012).

[270] Zakheim, D. a., Pavluchenko, a. S., Bauman, D. a., Bulashevich, K. a., Khokhlev, O. V.., Karpov, S. Y., "Efficiency droop suppression in InGaN-based blue LEDs: Experiment and numerical modelling," Phys. Status Solidi **209**(3), 456–460 (2012).

[271] "SILENSe Manual - Release Notes - V5.4.", STR Gr. (2013).

[272] "SILENSe Manual - Properties Editor.", STR Gr. (2013).

[273] "SILENSe Manual - Physics Summary.", STR Gr. (2013).

[274] Piprek, J., Farrell, R., Denbaars, S.., Nakamura, S., "Effects of Built-In Polarization on InGaN – GaN Vertical-Cavity Surface-Emitting Lasers," IEEE Photonics Technol. Lett. **18**(1), 2005–2007 (2006).

[275] Zhang, N., Liu, Z., Wei, T., Zhang, L., Wei, X., Wang, X., Lu, H., Li, J.., Wang, J., "Effect of the graded electron blocking layer on the emission properties of GaN-based green light-emitting diodes," Appl. Phys. Lett. **100**(5), 053504 (2012).

[276] Lin, R.-M., Yu, S.-F., Chang, S.-J., Chiang, T.-H., Chang, S.-P.., Chen, C.-H., "Inserting a p-InGaN layer before the p-AlGaN electron blocking layer suppresses efficiency droop in InGaN-based light-emitting diodes," Appl. Phys. Lett. **101**(8), 081120 (2012).

[277] Hsieh, D. H., Tzou, A. J., Kao, T. S., Lai, F. I., Lin, D. W., Lin, B. C., Lu, T. C., Lai, W. C., Chen, C. H., et al., "Improved carrier injection in GaN-based VCSEL via AlGaN/GaN multiple quantum barrier electron blocking layer," Opt. Express **23**(21), 27145 (2015).

[278] Taguchi, J., Yamamoto, H., Tonotani, J., Kim, Y., Ueda, I., Kuriyama, A., Takahasi, K., Morifuji, E., Kanda, M., et al., "Nitride-Based LEDs With p-InGaN Capping Layer," IEEE Trans. Electron Devices **50**(12), 2567–2570 (2003).

[279] Lee, S.-N., Son, J., Sakong, T., Lee, W., Paek, H., Yoon, E., Kim, J., Cho, Y.-H., Nam, O., et al., "Investigation of optical and electrical properties of Mg-doped p-InxGa1−xN, p-GaN and p-AlyGa1−yN grown by MOCVD," J. Cryst. Growth **272**(1-4), 455–459 (2004).

[280] Lee, S.-N., Sakong, T., Lee, W., Paek, H., Son, J., Yoon, E., Nam, O.., Park, Y., "Characterization of optical and electrical quality of Mg-doped InxGa1−xN grown by MOCVD," J. Cryst. Growth **261**(2-3), 249–252 (2004).

[281] Mohammad, S. N., "Contact mechanisms and design principles for alloyed ohmic contacts to n-GaN," J. Appl. Phys. **95**(12), 7940–7953 (2004).

[282] Mohammad, S. N., "Contact mechanisms and design principles for nonalloyed ohmic contacts to n-GaN," J. Appl. Phys. **95**(9), 4856–4865 (2004).

[283] Cao, X. A., Pearton, S. J., Zhang, A. P., Dang, G. T., Ren, F., Shul, R. J., Zhang, L., Hickman, R.., Van Hove, J. M., "Electrical effects of plasma damage in p-GaN," Appl. Phys. Lett. **75**(17), 2569 (1999).

[284] Cao, X. A., Zhang, A. P., Dang, G. T., Ren, F., Pearton, S. J., Shul, R. J.., Zhang, L., "Schottky diode measurements of dry etch damage in n- and p-type GaN," J. Vac. Sci. Technol. A Vacuum, Surfaces, Film. **18**(4), 1144 (2000).

[285] Cao, X. A., Pearton, S. J., Dang, G. T., Zhang, A. P., Ren, F.., Hove, J. M. Van., "GaN N- and P-Type Schottky Diodes : Effect of Dry Etch Damage," IEEE Trans. Electron Devices **47**(7), 1320–1324 (2000).

[286] Haberer, E. D., Chen, C. H., Hansen, M., Keller, S., DenBaars, S. P., Mishra, U. K.., Hu, E. L., "Enhanced diffusion as a mechanism for ion-induced damage propagation in GaN," J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. **19**(2001), 603 (2001).

[287] Malinverni, M., Martin, D.., Grandjean, N., "InGaN based micro light emitting diodes featuring a buried GaN tunnel junction," Appl. Phys. Lett. **107**(5), 051107 (2015).

[288] Diagne, M., He, Y., Zhou, H., Makarona, E., Nurmikko, a. V., Han, J., Waldrip, K. E., Figiel, J. J., Takeuchi, T., et al., "Vertical cavity violet light emitting diode incorporating an aluminum gallium nitride distributed Bragg mirror and a tunnel junction," Appl. Phys. Lett. **79**(22), 3720 (2001).

[289] Kaneko, S., Torii, H., Soga, M., Akiyama, K., Iwaya, M., Yoshimoto, M.., Amazawa, T., "Epitaxial Indium Tin Oxide Film Deposited on Sapphire Substrate by Solid-Source Electron Cyclotron Resonance Plasma," Jpn. J. Appl. Phys. **51**(1), 01AC02 (2012).

[290] Wu, T.-T., Lin, C.-C., Wu, Y.-L., Chen, C.-K., Lu, T.-C., Kuo, H.-C.., Wang, S.-C., "Enhanced Output Power of GaN-Based Resonance Cavity Light-Emitting Diodes With Optimized ITO Design," J. Light. Technol. **29**(24), 3757–3763 (2011).

[291] Iwase, H., Hoshi, Y.., Kameyama, M., "Electrical properties of indium-tin oxide films deposited on nonheated substrates using a planar-magnetron sputtering system and a facing-targets sputtering system," J. Vac. Sci. Technol. A Vacuum, Surfaces, Film. **24**(1), 65 (2006).

[292] Schwyn Thöny, S., Buchholz, J.., Waldner, S., "Optimization of Ion-assisted ITO films by Design of Experiment," Adv. Opt. Thin Film. IV **8168**, M. Lequime, H. A. Macleod, and D. Ristau, Eds., 81681H – 81681H – 8 (2011).

[293] Cao, X. A., Zhang, A. P., Dang, G. T., Ren, F.., Pearton, S. J., "Plasma Damage in p-GaN," J. Electron. Mater. **29**(3), 256–261 (2000).

[294] Keraly, C. L., Kuritzky, L., Cochet, M.., Weisbuch, C., "Light Extraction Efficiency Part A. Ray Tracing for Light Extraction Efficiency (LEE) Modeling in Nitride LEDs," [III-Nitride Based Light Emitting Diodes and Applications], T.-Y. Seong, J. Han, H. Amano, and H. Morkoc, Eds., Springer Netherlands, Dordrecht, 231–269 (2013).

[295] Pan, J.-W.., Wang, C.-S., "Light extraction efficiency of GaN-based LED with pyramid texture by using ray path analysis.," Opt. Express **20**(S5), A630–A640 (2012).

[296] Lee, T.-X., Gao, K.-F., Chien, W.-T.., Sun, C.-C., "Light extraction analysis of GaN-based light-emitting diodes with surface texture and/or patterned substrate.," Opt. Express **15**(11), 6670–6676 (2007).

[297] Zabelin, V., Zakheim, D. A.., Gurevich, S. A., "Efficiency improvement of AlGaInN LEDs advanced by ray-tracing analysis," IEEE J. Quantum Electron. **40**(12), 1675–1686 (2004).

[298] Beckmann, P.., Spizzichino, A., The scattering of electromagnetic waves from rough surfaces, Artech House, Inc., Norwood, MA (1987).

[299] Elson, J. M., "Infrared light scattering from surfaces covered with multiple dielectric overlayers.," Appl. Opt. **16**(11), 2872–2881 (1977).

[300] Elson, J. M., "Theory of light scattering from a rough surface with an inhomogeneous dielectric permittivity," Phys. Rev. B **30**(10), 5460–5480 (1984).

[301] Church, E. L.., Zavada, J. M., "Residual surface roughness of diamond-turned optics.," Appl. Opt. **14**(8), 1788–1795 (1975).

[302] Church, E. L.., Jenkinson, H. A., "Metal Surfaces of Diamond Finish of the Finish of the Measurement of By Differential Light Scattering," Opt. Eng. **16**(4), 164360 (1977).

[303] Church, E. L., Jenkinson, H. A.., Zavada, J. M., "Relationship between Surface Scattering and Mircotopographic Features," Opt. Eng. **18**(2), 182125 (1979).

[304] Maradudin, A. A.., Mills., D. L., "Scattering and absorption of electromagnetic radiation by a semi-infinite medium in the presence of surface roughness," Phys. Rev. B **11**, 1392–1415 (1975).

[305] Eastman, J. M., "Scattering by all-dielectric multilayer bandpass filters and mirrors for lasers," [Physics of Thin Films, Vol. 10], G. Ed. Hass and M. H. Francombe, Eds., Academic Press, New York, 167–226 (1978).

[306] Amra, C.., Bousquet, P., "Scattering From Surfaces And Multilayer Coatings: Recent Advances For A Better Investigation Of Experiment," Surf. Meas. Charact. **82**, 1009 (1989).

[307] Elson, J. M.., Bennett, J. M., "Vector Scattering Theory," Opt. Eng. **18**(2), 182116 (1979).

[308] Elson, J. M., Rahn, J. P.., Bennett, J. M., "Relationship of the total integrated scattering from multilayer-coated optics to angle of incidence , polarization , correlation length , and roughness cross-correlation properties," Appl. Opt. **22**(20), 3207–3219 (1983).

[309] Hummel, R. E.., Wissmann, P., CRC Handbook of Optical Properties: Optics of Small Particles, Interfaces and Surfaces, CRC Press LLC, Boca Raton, FA (1997).

[310] Elson, J. M.., Bennett, J. M., "Relation between the angular dependence of scattering and the statistical properties of optical surfaces," J. Opt. Soc. Am. **69**(1), 31–47 (1979).

[311] Nečas, D.., Klapetek, P., "Gwyddion," gwyddion.net, 2014, <http://gwyddion.net/> (1 January 2015).

[312] Synowicki, R. A., "Spectroscopic ellipsometry characterization of indium tin oxide film microstructure and optical constants," Thin Solid Films **313-314**, 394–397 (1998).

[313] Gerfin, T.., Grätzel, M., "Optical properties of tin-doped indium oxide determined by spectroscopic ellipsometry," J. Appl. Phys. **79**(3), 1722 (1996).

[314] Kim, K.-K., Kim, H., Lee, S.-N.., Cho, S., "Structural, optical, and electrical properties of E-beam and sputter-deposited ITO films for LED applications," Electron. Mater. Lett. **7**(2), 145–149 (2011).

[315] Ginley, D. S., Hosono, H.., Paine, D. C., Handbook of Transparent Conductors, D. S. Ginley, Ed., Springer Science+Business Media, LLC, Boston, MA (2011).

[316] Fallah, H. R., Ghasemi, M., Hassanzadeh, A.., Steki, H., "The effect of annealing on structural, electrical and optical properties of nanostructured ITO films prepared by e-beam evaporation," Mater. Res. Bull. **42**(3), 487–496 (2007).

[317] Chang, K.-M., Chu, J.-Y.., Cheng, C.-C., "Investigation of indium–tin-oxide ohmic contact to p-GaN and its application to high-brightness GaN-based light-emitting diodes," Solid. State. Electron. **49**(8), 1381–1386 (2005).

[318] Kim, D. W., Sung, Y. J., Park, J. W.., Yeom, G. Y., "A study of transparent indium tin oxide (ITO) contact to p-GaN," Thin Solid Films **398-399**, 87–92 (2001).

[319] Margalith, T., Buchinsky, O., Cohen, D. a., Abare, a. C., Hansen, M., DenBaars, S. P.., Coldren, L. a., "Indium tin oxide contacts to gallium nitride optoelectronic devices," Appl. Phys. Lett. **74**(26), 3930 (1999).

[320] Paine, D. C., Whitson, T., Janiac, D., Beresford, R., Yang, C. O.., Lewis, B., "A study of low temperature crystallization of amorphous thin film indium–tin–oxide," J. Appl. Phys. **85**(12), 8445 (1999).

[321] Kasiviswanathan, S., Srinivas, V., Kar, A. K., Mathur, B. K.., Chopra, K. L., "Observation of Deviation of Electronic Behaviour of Indium Tin Oxide Film At Grain Boundary Using Scanning Tunneling Microscope," Solid State Commun. **101**(11), 831–834 (1997).

[322] Banerjee, R., Das, D., Ray, S., Batabyal, A. K.., Barua, A. K., "Characterization of Tin Doped Indium Oxide Films Prepared By Electron Beam Evaporation," Sol. Energy Mater. **13**, 11–23 (1986).

[323] Raoufi, D., Kiasatpour, A., Fallah, H. R.., Rozatian, A. S. H., "Surface characterization and microstructure of ITO thin films at different annealing temperatures," Appl. Surf. Sci. **253**(23), 9085–9090 (2007).

[324] Raoufi, D., "Morphological characterization of ITO thin films surfaces," Appl. Surf. Sci. **255**(6), 3682–3686, Elsevier B.V. (2009).

[325] Wang, R. X., Beling, C. D., Fung, S., Djurišic, a. B., Ling, C. C.., Li, S., "Influence of gaseous annealing environment on the properties of indium-tin-oxide thin films," J. Appl. Phys. **97**(3), 033504 (2005).

[326] Mori, N., Ooki, S., Masubuchi, N., Tanaka, A., Kogoma, M.., Ito, T., "Effects of postannealing in ozone environment on opto-electrical properties of Sn-doped In2O3 thin films," Thin Solid Films **411**(1), 6–11 (2002).

[327] Wang, R. X., Beling, C. D., Fung, S., Djurišić, a B., Ling, C. C., Kwong, C.., Li, S., "Influence of annealing temperature and environment on the properties of indium tin oxide thin films," J. Phys. D. Appl. Phys. **38**(12), 2000–2005 (2005).

[328] J. A. Woollam Co., I., "CompleteEASE^{TM} Data Analysis Manual," Lincoln, NE (2008).

[329] Shigesato, Y., Takaki, S.., Haranoh, T., "Electrical and structural properties of low resistivity tin-doped indium oxide films," J. Appl. Phys. **71**(7), 3356 (1992).

[330] Sun, X. W., Huang, H. C.., Kwok, H. S., "On the initial growth of indium tin oxide on glass," Appl. Phys. Lett. **68**(19), 2663 (1996).

[331] Muranaka, S., Bando, Y.., Takada, T., "Influence of Substrate Temperature and Film Thickness on the Structure of Reactively Evaporated In2O3 Films," Thin Solid Films **151**(3), 355–364 (1987).

[332] Habermeier, H.-U., "Properties of Indium Tin Oxide Thin Films Prepared By Reactive Evaporation," Thin Solid Films **80**, 157–160 (1981).

[333] Limpijumnong, S., Reunchan, P., Janotti, A.., Van De Walle, C. G., "Hydrogen doping in indium oxide: An ab initio study," Phys. Rev. B - Condens. Matter Mater. Phys. **80**, 193202 (2009).

[334] Varley, J. B., Peelaers, H., Janotti, A.., Van de Walle, C. G., "Hydrogenated cation vacancies in semiconducting oxides.," J. Phys. Condens. Matter **23**, 334212 (2011).

[335] Reunchan, P., Zhou, X., Limpijumnong, S., Janotti, A.., Van De Walle, C. G., "Vacancy defects in indium oxide: An ab-initio study," Curr. Appl. Phys. **11**(3), S296–S300, Elsevier B.V (2011).

[336] Koida, T., Fujiwara, H.., Kondo, M., "Hydrogen-doped in2O3 as high-mobility transparent conductive oxide," Japanese J. Appl. Physics, Part 2 Lett. **46**(28), L685–L687 (2007).

[337] Serikawa, T.., Shirai, S., "Studies of H2+ Implantation Into Indium-Tin Oxide Films," Nucl. Instruments Methods Phys. Res. **B37**(38), 732–734 (1989).

[338] Barna, P. B.., Adamik, M., "Fundamental structure forming phenomena of polycrystalline films and the structure zone models," Thin Solid Films **317**(1-2), 27–33 (1998).

[339] Bellingham, J. R., Phillips, W. A.., Adkins, C. J., "Electrical and optical properties of

amorphous indium oxide," J. Phys. Condens. Matter **2**(28), 6207–6221 (1990).

[340] Bender, M., Seelig, W., Daube, C., Frankenberger, H., Ocker, B.., Stollenwerk, J., "Dependence of oxygen flow on optical and electrical properties of DC-magnetron sputtered ITO films," Thin Solid Films **326**(1-2), 72–77 (1998).

[341] Fan, J. C. C., Bachner, F. J.., Foley, G. H., "Effect of O2 pressure during deposition on properties of rf-sputtered Sn-doped In2O3 films," Appl. Phys. Lett. **31**(11), 773 (1977).

[342] Hoffmann, H., Pickl, J., Schmidt, M.., Krause, D., "HF-Sputtered Indium Oxide Films Doped with Tin," Appl. Phys. **16**(3), 239–246 (1978).

[343] Buchanan, M., Webb, J. B.., Williams, D. F., "Preparation of conducting and transparent thin films of tin-doped indium oxide by magnetron sputtering," Appl. Phys. Lett. **37**(2), 213 (1980).

[344] Na, J., Cho, Y., Kim, Y., Lee, T.., Park, S., "Effects of Annealing Temperature on Microstructure and Electrical and Optical Properties of Radio-Frequency-Sputtered Tin-Doped Indium Oxide Films," J. Am. Ceram. Soc. **72**(4), 698–701 (1989).

[345] Ray, S., Banerjee, R., Basu, N., Batabyal, A. K.., Barua, A. K., "Properties of tin doped indium oxide thin films prepared by magnetron sputtering," J. Appl. Phys. **54**(6), 3497 (1983).

[346] Diagne, M., He, Y., Zhou, H., Makarona, E., Nurmikko, A. V., Han, J., Takeuchi, T.., Krames, M., "A High Injection Resonant Cavity Violet Light Emitting Diode Incorporating (Al,Ga)N Distributed Bragg Reflector," Phys. Status Solidi **188**(1), 105–108 (2001).

[347] Jeon, S. R., Song, Y. H., Jang, H. J., Yang, G. M., Hwang, S. W.., Son, S. J., "Lateral current spreading in GaN-based light-emitting diodes utilizing tunnel contact junctions," Appl. Phys. Lett. **78**(21), 3265–3267 (2001).

[348] Ozden, I., Makarona, E., Nurmikko, a. V., Takeuchi, T.., Krames, M., "A dual-wavelength indium gallium nitride quantum well light emitting diode," Appl. Phys. Lett. **79**(2001), 2532–2534 (2001).

[349] Takeuchi, T., Hasnain, G., Corzine, S., Hueschen, M., Schneider, Jr., R. P., Kocot, C., Blomqvist, M., Chang, Y., Lefforge, D., et al., "GaN-Based Light Emitting Diodes with Tunnel Junctions," Jpn. J. Appl. Phys. **40**(8), 861–863 (2001).

[350] Krishnamoorthy, S., Akyol, F.., Rajan, S., "InGaN/GaN Tunnel Junctions For Hole Injection in GaN Light Emitting Diodes," Appl. Phys. Lett. **105**, 141104 (2014).

[351] Zhang, Z.-H., Tan, S. T., Kyaw, Z., Ji, Y., Liu, W., Ju, Z., Hasanov, N., Wei Sun, X.., Volkan Demir, H., "InGaN/GaN light-emitting diode with a polarization tunnel junction," Appl. Phys. Lett. **102**(19), 193508 (2013).

[352] Krishnamoorthy, S., Kent, T. F., Yang, J., Park, P. S., Myers, R. C.., Rajan, S., "GdN nanoisland-based GaN tunnel junctions," Nano Lett. **13**(6), 2570–2575 (2013).

[353] Fritze, S., Dadgar, A., Witte, H., Rohrbeck, A., Hoffmann, A.., Krost, A., "High Si

and Ge n-type doping of GaN doping - Limits and impact on stress," Appl. Phys. Lett. **100**, 122104 (2012).

[354] Kuwano, Y., Kaga, M., Morita, T., Yamashita, K., Yagi, K., Iwaya, M., Takeuchi, T., Kamiyama, S.., Akasaki, I., "Lateral Hydrogen Diffusion at p-GaN Layers in Nitride-Based Light Emitting Diodes with Tunnel Junctions Lateral Hydrogen Diffusion at p-GaN Layers in Nitride-Based Light Emitting Diodes with Tunnel Junctions," Jpn. J. Appl. Phys. **52**, 08JK12 (2013).

[355] Simon, J., Zhang, Z., Goodman, K., Xing, H., Kosel, T., Fay, P.., Jena, D., "Polarization-Induced Zener Tunnel Junctions in Wide-Band-Gap Heterostructures," Phys. Rev. Lett. **103**(2), 026801 (2009).

[356] Blank, T. V.., Gol'dberg, Y. a., "Mechanisms of current flow in metal-semiconductor ohmic contacts," Semiconductors **41**(11), 1263–1292 (2007).

[357] Cao, X. a., Stokes, E. B., Sandvik, P. M., LeBoeuf, S. F., Kretchmer, J.., Walker, D., "Diffusion and tunneling currents in GaN/InGaN multiple quantum well light-emitting diodes," IEEE Electron Device Lett. **23**(9), 535–537 (2002).

[358] Fedison, J. B., Chow, T. P., Lu, H.., Bhat, I. B., "Electrical characteristics of magnesium-doped gallium nitride junction diodes," Appl. Phys. Lett. **72**(22), 2841–2843 (1998).

[359] Sakowski, K., Marcinkowski, L., Krukowski, S., Grzanka, S.., Litwin-Staszewska, E., "Simulation of trap-assisted tunneling effect on characteristics of gallium nitride diodes," J. Appl. Phys. **111**(12), 123115 (2012).

[360] Chow, T. P.., Ghezzo, M., "III-Nitride, SiC, and Diamond Materials For Electronic Devices," Mater. Res. Soc. Symoposium Proc., D. K. Gaskill, C. D. Brandt, and R. J. Nemanich, Eds., 69–73, Materials Research Society, Pittsburgh, PA (1996).

[361] Mackowiak, P., SarzaLa, R. P., Wasiak, M.., Nakwaski, W., "Cascade nitride VCSEL designs with tunnel junctions," Appl. Phys. A Mater. Sci. Process. **78**(3), 315–322 (2004).

[362] Sarzala, R. P., Wasiak, M.., Nakwaski, W., "Design Guidelines for Fundamental-Mode-Operated Cascade Nitride VCSELs," IEEE Photonics Technol. Lett. **15**(4), 495–497 (2003).

[363] Maækowiak, P., Sarza, R. P. A., Wasiak, M.., Nakwaski, W., "An attempt to design room-temperature-operated nitride diode VCSELs," Opto-Electronics Rev. **12**(4), 411–416 (2004).

[364] Nash, F. R., "Mode guidance parallel to the junction plane of double-heterostructure GaAs lasers," J. Appl. Phys. **44**(1973), 4696–4707 (1973).

[365] Mackowiak, P., Sarzala, R. P., Wasiak, M., Nakwaski, W., Search, H., Journals, C., Contact, A., Iopscience, M.., Address, I. P., "Radial optical confinement in nitride VCSELS," J. Phys. D. Appl. Phys. **2041**, 2041–2045 (2003).

[366] Margalith, T., Coldren, L. A.., Nakamura, S., "Implantation for Current Confinement in Nitride-Based Vertical Optoelectronics," US 0180980 A1, Google Patents, United

States of America (2003).

[367] Margalith, T., "Development of Growth and Fabrication Technology for Gallium Nitride-Based Vertical Cavity Surface Emitting Lasers," University of California, Santa Barbara (2002).

[368] Chowdhury, S., "AlGaN/GaN CAVETs for high power switching application," University of California, Santa Barbara (2010).

[369] Pearton, S. J.., Ueda, O., Materials and Reliability Handbook for Semiconductor Optical and Electron Devices, Springer, New York, NY (2013).

[370] Moloney, J. V., "Spontaneous generation of patterns and their control in nonlinear optical systems," J. Opt. B Quantum Semiclassical Opt. **1**, 183–190 (1999).

[371] Lundeberg, L. D. A., Lousberg, G. P., Boiko, D. L.., Kapon, E., "Spatial coherence measurements in arrays of coupled vertical cavity surface emitting lasers," Appl. Phys. Lett. **90**(021103), 021103–1 – 3 (2007).

[372] Gelžinytė, K., Ivanov, R., Marcinkevičius, S., Zhao, Y., Becerra, D. L., Nakamura, S.., Denbaars, S. P., "High spatial uniformity of photoluminescence spectra in semipolar (20 2 $\bar{}$ 1) plane InGaN / GaN quantum wells High spatial uniformity of photoluminescence spectra in semipolar ð 20 21 plane InGaN / GaN quantum wells," J. Appl. Phys. **117**(023111), 023111–1 – 9 (2015).

[373] Joyce, W. B., Wemple, S. H., "Steady-state junction-current distributions in thin resistive films on semiconductor junctions (solutions of $\bigtriangledown 2v = \pm ev$)," J. Appl. Phys. **41**(9), 3818–3830 (1970).

[374] Jeon, S.., Yang, G. M., "Vertical-Surface-Emitting Diode Using a GaN Buried Tunnel Junction Current Aperture," J. Korean Phys. Soc. **41**(6), 1021–1024 (2002).

[375] Haberer, E. D., Sharma, R., Meier, C., Stonas, a. R., Nakamura, S., DenBaars, S. P.., Hu, E. L., "Free-standing, optically pumped, GaN⁄InGaN microdisk lasers fabricated by photoelectrochemical etching," Appl. Phys. Lett. **85**(22), 5179 (2004).

[376] Haberer, E. D., Sharma, R., Stonas, a. R., Nakamura, S., DenBaars, S. P.., Hu, E. L., "Removal of thick (>100 nm) InGaN layers for optical devices using band-gap-selective photoelectrochemical etching," Appl. Phys. Lett. **85**(5), 762 (2004).

[377] Gao, Y., Stonas, R. A., Ben-Yaacov, I., Mishra, U., DenBaars, S. P.., Hu, E. L., "AlGaN/GaN Current Aperture Vertical Electron Transistors Fabricated By Photoelectrochemical Wet Etching," Electron. Lett. **39**(1), 148–149 (2003).

[378] Gao, Y., Ben-Yaacov, I., Mishra, U. K.., Hu, E. L., "Optimization of AlGaN⁄GaN current aperture vertical electron transistor (CAVET) fabricated by photoelectrochemical wet etching," J. Appl. Phys. **96**(11), 6925 (2004).

[379] Tamboli, A. C., Hirai, A., Nakamura, S., DenBaars, S. P.., Hu, E. L., "Photoelectrochemical etching of p-type GaN heterostructures," Appl. Phys. Lett. **94**(15), 151113 (2009).

[380] Megalini, L., Kuritzky, L. Y., Leonard, J. T., Shenoy, R., Rose, K., Nakamura, S.,

Speck, J. S., Cohen, D. A.., Denbaars, S. P., "Selective and controllable lateral photoelectrochemical etching of nonpolar and semipolar InGaN/GaN multiple quantum well active regions," Appl. Phys. Express **8**, 066502 (2015).

[381] Gan, K. G.., Bowers, J. E., "Measurement of gain, group index, group velocity dispersion, and linewidth enhancement factor of an InGaN multiple quantum-well laser diode," IEEE Photonics Technol. Lett. **16**(5), 1256–1258 (2004).

[382] Zhang, Y. M., Piprek, J., Margalit, N., Anzlowar, M.., Bowers, J., "Cryogenic Performance of Double-Fused 1 . 5-um Vertical Cavity Lasers," J. Light. Technol. **17**(3), 503–508 (1999).

[383] Piprek, J., Babić, D. I.., Bowers, J. E., "Simulation and analysis of 1.55 μm double-fused vertical-cavity lasers," J. Appl. Phys. **81**(8), 3382 (1997).

[384] Babic, D. I., Piprek, J., Streubel, K., Mirin, R. P., Margalit, N. M., Mars, D. E., Bowers, J. E.., Hu, E. L., "Design and Analysis of Double-Fused 1.55-um Vertical-Cavity Lasers," IEEE J. Quantum Electron. **33**(8), 1369–1383 (1997).

[385] Murai, A., Thompson, D. B., Chen, C. Y., Mishra, U. K., Nakamura, S.., DenBaars, S. P., "Light-Emitting Diode Based on ZnO and GaN Direct Wafer Bonding," Jpn. J. Appl. Phys. **45**(No. 39), L1045–L1047 (2006).

[386] Murai, A., Thompson, D. B., Masui, H., Fellows, N., Mishra, U. K., Nakamura, S.., DenBaars, S. P., "Hexagonal pyramid shaped light-emitting diodes based on ZnO and GaN direct wafer bonding," Appl. Phys. Lett. **89**(17), 171116 (2006).

[387] "Google Image Search: visible light communication.", Google, 2015, <https://www.google.com/search?q=LiFi&biw=1913&bih=560&source=lnms&tbm=isch&sa=X&ved=0CAkQ_AUoBGoVChMIgOidi5WWyQIVFPBjCh2iNgBm#tbm=isch&q=visible+light+communication&imgrc=_>.

[388] Sikdar, D.., Premaratne, M., "Optical nanoantennas set the stage for a NEMS lab-on-a-chip revolution," J. Appl. Phys., 2015.

[389] Ulrich, L., "Whiter brights with lasers," IEEE Spectr. **50**(11), 37–56 (2013).

[390] Bayo, M. A. C., "Theory of elasticity and electric polarization effects in the group-III nitrides," University College Cork, Ireland (2013).

[391] Ioffe Institute, St. Petersburg, R., "Web Archive on Semiconductor Data," <http://www.ioffe.rssi.ru/SVA>.

[392] Suematsu, Y.., Adams, A. R., Handbook of Semiconductor Lasers and Photonic Integrated Circuits, London: Chapman & Hall (1994).

[393] Wintner, E.., Ippen, E. P., "Nonlinear carrier dynamics in GaxIn1−xAsyP1−y compounds," Appl. Phys. Lett. **44**(10), 999–1001 (1984).

[394] David, A.., Grundmann, M. J., "Droop in InGaN light-emitting diodes: A differential carrier lifetime analysis," Appl. Phys. Lett. **96**(10), 1–4 (2010).

[395] Shen, Y. C., Mueller, G. O., Watanabe, S., Gardner, N. F., Munkholm, A.., Krames, M. R., "Auger recombination in InGaN measured by photoluminescence," Appl.

Phys. Lett. **91**(14), 37–40 (2007).

[396] Zhang, M., Bhattacharya, P., Singh, J.., Hinckley, J., "Direct measurement of auger recombination in In0.1Ga0.9N/GaN quantum wells and its impact on the efficiency of In 0.1Ga0.9N/GaN multiple quantum well light emitting diodes," Appl. Phys. Lett. **95**(20), 201108 (2009).

[397] Meneghini, M., Trivellin, N., Meneghesso, G., Zanoni, E., Zehnder, U.., Hahn, B., "A combined electro-optical method for the determination of the recombination parameters in InGaN-based light-emitting diodes," J. Appl. Phys. **106**(11), 4–7 (2009).

[398] Scheibenzuber, W. G., Schwarz, U. T., Sulmoni, L., Dorsaz, J., Carlin, J.-F.., Grandjean, N., "Recombination coefficients of GaN-based laser diodes," J. Appl. Phys. **109**(9), 093106 (2011).

[399] Kioupakis, E., Rinke, P., Delaney, K. T.., Van de Walle, C. G., "Indirect Auger recombination as a cause of efficiency droop in nitride light-emitting diodes," Appl. Phys. Lett. **98**(16), 161107 (2011).

[400] Kioupakis, E., Yan, Q., Steiauf, D.., Van de Walle, C. G., "Temperature and carrier-density dependence of Auger and radiative recombination in nitride optoelectronic devices," New J. Phys. **15**(12), 125006 (2013).

[401] Romanov, A. E., Young, E. C., Wu, F., Tyagi, A., Gallinat, C. S., Nakamura, S., Denbaars, S. P.., Speck, J. S., "Basal plane misfit dislocations and stress relaxation in III-nitride semipolar heteroepitaxy," 1–12 (2011).

[402] Romanov, A. E., Baker, T. J., Nakamura, S.., Speck, J. S., "Strain-induced polarization in wurtzite III-nitride semipolar layers," J. Appl. Phys. **100**(2), 023522 (2006).

[403] Speck, J. S.., Chichibu, S. F., "Nonpolar and Semipolar Group III Nitride-Based Materials," MRS Bull. **34**(May), 304–309 (2009).

[404] Chichibu, S. F., Uedono, A., Onuma, T., Haskell, B. a., Chakraborty, A., Koyama, T., Fini, P. T., Keller, S., Denbaars, S. P., et al., "Origin of defect-insensitive emission probability in In-containing (Al,In,Ga)N alloy semiconductors.," Nat. Mater. **5**(10), 810–816 (2006).

[405] Park, S.-H.., Chuang, S.-L., "Crystal-orientation effects on the piezoelectric field and electronic properties of strained wurtzite semiconductors," Phys. Rev. B **59**(7), 4725–4737 (1999).

[406] Sakai, S.., Yamaguchi, A. A., "Theoretical analysis of optical polarization properties in semipolar and nonpolar InGaN quantum wells for precise determination of valence-band parameters in InGaN alloy material," Phys. status solidi **252**, 1–5 (2015).

[407] Schade, L., Schwarz, U. T., Wernicke, T., Rass, J., Ploch, S., Weyers, M.., Kneissl, M., "On the optical polarization properties of semipolar InGaN quantum wells," Appl. Phys. Lett. **99**(5), 051103 (2011).

[408] Goldhahn, R.., Piprek, J., Nitride Semiconductor Devices: Principles and Simulation, Wiley-VCH (2007).

[409] Johnson, P. B.., Christy, R. W., "Optical Constants of the Noble Metals," Phys. Rev. B **6**(12), 4370–4379 (1972).

[410] Johnson, P. B.., Christy, R. W., "Optical constants of transition metals: Ti, V, Cr, Mn, Fe, Co, Ni, and Pd," Phys. Rev. B **9**(12), 5056–5070 (1974).

[411] Ashida, T., Miyamura, A., Oka, N., Sato, Y., Yagi, T., Taketoshi, N., Baba, T.., Shigesato, Y., "Thermal transport properties of polycrystalline tin-doped indium oxide films," J. Appl. Phys. **105**(7), 73709 (2009).

[412] Wu, Z. L., Reichling, M., Hu, X. Q., Balasubramanian, K.., Guenther, K. H., "Absorption and thermal conductivity of oxide thin films measured by photothermal displacement and reflectance methods.," Appl. Opt. **32**(28), 5660–5665 (1993).

[413] Cahill, D. G.., Allen, T. H., "Thermal conductivity of sputtered and evaporated SiO2 and TiO2 optical coatings," Appl. Phys. Lett. **65**(3), 309–311 (1994).