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An Ultra-Wideband High Power-Added Efficiency Power Amplifier Design for 3 to 9 GHz Operation

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by

Zixi Liu

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ABSTRACT OF THE THESIS

An Ultra-Wideband High Power-Added Efficiency Power Amplifier Design for 3 to 9 GHz Operation

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Master of Science in Electrical and Computer Engineering

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Professor Yuanxun Wang, Chair

The development of materials and communication theories in the past several decades has led to more possibilities in power amplifier design and applications. In this thesis, a broadband power amplifier with power-added efficiency (PAE) between 25% to 48% (within the band of 3.3 GHz to 8.5 GHz) with a 12 V direct-current (DC) power supply and 32 dBm output power is implemented. The power amplifier consists of two single-stage gallium nitride (GaN) high-electron-mobility transistor (HEMT) amplifiers and two Marchand Baluns (balanced-unbalanced) for input and output matching. The amplifying stages have $25\,\Omega$ source impedance and $100\,\Omega$ load impedance for optimal PAE performance. The Marchand Baluns are based on two $\lambda/4$ short-circuit stubs connected to the balanced ports and a $\lambda/2$ open-circuited stub for the unbalanced port. One challenge in the Marchand Balun design is accommodating the impedance environment and ensuring close to $50\,\Omega$ source and load impedance at the input and output ports of the entire power amplifier module.

The thesis of Zixi Liu received approval from:

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University of California, Los Angeles

2025

To my parents,

for their unconditional love and support.

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LIST OF ABBREVIATIONS

Balun	Balanced-Unbalanced
CMOS	Complementary Metal-Oxide Semiconductor
GaN	Gallium Nitride
HEMT	High-Electron-Mobility Transistor
PA	Power Amplifier
PAE	Power-Added Efficiency
RF	Radio Frequency
T-Line	Transmission Line
UWB	Ultra-Wideband

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CHAPTER 1

Introduction

1.1 Background

Communication circuits have advanced rapidly over the past two decades, and commercialized products have significantly changed our lives, from 2G technology in the early 21st century to 5G and even 6G technology in the 2020s. Technological advances have also presented challenges to circuit design rubrics and requirements. With increased information capacity and users, communication systems nowadays require larger bandwidths and more channels.

The developments in materials have also changed the landscape of radio frequency (RF) circuit design in the past two decades. Introduced in the 1990s, gallium nitride (GaN) offers more possibilities for communication circuit designs. The large band gap of GaN enables the transistors to withstand higher voltages and thus deliver more power. The popularity of GaN devices has also boomed in the past ten years, ranging from RF circuits (e.g., 5G stations) to charger adapters, enabling more compact engineering solutions.

Power amplifiers (PAs), critical components in wireless communication transmitters, amplify signals for long-distance transmission. Consider the four factors in system design: power, size, cost, and performance. The introduction of GaN transistors can: a) increase the power efficiency of the circuit while producing a high-power output signal; b) reduce the size of the circuit by simplifying design; c) reduce the cost by reducing the number of electronic components; d) increase the output

signal power level through enhanced voltage handling capabilities.

In addition, gallium nitride power amplifiers can produce gain over a relatively wide band, meaning a single amplifier can work for multiple bands with acceptable performance. This advantage can save both the cost and the physical size of a circuit system. These advantages of GaN have made it one of the most attractive candidates in power amplifier designs.

1.2 Design Purposes and Environment

The objective of this power amplifier design started with an operating frequency of 3 to 9 GHz, which fell into the centimeter wave region. One advantage of centimeter waves is the reduced sensitivity to distance and lower power loss during transmission, a common issue for the 28-GHz 5G network we are currently using.

In addition to the frequency operating range, the power amplifier should be differential instead of single-ended. Introducing a differential stage can significantly reduce the common-mode noise of the circuit. To be more specific, when analyzing the small-signal model (i.e., linear model) of a fully differential amplifier, common-mode components are suppressed by the balanced symmetry of the two differential branches, reducing the common-mode noise at the same time. In contrast, the differential signals experience significantly higher amplification compared to the common-mode components.

In this design, the author applied the Hughes Research Lab (HRL) GaN high-electron-mobility transistors (HEMTs) with a 12 V voltage supply. Another crucial design aspect of power amplifiers is the power consumption and amplification of signal power: gain, power-added efficiency (PAE), and 1-dB compression point ($P_{\text{1-dB}}$). The design objective was to reach a 12 dB gain with a PAE of no less than 40% throughout the band after layout. The output power level was set to 30 dBm

(1 W) on a 50 Ω load impedance. Power amplifiers generally reach maximum PAE in the gain compression region; hence, the $P_{1\text{-dB}}$ point is unimportant, but mitigating gain compression can improve the PAE performance.

1.3 Topology and Design Process

The topology of this thesis consists of several basic modules: an input Marchand Balun (balanced-unbalanced), two single-stage amplifiers with input and output matching networks, and an output Marchand Balun. The input and output of the completed power amplifier (PA) module are matched to a 50 Ω source/load impedance pair.

The design approached as the following steps:

1. design of an amplifying stage (e.g., a single-stage amplifier) to validate the design topology and the potentials in gain and PAE;
2. design of Marchand Baluns (both the input and the output) and combine them with the two single-ended amplifiers into a differential PA;
3. ensuring the performance of the differential PA, double checking design parameters, and tuning for optimal performance;
4. layout of the differential PA and final testing;

1.4 Previous Works

This thesis contains two major sections where previous works contributed to the final outcome. There are two major challenges in this work: the design of a PA over a wide bandwidth and the design of low-loss Marchand Baluns for differential architecture.

For the power amplifier topology [1], J. Yan and other researchers mentioned that their power amplifier could deliver 41 to 43 dBm output power with a PAE from 47% to 63% under 30 V power supply. The researchers introduced a cascode (two transistors in a chain) topology for consistent gain and efficiency throughout the 0.5 to 2.5 GHz band. The high gain and PAE performance led to the author's decision to initiate this design with a cascode amplifying stage.

For the Marchand Baluns, Hammed [2] introduced a design of ultra-wideband (UWB) Marchand Balun that worked from 3.1 to 10.6 GHz with $|S_{11}| < -10\,\text{dB}$. Since the design was close to the expected operating band of this thesis, the design of Marchand Baluns stemmed from this paper. However, due to the different impedance settings, the Marchand Baluns required modifications to function properly for this thesis.

CHAPTER 2

Fundamental Concepts and Approaches

2.1 Fundamental Concepts

2.1.1 Gain

Gain describes the circuit's ability to amplify the signal input and deliver it to the output. The gain of a circuit is defined as the ratio of the output signal magnitude to the input signal magnitude. However, there is a difference between the typical voltage gain in analog circuit design and the power gain used for power amplifier design. While voltage gain measures the amplification of the signal voltage, power gain quantifies the actual energy transfer to the load. This energy transfer quantification is essential in power amplifiers where efficiency and impedance matching play crucial roles in PA design. To express the definition of gain in equation form:

$$A_V = \frac{V_{\text{out}}}{V_{\text{in}}} \quad \text{(unitless or expressed in decibels: } 20\log_{10}(A_V)\text{)} \tag{2.1}$$

$$G_P = \frac{P_{\text{out}}}{P_{\text{in}}} \quad \text{(unitless or expressed in decibels: } 10\log_{10}(G_P)\text{)} \tag{2.2}$$

In addition, there is a difference between small-signal gain and large-signal gain. Small-signal gain is based on a linear model where the signal needs to be relatively small compared to the biasing point. However, the large output signal power in a PA means that the signal is no longer relatively small. This means the power gain of a PA differs from the small-signal S-parameter gain S_{21}. Researchers utilize harmonic balance simulations to obtain large-signal gain in power amplifier design. Though not accurate, the small-signal voltage gain (S_{21}) is a helpful tool in

demonstrating the amplifier's potential during the designing phase. The original goal for this power amplifier's large-signal power gain was 12 dB under gain compression (where $|S_{21}|$ voltage gain is approximately 15 dB without compression).

2.1.2 S-Parameters

S-parameters are crucial in describing the circuit behavior under a high-frequency environment, which represents the interaction between the incident and reflected voltage waves.

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{2.3}$$

Take a two-port system as an example, which is shown in Figure 2.1 [3]. The relationship between the four voltage waves can be written as in Equation 2.3. S_{11} refers to the input return loss, which indicates the quality of the input matching network, whereas S_{22} denotes the output return loss and assesses the quality of the output matching network. In most narrow-bandwidth designs, designers generally aim for a lower than -20 dB magnitude for $|S_{11}|$ and $|S_{22}|$ after impedance matching. However, achieving such a high-quality matching in an ultra-wideband environment is impossible. In this design, the author aimed for $|S_{11}| < -10\,\text{dB}$ and $|S_{22}| < -10\,\text{dB}$ matching throughout the 3 to 9 GHz band.

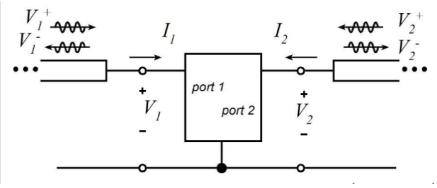

Figure 2.1: Two-Port System S-Parameters Definition

S_{21} and S_{12} describe the input and output interaction. S_{21} is the forward voltage gain of the system, and S_{12} is the isolation of the system. The two-port system is unilateral if $|S_{12}|$ is zero. In small-signal radio frequency design, $|S_{21}|$ is the small-signal voltage gain. However, in power amplifier

design, $|S_{21}|$ is not the gain of power amplifiers in regular operation. S_{21} parameter can only hint at the large-signal gain and how to tune the circuit.

2.1.3 Input and Output Matching

In the design of power amplifiers, the matching rubrics are different from common approaches. To maximize output power and efficiency, the output ports of the two amplifying stages were matched based on the load-pull analysis results. In this design, the single-stage amplifying architecture offered a higher power output with significantly improved efficiency at a load impedance of 100 Ω; therefore, a non-50 Ω load was selected. The output Marchand Balun then converted the 100 Ω loads of the two amplifying stages to a single-ended 50 Ω output. This conversion also applied to the input ports where the input impedances of the amplifying stages were set to 25 Ω. The author mainly utilized L-C networks and inductive degeneration in this design to match the input and output ports.

2.1.3.1 L-C Matching Network

L-C matching is a common approach in impedance matching. In this design, both the input and output ports of the amplifying stages contained at least one L-C matching network. Both inductors and capacitors are frequency-dependent; hence, the changes in reactance and susceptance also depend on the operating frequency. A series-connected inductor or capacitor changes the impedance along a constant resistance circle on the Smith Chart. In contrast, a shunt-connected inductor or capacitor changes the admittance along a constant conductance circle. By introducing a series-shunt network, the impedances at specific frequencies can be modified to any impedance points on the Smith Chart. In unilateral systems, the required inductor and capacitor values can be calculated. However, due to the bilateral nature ($|S_{12}| \neq 0$) of gallium nitride transistors, the

calculation is more for the magnitude level than the exact number.

$$\begin{aligned} \text{Inductive reactance:} \quad & X_L = \omega L \\ \text{Capacitive reactance:} \quad & X_C = -\frac{1}{\omega C} \\ \text{Inductive susceptance:} \quad & B_L = -\frac{1}{\omega L} \\ \text{Capacitive susceptance:} \quad & B_C = \omega C \end{aligned} \tag{2.4}$$

For example, at 6 GHz (the center operating frequency), if the required change in reactance and susceptance are assigned as $\pm 10\,\Omega$ and $\pm 10\,\text{S}$ respectively, the corresponding inductance and capacitance values are:

$$\begin{aligned} \text{Series-connected } L &= \frac{X_L}{\omega} = \frac{10}{2\pi \times 6 \times 10^9} \approx \boxed{0.265\,\text{nH}} \\ \text{Series-connected } C &= \frac{1}{\omega |X_C|} = \frac{1}{2\pi \times 6 \times 10^9 \times 10} \approx \boxed{2.65\,\text{pF}} \\ \text{Shunt-connected } C &= \frac{B_C}{\omega} = \frac{10}{2\pi \times 6 \times 10^9} \approx \boxed{265\,\text{pF}} \\ \text{Shunt-connected } L &= \frac{1}{\omega |B_L|} = \frac{1}{2\pi \times 6 \times 10^9 \times 10} \approx \boxed{2.65\,\text{pH}} \end{aligned} \tag{2.5}$$

2.1.3.2 Inductive Degeneration

Another common matching approach is inductive degeneration. This approach was used in the single-stage design to improve stability and assist input matching. The analysis is shown below with the schematic [4] in Figure 2.2.

$$V_P = \left(I_X + \frac{g_m I_X}{C_{GS1} s} \right) L_1 s \tag{2.6}$$

$$V_X = V_{GS1} + V_P \tag{2.7}$$

$$\frac{V_X}{I_X} = \frac{1}{C_{GS1} s} + L_1 s + \frac{g_m L_1}{C_{GS1}} \tag{2.8}$$

For input matching, the designers generally set the real part ($\frac{g_m L_1}{C_{GS1}}$) as $50\,\Omega$. However, inductive degeneration primarily served to enhance the stability of the PA in this thesis. The inductive

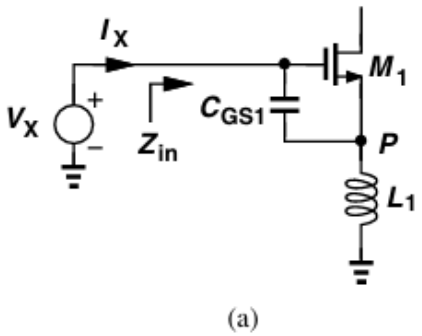

Figure 2.2: Inductive Degeneration Demonstration

degeneration also served as an equivalent model for the inductive effect of the bond wire connecting between the chip and the printed circuit board (PCB).

2.1.3.3 Feedback Loop

In the previous work [1], the researchers also applied an R-C feedback loop for the cascode PA topology, which enhanced stability and broadband input matching. However, feedback also reduced the circuit's gain. In a cascode design, the gain of the power amplifier is high enough to compensate for such loss, but it is not acceptable for a single-stage design. Therefore, the author decided not to use feedback for the single-stage amplifiers.

2.1.4 Gain Compression and Power-Added Efficiency

Gain compression in a power amplifier occurs when the output power deviates from linearity at high input levels, leading to a reduction in gain. The input power level that causes a 1 dB gain drop is defined as the 1-dB gain compression point ($P_{1\text{-dB}}$). This nonlinear behavior arises as transistors approach saturation. The maximum power-added efficiency (PAE) occurs in the gain compression region for most PAs. However, gain compression can also introduce distortion (e.g., harmonic generation, intermodulation), which should be considered while choosing the input power level for

optimal PAE performance.

One of the key objectives in this design was to reach a high PAE throughout a wide bandwidth with a 12 V direct-current (DC) supply. PAE quantifies how effectively a power amplifier converts the input signal power into useful RF output power, accounting for both amplification gain and DC power consumption. It is calculated as:

$$\text{PAE} = \frac{P_{\text{RF-out}} - P_{\text{RF-in}}}{P_{\text{DC}}} \times 100\% \tag{2.9}$$

where P_{out} is the RF output power, P_{in} is the RF input power, and P_{DC} is the DC supply power consumed. Unlike drain efficiency, which ignores input power in the calculation, PAE highlights the amount of power the amplifier adds to the signal. This thesis originally aimed to design a PA with 40% PAE throughout the operating band after layout.

2.1.5 Stability

Stability refers to an amplifier's ability to avoid oscillations (unwanted signal generation) under all operating conditions and source/load impedance pairs. There are two main parameters for checking the stability of a circuit: the stability K factor and the Δ factor. The stability results depend on the testing environment, meaning the source and load impedance should be set according to our design. The circuit is stable if $K > 1$ and $|\Delta| < 1$ at the same time, where,

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.10}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.11}$$

In designing wideband PAs, the designers should check for unconditional stability across all relevant frequencies with given source/load impedance pair values, avoiding instability at harmonics. A rule of thumb is to check stability across DC to the third-order harmonics of the operating frequencies. In this design, the author decided to run stability simulations from 0 Hz to 30 GHz.

2.2 Power Amplifier Classes

There are multiple classes of power amplifiers, and the most fundamental four are A, B, AB, and C. These four amplifier classes are differentiated by their conduction angles—the portion of the input signal cycle during which the transistors conduct current. There are other PA classes that contain more complicated harmonic matching modules for higher efficiency. However, the harmonic matching design does not fit the ultra-wideband requirement of this project.

2.2.1 Class A (conduction angle = 360°)

Class A amplifiers conduct current during the entire operation. The gate voltage biasing point is above the threshold voltage ($V_{GS} > V_{th}$), enabling the output voltage to swing from 0 V to $+V_{DD}$ (single power supply) or $-V_{DD}$ to $+V_{DD}$ (dual power supply). In the absence of an RF input signal, the output remains at the DC quiescent point. This reduces the efficiency of Class A power amplifiers, but it can preserve the high linearity of the input signal. However, for high-PAE solutions, a Class A amplifier is not a viable option. The maximum theoretical efficiency of Class A is 50% with inductive load and usually drops to less than 30% in applications [4]. A schematic of Class A PA operation is shown in Figure 2.3 [4].

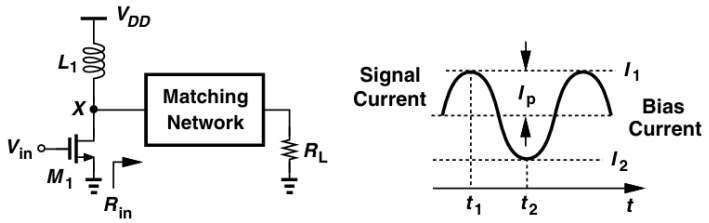

Figure 12.11 *Class A stage.*

Figure 2.3: Class A Power Amplifier Operation

2.2.2 Class B (conduction angle = 180°)

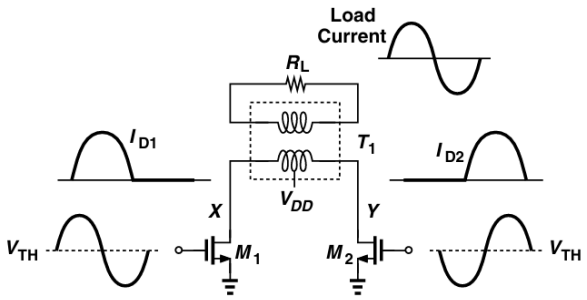

Figure 12.15 *Class B stage.*

Figure 2.4: Class B Power Amplifier Operation

Class B amplifiers are biased at the threshold voltage ($V_{GS} = V_{th}$), operating with a 180° conduction angle where current flows only during half of the input signal cycle. Compared to Class A PAs, Class B can reach higher efficiency, up to 78.5% [4]. However, to implement this half-cycle feature, the PAs typically require a cascode configuration called push-pull, which is more complex than single-stage Class A counterparts. In a Class B PA, each transistor turns on for only half of the cycle, which reduces the DC power consumption and boosts up the PAE. The problem with Class B PA is the crossover distortion when the two transistors switch between ON/OFF states. A schematic of Class B PA operation is demonstrated in Figure 2.4 [4].

2.2.3 Class AB (conduction angle = 180° < conduction angle < 360°)

A modification of Class B is the Class AB power amplifier. This class of PA has an efficiency between Class A and Class B, and it is widely used in RF applications. Introducing an overlap in the conduction states of the two transistors can reduce crossover distortion while maintaining high efficiency. This was the class of PA used in the previous work [1] and was implemented by the author for the cascode configuration.

Though with different architectures, the PA based on the single-stage amplifiers was also Class AB. For the depletion-mode GaN HEMTs in this project, the transistors still conduct a biasing current while the biasing voltage V_{GS} is negative. In addition, the assembled PA has differential inputs for the two amplifying stages, which is similar to the topology shown in Figure 2.4. By definition, the PA in this thesis is a Class AB type, which has a conduction angle between Class A and B. This can be further proved by the efficiency potential of the circuit in later chapters.

2.2.4 Class C (conduction angle = $0° <$ conduction angle $< 180°$)

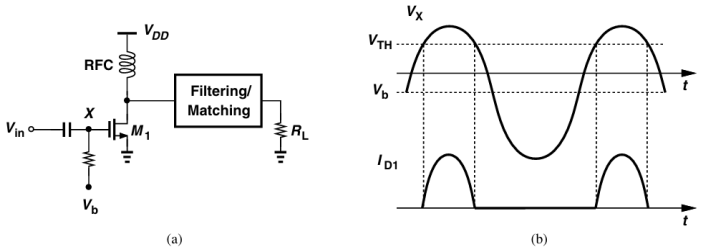

Figure 12.20 *(a) Class C stage and (b) its waveforms.*

Figure 2.5: Class C Power Amplifier Operation

Unlike previous classes, this class of PAs has a conduction angle less than 180°. This conduction feature sacrifices the system's linearity but promotes high efficiency, where Class C PAs can reach higher than 80% PAE in simulation. However, due to the current cut-off and non-linearity, Class C PAs are used more for pulsed signal transmission. A schematic of Class C PA operation is shown in Figure 2.5 [4].

2.3 Load-Pull Simulation

Load-pull analysis helps designers find the load impedance for the optimal performance of a circuit, including output power and PAE with acceptable linearity. In power amplifier designs, the load impedance can significantly affect the power output level, resulting in a difference in PAE

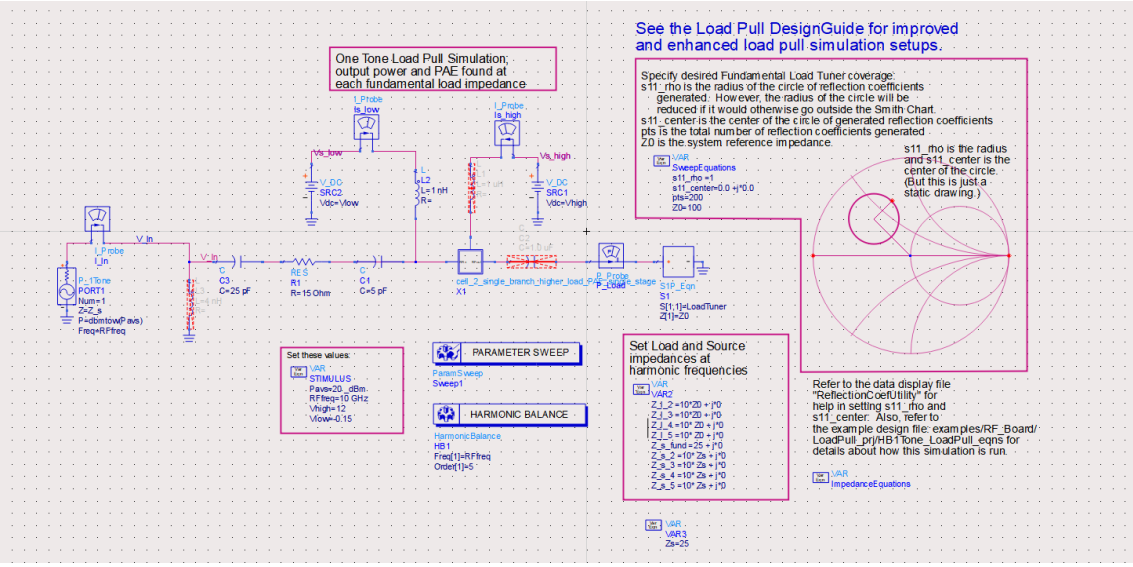

Figure 2.6: Load-Pull Test Schematic

performance. The author referred to the Advanced Design System (ADS) design guide when setting up the load-pull simulation. By changing the testing load impedance and referring to the Smith Chart, RF designers can find the potential of PAE with the given load and the corresponding source impedance. Figure 2.6 was the load-pull test bench used during the single-stage design. The input matching network was moved out from the PA module to the test bench for higher accuracy in PAE, as shown in the figure. The optimal load impedance for the single-stage amplifiers was found to be 100 Ω.

2.4 Differential Pair Matching with Marchand Baluns

In this design, the input signal was split first for the two amplifying branches, and then the signal was combined again for the power output. Therefore, the design required two balun modules: the input balun converts the single-ended input (unbalanced) into differential signals (balanced) for the two amplifying stages; the output balun converts differential signals from the amplifying stages' outputs into a single-ended signal for the PA module 50 Ω load.

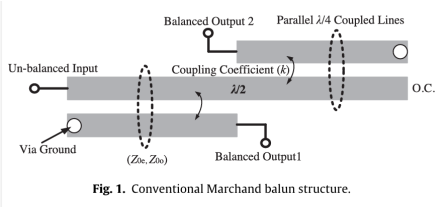

Figure 2.7: Marchand Balun Structure Demonstration

Marchand Balun is a common approach in balun design. It consists of two coupled transmission lines (T-Lines): two $\lambda/4$ T-Lines, each with one terminal connected to one of the differential ports and the other to the ground; and one $\lambda/2$ T-Line coupled with the two $\lambda/4$ T-Lines, with one end connected to the single-ended port and one end being open. A schematic is shown in Figure 2.7 [2]. Marchand Baluns have a 3:1 matching capacity, meaning with the 6 GHz center frequency, it can split power between 3 to 9 GHz efficiently.

To reduce the system complexity, the author first implemented the ideal Marchand Baluns in testing [5]. The design of the ideal Marchand Baluns was based on a two-port environment, meaning the differential ports were connected. In this case, the Port 2 (differential ports) impedance would be twice that of the desired unconnected differential port impedance. The author obtained ideal input and output baluns by using ideal coupled lines in the ADS library. The author configured the input balun's differential port impedance to 25 Ω (meaning Port 2 was 50 Ω for S-parameters simulation) and set the single-ended port to 50 Ω. However, during the layout, the author found that the bandwidth of this design was less than the all-50 Ω design, leading to a narrower bandwidth after the layout. This part will be further discussed in Chapter 6. As for the ideal input balun, the differential port impedance equals 25 Ω if Z_r is set to 25 Ω, and Z_r = 50 Ω leads to 50 Ω differential ports.

The ideal output Marchand Balun was also constructed in the same configuration, only with differences in Z_e, Z_o, Z_r, and Z_1. Compared to the input balun (differential port impedance =

25 Ω), the Z_e and Z_o of the output balun were doubled for 100 Ω differential port impedance (Port 2 impedance was 200 Ω for S-parameters simulation). This would be a helpful guideline in the layout section for transmission line (T-Line) widths. There are also other approaches to the balun module. One of them is inductive transformers. However, due to the lossy nature of transformers, the peak PAE would drop to less than 25% in simulation. For the conciseness of this thesis, the setup and results will not be discussed.

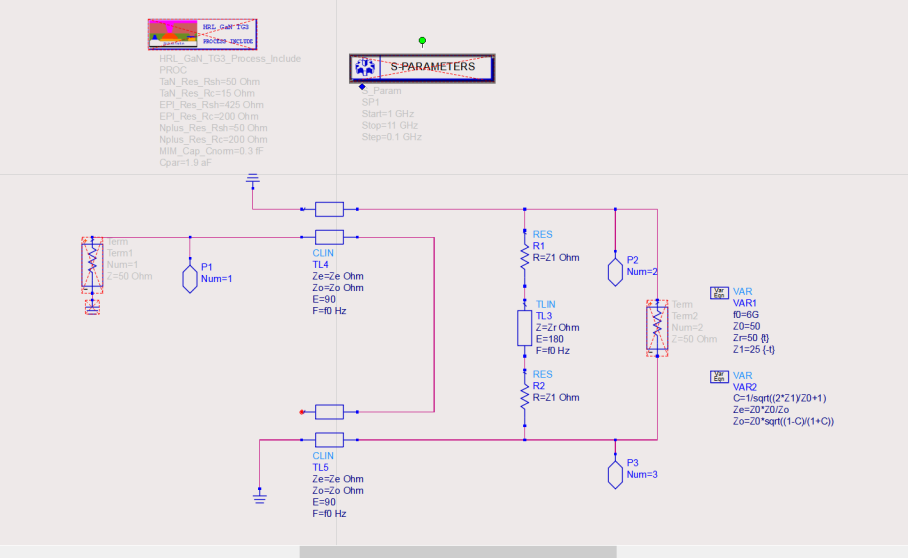

Figure 2.8: Ideal Input Marchand Balun Schematic (Differential Port Impedance = 25 Ω)

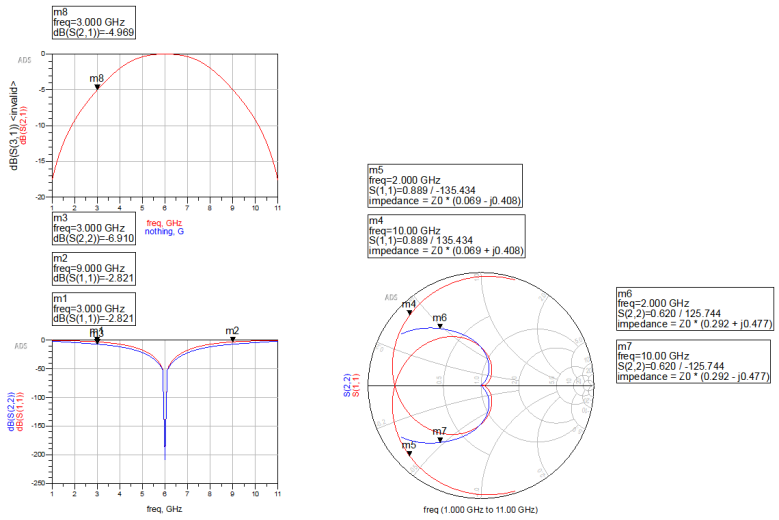

Figure 2.9: Ideal Input Marchand Balun S-parameters Simulation Results

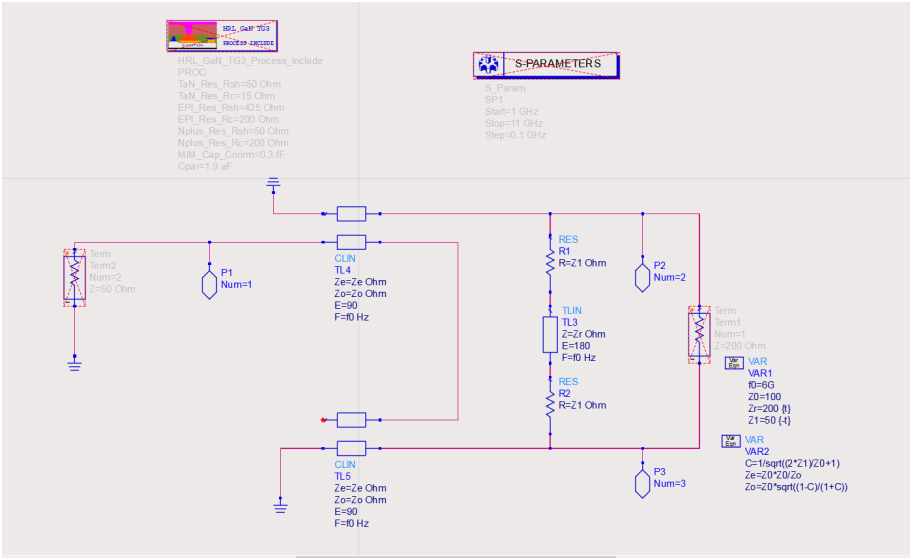

Figure 2.10: Ideal Output Marchand Balun Schematic (Differential Port Impedance = 100 Ω)

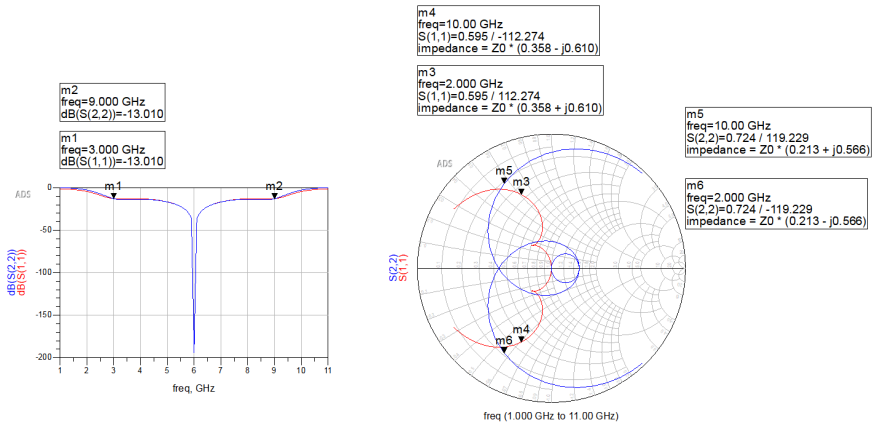

Figure 2.11: Ideal Output Marchand Balun S-parameters Simulation Results

CHAPTER 3

Cascode Approach

Under the influence of the previous work [1], the design was initiated using a cascode design for the amplifying stages. This approach has several advantages compared to single-stage amplifiers.

3.1 Cascode Topology Advantages

When designing complementary metal-oxide-semiconductor (CMOS) amplifiers, a cascode topology is a common approach for achieving a higher gain for the amplifier compared to the single-stage counterpart. Two-stage amplifiers have two main advantages:

3.1.1 Two-Stage Amplification

The most significant advantage of cascode design is that it has two amplifying stages: a common-source and a common-gate stage. A simplified voltage gain analysis is given as follows (r_{ds} is the drain-source on-resistance):

$$\begin{aligned} A_v &= g_{m_1} \cdot \left(R_{in_2} \parallel r_{ds_1}\right) \cdot g_{m_2} \left(R_{in_2} \parallel Z_L\right) \\ &= g_{m_1} \cdot \left(\frac{1}{g_{m_2}} \parallel r_{ds_1}\right) \cdot g_{m_2} \left(r_{ds_2} \parallel Z_L\right) \\ &= g_{m_1} \cdot g_{m_2} \cdot \frac{r_{ds_1}}{l + g_{m_2} \cdot r_{ds_1}} \cdot \frac{r_{ds_2} \cdot Z_L}{r_{ds_2} + Z_L} \end{aligned} \tag{3.1}$$

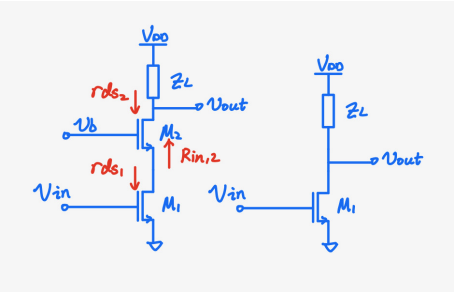

Figure 3.1: Cascode vs. Single-Stage Analysis

While for the single-stage design:

$$\begin{aligned} A_v &= g_{m_1} \cdot \left(r_{ds_1} \parallel Z_L\right) \\ &= g_{m_1} \cdot \frac{r_{ds_1} \cdot Z_L}{r_{ds_1} + Z_L} \end{aligned} \tag{3.2}$$

Assume $r_{ds_1} \approx r_{ds_2}$ under identical transistor size and biasing for analytical simplification. By comparing the two equations, it is obvious that the cascode topology has an additional gain boost of $g_{m_2} \cdot \frac{r_{ds_1}}{1+g_{m_2} \cdot r_{ds_1}}$. Though this calculation is derived from small-signal analysis, it still demonstrates that the cascode configuration has the ability to deliver higher power to the same load compared to single-stage amplifiers, provided that gain compression does not occur.

3.1.2 Consistent Load and Feedback Loop

By applying a second stage, the equivalent small-signal output resistance (R_{out}) of cascode amplifiers is higher than the R_{out} of single-stage amplifiers with the same operating conditions [6]. This increase in output resistance reduces the sensitivity of cascode amplifiers against load variations. In addition, the common-gate stage blocks the direct coupling between the input and output ports, creating better isolation and reducing the Miller effect. These characteristics will assist cascode amplifiers with forming a consistent gain throughout the wide operating band, which is the performance this thesis aims for.

Feedback loop also played a significant role in stabilizing the cascode design. Compared to single-

stage amplifiers, the additional gain increase of cascode topology can compensate for the gain loss of feedback while retaining the stabilization benefit. The system obtained stability in the simulation (from DC to 16.2 GHz) as the author added a resistor-capacitor (R-C) feedback path between the input and output ports. This ensured that the stability K factor would always be less than 1, while the Δ factor would be greater than 1 throughout the frequencies. However, the cascode amplifier (Figure 3.2) became unstable beyond 16.2 GHz, which presents a potential hazard.

Another advantage of feedback is its effect on input and output matching. From Figure 3.4, we can see a well-matched input and output impedance throughout the wide bandwidth. The feedback loop ensured a flat gain curve over the operating band, with a gain variation of less than 1 dB.

3.2 Non-Ideality in PA Design and Considerations

The non-ideality in circuit elements can cause a significant difference between ideal and non-ideal design outcomes. Therefore, the author began the design process by taking into account the presence of non-ideal factors. In this design, the capacitors generally had relatively small values, causing fewer problems than the inductors. Hence, the main concern in non-ideal components fell on the inductors. For an inductor with 1 nH inductance and quality factor Q = 10 @ 2 GHz:

$$\begin{aligned} Q &= \frac{2\pi f L}{R}, \\ R &= \frac{2\pi f L}{Q} \\ &= \frac{2\pi \times 2 \times 10^{9}\,\text{Hz} \times 1 \times 10^{-9}\,\text{H}}{10} \\ &= \frac{4\pi}{10}\,\Omega \approx \boxed{1.257\,\Omega} \end{aligned} \tag{3.3}$$

The author estimated the resistance of inductors from here. For example, a 5 nH inductor would have around 6 Ω resistance. The reason for choosing a relatively low frequency for calculation is that this estimation will be more conservative regarding the loss due to inductors. Most commercial inductors exhibit lower resistance than the values calculated (for a given L value) using this model.

3.3 Approach to Cascode Amplifiers

The two-stage cascode schematic is presented in Figure 3.2 [1]. The dimensions of the transistors were determined based on the transistor datasheets. To start with, the author referred to the datasheets provided by the HRL. The datasheets demonstrated the gain and PAE potentials when transistors are properly matched.

There were four presets in the HRL library for transistor sizes (multiplication · channel width): $2 \cdot 25\,\mu m$, $4 \cdot 37\,\mu m$, $6 \cdot 50\,\mu m$, and $12 \cdot 50\,\mu m$. Only the $12 \cdot 50\,\mu m$ combination provided the current and transconductance required for proper amplification in the cascode setting after tests. For simplicity, the author used the same dimension for both transistors in the cascode topology and assumed an even (6 V vs. 6 V) drain-source voltage division between the upper and lower transistors.

Another factor of biasing was the gate-source voltage of the transistors and the biasing current introduced by the V_{GS}. Unlike traditional CMOS technology, the depletion-mode GaN HEMTs could operate under zero or negative V_{GS}. Due to the objective of chasing a high PAE while keeping the output power level, the power amplifier's DC power should be reduced to the minimum amount required for operation. By combining the datasheets and simulation results, the author found that the biasing current needs to be within the range of 100 to 200 mA for desired amplification and output power. Due to the confidentiality of the original datasheets, the graphs are not shown here [7].

There are two main factors when we consider the biasing current: a) the gain of the amplifier and b) the DC power consumption of the PA. Both factors are crucial for high efficiency and high power output. After testing multiple data points, the author applied 0.05 V as V_{GS} for the cascode amplifier transistors. This voltage setting was not the only optimal choice for biasing; the cascode amplifier could work properly with a biasing point from -0.20 V to +0.10 V.

Another factor was the input and output impedances used for the design environment. The author started the design with a 25 Ω source/load testing environment as in the previous work [1]. However, from the load-pull analysis, the amplifying stage required a 50 Ω load to reach the acceptable PAE range. A 25 Ω output environment would reduce the PAE to less than 30% over the entire band. Therefore, in the cascode design, the source/load impedance pair was set to a 25 Ω source and a 50 Ω load.

3.4 Matching and Load-Pull Analysis

3.4.1 Matching Network Results

Figure 3.2 presents the schematic incorporating impedance matching networks, with the input port matched to 25 Ω and the output port to 50 Ω. The values for elements are also recorded in the figure. Both transistors' V_{GS} were set to 0.05 V. The results on S-parameters and stability from 1 GHz to 11 GHz are also included. The stability from 0 to 30 GHz was also simulated and recorded in Figure 3.5. However, the amplifier was not unconditionally stable above 16.2 GHz. The $|S_{11}|$ was less than -15 dB, and the $|S_{22}|$ was less than -10 dB throughout the operating band. The small-signal gain of the circuit was 18 dB throughout the 3 to 9 GHz bandwidth.

For the four square graphs in Figure 3.4: the top left is the $|S_{21}|$ small-signal gain curve, the top right is the $|S_{11}|$ (red) and the $|S_{22}|$ (blue); the bottom left includes the stability K factor (blue) and the Δ factor (red); the bottom right figure is a rescaled stability graph that only has an amplitude of 2 on the Y-axis for clarity. This format works for all S-parameters simulation result figures in this thesis.

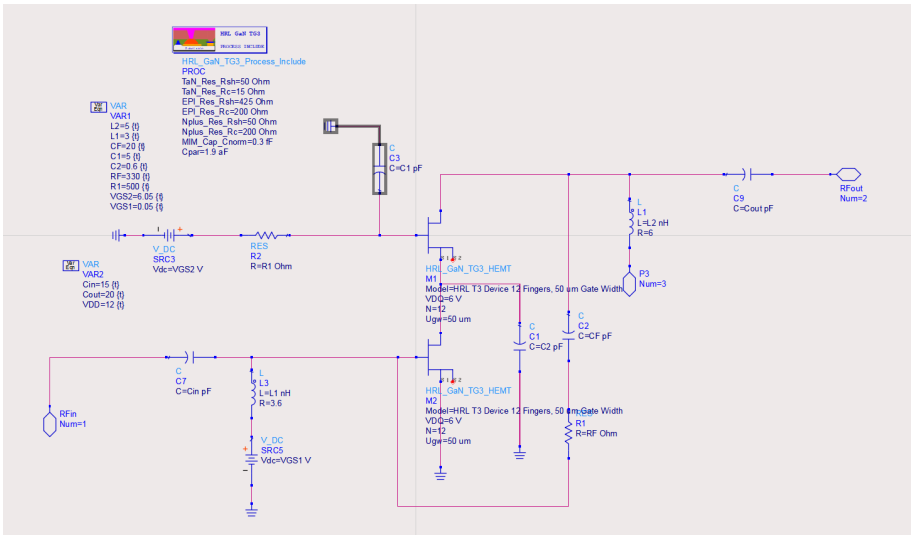

Figure 3.2: Schematic of the Cascode Approach with Input and Output Impedance Matched

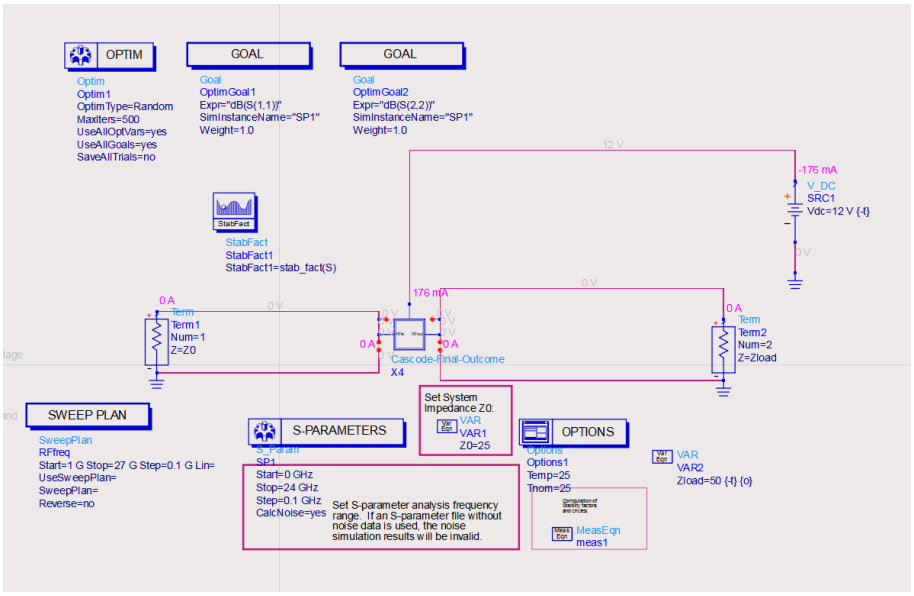

Figure 3.3: S-Parameters Test Schematic

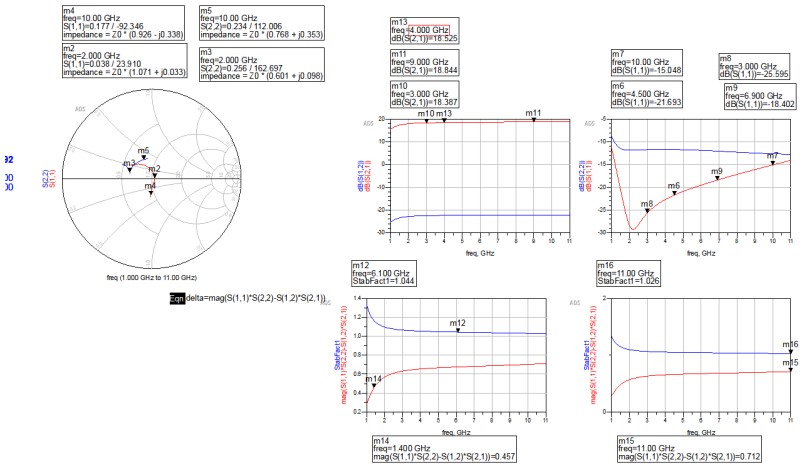

Figure 3.4: S-Parameters, Stability Factor, and Δ Factor Simulation Results for the Cascode Approach

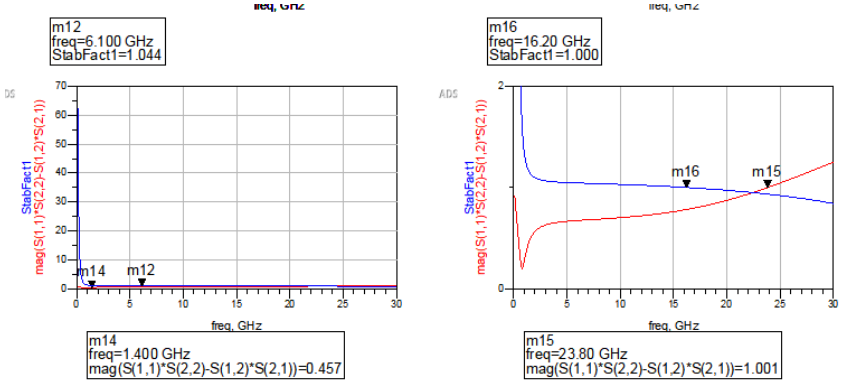

Figure 3.5: Stability Factor and Δ Factor Simulation Results for the Cascode Approach over 0 to 30 GHz Bandwidth

3.4.2 Load-Pull Results

The load-pull test is based on a given pair of source/load impedance values with designated input power and frequency. Hence, load-pull results only demonstrate the PAE potentials under specific settings. The author began with an input signal power (P_{in}) of +10 dBm and a signal frequency of 6 GHz. The amplifying stage could provide approximately 18 dB gain at this point. Then, the author increased the P_{in} to find the optimal input power range for the highest PAE values. The results showed that the single-branch cascode amplifier had the peak PAE value when $P_{in} = 20\,\text{dBm}$ with the given setting. After settling down the input power level, the author changed the input signal frequency from 3 GHz to 9 GHz. The highest PAE occurred near the center frequency; hence, the 6 GHz load-pull result is shown in Figure 3.7. The marker M3 in the bottom right Smith Chart (Figure 3.7) was approximately the corresponding source impedance at 6 GHz from the Smith Chart shown in Figure 3.4. The harmonic balance 1-tone simulation result under the same setting is shown in Figure 3.9, where the PAE was 34.8%. Note that the input matching network was built in the test bench to calculate the biasing port current for more accurate results, so the input matching network inside the amplifier module was shorted or opened correspondingly for this test.

With the $Z_{source} = 25\,\Omega$, $Z_{load} = 50\,\Omega$, and $P_{in} = 20\,\text{dBm}$ environment, the PAE of the cascode amplifying stage varied between 35% to 30% throughout the band. This PAE was lower than the objective of this thesis. The results did not improve significantly when the biasing points were changed.

Further increase in load impedance did not significantly improve PAE results. After re-matched the output impedance ($R_f = 400\,\Omega$, $C_{out} = 40\,\text{pF}$, etc.) and re-ran load-pull analysis under $100\,\Omega$ load while keeping other test bench settings the same, the maximum PAE only increased by 2%. For the conciseness of this thesis, only the results, instead of the entire procedures, are mentioned here (Figure 3.10).

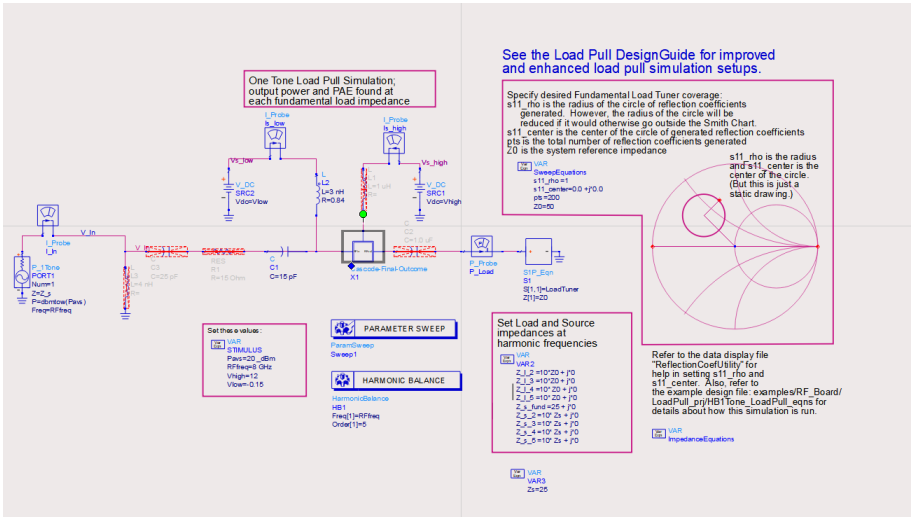

Figure 3.6: Load-Pull Test Schematic for the Cascode Architecture with $Z_{source} = 25\,\Omega$, $Z_{load} = 50\,\Omega$, $P_{in} = 20\,\text{dBm}$, $f_{in} = 6\,\text{GHz}$

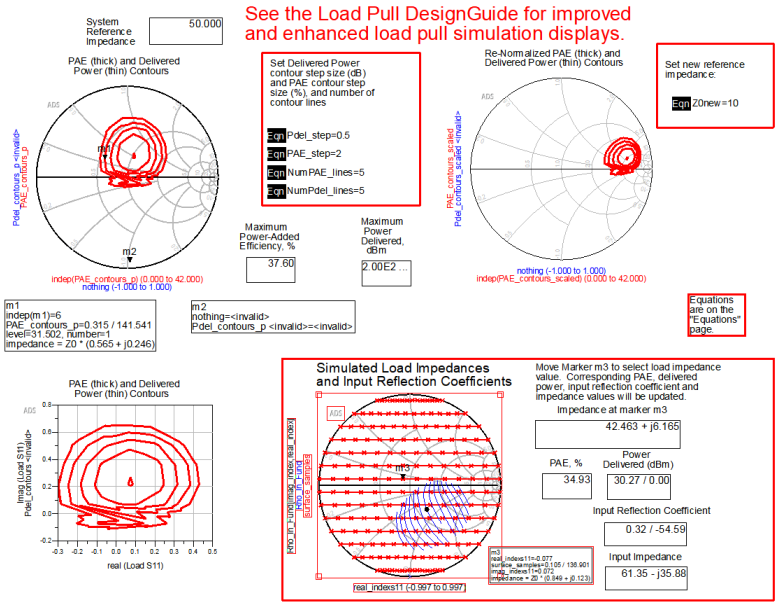

Figure 3.7: Load-Pull Result for the Cascode Architecture with $Z_{source} = 25\,\Omega$, $Z_{load} = 50\,\Omega$, $P_{in} = 20\,\text{dBm}$, $f_{in} = 6\,\text{GHz}$

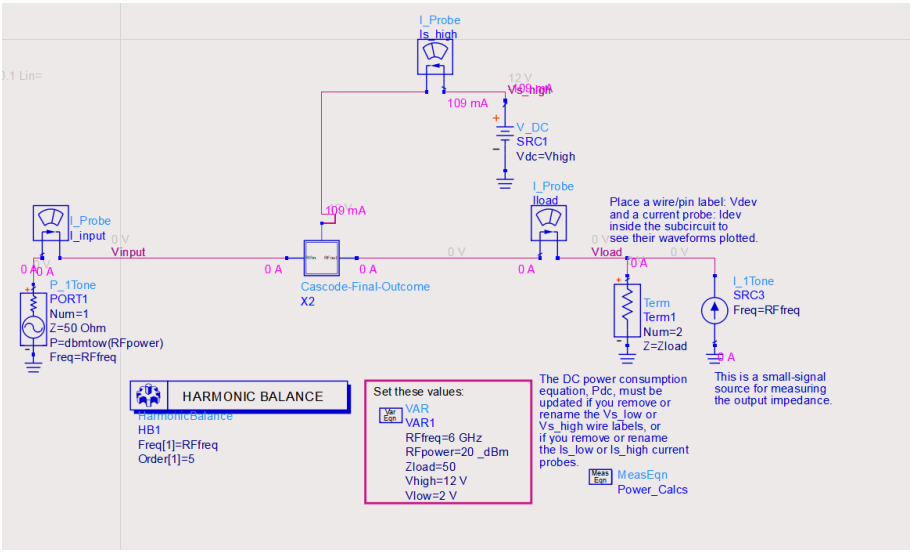

Figure 3.8: Harmonic Balance 1-Tone Test Schematic for the Cascode Architecture with $Z_{source} = 25\,\Omega$, $Z_{load} = 50\Omega$, $P_{in} = 20\,\text{dBm}$, $f_{in} = 6\,\text{GHz}$

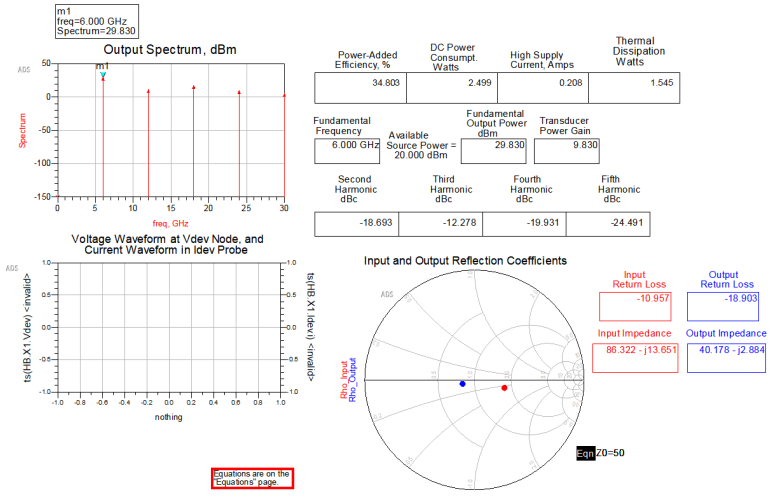

Figure 3.9: Harmonic Balance 1-Tone Result for the Cascode Architecture with $Z_{source} = 25\,\Omega$, $Z_{load} = 50\,\Omega$, $P_{in} = 20\,\text{dBm}$, $f_{in} = 6\,\text{GHz}$

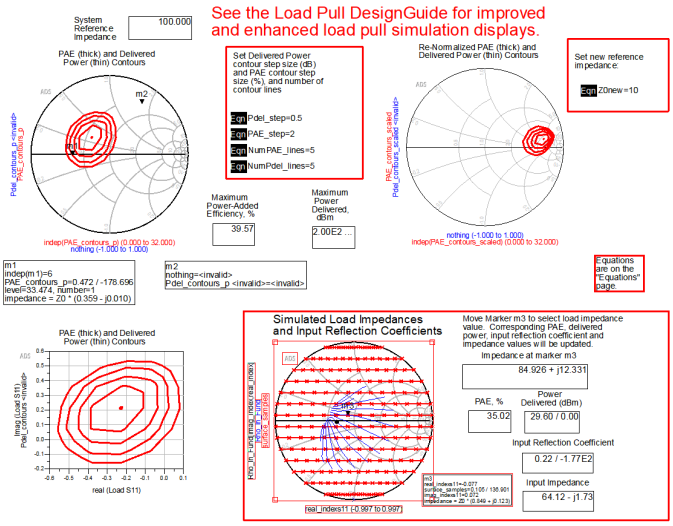

Figure 3.10: Load-Pull Result for the Cascode Architecture with $Z_{source} = 25\,\Omega$, $Z_{load} = 100\,\Omega$, $P_{in} = 20\,\text{dBm}$, $f_{in} = 6\,\text{GHz}$

3.5 Analysis and Conclusion on Cascode Architecture

The cascode design provided several desirable characteristics: consistent gain and matching throughout the operating band. However, the PAE of this topology was not desirable. Due to the $V_{DD} = 12\,\text{V}$ setting, each transistor was configured to a drain-source voltage (V_{DS}) of 6 V as the voltage headroom, which is not sufficient for large output signal levels. In the harmonic balance PAE simulation, the cascode topology endured severe gain compression, from 18 dB to 6 dB. The author also attempted to manipulate the voltage division between the two cascaded transistors, but the results did not improve significantly. After multiple attempts, the author decided to discard the cascode approach and move to a single-stage design.

CHAPTER 4

Single-Stage Amplifier Design

Compared to the cascode configuration, the single-stage approach has a relatively simple architecture, but there are several more challenges to overcome:

a) Unlike the cascode topology, the single-stage design is more sensitive to a feedback loop. This means a feedback loop for matching and stabilization is not a viable option while preserving a relatively high gain.

b) The input matching network is more complicated than the cascode amplifiers. In order to stabilize and match the input, the matching network has to integrate multiple approaches, which will be discussed in the next section.

c) The consistent gain of the cascode topology is hard to realize in the single-stage design. In the previous chapter, the author demonstrated the ability to have a less than 1 dB gain variation throughout the band with cascode topology. However, the single-stage configuration cannot deliver similar gain performance.

The advantage of the single-stage amplifier was its ability to apply a 12 V voltage headroom for the transistor to deliver output power. This helped the power amplifier to achieve a higher PAE.

4.1 Design of the Single-Stage Input Matching Network

4.1.1 General Considerations

One of the key takeaways from the cascode approach was the biasing point of transistors. The author first constructed the single-stage amplifiers based on the same biasing parameters as the

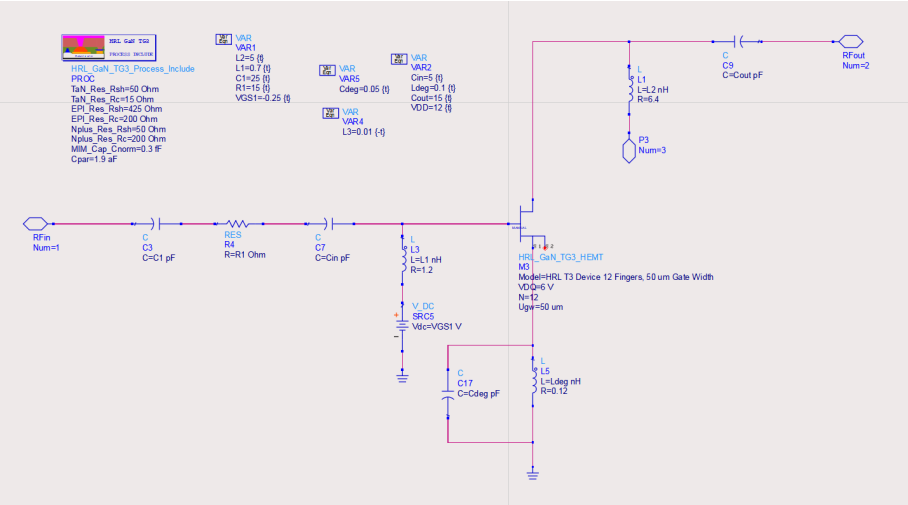

Figure 4.1: Schematic of the Single-Stage Approach with Input and Output Impedance Matched

cascode design. During the test, the author found that the biasing point can be further reduced for higher PAE while maintaining an acceptable gain. The new biasing point was $V_{GS} = -0.25\,\text{V}$ for the single-stage amplifier. This biasing could not improve the PAE of the cascode configuration but significantly enhanced the single-stage amplifiers' PAE throughout the operating band.

4.1.2 Modification on the Input Matching Network

As shown in Figure 4.1, the amplifier included not only L-C matching networks but also other distributed elements for input matching. Without the C_1 capacitor preceding the L-C network, the input S_{11} curves were located in the upper-right quadrant of the Smith Chart. To address the inductive nature of the amplifier, the C_1 capacitor was introduced, resulting in improved input matching for the amplifier. In addition, by introducing a resistor R_1 on the input signal path, the input and output return loss further improved by 3 to 5 dB while maintaining the gain. It is more effective than multistage L-C matching, which could introduce more loss due to inductors.

4.1.3 Inductive Degeneration Implementation

Another approach was inductive degeneration, a common approach in RF designs that can contribute to easier input matching and improved stability. The inductive degeneration was first introduced to increase the resistance (real part) of the input impedance, and the amplifier could get a good match with a 0.6 nH degenerative inductor (this also reduced the required resistance from R_1). However, the 0.6 nH degeneration introduced a significant drop in gain at higher frequencies (from 7 to 9 GHz) of the amplifier. This was due to the frequency-dependent reactance of inductors. The reactance of an inductor under 3 GHz is one-third of the reactance under 9 GHz.

The author made two adjustments to compensate for the gain loss:

a) Introducing a capacitor to bypass the inductor at high frequencies. The problem with such an approach was the reduction in efficiency across the lower-frequency band. Therefore, the capacitor had to be small enough to avoid its effect at lower frequencies.
b) Reducing the inductive degeneration and only utilizing the degeneration effect to stabilize the amplifier. This approach was not detrimental to both the gain and the PAE of the amplifying stage.

4.1.4 Adjustment in Load

The final step was to determine the optimal load of the amplifying stage through load-pull analysis. Based on the load-pull simulation results, the amplifier achieved the peak PAE with a load of 100 Ω, outperforming the 50 Ω load setting by approximately 10%. In the later Marchand Balun design process, this increase in load impedance would be compensated through an optimized balun configuration to achieve 50 Ω impedance matching at the output of the entire PA module. Therefore, the author applied the 100 Ω load environment for the single-stage amplifiers.

4.2 Simulation Results and Analysis

Compared to the cascode counterpart, the small-signal gain and matching were less desirable for the single-stage configuration (the test bench was the same as Figure 3.3 with the settings for the single-stage amplifier). $|S_{11}|$ was less than -10 dB for most of the band, while $|S_{22}|$ was less than -5 dB. The output matching was significantly less desirable compared to the cascode amplifier. Due to the large-signal nature of the power amplifier output, the author concentrated more on the PAE and output power performance. The load-pull test demonstrated the high PAE potential of the single-stage design: the amplifying stage reached more than 60% PAE throughout the band with ideal inductors. The PAE dropped when the Q = 10 @ 2 GHz rubric was applied to the inductors but still had more than 40% PAE throughout the band with a peak PAE of more than 55%. This significantly improved PAE result outperformed the cascode topology that only had a 40% peak PAE even with ideal inductors.

Another advantage of the single-stage amplifiers was unconditional stability up to the third harmonic frequency (Figure 4.3). Therefore, the single-stage power amplifier was more robust from a stability point of view. The amplifying stage was under gain compression when it reached the peak PAE, but the compression was less significant compared to the compression of the cascode amplifier. The output power of the single-stage amplifier could reach 30 dBm with a stable 8.7 to 9.5 dB gain over the operating band. In the simulation of the single-stage amplifier, the PAE maintained over 50% from 3.8 to 9 GHz and only dropped at the marginal frequencies. The design of the single-stage topology was settled here. The next step moved to implementing the differential architecture.

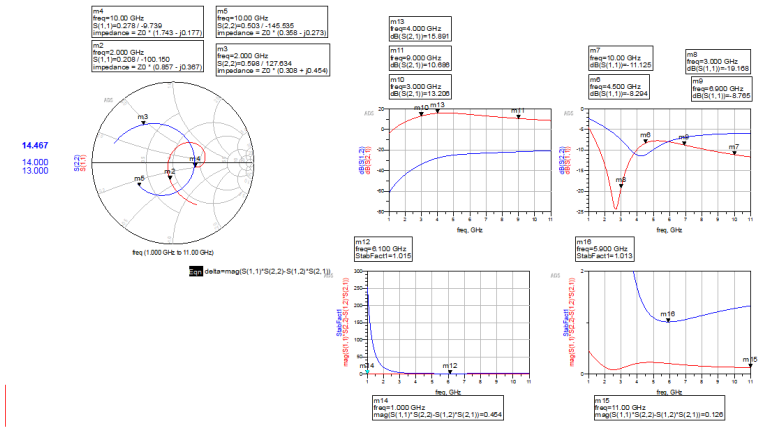

Figure 4.2: S-Parameters, Stability Factor, and Δ Factor Simulation Results for the Single-Stage Approach, with Q = 10 Rubric Applied

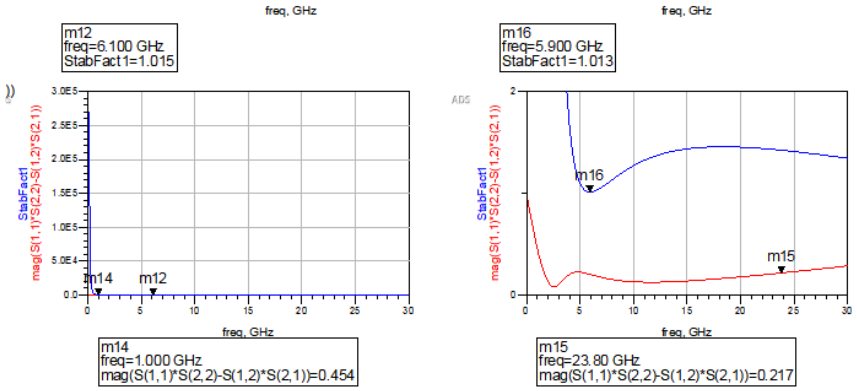

Figure 4.3: Stability Factor and Δ Factor Simulation Results for the Single-Stage Approach over 0 to 30 GHz Band, with Q = 10 Rubric Applied

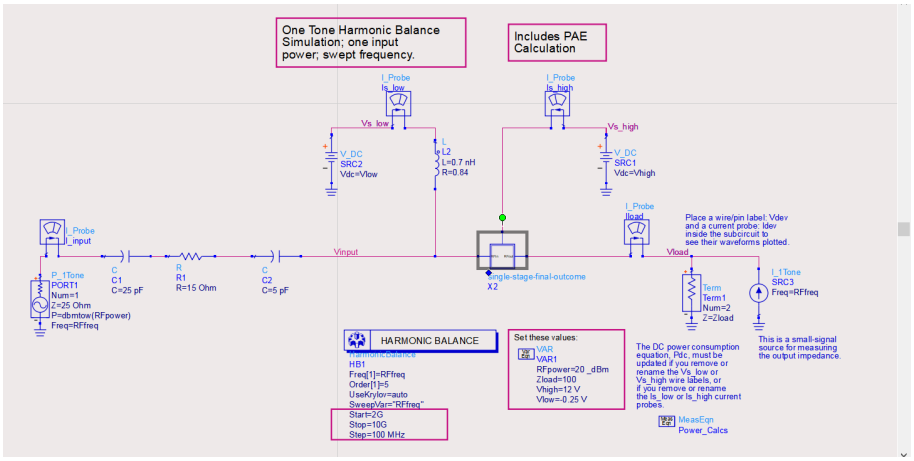

Figure 4.4: Harmonic Balance 1-Tone Test Schematic for the Single-Stage Architecture with PAE vs. Frequency, Sweeping from 2 GHz to 10 GHz

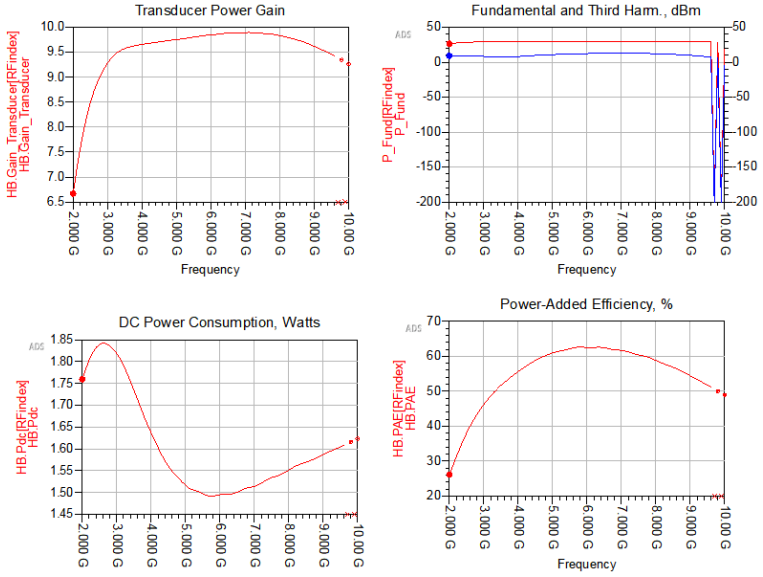

Figure 4.5: Harmonic Balance 1-Tone Simulation Results on PAE vs. Frequency, Sweeping from 2 GHz to 10 GHz, with Ideal Inductors

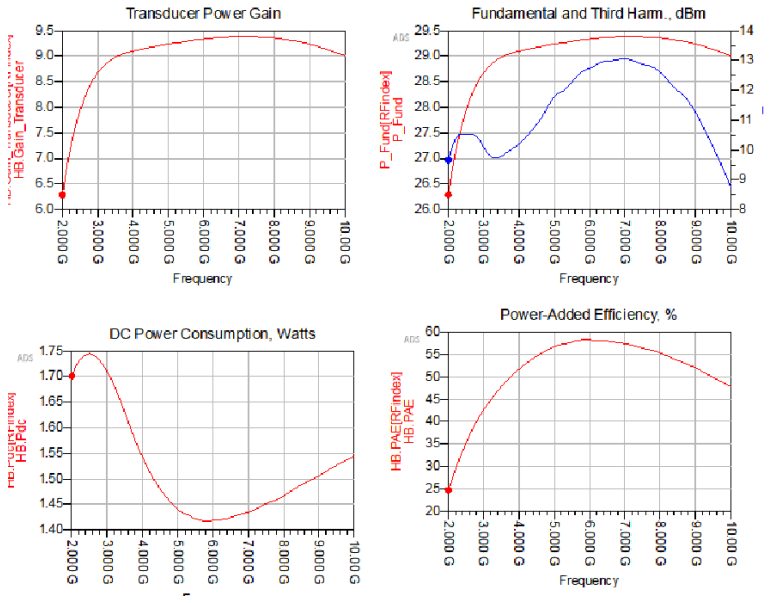

Figure 4.6: Harmonic Balance 1-Tone Simulation Results on PAE vs. Frequency, Sweeping from 2 GHz to 10 GHz, with Q = 10 Rubric Applied

CHAPTER 5

Differential PA Performance Before Layout

5.1 Setup

In this section, the author combined the ideal Marchand Baluns (Figure 2.8 and Figure 2.10) with the single-stage amplifiers from Chapter 4. The schematic is shown in Figure 5.1, where the two central modules are the two amplifying stages (Figure 4.1), and ideal input and output baluns are connected to the left and right of the amplifying stages, respectively. The assembled PA module works under a 50 Ω source/load impedance environment.

Then, the author performed the same test for the entire PA module. The first test was to ensure the stability and return loss of the circuit, which was based on the same test bench as in Figure 3.3 with a 50 Ω source/load pair of ports.

5.2 Results and Analysis

5.2.1 S-Parameters and Stability

Note that for the ideal Marchand Baluns, the $|S_{11}|$ parameters reached 0 dB at marginal frequencies (Figure 2.9 and Figure 2.11), causing simulation errors at these frequencies. The spike in stability factor K and $\Delta = 1$ only happened at f_{in} = 0, 12, and 24 GHz (Figure 5.3). This would not happen with the post-layout non-ideal baluns. Hence, the differential PA is stable from 0 to 30 GHz.

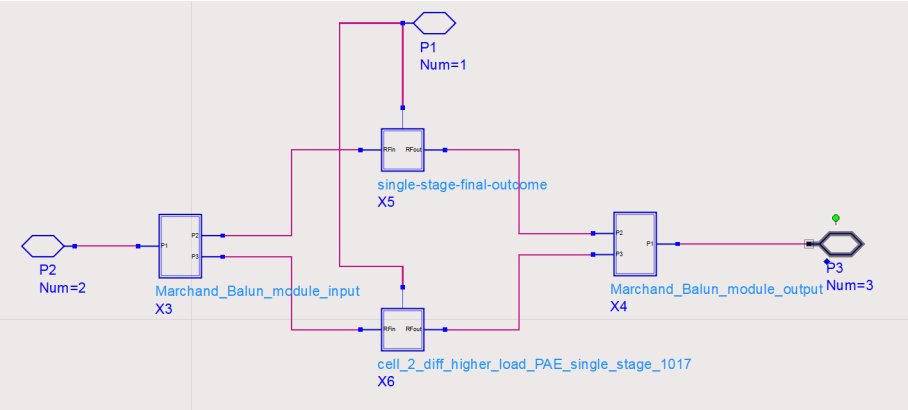

Figure 5.1: Combined Differential PA Schematic

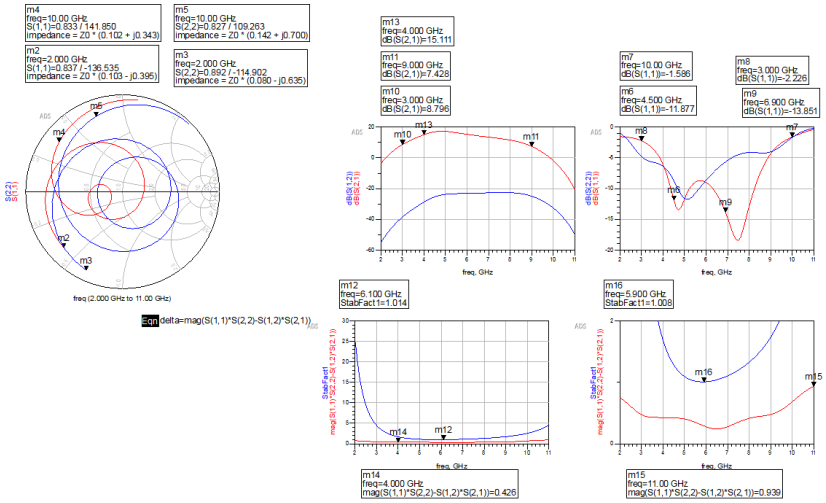

Figure 5.2: S-parameters, Stability Factor, and Δ Factor Performance of the Differential PA

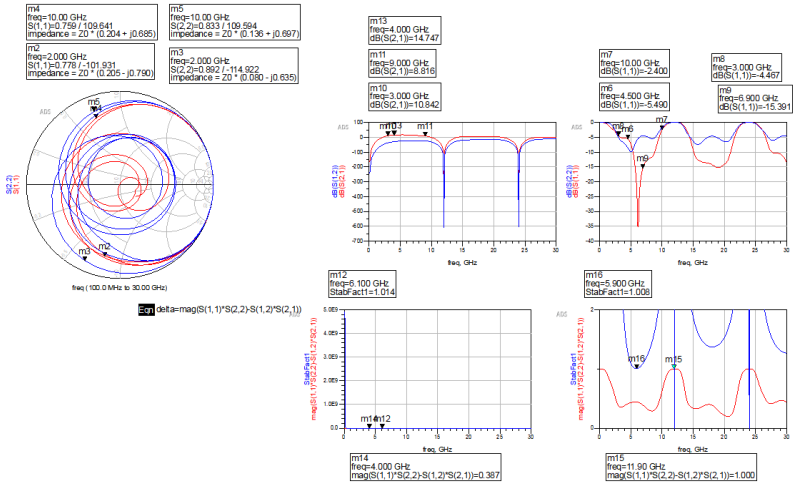

Figure 5.3: S-parameters, Stability Factor, and Δ Factor Performance over 0 to 30 GHz Band of the Differential PA

5.2.2 Large-Signal Gain and PAE

The gain and PAE for large-signal input power require harmonic balance simulation for more accurate results.

5.2.2.1 PAE and Gain vs. Input Power

In this section, the author used the design guide included in the ADS to analyze the effects of input power levels on the gain and the PAE of the differential PA design. The power sweep simulation was performed under 5 GHz, which is the center of the peak small-signal gain region. The 5 GHz input frequency was selected to evaluate the PA's performance in the region where the most severe gain compression occurs. Note that in the high PAE performance region, the power amplifier endured gain compression and distorted output signal (Figure 5.5). The distorted output signal still held an acceptable waveform, meaning the gain compression and the phase difference between the two signal paths were acceptable under the peak PAE performance setting.

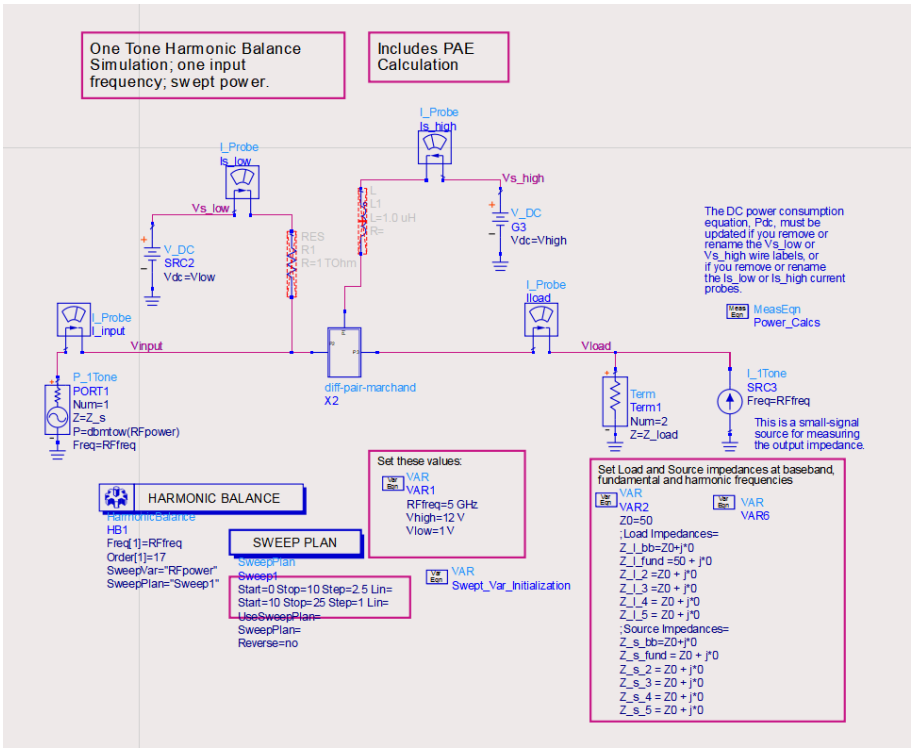

Figure 5.4: Schematic for Gain and PAE vs. Input Power Test of the Differential PA, with $f_{in} = 5\,\text{GHz}$

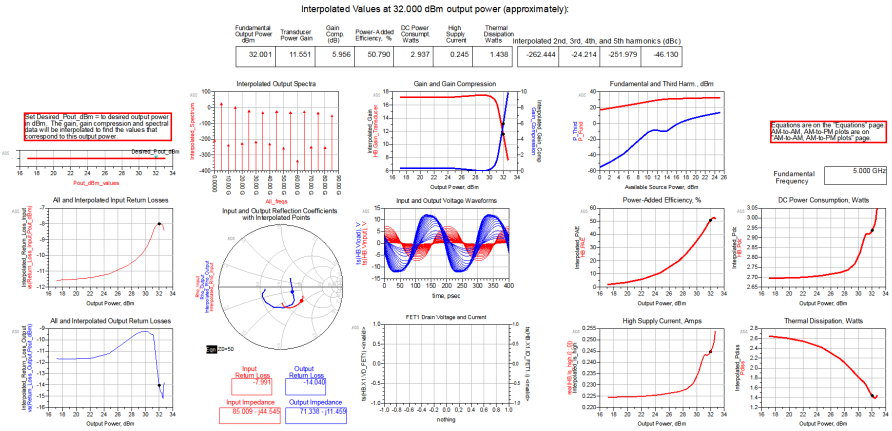

Figure 5.5: Results for Gain and PAE vs. Input Power Test of the Differential PA, with $f_{in} = 5\,\text{GHz}$

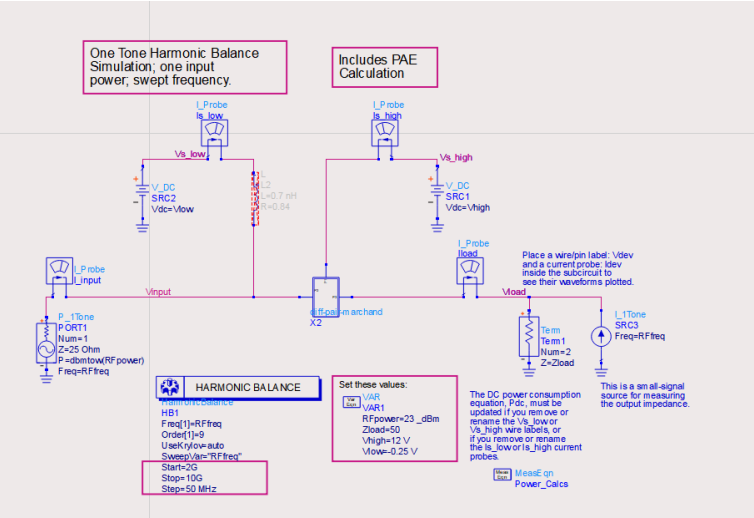

Figure 5.6: Schematic for Gain and PAE vs. Frequency Test of the Differential PA, with P_{in} = 23 dBm

5.2.2.2 PAE and Gain vs. Frequency with a Given Input Power

In the previous chapter, the power sweep of one amplifying stage showed that the highest PAE was achieved at P_{in} = 20 dBm. Since the input Marchand Balun split the power into two branches, there was a 3 dB reduction in the input power of each branch. Hence, for the differential pair, the input power should be 23 dBm for peak PAE performance. Different from the previous power sweep simulation, the input power was fixed in this test, and the only variable changing was the input signal frequency.

The simulation showed that with the ideal Marchand Baluns, the PA could provide 10 dB gain with a 3-dB bandwidth over the 3 to 9 GHz operating band. The maximum PAE reached 57% @ 6.8 GHz. The PAE was more than 40% over the 3.8 to 7.9 GHz band, with the marginal band PAE still around 30%. This is an acceptable performance considering the 3:1 bandwidth of Marchand Baluns.

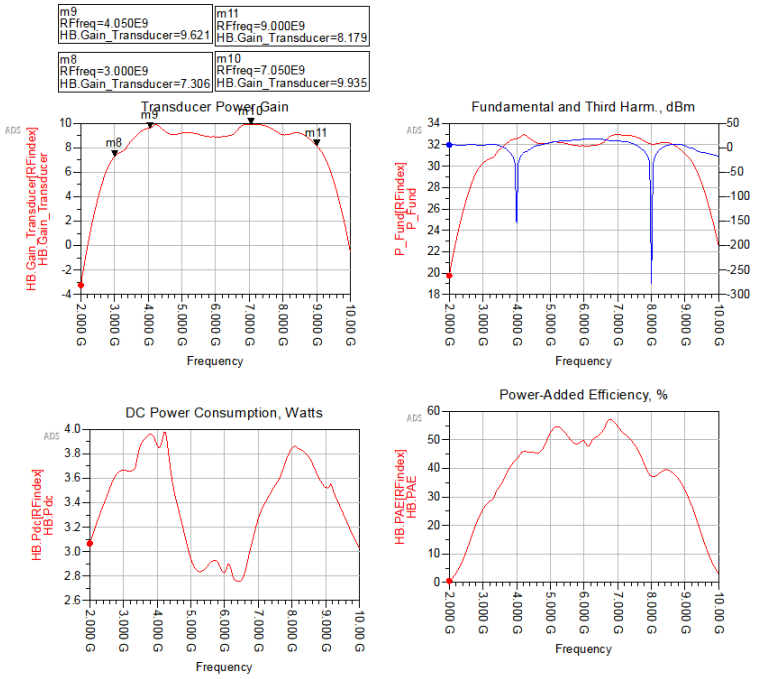

Figure 5.7: Results for Gain and PAE vs. Frequency Test of the Differential PA, with $P_{in} = 23$ dBm

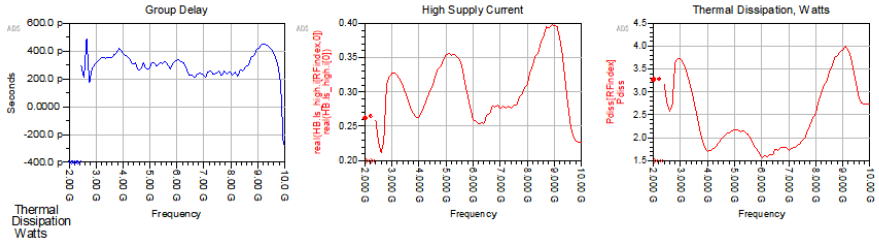

Figure 5.8: Group Delay, Current, and Heat Dissipation vs. Frequency of the Differential PA, with $P_{in} = 23$ dBm

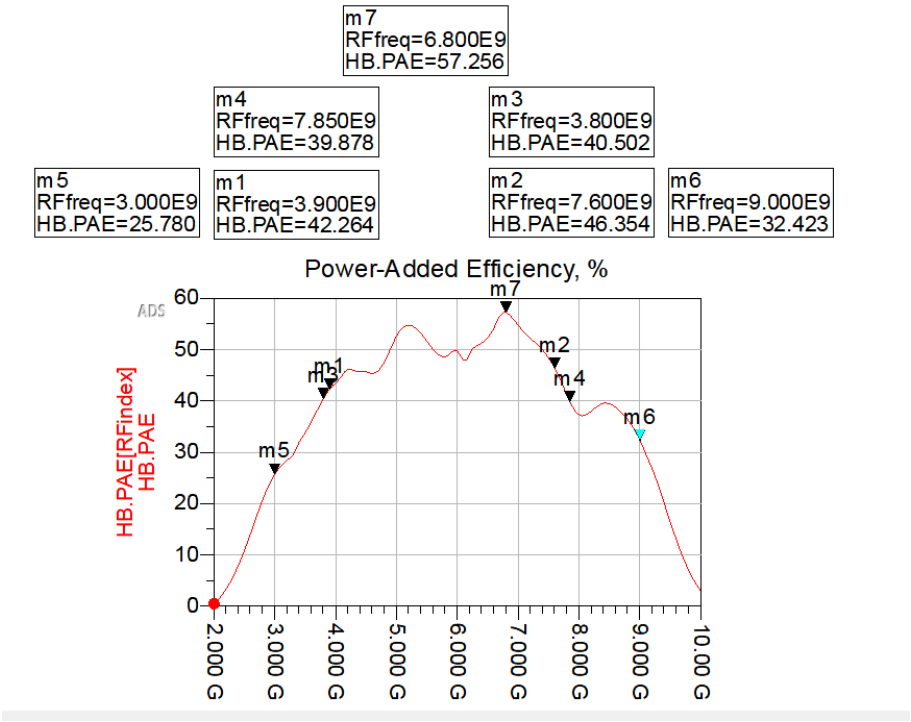

Figure 5.9: Marked PAE vs. Frequency Results of the Differential PA, with $P_{in} = 23\,\text{dBm}$

CHAPTER 6

Layout and Post-Layout Simulations

6.1 Marchand Balun Layout Setup

6.1.1 Layout Substrate

The layout substrate is demonstrated in Figure 6.1. The setup was the same as Hammed's ultra-wideband Marchand Balun [2]. However, both the input and the output Marchand Baluns in this design deviated from a uniform 50 Ω impedance environment; hence, the author had to design Marchand Baluns with non-50 Ω differential port impedance values.

6.1.2 Input Marchand Balun

The input Marchand Balun design was close to the result from Hammed's work [2]. The modification was mainly for the 25 Ω impedance for both differential ports. For clarity, both the 2-D view and the 3-D view are provided (Figure 6.2 & Figure 6.3). The grey layer in the figures is the Overlay2 (the lower conductor layer) in Figure 6.1; the red layer is the Overlay in Figure 6.1, and it is the upper conductor layer in the 2-D and 3-D layout graphs.

As for the ports, the red pad on the right (Figure 6.2) is the single-ended port (Port 1). The two grey pads on the left are Port 2 (upper) and Port 3 (lower) in the 2-D drawing. The yellow lines with the pads were for the ADS T-Line test environment setting. The two differential ports (Port 2 & Port 3) are on the same Overlay2 layer in the layout. The exact dimensions are provided in Table 6.1.

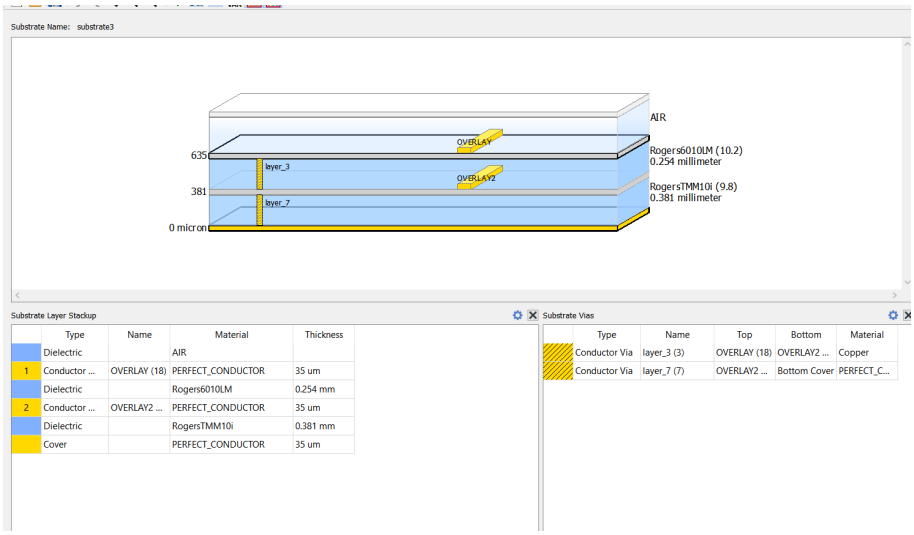

Figure 6.1: Layout Substrate of Marchand Baluns

The results for the $|S_{11}|$, insertion loss, and phase difference are presented in Figure 6.4 to Figure 6.6. The post-layout input Marchand Balun had more insertion loss in the lower frequencies compared to the higher frequencies. However, as the author tried to increase the $\lambda/4$ and $\lambda/2$ T-Line lengths, the loss at higher frequencies increased much faster than the loss reduction at lower frequencies. Hence, the author decided to keep this configuration. Since Marchand Baluns split the single-ended input power into two branches, a 3-dB loss on each path is expected; the actual loss on each signal path is $||S_{21}| + 3\,\text{dB}|$ and $||S_{31}| + 3\,\text{dB}|$, respectively. The input Marchand Balun could provide an input return loss bandwidth of better than 10 dB ($|S_{11}| < -10\,\text{dB}$) from 3.6 GHz to 8.3 GHz. The phase difference between the two branches was close to 180° (Figure 6.6), which proved the functionality of the input Marchand Balun.

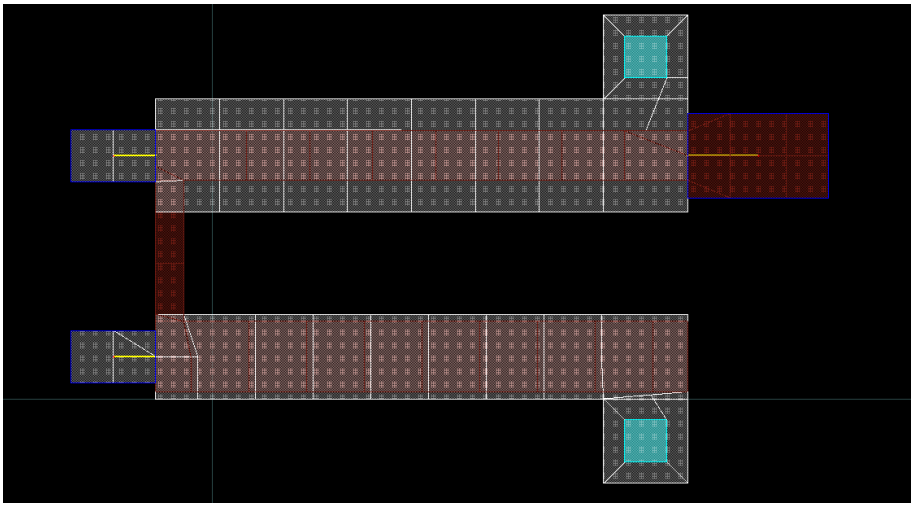

Figure 6.2: 2-D View of the Post-Layout Input Balun

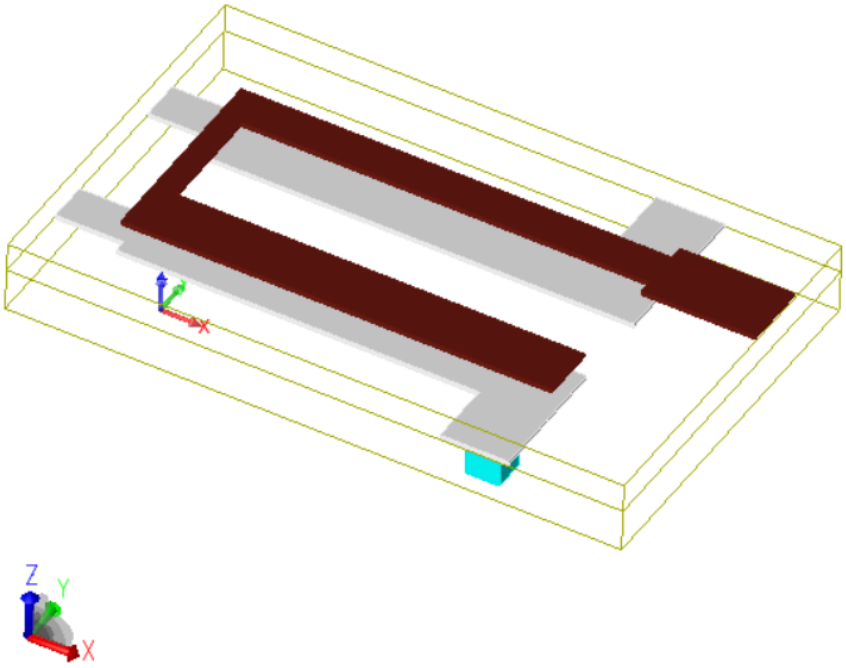

Figure 6.3: 3-D View of the Post-Layout Input Balun

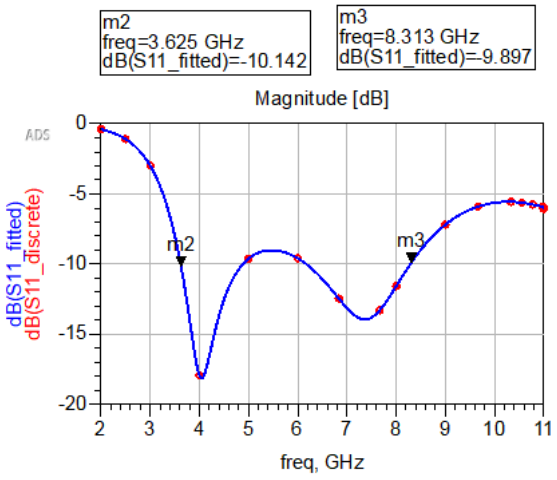

Figure 6.4: $|S_{11}|$ of the Post-Layout Input Balun

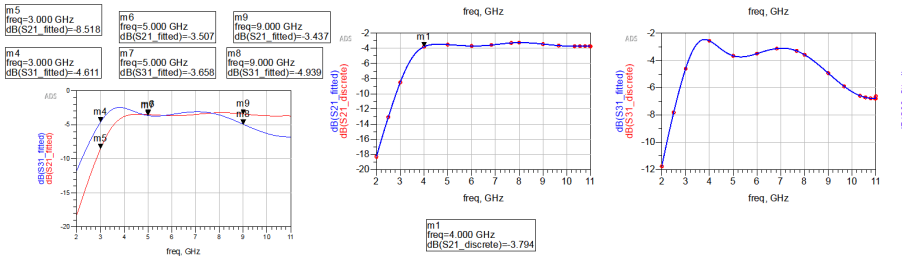

Figure 6.5: Insertion Loss of the Post-Layout Input Balun

Table 6.1: Input Marchand Balun Microstrip T-Line Dimensions

Microstrip Description	**Width** (µm)	**Height** (µm)
Port (2 & 3) (The leftmost two gray pads)	600	370
Port 1 (The rightmost red pad)	1000	600
Port 2 $\lambda/4$ T-Line (Upper gray long T-Line)	3780	800
Port 3 $\lambda/4$ T-Line (Lower gray long T-Line)	3780	600
Port 1 T-Line section that coupled with Port 2 $\lambda/4$ T-Line (Upper red long T-Line)	3780	350
Port 1 T-Line section that coupled with Port 3 $\lambda/4$ T-Line (Lower red long T-Line)	3780	500
Connection between the two $\lambda/4$ T-Lines for forming the single-ended $\lambda/2$ T-Line (Red T-Line between the upper and lower groups)	200	1000
Port 2 & 3 grounding panel (Two gray squares on the right side)	600	600
Port 2 & 3 grounding vias (Two cyan squares)	300	300

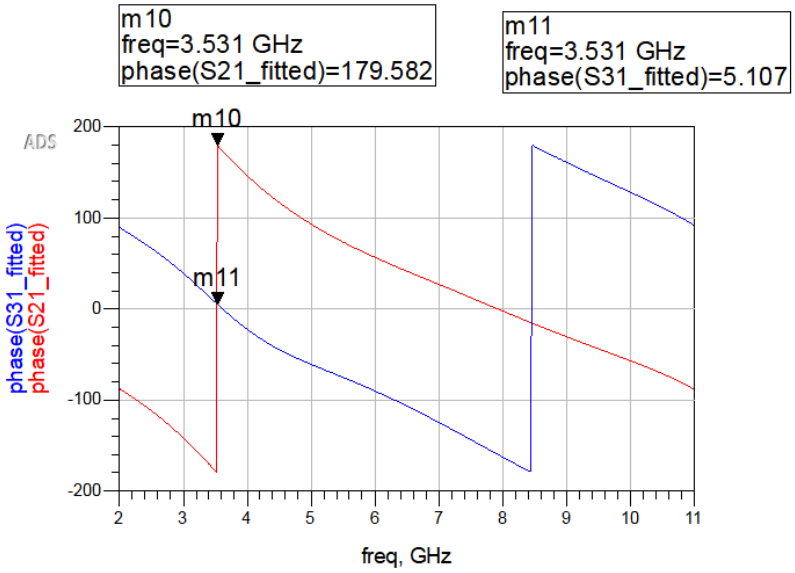

Figure 6.6: Phase Difference Between the Two Paths of the Post-Layout Input Balun

6.1.3 Output Marchand Balun

The setup of the output Marchand Balun was the same as the input balun, with some modifications in parameters for achieving the 100 Ω differential outputs. Similarly, the $|S_{11}|$ (from the single-ended port, which is the output port of the entire PA module), insertion loss, and phase difference were measured (Figure 6.9 to Figure 6.11). The output Marchand Balun provided a $|S_{11}| < -10$ dB bandwidth from 3.6 GHz to 7.6 GHz. The phase difference between the two branches was close to 180°, which proved the functionality of the output Marchand Balun. If we compare both the input and the output baluns to the all-50 Ω design [2], the bandwidth of both the input and the output baluns were less than the all-50 Ω Marchand Balun.

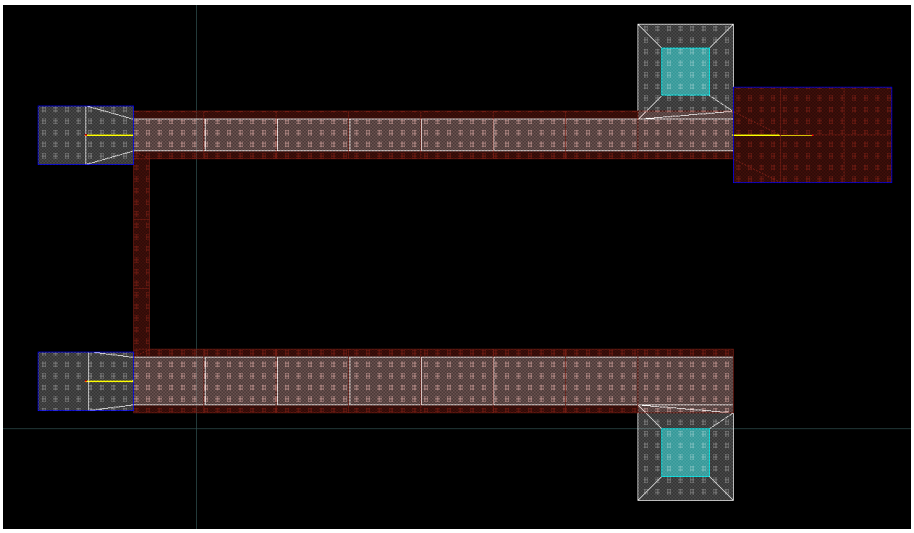

Figure 6.7: 2-D View of the Post-Layout Output Balun

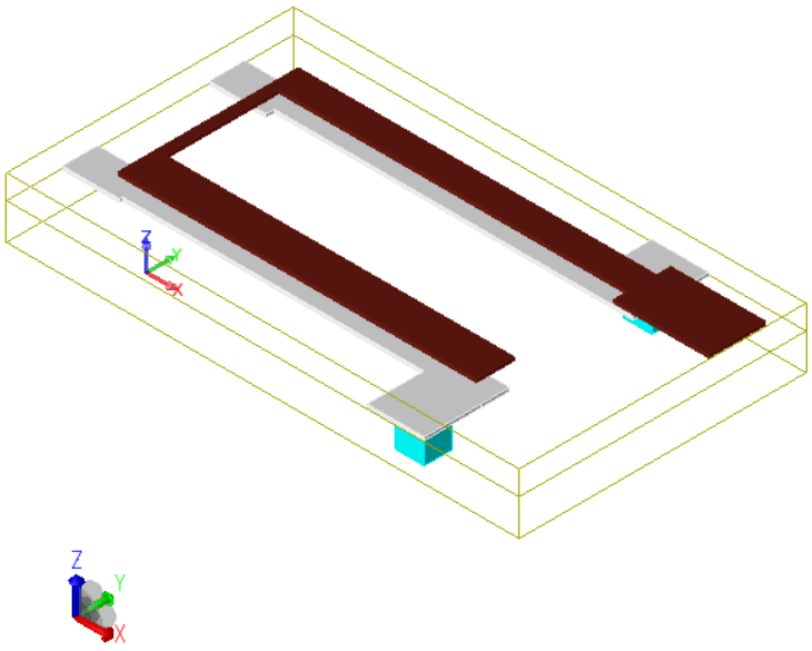

Figure 6.8: 3-D View of the Post-Layout Output Balun

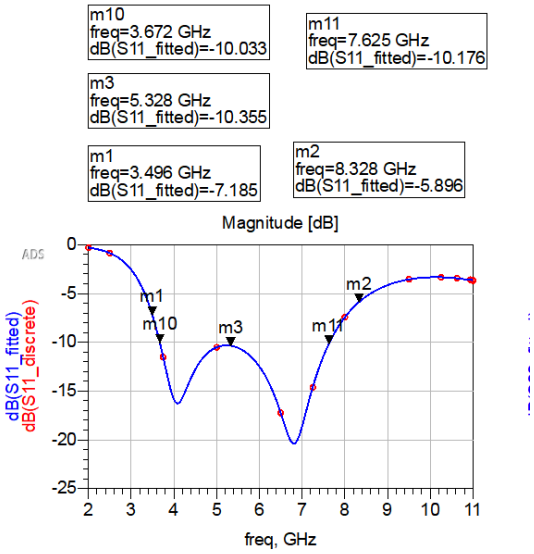

Figure 6.9: $|S_{11}|$ (Single-Ended Port) of the Post-Layout Output Balun

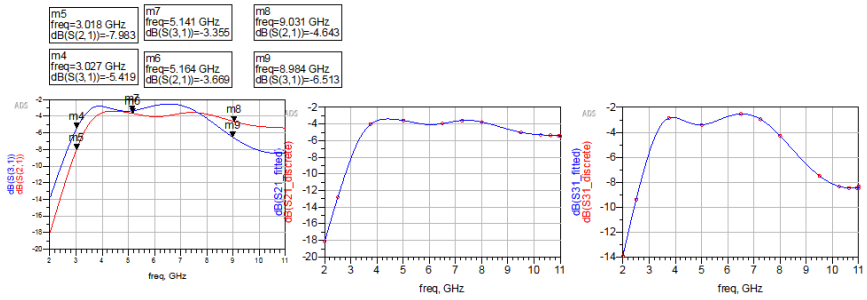

Figure 6.10: Insertion Loss of the Post-Layout Output Balun

Table 6.2: Output Marchand Balun Microstrip T-Line Dimensions

Microstrip Description	**Width** (µm)	**Height** (µm)
Port (2 & 3) (The leftmost two gray pads)	600	370
Port 1 (The rightmost red pad)	1000	600
Port 2 $\lambda/4$ T-Line (Upper grey long T-Line)	3780	200
Port 3 $\lambda/4$ T-Line (Lower grey long T-Line)	3780	300
Port 1 T-Line section that coupled with Port 2 $\lambda/4$ T-Line (Upper red long T-Line)	3780	300
Port 1 T-Line section that coupled with Port 3 $\lambda/4$ T-Line (Lower red long T-Line)	3780	400
Connection between the two $\lambda/4$ T-Lines for forming the single-ended $\lambda/2$ T-Line (Red T-Line between the upper and lower groups)	100	1200
Port 2 & 3 grounding panel (Two gray squares on the right side)	600	600
Port 2 & 3 grounding vias (Two cyan squares)	300	300

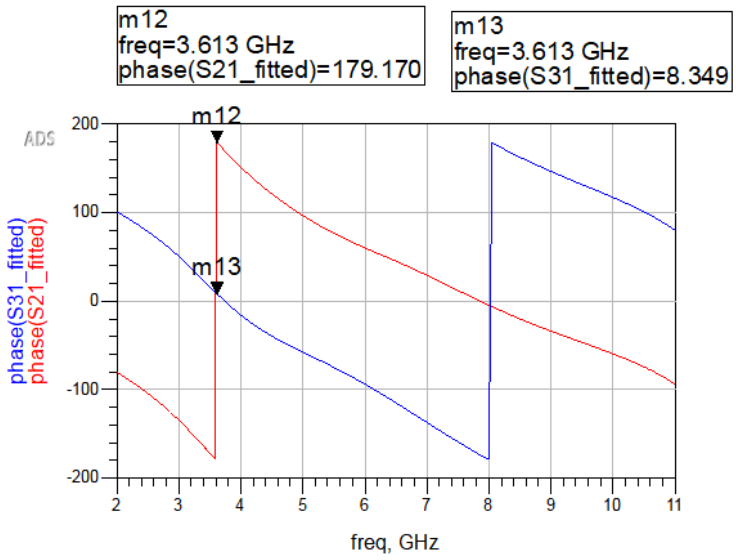

Figure 6.11: Phase Difference Between the Two Paths of the Post-Layout Output Balun

6.2 Layout of the Amplifying Stages with Matching Networks

6.2.1 R-L-C Lumped-Element Input/Output Matching Network

The matching condition might endure significant changes after tape-out for PA designs. For this reason, both the input and output matching networks were based on lumped elements for easier post-tape-out tuning. As for the lumped elements, the author referred to the outcomes after post-layout tuning and chose elements based on those values. The element configurations are included in Table 6.3 and Figure 6.12. The voltage biasing points were not changed in the layout. Note that a small microstrip pad connecting the source of the transistors and the ground panel replaced the degenerative inductor and capacitor in Figure 4.1. The HRL transistor layout replaced the transistor module in the schematics.

Table 6.3: Lumped Element Configurations for the Input and Output Matching Networks of the Amplifying Stages

Element Value for Layout, Serial Number of the Element, and Value in the Pre-Layout Schematic	**Length** (µm)	**Width** (µm)	**Height** (µm)
Capacitor $C_1 = 15\,\text{pF}$ (GJM1555C1H150GB01D) [8] $C_{1,pre} = 25\,\text{pF}$	1000	500	550
Resistor $R_1 = 30\,\Omega$ (SFR01MZPJ300) [9] $R_{1,pre} = 15\,\Omega$	1000	500	350
Capacitor $C_{in} = 20\,\text{pF}$ (GRM1555C1H200GA01) [10] $C_{in,pre} = 5\,\text{pF}$	1000	500	550
Inductor $L_1 = 1.4\,\text{nH}$ (PE-0201CC2N0STT) [11] $L_{1,pre} = 0.7\,\text{nH}$	600	450	450
Inductor $L_2 = 7.6\,\text{nH}$ (BWCS000604047N6J00) [12] $L_{2,pre} = 5\,\text{nH}$	600	400	400
Capacitor $C_{out} = 15\,\text{pF}$ (GJM1555C1H150GB01D) [8] $C_{out,pre} = 15\,\text{pF}$	1000	500	550

6.2.2 Transmission Line Setup

For simplicity of design, the matching network was constructed based on the same substrate as the Marchand Baluns. For the amplifying stages, the inputs were matched to 25 Ω, and the outputs were matched to 100 Ω. The author started by applying 25 Ω T-Lines for the input matching network and 100 Ω T-Lines for the output matching network. This configuration showed a negligible difference compared to an all-50 Ω T-Line configuration for both the input and output matching networks.

As for estimation of transmission line widths and characteristic impedance (Z_0), the equivalent dielectric constant of the two-layer substrate is calculated:

$$\begin{aligned} \varepsilon_{\text{eff}} &= \frac{\varepsilon_{r1} h_1 + \varepsilon_{r2} h_2}{h_1 + h_2} \\ &= \frac{10.2 \times 0.254\,\text{mm} + 9.8 \times 0.381\,\text{mm}}{0.254\,\text{mm} + 0.381\,\text{mm}} \\ &= \frac{(2.5908 + 3.7338)\,\text{mm}}{0.635\,\text{mm}} \\ &\approx 9.95 \end{aligned} \tag{6.1}$$

The equation of T-Line characteristic impedance is given as

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{\text{eff}}}} \left[\frac{W}{h} + 1.393 + 0.667 \ln\left(\frac{W}{h} + 1.444 \right) \right]^{-1} \tag{6.2}$$

where the microstrip thickness is set to 0.035 mm.

By solving the equation for $Z_0 = 25\,\Omega$, $50\,\Omega$, and $100\,\Omega$ respectively, we can get $W = 1.52$ mm for $Z_0 = 25\,\Omega$, $W = 0.42$ mm for $Z_0 = 50\,\Omega$, and $W = 0.12$ mm for $Z_0 = 100\,\Omega$. However, in the actual simulation, the microstrip width did not impact the input and output matching network significantly. Hence, the matching networks were implemented with T-Lines of the same Z_0, with the tuned T-Line dimensions recorded in Table 6.4, Figure 6.13, and Figure 6.14. Spaces for lumped elements

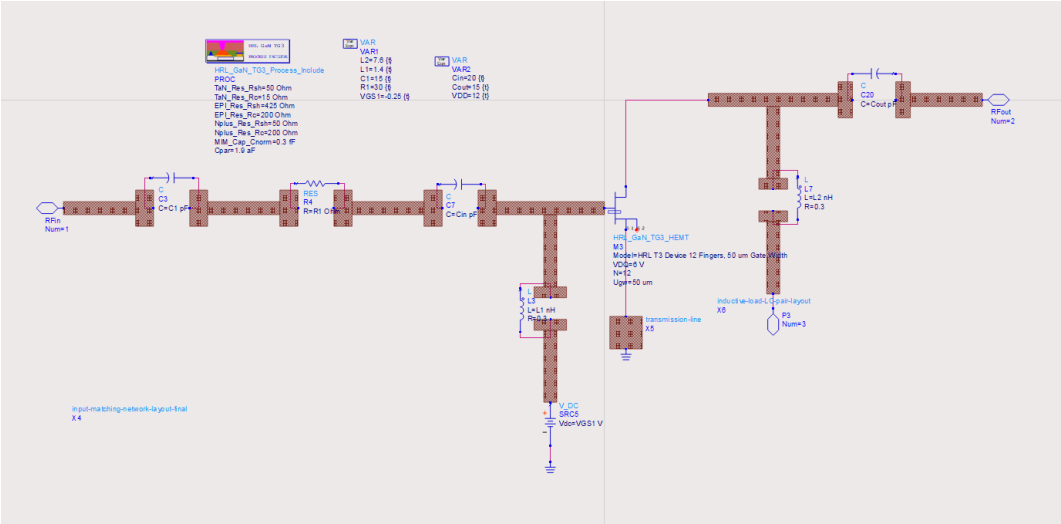

Figure 6.12: Layout of the Amplifying Stages (one Branch is Shown)

were reserved in the layout according to the dimensions specified in Table 6.3. The T-Line widths (lengths of the signal paths) in Table 6.4 were set to those values to avoid distributed parameter effects (ensuring short electrical lengths).

Table 6.4: Microstrip Dimensions of the Amplifying Stage Matching Networks

Microstrip Description Figure 6.13 & 6.14	**Width** (µm)	**Height** (µm)
Group 1	1000	180
Group 2	1500	180
Group 3	1800	180
Grounding Pad for Transistors	400	400

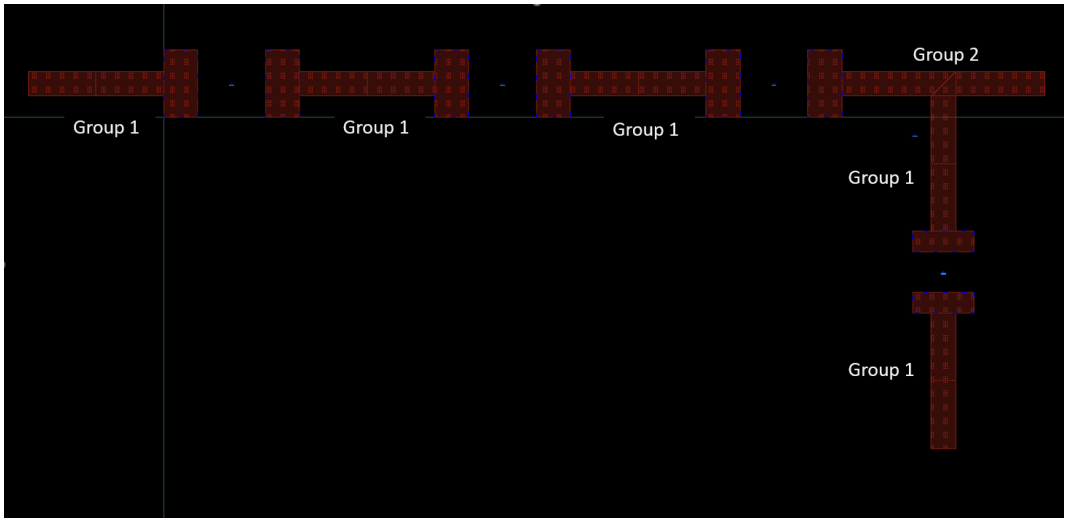

Figure 6.13: Layout of the Input Matching Network of the Amplifying Stages

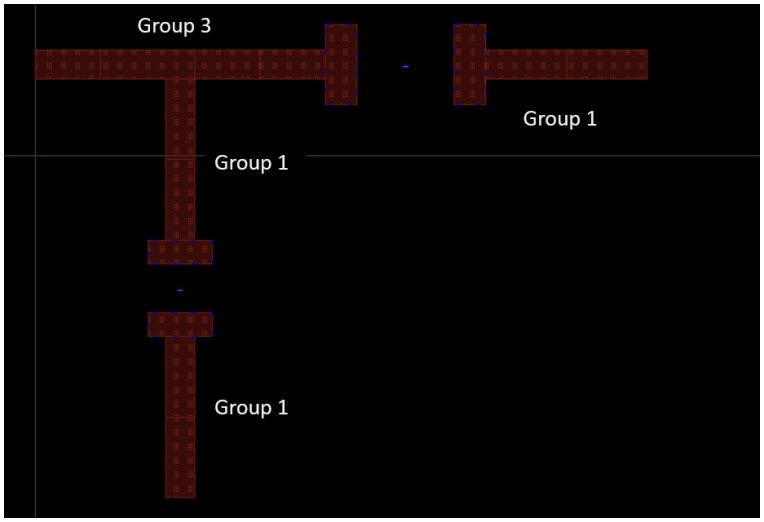

Figure 6.14: Layout of the Output Matching Network of the Amplifying Stages

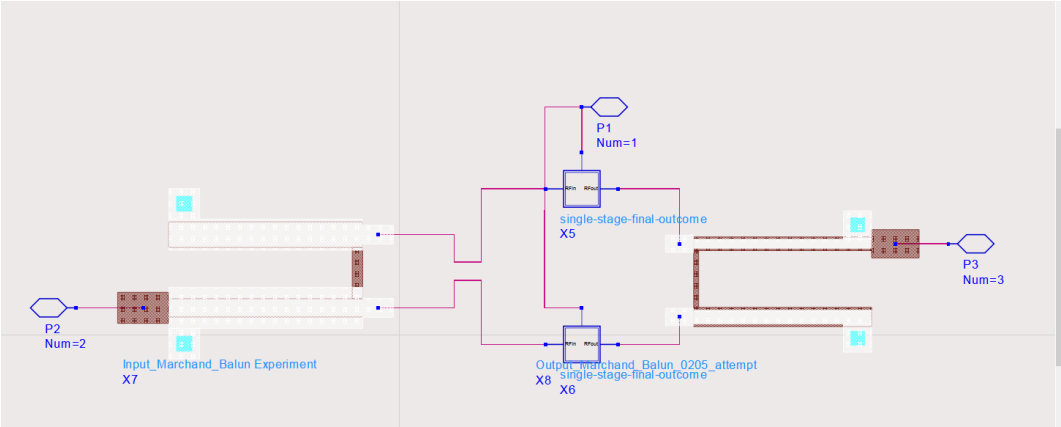

Figure 6.15: Schematic of the Post-Layout Marchand Balun and Assembled PA

6.3 Post-Layout Simulations of the PA

By replacing the ideal Marchand Baluns with the post-layout ones, the PA module became the schematic shown in Figure 6.15, where the two boxes in the center are the symbols of the two post-layout amplifying stages (refer to Figure 6.12). The same test in Chapter 5 was performed on the post-layout PA.

6.3.1 S-Parameters and Stability

The stability of the post-layout PA followed a similar pattern to that of the pre-layout one. The power amplifier was stable from 0 to 30 GHz. The input matching had $|S_{11}| < -10\,\text{dB}$ for most frequencies above 4 GHz, which was less desirable compared to the pre-layout case. Overall, the S-parameters graphs demonstrated the same pattern as the pre-layout counterparts.

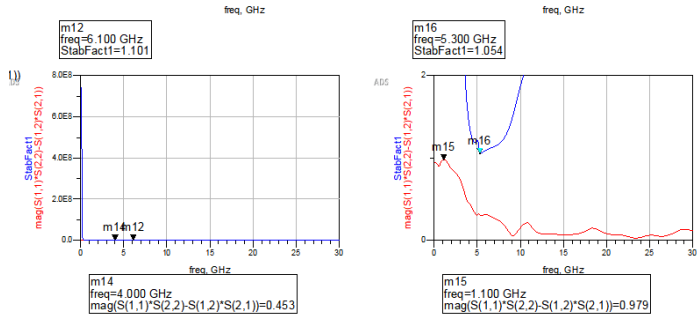

Figure 6.16: Stability Factor and Δ Factor Performance of the Post-Layout PA from 0 to 30 GHz

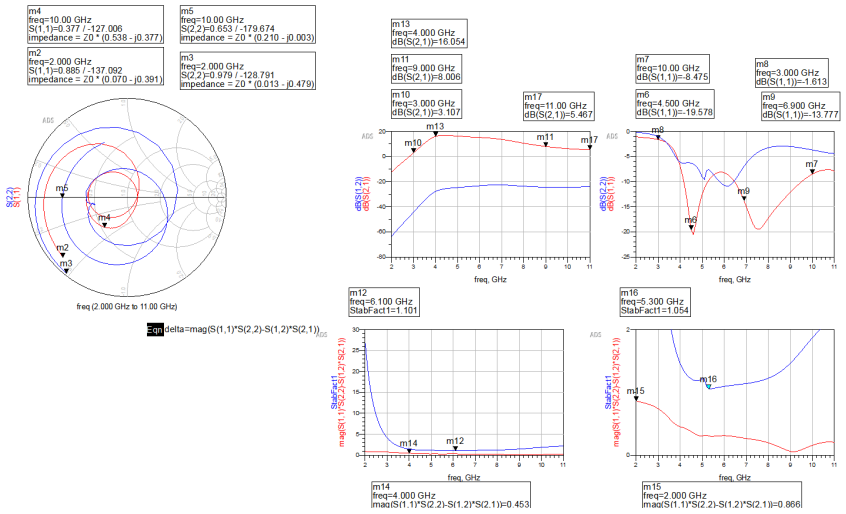

Figure 6.17: S-parameters, Stability Factor, and Δ Factor Performance of the Post-Layout PA from 2 to 11 GHz

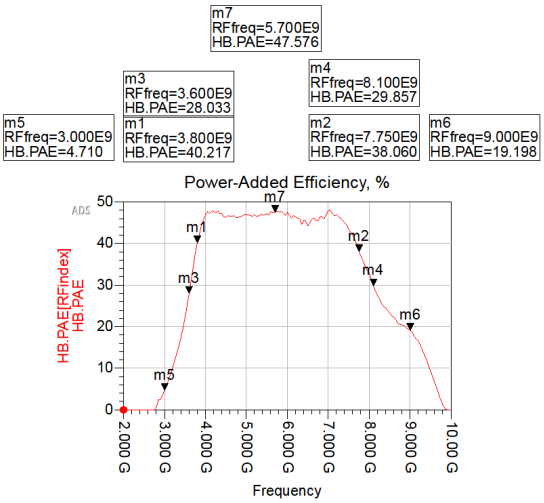

Figure 6.18: Results for Gain and PAE vs. Frequency Test of the Post-Layout PA, with $P_{in} = 23$ dBm and Markings for PAE Values

6.3.2 Harmonic Balance Analysis

Compared with the results in Figure 5.5 and Figure 5.9, the peak PAE in Figure 6.18 dropped about 2% due to the loss in layout. The main difference was the high-PAE operating bandwidth: the post-layout Marchand Baluns could not support the same bandwidth as the ideal models, causing a narrower band that could operate with high PAE. Despite this drawback, the PAE surpassed 40% from 3.8 GHz to 7.7 GHz and remained above 30% from 3.6 GHz to 8.1 GHz. The gain of the PA dropped by 2 dB (from 10 dB to 8 dB) compared to the pre-layout gain. In the input power sweep simulation with $f_{in} = 5$ GHz, the output and input signals were distorted more than the tests with ideal baluns (Figure 6.19).

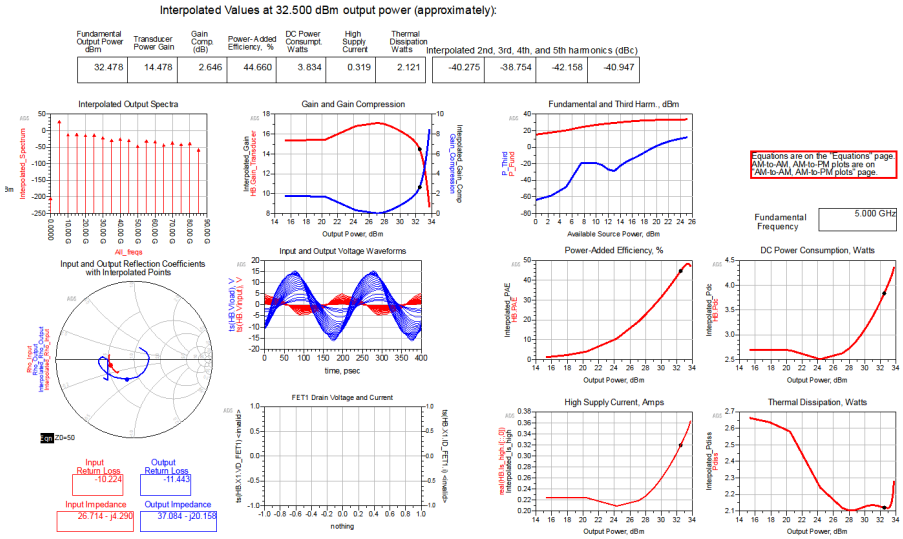

Figure 6.19: Result for Gain and PAE vs. Input Power Test of the Post-Layout PA, with $f_{in} = 5\,GHz$

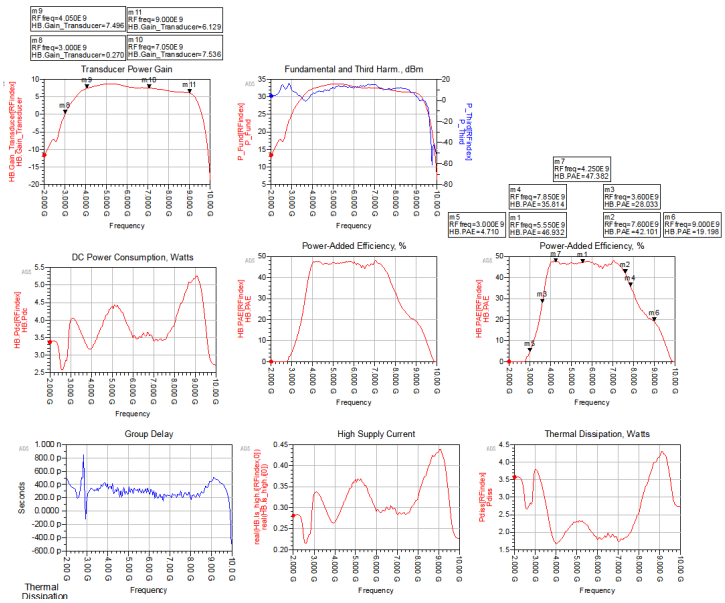

Figure 6.20: Result for Gain and PAE vs. Frequency Test of the Post-Layout PA, with $P_{in} = 23\,\text{dBm}$

CHAPTER 7

Conclusion and Further Development

In this thesis, the author took a complete path of designing an ultra-wideband power amplifier with the help of gallium nitride HEMTs. The design outcome was less desirable than the original objective. If there is an opportunity for further study, the power amplifier can be improved in the following three aspects:

a) better input and output Marchand Baluns, enabling wider bandwidth with better insertion loss and input return loss performance.

b) improve the design of the input matching network; however, this will not impact large-signal performance as significantly as the previous proposal.

c) choosing a higher voltage supply environment for higher efficiency and high power output range that works better with GaN transistors.

Again, I would like to express my deepest gratitude to Prof. Yuanxun Wang for his unwavering guidance, insightful feedback, and patient mentorship throughout this research journey. I would also like to appreciate the assistance from my colleagues at the Digital Microwave Lab (DMLab) at the University of California, Los Angeles. Their expertise and encouragement were instrumental in shaping both this work and my growth as a researcher.

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