UNIVERSITY OF CALIFORNIA

SANTA CRUZ

HIGH-DENSITY WIRELESS NEURAL RECORDING SYSTEM

A dissertation submitted in partial satisfaction
of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

by

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June 2013

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Abstract

High-Density Wireless Neural Recording IC

by

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This thesis focuses on integrated and miniaturized wireless neural recording systems for bio-instruments for the in-depth understanding on animal behavior, human brain activities, and complex neuroprosthetic devices to treat various neurological diseases. The interdisciplinary nature of the system requires a wide range of knowledge in biology and electronics to build such systems. A unique environment where the system should operate imposes challenging design constraints and system-level issues, which can be solved only by considering both biology and electronics. Fundamental building circuits including amplifiers, filters, analog-to-digital converters (ADCs) are addressed first. Then sub-systems, which consist of those basic circuits, are analyzed with an emphasis on trade-offs, which should be carefully considered to achieve optimal design. Specifically, an ultra wideband communication system for biomedical applications is proposed to overcome the limitation of the data bandwidth and power consumption existing in current conventional systems. Several ICs are designed and fabricated in 0.35μm CMOS process to verify the proposed concepts and ideas. Prototype systems are

implemented using those fabricated chips, and their test results from the bench top and in animal implantation are presented.

Acknowledgements

First of all, I thank my Lord in Heaven for helping me and allowing me to write this thesis.

I thank my advisor Prof. Sung Mo Kang for his invaluable guidance and supporting during the course of my thesis. With his help and encouragement, I was able to complete this work.

I would like to thank Dr. Mehmet R. Yuce for his assistance through various technical discussions, information, and collaborations. I would also like to thank Prof. Kenneth Pedrotti and Associate Prof. Matthew Guthaus for spending time on serving my thesis committee.

Colleagues were very helpful and make my stay here rewarding. I would like to thank them all, especially Eric Basham for the snail dissection and setting up ex-vivo recording, and Linh Hoang for CAD tool support.

My family's constant support and encouragement helped me identify and pursue opportunities in research and higher education. I deeply thank my wife Jung Eun for her love and support in my life.

Chapter 1

Introduction

Since Hodgkin and Huxley's pioneering work on the analysis of the action potential [1], an enormous amount of knowledge about the structure and functions of the nervous system has been accumulated. Extensive understanding of the neural activities at the cellular level has been achieved through the techniques of extracellular recording and stimulation, and there are many ongoing studies about the behavior of a large network of neurons, which will eventually lead to the thorough understanding of human behavior. Neuroscientists have been using neural recording systems for those kinds of studies in their experiments both *in vivo* and *in vitro*.

With the emergence of several technical innovations in microelectronics, researchers began to try to use established techniques and knowledge to treat nerve-system-related diseases and to help disabled people. The remarkable success of cochlear implants for the deaf and deep brain stimulation (DBS) for Parkinson's disease revealed the possibility that implantable neuroprosthetic devices can be an efficient and practical method to treat neurological diseases and disabilities related to the nerve-system. Retinal prostheses for the blind [2], [3], brain-machine interface for those with spinal cord injuries [4] - [6], epilepsy suppression [7], and more advanced cochlear implants [8], and DBS of the subthalamic nucleus for Parkinson's disease [9] are actively under development and garnering more interest and support. As the range of applications is growing and the functionality is becoming more complex and

sophisticated, neuroprosthetic devices are gradually evolving to a closed-loop controlled system, which is composed of three main functional blocks of neural recording, neural signal processing, and neuromuscular stimulation. The bio-signals monitored by the recording blocks are processed to generate a command signal to stimulate a particular neuron or muscle to evoke expected results in the biological objects. Those recording and stimulation processes are analogous to the read and write functions of the computer systems. Therefore, the neural recording system is not only the basic tool to understand the neural activities, but also the key component to determine the overall performance of the entire neuroprosthetic devices.

1.1 Design Considerations

Modern neural recording systems for advanced neuroprosthetic devices and research on neuroscience are facing challenging requirements and constraints on the electronics design. An increasing number of recording channels are required to improve the performance of the neuroprosthetic devices and to facilitate the study of complex brain activities in the field of neuroscience. However, the mobile nature of the applications forces the entire system to operate on a very limited power budget. Most available power sources for this specific kind of system unfortunately do not have sufficient capacity. Moreover, the implanted devices should not consume too much power even when it operates on a reliable power source because of the possible heat damage to the tissue surrounding the device. Therefore, low power operation is inevitable. In addition, the space available to host the system in the biological object is usually very small and restricted. Therefore, it is necessary to integrate as many

components as possible on a single chip to miniaturize the system. However, as the number of channels and the complexity of the system increase, the power consumption and size of the entire system increase as well, which is against the constraint set by the applications. These issues make it very challenging to design the system, which demands a systematic approach in the early design stages. Wireless capability is another critical issue. Power and data need to be transmitted to the implanted system, which is inside the body of animals or patients. Wired connections have a critical infection problem, and they seriously hinder the free movement of the objects. Thus, wireless telemetries are essential for the design of systems targeted for actively moving biological objects. Wide bandwidth data telemetry is on special demand as the number of channels increases. Flexibility of the system is also critical because the properties of the bio-signals have a wide range of variations from one object to another and even severely change in the same object over time. Therefore, flexibility to change critical system parameters, such as gain and bandwidth of the amplifiers, is needed to maintain a good system performance.

1.2 Overview

Various design issues mentioned above will be discussed in more detail and will be followed by a design to overcome those challenges. The rest of the thesis is organized as follows.

Chapter 2: Review of Neural Recording Systems presents a review of neural recording, including the design of the basic circuits frequently used in neural

recording systems, such as preamplifiers, filters, and analog-to-digital converts (ADCs).

Chapter 3: Basic Building Block Design describes the proposed basic circuit blocks for the integrated neural recording systems. This chapter explains the design of a full-differential self-biased preamplifier, a passive RC-filter with Miller capacitance technique, and a fully-differential SAR ADC in detail.

Chapter 4: Subsystem Design explains how to assemble the basic building blocks to form sub-systems, which have specific purposes of recording, stimulation, and wireless transmitting of power and data. Emphasis is placed on the trade-offs between various design parameters to achieve optimal solutions.

Chapter 5: High-density Neural Recording IC discusses the design of a 128-channel wireless neural recording system composed of sub-circuit blocks explained in Chapter 3 and 4.

Chapter 6: Chip Test Results presents the test results of various prototype chips fabricated in 0.35μm CMOS process. The first chip is a 4-channel analog front-end chip that verifies the proposed concepts and ideas of fully-differential self-biased amplifier and passive RC filter with Miller technique. The second chip is a 16-channel neural recording IC. The chip was designed by using the proposed optimization method explained in Chapter 4. The third chip is a UWB Tx chip, and the last one is a 128-channel wireless neural recording IC. For each prototype chip, bench-top test results are provided along with a few animal test results.

Chapter 7: Conclusions, which briefly summarize this thesis work.

Chapter 2

Review of Neural Recording Systems

2.1 Mechanisms of Neural Recording

Fig. 2.1 is a simplified illustration of the extracellular action potential. When a neuron fires an action potential, different parts of the cell membrane become depolarized by the opening of voltage-controlled ion channels leading to flows of ion currents both inside and outside of the neuron. As the surrounding body fluid is conducting media, a time-varying potential field is generated around the neurons. As extracellular media is resistive, the extracellular potential is approximately proportional to the current across the neuron membrane. The membrane behaves like an RC circuit, and most of the current flows through the membrane capacitance. Fig. 2.2 shows a simplified circuit model for the neural recording environment. The recording electrode is modeled as a parallel RC circuit, where R represents the Faradaic resistance and C models the double-layer capacitance.

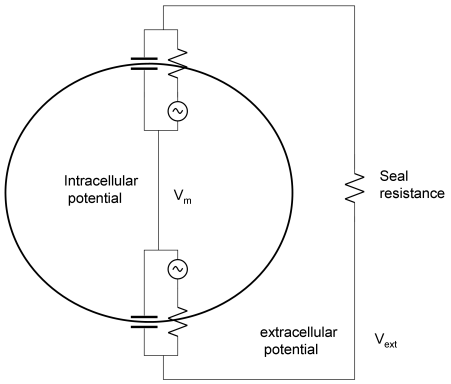

Fig. 2.1. A simplified circuit model of extracellular action potentials.

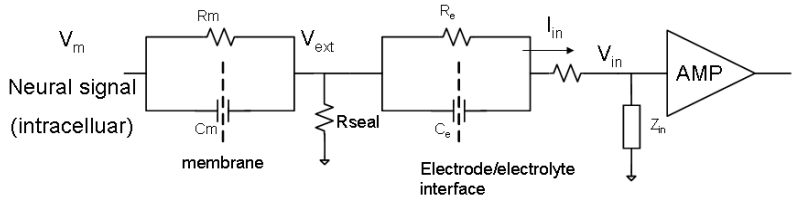

Fig. 2.2. A simplified circuit model for the neural recording environment.

2.2 Neural Interface Circuits

Neural interface circuits are the basic building blocks of the neural recording systems. They include low-noise preamplifiers to amplify the weak bio-signals, analog filters to maximize the signal-to-noise ratio (SNR) of the amplified signal, and analog-to-digital converters (ADC) to digitize the signal for further processing in digital domain.

2.2.1 Low-noise Preamplifiers

The signals generated by neurons are very small in amplitude and very noisy. For example, the amplitude of the extracellular action potentials induced at the recording microelectrode in general is no more than a few hundred μV. One of the major noise sources in the neural recording is the microelectrode itself. The noise contributed by the electrode is given by the well-known Nyquist's formula, and its value is typically tens of μV when the recording bandwidth is set to 10 KHz [10]. In addition, the biological background noise, which has various origins, degrades the signal quality significantly. Local field potentials (LFPs) and other far-field signals tend to have larger signal amplitudes than that of the extracellular action potential. Therefore, at the first stage of the recording systems, a low-noise preamplifier is

required to amplify the small potential difference between the recording electrode and reference electrode.

The different neural signals have different signal amplitude and bandwidth. Their typical values are presented in the Table 2.1. The amplifier's gain should be sufficiently large to ensure proper processing of the signal at later stages of the system. In addition, the bandwidth of the amplifier, mostly determined by the high frequency cut-off of the amplifier, needs to match that of the target signal such that the signal-to-noise ratio (SNR) is maximized. The low-frequency cut-off of the amplifier also has to be sufficiently low to guarantee that the low-frequency content of the bio-potentials is not lost. For example, to properly record the extracellular action potentials from neurons, a total signal gain of more than 1000 is necessary to achieve 100mV signal, and the high-frequency cut-off of the amplifier needs to be set to 10 KHz, while the low-frequency cut-off should be smaller than 200Hz.

Table 2.1. Amplitude and bandwidth of various bio-potentials.

Signal	**Bandwidth (Hz)**	**Signal Range (mV_{pp})**
ECG	0.05 ~ 256	0.1 ~ 10
EEG	0.05 ~ 128	0.02 ~ 0.4
ECoG	0.1 ~ 64	0.02 ~ 1
EMG-1	1 ~ 1K	0.02 ~ 1
EMG-2	1 ~ 128	0.02 ~ 1

LFPs	0.1 ~ 100	0.1 ~ 1
EAPs	100 ~ 10K	0.04 ~ 0.2

Usually, there is a large DC offset voltage at the electrode– electrolyte interface [11]. This DC offset voltage is called the half-cell potential and has a critical effect on the bio-potential amplifier design. Since the half-cell potential typically has an amplitude of more than a few hundred mV, the amplifier output would be saturated if these large DC offset voltages are not considered during the amplifier design. These unique constraints on both the DC offset and the low frequency nature of the signal make the bio-potential amplifier design distinct from other types of amplifier designs.

Input impedance is also important and should be considered with care at the design stages. The extracellular action potential is sensed by the electrode and amplified by the neural amplifier. The actual input voltage of the amplifier is determined by the impedance ratio of the electrode and amplifier's input impedance. The impedance of the recording electrode varies according to the geometry and material. For micro-electrode arrays, which are widely used in multi-channel recordings, the impedance could be as high as 1MΩ at 1 KHz. Therefore, to minimize the signal loss, the input impedance of the amplifier needs to be at least a few MΩ at 1 KHz.

Noise is another critical concern in the recording system design. There are three major noise sources that affect the signal quality in neural recording: biological

noise, electrode noise, and electronic noise. Among them, the biological background noise has the largest contribution. The amplifier should be designed so that the input equivalent noise is smaller than that of the electrode and biological background noises.

2.1.1.1. Negative feedback amplifier

A capacitively-coupled negative feedback amplifier [12], [13] is widely used in the neural recording systems, and its circuit is shown in Fig. 2.3 [13]. It consists of an operational transconductance amplifier (OTA) as an amplification component, capacitors to form a feedback network, and biasing resistors. It has the advantage of automatically rejecting DC offset voltages by the input capacitance C_1, and this feature makes it suitable for neural recording applications [12], [13], [14]. The selected value of C_1 should be such that the input impedance of the amplifier is sufficiently large compared to the electrode impedance. As the input node of the OTA is virtually AC ground when both $C_L \gg C_2$ and $g_m/2\pi f_s C_L \gg 1$ are satisfied (f_s is the signal bandwidth), where the OTA can reasonably be regarded as an operational amplifiers, the differential input impedance of the amplifier is simply $(j2\pi fC_1)^{-1}$. C_1 should be chosen carefully according to the target signal because the different neural signals have different signal bandwidths and the impedance of the electrode is frequency-dependent. For instance, in the extracellular action potential recording, C_1 should be less than 16 pF to make the input impedance larger than 10 MΩ at 1 KHz, because most of the signal energy is concentrated around 1 KHz and the impedance of the microelectrode ranges from several hundred KΩ to a few MΩ at 1 KHz.

The biasing resistor R_B serves two purposes. First, it sets a proper DC bias voltage at the input node of the OTA. The bias voltages are usually set to the midway voltage between V_{dd} and V_{ss}, which is equivalent to the circuit ground in case a dual power supply level is used. Second, it determines the low-frequency cut-off of the amplifier by forming a high pass filter with the input capacitor C_1. Therefore, the cut-off frequency of the filter is $(2\pi R_B C_1)^{-1}$, and to achieve the cut-off frequency of less than 1Hz, R_B should have a resistance of several GΩ. It is challenging to implement on-chip resistors with such a high impedance. Several methods have been proposed including diode-connected MOS transistors [12], MOS-bipolar devices acting as pseudo resistors [13], and MOS transistors biased in a sub-threshold region [14].

When the condition $C_L \gg C_2$ is met, most output current of the OTA flows through C_L. Therefore, the output voltage V_{out} can be described as follows.

$$V_{out} = -g_m V_X \cdot \frac{1}{j\omega C_L} . \tag{2.1}$$

Also, we can assume that the input impedance of the OTA is large enough so that the follow equation is valid.

$$C_1(V_{in} - V_X) = C_2(V_X - V_{OUT}) . \tag{2.2}$$

By (2.1) and (2.2), the gain of the amplifier can be calculated as below.

$$A(\omega) = \frac{V_{out}}{V_{in}} = \frac{C_1/C_2}{1 + j\omega \dfrac{(C_1/C_2)C_L}{g_m}} . \tag{2.3}$$

From (2.3), we can determine the amplifier's mid-band gain A_M and high frequency cut-off ω_{HF} as C_1/C_2 and $g_m(A_M C_L)^{-1}$, respectively.

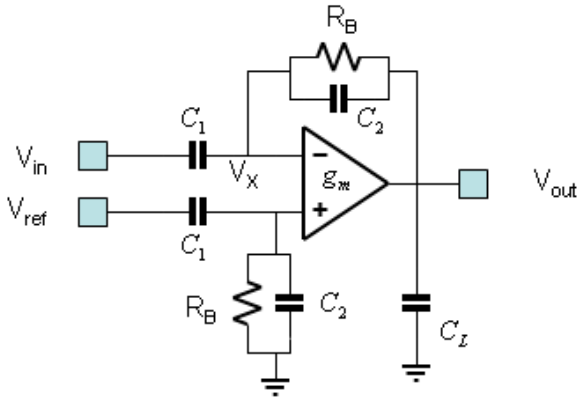

Fig. 2.3. A negative capacitive feedback amplifier.

OTA has critical effects on the overall performance of the amplifier, such as input equivalent noise, offset voltages, and common mode rejection ratio (CMRR). A current-mirror OTA with cascade output stage [13] is commonly used in conventional designs.

The chosen width and length of the input transistors should be large enough to make the 1/f noise as small as possible. Subthreshold design is often employed for a low-power operation [13]. However, the subthreshold design requires very careful simulations and layout techniques due to large process variations and poor matching between critical devices.

2.1.1.2 Chopper amplifier

Several researchers have proposed using chopper-modulated amplifiers for biomedical applications [15], [16] because of their ability to suppress low-frequency noise such as 1/f noise and DC offset voltages. This technique is especially useful for the amplification of the far-field signal, the frequency of which is so low that the

major noise source to affect the signal is 1/f noise rather than thermal noise. The fundamental idea of the chopper amplifier is to shift the original signal to a higher frequency band and perform the amplification at that frequency band where the noise and offset of the amplifier does not exist. The block diagram in Fig. 2.4 explains the concept and operation of the chopper amplifier. The incoming neural signal is first chopper-modulated so that the signal spectrum is shifted to a higher frequency band. After modulation, an amplifier provides the required signal gain by adding the amplifier's intrinsic noise. It should be noted that the noise added by the amplifier is not chopper-modulated with the neural signal. A high-pass filter then removes the low-frequency noise added by the amplifier, and then the filtered signal is shifted back to the original signal band by the chopper demodulation followed by a low-pass filter. Therefore, the 1/f noise added by the amplifier is effectively removed, making it possible to achieve an extremely low input equivalent noise of the amplifier. The chopper amplifier is inherently a DC-coupled amplifier, and as a consequence, there is no need for DC blocking capacitors at the input. The major disadvantage of the chopper amplifier is the clock noise, which can affect the weak neural signal unless extensive care is taken at the design stage. In addition, the switch for the chopper modulation can add its intrinsic noise to the neural signal, making the signal noise of the original signal worse unless designed appropriately.

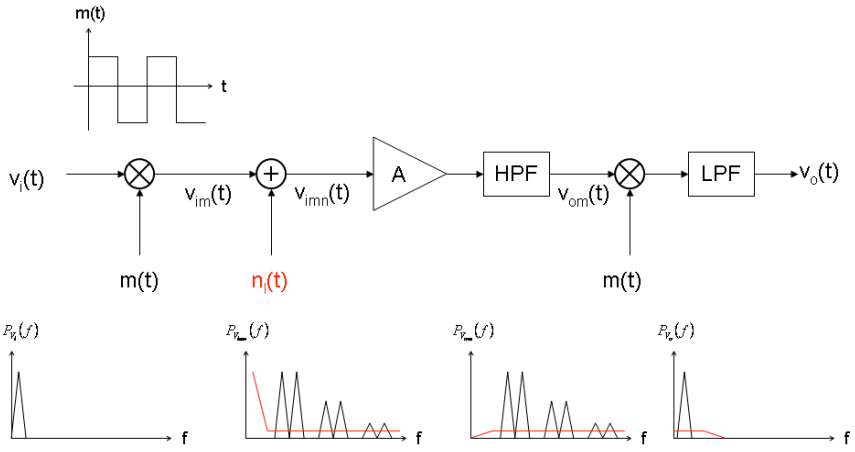

Fig. 2.4. Block diagram of a basic chopper amplifier.

2.2.2 Filters

Although the amplifiers can serve as a 1st-order low pass filter, it is usually not sufficient to obtain a reasonably good signal-to-noise ratio due to the extremely weak power of the neural signal. In poor recording environments, the amplitude of the extracellular action potential could be as low as 50μV. In addition, reducing the noise power is always preferred so that a larger number of neurons around the recording electrode can be monitored with the same number of recording electrodes. Therefore, most neural recording systems employ separate band-pass or low-pass filters following the preamplifiers.

Those filters should have an appropriate cut-off frequency and order to maximize the signal-to-noise ratio. In most cases, a 1st-order filter is used, resulting in 2nd-order overall filtering when combined with the amplifier. For extracellular action potential recording, the cut-off frequency of 10 KHz is typical, and this frequency

should be lowered even more for other far-field signals, such as LFPs or EEG. Such low cut-off frequencies required for proper system operation impose challenging IC design issues.

2.2.2.1. Passive R-C filter

The most straightforward choice for the implementation of low-order filters such as 1st-order low-pass filters is the passive R-C filters. The passive L-C filters are rarely used because the inductance for the required cut-off frequency is too large to be integrated on a chip. For example, to achieve the 10 KHz cut-off frequency with a 100pF on-chip capacitor, an on-chip inductor of 2.5H is required, which is impossible to implement on a chip. Passive filters have the advantage of not consuming any static power compared to other types of the filters, but they require large areas even with R-C combinations. This limitation becomes more imposing as the number of recording channels increases.

2.2.2.2. Active filter

Active filters are widely used for the implementation of high-order filters. A high complexity 4th-order band-pass filter tuned for a one-octave passband of 20-40Hz [17] was demonstrated using OTAs and capacitors. A technique of stagger tuning, where two second-order band-pass filters are cascaded and tuned to slightly different frequencies, resulted in a wider and flatter pass band than those of individual filters. All the transistors were operated in the subthreshold region to save power consumption in the active circuits. The large resistors were realized by the OTAs with a very small transconductance. When a test voltage source V_{test} is applied between

two ports of the circuit in Fig. 2.5, the current is determined by the transconductance of the OTA. Therefore, the equivalent resistance between two ports is given below as:

$$R = \frac{V_{test}}{I_{test}} = \frac{1}{g_m} . \tag{2.4}$$

As shown in (2.4), a large resistance can be achieved by reducing the transconductance of the OTA.

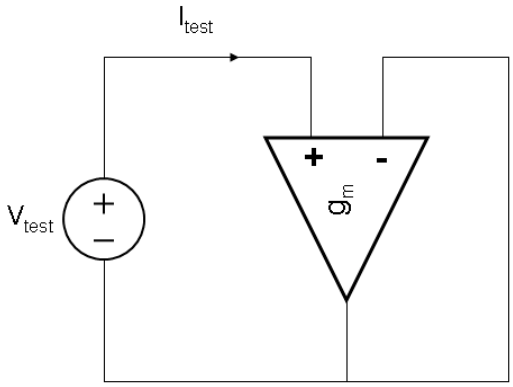

Fig. 2.5. A large resistor realized by an OTA.

2.2.2.3. Switched capacitor filter

In the switched capacitor filter, resistors are realized with switched capacitors. The circuit in Fig. 2.6 shows how the switched capacitors can be used to replace resistors. Here, a capacitor is connected to two switches and two different voltage sources. When S_1 closes with S_2 open, and then S_2 closes with S_1 open, the amount of charge transferred from V_1 to V_2 is as below.

$$\Delta q = C \cdot (V_1 - V_2) . \tag{2.5}$$

If the switching frequency of each switch is f_S, then the total amount of transferred charge per second, the current from V_1 to V_2, can be written as below.

$$i_S = C \cdot (V_1 - V_2) \cdot f_S = \frac{(V_1 - V_2)}{(C \cdot f_S)^{-1}} . \quad (2.6)$$

The above equation (2.6) states that the switched capacitor is equivalent to a resistor whose resistance is $(Cf_S)^{-1}$. Therefore, by lowering the switching frequency f_S, it is possible to achieve a very large resistance. A major advantage of the switched capacitor is that its value can be precisely controlled by adjusting the switching frequency, making it less susceptible to process variations compared to other types of resistors available in integrated circuits. However, great care must be taken at the design stage to minimize the charge injection noise and the switching noise, such as the clock feed through [18].

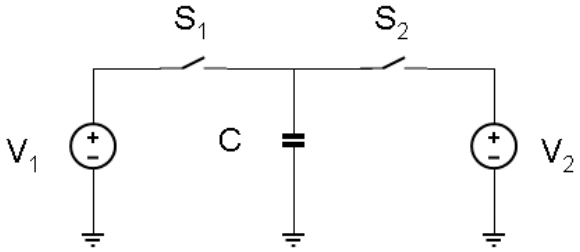

Fig. 2.6. A switched capacitor.

2.2.3 Analog-to-Digital Converters

Analog-to-digital converter (ADC) is an electronic circuit that converts analog signals into digital signals. This converting process is often called digitization. The purpose of digitization of the signals in neural recording applications is to facilitate

the complex signal processing, such as the spike sorting, by taking advantage of the powerful digital signal processing technique. Analog signal processing techniques can also be used. However, it is more reliable and efficient to perform the signal processing in the digital domain than in the analog domain. Also, a digital signal is preferred in view of wireless communication. Therefore, ADCs play a critical role in the implementation of the integrated neural recording system.

ADC has a lot of specifications and design parameters, but among them, the resolution and the sampling rate are the two most important parameters that affect the overall signal processing at later stages of the system. Those two parameters not only affect the signal processing results, but also have a significant impact on the system performance in terms of power consumption and chip area. These aspects will be discussed in detail in Chapter 4.

2.3 Neural Recording Systems and Issues

A multi-channel neural recording system is used in neuroscience experiments to study complex neural networks of animals in their natural environments [19]. However, many of the basic neuroscience questions remain unresolved due to a lack of ability to simultaneously interface with a large population of neurons in awake, unrestrained behaving animals in a long-term setting. Such a technology would help explore and reveal the mechanisms of short-term and long-term memory formation and retention, the substrate of consciousness, sensorimotor integration, and cortical plasticity.

The neural recording system is also a critical component in the brain-computer interface system used for cortical-controlled neural prosthetics. The cortical-controlled neural prosthetics have a wide range of applications, such as upper and lower limb prostheses [5], [6], [20], [21], bladder and bowel movement control for spinal cord injury (SCI) patients [22], [23], respiration control for SCI patients [24], and hand-grasping function restoration [25].

To support these applications, a neural recording system has to meet the challenging requirements imposed by the environment. First, it must record a large number of channels simultaneously; and high-resolution recording can advance fundamental neuroscience studies and has the potential to improve the performance of neural prosthetic devices. Second, a wireless telemetry that transmits recorded neural data is preferable because tethering wires imposes significant restrictions on the subjects and inhibits free movement in their natural environment. Third, on-the-fly processing of neural data is necessary to enable prosthetic devices to function in real-time. In addition, a fast processing capability removes the necessity of storing the large amount of raw data. Fourth, the specifications of the recording system should be designed with programmability and versatility that accommodate a wide range of bio-potentials in different applications. Finally, the power consumption and the chip area have to be minimized due to the limited space available at the recording site, and the system should be powered wirelessly or operated on a rechargeable battery.

Several neural recording ICs previously reported in literature can support simultaneous multi-channel recording [26], [27], [28], wireless data telemetry (spike

information for 100 channels and raw data for one channel) [29], [30], and on-chip spike detection [29], [31], [30], [32]. However, one of the major limitations of the previous systems is that they only allow a subset of electrodes to be recorded simultaneously and transmitted to the outside, mainly due to the limited bandwidth of the wireless telemetry. Many systems were not optimized and incurred an unnecessary increase in power consumption and chip area. There have been several systems with integrated functions of recording, processing (spike detection or spike feature extraction), and wireless telemetry [33], [29], [34], [35], [36], [17], [37], [38], [30]. However, a fully-integrated IC with simultaneous recording, on-chip spike *detection* and *feature extraction,* and low-power wireless telemetry that can support raw data from more than 100 channels has not been reported.

Chapter 3

Basic Building Block Design

3.1 Self-biased Fully-differential Preamplifiers

A fully differential and self-biased OTA was presented [14], as shown in Fig 3.1. This self-biased fully differential OTA enables the amplifier to operate at a low voltage with an exceptionally large CMRR and in a small area. A fully differential output has a great advantage over a single-ended output because it has a much larger CMRR. Since the OTA is self-biased, there is no need for a common mode feedback (CMFB) circuitry that sets an output common mode level, which enables the amplifier to be implemented with a low power and a small area for miniaturization. When a common mode signal is applied to the input pair of OTA, the output signal is suppressed by the negative feedback loop formed by the self-biased current source pair M_{PSC1}, M_{PSC2}, M_{NSC1}, and M_{NSC2}. However, when a differential signal is applied, the total source current supplied by M_{PSC1} and M_{PSC2} remains the same. Hence, the OTA amplifies only the differential signals.

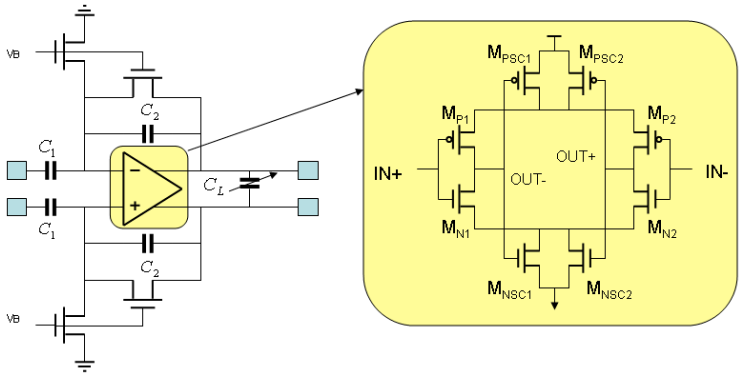

Fig. 3.1. An amplifier with a fully differential and self-biased OTA.

Due to the symmetrical structure of the circuit, a half-circuit model can be used, as shown in Fig. 3.2, to determine the DC operating point from the following equation.

$$\frac{1}{2}\left(\frac{W}{L}\right)_{p2}\mu_p C_{ox}\left(V_{SG,p2}+V_{th,p}\right)^2\cdot(1+\lambda_p V_{SD,p2}) = \frac{1}{2}\left(\frac{W}{L}\right)_{n2}\mu_n C_{ox}\left(V_{GS,n2}-V_{th,n}\right)^2\cdot(1+\lambda_n V_{DS,n2}) \quad (3.1)$$

With a channel length longer than the minimum feature size of the process chosen for the analog amplifier design in general, we can ignore the Early effect, resulting in the DC output common level as below.

$$V_O = \frac{V_{DD}+V_{th,p}+\sqrt{\kappa}\cdot V_{th,n}+\sqrt{\kappa}\cdot V_{SS}}{\sqrt{1+\kappa}}, \quad \text{where} \quad \kappa = \frac{\left(\frac{W}{L}\right)_{n2}\mu_n}{\left(\frac{W}{L}\right)_{p2}\mu_p} \quad (3.2)$$

From the equation (3.2), it can be seen that the DC output common level V_O is purely determined by the geometric parameter of M_{P2} and M_{N2}. In general, it is preferable to set V_O to $(V_{dd} + V_{ss})/2$, which is GND in this design, for maximum output range. Assuming a symmetrical dual power supply level, ($V_{dd} = -V_{ss}$) the desired geometric ratio of two source transistors, κ, can be set as below.

$$V_O = \frac{V_{DD}+V_{th,p}+\sqrt{\kappa}\cdot V_{th,n}+\sqrt{\kappa}\cdot V_{SS}}{\sqrt{1+\kappa}} = 0 \quad (3.3)$$

$$\kappa = \left(\frac{V_{DD}-\left|V_{th,p}\right|}{V_{DD}-V_{th,n}}\right)^2 \quad (3.4)$$

To determine the transconductance of the OTA, we again take advantage of the symmetry of the circuit for the analysis. As explained above, for the differential input, we can assume that M_{P2} and M_{N2} in Fig. 3.2 form a constant current source. Thus, the transconductance of the half circuit is simply the sum of transconductance of the two input transistors, M_{N1} and M_{P1}, resulting in the overall transconductance as below.

$$g_m = 2g_{m,half} = 2\left(g_{mn1} + g_{mp1}\right). \tag{3.5}$$

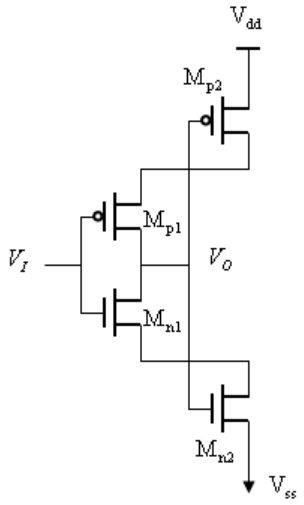

Fig. 3.2. The half circuit model for the analysis of OTA.

3.2 Passive Filters with Miller Capacitance Technique

To overcome the problems of passive filters mentioned in the previous chapter, a Miller capacitance technique is adopted at the expense of a small static power [14]. In Fig. 3.3 (a), the equivalent impedance Z_{eq} can be calculated as below,

where, R_{out} and A are the output impedance and voltage gain of the Miller amplifier, respectively.

$$Z_{eq} = \frac{V_i}{I_i} = \frac{R_{out}}{1+A} + \frac{1}{j\omega(1+A)C} = R_{eq} + \frac{1}{j\omega C_{eq}} . \tag{3.6}$$

From (3.6), we can determine that the equivalent capacitance and resistance is modified by the factor (1+A).

$$R_{eq} = \frac{R_{out}}{1+A}, \qquad C_{eq} = (1+A)C . \tag{3.7}$$

For a fully differential signaling scheme, the circuit is modified as Fig. 3.3 (b). In this circuit, the gain of the amplifier should be greater than 3 to achieve the area reduction of the capacitance. The circuit of the proposed filter with the Miller capacitance technique is shown in Fig. 3.4.

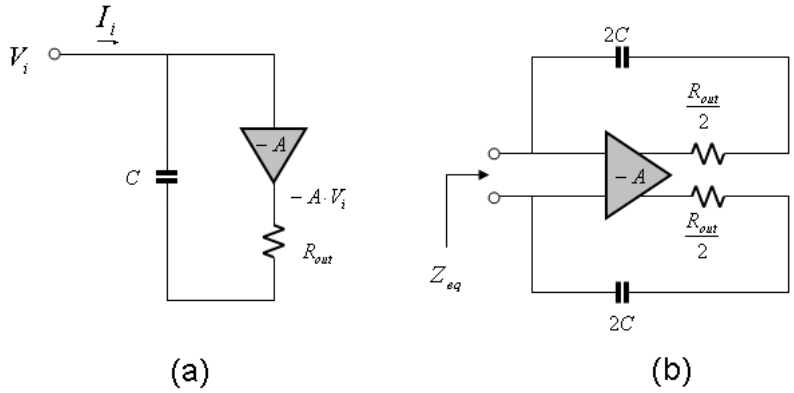

Fig. 3.3. (a) Increased capacitance using Miller effect and (b) for fully differential signaling scheme.

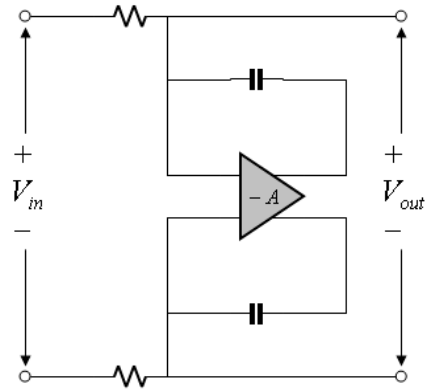

Fig. 3.4. Low pass filter with Miller capacitance technique.

3.3 Fully-differential Low-power SAR ADC

Successive approximation register (SAR) ADC is well suited for low-power and small-area applications because it requires a minimal analog circuitry [39]. The resolution of the ADC can be adjusted from 6 to 9 bits by external control signals. To reject the common mode noise, an ADC is designed to directly digitize a differential signal. The block diagram of the SAR ADC is given in Fig. 3.5. The comparator of the ADC is based on a track-and-latch comparator, and its schematic is shown also in Fig. 3.5. The sizes of the transistors N1, N2, N3, N4, P1, and P2 can directly affect the offset of the ADC and therefore are chosen to be large enough to guarantee that the offset is determined only by a few least significant bits (LSBs) when the minimum reference voltage is applied.

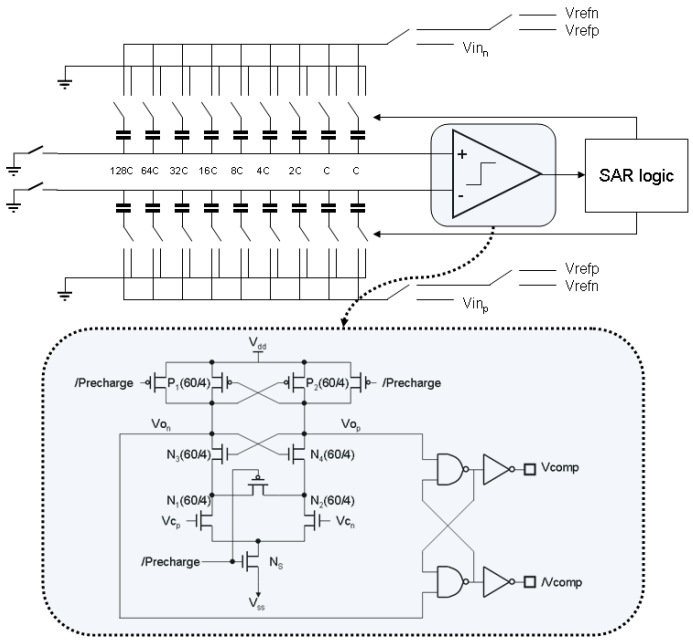

Fig. 3.5. Schematic of a fully differential SAR-ADC and a comparator used.

Chapter 4

Subsystem Design

This chapter discusses the design of critical functional blocks of the integrated wireless neural recording systems. An analog front-end is often called a neural interface circuit because it receives neural signals from the recording electrodes and performs basic analog operations, such as amplifications and filtering, and if necessary, converts the signal into a digitized form. Wireless telemetry is a circuit block that wirelessly transmits the final data to the receiver away from the recording site. These functional blocks are composed of basic circuit blocks described in the previous chapter and play important roles during the operation of the system. Discussed next are how to optimize the design of the analog front-end block and how to design high-data rate wireless telemetry based on UWB.

4.1 Integrated Front-end Blocks for Neural Recording Systems

Advances in micro-electrode arrays (MEAs) have enabled neuroscientists and researchers in biomedical engineering to take advantage of a large number of channels [40], which has made it possible to pursue a variety of neuroprosthetic applications, such as brain-controlled limb prostheses to treat spinal cord injuries and paralysis. A Brain Machine Interface (BMI) is at the core of these applications to sense the brain signals.

These applications, by nature, impose serious limitations on the power and the chip area in the design of neural recording systems. Researchers have developed

several kinds of neural recording systems [41], [42], [43], [44], [45], which are generally composed of pre-amplifiers to amplify the small extracellular potentials, low-pass filters to reject the high frequency noise, multiplexers, and analog to digital converters (ADCs), followed by the wireless telemetry circuits to transmit data out of the body.

Significant efforts have been devoted to minimizing the power of each individual circuit block of the neural recording systems to maximize the system's resolution. However, almost no attention has been paid to determining the trade-offs among those circuit blocks to achieve an optimal design. For example, designers determine their system's resolution without considering electrode noise, even though the noise contributed by the electrode is significant, leading to higher-than-required resolution, eventually consuming unnecessarily a large power and a large chip area. The multiplexing ratio is also an important system design parameter because it is the key parameter in the trade-off between the system's power consumption and chip area. However, there has been no analysis of this critical parameter, which is usually chosen in an arbitrary manner. An analysis of an optimal design would greatly help to optimally design a low-power neural recording system and integrate more functions, such as signal processing, to overcome the interference among electrodes to reduce the data rate. We will investigate such a design methodology for a neural recording system.

4.1.1. Architecture and Circuit Modeling

Fig. 4.1 shows the general architecture of the multi-channel neural recording system. The total number of the channels is N(=2^n) and the total number of the ADCs is M(=2^m), resulting in a multiplexing ratio of 2^{n-m}. A low-noise pre-amplifier is required to amplify the small potential difference between the recording microelectrode and a relatively large reference electrode when an action potential is generated inside the neuron. Typically, these extracellular potentials have amplitudes from 50 μV to 1 mV, and most signal energy is located between 300 Hz to 10 KHz.

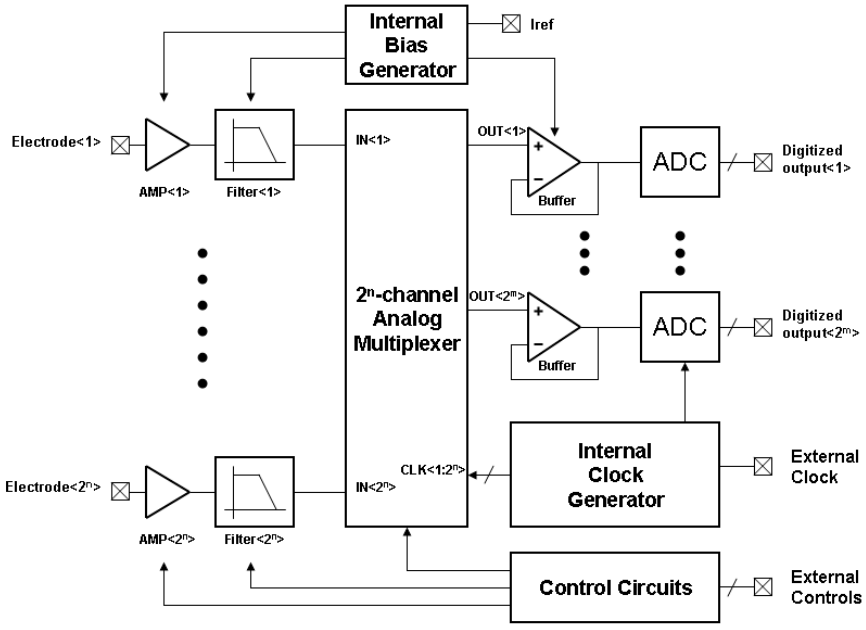

Fig. 4.1. General architecture of the multi-channel neural recording system.

Fig. 4.2 shows the schematic of a pre-amplifier composed of an operational transconductance amplifier (OTA) and a feedback network. A capacitive negative feedback amplifier is widely used in neural recording systems [13] because there is

usually a DC offset of 1-2 V across the electrode-tissue interface [11]. The gain of the amplifier is determined by the ratio of the two capacitances in the feedback network.

$$G_{amp} = \frac{C_1}{C_2} \quad . \tag{4.1}$$

The input-referred noise voltage of this amplifier [13] is given by

$$\overline{v_{ni,amp}^2} = \left(1 + \frac{1}{G_{amp}}\left(1 + \frac{C_{in}}{C_2}\right)\right)^2 \cdot \frac{16k_BT}{3g_m} \cdot f_{Neuron} \quad , \tag{4.2}$$

where C_{in} is the input capacitance of the OTA, g_m is the transconductance of the OTA, and f_{Neuron} is the signal bandwidth of the action potential. The physical size of the amplifier is mostly determined by the feedback capacitors, and hence the size is approximately proportional to the amplifier gain.

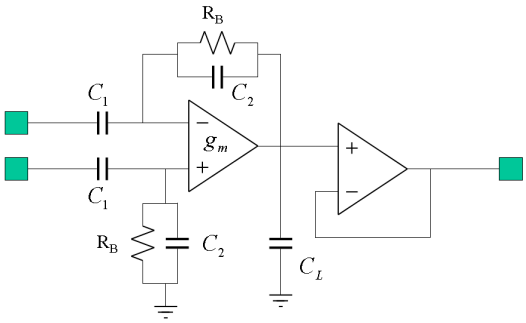

Fig. 4.2. Circuit diagram of pre-amplifier.

Although the pre-amplifier can provide the 1st-order low-pass filtering capability, dedicated low-pass filters are used to further minimize the high frequency noise. The cut-off frequency of low-pass filters is usually set to f_{Neuron}, 10 KHz. Several kinds of low-pass filters, such as gm-C filters and passive RC filters, can be

used for this purpose. Among those, passive RC filters are the most straightforward and easy to implement. However, the area of a passive element is relatively large for on-chip implementation due to the low cut-off frequency. To overcome this disadvantage, the Miller effect can be used at the expense of increased power consumption [14] as proposed in chapter 3. Because the cut-off frequency of the filters is independent of the multiplexing ratio, we can represent the power consumption for filtering as a constant, P_{LPF1}. However, filters also need buffers to drive the analog multiplexer, and these buffers must meet the slew rate and output impedance constraints. Fig. 4.3 shows a simplified model of low-pass filters and analog multiplexers. In most cases, the slew rate is the limiting factor, while the output impedance is easily achievable. As the slew rate of the buffer is proportional to the biasing current, the following inequality holds:

$$\frac{2G_{amp}V_{Neuron}}{(1/\lambda)(1/f_S)} \le \frac{I_{BF}}{C_{pmux}}. \tag{4.3}$$

Here, V_{Neuron} is the maximum amplitude of the extracellular potential, which means that the maximum signal change between two consecutive channels can be $2V_{Neuron}$. The sampling rate of the ADCs, f_s , increases with the multiplexing ratio. This can be expressed as $f_s=2^{n-m}2f_{Neuron}$, if we use the Nyquist sampling ratio. C_{pmux} is the parasitic loading capacitance, which is also proportional to the multiplexing ratio of the analog multiplexers and is equal to $C_{pmux1}2^{n-m}$ where C_{pmux1} is the parasitic loading of just one channel. The timing margin ratio λ is determined by the sampling clock's jitter,

skew, and the minimum timing window of the ADC. Therefore, (4.3) can be rewritten as

$$I_{BF} \geq 4\lambda G_{amp} V_{Neuron} f_{Neuron} C_{pmux1} 2^{2(n-m)} . \tag{4.4}$$

The mathematical model of the total power consumption of filters is:

$$\begin{aligned} P_{FILTER,total} &= 2^n \cdot (2V_{dd} \cdot I_{BF} + P_{LFP1}) \\ &= 2^n \left(2V_{dd} \cdot 4\lambda G_{amp} V_{Neuron} f_{Neuron} C_{pmux1} 2^{2(n-m)} + P_{LPF1}\right) \\ &= 8\lambda V_{dd} G_{amp} V_{Neuron} f_{Neuron} C_{pmux1} 2^{3n-2m} + 2^n P_{LPF1} \end{aligned} . \tag{4.5}$$

However, when one ADC is used per one channel, there is no need for buffers and the above model is simplified to:

$$P_{FILTER,total} = 2^n P_{LPF1} . \tag{4.6}$$

Usually, the chip area of the filtering part is independent of the multiplexing ratio, and the buffers' area is negligible compared to filtering part. Thus, the total filter area can be described as

$$\begin{aligned} A_{FILTER,total} &= 2^n \cdot (A_{BF1} + A_{LPF1}) \quad \text{when } n > m, \\ &= 2^n A_{LPF1} \quad \text{when } n = m, \end{aligned} \tag{4.7}$$

where A_{BF1} is the area of one buffer and A_{LPF1} is that of a filter.

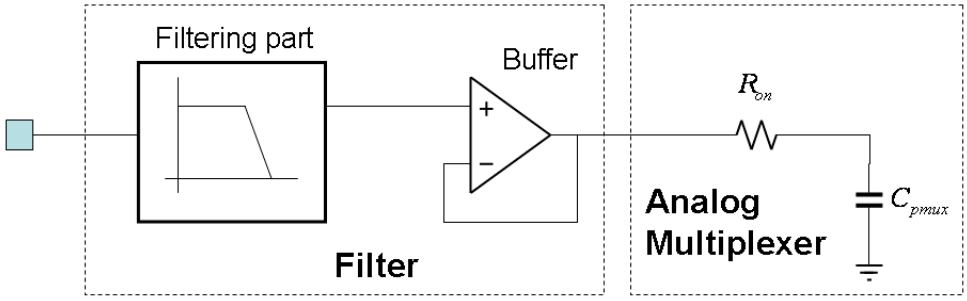

Fig. 4.3. Simplified modeling of filter and analog multiplexer.

Crosstalk noise can cause a serious problem in multi-channel recording systems. There are three possible crosstalk noise sources in an integrated neural recording system. The first is the capacitive coupling between metal interconnections, the second is the finite turn-off resistance of the analog switches due to subthreshold conduction, and the third is the capacitive coupling through the parasitic capacitances of the transistor. As for capacitive coupling between metal lines, those coupling capacitances can be eliminated by careful shielding of each signal line at the expense of increased bussing area [18]. In general, the signal common-mode level is set to the middle of the power supply level, and the amplified signal rarely exceeds a few hundred mV. Therefore, there is a large back-bias effect making the subthreshold conduction negligible. In general, the turn-off resistance is more than several GΩ, which is significantly larger than the turn-on resistance of the analog switches. As a result, the only remaining crosstalk noise source is the parasitic coupling in the MOS transistors through the source-to-substrate junction capacitance and the drain-to-substrate junction capacitance. We can model the crosstalk noise from a channel using the Thevenin's equivalent circuit as shown in Fig. 4.4. The equivalent voltage amplitude and source impedance can be calculated as below,

$$Z_{OFF}(s) = \frac{1}{sC_{JSB}} + \left(R_{Bulk} \parallel R_{OUT} + \frac{1}{sC_{JDB}} \right) \cong \frac{1}{sC_{JSB}} + \left(R_{Bulk} \parallel \frac{1}{sC_{JDB}} \right) = \frac{1}{sC_{JSB}} + \frac{R_{Bulk}}{1 + sR_{Bulk}C_{JDB}} , \quad (4.8)$$

$$V_{NOFF}(s) = \frac{R_{Bulk}}{R_{OUT} + \frac{1}{sC_{JSB}} + R_{Bulk}} \cdot V_N = \frac{sR_{Bulk}C_{JSB}}{1 + s(R_{OUT} + R_{Bulk})C_{JSB}} , \quad (4.9)$$

where C_{JSB} is the source-to-substrate junction capacitance, C_{JDB} is the drain-to-substrate junction capacitance, R_{Bulk} is the substrate resistance, and R_{OUT} is the output

impedance of the buffers in the filter. Using this equivalent circuit, we can model the worst-case crosstalk noise in the N-channel neural recording system, as shown in Fig. 4.5. From this, the crosstalk noise can be calculated as

$$V_{COUPLING} = \frac{R_{OUT} + R_{ON}}{R_{OUT} + R_{ON} + \frac{Z_{OFF}}{N-1}} \cdot (N-1) V_{NOFF} = \frac{R_{OUT} + R_{ON}}{R_{OUT} + R_{ON} + \frac{Z_{OFF}}{N-1}} \cdot \frac{s(N-1)R_{Bulk}C_{JSB}}{1 + s(R_{OUT} + R_{Bulk})C_{JSB}} \cdot V_N$$

$$\therefore \frac{V_{COUPLING}}{V_N}(j\omega) = \frac{R_{OUT} + R_{ON}}{R_{OUT} + R_{ON} + \frac{1}{j\omega(N-1)C_{JSB}} + \frac{R_{Bulk}/(N-1)}{1 + j\omega R_{Bulk}C_{JDB}}} \cdot \frac{j\omega(N-1)R_{Bulk}C_{JSB}}{1 + j\omega(R_{OUT} + R_{Bulk})C_{JSB}} \quad , \qquad (4.10)$$

where R_{ON} is the turn-on resistance of the switches and is set to 5 KΩ. C_{JSB} and C_{JDB} are set to 7.1fF, which is typical for 0.35 µm CMOS process. R_{OUT} and R_{Bulk} are set to 4 KΩ and 10 Ω, respectively. With these values, we can determine that the worst-case crosstalk noise by the parasitic capacitances in the analog multiplexer is approximately 120dB at 10 KHz for the 128 channels.

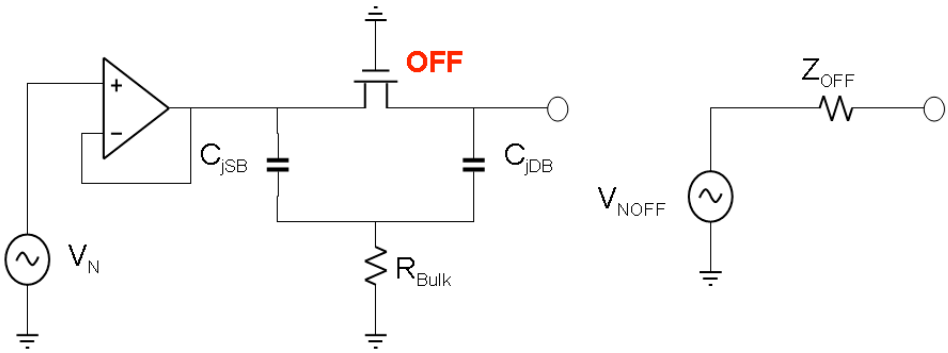

Fig. 4.4. Crosstalk noise due to the parasitics of the switch and its Thevenin's equivalent circuit.

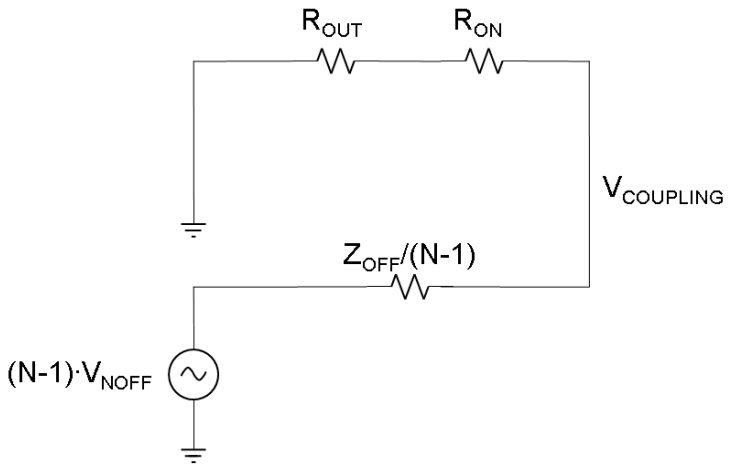

Fig. 4.5. Modeling of crosstalk noise in N-channel analog multiplexer.

Similar to the buffers that drive the analog multiplexer presented previously, the power consumption of the buffers to drive ADCs is also determined by the slew rate, which means the biasing current of one buffer is proportional to the multiplexing ratio as shown below:

$$\begin{aligned} I_{BA} &\geq 2G_{amp}V_{Neuron}f_S C_{in,ADC} \\ &\geq 2G_{amp}V_{Neuron}2^{n-m+1}f_{Neuron}C_{in,ADC}. \end{aligned} \tag{4.11}$$

Here, $C_{in,ADC}$ is the input capacitance of the each ADC. Therefore, the total power consumption of the 2^m buffers is independent of the multiplexing ratio as below,

$$\begin{aligned} P_{BUF,total} &= M \cdot 2V_{dd}I_{BA} \\ &= M \cdot V_{dd} \cdot 2^{n-m+3}G_{amp}V_{Neuron}f_{Neuron}C_{in,ADC} \\ &= V_{dd} \cdot 2^{n+2}G_{amp}V_{Neuron}f_{Neuron}C_{in,ADC} \end{aligned}, \tag{4.12}$$

where V_{dd} is the power supply voltage. Also, the total power consumption of 2^m ADCs is constant, regardless of the multiplexing ratio, because the power consumption of one ADC is roughly proportional to the sampling rate and the

sampling rate is proportional to the multiplexing ratio. In other words, the power consumed by the one ADC increases as the multiplexing ratio does. However, the total power consumption of the ADCs remains the same because the number of ADCs decreases proportionately. However, the total area consumed by ADCs is directly proportional to the number of ADCs multiplied by the area of one ADC, A_{ADC1}.

$$A_{ADC,total} = M \cdot A_{ADC1} = 2^m \cdot A_{ADC1} \propto 2^m \cdot C_{in,ADC} . \quad (4.13)$$

The last relationship is generally valid because sampling capacitors occupy most of the chip area in SAR ADC.

4.1.2. System Resolution

The dynamic range to noise ratio (DNR) of a neural recording system cannot exceed that of an input signal at the pre-amplifier's input, regardless of the amplifier's input equivalent noise voltage and the number of bits of the ADC. Generally, the area of SAR ADC increases exponentially with the number of bits. Also, the worst-case power consumption of the ADC is proportional to the sampling capacitance, which increases exponentially with the number of bits as well [39]. In addition, the amplifier's input equivalent noise voltage decreases as the gain of the amplifier increases, as can be seen in (4.2). This means that there is a trade-off between the amplifier's area and the noise. The amplifier gain is not the only design parameter that affects the amplifier's input equivalent noise. Noise can also be reduced by increasing the OTA's transconductance, which increases the power and the area of the OTA. Therefore, to avoid wasting the power and the chip area when increasing

the system's resolution, it is critical to know the fundamental limit of the system's dynamic range determined by the input signal to avoid over-design.

The amount of thermal noise contributed by the electrode is given by the Nyquist's formula

$$V_{RMS} = \sqrt{4k_B TR\Delta f}\,, \tag{4.14}$$

where k_B is Boltzmann's constant ($k_B = 1.38\times10^{-23}$ Joules/Kelvin), T is the temperature (in degrees Kelvin), R is the resistance of the electrode (in Ohms), and Δf is the recording bandwidth (in Hz). The resistance of the electrode includes the resistance of the metallic portion of the microelectrode and the seal resistance, sometimes called the spreading resistance, which is the resistance of the saline bath between the metallic interface and ground electrode [46]. For an electrode with a resistance of 1 MΩ operating at 27°C with a 10 KHz recording bandwidth, the RMS noise voltage is 12.6 μV. Furthermore, there is as much background noise, which is a sum of many smaller spikes, as thermal noise [47]. In general, the maximum amplitude of extracellular spike potentials is less than 1 mV, and the noise is around 20 μV for 1 MΩ. Therefore, the DNR of input signal is about 34 dB. This implies that regardless of how large the number of bits of the ADC and how small the amplifier noise, the system's effective number of bits cannot exceed 6. Therefore, it is reasonable to make the ADC's DNR the same as that of input signal and make the amplifier's input equivalent noise negligible to achieve as large a DNR as possible (in this case, 6 bits). Thus, we can set the number of bits in the ADC, N_B, to satisfy following relationship.

$$V_{noise,eltd}^2 = \left(\frac{1}{\sqrt{2}} \frac{V_{Neuron}}{2^{N_B-1}} \right)^2 . \quad (4.15)$$

In this work, we set the amplifier's noise power to be 1/10 of the electrode noise power. This results in the small 4.8% increase in the total equivalent RMS noise voltage. From (4.2) and (4.15), we can express the relationship mentioned above as:

$$\left(1 + \frac{1}{G_{amp}}\left(1 + \frac{C_{in}}{C_2}\right)\right)^2 \cdot \frac{16k_BT}{3g_m} \cdot f_{Neuron} = V_{noise,eltd}^2 \times 0.1 = \left(\frac{V_{Neuron}}{2^{N_B-1}}\right)^2 \times \frac{1}{20} . \quad (4.16)$$

This equation can be rewritten as:

$$G_{amp} = \frac{\left(1 + \frac{C_{in}}{C_2}\right)}{-1 + \sqrt{\frac{g_m}{g_{m,\min}}}} \left(, \text{where } g_{m,\min} = \frac{5 \cdot 4^{N_B+2} k_B T f_{Neuron}}{3V_{Neuron}^2} \right) . \quad (4.17)$$

This equation sets the lower bound for g_m, the OTA's transconductance. If we choose a small g_m for low-power operation (by reducing DC bias current of the OTA), the amplifier gain should increase to meet the noise constraint, and this results in the increased chip areas because we have to increase the size of the feedback capacitance C_1. Therefore, there exists a trade-off where the optimal design can be found by setting the g_m and G_{amp} such that the power and area product of the amplifier is minimal. This power and area product of the amplifier is proportional to the product of g_m^2 and G_{amp}, if the transistor operates in the saturation region and the width of the transistors is unchanged.

$$g_m^2 G_{amp} = \frac{b \cdot g_m^2}{\sqrt{g_m} - a} \quad (, where \quad a = \sqrt{g_{m,\min}}, \quad b = \left(1 + \frac{C_{in}}{C_2}\right) \cdot \sqrt{g_{m,\min}}) . \quad (4.18)$$

To determine the minimum, we differentiate the above equation with respect to g_m.

$$\frac{\partial\left(g_m^2 G_{amp}\right)}{\partial g_m} = b \cdot \frac{2g_m \cdot \left(\sqrt{g_m} - a\right) - g_m^2 \cdot \frac{1}{2\sqrt{g_m}}}{\left(\sqrt{g_m} - a\right)^2} = b \cdot \frac{g_m \cdot \left(\frac{3}{2}\sqrt{g_m} - 2a\right)}{\left(\sqrt{g_m} - a\right)^2} \quad (4.19)$$

Setting this equation to zero, we find the $g_{m,opt}$ that makes (4.18) minimum.

$$g_{m,opt} = \left(\frac{4}{3}\right)^2 \cdot a^2 = \frac{16}{9} \cdot g_{m,\min} = 1.78 \cdot g_{m,\min} \quad (4.20)$$

From (4.17), the optimal gain of the amplifier is given by:

$$G_{amp,opt} = 3\left(1 + \frac{C_{in}}{C_2}\right) \quad (4.21)$$

For values of $C_{in}/C_2 = 7$ the optimal value of the amplifier's gain is 24. With conservative margins, it is proper to choose 50 as the pre-amplifier's gain. However, it is typical to employ an additional amplifier after the analog multiplexer because this preamplifier alone cannot provide enough signal gain. The second amplifier is shared by all the recording channels and does not need to be a low-noise amplifier; the power consumption and chip area required are usually negligible compared to other circuit blocks.

4.1.3. Trade-off between System Power and Chip Area

In this section, using real circuit examples, we will discuss the optimal number of ADCs when the total number of channels is given. Simply, the total power consumption of the system is the sum of each block's power consumption, given by:

$$P_{system} = P_{AMP,total} + P_{FILTER,total} + P_{MUX,total} + P_{BUF,total} + P_{ADC,total} \quad (4.22)$$

In real implementations, the power consumption of one amplifier with the optimal transconductance and gain given by (4.20) and (4.21), respectively, was 170 μW. Therefore, the total power consumption of 2^n amplifiers is simply:

$$P_{AMP,total} = 2^n \cdot 170(\mu W) \quad . \tag{4.23}$$

The power consumption for pure filtering was 99 μW. Using (4.15) and (4.16), the total power consumption of the filters was described as:

$$\begin{aligned} P_{FILTER,total} &= 99 + 0.13 \cdot 2^{2(n-m)} (\mu W), \quad \text{when} \quad n > m \\ &= 99 \qquad\qquad\qquad\quad (\mu W), \quad \text{when} \quad n = m \end{aligned} \quad . \tag{4.24}$$

The power consumed by the analog multiplexer was so small that it is negligible. Also, the power consumption of buffers and ADCs were, respectively:

$$P_{BUF,total} = 2^{n+2} \cdot 3.62(\mu W) \quad . \tag{4.25}$$

$$P_{ADC,total} = 2^n \cdot 0.89(\mu W) \quad . \tag{4.26}$$

Table 2 shows the calculation results for various numbers of channels and ADCs, and it can be seen that in terms of power consumption, the one-ADC per one-channel system is the best. This is a very natural result because it does not need buffers to drive the analog multiplexer.

Also, the total chip is approximately the sum of areas of each block, which is:

$$A_{system} = A_{AMP,total} + A_{FILTER,total} + A_{MUX,total} + A_{BUF,total} + A_{ADC,total} \quad . \tag{4.27}$$

However, the area of the multiplexer is very small compared to those of other circuit blocks. Therefore, (4.27) can be rewritten as:

$$A_{system} \cong A_{AMP,total} + A_{FILTER,total} + A_{BUF.total} + A_{ADC,total} \quad . \tag{4.28}$$

The area occupied by the pre-amplifiers is determined by the number of channels, not by the multiplexing ratio, because the area of the amplifier is predominantly determined by the size of the feedback capacitances, which is independent of the multiplexing ratio. Therefore, the area of the amplifier can be treated as a constant. The area of one amplifier whose gain is determined by the (4.21), was 120000μm^2 when implemented with 0.35μm CMOS process. Therefore, we can model the area of the 2n amplifiers simply as below:

$$A_{AMP,total} = 2^n \cdot 120000\mu m^2 . \tag{4.29}$$

Also, the total area of the filters was modeled according to (4.7), and it is given by:

$$\begin{aligned} A_{FILTER,total} &= 2^n \cdot (A_{BF1} + A_{LPF1}) = 2^n \times 82950\mu\text{m}^2, \quad \text{when } n > m \\ &= 2^n A_{LPF1} = 2^n \times 78330\mu\text{m}^2 \quad , \quad \text{when } n = m \end{aligned} . \tag{4.30}$$

The area of one buffer to drive ADCs was 14100 μm^2, making the total area occupied by 2^m buffers:

$$A_{BUF,total} = 2^m \cdot 14100\mu m^2 . \tag{4.31}$$

The optimal number of bits of ADCs determined was 6. With a conservative margin, we set the number of bits of the ADC to be 9. This resulted in a size of 848000μm^2 per ADC. Therefore, the total area of 2m ADCs is simply given by:

$$A_{ADC,total} = 2^m \cdot 848000\mu m^2 . \tag{4.32}$$

Using (4.29)-(4.32), the total chip area described as (4.28) is:

$$\begin{aligned} A_{system} &= \left(2^n \times 0.203 + 2^m \times 0.862\right)\text{mm}^2 \quad , \text{when } n > m \\ &= 2^n \times 1.06\text{mm}^2 \quad , \text{when } n = m \end{aligned} . \tag{4.33}$$

Table 3 is the calculated area of the neural recording system with various channel numbers and ADCs. The total chip area increases with the number of ADCs, which can be observed clearly. Therefore, there must be an optimal multiplexing ratio that minimizes the system's power-area product.

Table 4 is the power-area product based on Table 4.1 and Table 4.2. From Table 4.3, we can determine that the optimal number of channels per one ADC is 16. Fig. 4.6 shows the power-area product of the 128-channels system as a function of the multiplexing ratio. As expected, at the extremes of the multiplexing ratio, the power-area product is dominated by either the power or the area.

Though this example uses the area and power values for specific circuit topologies and process technology, the optimization methodology is applicable to other topologies and technologies. Optimal design can vary for different applications, even with the same specifications. The design must assign priorities to different performance metrics (i.e., power and area of individual blocks and system) and take the additional constraints into account. For example, one might reuse a circuit block that is a part of the overall system. In such a case, the optimization has to be based on the given condition. In general, it is necessary for designers to ensure that a proper design methodology is adopted to take into account all of the parameters in order to make the right choice of system architecture.

Table 4.1. System power [mW] according to various numbers of channels and ADCs.

Power	m=0 (1 ADC)	m=1 (2 ADC)	m=2 (4 ADC)	m=3 (8 ADC)	m=4 (16 ADC)	m=5 (32 ADC)	m=6 (64ADC)	m=7 (128ADC)
n=4 (16ch)	5.08	4.68	4.58	4.56	**4.5**	N.A	N.A	N.A
n=5 (32ch)	13.36	10.16	9.36	9.17	9.11	**9.1**	N.A	N.A
n=6 (64ch)	52.28	26.27	20.33	18.73	18.33	18.23	**18.2**	N.A
n=7(128ch)	309	105	53.4	40.7	37.5	36.7	36.5	**36.4**

Table 4.2. Chip area [mm^2] according to various numbers of channels and ADCs

Area	m=0 (1 ADC)	m=1 (2 ADC)	m=2 (4 ADC)	m=3 (8 ADC)	m=4 (16ADC)	m=5 (32ADC)	m=6 (64ADC)	m=7 (128ADC)
n=4 (16ch)	**4.1**	5.0	6.7	10.1	17.0	N.A	N.A	N.A
n=5 (32ch)	**7.4**	8.2	9.9	13.4	20.3	33.9	N.A	N.A
n=6 (64ch)	**13.9**	14.7	16.4	19.9	26.8	40.6	67.8	N.A
n=7 (128ch)	**26.8**	27.7	29.4	32.9	39.8	53.6	81.2	135

Table 4.3. Power and chip area product [mW•mm^2] with respect to various numbers of channels and ADCs

Unit [mW•mm^2]	m=0 (1 ADC)	m=1 (2 ADC)	m=2 (4 ADC)	m=3 (8 ADC)	m=4 (16 ADC)	m=5 (32 ADC)	m=6 (64ADC)	m=7 (128ADC)
n=4 (16ch)	**20.82**	23.40	30.69	46.06	76.50	N.A	N.A	N.A
n=5 (32ch)	98.86	**83.31**	92.66	122.8	184.9	308.5	N.A	N.A
n=6 (64ch)	726.7	392.8	**333.4**	372.7	491.2	740.1	1234	N.A
n=7(128ch)	8281	2909	1570	**1339**	1493	1967	2964	4914

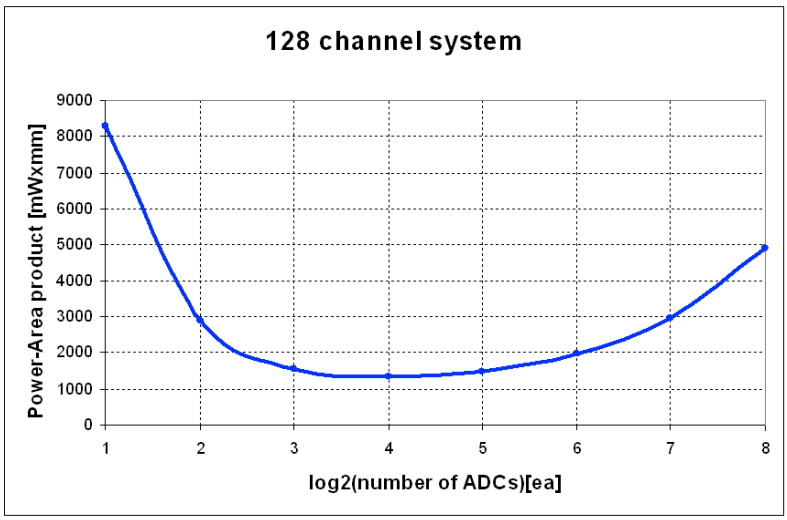

Fig. 4.6. Power-area product of 128-channels system as a function of the multiplexing ratio.

4.2 Ultra-wideband Data Telemetry

Although there are several communication standards for biomedical applications, most cannot warrant a sufficient bandwidth for simultaneous recording from more than 100 channels. For example, the MICS band, which is allocated for the unlicensed use of implantable devices, allows only 300kHz for data transmission. Other wireless technologies such as Wi-Fi and Bluetooth cannot be used directly, due to the power and area constraints on the implanted device. Therefore, there is a need for higher-bandwidth data transmission telemetry that consumes low-power and occupies less physical area.

UWB is a recently formed wireless technology used for low/high data rate wireless personal area network (WPAN) and short-range applications. It has the widest bandwidth (3.1GHz ~ 10.6GHz) among all technologies and the smallest emission power density (-41.3dBm/MHz), providing an opportunity for a wideband

wireless telemetry for neural recording systems. The reported receiver designs of UWB systems have consumed more power than those of narrow band communications [48]. However, in our neural recording applications, the implanted device requires only a transmitter and the receiver outside the body, unlike the other short range applications. Hence the transmitter power consumption and complexity have been traded off with that of the receiver, as the receiver is located outside and its power consumption and size are not crucial. This greatly simplifies the complexity of the implanted telemetry design, leading to reduction in power and area.

In this system, the impulse radio based UWB (IR-UWB) is employed, as the targeted application does not require a multiple access communication which requires complex transmitters consuming high power [49], [50]. In IR-UWB, short pulses are generated for sending data, and both the center frequency and bandwidth of the pulse need not be very accurate. Such a process is simple to design in a CMOS technology, resulting in a very simple, small-area, and low-power transmitter design, while providing a sufficient data bandwidth by virtue of its wideband nature.

4.2.1. Ultra Short Pulse Generations

In this section, we will analyze pulse generation schemes in both time and frequency domains. The method described here can be applied to different applications to meet the spectral mask of the UWB band. There are various methods to generate pulses. Among all methods, using the delay-and-AND gate or delay-and-XOR gate is the least complex way in CMOS integrated circuit technologies [51]. The delay unit can be realized using digital gates, such as inverters, analog

differential delay cells [52], and flip-flops or controllable capacitors [53]. A general scheme for such pulse generations is provided in Fig. 4.7.

The data signal s(t) and the delayed replica $s_d(t)$ are passed through an XOR gate or an AND gate to obtain a UWB narrow pulse x(t). A narrow band square wave can be represented by:

$$x(t) = \sum_{n=-\infty}^{\infty} g_T(t - nT_b), \tag{4.24}$$

where T_b is the bit period and

$$g(t - nT_b) = \begin{cases} A & nT_b < t \le (nT_b + \tau) \\ 0 & (nT_b + \tau) < t \le (n+1)T_b \end{cases}, \tag{4.25}$$

where A is the amplitude of the pulse and τ is the width of the UWB pulses obtained from the delay element as depicted in Fig. 4.8. The Manchester NRZ data is preferred because it always has a transition repeated in every bit period T_b. Assuming there is a pulse repeated in every bit period, the Fourier series of the signal in (4.24) is given by [54]:

$$x(t) = \frac{A\tau}{T_b} + \frac{2A\tau}{T_b} \sum_{k=1}^{+\infty} \frac{\sin(\pi k\tau / T_b)}{(\pi k\tau / T_b)} \cos(kwt). \tag{4.26}$$

The signal includes a DC term and the fundamental frequency together with harmonic frequencies. As can be seen, a rectangular UWB pulse has a sinc envelope as a coefficient. The first zero of sinc(x) will occur at $x = \pi$, that is $n = T_b/\tau$ in (4.26). It corresponds to a frequency of n/T_b or $1/\tau$. This first zero defines the distribution of

the UWB signal in the frequency domain as well as the number of the discrete spectral components. Fig. 4.9 shows waveforms for UWB pulses with two different widths that are obtained from the circuit design. Spectrum plots are for the pulses that have the width of 2 ns (Fig 4.9-a) and 500ps (Fig 4.9-c). As the design targets a data rate of 100 Mbps, Tb = 1/100 MHz = 10 ns. If we select the pulse width τ= 2 ns, the number of spectral components is Tb/τ = 5 (Fig. 4.9-b). When τ = 0.5 ns, the number of spectral lines are 20 (See Fig. 4.9). The distance between two spectral lines defines the data frequency (i.e., 100 MHz).

The best value for the delay is $\tau = T_b/2$. It results in the maximum power for the discrete spectral lines at the symbol rate frequency [54]. Using (4.26), the amplitude of the spectral lines becomes inversely proportional to their frequencies (amplitudes= $2A/k\pi$). In the UWB transmission, the power spectrum of these discrete lines should be lower than that of the allowed spectral mask by the UWB regulations, and this is why it is easy to have both A and the delay τ in (4.26) to control the power level of the signal such that it will fall within UWB spectral mask. Another observation is that once τ is arranged, increasing the bit period T_b yields a large number of spectral lines, as illustrated in Fig. 4.9.

The square pulse x(t) is passed through a pulse-shaping filter to decrease inter-symbol interference (ISI) during transmission. As square waves cause higher ISI, a pulse-shaping filter is used. A Gaussian pulse in UWB is generated after the pulse-shaping filter. In practice a high-pass filter of one or more order is used to obtain such a shape [51]. If we look into (4.26), we see that rectangular-shaped data extends over

an unlimited frequency band. When a high-pass filter (HPF) is used, the UWB frequency from 3.1 to 10.6 GHz frequencies can be selected. However, for the UWB band of 0-960 MHz, a low-pass filter should be used. In the frequency domain, the distance between two discrete spectral lines is $1/T_b$=100 MHz. Note that the data information is contained in these discrete spectral lines at $1/T_b$ (Fig. 4.9). When one of the UWB bands shown in Fig. 4.9 is transmitted, a narrow bandwidth band-pass filter (BPF) filter is used at the receiver site to obtain one of the spectral lines for the symbol detection.

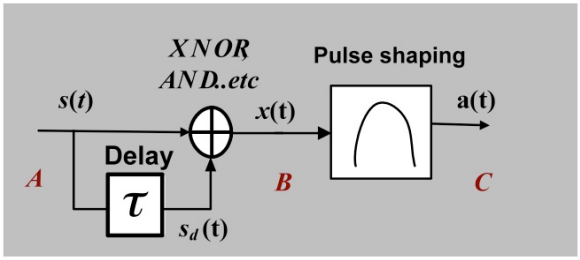

Fig. 4.7. An IR-UWB pulse generation scheme.

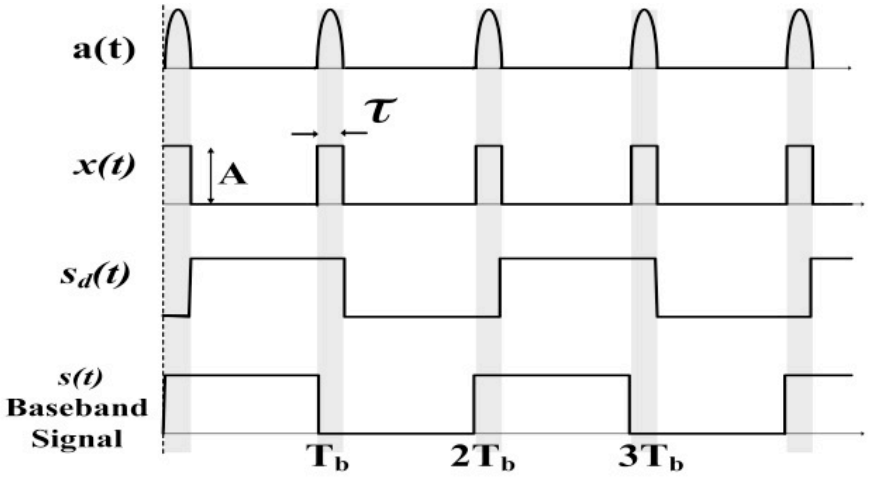

Fig. 4.8. Timing diagram for UWB pulse generation.

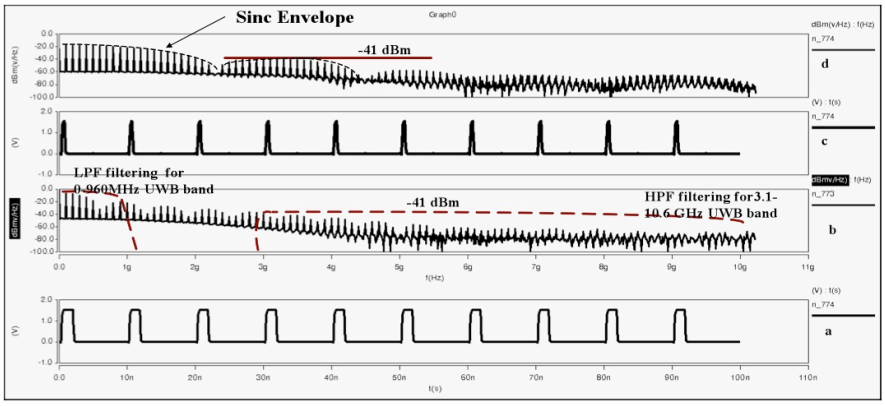

Fig. 4.9. Waveforms for UWB square waves.

4.2.2. CMOS UWB Transmitter Design

There are two common transmitter categories used for the UWB technology. The first category included a pulse generator and an up-converter that uses a mixer and a local oscillator (LO) to transfer the based band signal into UWB band. The second category consists of a pulse generator and a pulse-shaping circuitry only where the pulse directly falls in the UWB band. In those transmitters, there is no need for a mixer or a LO, which significantly reduces the complexity and power consumption of the transmitter [55]. As the transmitter in this application does not require a multi-access communication protocol and the power consumption is the most critical design specification, the second type of transmitter design techniques is used for our multi-channel neural recording system.

Fig. 4.10 is the block diagram of the IR-UWB transmitter. The first stage of the transmitter is an encoder, which enables the receiver to recover clocks directly from the encoded data and also to distinguish the data from different channels. The

encoded data is then passed to a narrow pulse generator. The pulse generator circuit used is shown in Fig. 4.11. In this circuit, a pulse width is adjusted by control voltage V_c. Generated pulses are passed through the pulse-shaping filter to fit them into the FCC emission mask and to eliminate the transmission of unnecessary bands.

Unlike other UWB applications, power amplifiers are not necessary since low power needs to be transmitted for a short-distance range in neural recording systems. Instead, a wideband-matching filter is used to regulate the transmitted power.

The transmitter can be configured to different pulse modulation schemes: on-off keying (OOK), pulse-position modulation (PPM), and binary phase shift keying (BPSK). A signal OOK_in is generated by passing the NRZ and the Manchester NRZ baseband signals through an AND gate. As shown in Fig. 4.12, when the signal OOK_in is given to the pulse generator circuit, depicted in Fig 4.11, x(t) will be an OOK modulated signal (Fig. 4.12). During the bit "1", a pulse is transmitted, and meanwhile there is no pulse during the bit "0". The PPM signal is generated as follows: Manchester NRZ is passed through the pulse-generation circuit. The resulted narrow pulses are added (using an XOR gate) with the OOK UWB (Fig 4.12-d) to obtain the PPM UWB in Fig. 4.12. The pulse position is different for bit "1" than for bit "0". The bits are positioned to make the bit detection easier at the receiver site. To generate a BPSK signal, the pulse is inverted by 180° when the bit is "0".

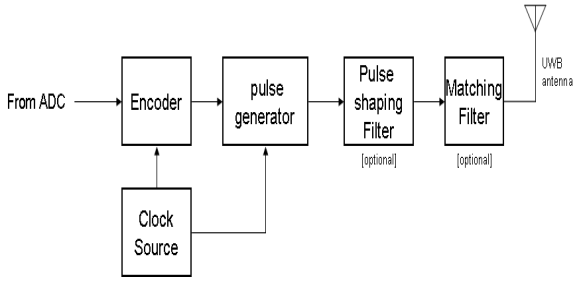

Fig. 4.10. Block diagram of IR-UWB wireless transmitter.

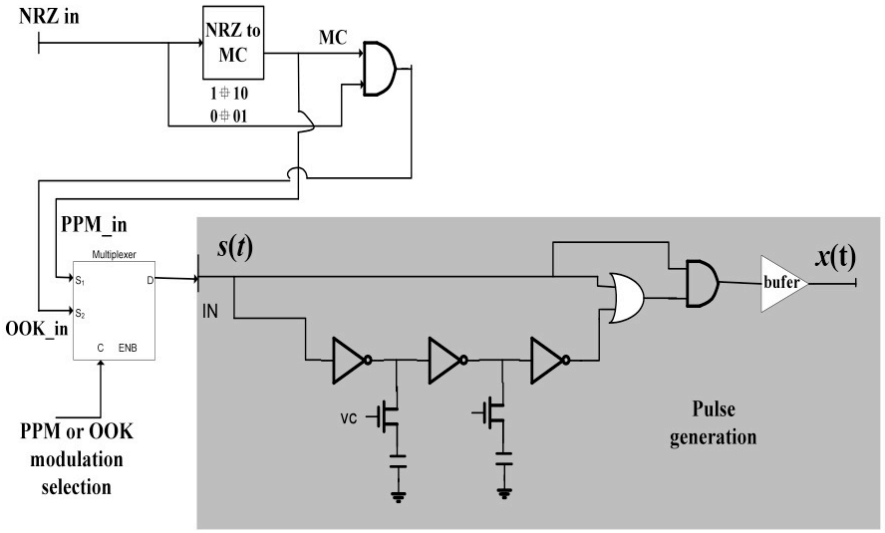

Fig. 4.11. Circuit used for pulse generation and modulation selection.

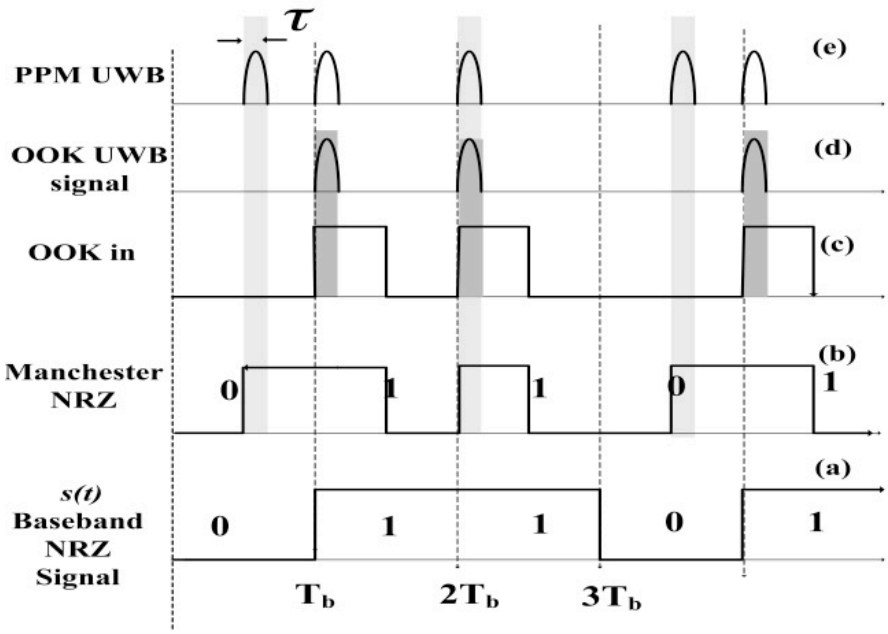

Fig. 4.12. Time diagram for PPM and OOK modulation.

Chapter 5

128-channel Integrated Wireless Neural Recording IC

To overcome the limitations of the previous works mentioned in Chapter 2, This chapter presents an integrated low-power IC chip that can record, process, and wirelessly transmit neural signals in real-time. This IC chip is able to simultaneously record and transmit raw data from 128 channels wirelessly [56], [58], [59] and serves as the core hardware for applications mentioned above when combined with additional components.

5.1 Chip Architecture

The chip has eight 16-channel front-end blocks. Each block consists of amplifiers, a multiplexer, and an ADC. The front-end blocks are followed by a data serializing circuit, a DSP unit for spike detection and feature extraction, a digital MUX, an encoder, and a UWB transmitter (Fig. 5.1). On-chip bias generators provide DC bias voltages to the front-end blocks. At the front-end, weak and noisy neural signals from electrodes are amplified by self-biased, fully-differential pre-amplifiers and time-multiplexed by an analog multiplexer (Fig. 5.2). A second amplifier provides additional gain for the proper operation of the subsequent ADC. A successive-approximation-register (SAR) ADC is used to digitize the 16-to-1 time-multiplexed analog signals. The amplifiers are designed to have programmable gain and bandwidth to meet the requirements of various biological experiments. There is a trade-off between power and area because as we increase the number of channel per

one ADC, the chip area decreases, while the power consumption increases due to the increased multiplexer loading [10]. Careful analysis shows that the power and area product is minimized when a 16:1 multiplexer is used in the technology [10]. A sequential turn-on method in the front-end blocks is utilized to save power. Two of the 16 channels are fully turned on at any given time, which leads to a 71% additional power reduction. For example, only the first and second channels are fully turned on when a sample from the first channel is being digitized (Fig. 5.2). At the next clock cycle, when the ADC accesses the second channel, the first channel is turned off, and the third channel is turned on. In this technique, only the buffer to drive the analog multiplexer and the ADC are sequentially turned on, and the preamplifiers, which draw a very small current compared to the buffers, are always turned on.

For an electrode with resistance of 1MΩ operating at 27°C with a 20 kHz recording bandwidth, the RMS noise voltage is 18.2 μV according to Nyquist's formula. In general, the magnitude of extracellular spikes is less than 1mV, resulting in a 35dB signal-to-noise-ratio (SNR) of the input signal. With this estimated noise figure, we designed our ADC to have a 9-bit resolution with a conservative margin [10]. The sampling rate of one channel was chosen to be 40 ksample/s to avoid aggressive interpolation of spike samples and produced data rate as below:

$$40\text{ksample/s/channel} \times 128\text{channels} \times 9\text{bits/sample} = 46.08\text{Mbit/s}. \quad (5.1)$$

The 9-bit sampled data from eight front-end blocks are fed into digital data serializing circuits or a DSP engine for spike feature extraction according to the mode setting. The chip can operate in one of the two modes. In streaming mode, all the

sampled data from eight front-end blocks are fed into the digital data serializing circuits and serialized by the blocks, resulting in a 9-bit parallel digital data stream. This 9-bit data is expanded to a 16-bit data to include a 7-bit filler data for channel separation at the receiver side and is serialized again in the encoder. This final serialized data at the rate of 81.92Mbps is then Manchester coded at the UWB transmitter to generate UWB pulses, which are transmitted through an off-chip UWB antenna. A pulse-shaping filter is used to ensure that the emitted power spectrum of the UWB pulses is under the FCC regulation mask. When operating in the DSP mode, a selected channel is connected to the on-the-fly spike feature extraction block, and the features are transmitted wirelessly for further processing.

The clock signal of 81.92MHz is applied to the chip externally and the on-chip internal clock generation circuit provides appropriate clock signals for each circuit blocks, as shown in Fig. 5.1. In this design, we chose an off-chip crystal oscillator that can supply the required clock signal with a sufficient accuracy. The physical dimension of the commercial available crystal oscillator is small enough to be integrated with this chip in a hermetic sealing to form a higher-level system.

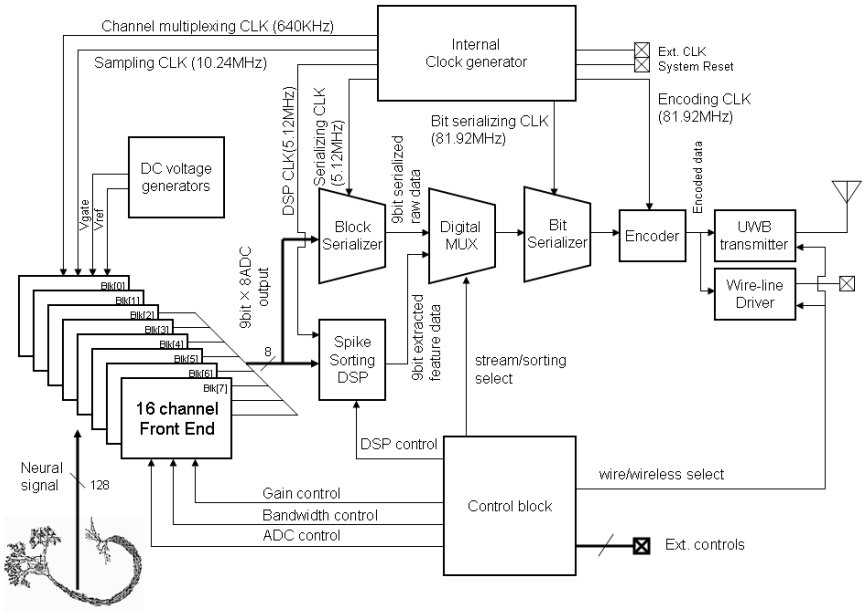

Fig. 5.1. Block diagram of the integrated neural recording system.

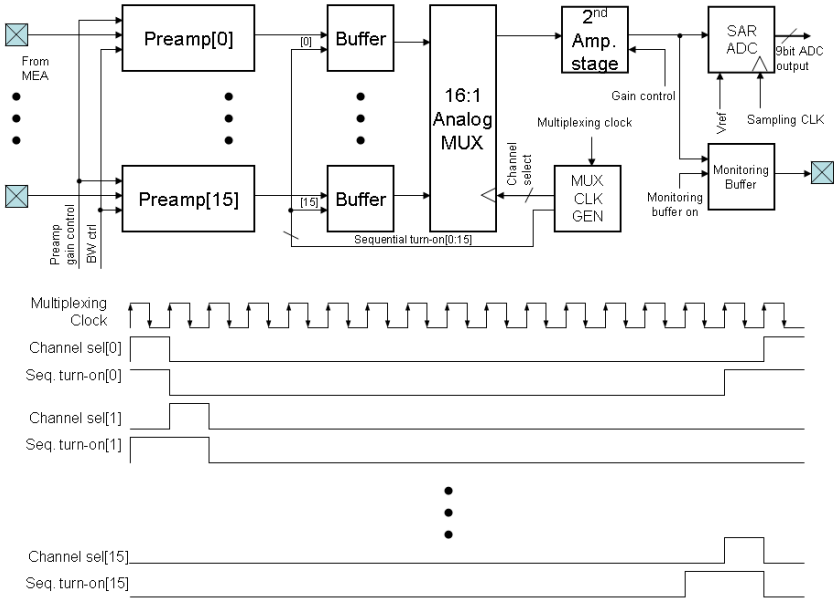

Fig. 5.2. Schematic of 16-channel front-end blocks (Sequential turn-on scheme is used to reduce the power consumption.).

5.2 Front-end Block Circuit Design

The preamplifier (Fig. 5.3) uses ac-coupling at the input to reject the large DC offset occurring at the electrode-tissue interface [29]. The gain of the preamplifier is 40dB, which is set by the ratio of feedback capacitances C_1/C_2. The second amplifier with a non-inverting resistive negative feedback provides an additional gain of 17dB to 20dB according to external controls. C_1 and C_2 were chosen to be 20pF and 200fF, resulting in differential input impedance of 16MΩ at 1kHz. The high-frequency roll-off of the preamplifier is configurable from 2kHz to 20 kHz in 16 steps by varying the load capacitance C_L. The low frequency roll-off is tunable from 0.1Hz to 200Hz by changing the gate voltage V_B of the NMOS used as bias resistors. The gate voltage provided by the bias generator is adjustable from 600mV to 1V by 50mV steps. The adjusting range and the step size of V_B are designed to achieve the target programmability of low frequency roll-off in the presence of the process variations.

Operational transconductance amplifiers (OTA) have critical effects on the overall performance of the preamplifier. A high common-mode rejection ratio (CMRR) is preferred to suppress the 60Hz power interference in the neural recordings [57], which makes the preamplifiers saturated and disables signal processing at the later stages of the system. A proposed fully differential self-biased OTA [14] shown in Fig. 5.3 enables a 90dB CMRR and an 80dB power supply rejection ratio (PSRR) with $4.9\mu V_{rms}$ input referred noise integrated from 0.1Hz to 20kHz. A fully differential output signaling was chosen to improve the common mode noise rejection. A common mode feedback (CMFB) circuit is not required because the

output common voltage level is self-biased by the negative feedback leading to the low power and small area of the preamplifier.

Each preamplifier and buffer draws 2μA and 20.3μA, respectively, to drive the analog multiplexer when it is turned on by the sequential turn-on control signals, leading to an average current of 2.54μA. The second amplifier draws 40.6μA to drive 10pF input sampling capacitance of the SAR ADC.

Care was taken to minimize the coupling noise from adjacent channels. All input signal lines that connect the inputs of the preamplifiers to bonding pads were shielded by quiet ground lines. In addition, the space between input signal line and shielding line was determined so that the metal parasitic capacitance is small enough to not affect the input impedance of the preamplifiers.

The total sampling capacitance of the SAR ADC is 10pF, and the power consumption is 14μW, which is very small compared to other analog circuits. The on-chip DC voltage generators supply the reference voltages, and the voltage levels are controlled by the external control signals, which are variable from 100mV to 500mV by 50mV steps.

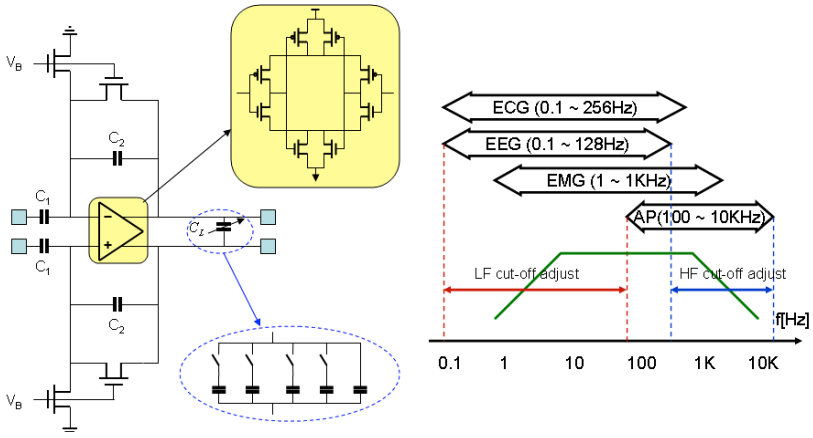

Fig. 5.3. Schematic of preamplifier and OTA used.

5.3 UWB Telemetry

Fig. 5.4 shows the block diagram of the UWB transmitter. The sampled and serialized data is Manchester encoded first, and then either on-off keying (OOK) or pulse-position modulation (PPM) is employed to generate short pulses. The redundant fillers are set to all "1" for channel<0> and all "0" for other channels in case of PPM, and the fillers for channel<0> are set to 7-bit 'logic low' of Manchester coding in case of OOK (Fig. 5.5). Therefore, the final maximum pulse repetition rate at the UWB transmitter output is twice the output data rate, 163.84 Mpulses/s in case of using PPM and the same as the output data rate, 81.92Mpulses/s for OOK. A short pulse generator is based on a simple edge detector [53], and the circuit implementation is shown in Fig. 5.4. The pulse width can be controlled to be from 180ps to 980ps by an external control voltage V_C for adjusting the transmitting power. The generated short pulses are then passed through a high-pass filter to

remove the low frequency component of the pulses and for the transmitting power to fit under the FCC emission mask. The filtered pulses are finally fed into the off-chip UWB antenna. The size of the antenna is small enough to be implantable or to be carried by the animals because of the high-frequency nature of the UWB.

The UWB receiver can be built from off-the-shelf components (Fig. 5.4), as it is outside the biological objects. The signal received by an UWB antenna is passed through 1GHz band-pass filter (BPF), whose center frequency is 4GHz, to remove the interfering signals from other narrowband wireless devices. The signal is then amplified by the low-noise amplifier (LNA) stages, which plays a critical role in determining the maximum distance between the implanted transmitter and receiver outside the biological subject. A RF diode and a low-pass filter (LPF) down convert the UWB signal to a low frequency by performing envelope detection, and the digital data is finally recovered by FGPA (Fig. 5.4).

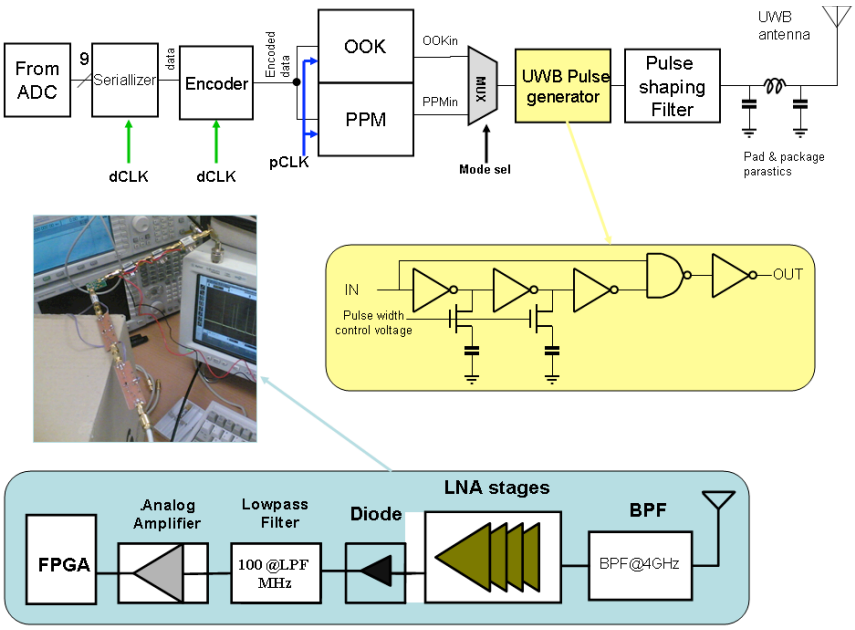

Fig. 5.4. Block diagram of on-chip UWB Tx, and UWB Rx with photo of its implementation using off-the-shelf components.

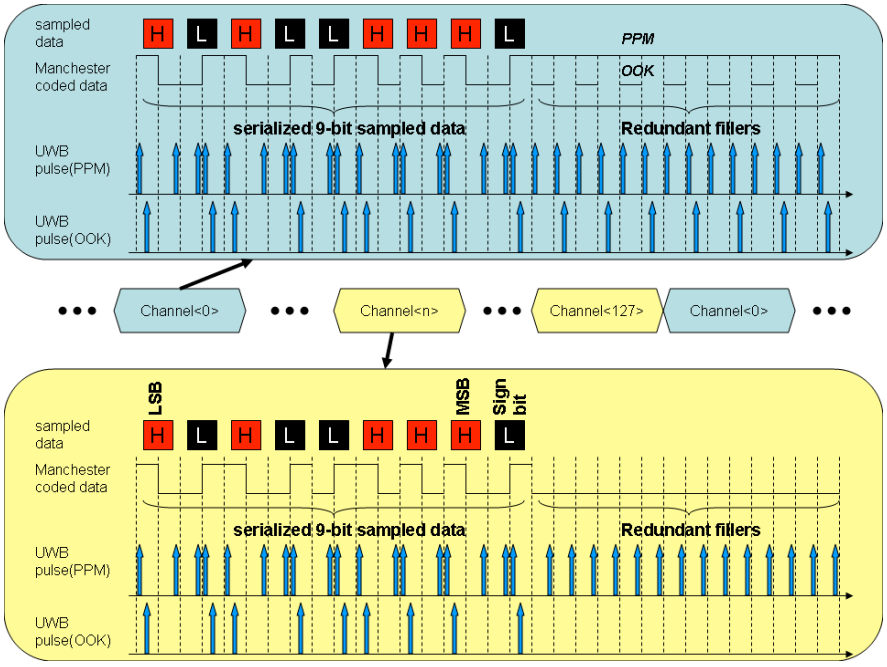

Fig. 5.5. Data format of the UWB transmitter.

Chapter 6

Chip Test Results

To verify the proposed concepts and ideas, four prototype chips were designed and fabricated. The first chip is a 4-channel analog front-end recording IC and has four preamplifiers, four filters, a 4:1 analog multiplexer, and an output buffer. The purpose of this first prototype chip is to verify the proposed amplifiers and filters that were explained extensively in Chapter 3. The second chip is a 16-channel neural recording IC. The IC was optimized by the design methodology proposed in Chapter 4. The third prototype chip is a CMOS IR-UWB Tx, whose operation and the circuit realizations were also presented in Chapter 4. The final chip is a 128-channel integrated neural recording IC with UWB telemetry, whose design is explained in detail in Chapter 5. The previous first, second, and third prototype chip designs were employed as subsystems and critical circuit blocks in this chip design. All chips were fabricated using National Semiconductor's 0.35μm CMOS process, and micro-photos of the chips are shown in Fig. 6.1, 6.2, 6.3, and 6.4, respectively.

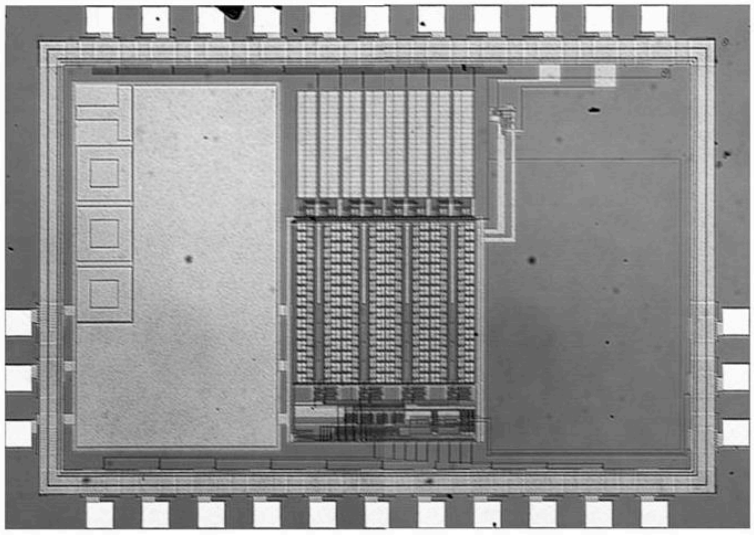

Fig. 6.1. Micro-photo of the 4-channel analog front-end recording IC.

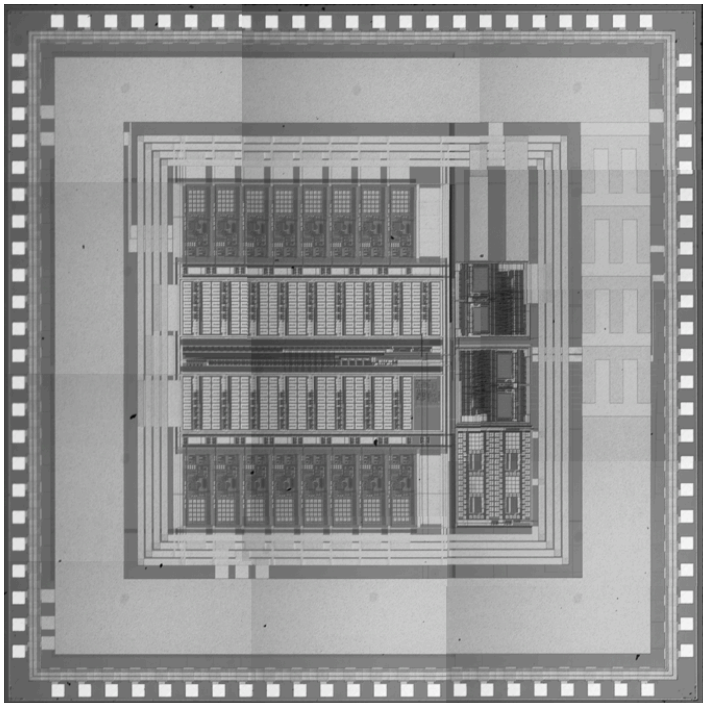

Fig. 6.2. Micro-photo of the 16-channel neural recording IC.

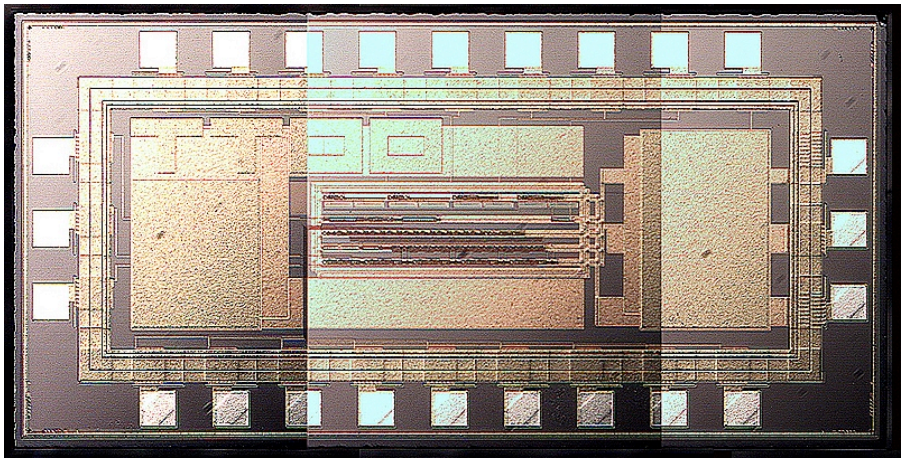

Fig. 6.3. Micro-photo of the CMOS IR-UWB Tx IC.

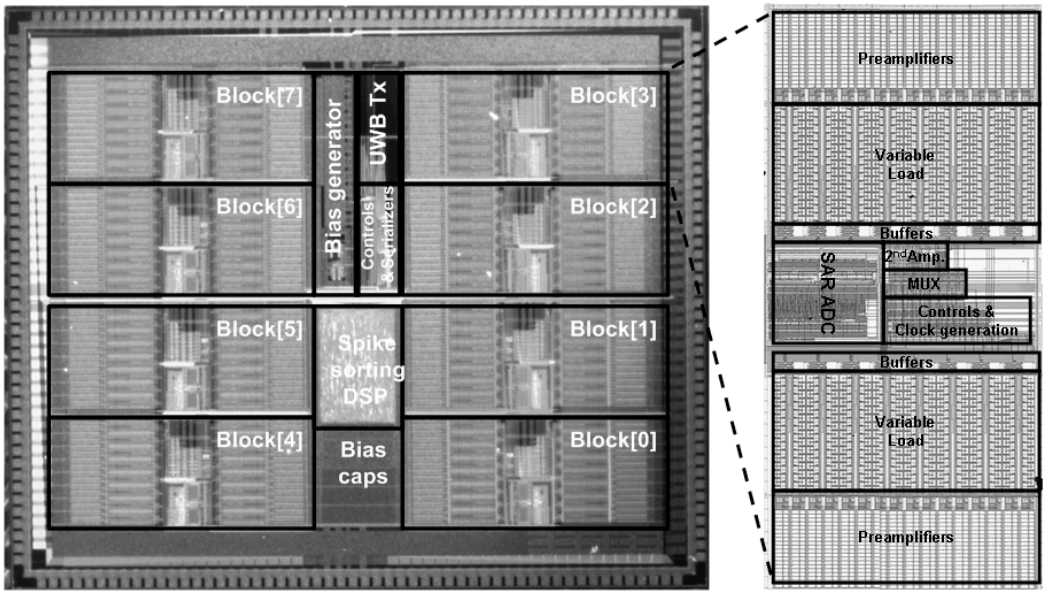

Fig. 6.4. Micro-photo of the 128-channel integrated neural recording IC with UWB telemetry.

6.1 Bench-top Tests

Bench-top tests were performed to verify the fabricated chip operation and to characterize the performances of each circuit block in the fabricated chips. As the first

(4-channel analog front-end chip), second (16-channel neural recording chip), and third prototype chip (CMOS IR-UWB Tx chip) designs were used as subsystems and critical circuit blocks in this chip design, all the prototype chips naturally show the same bench-top test results in terms of analog circuit performance, such as gain and bandwidth. Here are presented the bench-top test results of the final 128-channel neural recording IC, as a representative one in Table 6.1. The measured performances of the chips matched the simulation results within the process variations.

Table 6.1. Summary of bench-top test results of the fabricated chips.

Chip performance	
Number of channels	128
Signal gain of the preamp	40dB
Input impedance (at 1KHz)	16MΩ
Input referred noise	4.9μV_{rms}
CMRR of the preamp	90dB
PSRR of the preamp	80dB
LF roll-off of the preamp	0.1Hz ~ 200Hz *
HF roll-off of the preamp	2KHz ~ 20KHz *
Signal gain of the 2nd amp	17dB ~ 20dB *
ADC resolution	6 ~ 9 bits *
ADC sampling rate	640Ksample/sec
DSP's functionality	On-the-fly spike feature extraction for one selected channel
Power dissipated by DSP	0.1mW
Maximum UWB data rate	90Mbps
Power dissipated by UWB	1.6mW
Power supply level	±1.65V
Total chip power dissipation	6.0mW
Technology	0.35μm 4M2P CMOS
Total chip area	8.8mm ×7.2mm

* specification is programmable through external controls

Fig. 6.5 shows the waveforms obtained during the test of the prototype CMOS IR-UWB telemetry. The PSD of the UWB pulses generated by the UWB Tx is well below the FCC emission mask, confirming the proper operation of the UWB telemetry. The received data was verified to match with the test pattern fed to the UWB Tx in the chip, and its waveforms are also shown in Fig. 6.5. The Rx was implemented using off-chip components, and its photo is presented in Fig. 6.6.

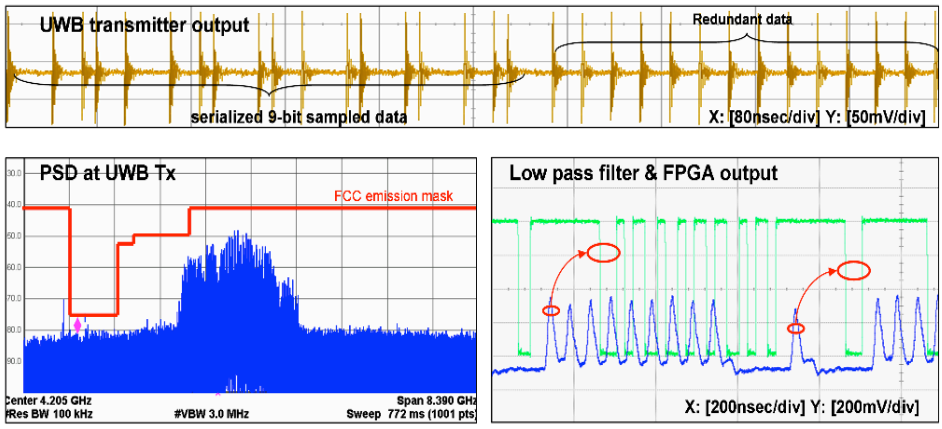

Fig. 6.5. Waveforms obtained during the integrated UWB telemetry test.

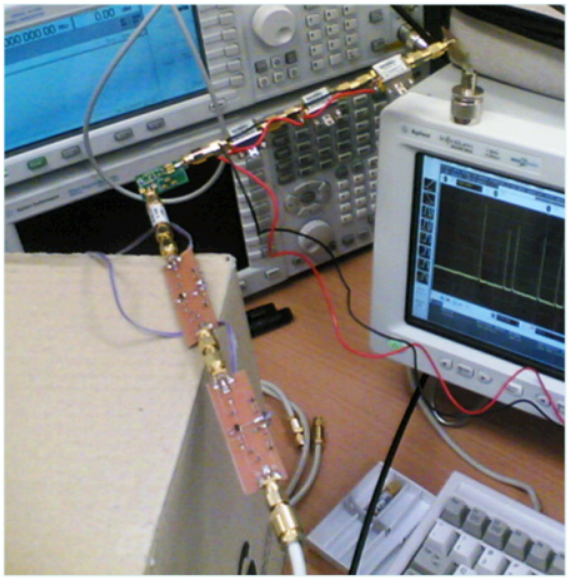

Fig. 6.6. Photo of the UWB Rx implemented using off-chip components. The Rx was fabricated in New Castle University, Australia and the whole UWB telemetry composed of Tx and Rx was tested both in New Castle University and UCSC.

6.2 Animal Tests

To verify the proper operation of the proposed system in real recording environments, *ex-vivo* and *in-vivo* recordings were performed in different biological objects. Human electroencephalographs (EEGs) and electrocardiograms (ECGs) were also recorded with the proposed systems.

6.2.1 *Ex-vivo* recording from a dissected snail brain

Ex-vivo extracellular recordings were obtained from an intact circumoesophageal ring dissected from H. Aspersa (Fig. 6.7 and Fig. 6.8). Specimens were prepared after cold 50mM MgCl anesthetization via a lateral slice. This allowed

removal of the intact circumoesophageal ring, which was subsequently rinsed and pinned out in Ringer's solution on a Sylgard coated dish. This preparation allowed control of extraneous noise sources to test the filtering capability of the chip and collection of several types of intracellular signals.

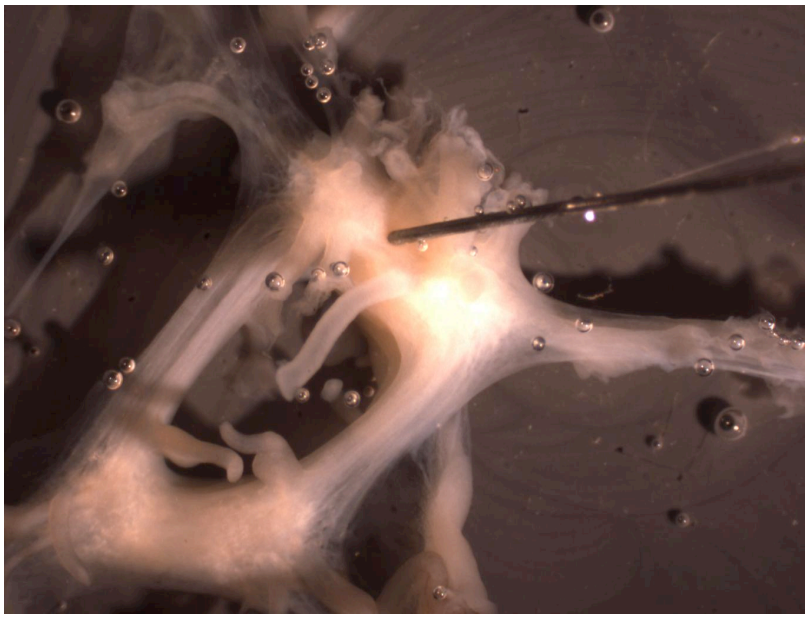

Fig. 6.7. Extracellular recordings from an intact circumesophogeal ring. Note the position of the electrode, external to the ganglion sheath, in between the pedal ganglia.

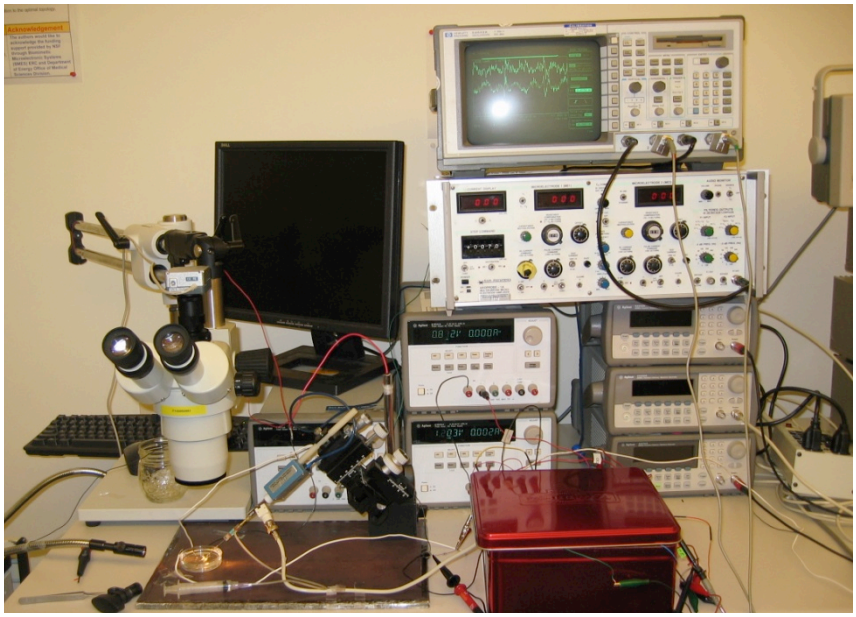

Fig. 6.8. Experimental Setup of *ex-vivo* recordings. All the electronic parts were placed in the metal box for shielding and isolation purpose.

The extracellular electrode is from FHC, Brunswick, ME (catalog 16-75-3), and is an ultra small concentric bipolar electrode with a 25µm platinum tip. The electrode impedance was measured as Z=190 kΩ (Randal equivalent circuit model of 639 pF and 327.7 kΩ) at 1 KHz with an HP4192A impedance analyzer. The chip used in this experiment was the 16-channel neural recording IC, shown in Fig. 6.2. As the experimental setup had only one recording electrode connected to one of 16 amplifiers, the chip was not operated in multiplexing mode, and the recordings were made at the output of the analog multiplexer bypassing the ADC. The built-in analog buffers driving the external oscilloscope for the signal storage accessed the output of the analog multiplexers. Fig. 6.9 shows various extracellular action potentials

recorded and stored by the experimental setup shown in Fig. 6.8. In this recording setup, all the electronic parts were placed in a metal box to shield the system from the external noise. The recording electrode and the coated glass dish that contained the Ringer's solution and the biological object were also placed on a thick metal plate for the shielding and isolation of the signal source from the noise.

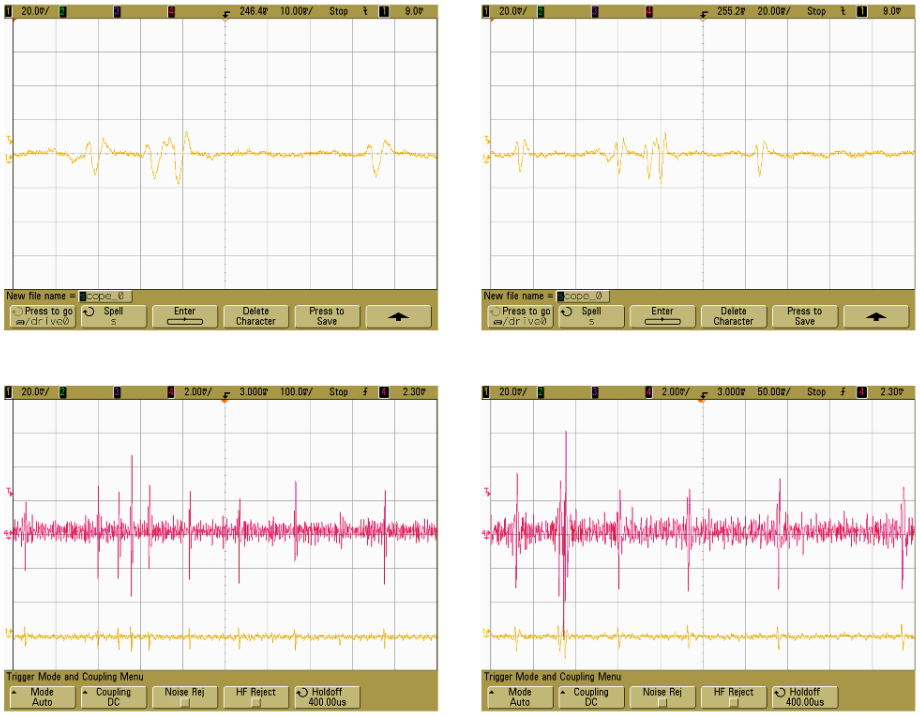

Fig. 6.9. Extracellular recordings from several different neurons.

6.2.2 *In-vivo* recording from a brain of live rat

In-vivo recording with a live rat was performed. For this experiment, a wireless neural recording system was implemented using the 4-channel analog front-end IC shown in Fig. 6.1 [60]. The block diagram and photo of the system used in the experiment is shown in Fig. 6.10.

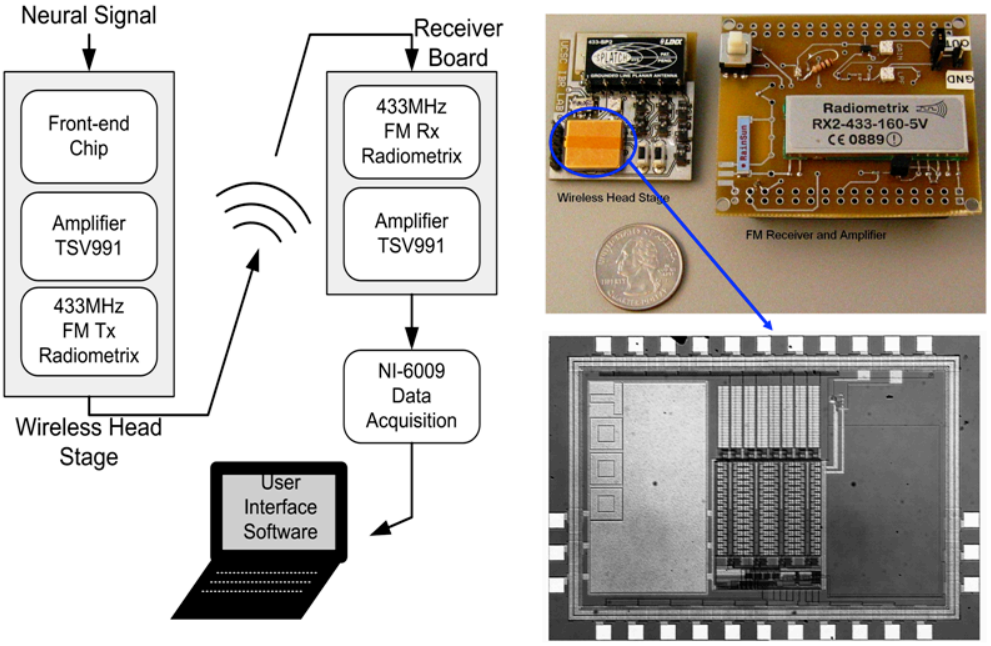

Fig. 6.10. Block diagram and photo of the recording system used in the experiment on the live rat.

The entire system can be separated into three major parts: wireless head stage, receiver board, and software user interface. Neural signals from the subjects are amplified and filtered by the custom IC. Then, one selected channel is connected to the FM transmitter through the control signal supplied by the on-board switches. The system did not have any on-board clock source to automatically control the analog multiplexer, thus the user has to push switches to reconfigure the system whenever there is a need to change the recording channel. The 433 MHz frequency modulation (FM) signal is transmitted via an antenna. At the receiver side, after demodulation, a low-pass filter is used to remove high frequency noises. As the AC output level of FM demodulator is only 400mV, an amplifier is used before the NI data acquisition

device for PC display captures the signal. A user interface software is programmed in LabView to display and record the captured data.

Fig. 6.11 shows a rat wearing the system with electrodes connected. A micro-wire electrode (Fig. 6.11) was used in the experiment and the measured impedance of the electrode was 100KΩ. The system successfully recorded the neural signal for two days. A part of the recorded signal is shown in Fig. 6.11.

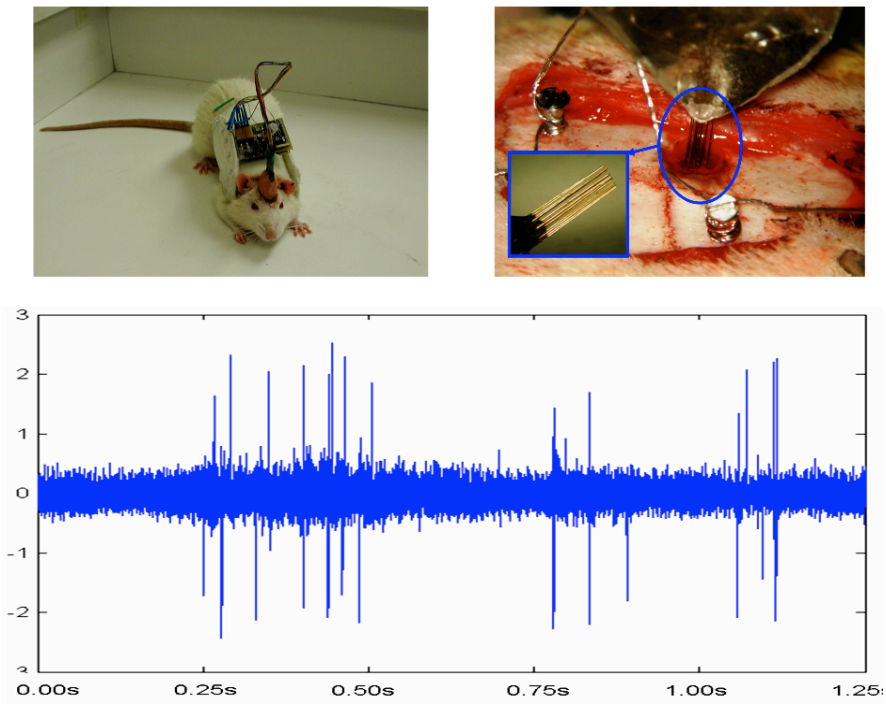

Fig. 6.11. A live rat wearing the recording system for in-vivo extracellular recording from the brain (top left). The microwire electrode implanted in the brain of a live rat (top right). Recorded neural signal from the live rat (bottom). Photos were taken at Arizona State University.

6.2.3 Human EEG recording

A 4-channel wireless neural recording system with the first prototype chip has been implemented and used in the human EEG recording experiments. The difference between this system and the one presented in the section 6.2.2 is that this system can simultaneously record all 4 channels, whereas the previous one can only select one channel out of four and monitor that selected channel until the user changes the configuration. The block diagram of the system is shown in Fig. 6.12.

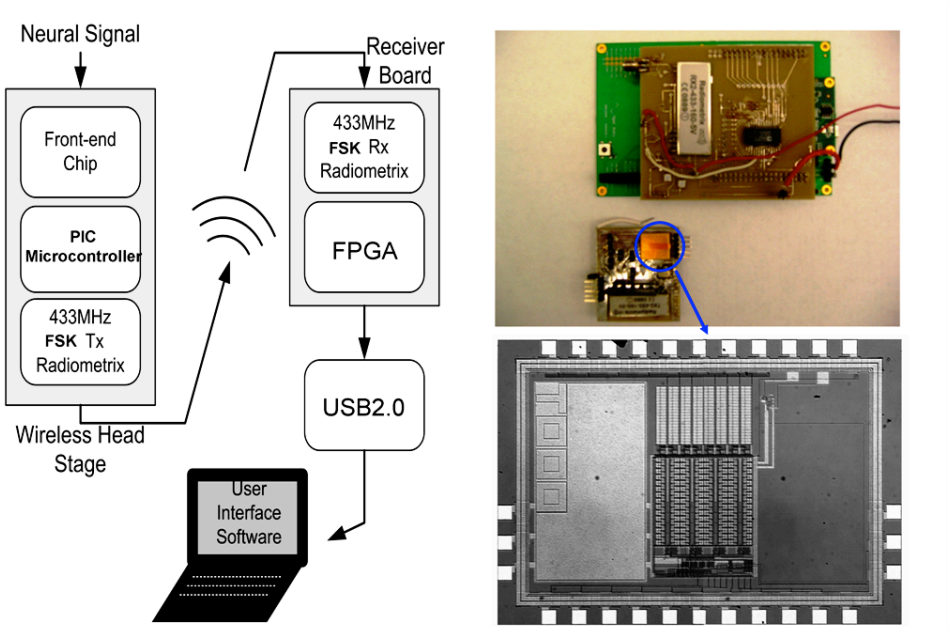

Fig. 6.12. Block diagram and photo of the recording system used in the experiment on human EEG recording.

The implemented system is composed of two parts: a wireless neural interface and a wireless receiver with a USB interface. The wireless neural interface consists of four EEG electrodes; an analog front-end that performs amplification, filtering, and

multiplexing; a microcontroller for the digitization and encoding of the recorded data; and a wireless transmitter. The four recording channels share one analog-to-digital converter (ADC) through time multiplexing to minimize the system size and power consumption. The sampling rate of the system is set to 500 samples/sec/channel, and the resolution of the ADC is 10 bits/sample. Since 6 bits are added to each sample as a frame header, the total data rate is 32 Kb/s (4 channels · 500 samples/sec/channel · 16 bits/sample). The microcontroller formats the data into a specific frame structure so that the receiver can easily identify samples from different channels. The frame structure consists of a 6-bit frame header for channel identification and data synchronization and a 10-bit frame body that contains the actual waveform information. Frame-structured digitized data is wirelessly transmitted to the receiver via a 433 MHz frequency-shift-keying (FSK) transmitter. The transmitted signal power level is maintained at a high enough level to eliminate the need for error-control coding, which can increase the system size and the power. The gain of the amplifiers is adjustable and initially configured to 1000. The bandwidth is also adjustable, and the low- and high- frequency cut-offs are set to 0.1Hz and 250Hz, respectively. A microcontroller (PIC12F615, Microchip) is used to digitize the time-multiplexed analog signal and encode for data framing. The encoded digital data is fed to the 433 MHz FSK transmitter chip (TX2-433, Radiometrix), which drives a 50Ω planar antenna (ANT433SP, Antenna Factor). The size of the wireless interface is $3.9 \cdot 4.4 \cdot 1.2 mm^3$ and has a total weight of 20g. The power source for the wireless interface is two 1.55V watch batteries, with a total power consumption of 28mW. The

wireless transmitter chip consumes most of the power, and the power consumed by the analog front-end chip and the microcontroller is negligible.

The real-time wireless receiver, which is connected to a PC via a high-speed USB interface, receives the wirelessly transmitted data from the wireless neural interface. The received signal is amplified first and demodulated by the radio frequency (RF) front-end producing baseband digital data. This digital bit stream is fed to a field-programmable gate array (FPGA) for the bit and frame synchronizations. After both bit and frame synchronizations are completed, the recovered data is transferred to the PC via the USB interface and stored.

The wireless receiver was built using a commercial RF front-end chip (RX2-433, Radiometrix) and a compact integration board (XEM3005, Opal-Kelly) featuring the Xilinx Spartan-3E FPGA and onboard SDRAMs. As the receiver is located away from the object, and the physical size of the receiver is relatively less important than that of the wireless interface carried by the object, we adopted a conventional rod-type antenna in the receiver to maximize the system performance. 5V power is supplied from the PC to the receiver through the USB interface. Fig. 6.13 shows a photo of a person who is wearing the implemented recording system and part of the recorded waveforms.

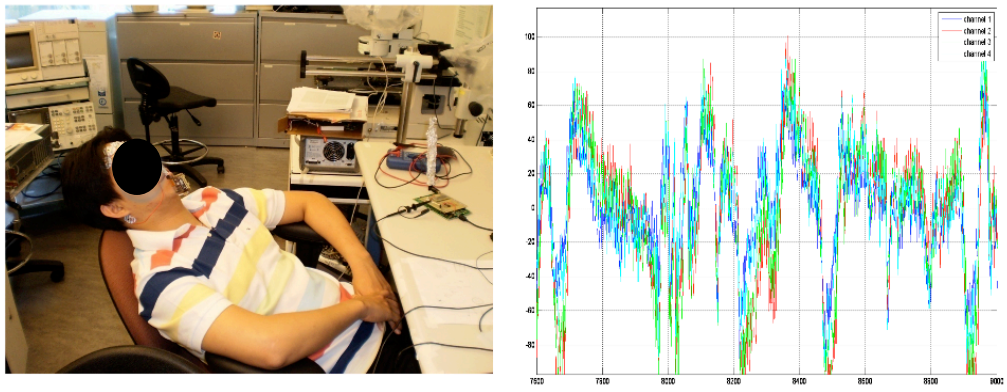

Fig. 6.13. A person wearing the system for EEG recording (left) and obtained EEG signal (right).

6.2.4 Human ECG recording

Human ECG was also recorded with the same system presented in the previous chapter, with adjustments of the gain and bandwidth. Fig. 6.14 shows recorded ECG waveforms. The PQRST features were clearly identified in the experiments.

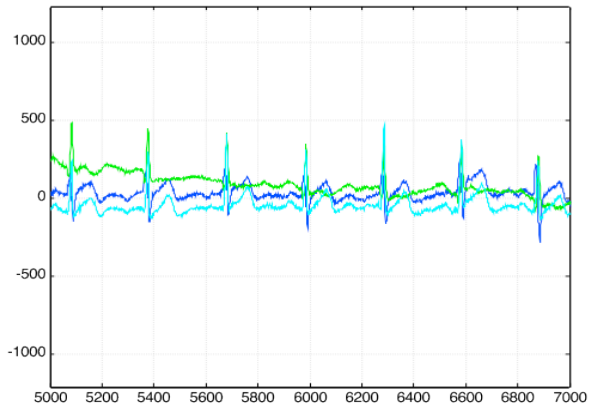

Fig. 6.14. Obtained ECG signal with the implemented recording system.

Chapter 7

Conclusions

The design methodology for the integrated neural recording system and the integrated wireless neural recording ICs have been presented with test results.

The neural recording system has requirements and constraints imposed by the unique operating environments, which are significantly different from other pure electronics-oriented applications. Thus system designers need to consider those constraints collectively and determine the optimal system parameters, rather than solely focus on achieving the best state-of-the-art performance in each circuit block.

A novel fully-differential and self-biased amplifier and filters with Miller capacitance technique have been proposed and experimentally verified. The parameters of the circuits were optimized so that the overall product of the system power and area is minimal. An analysis on the crosstalk between recording channels have been performed and the system architecture was also optimized by the design methodology proposed in this thesis.

UWB telemetry has been proposed for simultaneous wireless transfer of the recorded data from more than 100 recording channels. Theoretical analysis of the UWB pulse generation and circuit implementation of the integrated CMOS UWB TX have been discussed. Implementation of the UWB RX using off-chip components has also been explained.

A 4-channel analog front-end chip, a 16-channel neural recording IC, a CMOS IR-UWB TX chip, and a 128-channel neural recording IC with UWB telemetry have been fabricated using a 0.35μm CMOS process and tested both on the bench-top and in animals. The measured performances of these chips matched simulation results and were verified under different testing conditions.

The sequential turn-on method is used to minimize the power consumption of the front-end blocks, which are the most power-consuming circuits. Wireless transmission at a high data rate was achieved through a low-power implantable UWB wireless transmitter. The total power consumption is only 6mW even for transmitting raw data from all 128 channels. The front-end has been designed for amplifiers to have programmable gains and bandwidth to offer flexibility in recording various bio-potentials.

Experiments with different real biological objects have been performed to verify the overall operation of the fabricated chips. Ex-vivo extracellular recording from a dissected snail brain, in-vivo extracellular recording from the brain of a live rat, in-vitro extracellular recording from MEAs with cultured snail neurons, and human EEG and ECG recordings have been verified with the fabricated chips.

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