Title

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A 0.66 W/mm² Power Density, 92.4% Peak Efficiency Hybrid Converter with nH-Scale Inductors for 12 V System

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As passive components play a critical role in determining the overall footprint of power management solutions, significant efforts have been put into new converter topologies, operating principles, and packaging techniques aimed at reducing the size of passive components [1]–[5]. To achieve these goals, one can increase the effective switching frequency [3]–[5], or use hybrid converter topologies and/or resonant operation to better utilize inductors and capacitors for power transfer. Packaging that prioritizes close proximity and low parasitics is also of particular interest [5]. Starting from the preliminary discrete-circuit implementation in [6], this work strives to achieve the high-density goals based on a new integrated hybrid converter topology and operation, high switching frequency, and advanced packaging, which collectively enable the use of nano-Henry scale inductors. The prototype is fabricated in 3.23 mm² of a 1P6M 0.13 μm BCD process (Die micrograph).

Fig. 1 shows a block diagram and power stage topology of the new converter design. The control blocks include 4 linear regulators (LRs); an output voltage regulator comprised of an error amplifier (EA), a new ramp generator (RG), a phase-shift modulator (PSM) and a tunable non-overlapped signal generator (SG); current biasing circuits; and a serial-interfaced programing register for tuning. In order to reduce the required inductance to 10 nH, which is 3.6X lower than the lowest inductance used in the resonant switched-capacitor (ReSC) converter demonstrated in [2], the power stage employs a new Integrated Transformer-less Stacked Active Bridge (ITSAB) converter. The converter die is flip-chipped onto a compact 6.5 mm x 6.5 mm package substrate with IPD inductors L1, L3, flying capacitors C1-C3, input/output capacitors Cin/Co, and decoupling capacitors for the LRs as shown in Fig. 1.

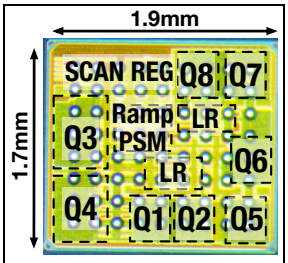
The operation of the ITSAB converter can be divided into 4 time-intervals as illustrated in Fig. 2. The operation of the switched capacitors (SC) resembles that of a Dickson-star SC converter, ensuring the steady-state voltages across C1, C2, and C3 are $3Vin/4$, $2Vin/4$, and $Vin/4$, respectively. Unique to this ITSAB converter, the inductors have ideally flat-top current waveforms with magnitude of $Io/2$ in State 1 and 3 as the capacitors are connected such that the voltages across the inductors are close to zero. The inductor currents flip directions during State 2(4) when they are discharged (charged) by $Vin/4$. Duration of State 2 and 4, t_Φ, is the phase shift between the 50% duty-cycle control signals Φ_S-Φ_{Sb} and Φ-Φ_b. Unlike the ReSC converter in [2], the passive component values are selected to ensure that the time constant formed by L1 (L3) and C1-C2 (C3-C2) is well above the switching period Ts across all operating points so that the converter operates in inductive mode. Thus, the current shape is close to a trapezoid with zero average value and RMS at ~$Io/2$. From charge balance it follows that

$$\mathrm{Io} = (\mathrm{Vin}/8\mathrm{Lf_s}) * \Phi(1-\Phi) \quad (1)$$

where $\Phi = 2t_\Phi/T_s$ is the phase shift. Therefore, by modulating t_Φ, Io and thus the output voltage Vo can be regulated.

As illustrated in Fig. 3 (top left), when the deadtime of Φ_S-Φ_{Sb} is properly designed, Q3 and Q4 can achieve full zero-voltage switching as inductor currents $I_{L1,3}$ flip directions during State 2 and 4. In addition, Q5-8 experience partial ZVS. Therefore, the ITSAB converter can operate at more than 2X of the resonant frequency determined by L1(L3) and C1(C3) while achieving high efficiency.

The circuit structures of RG and PSM along with a simplified timing diagram are provided in Fig. 3. The ITSAB converter is unique in that the full output regulation only requires a phase shift within ~25% as derived from Eq. 1. Therefore, while a regular sawtooth waveform, which is generated between zero and VH reference voltage, is needed for frequency generation, directly using this signal for PSM would result in poor immunity to high frequency noise. To overcome this issue, RG utilizes a second branch to generate the ramp_pre signal with 2X charging current for 2X ramp slope, followed by a source follower to position the final ramp signal in the range with the error voltage m and input common-mode of the PSM comparator CMP. Signal ramp_pre is also used to generate max_Φ_S, which determine the phase-shift upper limit (~25%). CMP's output largely defines t_Φ. A short delay is added to the clk signal path for Φ such that a phase shift offset is included in t_Φ, which improves light load regulation, and compensates possible delay mismatches between signal paths. Masked by clk_half(_bar) generated from a half counter, Φ and Φ_S always maintain 50% duty-cycle.



Die micrograph.

The table in Fig. 4 details the source and gate voltage levels in all operating states, which guide the strategy for designing the LRs at appropriate voltages. VSS8 and VSSL7 are generated by Subtraction LRs. Since the voltage relationship (VSS8 > VSSL7 > Vo) is always maintained with enough voltage headroom for the LR's pass transistors, the two Subtraction LRs are stacked in series to Vo to enable current reuse and reduce LRs' voltage overheads and associated losses. In a similar manner, the Summation LR circuit is utilized to generate VDD5 or VDDH6, using suitable resistors and operational amplifiers as detailed in Fig. 4 (top-right).

Fig. 4 (bottom) depicts an independently controlled push-pull gate driver for high-side switches Q4-Q7 that require large gate voltage swings across two voltage domains, VDDH-VDDM and VDDM-VSSH. The values of these voltage levels for gate drivers GDx are labeled with the same color scheme in Fig. 1. Stacked thin-ox devices M1-M4 are used to improve the gate driver's speed and size. Shoot-through current in M1-M4 is minimized using a dedicated non-overlap SG. The level shifter shown in Fig. 4 (bottom-right) is used to provide the push and pull signals at high voltage domains. In this level shifter, MIM capacitors are used to couple signals between different domains with minimal latency while keeping small area. The cross-coupled inverters at the high voltage domain employ weak NMOS transistors to ensure rail-to-rail operation.

The ball-grid-array (BGA) package substrate that houses the converter die and the passive devices is soldered on PCB for testing. To capture the currents $I_{L1,3}$, 10 nH inductors are replaced by two identical wires (~74 nH each) as shown in Fig. 5. Waveforms are captured at 9.6V input, 2.38 V/1 A output, and f_s=3 MHz. 0.5 A load transient test is performed at 50 mA/μs transient rate to verify the regulation and loop stability. 50 mV (40 mV) undershoot (overshoot), 80 μs (60 μs) setting time are observed during the step-up (step-down) transient. The converter efficiency is measured and evaluated at different regulated voltage levels over wide ranges of output currents, switching frequencies, and two input voltages of 9.6 V and 12 V, as shown in Fig. 6 (top). Compared to prior state-of-the-art designs in Fig. 6, the proposed converter achieves comparable efficiency and an outstanding power density of 0.66 W/mm², while using inductors that are 3.6X to 56X smaller than prior works for a similar input voltage range.

References:

[1] K. Wei *et al.*, "A Direct 12V/24V-to-1V 3W 91.2%-Efficiency Tri-State DSD Power Converter with Online VCF Rebalancing and In-Situ Precharge Rate Regulation," *ISSCC*, Feb. 2020

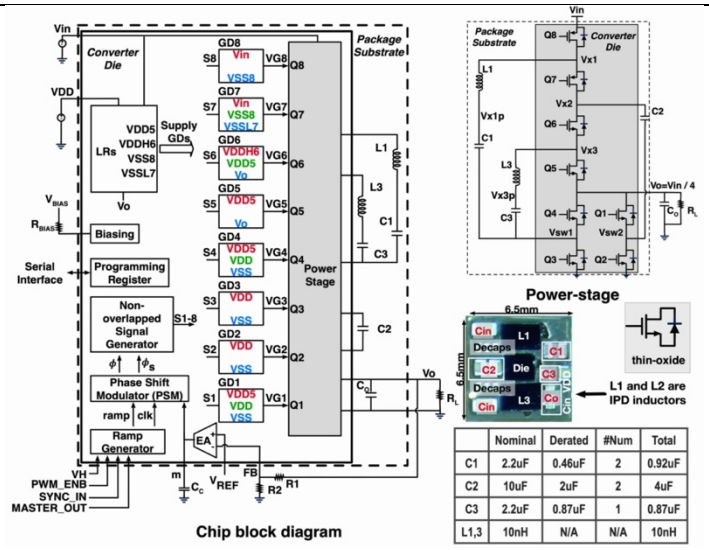
[2] C. Schaef *et al.*, "A Highly Integrated Series–Parallel Switched-Capacitor Converter With 12 V Input and Quasi-Resonant Voltage-Mode Regulation," *JESTPE*, Jun. 2018

[3] C. Hardy *et al.*, "A Flying-Inductor Hybrid DC–DC Converter for 1-Cell and 2-Cell Smart-Cable Battery Chargers," *JSSC*, Dec. 2019

[4] W.-C. Liu *et al.*, "A 94.2%-peak-efficiency 1.53A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65nm CMOS," *ISSCC*, 2017

[5] Z. Xia *et al.*, "A Two-Stage Cascaded Hybrid Switched-Capacitor DC-DC Converter with 96.9% Peak Efficiency Tolerating 0.6V/μs Input Slew Rate During Startup," *ISSCC*, Feb. 2021

[6] J. Zhu *et al.*, "A Family of Transformerless Stacked Active Bridge Converters," *APEC*, Mar. 2019



	Nominal	Derated	#Num	Total
C1	2.2uF	0.46uF	2	0.92uF
C2	10uF	2uF	2	4uF
C3	2.2uF	0.87uF	1	0.87uF
L1,3	10nH	N/A	N/A	10nH

Fig. 1. Block diagram and power-stage topology of the new Integrated Transformer-less Stacked Active Bridge (ITSAB) converter. (Bottom right) Package with IPD inductor

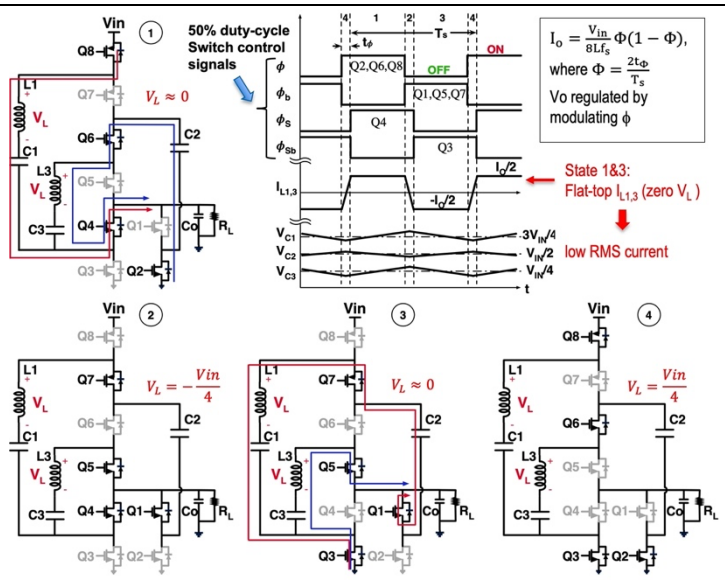


Fig. 2. Power stage operation and timing diagram of the ITSAB converter

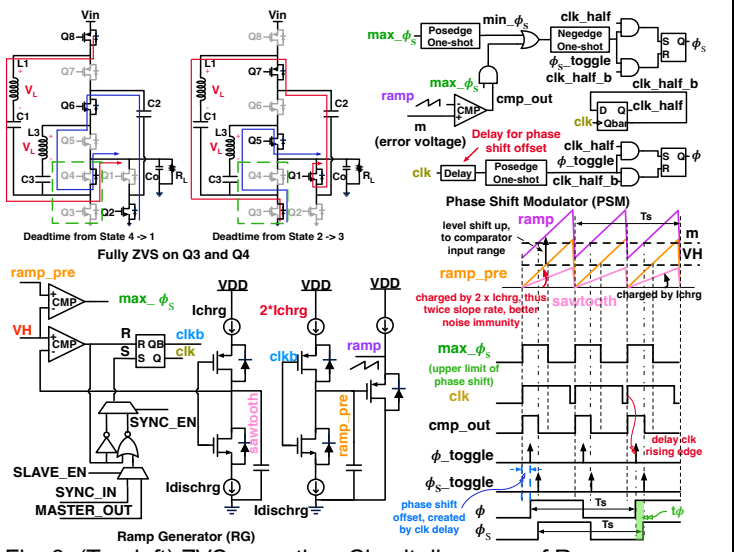


Fig. 3. (Top left) ZVS operation. Circuit diagrams of Ramp Generator (Bottom left) and Phase Shift Modulator (Top right), and their timing diagram (Bottom right)

Switch	Source Voltage		Gate Voltage	
	ON	OFF	Low swing	High swing
Q8	Vin (9.6V)	Vin (9.6V)	VSS8 (6V) (Vin-VDD)	Vin (9.6V)
Q7	0.75Vin (7.2V)	Vin (9.6V)	VSSL7 (3.6V) (VSS8-Vo)	Vin (9.6V)
Q6	0.5Vin (4.8V)	0.25Vin (2.4V)	Vo (2.4V)	VDDH6 (8.4V) (VDD5+Vo)
Q5	0.25Vin (2.4V)	0.25Vin (2.4V)	Vo (2.4V)	VDD5 (6V) (VDD+Vo)
Q1,4	0.25Vin (2.4V)	GND (0V)	GND (0V)	VDD5 (6V) (VDD+Vo)
Q2,3	GND (0V)	GND (0V)	GND (0V)	VDD (3.6V)

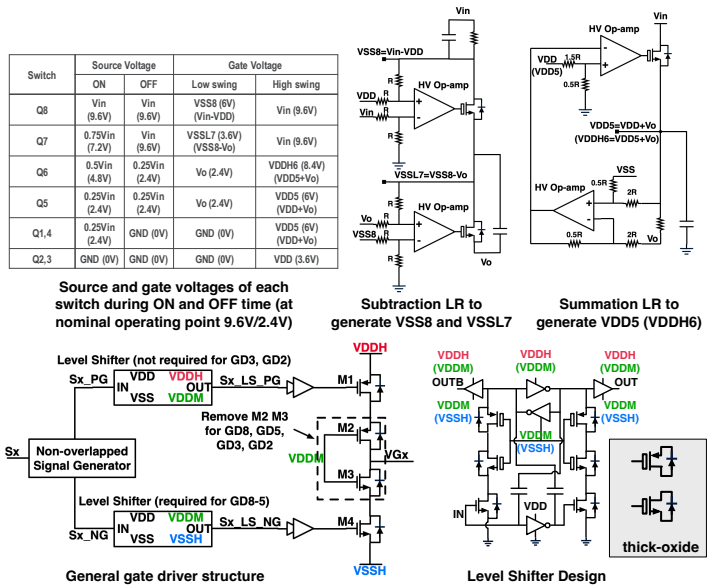


Fig. 4. Gate driving strategy with LRs, level shifter and gate drivers

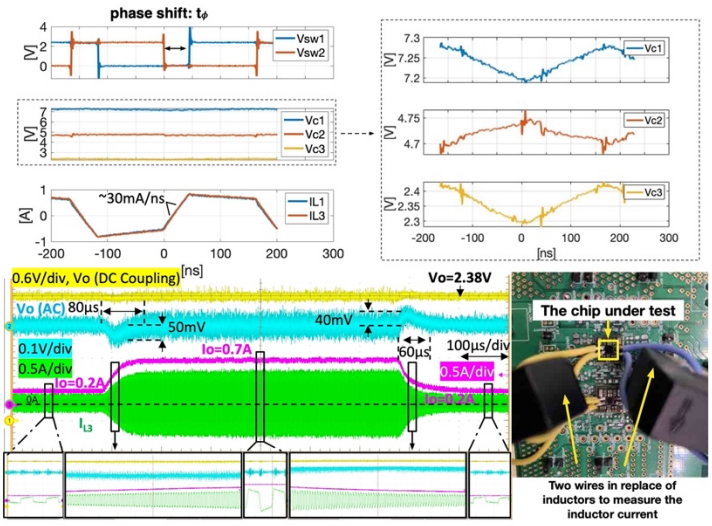
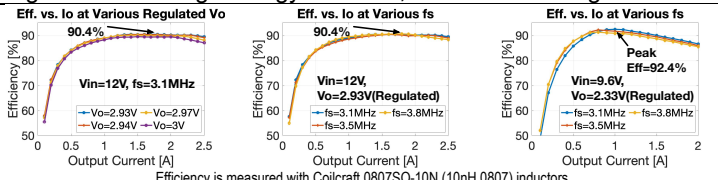


Fig. 5. (Top) Measured 9.6V/2.38V-1A steady-state operation waveforms using two identical wires (~74nH each). (Bottom) Load transient test (0.2A -> 0.7A -> 0.2A) and its testbench.



	This Work	[1]	[2]	[3]	[4]	[5]
Topology	**ITSAB**	Tri-State DSD	3:1 ReSC	Hybrid SC	Hybrid Dickson	Cascade Hybrid
Technology	**130nm**	180nm	180nm	130nm	65nm	180nm
Inductor	**2x10nH**	2x560nH	36nH	1uH	180nH	240nH
Tested Inductor Switching Frequency	**2-5MHz**	200k-2MHz	1.7MHz	2.3MHz	400k-10MHz	1.5MHz*
Input Voltage (Vin)	Vin≥9V				Vin<9V	
	9.6-12V	12V/24V	12V	9V	3-4.5V	4-6V
Output Voltage (Vo)	**2.3-3.2V**	1V	3.5-3.8V	3-4.2V	0.3-1V	0.4-1.2V
Peak Output Current	**2.5A**	3A	1.24A*	3.4A	1.53A	1A
Power Density** [W/mm2] @ CR	**0.66*** @ 4.1**	0.08@12	0.38 @ 3.4	0.4 @ 2.7	0.13 @ 5.2	0.1 @ 4.5
Efficiency @ CR	**92.4% @ 4.12**	91.2% @ 12	82% @ 3.4	94.3% @2.5	88.3% @ 5.2	96.9% @4.2
Regulation Method	**Phase shift modulation**	Duty cycle	Deadtime control	Duty cycle	Duty cycle	Ripple Injection

*Estimated from reported measurement results
***Assuming 0807 package inductor
**Area counts active die, flying capacitors and inductors only. Calculated at given conversion ratio (CR)=Vin/Vo.

Fig. 6. (Top) Measured efficiency at different conditions. (Bottom) Comparison with prior arts.