# Designs of Fully On-chip Antennas in (Bi)CMOS Technology

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**ABSTRACT:** The paper presents several feasible millimeter wave on-chip antenna designs suitable to be fabricated in CMOS technology without any additional process. The results are listed and compared with state-of-the-art designs in the literature. The difficulties in designing high efficiency antenna on CMOS chip are discussed.

## INTRODUCTION

CMOS technology has been proven as an effective platform for low power millimeter wave (mmWave) transceiver systems. For near-future applications of mmWave receivers with on-chip antennas (OCAs), such as mmWave imaging and multi-gigabit-per-second short range wireless communications, it is strongly desirable to achieve high efficiency antennas, which would lead to integrated systems with efficiency much higher than the current state of the art. In terms of bandwidth, a wideband antenna performance is also required. Besides, for the purpose of cost, a miniaturized size is also a prerequisite for on-chip antenna.

However, it is very challenging to achieve a high gain, wide band and high efficiency on-chip antenna by CMOS technology. Antenna radiating above a lossy silicon substrate usually results in very low radiation efficiency. Another concern is the electromagnetic interference (EMI) phenomenon when antenna and front-end are in proximity range and sharing the same substrate [1]. To alleviate these problems, a ground plane at lower metal layer inside CMOS (e.g., M1, the lowest metal layer) is preferable to stop the wave travelling inside the lossy silicon and hereby suppress the EMI. However, since the extremely thin total thickness of silicon dioxide (typically around 1% guided wavelength in silicon dioxide), a ground plane at M1 strongly limits the antenna substrate thickness and therefore limits the bandwidth, and meanwhile ohmic losses get much stronger so that the antenna radiation efficiency gets strongly degraded.

In this review paper, several proposed on-chip antenna designs are shown and the results are organized in Table 1 to compare some of our work to the state-of-the-art CMOS on-chip antennas in the literature. Based on the results, it can be observed that on-chip antenna design without extra process, with a ground plane below silicon and a ground plane at M1 (inside silicon dioxide) will provide more and less similar gain level and the latter case implies a narrower bandwidth. The designs of lens-based antenna [2, 3], superstrate antenna [4], and through-substrate-via (TSV) based antenna [5] show high gain but require extra process and/or exhibit bulky sizes. In [6, 7], the potential to use high impedance surface (HIS) or artificial magnetic conductor (AMC) for OCA application was explored. In [6, 8], it was reported that in addition to placing HIS below a dipole antenna to act as a reflection layer, HIS could also be excited as a radiator directly by means of the leaky mode property inside the structure.

## PROPOSED CMOS ON-CHIP ANTENNA

Several high performance on-chip antennas have been investigated at the authors' institution, shown in [6, 9, 10]. Their configurations are shown in Fig.1 and Fig.2 and their main results are summarized and organized in Table.1. Fig.1 (a) shows the micrograph of a bowtie slot antenna fabricated in 180 nm BiCMOS process. The bowtie slot antenna is placed at top metal layer (M6) and with a ground plane below silicon substrate. The measured results of the bowtie antenna show a very wide bandwidth, covering the most of the W-band (from 70 GHz to 110 GHz).

Fig.1 (b) and (c) show the top view and side view of a cavity backed slot antenna fed by a microstrip line. The cavity is composed by top and bottom metal layer (M6 and M1) and vias in between. The cavity functions not only as a shielding structure to prevent the overwhelming dielectric loss in silicon but also enhance the slot antenna radiation. The slot antenna is fed by the microstrip line directly and also by the $TE_{110}$ cavity mode. It was concluded that when properly choosing the location of the slot, the two feeding mechanism would be constructive and improve the antenna gain.

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Fig.1 (d) shows the top view of an extremely flat E-shape patch antenna. The patch antenna is located at M6 and has a ground plane at M1. The bandwidth of the patch antenna is enhanced by creating an additional resonance due to the two notches. Despite the extremely thin antenna substrate (9.6 µm), a 13 GHz bandwidth has been achieved for a 94 GHz E-shape patch design. Also, among W-band antennas listed in Table.1, the E-shape patch antenna has the smallest area usage, which is abstracting in terms of cost. Fig.1 (e) shows a slot antenna over an extremely thin substrate integrated waveguide. The waveguide is realized between M1 and M6, and vias in between, which is similar to the cavity in Fig.1 (c). A taping shape microstrip is used to match the 50 ohm microstrip line with the waveguide.

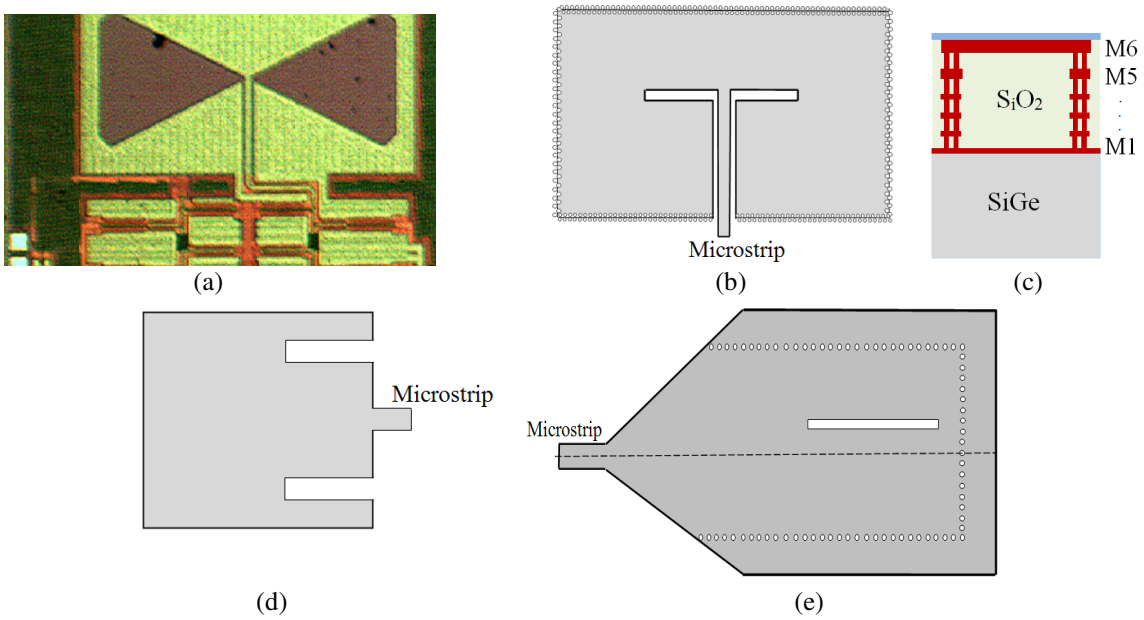


**Fig. 1 (a) Micrograph of bowtie antenna; (b) top view of extremely flat (9.6 µm) cavity backed slot antenna; (c) side view of the extremely flat cavity backed slot antenna; (d) top view of the extremely flat E-shape patch antenna; (e) top view of an extremely flat substrate integrated waveguide antenna. Designs (b)-(e) are extremely flat because they have a ground plan at M1.**

The configuration of using HIS in CMOS OCA design is shown in Fig.2. Fig.2 (a) shows the design of HIS below a dipole antenna, by patterning M1. The ground of the HIS is placed below the Si-Ge layer. The HIS is acting as an artificial magnetic conductor (AMC) at the designed frequency band. In [6], it was also reported that HIS could be fed directly as radiator without dipole on the top. The HIS is located at top metal layer M6, with a ground plane at M1. As explained in [8], a TM-like leaky mode is excited inside the HIS with a large attenuation constant, which is due to the strong ohmic losses. And because of the large attenuation constant, only a small numbers of periodic elements are employed in the antenna design, which is different from traditional large number of elements in highly directive leaky wave antennas.

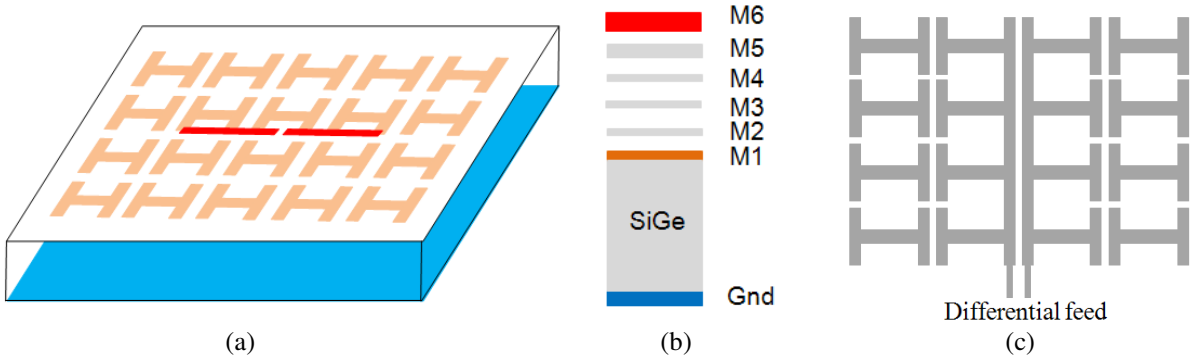


**Fig. 2 (a) Dipole antenna above HIS (b) side view of dipole over HIS (c) top view of HIS antenna without dipole**

The performance of all the antennas mentioned above and state-of-the-art OCAs is listed in Table 1, including the antenna size, operating frequency, bandwidth and peak gain. According to Table 1, off-chip antennas (i.e., antennas that requires extra process off-chip), especially antennas with lens, exhibit much higher gain. Novel designs should be investigated to improve the gain and gain bandwidth of on-chip antennas and achieve a wider bandwidth for on-chip antennas with extra process.

**Tab. 1 Performance of proposed (Bi)CMOS on-chip antennas and other state-of-the-art work**

| **Our work** | | | | | | |
|---|---|---|---|---|---|---|
| | Freq. (GHz) | Chip area (mm × mm) | Gain (dBi) | -10dB input BW (GHz) | Fully on-chip | Isolation with circuits |
| Bowtie slot [9] | 94 | 1.4 × 0.9 | 1 (mea.) | 40 (mea.) | Yes | No |
| Cavity backed slot [10] | 140 | 1.2 × 0.6 | -2 (sim.) | 7 (sim.) | Yes | Yes |
| E shape patch [9] | 140 | 0.7 × 0.7 | -2 (sim.) | 10 (sim.) | Yes | Yes |
| E shape patch | 94 | 1.2 × 0.8 | -3 (sim.) | 13 (sim.) | Yes | Yes |
| HIS antenna with dipole [6] | 94 | 2.2 × 1.2 | 1 (sim.) | 12 (sim.) | Yes | No |
| HIS antenna w/o dipole [6] | 140 | 1.4 × 0.9 | - 1.5 (sim.) | 12 (sim.) | Yes | Yes |
| Waveguide slot [9] | 140 | 2 × 0.6 | 0 (sim.) | 5 (sim.) | Yes | Yes |
| **Examples of state-of-the-art work** | | | | | | |
| Patch fed by TSV [5] | 110 | N/A | -3 (mea.) | 10 (mea.) | Yes | No |
| Patch with ground at M4 [11] | 60 | 1.22 × 1.58 | -3.23 (mea.) | 0.81(mea.) | Yes | Yes |
| Slot with lens [2] | 90 | 1.8 × 1.4 | - 5.7 (mea.) w/o lens 15 (sim.) w/ lens | 4 GHz | No | Yes |
| Dipole with lens [3] | 60 | NA | 8 (mea.) | NA | No | No |
| Patch with superstrate [4] | 94 | 1.6 × 1 | 3 (mea.) | 6 (mea.) | No | Yes |

## ON-CHIP ANTENNA RADIATION MEASUREMENT

Measurement of on-chip antenna gain and radiation pattern is challenging due to several constraints. One of the difficulties is that the antenna feed probe has to be in the very proximity near-field range of the OCA. For off-chip antenna (e.g., antenna in package), this issue could be avoided by feeding the antenna in the backside of the antenna main beam. Figure 3 shows our setup for the antenna gain measurement. For the figure visibility, the absorbers are removed in the range around the probe station. A signal generator drives a ×6 frequency multiplier, providing the W-band power to a transmit W-band horn antenna.

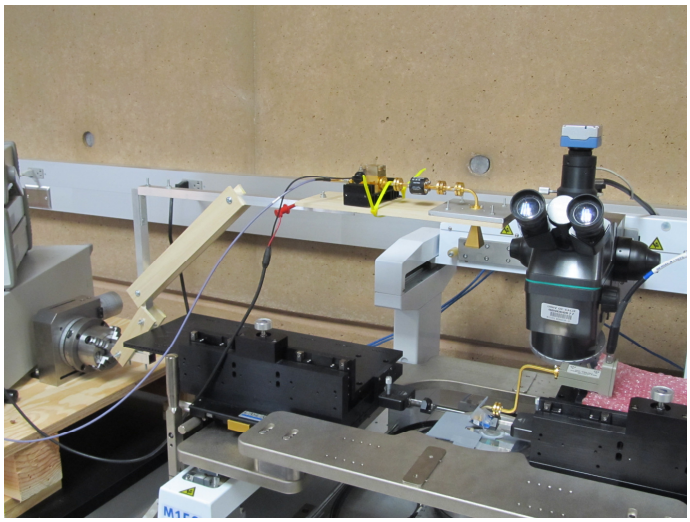

**Fig. 3 On-chip antenna measurement setup. Signal is transmitted by a horn antenna on a rotating arm. The on-chip bowtie slot antenna is probed and the received signal is down-converted, and then measured with a spectrum analyzer.**

At the receiving side, a harmonic mixer is employed to down-convert the frequency and connects to spectrum analyzer. A rotary table and rotation arm enables the pattern measurement. The antenna gain calibration is based on two W-band horn antennas separated at the same distance between horn antenna and the on-chip antenna. Losses in the probes and additional 0.5 dB transition loss between probe and on-chip coplanar waveguide were considered in the gain calculation of the bow tie antenna. However, due to strong interferences, the measured (averaged) 1dB gain is to be considered an approximate value.

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