On-Chip High Speed Localized Cooling Using Superlattice Microrefrigerators

Yan Zhang, James Christofferson, Ali Shakouri, Gehong Zeng, John E. Bowers, *Fellow, IEEE*, and Edward T. Croke

***Abstract*—In this paper, we addressed heating problems in integrated circuits (ICs) and proposed a thin-film thermionic cooling solution using Si/SiGe superlattice microrefrigerators. We compared our technology with the current most common solution, thermoelectric coolers, by strengthening the advantages of its compatible fabrication process as ICs for easy integration, small footprint in the order of $\sim 100 \times 100$ μm^2, high cooling power density, 600 W/cm^2 and fast transient response less than 40 μs. The thermoreflectance imaging also demonstrated its localized cooling. All these features combined together to make these microrefrigerators a very promising application for on-chip temperature control, removing hot spots inside IC.**

***Index Terms*—Hot spots, localized cooling, microrefrigerators, optoelectronics, superlattice, thermionic, thermoelectric, thin-film refrigerator.**

NOMENCLATURE

MTF	Mean time to failure, hour.
J	Current density, A/cm^2.
Ea	Activation energy, eV.
K	Boltzmann Constant, 8.616 $\times 10^{-5}$ eV/K.
ZT	Figure of merit.
S	Seebeck coefficient, μV/K.
σ	Electrical conductivity, $(\Omega$*cm$)^{-1}$.
β :	Thermal conductivity, W/mK.
T	Temperature, K or °C.
COP	Coefficient of performance.
Q	Heat load, W.
R	Electrical resistance of the microrefrigerator/TEC, Ω.
I	Current sent to power the TEC/microrefrigerator, A.
A	Device area, μm^2.
P	Maximum cooling power density, W/cm^2.

I. INTRODUCTION

THE current trend in microelectronic devices is to increase the level of integration, minimize the die size, and at the same time increase clock speed (higher frequency). This will result in higher power dissipation thus an increase in the die temperature. The increasing die temperature will directly affect the quality and reliability issue of integrated circuits (ICs) due to electromigration and oxide breakdown [1]–[3]. The lifetime of IC device exponentially decreases with the increasing die temperature, which could be described by Black's equation [4] as illustrated in Fig. 1. According to Intel's predictions, within the next five to ten years, the increasing power requirements of the IC chip is going to exceed the cooling capability of current techniques. To satisfy this demand, we need make the case temperature ~20 °C lower than its current value [5].

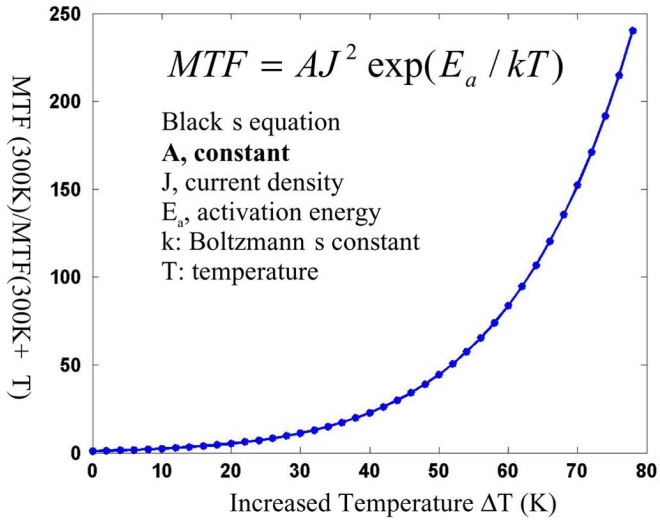

Fig. 1. Illustration of exponential relation of meantime to failure (MTF) with increased temperature. (Color version available online at http://ieeexplore.ieee.org.)

One distinguished characteristic of ICs' temperature profile is uneven temperature distribution, which leads to "hot spots." The temperature inside the chip could vary 5 °C ~30 °C from one location to another in microprocessor. Current microprocessors have an average heat flux of 10–50 W/cm^2. However, a peak flux can reach six times this average value [5]. Thus, reducing or eliminating hot spots could lower the thermal design requirements for the whole package.

Current available cooling technologies mainly consist of three categories with their own advantages and disadvantages [5].

First, is circulated liquid cooling, which moves heat sink away from the processors by increasing the surface area. However, this technology is not active cooling technology thus it will not help to lower the thermal resistance of the whole package. Most of all, reliability is a big concern if the liquid hose is leaking.

The second technology is refrigeration. Active cooling can provide an effective thermal resistance (R_{th}(effective)=(T_c-T_a

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Y. Zhang, J. Christofferson, and A. Shakouri are with the Electrical Engineering Department, University of California, Santa Cruz, CA 95064 USA (e-mail: ali@soe.ucsc.edu).

G. Zeng and J. E. Bowers are with the Electrical and Computer Engineering Department, University of California, Santa Barbara, CA 93106 USA.

Edward T. Croke is with HRL Laboratories, LLC, Malibu, CA 90265 USA.

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)/P, T_c, package top surface temperature, T_a, ambient temperature, the active cooling normally creates a cooling surface lower than the ambient, which (T_c-T_a)<0, which was defined as the negative effective thermal resistance.) less than 0.0 C/W. The effective thermal resistance refers to the total thermal pass above the package, which includes interface material, heat spreader, cooling components and heat sink etc. However, as the same problem as the first method, the limited space, noise and reliability are the main concerns.

The third technology is the most widely used cooling solution for semiconductor industries, thermoelectric (TE) devices. Thermoelectric cooling is silent and environmental green solution. It is active cooling with no moving parts, which could provide an effective heat sink resistance less than 0.0 C/W as well. Usually, we use figure of merit (ZT) as a measure of maximum cooling capability and the coefficient of performance (COP) to measure the cooling efficiency. The ZT has the expression $\mathrm{ZT} = S^2\sigma T/\beta$, where S is the Seebeck coefficient, σ, electrical conductivity, β, thermal conductivity, and T, absolute temperature. The ZT value is directly related to the COP of thermoelectric modules. Typical commercial modules have a ZT $\sim$ 1, which corresponds to COP $\sim$ 0.6 for 30 °C temperature difference. In addition, BiTe/SbTe and PbTe, the common TE materials are all bulk material, which make them incompatible with standard microprocessor chips. Currently, the smallest thermoelectric micromodule has a short leg length on the order of 0.2–0.3 mm, but with ceramic caps and thermal paste etc, the whole module is nearly to 1-mm-thick and 3–10 mm in diameter [6].

However, all these techniques only target on lowering the whole package temperature and none of them addresses the hot spots cooling. The hot spots in microprocessors are normally in the order of 300–400 μm in diameter, thus even the smallest thermoelectric module is still too large for spot cooling. There is an approach called optimized cell placement [7], which theoretically addresses the issue of reducing/eliminating hot spots by rearranging cell positions. It optimizes the device power map and reduces peak temperature. By implementing this method, the temperature gradient inside the chip could be improved by a factor of two though at the cost of increasing wire length and cell area, which limits minimization package and may bring more Joule heating inside the chip. Through statistical methods of power and timing analysis, like McPower [8] and Mean Estimator of Density (MED) [9] etc., it is possible to find the nominal on-chip temperature profile. However, this method will require the change of cell position thus it will require the IC design engineers involve in the thermal design process at the very beginning of the die design stage. Furthermore, the most concern is about the die size because of the cost of the die exponentially increasing with die area. Thus, developing a high cooling power density and easy integration thin film refrigerator could have a strong impact in IC optimization [10].

There are some recently exciting developments in thin film refrigerators using superlattice and quantum dot structure, which shows promising ZTs. For example, Venkatasubramanian *et al.* [11] demonstrated that the BiTe/SbTe superlattice could reach a ZT of 2.4 at 300 K. Harman *et al.* [12] at MIT Lincoln lab demonstrated PbTe quantum dots with ZT of 1.6–2.0 at 300 K.

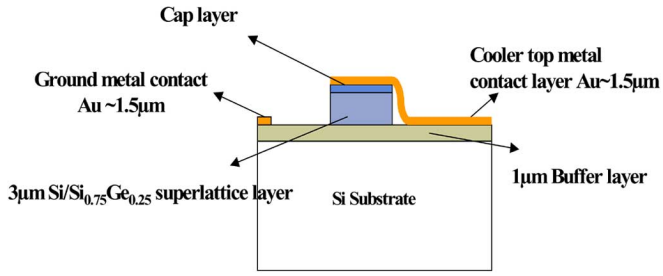


Fig. 2. Schematic cross-view of Si/SiGe microrefrigerator structure. (Color version available online at http://ieeexplore.ieee.org.)

The small footprint of these superlattice devices and the enhanced ZT propose a promising alternative solution for microprocessor hot spots cooling.

In our studies, we mainly focused on Si and InP-based materials for the convenience of monolithic integration with chips. In previous studies, thin film refrigerators based on InP [13] and SiGe/Si [14] were demonstrated with devices fabricated on a conventional silicon substrate and diameter ranging from 150 μm down to 20 μm. It could achieve 7–8 °C cooling at 100 °C ambient temperature [15]. In this paper, we mainly present the results of cooling power density and transient response measurements for these microrefrigerators.

II. Experiments

A. Device Fabrication

The microrefrigerator sample under test consisted of a 3-μm-thick superlattice layer with the structure of 200 × (3-nm Si/12-nm $Si_{0.75}Ge_{0.25}$) doped to 5e19 cm^{-3}, a 1-μm $Si_{0.8}$ $Ge_{0.2}$ buffer layer with the same doping concentration as the superlattice; and a 0.3-μm $Si_{0.8}$ $Ge_{0.2}$ cap layer doped to 1.9e20 cm^{-3}. The most important part of the device is the superlattice layer. It acts as a barrier layer in the thermionic emission process, and it can also reduce the thermal conductivity to prevent the backflow of heat from substrate to cold junction. The buffer layer on top of the Si substrate was included in order to reduce strain due to lattice mismatch between the substrate and the superlattice. The cap layer with higher doping concentration was included in order to improve the ohmic contact between the metal and semiconductor. The samples were grown with a molecular beam epitaxy (MBE) machine on five inch diameter (001)-oriented Si substrates, p-type doped to 0.003 $\sim$ 0.007 Ω-cm with boron. A Ti/Al/Ti/Au layer was evaporated on top of the samples for electrical contact. Fig. 2 illustrates a cross section view of the device structure.

B. Cooling Measurements

The cooling of the device was measured using Omega Type E thermocouple with a tip size of 50 μm. The schematic of the thermocouple measurements was illustrated in Fig. 3. We used differential temperature measurements by two thermocouples: one thermocouple on top the device and the other one on substrate. The sample was placed on a temperature control stage to keep the substrate temperature constant. An automatic Labview program was used to control measurement process. A constant current was supplied to the refrigerator stepping from 0 mA to 500 mA with the step size of 25 mA; the temperature difference

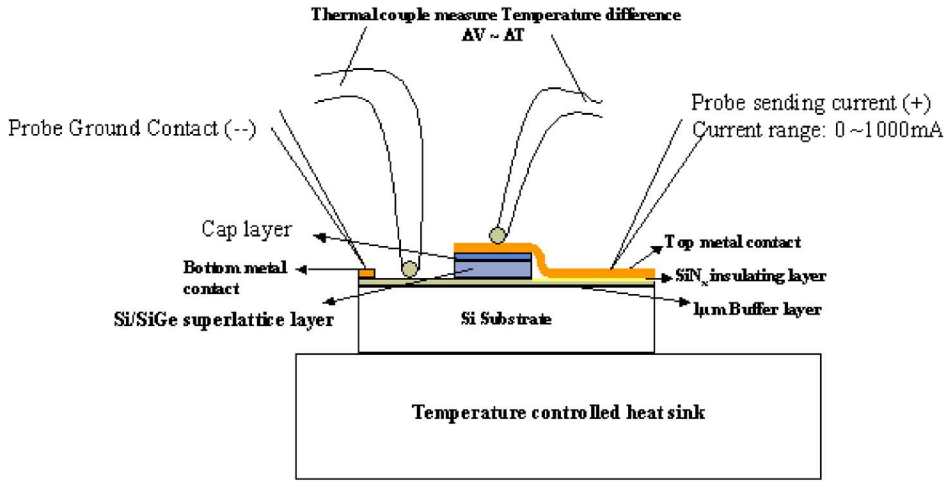


Fig. 3. Thermocouple measurement setup schematic. (Color version available online at http://ieeexplore.ieee.org.)

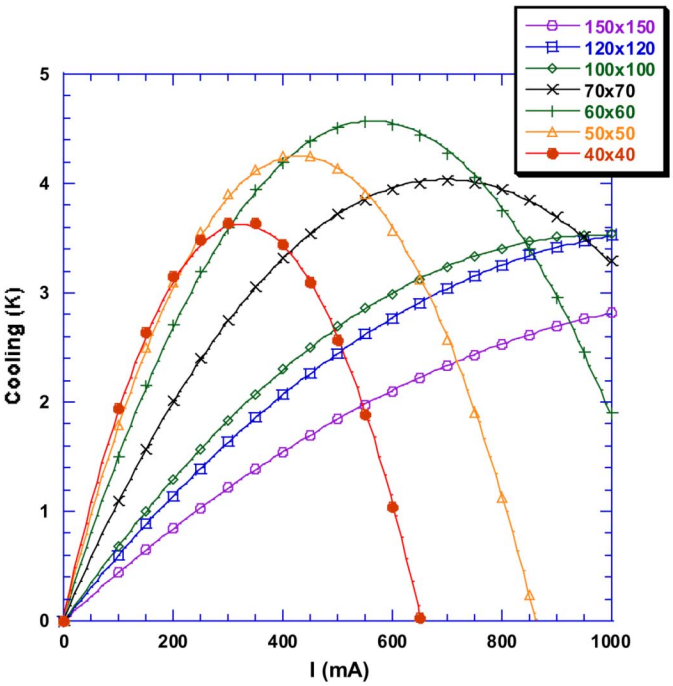


Fig. 4. Microrefrigerator cooling versus supplied current for various device sizes. (Color version available online at http://ieeexplore.ieee.org.)

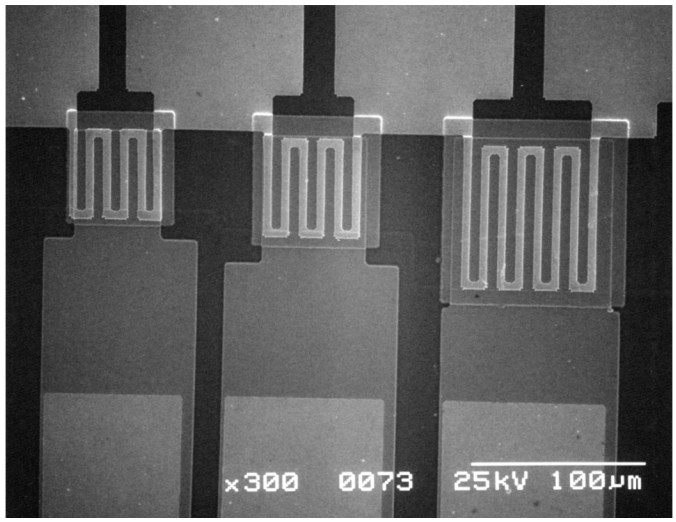


Fig. 5. Scanning electron microscope picture of Si/SiGe microrefrigerators integrated with thin film heaters/sensors.

was recorded at every step. Thus, a plot of the microrefrigerator cooling versus supplied current could be obtained. Fig. 4 illustrates cooling performance for various device sizes for a typical microrefrigerator with 3-μm $Si/Si_{0.8}$ $Ge_{0.2}$. Because of nonideal parasitic Joule heating from substrate, contact probe, and metal-semiconductor contact resistance, there is an optimized size to achieve the best cooling performance.

C. Cooling Power Measurements

For convenient measurements of cooling power density, we integrated a thin layer of metal heater/sensor on top of microrefrigerators. Fig. 5 shows a scanning electron microscopic (SEM) picture of the microrefrigerator integrated with a layer of thin film metallic wires. The integrated heater wires could work both as a sensor for temperature measurements and supplying heat on top of the device. While measuring the cooling power density, a constant current was supplied to the heater, and the cooling of microrefrigerators was measured by thermocouple at the same time. By increasing the constant current to the heaters, more heat load was added on top of the refrigerators. The maximum cooling power is defined as the heat load power that makes the device's maximum cooling temperature equal to zero. As a comparison, we also measured the cooling power density of the commercial TE modules. We put the TEC one side on top of the temperature controller and heat up the other side using a 100-μm-thick silicon substrate with 330×330 μm^2 heater wires.

D. Transient Response Measurements

In measuring the transient response of our device, a pulsed current with 1-kHz frequency was applied to the heater. The resulting temperature difference across the superlattice creates a thermoelectric voltage according to the Seebeck effect. With the heater turning on and off, the resulting thermoelectric voltage across the superlattice will response to the changes. Tektronics oscilloscope TDS 3054 with 500-mHz bandwidth was used to monitor the thermoelectric voltage response. The obvious rising

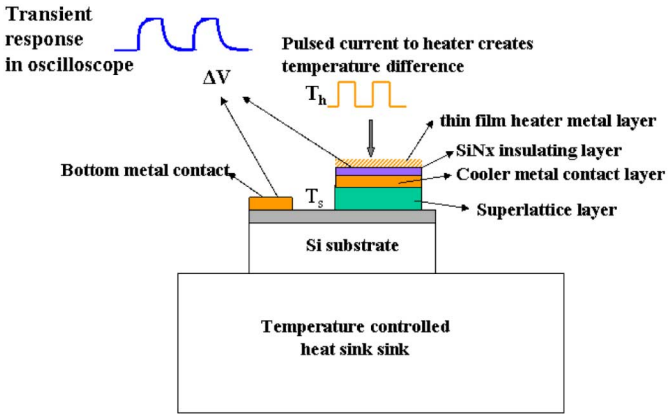


Fig. 6. Schematic of transient response measurements. (Color version available online at http://ieeexplore.ieee.org.)

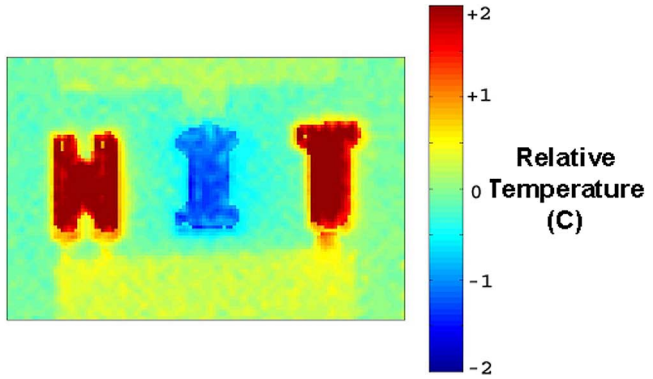


Fig. 7. Thermoreflectance imaging shows the localized heating of the integrated heater sensor on top of Si/SiGe superlattice microrefrigerator. (Color version available online at http://ieeexplore.ieee.org.)

and falling edge could be observed. We choose the falling edge to study the time constant. Though this measurement is not a direct measurement of cooling transient, but the cooling and heating transport are through the same superlattice layers. In this case, the heating transient is equivalent to the cooling transient. A schematic setup of the measurements is shown in Fig. 6. The collected data was an average of 512 measurements, and could fit well with an exponential curve. The decay time constant of the exponential function was defined as the transient response of the thin film superlattice refrigerator.

E. Results and Discussions

Conventional thermoelectric refrigerators are based on the Peltier effect at the junction between two dissimilar materials, e.g., a metal and a semiconductor. Upon current flow, electrons absorb thermal energy from lattice at one junction and transport it to another junction further away. Using SiGe/Si superlattice material and thermionic emission of electrons over heterostructure barriers, one can improve the cooling performance through evaporative cooling of electron gas and by reducing the lattice thermal conductivity between hot and cold junctions. Experimental results showed the cooling efficiency could improve four times with the superlattice-designed structure as compared with bulk materials [16].

A useful microrefrigerator should be able to create a significant temperature difference across the device. Fig. 4 illustrates cooling performance of various device sizes for a typical microrefrigerator with 3-μm Si/$Si_{0.8}$ $Ge_{0.2}$. Because of nonideal parasitic Joule heating from substrate, contact probe, and metal-semiconductor contact resistance, there is an optimized size to achieve the best cooling performance. Furthermore, the cooling performance could be improved when the device is operating at higher temperature [17]. At higher temperature, there will be more electrons with higher energy involved in the thermionic emission process, which could go over the barrier and contribute to the cooling. If the stage temperature raised up to 100 °C, the maximum cooling could be expected to increase up to four times as it is cooling at 25 °C [18].

Fig. 7 shows the temperature distribution on top of three devices fabricated with the shape of heterostructure integrated thermionic (HIT) refrigerators by noncontact thermoreflectance measurements [19]. One can see the localized heating

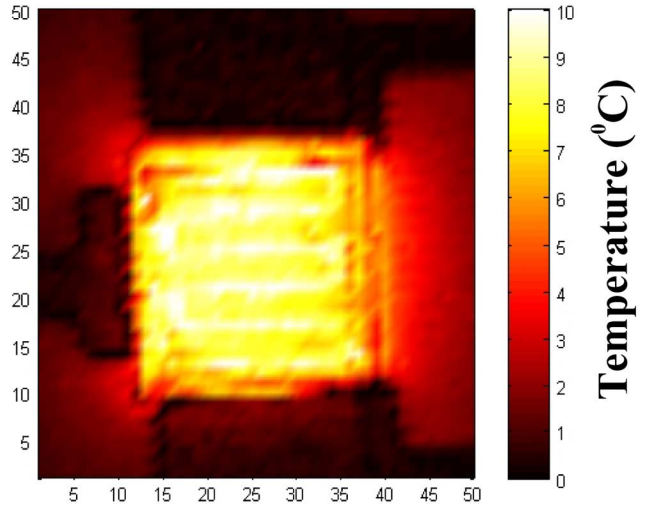


Fig. 8. HIT refrigerator picture shows the localized cooling and heating of the device. (Color version available online at http://ieeexplore.ieee.org.)

and cooling for devices separated less than 30 μm without any crosstalk. The thermoreflectance imaging has a lateral resolution of 500 μm and temperature resolution of 0.1 °C. It clearly demonstrates temperature distribution on top of the microrefrigerator. When we measure the cooling power density of the microrefrigerator, we also use the thermoreflecantce image to examine the quality of the heater wires and check whether the heating are localized on top of the microrefrigerator. Fig. 8 illustrates the localized heating by the heat wires on top of the microrefrigerator.

Fig. 9 shows the maximum cooling temperature relation with applied heat load density for both commercial TE modules and the Si/SiGe thin film microrefrigerator. The maximum cooling power is defined as heat load per unit area when maximum cooling temperature equals zero. The heat load of the heater could be calculated by Q= I^2R (Q, heat load; I, current supplied to the thin film wire, R, its resistance). Maximum cooling power density of the device is, $P = Q/A$, (Q heat load, A refrigerator area). We measured cooling power density of 10 W/cm^2, 50 W/cm^2, and 600 W/cm^2 for 1-mm-leg TE module, ultrathin (0.2-mm-leg) TE module and thin film microrefrigerators individually.

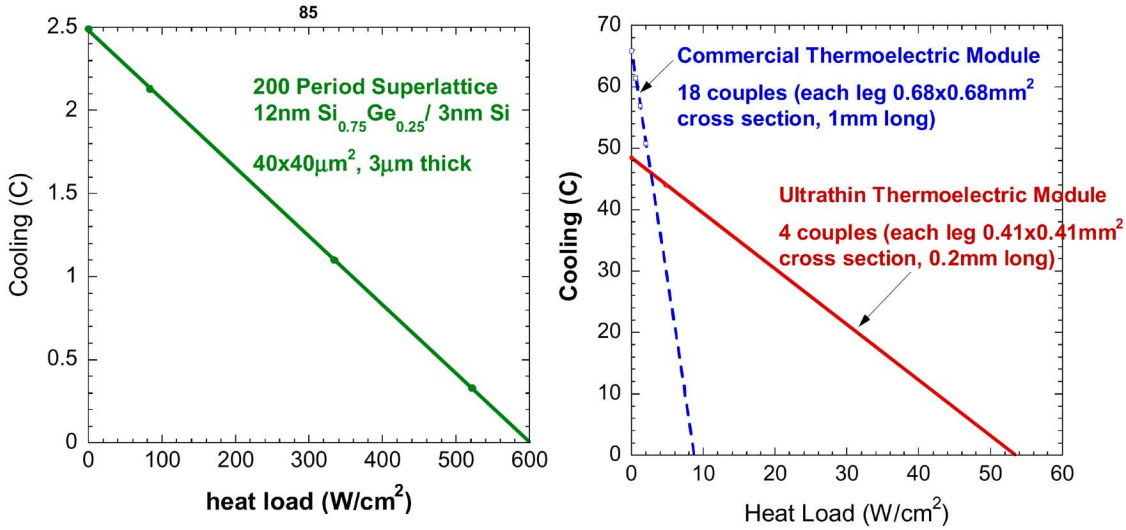


Fig. 9. Maximum cooling versus heat load comparison for a typical SiGe microrefrigerator with the commercial TE modules. (Color version available online at http://ieeexplore.ieee.org.)

TABLE I
COMPARISON OF THE POWER EFFICIENCY FOR COMMERCIAL TE MODULES WITH THIN FILM MICROREFRIGERATOR

	1mm-leg TE module	0.2mm-leg TE module	Thin film micro-refrigerator
I max (A)	1.75	2.5	0.3
R (ohm)	20	17.71	0.3
Consumed Electrical Power (W)	61.3	110.7	0.03
Cooling Power Density (W/cm2)	10	50	600
Device Size (μm2)	462400	168100	1600
COP	0.1%	0.1%	35.6%

The coefficient of performance (COP) was defined as the actual cooling power divided by the total power consumed. With the available data that we obtained from the cooling power density measurements in Fig. 9, we could also deduce the COP and make a comparison of the commercial TEC with the thin film microrefrigerator. The commercial TE module with a 1-mm-long leg could create a temperature difference of 68 °C with a cooling power density of 10 W/cm^2, COP of 0.1%. The ultrathin TE module with a 0.2-mm-long leg could create a temperature difference of 50 °C with cooling power density of 50 W/cm^2, COP of 0.1%. The thin-film microrefrigerator could only create a temperature difference of 2.5 °C but with a high cooling power density of 600 W/cm^2, COP could achieve 35.6%. Table I lists all the parameters used for COP calculation for all TE modules and microrefrigerator.

Furthermore, the transient response of the current SiGe/Si superlattice refrigerator is several orders of magnitude better than the bulk TE refrigerators. The standard commercial TE refrigerator has a response time on the order of tens of seconds. Fig. 10 shows the fitted transient response of a typical SiGe/Si superlattice sample, the decay time constant is $\sim$ 34 μs, which is in an order of 10^5 faster than the bulk TE refrigerators. In fact, the actual transient response of the device is faster than the measured value. The thermoreflectance method shows a transient response of $\sim$20 μs [20] directly on top of microrefrigerator. The transient response measured by heater sensor is slower than the thermal reflectance measurement because of the extra thermal mass of thin film heater-metal-wires.

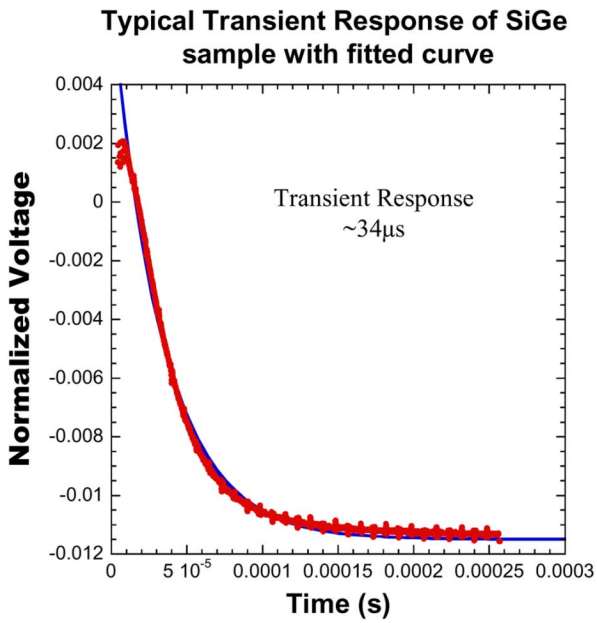


Fig. 10. Fitted transient response of SiGe/Si superlattice microrefrigerator. (Color version available online at http://ieeexplore.ieee.org.)

III. Conclusion

In this paper, we demonstrated the localized cooling of Si/SiGe superlattice thin film microrefrigerator. The cooling power density of the microrefrigerator has been measured and COP was calculated and compared with the commercial TEC modules. The Si/SiGe superlattice microrefrigerator has a cooling power density of 600 W/cm^2 and a fast transient response less than 40 μs. As compared with conventional bulk TE modules, thin film integrated SiGe/Si superlattice microrefrigerators have potential applications in high power, high-speed optoelectronics devices, and microprocessors for on-chip localized temperature control.

According to our theoretical simulation, the current limitation of the superlattice refrigerators still lies in the contact resistance between the metal and cap/buffer layer, which is on the order of 10^{-6} Ωcm^2 for current devices. It predicts a 20–30 °C of cooling with a cooling power density exceeding several thousands of W/cm^2 is possible with the optimized SiGe superlattice structure and non-ideal factors removed [21].

Future research interests will focus on improving cooling efficiency and integrating microrefrigerators with electronic and optoelectronic devices.

References

[1] J. W. McPherson and D. A. Baglee, "Acceleration factor for thin gate oxide stressing," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 1985, p. 1.

[2] Z. A. Weiberg, "Exciton or hydrogen diffusion in SiO2," *Appl. Phys. Lett.*, vol. 27, no. 8, p. 437, 1975.

[3] K. P. Cheung, "Unifying the thermal-chemical (TC) and anode-hole-injection (AHI) gate-oxide breakdown models," *Microelectron. Rel.*, vol. 41, p. 193, 2001.

[4] J. R. Black, "Electromigration—A brief survey and some recent results," *IEEE Trans. Electron Devices*, vol. 16, no. 4, pp. 338–347, Apr. 1969.

[5] G. M. Chrysler, "Building Blocks for thermal management of electronics," *Next-Generation Thermal Management Materials and Systems*, 2002.

[6] V. Semenyuk, "Thermoelectric Micro Modules for Spot Cooling of High Density Heat Sources," in *Proc. 20th Int. Conf. Thermoelect.*, 2001, p. 391.

[7] Y.-K. Cheng, C.-H. Tsai, C.-C. Teng, and S. Kang, *Electrothermal Analysis of VLSI Systems*. New York: Academic, 2000.

[8] R. Burch, F. Najm, P. Yang, and T. Trick, "McPower: A Monte Carlo approach to power estimation," in *Proc. ACM/IEEE Int. Conf. Computer-Aided Design*, 1992, pp. 90–97.

[9] M. G. Xakellis and F. N. Najm, "Statistical estimation of the switching activity in digital circuits," *Proc. ACM/IEEE Design Autom. Conf.*, p. 728, Jun. 1994.

[10] J. W. Vandersande and J.-P. Fleurial, "Thermal management of power electronics using thermoelectric coolers," in *Proc. 15th Int. Conf. Thermoelect.*, New York, 1996, p. 252.

[11] R. Venkatasubramanian, E. Siivola, T. Colpitts, and B. O'Quinn, "Thin-film thermoelectric devices with high room-temperature figures of merit," *Nature 413*, pp. 597–602, Oct. 11, 2001.

[12] T. C. Harman, P. J. Taylor, M. P. Walsh, and B. E. LaForge, "Quantum dot superlattice thermoelectric materials and devices," *Science*, vol. 297, pp. 2229–2232, Sep. 27, 2002.

[13] C. LaBounty, D. Vashaee, X. Fan, G. Zeng, P. Abraham, A. Shakouri, and J. E. Bowers, "P-type InGaAs/InGaAsP superlattice coolers," in *Proc. 19th Int. Conf. Thermoelect.*, Cardiff, U.K., Aug. 2000.

[14] Z. Gehong, A. Shakouri, C. L. Bounty, G. Robinson, E. Croke, P. Abraham, F. Xiafeng, H. Reese, and J. E. Bowers, "SiGe micro-cooler," *Electron. Lett*, vol. 35, no. 24, pp. 2146–2147, Nov. 1999.

[15] X. Fan, G. Zeng, E. Croke, C. LaBounty, C. C. Ahn, A. Shakouri, and J. E. Bowers, "SiGeC/Si superlattice microcooler," *Appl. Phys. Lett.*, vol. 78, no. 11, Mar., 12 2001.

[16] X. Fan, G. Zeng, C. LaBounty, E. Croke, D. Vashaee, A. Shakouri, C. Ahn, and J. E. Bowers, "High cooling power density SiGe/Si micro coolers," *Electron. Lett.*, vol. 37, no. 2, pp. 126–127, Jan. 18, 2001.

[17] X. Fan, G. Zeng, C. LaBounty, E. Croke, C. Ahn, J. E. Bowers, and A. Shakouri, "SiGeC/Si superlattice micro cooler," *Appl. Phys. Lett.*, vol. 78, no. 11, Mar., 12 2001.

[18] J. Christoffrson, D. Vashaee, A. Shakouri, X. Fan, G. Zeng, C. LaBounty, J. E. Bowers, and E. Croke, "Thermal characterization of thin film superlatttice micro refrigerators," in *Proc. Int. Symp. Compound Semicond.*, Oct. 2000, pp. 49–54.

[19] J. Christofferson, D. Vashaee, A. Shakouri, P. Melese, X. Fan, G. Zeng, C. Labounty, J. E. Bowers, and E. T. Croke III, "Thermoreflectance imaging of superlattice micro refrigerators," in *Proc. SEMITHERM XVII Symp.*, San Jose, CA, Mar. 2001, pp. 58–62.

[20] F. Alberto, C. James, S. Ali, X. Fan, G. Zeng, C. LaBounty, J. E. Bowers, and Ed. Croke, "Transient response of thin film SiGe micro coolers," in *Proc. Int. Mech. Eng. Congress Exhibition (IMECE'01)*, New York, Nov. 2001.

[21] C. LaBounty, A. Shakouri, and J. Bowers, "Design and characterization of thin film microcoolers," *J. Appl. Phys.*, vol. 89, no. 7, p. 4059, 2001.

Yan Zhang received the B.S. degree from Shanghai University, Shanghai, China, in 1997, the M.Sc. degree from the National University of Singapore, in 2000, and the Ph.D. degree from the Electrical Engineering Department, University of California, Santa Cruz, in 2005.

Her current research is on nano-scale heat and current transport in semiconductor devices, microrefrigerator for on-chip cooling solution, thermal characterization and testing for semiconductor devices, and thermionic energy conversion for waste heat recovery.

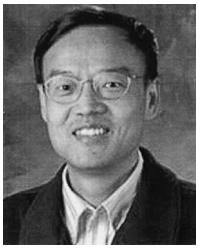
James Christofferson received the B.S. degree in physics, the M.S. degree in computer engineering, and the Ph.D. degree in electrical engineering from the University of California, Santa Cruz (UCSC), in 2004.

His research involved microscale thermal imaging and analysis of semiconductor structures. He is currently a Postdoc Researcher in UCSC's Quantum Electronics Laboratory experimenting on optical coherence microscopy, and femptosecond pump probe interferometry in order to image phonons, thermal waves, and see beneath opaque surfaces.

Ali Shakouri received the B.S. degree from Ecole Nationale Superieure des Telecommunications de Paris, Paris, France in 1990 and the Ph.D. degree from the California Institute of Technology, Pasadena, in 1995.

He is a Professor of electrical engineering at the University of California, Santa Cruz. He is the Director of the Thermionic Energy Conversion Center (a multi university research initiative aiming to improve direct thermal to electric energy conversion technologies). His current research is on nanoscale heat and current transport in semiconductor devices, submicron thermal imaging, micro refrigerators on a chip and novel optoelectronic integrated circuits.

Dr. Shakouri received the Packard Fellowship in 1999 and the NSF Career Award in 2000.



Gehong Zeng received the B.S. degree from South China Institute of Technology, Guangzhou, China, in 1982 and the M.S. and Ph.D. degrees from Shaanxi Microelectronics Research Institute, Xian, China, in 1987 and 1992, repectively.

He was previously with the Kunming Institute of Physics, China, working on infrared detectors and imagers. He is now with the Electrical and Computer Engineering Department, University of California, Santa Barbara. His research interests include design, fabrication, and testing of optoelectronic devices.

John E. Bowers (F'93) received the M.S. and Ph.D. degrees from Stanford University, Stanford, CA.

He is Director of the Multidisciplinary Optical Switching Technology Center (MOST), and a Professor in the Department of Electrical Engineering, University of California, Santa Barbara. He is cofounder of the Center for Entrepreneurship and Engineering Management, and a cofounder of Terabit Technology and Calient Networks. He has published six book chapters, 350 journal papers, 600 conference papers, and has received 38 patents. His research interests are primarily concerned with optoelectronic devices and optical networking.

Dr. Bowers received the IEEE LEOS William Streifer Award and the South Coast Business and Technology Entrepreneur of the Year Award. He is a Fellow of OSA and the American Physical Society.

Edward T. Croke received the B.S. degree from Cornell University, Ithaca, NY, in 1986, and the Ph.D. degree from the California Institute of Technology (Caltech), Pasadena, in 1991.

He joined HRL Laboratories, LLC, Malibu, CA, shortly after graduating from Caltech in April 1991, where he has primarily been involved with the growth of Si-related heterostructures including SiGe and SiGeC alloys by M.B.E. Among his accomplishments, he has designed and implemented a novel carbon source for e-beam deposition of SiGeC random alloys. He also demonstrated coherent growth of SiGeC/Si superlattices on (100) Si substrates by M.B.E. and discovered a dramatic improvement in the surface morphology and crystallinity of high-Ge and high-C content SiGeC/Si superlattices through the use of Sb as a surfactant. Recently, he has been involved with efforts, under the DARPA QuIST program, to develop a quantum repeater in the InGaAs/InP materials system. He has also developed a low-temperature, electron spin resonance spectrometer (with Janis Research Co.) capable of performing sensitive electronic measurements at 250 mK in magnetic fields approaching 9 Tesla. He has authored or coauthored over 50 journal articles in the area of SiGeC MBE growth and the properties of SiGeC microcoolers.