Lawrence Berkeley National Laboratory

Recent Work

Title

SCHOTTKY BARRIER INSTABILITIES DUE TO CONTAMINATION

Permalink

<https://escholarship.org/uc/item/0p98j9q7>

Authors

Newman, N.
Liliental-Weber, Z.
Weber, E.R.

Publication Date

1988-03-01

Center for Advanced Materials

CAM

RECEIVED
LAWRENCE

BERKELEY LABORATORY

JUN 23 1988

Submitted to Applied Physics Letters

LIBRARY AND
DOCUMENTS SECTION

Schottky Barrier Instabilities Due to Contamination

N. Newman, Z. Liliental-Weber, E.R. Weber, J. Washburn, and W.E. Spicer

March 1988

TWO-WEEK LOAN COPY

*This is a Library Circulating Copy
which may be borrowed for two weeks.*

Materials and Chemical Sciences Division

Lawrence Berkeley Laboratory • University of California

ONE CYCLOTRON ROAD, BERKELEY, CA 94720 • (415) 486-4755

LBL-25069
c. 2

DISCLAIMER

This document was prepared as an account of work sponsored by the United States Government. While this document is believed to contain correct information, neither the United States Government nor any agency thereof, nor the Regents of the University of California, nor any of their employees, makes any warranty, express or implied, or assumes any legal responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by its trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof, or the Regents of the University of California. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof or the Regents of the University of California.

Schottky Barrier Instabilities Due to Contamination

N. Newman

Stanford Electronics Laboratory, Stanford University, Stanford, CA 94305
Center for Advanced Materials, Materials and Chemical Sciences Division, Lawrence Berkeley
Laboratory, 1 Cyclotron Road, Berkeley, CA 94720

Z. Liliental-Weber, E.R. Weber and J. Washburn

Center for Advanced Materials, Materials and Chemical Sciences Division, Lawrence Berkeley
Laboratory, 1 Cyclotron Road, Berkeley, CA 94720
Dept. of Materials Science and Mineral Engineering, University of Calif., Berkeley, CA 94720

W. E. Spicer

Stanford Electronics Laboratory, Stanford University, Stanford, CA 94305

We report here a systematic study of the annealing-induced changes in the barrier height of Schottky barrier diodes fabricated on atomically-clean and contaminated surfaces. Al, Ag, Au and Cr/GaAs(110) diodes were fabricated by *in-situ* deposition on clean *n*-type GaAs(110) surfaces prepared by cleavage in ultrahigh vacuum and on contaminated surfaces prepared by cleavage and exposure to the atmosphere for ~1-2 hours. This study demonstrates that the as-deposited barrier height and the annealing-induced changes in the barrier height of diodes formed with an interfacial layer of contamination are distinctly different from the characteristics of diodes formed on clean semiconductor surfaces. The presence of an interfacial layer of contamination is found to significantly degrade the stability of the diode's barrier height to annealing.

A large number of commercial electronic devices depend on the formation of Schottky barriers which are reliable, reproducible and stable against time and temperature. The fabrication of structures which fulfill these requirements is one of the most challenging problems facing the semiconductor device manufacturer today. Typically, the Schottky barriers are formed using conventional integrated circuit fabrication methods which include a chemical clean and exposure to the atmosphere before insertion into the metal-deposition vacuum chamber.^{1,2} This procedure allows a thin layer of contamination to form on the semiconductor surface prior to metal deposition.^{1,3} In this work, we directly compare the electrical characteristics of annealed metal/GaAs junctions which are formed on atomically-clean surfaces with those formed on surfaces exposed to the atmosphere for a brief period.

Al, Ag, Au and Cr/ GaAs(110) diodes were fabricated by *in-situ* deposition on clean *n*-type GaAs(110) surfaces prepared by cleavage in ultrahigh vacuum (UHV) and on contaminated surfaces prepared by cleavage and exposure to the atmosphere for ~1-2 hours. Henceforth, these diodes will be referred to as UHV-cleaved diodes and air-exposed diodes, respectively. The samples used were $2.5 \times 10^{16} \text{ cm}^{-3}$ Si-doped GaAs. The UHV-cleaved diodes were fabricated in a vacuum chamber which was baked-out to obtain UHV conditions (base pressure 2.4×10^{-10} torr). Average pressures were kept below 10^{-9} Torr during the initial stages of Schottky barrier formation ($< 100 \text{ \AA}$). So that the air-exposed surfaces were not subjected to any unnecessary heat before metallization, a chamber bakeout was not performed. For the diodes produced on the air-exposed surfaces, the pressure during metal deposition was approximately 10^{-7} torr. Diodes of typically $460 \text{ }\mu\text{m}$ in diameter were defined by a shadow mask placed just in front of the samples. After the diodes were fabricated, current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed in atmospheric conditions at room temperature. Annealing was performed for 10 min. in N₂ at atmospheric pressure.

Forward-bias I-V characteristics, as shown in Fig. 1, are used to determine the I-V barrier height and ideality factor using the conventional thermionic emission equation. See Ref. 4 for a complete description of the I-V technique. The C-V method described in Ref. 4 is used to determine the junction capacitance (C) as a function of voltage (V) from 0 to -2 V. The C-V barrier height is then inferred by adding the intercept of the C^{-2} versus V curve (i.e. the diffusion voltage) to the difference between the Fermi-level and the conduction band minimum (CBM) in the bulk ($\sim 0.065 \text{ eV}$) minus the Gummel-Scharfetter factor ($V_t = \sim 0.0253 \text{ eV}$ at 22° C).^{1,4} Table I summarizes the results.

With the exception of the annealed Cr/GaAs system, the data for UHV-cleaved diodes have been presented in earlier publications.^{4,5,6,7} For each of the Al, Ag, Au and Cr/GaAs systems formed on clean UHV-cleaved surfaces, the electrical characteristics of 5-10 diodes have been measured on each of ~1 to 2 dozen cleaved-GaAs-surfaces (i.e. over 60 diodes total for each system) and the results have been found to be consistent with the values reported in Table I and our earlier publications.^{4,5,6,7,8,9} To our knowledge, this level of reproducibility in the electrical characteristics of GaAs Schottky barriers has not been reported in the literature. The results have also been reproduced to within experimental error by other laboratories.¹⁰ For the air-exposed samples,

the values in Table I were determined from the electrical characteristics of a total of 5-10 diodes measured on each of at least 3 different cleaved-GaAs-surfaces for the unannealed cases and at least 2 different cleaved-GaAs-surfaces for the annealed cases.¹¹

As can be seen in Fig. 1 and Table I, I-V and C-V measurements of both the UHV-cleaved and air-exposed diodes are characteristic of near-ideal Schottky barriers with ideality factors very close to unity. This demonstrates that the presence of the interfacial oxide layer does not significantly degrade the near-ideal electrical characteristics. Ellipsometry has shown that exposure of clean GaAs to atmospheric conditions for several hours will allow a 5-10 Å oxide layer to grow on the surface of the crystal.³ The presence of a thin interfacial layer of this thickness is not expected to cause a significant error in the I-V and C-V barrier height determinations.¹ This conclusion is consistent with the fact that the I-V data are characterized by a near unity factors and that I-V and C-V barrier height determinations are within experimental error when the I-V barrier height determinations are corrected for tunneling and the image force.¹²

As can be seen in Fig. 1a and 1b, a large change in the barrier height of the Cr and Ag diodes formed on air-exposed surfaces occurs upon annealing (80 meV and 160 meV, respectively). In contrast, the barrier heights of Cr diodes formed on UHV surfaces do not change significantly (<10 meV) and that of Ag shows only a small, almost insignificant increase (~ 20 meV). This indicates that the interfacial layer of contamination which is formed on the GaAs surface by air-exposure can cause dramatic effects to the stability of diodes formed. In the case of Al, both the air-exposed and UHV-cleaved diodes are found to increase their barrier height by 70 meV. This is illustrated in Fig. 1c and Table I. In the case of Au, the air-exposed and UHV-cleaved diodes are found to decrease their barrier height by 180 meV and 120 meV, respectively.

A number of studies since the mid-1970's have found that the rectifying properties of Au/GaAs diodes degrade upon annealing.^{13,14} Recently we have conclusively shown that the degradation is due to a shunt current pathway at the diode periphery which comprises less than 1% of the total area of the device.^{6,8,15} In Fig. 2 we show the results of I-V measurements for diodes formed on air-exposed GaAs(110) surfaces. By using a semiconductor etch ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$, 2:1:20 for 1 min.) and effectively using the Au dot as a mask, we are able to isolate the electrical characteristics of the central portion of the device from that of the periphery. The near-ideal Schottky characteristics with a near unity ideality factor (1.05) found after mesa etching can be associated with the electrical characteristics of the central portion of the annealed Au diodes. Therefore, the voltage dependence of the ideality factor of annealed Au/GaAs diodes before mesa-etching (Fig. 2) can be attributed to the measured current being a sum of the current through the central portion of the device with a near-unity factor and a peripheral current with an ideality factor typically greater than or equal to 2. We first discovered this for UHV-cleaved Au diodes at higher annealing temperatures where much larger peripheral Ohmic-like currents are found to dominate the electrical characteristics of the device. The I-V data for the UHV diodes have been shown in Ref. 6,8 and 15. Recent Transmission Electron

Microscopy (TEM) results have found that annealed diodes formed on UHV-cleaved GaAs surfaces have flat interfaces, while annealed diodes formed on air-exposed have rough interfaces with a large number of protrusions extending into the semiconductor.⁸ These results show that the changes which occur upon annealing are not due to changes in the current transport by tunneling through highly doped n+ regions¹³ or recombination at the metallic protrusions¹⁴ in the central portion of the device, as suggested by others. The mechanism responsible for the Ohmic behavior at the periphery is unclear. The presence of large strain-fields which can cause distortion of the semiconductor bands or changes in chemistry of defect formation at the periphery are believed to be important.

In the following discussion, we discuss the implications of these results to a recently-developed model of Schottky barrier formation. Because of space limitations and the large number of models in the literature, the discussion presented here will concentrate on a model suggested by our group recently.¹⁶ The Unified Defect Model (1979) has hypothesized that the barrier height is established by the energy levels of native defects formed at the surface during the metal deposition.^{9,17} Recently (1987), the Advanced Unified Defect Model (AUDM) has appended the original model to specify that the dominant defect responsible for Fermi-level pinning is the AsGa (arsenic on gallium site) antisite defect.¹⁸ This defect is known to be a double donor in character with energy levels at 0.52 eV and 0.75 eV above the valence band maximum (VBM).¹⁹ To account for the pinning positions for thin and thick metal coverages on n- and p-type surfaces, this model has suggested that a comparatively smaller number of compensating acceptors with an energy level farther than 0.9 eV from the CBM are formed (e.g. GaAs, a gallium on an arsenic site). According to this model, alterations in stoichiometry of the As and Ga concentrations by chemical reactions at the interface may lead to changes in the relative concentrations of the defects formed and therefore the Fermi-level pinning position. The presence of excess As would lead to the dominance of the AsGa defect, an increase in the number of donors and pinning closer to midgap. For Ga rich conditions, the opposite occurs and pinning is closer to the VBM. Although the chemistry is not completely understood for each system and the nature of the contaminants is not known, we find some strong correlations between the expected stoichiometry and changes in barrier height upon annealing.

In an open system, Au is expected to react almost exclusively with Ga, forming an alloy of Au and Ga.²⁰ For the case of the UHV-cleaved surfaces, high resolution TEM micrographs⁸ and quantitative Surface Analysis by Laser Ionization (SALI) results²¹ have shown that the concentration of Ga in the Au is sufficiently small that no new crystallographic phases are formed. The resulting metallic overlayer consists of Ga dissolved in the crystalline Au phase.⁸ After annealing, the presence of a higher concentration of Ga in the crystalline Au phase and a significant excess of As released by the reaction and trapped near the interface has been detected.^{8,21} For this case, the AUDM would predict an increase in the AsGa donor concentration at the interface and the interface Fermi level pinning position would therefore move toward midgap. The AUDM's prediction is therefore consistent with the observation that the barrier height to n-type material decreases upon annealing. In

contrast, Al is expected to react almost exclusively with As, resulting in a decrease in the As/Ga ratio at the interface after annealing.^{5,22} The model's prediction is therefore consistent with the observation that the barrier increases upon annealing. Ag is known to be unreactive^{5,20,23} and Cr is known to react with both Ga and As.²⁴ In both cases, no significant change was found upon annealing, consistent with the model's predictions.

In the case of air-exposed surfaces, the effects of chemical reactions between the metal, the semiconductor and the interfacial contamination layer must be taken into account. Because Au does not react with oxygen, the interfacial layer of contamination is expected to be composed primarily of oxides of GaAs. Upon annealing the thermodynamically stable products of the reaction; $\text{GaAs} + \text{O}_2 \rightarrow \text{Ga}_2\text{O}_3 + \text{As}$ are expected to form.²⁵ The release of As by this reaction and the reaction between Au and GaAs (i.e. $\text{Au} + \text{GaAs} \rightarrow \text{AuGa}_x + \text{As}$)^{8,20,21} can be correlated with the decrease in barrier height, consistent with the AUDM's predictions. Because Al is known to reduce any oxides of GaAs²⁰, the presence of an interfacial oxide layer will reduce the extent of reaction between the Al and GaAs, resulting in a smaller amount of free Ga at the interface than in the UHV-cleaved case. For the unannealed diodes, the observation that the barrier height of the diodes formed on the air-exposed surface is smaller than that of those formed on the UHV-cleaved surface is consistent with the decrease in the As/Ga ratio, as predicted by the AUDM. Also, the increase in barrier height upon annealing is consistent with the uptake of As by the reaction of Al, as was found in the UHV sample. For Ag, the presence of an interfacial oxide layer leads to a decrease in barrier height upon annealing. Because Ag is unreactive when deposited on GaAs^{5,20,23}, the thermal reaction between GaAs and oxygen to form Ga_2O_3 and As would be expected upon annealing.²⁵ The correlation with the expected release of As and the observed barrier height decrease is therefore consistent with the AUDM's prediction. In the case of Cr, predicting the stoichiometry at the interface is more difficult than for the other metals. Cr reacts with GaAs and GaAs-oxides to release both As and Ga.²⁴ It can be speculated that the presence of an interfacial oxide may allow for the additional reaction of Cr with the Ga_2O_3 to release Ga, consistent with the model's correlation between a barrier height increase and a decrease in the near-interfacial As/Ga ratio.

In conclusion, we find a correlation between the annealing-induced changes in barrier height and the expected stoichiometry of the near-interfacial GaAs, in agreement with predictions of the AUDM. The extension of this work to GaAs(100) surfaces prepared by heat cleaning and/or chemical processing as used for I.C. device applications will be of great practical importance. However, because of the extremely complex chemistry in these systems, further work is needed to determine the As/Ga stoichiometry near the interface before a reliable comparison can be made.

ACKNOWLEDGEMENTS: The work was supported by DARPA and ONR under contract N00014-83-0073. This work was supported partially by SDIO/IST program administered by ONR through contract N00014-86-K-0668 and the AFOSR under Contract AFOSR-86-0263 and the Materials Science Division of the DOE under contract DE-AC03-76SF00098.

TABLE I: Results of I-V and C-V electrical measurements

	Diodes formed on <u>AIR-EXPOSED GaAs (110)</u>			Diodes formed on <u>CLEAN UHV-CLEAVED GaAs (110)</u>		
	ϕ_{bo} (eV) ± 0.02 -----	I-V n -----	ϕ_b (eV) ± 0.05 -----	ϕ_{bo} (eV) ± 0.02 -----	I-V ^b n -----	ϕ_b (eV) ± 0.05 -----
<u>Al</u>						
unannealed	0.76	1.07	0.84	0.83	1.06	0.87
370° C anneal	0.83	1.07	0.90	0.90	1.05	0.92
<u>Ag</u>						
unannealed	0.95	1.07	1.06	0.89	1.06	0.94-0.97
370° C anneal	0.79	1.06	0.85	0.91	1.07	0.92-0.99
<u>Au</u>						
unannealed	0.83	1.08	0.94	0.92	1.05	1.00
370° C anneal	0.65	1.06	0.72	0.80 ^a	1.06 ^a	0.88 ^a
<u>Cr</u>						
unannealed	0.68	1.06	0.79	0.66	1.06	0.74
370° C anneal	0.76	1.08	0.88	0.67	1.06	0.74

a The data in this table for Au diodes formed on the clean UHV-cleaved diodes is from a 430° C anneal, as reported in Ref. 5.

b I-V characteristics for the unannealed diodes formed on the UHV-cleaved surfaces have also been measured *in-situ* in UHV. In the case of the Al, Ag, and Au/GaAs systems, essentially identical barrier heights and ideality factors were found. In the case of Cr, the barrier height was found to be smaller by ~0.02 eV, a small but significant difference.

FIGURE CAPTIONS:

Fig. 1: Typical current-voltage (I-V) measurements for diodes formed on clean *n*-type GaAs(110) surfaces prepared by cleavage in ultrahigh vacuum (UHV) and on air-exposed surfaces prepared by cleavage and exposure to the atmosphere for ~1-2 hours.

Fig. 2: Typical current-voltage (I-V) measurements for Au diodes formed on air-exposed surfaces prepared by cleavage and exposure to the atmosphere for ~1-2 hours. As can be seen, the near-ideal characteristics of the unannealed Au diodes (bottom curve) degrade upon annealing at 370° C (top curve). Note that the log I-V curve is very non-linear in the top curve. The ideality factor is therefore voltage dependent and varies from 1.15-1.27 for the I-V data shown. However, we note that upon mesa-etching (middle curve), the log I-V electrical characteristics are found to exhibit strongly rectifying Schottky characteristics with a near unity ideality factor (1.06).

Figure 1

Figure 2

REFERENCES:

1. E.H. Rhoderick, Metal-Semiconductor Contacts (Clarendon, Oxford, England, 1980).
2. Sorab K. Ghandi, VLSI Fabrication Principles, Silicon and Gallium Arsenide, John Wiley and Sons, New York (1983).
3. A.C. Adams and B.R. Pruniaux, *J. Electrochem. Soc.* **120**,408 (1973).
4. N. Newman, M. van Schilfgaarde, T. Kendelewicz, M. D. Williams and W. E. Spicer, *Phys. Rev. B* **33**, 1146 (1986).
5. N. Newman, K.K. Chin, W.G. Petro, T. Kendelewicz, M.D. Williams, C.E. Mc Cants and W.E. Spicer, *J. Vac. Sci. Technol.* **A3**, 996 (1985).
6. N. Newman, W. G. Petro, T. Kendelewicz, S. H. Pan, S. J. Eglash and W. E. Spicer, *J. Appl. Phys.* **57**, 1247 (1985).
7. N.Newman, W.E. Spicer and E.R. Weber, *J. Vac. Sci.Technol.* **B5**, 1020 (1987).
8. Zuzanna Liliental-Weber, R. Gronsky, J. Washburn, N.Newman, W.E. Spicer and E.R. Weber, *J. Vac. Sci. Technol.* **B4**, 912(1986); Z. Liliental-Weber, J. Washburn, N. Newman, W.E. Spicer and E.R. Weber, *Appl. Phys. Lett.* **49**, 1514 (1986); Zuzanna Liliental-Weber, E.R. Weber, N. Newman, W.E. Spicer, R. Gronsky and J. Washburn, Defects in Semiconductors, Edited by H.J. von Bardeleben, *Materials Science Forums* **10-12** (1986) pp. 1223-1228 (1986), Trans. Tech. Ltd., Switzerland.
9. N. Newman, W.E. Spicer, T. Kendelewicz and I. Lindau, *J. Vac. Sci. Technol.* **B4**, 931 (1986) and references therein.
10. A.B. McLean, R.H. Williams and J.F. McGilp, *Solid State Commun.*, in press.
11. With the exception of the annealed Ag/GaAs diodes, all of the unannealed and annealed diodes formed on the air-exposed surfaces were found to have electrical characteristics which were consistent for all of the diodes measured on each of the samples. Only in the case of the annealed air-exposed

Ag/GaAs diodes what a wider variation on one of the samples found. The I-V barrier height for the diodes on these inconsistent sample were found to sporadically range from ~0.71-0.91 eV ($n=1.05$ -1.08), as compared to a value of 0.79 eV ($n=1.05$) which was consistently found for the other annealed Ag air-exposed sample.

12. The I-V technique is sensitive to barrier lowering mechanisms such as the image force and tunneling. If I-V barrier height determinations are used to infer the interface Fermi level pinning position, a correction due to the image force and tunneling should be added (for the values of doping and barrier height referred to here, the correction is on the order of 0.07 eV).

13. C.J. Madams, D.V. Morgan and M.J. Howes, *Electron. Lett.* **11**, 574 (1975).

14. S. Guha, B.M. Arora and V.P. Salvi, *Solid State Electron.* **20**, 431 (1977).

15. D. Coulman, N. Newman, G.A. Reid, Z. Liliental-Weber, E.R. Weber and W.E. Spicer, *J. Vac. Sci. Technol.* **A5**, 1521 (1987).

16. For an extensive review of recent developments on the subject of Schottky barriers, see L.J. Brillson, *Surf. Sci. Rep.* **2**, 123 (1982).

17. W.E. Spicer, P.W. Chye, P.R. Skeath, C.Y. Su and I. Lindau, *J. Vac. Sci. Technol.* **16**, 1427 (1979); W. E. Spicer, I. Lindau, P.R. Skeath, C.Y. Su, and P.W. Chye, *Phys. Rev. Lett.* **44**, 420 (1980).

18. W.E. Spicer, T. Kendelewicz, N. Newman, R. Cao, C. Mc Cants, K. Miyano, I. Lindau and E.R. Weber, *Appl. Surf. Sci.*, in press.

19. E. R. Weber, H. Ennen, U. Kaufmann, J. Windscheif, J. Schneider and T. Wosinski, *J. Appl. Phys.* **53**, 6140 (1982).

20. John F. McGilp, *J. Mater. Res.* **2**, 516 (1987); Max Hansen, Constitution of Binary Alloys, Mc Graw-Hill, New York (1958); C. Thomas Tsai and R. Stanley Williams, *J. Mater. Res.* **1**, 352 (1986); Donald D. Wagman, William H. Evans, Vivian B. Parker, Richard H. Schumm, Iva Halow, Sylvia M. Bailey, Kenneth L. Churney and Ralph L. Nuttall, *Journal of Physical and Chemical Reference Data* **11**, pp. 2-1 to 2-379 (1982) and references therein.

21. J. Pallix, C.H. Becker and N. Newman, *MRS Bulletin* **12**, 52 (1987); J.B. Pallix, C.H. Becker and N. Newman, *J. Vac. Sci. Technol.*, in press.
22. Perry Skeath, C.Y. Su, I. Hino, I. Lindau and W.E. Spicer, *Appl. Phys. Lett.* **39**, 1269 (1981); R.Z. Bachrach, R.S. Bauer, J.C. McMenamin and A. Bienconi, *Inst. Phys. Conf. Ser.* **43**, 1073 (1979).
23. T.R. Ludeke, T.-C. Chiang and T. Miller, *J. Vac. Sci. Technol.* **B1**, 581 (1983).
24. J.H. Weaver, M. Grioni and J. Joyce, *Phys. Rev. B* **31**, 5348 (1985).
25. G.P. Schwartz, G.J. Gualtieri, J.E. Griffith, C.D. Thurmond and B. Schwartz, *J. Electrochem. Soc.* **127**, 2488 (1980); T. Sands, J. Washburn, and R. Gronsky, *Materials Letters* **3**, 247 (1985).

*LAWRENCE BERKELEY LABORATORY
TECHNICAL INFORMATION DEPARTMENT
UNIVERSITY OF CALIFORNIA
BERKELEY, CALIFORNIA 94720*