The Last Byte

The Art of Certifying Analog/Mixed-Signal Circuits

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■ **We can be** proud that the semiconductor industry has had a compound annual growth rate (CAGR) more than double the worldwide GDP for the past two decades. This success does not come without a reason. We have lived up to all challenges in making better electronics that are increasingly versatile, use less power, and also come in a smaller form factor.

The physical world surrounding us is intrinsically analog. Our five senses are based on processing analog signals. We use radio waves to receive and transmit information. To stay on our CAGR curve, which other industries may envy, we need to cater to human needs better by building integrated systems that can compute, sense, communicate, and interact with the surrounding environment. For this, pursuing a chip-integrated solution is appealing technically and economically.

Mixed-signal SoCs bring some bad news. Pushing quite a bit of analog content into a SoC is not a trivial job. As we strive to offer richer functionality to the end user, the analog components we would like to squeeze onto the chip are getting bigger and more complex.

Technology scaling is not necessarily on our side either. While it has made digital transistors tinier and faster, it does not always give us better analog devices. At smaller technology nodes, transistors can actually have worse analog characteristics and matching properties; they become more prone to process variations and noise. Analog/RF interfaces and high-speed I/Os, or anything else of a similar analog nature which we desire on a SoC, often break more easily and in different ways than their digital friends.

Today, design of big digital chips is empowered almost entirely by standardized EDA tools and flows. Much less tool support is available to analog designers and mixed-signal integration engineers. All these troubles have made analog test and integration arguably the biggest bottleneck in the SoC design flow, a somewhat astonishing fact given that mixed-signal SoCs are often a big-D and small-A system by the measures of device count and silicon area.

Help may be on the way if we become smarter at various aspects of analog test and verification. Judiciously optimizing test setups, deploying built-in tests, and tuning by reusing the digital processing power already there on the chip can go a long way to reining in test time and cost. In addition to making use of human expertise, leveraging machine intelligence has the promise of reducing the needed silicon measurements and/or simulation data and enabling low-cost alternative tests. Thinking about paradigm changes in analog design and modeling, deriving language-level verification support, and adapting existing digital tools to analog problems will add to our arsenal and help us deal with our grand challenges.

We are still some distance away from the era of push-button test and integration of analog/mixed-signal circuits. To get there, we will need to build systematic methodologies across several broad and critical areas: circuit design, design-time validation, test methodology and technology, and test cost reduction. With this, we may someday transform our

Digital Object Identifier 10.1109/MDAT.2014.2370852
Date of current version: 16 January 2015.

practice, an exercise of art to a great extent as it stands now, to that of engineering science. ■

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