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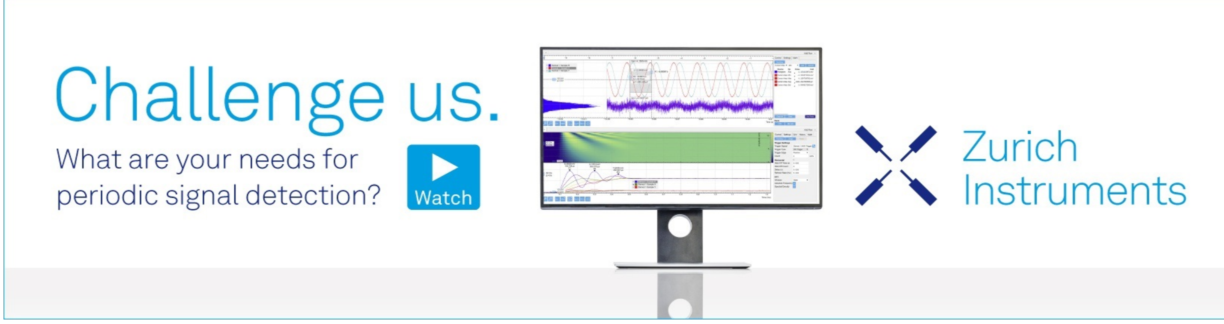

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ABSTRACT

We have demonstrated non-polar GaN power diodes (Schottky barrier diode and *p–n* junction diode) on foreign substrates featuring the true-lateral *p–n* and metal–semiconductor junctions. The diodes were fabricated on GaN islands laterally overgrown on the mask-patterned sapphire and Si substrates by metalorganic vapor phase epitaxy. The anode and cathode were formed on the opposed *a*-plane sidewalls of the island, making the device architecture essentially like the 90° rotation of the desired true-vertical power diodes. The ideality factor of the Schottky barrier diode remained 1.0 (from 1.00 to 1.05) over 7 decades in current. Specifically, a high critical electric field of 3.3 MV/cm was demonstrated on the *p–n* junction diode with avalanche capability. These performances reveal a strong potential of non-polar GaN with the true-lateral junctions for high power applications.

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GaN has wide bandgap, high critical electric field, and high electron saturation velocity, making it an ideal candidate for power switching electronics.[1] However, the development of GaN-based power electronics is still hampered by the low production yield and high cost of GaN native substrates with low threading dislocation density (TDD)—a key material metric to achieve high breakdown performance.[2] Alternatively, epitaxial lateral overgrowth (ELO) is known to render low-TDD GaN in the overgrown regions (wings) on inexpensive foreign substrates. ELO has in the past few decades evolved into a variety of derivative and associated techniques represented by pendeoepitaxy and aspect ratio trapping (ART) growth. These techniques are capable of further reducing threading dislocations (TDs) during epitaxy growth.[3–6] However, the unavoidable regeneration of considerable TDs at coalescence (i.e., the joining of adjacent GaN islands into continuous thin film) boundaries leads to periodic defective regions in GaN thin film which are detrimental for high-performance optical and power electronic devices.[3,5] As a result, there has been very few reports on the power electronics fabricated on the ELO-GaN on foreign substrates. In order to circumvent the coalescence-related issue, an effective yet straightforward approach should be to fabricate devices on the non-coalesceced GaN islands with in particular, tailored device architecture.

Here we demonstrated the fabrication of power devices on the non-coalesced GaN islands which were laterally overgrown from the mask-patterned foreign substrates to prevent the regeneration of TDs at coalescence stage. As schematically illustrated in Fig. 1, first, $Si_3N_4/SiO_2/Si_3N_4$ mask layers were patterned onto the foreign substrates-either (0001) sapphire substrate or AlN-nucleation layer (NL)/(111) Si template-forming high-aspect ratio serpentine-like channels [Fig. 1(a)]. The shape of the window region is ultra-long stripe (∼1 cm long and 2 μm wide) along *m*-direction. Then, the mask-patterned substrates were subject to metalorganic vapor phase epitaxy (MOVPE). Specifically, after GaN was nucleated on the bottom window region, a proprietary ART growth of GaN was carefully performed within the 3D serpentine channel to filter out most TDs [Fig. 1(b)].[7–9] After GaN island emerged from the top window region, the ELO was carried out accompanied by the *in situ* n^+/n^- doping for a Schottky barrier diode (SBD) [Fig. 1(d)] or $n^+/n^-/p$ doping for a *p–n* junction diode (PND)

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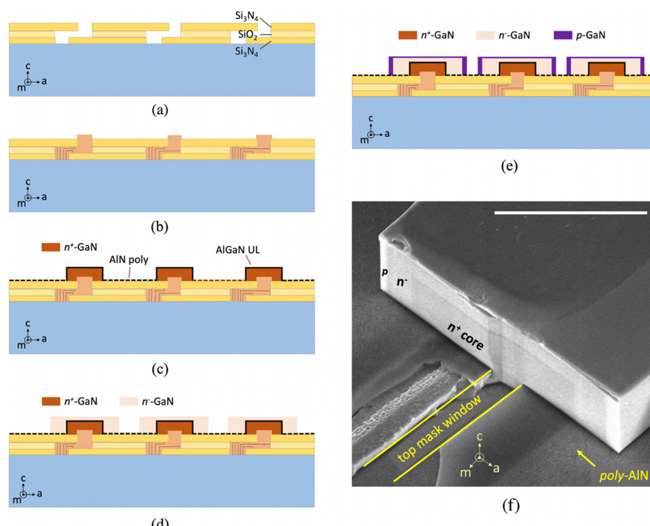

FIG. 1. (a)–(e) Schematic illustrations of the growth of GaN islands with rectangular core–shell doping profile: (a) serpentine-channeled mask patterned on foreign substrates; (b) the aspect ratio trapping (ART) growth of GaN via serpentine-channeled mask; (c) first stage lateral overgrowth of n^+-GaN by *in situ* doping of Si_{Ga} followed by AlGaN underlayer (UL) to intentionally introduce parasitic *poly*-AlN on the mask; (d) second stage lateral overgrowth of n^--GaN (for both SBD and PND); (e) third stage lateral overgrowth of *p*-GaN via *in situ* doping of Mg_{Ga} (for PND only). (f) The angled-view scanning electron microscopic image shows the rectangular core–shell doping profile of the GaN island and parasitic deposition of poly-AlN on the top SiN_x mask. The boundary of polycrystalline AlN layer on the mask is in line with the inserted AlGaN UL which is sandwiched between the n^--GaN shell and n^+-GaN core. The scale bar is 10 μm.

[Fig. 1(e)]. Specifically, we carried out the *in situ* n^+/n^- doping on both sapphire and AlN-NL/Si substrates and $n^+/n^-/p$ doping on sapphire substrate in this work. After growing the n^+-GaN core ([Si] $\sim 5\times10^{19}\,\mathrm{cm^{-3}}$), an n^+-$Al_{0.2}GaN$ underlayer (UL) of 15 nm thickness was inserted [Fig. 1(c)] to form parasitic layer of polycrystalline AlN on the SiN_x mask. This was to suppress desorption of Si from the mask and reduce unintentional incorporation of Si into the subsequent n^--GaN.[10] The AlGaN UL was heavily n-type doped ([Si] $> 1\times10^{19}\,\mathrm{cm^{-3}}$) so that the series resistance was made negligible compared to the overall resistance of the diode (see supplementary material). Then, the n^--GaN drift layer was grown with lateral thickness varying from 2.5 to 10 μm [Fig. 1(e)]. On top of that, *p*-GaN ([Mg] $\sim 3\times10^{19}\,\mathrm{cm^{-3}}$) was grown for PND with lateral thickness of $\sim$2 μm followed by ultra-thin p^+-GaN ([Mg] $> 10^{20}\,\mathrm{cm^{-3}}$) to improve Ohmic contact [Fig. 1(e)]. The growth parameters were adjusted in favor of the non-polar *a*-plane GaN growth throughout the ELO. The as-grown GaN stripe features rectangular core–shell n^+/n^- or $n^+/n^-/p$ doping profiles as a result of the parasitic *c*-plane growth. The angled-view scanning electron microscopy (SEM) image of the as-cleaved GaN island (one with the shortest n^--GaN lateral thickness of 2.5 μm) is shown in Fig. 1(f). The rectangular core–shell doping profile of $n^+/n^-/p$ and polycrystalline AlN onto the mask can be clearly distinguished.

A series of device processing steps were then implemented to fabricate SBD and PND characterized by the true-lateral *p*–*n* and metal–semiconductor junctions. As schematically depicted in Fig. 2(a), after patterning of Ni hard mask to cover roughly half of the stripes, Cl_2-based inductively coupled plasma-reactive ion etching (ICP-RIE) was utilized to tailor the shape of ultra-long stripe into shorter island arrays [Fig. 2(f)] and also to expose the *a*-plane n^+-GaN as a new sidewall of the island [Fig. 2(b)]. Then, for SBD, Ti/Al/Ni/Au was deposited onto the n^+-GaN sidewall with rapid thermal annealing (RTA) to form the Ohmic contact, while Ni/Au was deposited onto the opposed n^--GaN sidewall for the Schottky contact. For PND, Ni/Au/Ni was deposited onto the *p*-GaN sidewall of the island which serves a dual purpose. On one hand, it serves as hard mask to protect the underlying *a*-plane *p*-GaN during the second ICP-RIE process where the topmost *c*-plane *p*-GaN was removed. On the other hand, it also serves as the *p*-type Ohmic contact after a RTA treatment [Fig. 2(d), right]. It is fortunate that the possible plasma damages caused to the topmost *c*-plane of the island are less of an issue compared to the

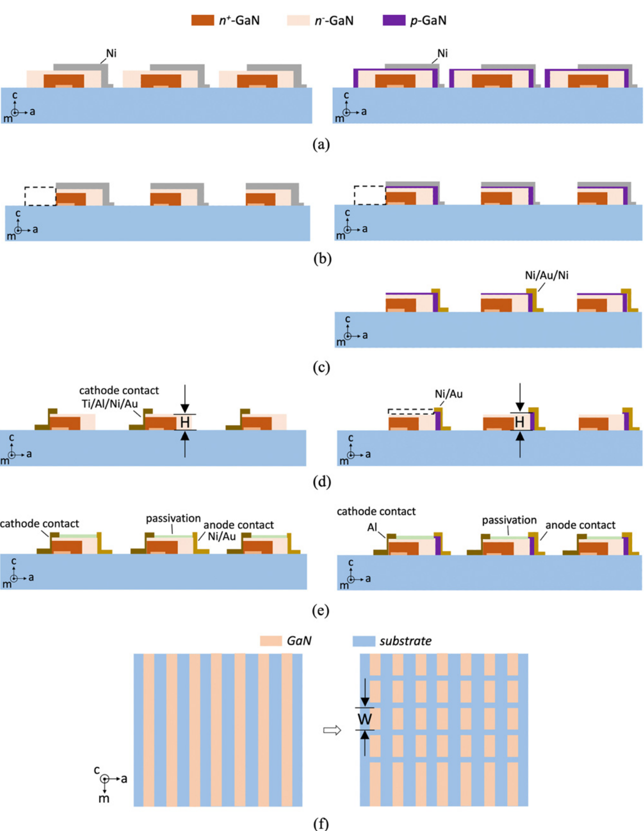

FIG. 2. (a)–(e) Cross-sectional schematic illustrations of the processing of non-polar true-lateral SBD (left column) and PND (right column) (the serpentine-channeled mask is omitted for simplicity): (a) Ni hard mask patterned for Cl_2-based ICP-RIE; (b) selective area ICP-RIE to tailor the island shape and to fully expose n^+-GaN; (c) PND (right): patterning of Ni/Au/Ni both for a second ICP-RIE and for using as anode contact; (d) PND (right): selective area Cl_2-based ICP-RIE to remove most of top p-type GaN, SBD (left): deposition of Ti/Al/Ni/Au onto the n^+-GaN sidewall for cathode contact; (e) PND (right): deposition of Ti/Al/Ni/Au onto the n^+-GaN sidewall for anode contact and passivation by polyimide, SBD (left): deposition of Ni/Au onto the *p*-GaN sidewall for anode contact and passivation by polyimide. (f) Plan-view schematic illustration of (b) where the ultra-long GaN stripes (left) are tailored into shorter GaN island arrays (right).

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otherwise necessary mesa etch where other crystallographic planes of GaN are subject to plasma damages, thanks to the superior chemical stability of $+c$-*plane* GaN among all the crystallographic planes.[11] Afterwards, Al was sputtered onto the n^{+}-GaN sidewall to form the Ohmic contact. Figures 3(a) and 3(b) are angled-view SEM images of the fabricated PND arrays and the magnified-view of a single PND, respectively. The GaN island has a typical H of 5 μm along c-direction as well as designed W of 100 μm and 200 μm along m-direction [W and H are schematically indicated in Figs. 2(d) and 2(f), respectively]. As it appears, the fabricated diode is characterized by the true-lateral p–n junction as well as metal contacts formed onto the opposed non-polar sidewalls of the island, making the architecture essentially like a true-vertical diode structure being rotated through a right angle and thus allowing to handle high current and field without crowding issues seen in a quasi-vertical structure.[12] Furthermore, the architecture can make the most of ELO process by enabling the drift layer—the critical segment to withstand high blocking voltage—to have lowest possible TDD by virtue of the ELO.

As schematically shown in Fig. 3(c), in order to reduce leakage current and increase breakdown voltage, aside from the passivation by polyimide, field plate and positive beveled p–n junction (a positive bevel angle is defined as one where more material is removed from the edge when progressing from the heavily doped side to the lightly doped side of the p–n junction and thus it is preferable for the termination of the single high-voltage junction with high-voltage power rectifiers)[13] were utilized as edge termination schemes to mitigate the electric field crowding and expand the depletion region at the surface. The field plate is wrapping around the three outer surfaces of island (i.e., top $+c$-plane and two opposed m-plane sidewalls). In particular, the positive beveled p–n junction was created at the bottom $-c$-plane surface (N-polar) of the island after a 25% tetramethylammonium hydroxide (TMAH) solution wet etch probably because of more stable N-polar p-GaN against TMAH etch than adjacent N-polar n^{-}-GaN, as is indicated by the SEM image in Fig. 3(c).

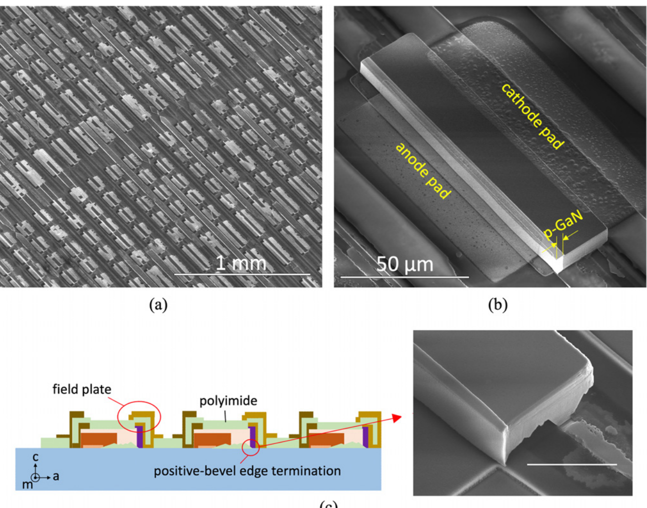

FIG. 3. The angled-viewed SEM images of (a) the fabricated PND arrays and (b) the magnified view of a single PND. (c) (left) The schematic illustration of the field plate and positive-bevel edge termination and (right) the angled-view SEM image of the GaN island where the positive beveled p–n junction as depicted in (c) (left) was created at the $-c$-plane bottom surface (N-polar) of the island after a 25% TMAH solution wet etch probably due to more stable N-polar p-GaN than n^{-}-GaN. The scale bar in (c) (right) is 10 μm.

We measured the electrical performances of the a-plane GaN SBD on Si and sapphire and the a-plane GaN PND on sapphire by Agilent B1505A Power Device Analyzer, respectively. In order to calculate current density, the device area was regarded as the total a-plane cross-sectional area (i.e., $W \times H$ where W and H are previously mentioned) of the island based on the structure and nature of the a-plane true-lateral diodes.

The forward I–V characteristics of the SBD on Si are shown in Figs. 4(a) and 4(b). The ideality factor n remains at a plateau of 1.0 (from 1.00 to 1.05) spanning over 7 decades of current (i.e., from $<10^{-7}$ A/cm^2 to 1 A/cm^2), a low turn-on voltage of 0.59 V, and a high on/off ratio of over 10^{10} are demonstrated, suggesting that the laterally overgrown n^{-}-GaN has superior material quality with low TDD after the ART growth in the serpentine channel. In addition, the lowered Schottky barrier height of non-polar GaN than that of $+c$-plane GaN also contributes to the observed low turn-on voltage (see supplementary material).[14,15] The forward specific on-resistance is calculated to be 0.6 mΩ cm^2 at 1 kA/cm^2. A further reduction in resistance is expected through device structure optimization, such as shortening the drift layer thickness according to the doping concentration. Figure 4(c) shows the reverse I–V characteristics of the SBD and a soft breakdown voltage of 175 V is achieved at leakage current density of 0.05 A/cm^2. The reverse leakage current could be suppressed to increase breakdown voltage with some proper edge termination designs in our future work. The forward and reverse I–V characteristics of the SBD on sapphire displayed similar performance.

Figures 5(a) and 5(b) show the I–V characteristics of the a-plane GaN PND on sapphire under forward and reverse bias, respectively. The forward specific on-resistance is measured to be 1.6 mΩ cm^2 at 1 kA/cm^2, and a high on/off ratio of 10^{10} is achieved. The lowest ideality factor ($n = 1.8$) is in the lower range of the reported values for a GaN PND which are typically larger than 2 owing to the SRH (Shockley–Read–Hall) recombination and series resistance of p-GaN.[16,17] Under reverse bias, leakage current was below the detection limit at room temperature for at least a reverse voltage of 300 V, and the highest breakdown voltage V_{br} is measured to be 490 V on the best-performing PND with W = 100 μm. The reverse I–V characteristics at 75 °C and 125 °C are also plotted in Fig. 5(b). Specifically, it is observed that V_{br} displays a positive temperature dependence, characteristic of avalanche breakdown due to impact ionization multiplication. In addition to the good crystal quality, the high breakdown voltage and low leakage current were achieved in part owing to the aforementioned passivation and edge termination schemes consisting of field plate and the wet-etch induced positive beveled p–n junction. In addition, for PND with W = 200 μm, large leakage current was often observed which is believed to be caused by the prismatic stacking faults in the GaN stripes (see supplementary material).

Using the one-sided junction model for the p^{+}–n^{-} junction diode, critical electric field ε_{crit} at the planar junction interface over a breakdown voltage of V_{br} is then given by

$$\varepsilon_{crit} = \sqrt{\frac{2e\,|N_d - N_a|\,V_{br}}{\epsilon_0 \epsilon_r}}\,(\text{non-punch through}), \qquad (1)$$

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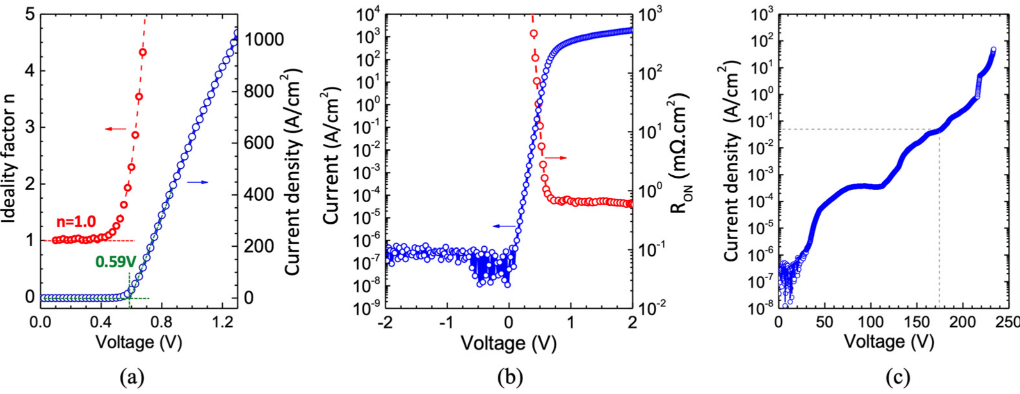

FIG. 4. *I–V* characteristics of the GaN SBD: (a) Forward *I–V* characteristic curve plotted in linear scale showing a turn-on voltage of 0.59 V, the ideality factor *n* remains 1.0 from 0.10 to 0.42 V corresponding to 7 decades in current; (b) current density and the specific on-resistance R_{ON} (plotted in semilogarithmic scale) vs forward bias *V*; (c) reverse *I–V* characteristics showing a soft breakdown voltage of 175 V occurring at 0.05 A/cm^2.

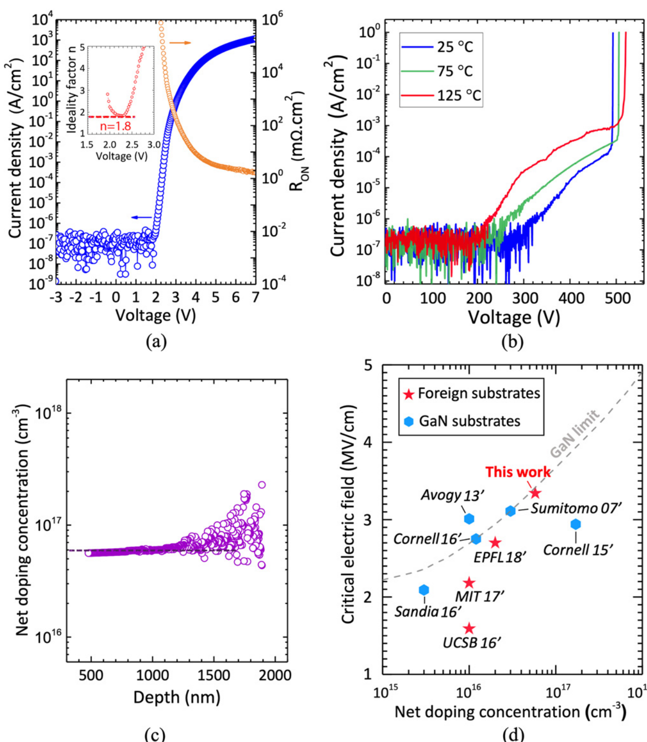

FIG. 5. (a)–(b) *I–V* characteristics of the GaN PND with edge termination: (a) current density and specific on-resistance R_{on} vs forward bias *V* (both are plotted in semilogarithmic scale), the inset shows the ideality factor *n* plotted against *V* of 1.5–3.0 V; (b) reverse *I–V* characteristics under 25 °C, 75 °C, and 125 °C, respectively, the breakdown voltage V_{br} increases from 490 V at 25 °C to 520 V at 125 °C, suggesting impact ionization-induced avalanche multiplication and breakdown. (c) Net doping concentration vs depletion depth, extracted from the *C–V* characteristics of GaN PND in the supplementary material. (d) Benchmark of critical electric field ε_{crit} vs net doping concentration $|N_d - N_a|$, where the simulated curve is calculated based on the impact ionization model under NPT case.

or

$$\varepsilon_{crit} = \frac{e|N_d - N_a|W_d}{2\epsilon_0\epsilon_r} + \frac{V_{br}}{W_d}\ \text{(punch through)}, \qquad (2)$$

wherein $|N_d - N_a|$ is the net doping concentration in which N_d and N_a are donor and compensated acceptor concentration in the depletion region on the n$^-$-doped side of the *p–n* junction. W_d is the depletion width. ϵ_0 is the vacuum permittivity, and *e* is electron charge. The relative permittivity ϵ_r is regarded as 9.5 for $\epsilon_\perp$ and as 10.4 for $\epsilon_\parallel$.[18]

Since V_{br} is obtained at 490 V at room temperature and $|N_d - N_a|$ is determined to be $6 \times 10^{16}\,\text{cm}^{-3}$ as shown in Fig. 5(c), according to the *C–V* profiling results of the PND available in the supplementary material, we can calculate the depletion width W_d at breakdown to be 3 μm, which is much shorter than the n^--GaN drift layer thickness of 8–10 μm in this PND, thus fitting into the non-punch through (NPT) scenario. Therefore, ε_{crit} is calculated to be 3.3 MV/cm (note that ϵ_r is 9.5 instead of 10.4 in an *a*-plane $p-n$ junction), making it the record high value of ε_{crit} in GaN devices on foreign substrate. It is worth mentioning that the calculated ε_{crit} from Eq. (1) represents the lower-bound based on the parallel-plane (ideal) breakdown voltage model, given that the perfect planar junction could not be achieved, the actual ε_{crit} should have been even higher despite the effective effort to minimize the electric field crowding at the edges in this work.[19,20]

On the other hand, ε_{crit} can also be derived in principle as a function of $|N_d - N_a|$ based on the model of impact ionization which is described by the following basic integral equations:[21]

$$1 - \frac{1}{M_n} = \int_0^{W_d} \alpha \exp[-\int_0^x (\alpha - \beta)dx']dx, \qquad (3)$$

$$1 - \frac{1}{M_p} = \int_0^{W_d} \beta \exp[\int_x^{W_d} (\alpha - \beta)dx']dx, \qquad (4)$$

where α and β are the electron and hole impact ionization coefficients, they are defined as the number of electron–hole pairs generated by a carrier per unit distance traveled, and they are functions of position

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and strongly dependent on the electric field which in turn is a function of position and net doping concentration.[21] W_d is the depletion width. M_n and M_p are the electron and hole multiplication factors. Avalanche breakdown occurs when M_n or M_p becomes infinitely large, leading to the integral for electrons or holes being 1. Since there exists no closed-form solution for the integral, we performed a finite-element analysis to investigate the dependence of critical field with varying net doping concentration, and the reference values of α and β as a function of electric field were from a Monte Carlo work.[22] The simulated result of ε_{crit} vs $|N_d - N_a|$ assuming NPT case is plotted as the gray dashed line in Fig. 5(d), which could also be interpreted as the performance limit of unipolar power devices in GaN.[23] It can be seen that the critical field has a positive dependence on the net doping concentration, which is partially responsible for the high value of ε_{crit} found in our PND in which the drift layer has relatively high doping concentration. In comparison, our results are benchmarked in the same plot with other values of ε_{crit} and $|N_d - N_a|$ in the literature.[20,24–30] It should be noted that all the values of ε_{crit} are subject to recalculation based on the varying values of $|N_d - N_a|$, V_{br} and drift layer width W_d (in the case of PT) reported in each reference and a common value of ϵ_r (9.5 for $\epsilon_\perp$ and 10.4 for $\epsilon_\parallel$). Furthermore, the simulated curve under NPT case in Fig. 5(d) could also well apply to the referenced works under PT case after taking full account of the moderate values of W_d and $|N_d - N_a|$ in each of these cases.[24–29] Therefore, the closeness of each mark in Fig. 5(d) to the simulated GaN limit curve also serves as a good measure of device performance, by which our result on foreign substrate is shown to be comparable to the best results of GaN devices on GaN substrate.

In summary, power diodes featuring the true-lateral $p-n$ and metal–semiconductor junctions were fabricated on the GaN islands grown on foreign substrates by a combination of ELO and ART growths. Such architecture was capable of unleashing the true potential of ELO by utilizing the low TDD region grown by ELO as the drift layer of a power device and of circumventing the problematic coalescence process of ELO, which might otherwise be inappropriate for power electronics. The good electrical performances were achieved on the fabricated SBD and PND, as highlighted by the avalanche capability demonstrated in the GaN devices on foreign substrates, revealing that the non-polar true-lateral GaN device is a promising candidate for high power applications.

See the supplementary material for more details of (1) bandgap of the GaN/AlGaN/GaN heterostructure employed in this work, (2) prismatic stacking faults in the GaN stripes, (3) *C*–*V* profiling measurement, and (4) estimate of Schottky barrier height of the *a*-plane SBD.

AUTHORS' CONTRIBUTION

J.W. and G.Y. contributed equally to this work.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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