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A Broadband Transimpedance Amplifier for Optical Receivers

THESIS

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MASTER OF SCIENCE

in Electrical Engineering and Computer Science

by

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DEDICATION

To

my parents

Whom I am deeply in debt to, forever.

Table of Contents

LIST OF FIGURES

LIST OF TABLES

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ABSTRACT OF THE THESIS

A Broadband Transimpedance Amplifier for Optical Receivers

By

Alireza Karimi Bidhendi

Master of Science in Electrical Engineering and Computer Science

University of California, Irvine, 2018

Professor Payam Heydari, Chair

This work presents a broadband transimpedance amplifier (TIA) for optical communication serial link front-ends, achieving 50 GHz of bandwidth. A brief background on the applications of TIAs, their design specifications and performance enhancement techniques are presented. Next, a TIA is introduced which is comprised of three stages and uses several techniques to enhance the bandwidth while maintaining a flat frequency response and limit the frequency peaking. The first stage is a shunt-peaked, shunt-series feedback stage incorporating a transformer-based positive feedback. The second and third stages are RC-degenerated common-emitter stage and an inductively degenerated emitter follower. An integrated 100 fF metal-insulator-metal capacitor shunts the TIA input to emulate the photo-diode junction capacitor. Analytical analysis and circuit and electromagnetic simulations is performed and compared with the measured results. Design is implemented in TowerJazz 0.13µm SiGe BiCMOS process occupying 0.58 mm^2 (including pads) of die area and dissipates 24 mW from a 2 V supply voltage (resulting in an energy efficiency metric of less than 0.5 pJ/bit). Transimpedance gain of 41 dBΩ and an input-referred current-noise spectral density of 39.8 pA/√Hz over the bandwidth are measured. The TIA achieves an open eye diagram at 50 Gb/s with a random rms jitter of 2.3 ps, including the jitter contribution of the test fixture and input source.

INTRODUCTION

The growing demand for high-speed data access for applications such as cloud computing, media streaming, mobile Internet access, and most recently Internet of Everything requires infrastructures that can handle Tera-bit-per-second communication such as data centers with high operation speed at every level of architecture hierarchy [1]. This demand has been created due to a sharp increase in the number of users and wireless sensor nodes for Internet of Things each of which starting to use multiple-input-multiple-output architectures [2] for faster wireless connectivity. Wearable and implantable bioelectronics for diagnose and health care applications [3], [4], [5], [6], [7], [8] further accelerate this trend. As such, new industry standards are being developed to respond to this high-speed data communication demand in different application spaces [9], [10], [11]. The current standard for supporting 100-Gb/s link operation uses 4 lanes, each operating at 25-28 Gb/s. For 400-Gb/s data rates and beyond, however, various design specifications and challenges should be taken into consideration, including (1) the link power efficiency (pJ/bit), (2) heat dissipation and maximum number of electrical-to-optical interface (I/O density), (3) insertion loss (IL), (4) bit-error-rate (BER), and (5) implementation complexity. A few architectures with different signal modulations have been proposed, among which non-return-to-zero (NRZ) and pulse amplitude modulation (PAM)-4 for different applications are the most likely candidates. PAM-4 achieves lower IL for the same bit-rate owing to half-speed symbol rate compared to NRZ. However, the vertical eye-diagram opening of PAM-4 is reduced by a factor of 3 (equivalent to 9.5 dB lower SNR). In addition, higher linearity and output signal amplitude are required [12]. The higher loss in SNR in PAM-4 modulation causes NRZ to be a viable, if not preferred, modulation for short-range

communication links such as Ultra-Short Range (USR), Extra-Short Range (XSR) and Very-Short Range (VSR), as defined by Optical Interconnect Forum (OIF) [9]. Furthermore, to reach an acceptable BER ($< 10^{-12}$) in a PAM-4 scheme, forward error correction (FEC) and equalization techniques should be implemented to reduce the residual inter-symbol interference (ISI), leading to high hardware complexity [13]. Recently, a wireline optical link using a high-speed VCSEL was presented in [14]. New fabrication technologies are also introduced to facilitate high data-rate electrical-optical interfaces on a silicon substrate with a small increase in fabrication cost compared to bulk CMOS processes. In [15], 50-56 Gb/s NRZ modulators and photo-diode (PD) are presented, demonstrating that NRZ remains a viable modulation for very high-speed links on silicon.

Being a fundamental circuit element, diodes are used for different purposes such as ESD protection, microwave and mm-wave signal generation ([16]), voltage regulation, light emission and light detection. In optical links LEDs and PDs are used in the transmit and receive side respectively, often on a separate module because of difficulties in integration with the back-end circuitry.

To achieve high-speed data rates with small number of channels, data is serialized in the optical transmitter before being sent out through the optical channel. In the receive side, a photo-diode creates an electrical current proportional in magnitude to the absorbed light intensity. Figure 1 shows a typical system block diagram of a conventional single-channel optical receiver. A transimpedance amplifier (TIA) is driven by the PD to amplify this electrical current to a proper voltage level for the limiting amplifier (LA). The LA provides additional gain to create a rail-to-rail signal for the subsequent decision circuits to recover the data and clock (through clock and data recovery circuit CDR) with minimum BER. LA is usually necessary and co-designed

with the TIA since the TIA alone cannot reach enough output voltage swing due to several trade-offs between noise, bandwidth and ISI. Finally, the data is deserialized using the recovered clock and is passed to a digital signal processor.

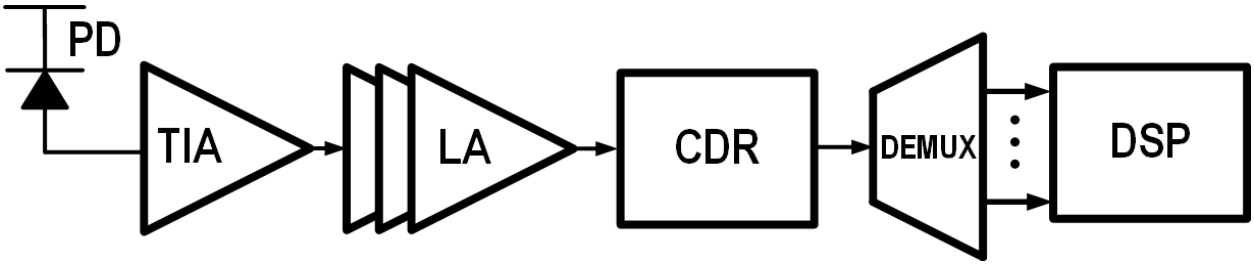

Figure 1 General block diagram of an optical receiver.

This work focuses on designing a broadband TIA in a 0.13μm SiGe BiCMOS process for very high data rate applications. This TIA provides 41 dBΩ of transimpedance gain across a 50-GHz bandwidth and shows an open eye diagram for 50-Gb/s data rate. Chapter 1 presents an overview on TIA specifications and link budget calculations. Chapter 2 expands on the analysis and design of each stage of the TIA. Chapter 3 presents simulation results and discussions on the targeted and achieved performance of the TIA. Chapter 4 illustrates complete measurement results, and chapter 5 concludes this thesis.

Transimpedance amplifier design overview

1.1. Performance specifications

This section briefly discusses important performance metrics for a TIA to be used in an optical link.

1.1.1. Gain and bandwidth

For midband frequencies, the transimpedance gain is defined as the ratio of the output voltage swing over the input current of the TIA. The current reaching the TIA is less than the current available from the source since TIA's input is shunted by the PD's parasitic capacitor C_D. At high frequencies, the gain starts to drop and the point where it reaches 3 dB lower than the midband value determines the bandwidth. Some techniques have been introduced [17], [18], [19] to extend the bandwidth, usually at the cost of higher in-band ripples or frequency peaking. Frequency peaking is accompanied with group delay variation (later in this section) resulting in increased jitter and closer eye diagram. The bandwidth is roughly set to 0.7 times of the data rate for NRZ modulation as a compromise between integrated noise and ISI [20].

1.1.2. Noise

Having a small input impedance, the noise of TIAs are specified in terms of their input-referred noise current only. Like any amplifier, the input noise of TIA is frequency dependent which is shown through a power spectral density $\overline{i_{n,in}^2}$. In a broadband application like ours, the final quantity of interest is the overall integrated noise over the bandwidth (usually from DC to at least 3-dB bandwidth). Other measures of noise like Noise Figure cannot be applied to these TIAs easily as the source impedance is not 50Ω and is poorly defined (it is equal to the C_D combined with the interfaces such as bondwire between the PD and TIAs input). Higher values of C_D deteriorate the noise performance so it is desired to use a technology to build a PD with high responsivity yet small parasitics.

1.1.3. Maximum input current

The TIA's input overload current from photodiode is expressed as [21] and [22],

$$i_{ovl}{}^{pp} = \min\{\frac{v_{i,ovl}{}^{pp}}{Z_{in}}, \frac{v_{o,ovl}{}^{pp}}{Z_T}\} \quad (1)$$

where $v_{i,ovl}{}^{pp}$indicates the maximum allowable peak-to-peak swing of the input, $v_{o,ovl}{}^{pp}$ is the maximum allowable peak-to-peak swing of the output, and Z_{in} and Z_T are the input impedance and transimpedance gain of the TIA, respectively. As a more precise and restrictive definition, the input overload current is defined as the maximum input current amplitude that TIA can tolerate, given a specific bit-error rate or jitter values. From (1), two observations are made: (a) As the input impedance is reduced, the maximum tolerable input overload current will increase; (b) The input overload current is limited by maximum allowable input or output voltage swing depending on whether the front-end gain compression first occurs in the input of TIA or its output. For high gain, low input impedance TIAs covering wide bandwidths, the compression occurs first in the output in most cases.

1.1.4. Group delay variation

Non-linearity of the transimpedance transfer function phase can cause data-dependent jitter, and thus needs to be carefully characterized. For practical evaluations of this spec, group delay variation (GDV, units of seconds) is defined as negative of the phase derivative with respect to time. Large variations in GDV means different portions of the data are delayed with unequal values, closing the eye diagram horizontally. As a rule of thumb, GDV should be about 10% of bit period [22].

1.1.5. Jitter

Besides the jitter introduced as a result of GDV, large input signals can further increase the jitter. To account for this, the input signal power is swept across the dynamic range and the resulted jitter is measured. Further discussions are given in [22] about how to separate different jitter types and their root cause.

1.2. Link budget calculation

Link budget requirements for maximum tolerable timing jitter, minimum output swing, dynamic range, and minimum transimpedance gain of a TIA operating with a BER of 10^{-12}, 50 GHz bandwidth and a data rate of 50 Gb/s are briefly described**.**

1.2.1. Maximum Tolerable Timing Jitter and Minimum Required Output Swing

The sensitivity of an optical receiver (i.e., minimum detectable input power) is degraded due to effects such as dispersion in the optical fiber, timing jitter from the TIA, and threshold offset in the decision circuit following the TIA. Extra power needs to be transmitted to account for these degrading effects. Power penalty due to timing jitter, PP_{jitter}, is expressed by

$$PP_{jitter} = \frac{1 - (B\sigma_{\Delta t})^2 \left(\frac{2\pi^2}{3} - 4\right)}{\left[1 - (B\sigma_{\Delta t})^2 \left(\frac{2\pi^2}{3} - 4\right)\right]^2 - 8Q^2 \left[(B\sigma_{\Delta t})^2 \left(\frac{\pi^2}{3} - 2\right)\right]^2} \quad (2)$$

where $\sigma_{\Delta t}$ denotes timing jitter or the standard deviation of the time variation Δt, B is the bit rate, and Q is the personick factor which is set to 7 for a BER of 10^{-12} [23]. From (2), for a maximum power penalty of 1 dB, the timing jitter $\sigma_{\Delta t}$ needs to be less than 12% of the bit interval, which becomes equal to 2.4 ps RMS (root-mean-square) for a 50 Gb/s data rate.

Power penalty due to threshold offset, $PP_{th,offset}$, in the decision circuit is expressed by [21]:

$$PP_{th,offset} = 1 + \frac{v_{th,DC}}{{v_{o,min}}^{pp}} \quad (3)$$

where ${v_{o,min}}^{pp}$ is the minimum peak-to-peak output swing of the TIA, and $v_{th,DC}$ is the threshold offset in the decision circuit. From (3), for a maximum decision threshold offset of 5 mV and a maximum power penalty of 1 dB, the peak-to-peak output swing should be greater than 20 mV.

1.2.2. Dynamic Range

The dynamic range of an optical receiver determines the range of input power for which the a specific BER is achieved. The lower-end of the TIA's dynamic range is determined by sensitivity and its upper-end is set forth by photodiode overload current (discussed in previous section). The TIA sensitivity is expressed as a function of the signal-to-noise ratio SNR, and the mean-square input-referred noise-current spectral density $\overline{i_{n,in}^2}$ over the TIA's bandwidth (BW) [24], i.e.,

$${i_{sens}}^{pp} = SNR\sqrt{\overline{{I_{n,in}}^2}.BW} \quad (4)$$

Assuming the TIA to have an RMS input-referred noise-current spectral density less than 35 pA/√Hz over a 50 GHz BW, then for operation with an SNR of 14 dB – or a BER of 10^{-12} for non-return-to-zero (NRZ) modulation – the minimum sensible input current ${i_{sens}}^{pp}$ is calculated from (4) to be 200 μA.

Assuming a 40 dBΩ TIA with a maximum peak-to-peak output overload swing ${v_{o,ovl}}^{pp}$ of 100 mV, the peak-to-peak overload current is calculated from (1) to be 1 mA.

1.2.3. Minimum Transimpedance Gain

The TIA is required to provide a minimum transimpedance gain to be able to detect the input random bit sequence at the edge of its sensitivity, where the minimum input current from photodiode is comparable with the input-referred noise-current of the TIA. The minimum required transimpedance gain Z_T is expressed by

$$Z_T = \frac{{v_{o,min}}^{pp}}{{i_{sens}}^{pp}} \quad (5)$$

Therefore, for an ${i_{sens}}^{pp}$ of 200 μA and a ${v_{o,min}}^{pp}$ of 20 mV, the minimum required transimpedance gain is calculated from (5) to be 40 dBΩ.

Transimpedance amplifier circuit design and analysis

2.1. Shunt-Series Feedback Stage Achieving G_m-Boosting

Three general approaches are adopted for the design of TIAs: (1) a shunt-shunt (input current, output voltage) resistive feedback amplifier as in [25], (2) an open-loop amplifier (e.g., bipolar common-base or CMOS common-gate) [20], and (3) a current-mode transimpedance amplifier [26]. The common-base topology imposes severe trade-offs on the main performance parameters, namely bandwidth, noise, and gain [20]. To relax these tight trade-offs, the two-stage shunt-series feedback amplifier of Figure 2, also misnamed as “regulated-cascode” (RGC), is commonly utilized. In Figure 2, the PD is modeled as a current source parallel with a capacitance C_{PD}. In most cases, the photodiode is implemented on a separate die than the TIA and packaging parasitics such as package lid capacitance and wirebonding inductances should be considered as well.

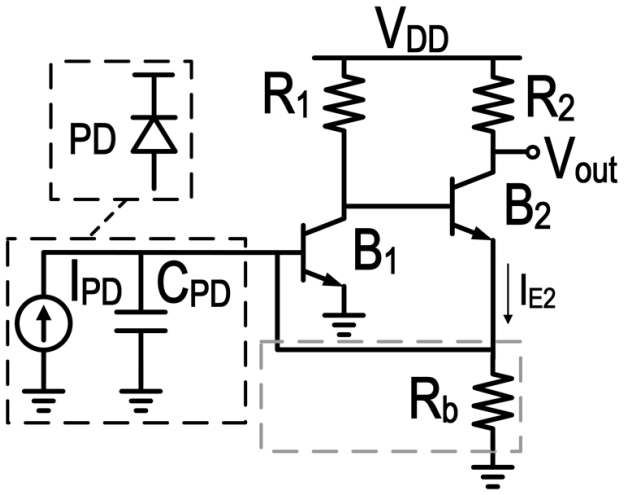

Figure 2 Basic circuit for the TIA with shunt-series (current-current) feedback

This TIA can be viewed as either (1) a common-base (B_2) transistor with a local feedback loop consisting of B_1 and R_1 or (2) a closed-loop current amplifier consisting of a two-stage open-loop amplifier (i.e., a common-emitter stage followed by another emitter-degenerated common-emitter stage) surrounded by a shunt-series resistive feedback R_b. The closed-loop amplifier's loop gain is $T_L \approx g_{m1}R_1g_{m2}(R_b||r_{\pi1})$. Using the H-parameters for analyzing the shunt-series feedback network and considering the loading effect of the feedback network on the open-loop amplifier, Figure 3 is derived, where the feedback elements are shown in gray. Neglecting base-collector capacitance C_μ, it is readily shown that the input impedance seen from current source I_{PD} is:

$$Z_{in} = \frac{1 + R_1(C_{\pi2} + C_P)s}{g_{m2}(1 + g_{m1}R_1)\left(1 + \frac{C_P s}{1 + g_{m1}R_1}\right)\left(1 + \frac{s}{\omega_{T2}}\right)} || \frac{R_{in}}{1 + \frac{s}{\omega_{in}}} \qquad (6)$$

where ω_{T2} is the transit frequency $\omega_{T2} = \frac{g_{m2}}{C_{\pi2}}$, C_P is the parasitic capacitance seen at the collector node of B_1 to ground, $R_{in} = R_b||r_{\pi1}$, $C_{in} = C_{PD} + C_{\pi1}$ and $\omega_{in} = \frac{1}{R_{in}C_{in}}$.

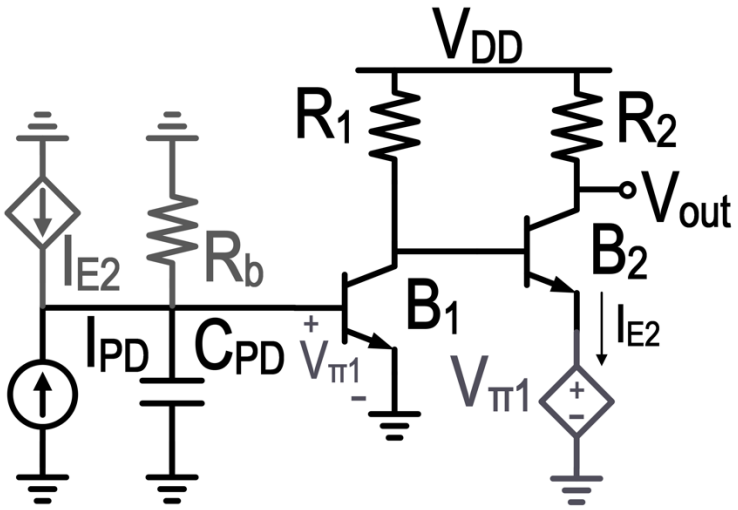

Figure 3 Open loop equivalent model of the TIA with shunt-series feedback

The input impedance contains a high frequency zero due to C_P and $C_{\pi 2}$, thereby causing peaking in its magnitude frequency response. At low frequencies, the impedance model is simplified to the familiar form $[g_{m2}(1+g_{m1}R_1)]^{-1}$. It is inferred that the negative feedback boosts the effective transconductance of B_2, thus pushing the TIA's input pole (normally dominated by the PD capacitor) to higher frequencies.

C_P also creates a high-frequency zero at approximately g_{m1}/C_P in the closed-loop transimpedance of this stage. The peaking in the transimpedance frequency response due to this zero should be considered, as it contributes to bandwidth enhancement. Ignoring the Early effect in transistor B_2 and solving the equations for Figure 3, the transimpedance is derived as:

$$Z_T = \frac{T_L Z_2 \left(1+\frac{s}{\omega_Z}\right)}{\left(1+\frac{s}{\omega_{in}}\right)(1+R_1 C_{\pi 2} s) + T_L \left(1+\frac{s}{\omega_{T2}}\right)\left(1+\frac{s}{\omega_Z}\right)} \tag{7}$$

where C_N is the loading capacitance at the output and we have:

$$\omega_Z = \frac{1+g_{m1}R_1}{R_1 C_P}, \quad Z_2 = \frac{R_2}{1+R_2 C_N s}, \quad T_L = (1+g_{m1}R_1) g_{m2} R_{in} \tag{8}$$

Assuming $T_L \gg 1$ and $\omega_{T2} \gg \omega_Z$, after rearranging the equation, we arrive at a more intuitive result:

$$Z_T \approx \frac{R_2\left(1+\frac{s}{\omega_Z}\right)}{(1+R_2C_N s)+\left(1+\frac{C_{in}+AC_{\pi 2}}{Ag_{m2}}s\right)} \tag{9}$$

where $A = 1 + g_{m1}R_1$. From (9), it is observed that the closed-loop feedback pushes the input pole to higher frequencies from its original value of g_{m2}/C_{in}. The output impedance seen from the collector of B_2 is multiplied by the loop gain, making the overall output impedance of the circuit to be very close to R_2.

2.2. Shunt-Series Feedback Stage Incorporating Shunt Peaking

The feedback amplifier of Figure 2 can operate up to a few GHz, as the input and output poles will eventually limit the bandwidth. Several bandwidth enhancement techniques have been investigated (e.g., see [27]). It has been shown that the bandwidth enhancement ratio (BWER) in CMOS amplifiers achieves an upper limit of 4.84 with the aid of a passive realizable network (pp. 394 in [27]). To save chip area and power, we avoid the higher-order passive networks introduced in [27], and choose the widely used shunt-peaking technique (i.e., inductor L_1 in series with R_1) in this design (Figure 4).

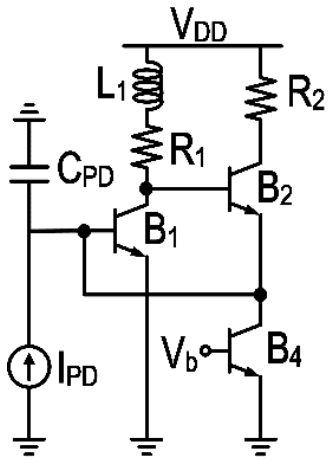

Figure 4 Shunt-peaked Gm-boosted amplification stage

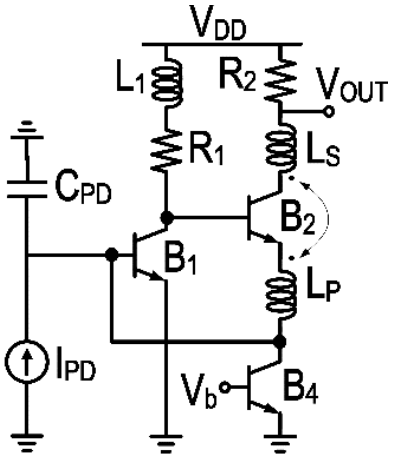

Figure 5 Dual feedback transformer-based TIA

The addition of the shunt-peaking inductor will create two poles and a zero in the feedback path (collector of B_1). This will translate into two zeros and one pole in the transimpedance transfer function, thus further increasing the bandwidth. Figure 6 shows the transimpedance frequency response for four values of L_1. The frequency peaking caused by the addition of L_1 is optimized in conjunction with subsequent amplification stages to extend the overall bandwidth. Note that, in practice, implementation of an inductor with very high self-resonance frequency will limit its size to few hundreds of pH, depending on the technology and accompanying metal stackup properties.

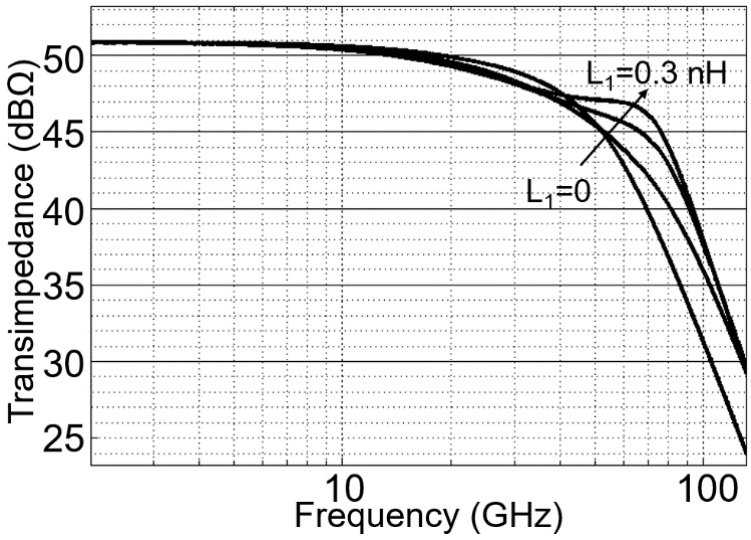

Figure 6 Simulated frequency response of the first stage vs. L_1. Higher L_1 causes more peaking in the high frequency response.

The transimpedance is derived from (7) by replacing R_1 with R_1+L_1s (neglecting C_P for simplicity):

$$Z_T \approx \frac{R_2\left(1+\frac{s}{\omega_{z,sp}}\right)}{1+a_1 s+a_2 s^2} \tag{10}$$

Where

$$a_1 = \frac{1}{\omega_{T2}} + \frac{C_{in}}{g_{m2}A} + \frac{1}{\omega_{z,sp}}\ , a_2 = \frac{1}{\omega_{T2}}\left(\frac{C_{in}}{g_{m1}} + \frac{1}{\omega_{z,sp}}\right)\ , \omega_{z,sp} = \frac{A}{g_{m1}L_1} \tag{11}$$

ω_{T2}, ω_{in} and A have the same definitions as in (6) and (9). From (10) we can estimate the location of the poles to be:

$$p_1 \cong \left(\frac{1}{\omega_{T2}} + \frac{C_{in}}{g_{m2}A} + \frac{1}{\omega_{z,sp}}\right)^{-1}, \qquad p_2 \cong \frac{\left(1+\frac{\omega_{T2}C_{in}}{g_{m2}A}+\frac{\omega_{T2}}{\omega_{z,sp}}\right)}{\left(\frac{C_{in}}{g_{m1}}+\frac{1}{\omega_{z,sp}}\right)} \tag{12}$$

where p_1 is close to $\omega_{z,sp}$. Equation (10) implies that increasing L_1 will linearly lower the zero frequency which is located between the two poles. This trend implies an increase in bandwidth.

The load capacitance C_N at the output node of this stage will contribute a high-frequency pole at $1/(R_2C_N)$. Finally, the input impedance seen from the PD is expressed as follows:

$$Z_{in} \approx \frac{1}{g_{m2}A} \times \frac{1 + \alpha_1 s + \alpha_2 s^2}{1 + \beta_1 s + \beta_2 s^2 + \beta_3 s^3} \tag{13}$$

Where

$$\alpha_1 = R_1(C_{\pi 2} + C_P), \alpha_2 = L_1(C_{\pi 2} + C_P), \beta_1 = \frac{C_{in}}{g_{m2}A} + \frac{C_{\pi 2}}{g_{m2}} + \frac{L_1}{R_1} + \frac{C_{\pi 2} + C_P}{g_{m2}g_{m1}R_{in}}$$
$$\beta_2 \cong \frac{(C_{\pi 2} + C_P)C_{in}}{g_{m1}g_{m2}} + \frac{L_1}{R_1}\left(\frac{C_{\pi 2}}{g_{m2}} + \frac{C_P}{g_{m1}}\right), \beta_3 = \frac{L_1(C_{in}(C_{\pi 2} + C_P) + C_{\pi 2}C_P)}{g_{m2}A} \tag{14}$$

2.3. Shunt-Peaked, Shunt-Series Feedback Stage Incorporating Transformer-Based Positive Feedback

To further increase the bandwidth and lower the input-referred noise (IRNoise), a transformer-based positive feedback path through the mutually coupled inductors L_P and L_S is introduced (cf. Figure 5). Using the equivalent circuit model in Figure 7 for a transformer, we build an equivalent circuit in Figure 8, where k is the coupling coefficient between the two inductors and $n = \sqrt{\frac{L_S}{L_P}}$. L_P introduces an inductive input reactance that further increases the bandwidth by resonating with C_{PD}. The effect of this transformer-based positive feedback network on the gain, input impedance, the circuit stability, and the IRNoise current will be illustrated in the following subsections.

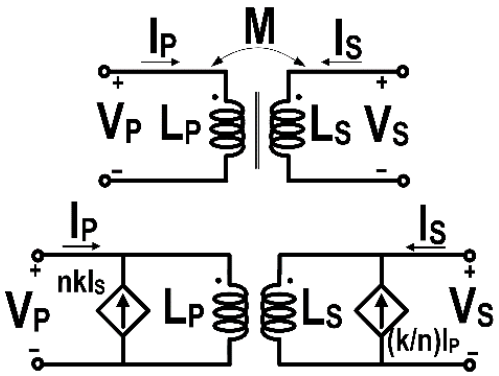

Figure 7 Transformer equivalent model

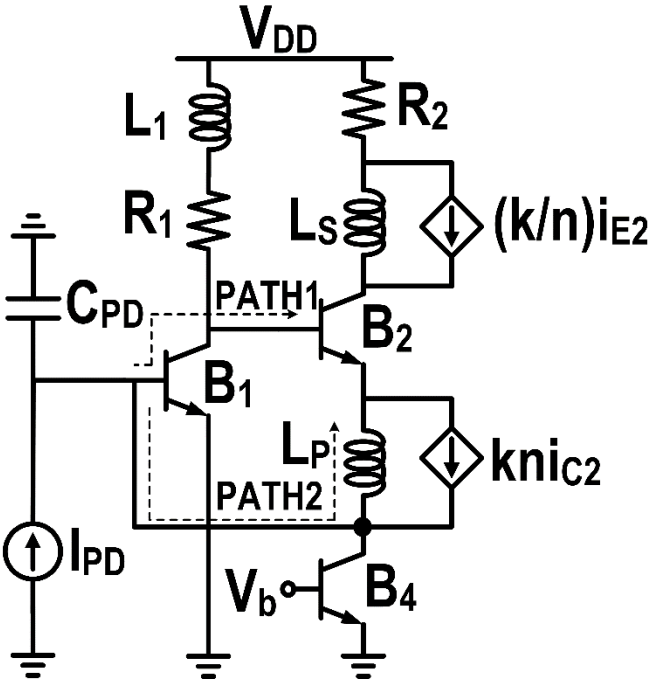

Figure 8 Small-signal model of the first amplification stage transformer-based positive feedback

2.3.1. Transimpedance Gain

Using the equivalent circuit of Figure 8, the normalized transimpedance gain of this shunt-peaked, shunt-series feedback amplifier is expressed by equation (15)

$$Z_T = \frac{g_{m2}R_2R_{in}(1+g_{m1}R_1)\left(1+\frac{L_1 g_{m1} s}{1+g_{m1}R_1}\right)}{(1+R_{in}C_{in}s)[1+R_1C_{\pi 2}s+(L_1+L_P)C_{\pi 2}s^2+L_P g_{m2}(1-nk)s]+R_{in}\left(1+g_{m1}(R_1+L_1 s)\right)(g_{m2}+C_{\pi 2}s)} \quad (15)$$

which is rewritten as:

$$Z_T \approx \frac{R_2\left(1+\frac{s}{\omega_{z,sp}}\right)}{1+b_1 s+b_2 s^2+b_3 s^3} \tag{16}$$

where

$$b_1 = a_1 + \frac{L_P(1-nk)}{AR_{in}}, b_2 = a_2 + \frac{C_{in}L_P(1-nk)}{A} + \frac{C_{\pi 2}(L_1+L_P)}{Ag_{m2}R_{in}}, b_3 = \frac{C_{in}C_{\pi 2}(L_1+L_P)}{Ag_{m2}} \tag{17}$$

Of interest is to study the effect of transformer's primary inductor on upper corner frequency and roll-off behavior of Z_T. Therefore, the third-order polynomial is simplified by evaluating its third-order term at the uncompensated input pole frequency of $\frac{Ag_{m2}}{AC_{\pi 2}+C_{in}}$, i.e.,

$$\tilde{Z}_T \approx \frac{R_2\left(1+\frac{s}{\omega_{z,sp}}\right)}{1+\tilde{b}_1 s+b_2 s^2} \tag{18}$$

where

$$\tilde{b}_1 = a_1 + \frac{L_P}{A}\left(\frac{1-nk}{R_{in}} - Ag_{m2}\frac{AC_{in}C_{\pi 2}}{(C_{in}+AC_{\pi 2})^2}\right) \tag{19}$$

Evaluating the damping ratio and corner frequency in (18), it is inferred that increasing L_P will reduce the corner frequency and damping ratio (note that the coefficient of L_P in $\tilde{b}_1$ is negative) at high frequencies. Being in series with the signal path, both L_P and L_S also act as series-peaking inductors, separating the parasitic capacitors between the input node and the emitter of B_2 and the output node and the collector of B_2, respectively. Figure 9 shows the simulated transimpedance frequency response for various values of identical coupled inductors, showing higher peaking for larger inductor values.

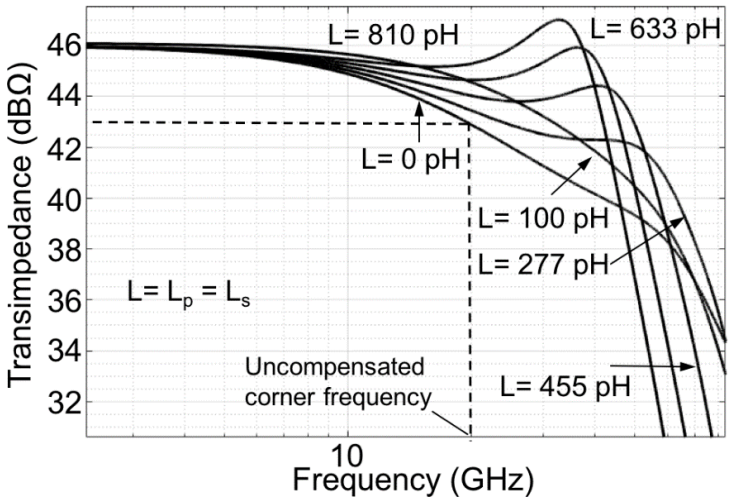

Figure 9 Dual-feedback transformer-based transimpedance stage gain vs. transformer inductances

The inductors L_P and L_S are designed based on co-optimization of this stage and subsequent stages for the purpose of achieving broadband flat frequency response with minimum in-band GDV. To find the optimum values of L_P and L_S and coupling factor *k* the same design approach explained in [28] is followed. In this design, L_P and L_S values are chosen to be 125 pH with a coupling coefficient of 0.6 and self-resonance frequency of >100 GHz. Figure 10 shows the effect of coupling factor *k* on the transimpedance frequency response.

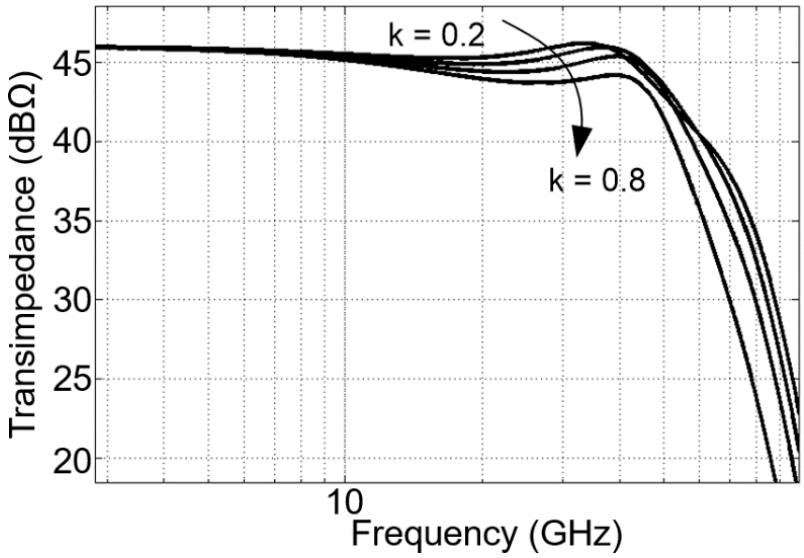

Figure 10 Simulated frequency response of the first stage of the dual-feedback transformer-based TIA vs. transformer coupling factor. Transformer inductor values are set at 500 pH for illustration purpose

A higher coupling factor will decrease the peaking at high frequencies, providing an additional degree of freedom for co-optimizing this stage with following stages for flat frequency response across the whole bandwidth. The layout of the transformer is shown in Figure 11. A single-turn stacked topology structure is implemented on the two topmost metal layers, providing a lower overall area, lower parasitic capacitance, higher self-resonance frequency and higher quality factor compared to a planar structure in this technology node.

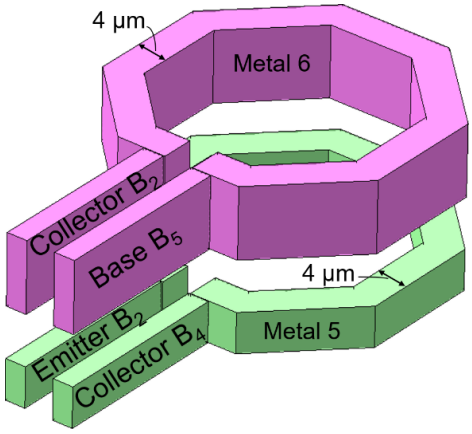

Figure 11 3D view of the monolithic transformer layout

Alternatively, one can identify two signal paths, PATH1 and PATH2, from the input to the output of this stage, as is indicated in Figure 8. The inductor L_P introduces a frequency-dependent phase shift to the signal traveling through PATH1. Intuitively, the bandwidth will be expanded if the gain at frequencies near the upper corner frequency of the frequency response is boosted. Choosing an appropriate L_P value to create 180º phase-shift between the signals at the base and emitter of B_2 at these high frequencies will increase the transconductance by 6 dB.

2.3.2. Input Impedance:

Following a procedure similar to that used for deriving the transimpedance gain, the impedance seen from the PD (i.e., Z_{in}) is $\frac{R_{in}}{1+R_{in}C_{in}} || Z_1$, where:

$$Z_1 = \frac{1 + (g_{m2}(1 - nk)L_P + R_1 C_{\pi 2})s + (L_P + L_1)C_{\pi 2}s^2}{(1 + g_{m1}R_1)\left(1 + \frac{g_{m1}L_1}{1 + g_{m1}R_1}s\right)(g_{m2} + C_{\pi 2}s)} \tag{20}$$

At midband frequencies where the second order terms can be neglected, Z_{in} is approximated as:

$$Z_{in} = \frac{L_P(1 - nk)s}{(1 + g_{m1}R_1)} + \frac{1}{g_{m2}(1 + g_{m1}R_1)} \tag{21}$$

From (21), it is seen that the effective resistance and inductance are scaled down by the factor $1 + g_{m1}R_1$. The scaling of the inductance allows us to accomplish two conflicting tasks at the same time. It allows us to resonate out the large PD capacitors and it also helps create peaking at the upper corner frequency of the circuit. Moreover, the effective inductance can be controlled by the transformer parameters, namely turn ratio n and coupling factor k.

2.3.3. Stability Analysis:

Within the shunt-series feedback loop, the mutually coupled inductors create a local positive feedback around the second common-emitter stage, resulting in a dual-feedback amplifier. The stability of this amplifier is studied in two steps. First, focusing on the positive feedback loop, Figure 12(a) shows an equivalent circuit for the second common-emitter stage to find the return-ratio (RR):

$$\mathrm{RR} = -\frac{i_R}{i_T} = -\frac{g_{m2} n k L_P s}{1 + \left(g_{m2} + \frac{1}{r_{\pi 2}}\right)\left(\frac{R_{in}}{1 + R_{in} C_{in}} + L_P s\right)} \tag{22}$$

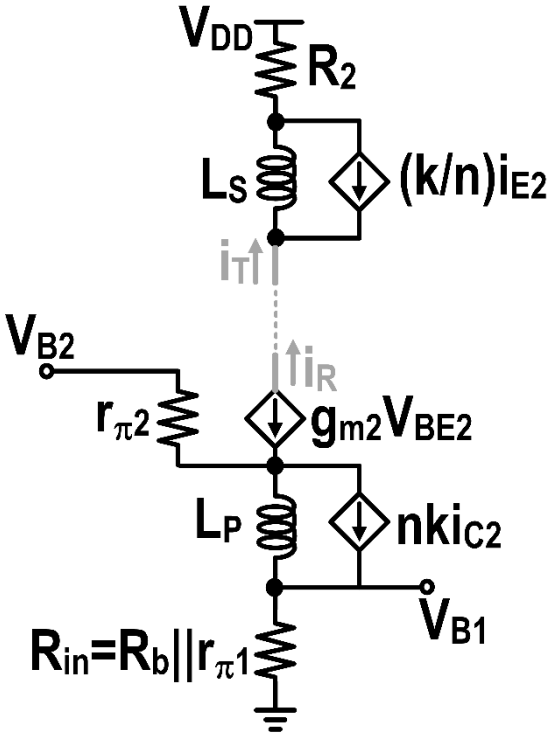

Figure 12 Positive feedback stability analysis schematic

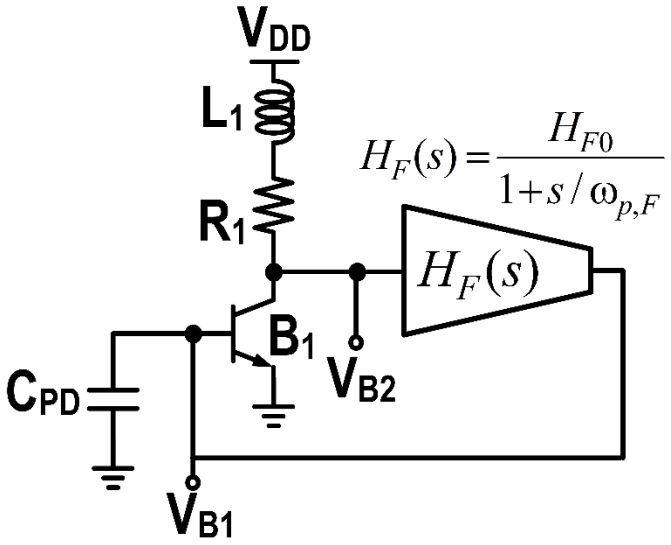

Figure 13 First stage stability analysis block diagram

To have an unconditionally stable positive feedback operation, |RR| < 1 at all frequencies [29]. Applying this condition on the complex rational function in (22) readily leads to nk < 1. In this work, a turn ratio of unity and a coupling coefficient of 0.6 have been adopted for the transformer.

Second, with nk < 1, the local positive feedback stage is unconditionally stable, and thus can be modeled by a first-order transfer function $H_F(s)$ within the shunt-series feedback network. Figure 12(b) shows the system block diagram which is used to analyze the stability of the shunt-series feedback network. Ignoring $C_{\pi 2}$ and the early effect of B_2, the loop-gain of this system, H_{loop}, is expressed as:

$$\mathrm{H_{loop}(s) = -g_{m1}(R_1 + L_1 s) \times H_F(s)} \tag{23}$$

which exhibits a dominant pole at:

$$\omega_{\mathrm{p,F}} = \frac{\mathrm{R_{in}C_{in} + g_{m2}L_P(1 - nk)}}{\mathrm{g_{m2}L_P(1 - nk)R_{in}C_{in}}} \tag{24}$$

Simulations were conducted to take the higher order terms into account, and a phase margin of 72° for the system was obtained.

2.3.4. Noise Analysis:

The noise performance of the shunt-peaked, shunt-series feedback stage of Figure 5 is presented in the appendix, in more details. The IRNoise current spectral density is derived as follows:

$$\overline{i_{n,eq}^2} \approx \overline{i_{n,B4}^2} + \overline{i_{n,B2}^2}\left[\left(\frac{1 - C_{\pi 2}(L_P + R_1 R_{in} C_{in})\omega^2}{g_{m2} R_{in}(1 + g_{m1} R_1)}\right)^2 + \left(\frac{C_{in}(1 - L_P C_{\pi 2}\omega^2)}{g_{m2}(1 + g_{m1} R_1)}\right)^2 \omega^2\right]$$
$$+ \overline{i_{n,B1}^2}\frac{1 + R_{in}^2 C_{in}^2 \omega^2}{g_{m1}^2 R_{in}^2} \qquad (25)$$
$$+ \overline{i_{n,R2}^2}\left[\left(1 - \frac{L_P(1 - nk)C_{in}\omega^2}{1 + g_{m1} R_1}\right)^2 + \left(\frac{C_{in}(1 - L_P C_{\pi 2}\omega^2)}{g_{m2}(1 + g_{m1} R_1)}\right)^2 \omega^2\right]$$

The shot noise of B_1 is divided by $(g_{m1}R_{in})^2$ and its contribution increases as frequency rises. Referring the noise power spectral density (PSD) of R_2 to the input, and low-pass response is observed. Moreover, its low frequency contribution on the $\overline{i_{n,eq}^2}$ is reduced as we increase the transformer primary inductor L_P. Intuitively, as the primary inductor increases, a smaller fraction of these noise PSDs will appear at the input. This reduction, however, is not significant since the inductor value is effectively reduced by a factor of $1 + g_{m1}R_1$. Figure 14 shows the simulated IRNoise current with respect to L_P, integrated over 4 different values of bandwidths.

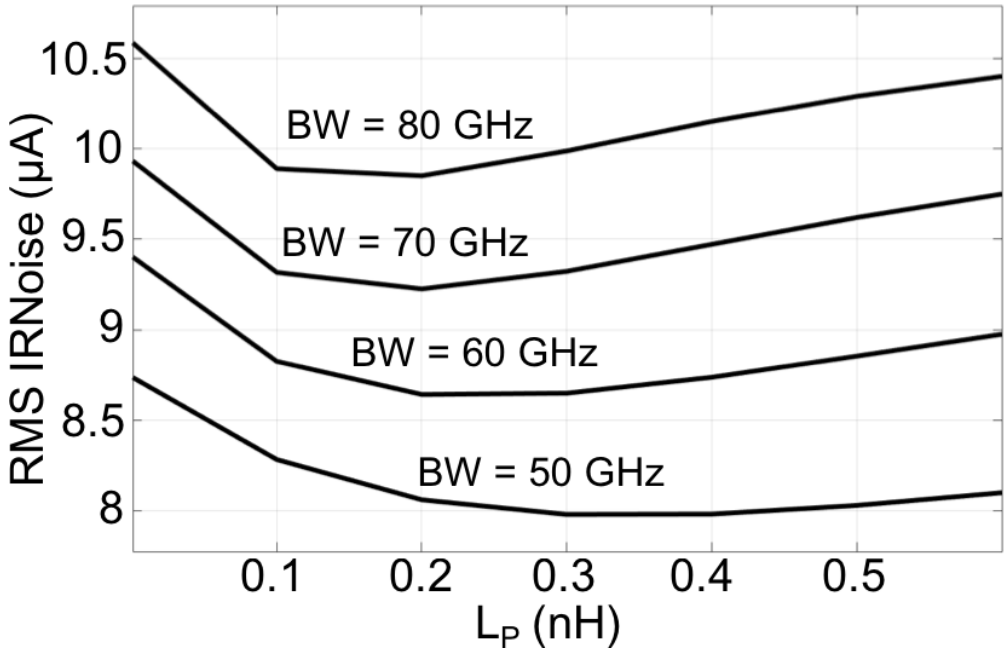

Figure 14 Simulated rms IRNoise current noise, integrated over multiple bandwidths vs. transformer's primary inductor

A consistent reduction in IRNoise current is observed for all values of bandwidth when the 125-pH primary inductor is employed compared to smaller L_P values. Moreover, as L_P continues to increase, the integrated high frequency noise will become significant and noise performance will deteriorate. The effect of transformer coupling ratio k is negligible, as it mainly affects the noise contributed by R_2. Increasing R_{in} and/or decreasing C_{in} will lower the shot noise current contribution of B_2, a behavior similar to that of a cascode transistor. Noise of the bias transistor B_4 directly appears at the input. While the use of shunt-series feedback results in an IRNoise similar to that of common-base structure, it can provide a much lower input impedance. The thermal noise of R_1 and the shot noise of B_1 exhibit similar contributions to the IRNoise current. Simulations show that both the output and IRNoise change negligibly when varying L_1.

2.4. Level-Shifter and RC-Degenerated Stage

The output of dual-feedback stage in Figure 5 is applied to the input of the circuit in Figure 15, where it is buffered and level-shifted using an emitter follower B_5 and then applied to a capacitive-peaking gain stage.

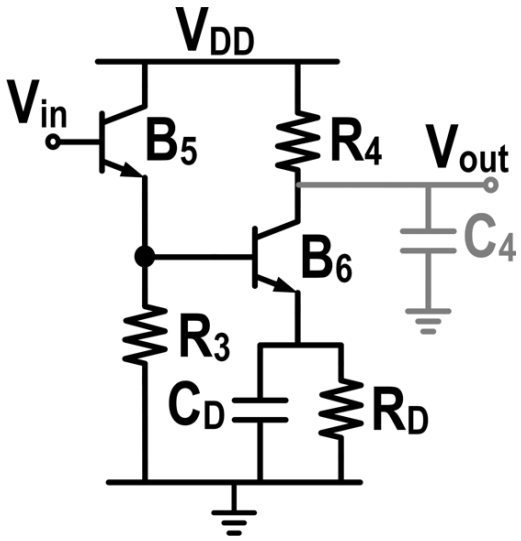

Figure 15 Capacitive-peaking gain stage for gain-bandwidth enhancement

Neglecting the Early effect in transistor B_6, the frequency response of the degenerated common-emitter stage is derived to be:

$$A_{ED} = A_{ED,DC} \times \frac{1 + \frac{s}{\omega_{z,ED}}}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{26}$$

where

$$A_{ED,DC} = \frac{-g_{m6}R_4}{1 + g_{m6}R_D + \frac{R_D}{r_{\pi 6}}} \cong \frac{-g_{m6}R_4}{1 + g_{m6}R_D}, \omega_{p1} = \frac{1}{R_4 C_4},$$
$$\omega_{p2} = \frac{1 + g_{m6}R_D + \frac{R_D}{r_{\pi 6}}}{R_D C_D} \approx \frac{1 + g_{m6}R_D}{R_D C_D}, \omega_{z,ED} = \frac{1}{R_D C_D} \tag{27}$$

This stage provides signal gain of $A_{ED,DC}$, introduces a zero $\omega_{z,ED}$ and two high frequency poles ω_{p1} and ω_{p2}. Bandwidth enhancement is achieved by placing the zero at the previous stage's upper corner frequency.

2.5. Inductively Degenerated Emitter-Follower Stage:

The poles generated by the RC-degenerated common-emitter stage, although located at high frequencies, still limit the bandwidth at about 25 GHz. In order to further increase the bandwidth, a modified emitter follower stage, depicted in Figure 16(a), is placed right after the RC-degenerated stage and before the output buffer.

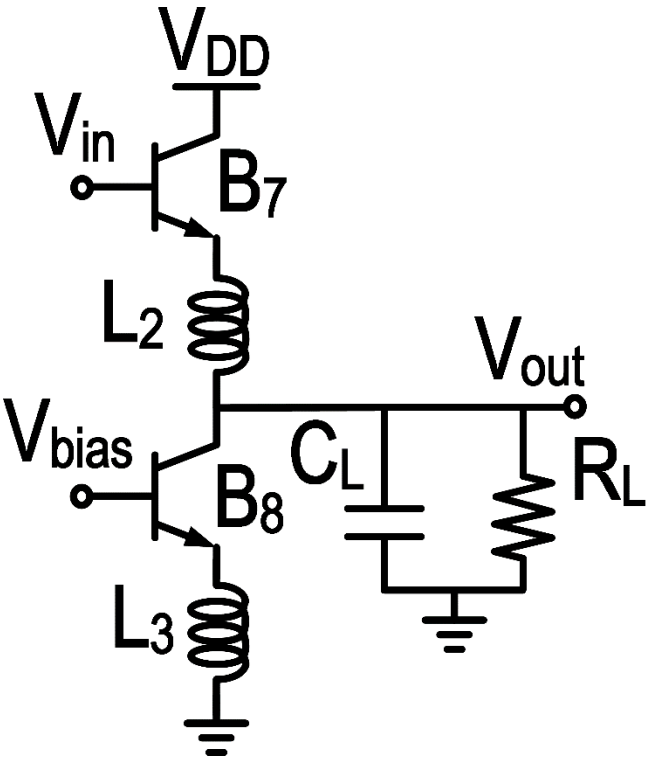

Figure 16 Modified emitter follower stage

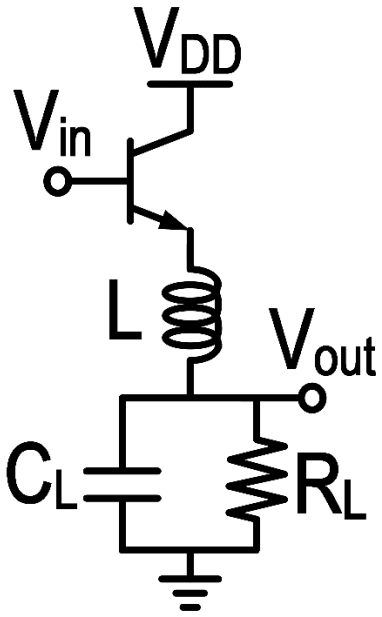

Figure 17 Emitter follower with only the series-peaking inductor L

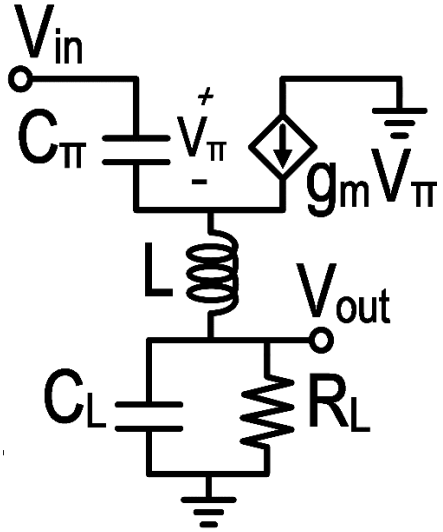

Figure 18 Small signal model of Figure 17

To analyze this stage and gain insight about its attributes, consider the schematic and equivalent model of an emitter follower which employs series-peaking in order to enhance the bandwidth (cf. Figure 16(b) and (c)). The voltage gain transfer function of this circuit is derived as:

$$A_V = A_{DC} \times \frac{1 + \frac{s}{\omega_T}}{1 + \gamma_1 s + \gamma_2 s^2 + \gamma_3 s^3} \tag{28}$$

where

$$\omega_T = \frac{g_m}{C_\pi}, A_{DC} = \frac{g_m R_L}{1 + g_m R_L}, \gamma_1 = \frac{R_L C_L + R_L C_\pi + g_m L}{1 + g_m R_L},$$
$$\gamma_2 = \frac{L(g_m R_L C_L + C_\pi)}{1 + g_m R_L}, \gamma_3 = \frac{L R_L C_L C_\pi}{1 + g_m R_L} \quad (29)$$

Using a similar approach as in [30], (28) is rewritten as:

$$A_V = \frac{1 + r\frac{s}{\omega_0}}{1 + \frac{1}{A_0} + \left(1 + \frac{1}{mA_0}\right)\frac{s}{\omega_0} + \frac{1 - r + \frac{r}{A_0}}{m}\frac{s^2}{\omega_0^2} + \frac{r(1-r)}{m}\frac{s^3}{\omega_0^3}}$$
$$\cong \frac{1 + r\frac{s}{\omega_0}}{1 + \frac{s}{\omega_0} + \frac{1 - r}{m}\frac{s^2}{\omega_0^2} + \frac{r(1-r)}{m}\frac{s^3}{\omega_0^3}} \quad (30)$$

where $r = \frac{C_\pi}{C}$, $C = C_\pi + C_L$, $\omega_0 = \frac{g_m}{C}$, $A_0 = g_m R_L$ and $m = \frac{C}{L g_m^2}$. The inductor L introduces a pair of complex conjugate poles in the frequency response, enhancing the bandwidth. Figure 19 shows the simulated magnitude of the voltage gain for several values of r and m.

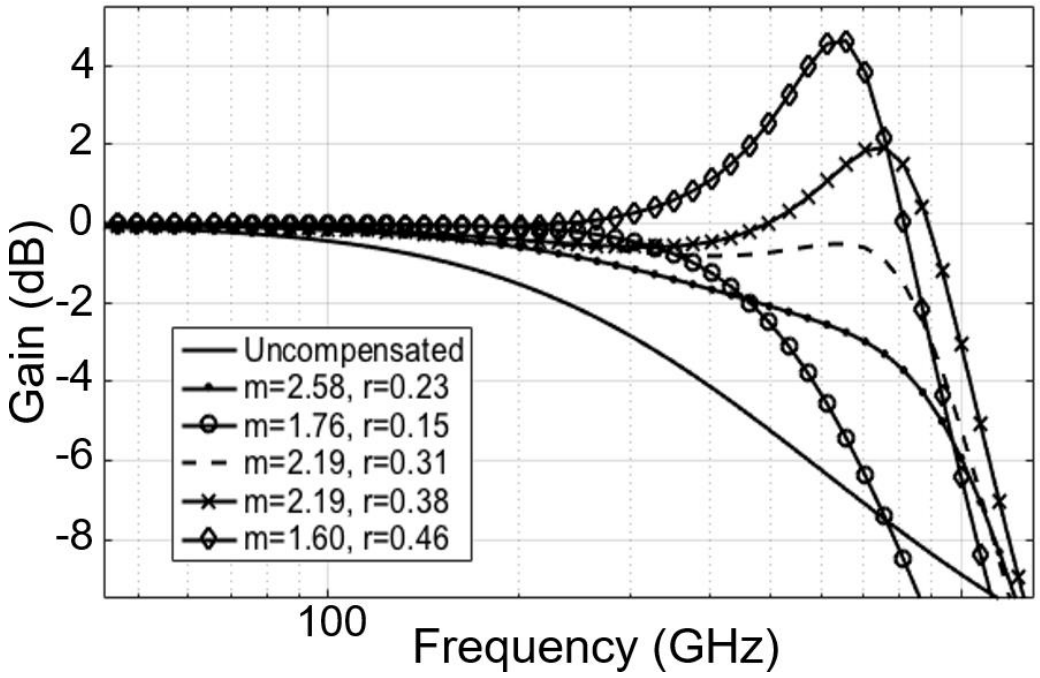

Figure 19 Bandwidth enhancement in the frequency response of the inductor degenerated emitter follower of Figure 16 normalized to the uncompensated corner frequency *[31]*

The solid line represents the uncompensated case (no inductor). Note that this stage is considered in isolation and the displayed bandwidth is not achieved in practice. In general, C_L is primarily determined by the next block in the receiver chain (e.g., clock-data recovery block). A BWER of 2.86 is achieved for m = 2.19 and r = 0.31 while keeping the peaking in the frequency response less than 0.9 dB.

In order to increase the BWER even further while introducing another degree of freedom to control the peaking in the high-frequency response, the current source is degenerated by an inductor, L_3, in its emitter. The output impedance seen from the collector of B_8 is:

$$Z_{o8} = r_{o8} + (1 + g_{m8} r_{o8}) L_3 s \tag{31}$$

where r_{o8} and g_{m8} are the output resistance and transconductance of B_8, respectively. This output impedance will show inductive behavior below the resonance frequency created by L_3 and the base-emitter capacitance of the B_8, $C_{\pi 8}$, which can be approximated as $f \approx \frac{1}{2\pi\sqrt{L_3 C_{\pi 8}}}$ [32].

This resonance frequency is greater than 86 GHz for the current design. The voltage gain of this stage (including the loading introduced by the output buffer) is derived as:

$$A_V = \frac{1 + \tau_1 s + \tau_2 s^2}{1 + \eta_1 s + \eta_2 s^2 + \eta_3 s^3 + \eta_4 s^4} \tag{32}$$

where

$$\tau_1 = \frac{1}{m_2 \omega_{o2}} + \frac{r}{\omega_{o1}}, \tau_2 = \frac{r}{m_2 \omega_{o1} \omega_{o2}}, \eta_1 = \frac{1}{m_2 \omega_{o2}} + \frac{1}{\omega_{o1}} + \frac{1}{A_0 m_1 \omega_{o1}},$$

$$\eta_2 = \frac{1 + r}{m_2 \omega_{o1} \omega_{o2}} + \frac{1 - r}{m_1 \omega_{o1}^2} + \frac{1}{A_0 m_1 \omega_{o1} m_2 \omega_{o2}}, \tag{33}$$

$$\eta_3 = \frac{1 - r}{m_1 \omega_{o1}^2 m_2 \omega_{o2}} + \frac{r(1 - r)}{m_1 \omega_{o1}^3}, \eta_4 = \frac{r(1 - r)}{m_1 m_2 \omega_{o1}^3 \omega_{o2}}$$

where $m_2 = \frac{C}{L_3 g_{m8}^2}$, $\omega_{o2} = \frac{g_{m8}}{C}$ and C, A_0, m_1 and ω_{o1} are defined as before. The frequency response of this stage is shown in Figure 20 for several values of r, m_1 and m_2.

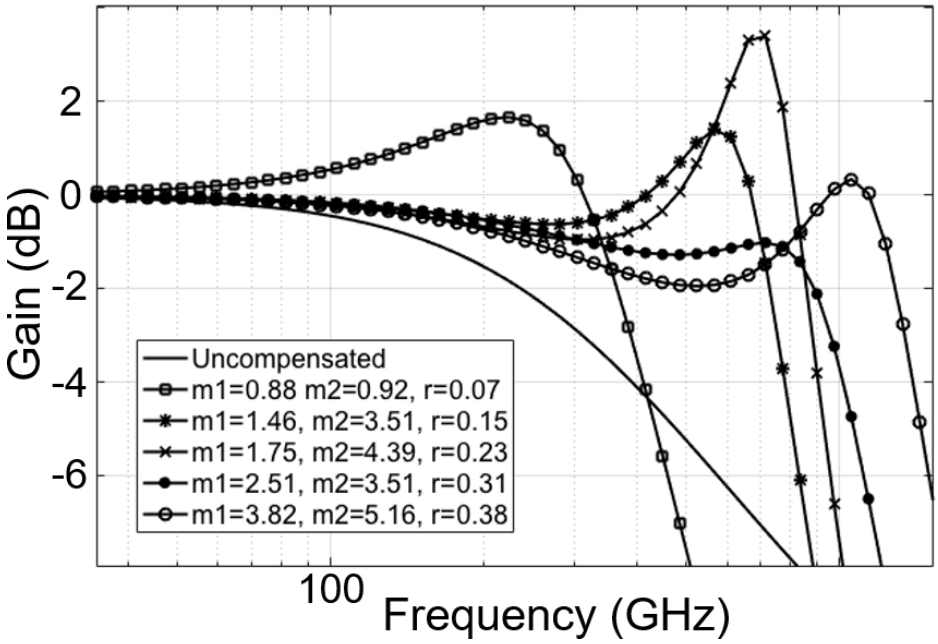

Figure 20 Bandwidth enhancement in the frequency response of the inductor degenerated emitter-follower of Figure 16 normalized to the uncompensated corner frequency *[31]*

Simulation shows that a BWER of greater than 3.1 is achieved with less than 1.1 dB peaking in the frequency response. The actual values used for the inductors are higher (L_2 = L_3 = 125 pH), considering that the inductor non-idealities, routing parasitic and loading from prior stage will affect the response.

Simulation Results

Figure 21 shows the complete schematic of the TIA. Based on post-layout and Sonnet EM simulations, the TIA shows a transimpedance gain of 42 dBΩ over a bandwidth greater than 50 GHz. The minimum detectable output swing and transimpedance gain are determined by the decision circuit block following the TIA, the input sensitivity of the TIA, and the maximum power penalty budget [21].

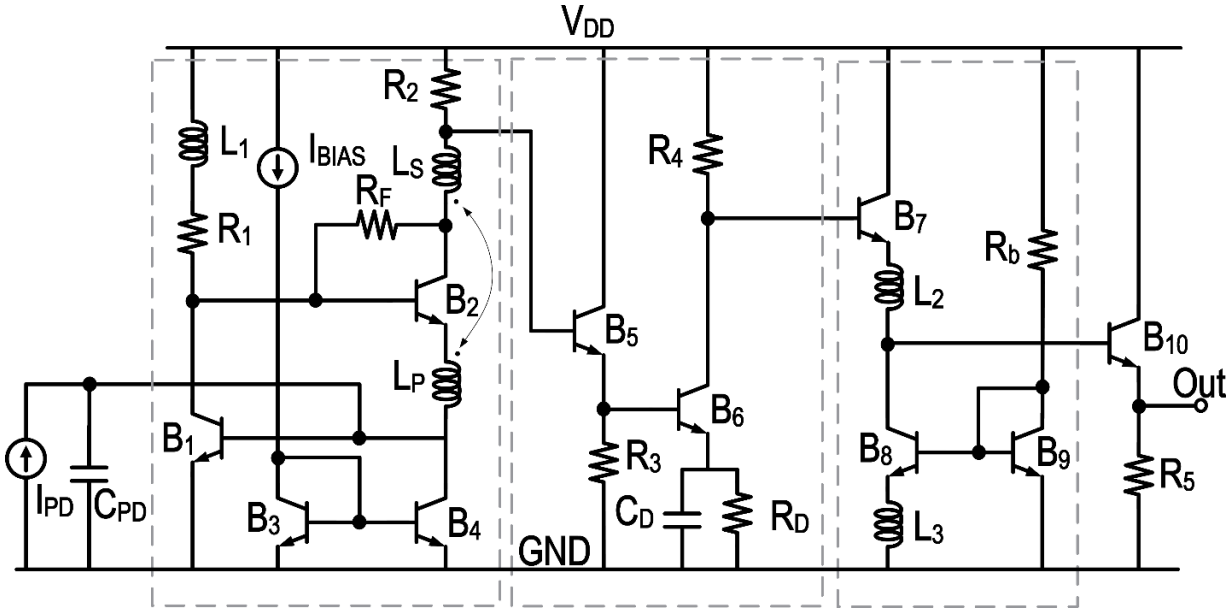

Figure 21 Circuit schematic of the proposed TIA *[33]*

It is shown that for a maximum decision threshold offset of 5 mV and a maximum power penalty of 1 dB, the peak-to-peak output swing should be greater than 20 mV [33]. Link budget calculations predict a dynamic range between 200 µA and 1 mA for the PD current [33]. For a

350-µA 50-Gb/s random bit sequence, the TIA shows an open eye with an RMS jitter of 880 fs. Considering that the timing jitter needs to be about 10% of the unit interval to have a low bit-error rate set forth by the required sensitivity of the receiver side, the TIA shows satisfactory jitter performance. Local feedback resistor R_F is chosen to be sufficiently large (850 Ω for this circuit) so that it helps extend the bandwidth of the first stage with negligible drop in gain [34].The output emitter-follower stage is added for measurement purpose only. Figure 22 shows the group-delay for various stages of the TIA. The overall response shows a GDV of 12 ps across the entire bandwidth.

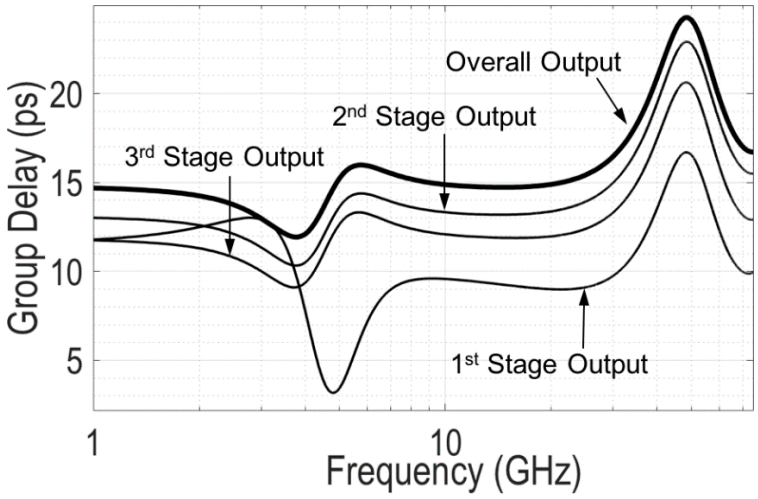

Figure 22 Simulated group-delay for different stages of the TIA *[31]*

The transmission line connecting the input of the circuit to the bondpad adds a small inductance in series with the signal path, forming a π network which causes the input noise current to drop [19]. This effect is shown in Figure 23 which demonstrates the behavior of IRNoise PSD with and without the input transmission line. Tradeoff exists between group delay variation, the amount of BW enhancement, high frequency noise suppression and insertion loss of the transmission line. The effect of this transmission line on the performance parameters

(namely frequency peaking and input impedance) are captured during the design optimization in conjunction with its high frequency noise suppression effect and insertion loss.

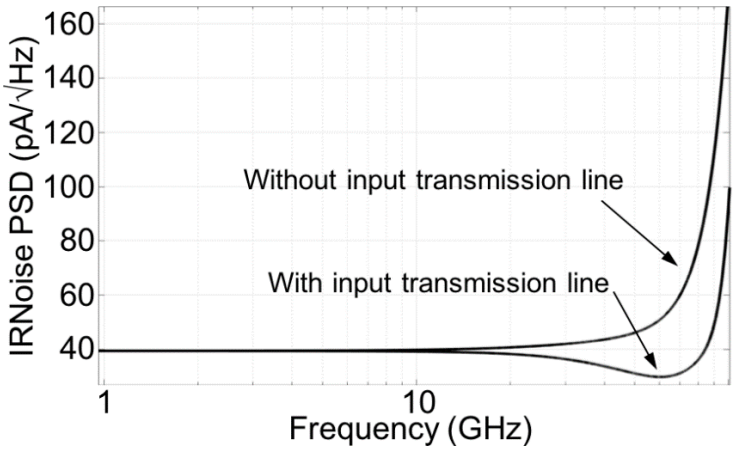

Figure 23 Simulated IRNoise current PSD of the TIA *[31]*

Figure 24 shows the eye diagram for the post-layout simulated circuit (including the EM models for inductors and signal paths) for 300-μA input current amplitude. The vertical eye opening (as well as the transimpedance gain) is reduced by the source-follower output buffer.

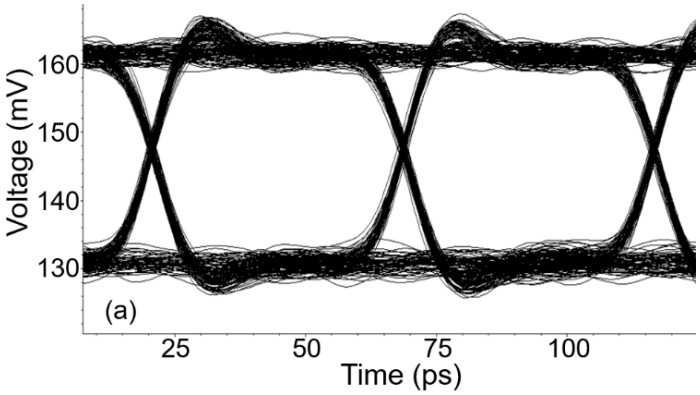

Figure 24 Simulated Eye Diagram for random input bit sequence at 21 Gb/s *[31]*

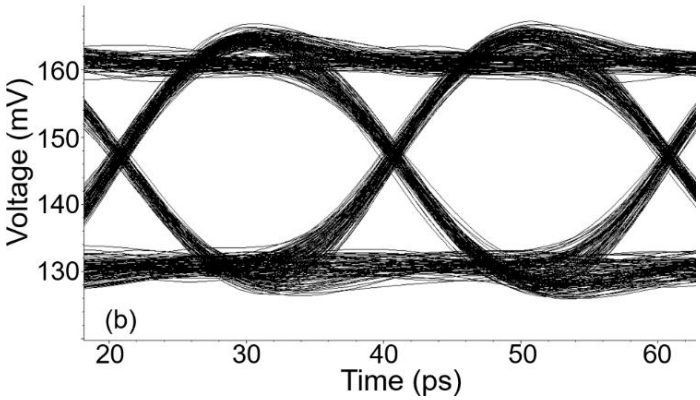

Figure 25 Simulated Eye Diagram for random input bit sequence at 50 Gb/s *[31]*

Measurement Results

The TIA was fabricated in a 0.13 µm SiGe BiCMOS process. Figure 26 shows the die micrograph of the chip, occupying 187×210 μm^2 core area and 1×0.575 mm^2 overall area (including pads). Minimum pad size and distance between the RF probes have been adopted to reduce the parasitic effects on the performance. An on-chip 100 fF MIM cap is integrated at the input of the TIA to emulate the PD parasitic capacitance. This capacitor shunts the input current created by the photodiode, creating a pole at the input node and limits the bandwidth. Although the small size of the input capacitor imposes a stringent requirement on the electrical-optical interface, it has been shown that PDs having high-performance and low junction capacitors are realizable [35].

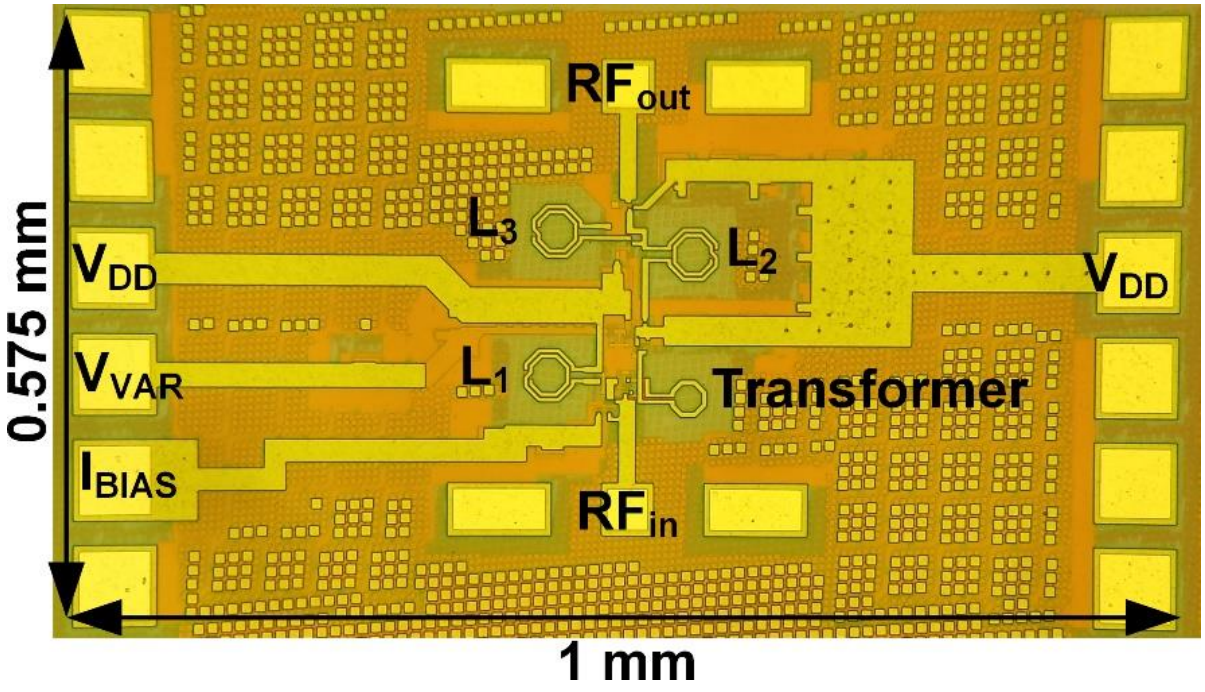

Figure 26 Die micrograph of the TIA on 0.13µm BiCMOS Process *[1]*

The transimpedance gain was measured via probing (Cascade Microtech I67-GSG-100 probe) using an Agilent E4448A spectrum analyzer and E8257D signal generator. No attenuator was needed since the signal generator power was tuned to fall within the TIA dynamic range. Since the magnitude of the TIA's input impedance is much less than 50 Ω, we can consider the signal generator to behave almost like a current source with a value of V_S/(50 Ω) A. Figure 27 shows both simulated and measured S_{11} and S_{22} of the TIA. Figure 27(a) indicates measured and simulated polar variation of S_{11} and S_{22} on Smith chart, whereas Figure 27(b) demonstrates magnitude responses of these return losses versus frequency. Referring to Figure 27(a)-(b), great agreement is observed between simulation and measurement. The measurement has been performed over two sets of frequency bands, 10 - 20 GHz and 20 - 40 GHz, due to calibration limitation of the measurement setup which created a jump in the measured S_{22} plot in Figure 27(b) when the results were merged. The transimpedance gain of the TIA is evaluated by measuring the TIA output power while accounting for the input reflection coefficient. The

measured and simulated transimpedance gain vs. frequency are shown in Figure 28, showing great agreement between the two. The cables, connectors and probes frequency responses were measured and calibrated out to account for their loss in the measurements.

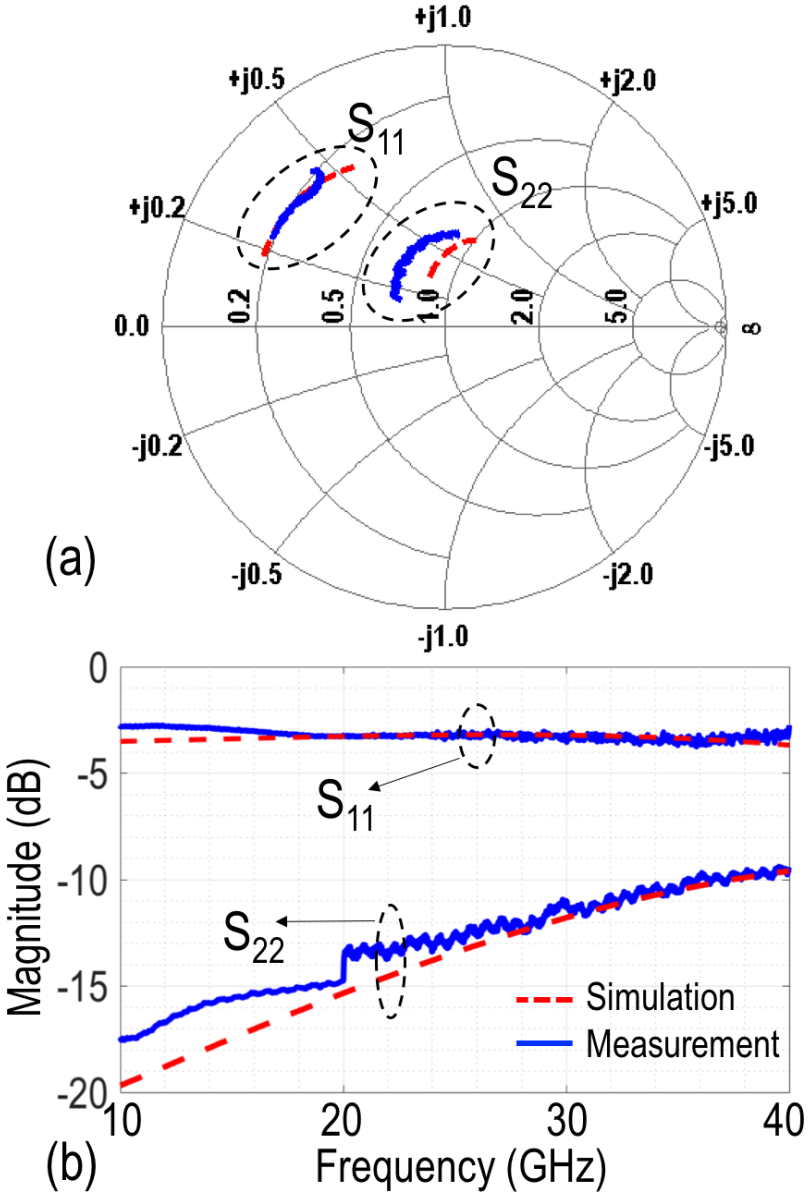

Figure 27 Measured and simulated S-parameters over the frequency range of interest *[31]*

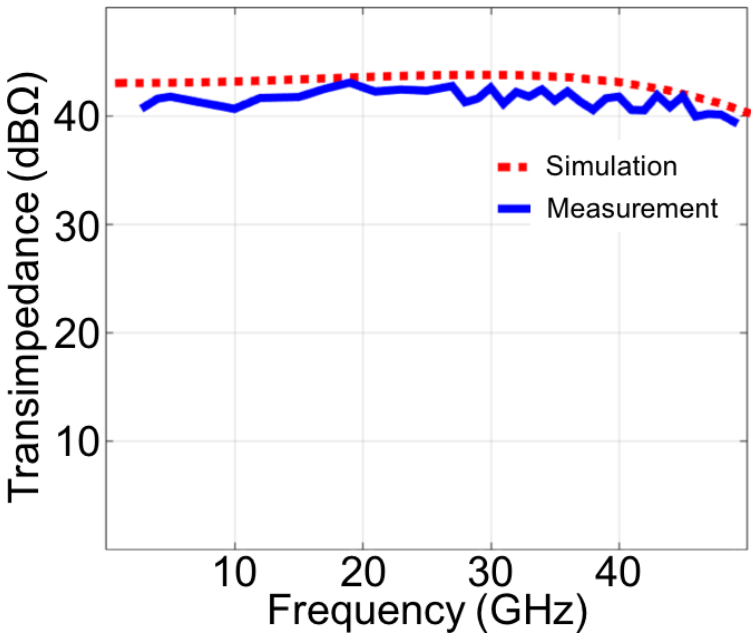

Figure 28 Transimpedance frequency response of the proposed TIA *[1]*

The input port impedance matching is not necessary in TIA designs since the source impedance is effectively the PD capacitance, a high impedance node. The TIA input should present a low impedance to the PD to allow its entire current to enter the TIA. However, for measurement purposes, i.e., to reduce the reflections stress on the eye diagram generated by a 50 Ω source, it is desirable to match the input to 50 Ω. Simulated input impedance is less than 11 Ω up to 22 GHz. Therefore, it is expected that the 50 Ω source contributes negligible artificial bandwidth enhancement at the input. The TIA achieves 41 dBΩ of transimpedance over a 50 GHz bandwidth. The measurement frequency span was limited by the spectrum analyzer.

Figure 29 shows that the integrated output noise voltage of the TIA, measured using the histogram function of Lecroy 100H sampling oscilloscope, is 1.76 mV rms. This quantity includes a 1.45 mV rms noise due to the oscilloscope. This corresponds to IRNoise spectral density of 39.8 pA/√Hz over a 50 GHz bandwidth. For an NRZ modulation, the BER is estimated as:

$$\mathrm{BER} = \mathrm{Q}\left(\frac{i_{s,pp}}{2i_{n,rms}}\right), \mathrm{Q}(x) = \int_{x}^{\infty} \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{y^2}{2}\right) dy \quad (34)$$

where $i_{s,pp}$ and $i_{n,rms}$ are the peak-to-peak current signal amplitude and the input-referred rms noise current. For a target 10^{-12} BER and measured integrated rms noise current of 9 µA, the TIA sensitivity of 120 µA is obtained.

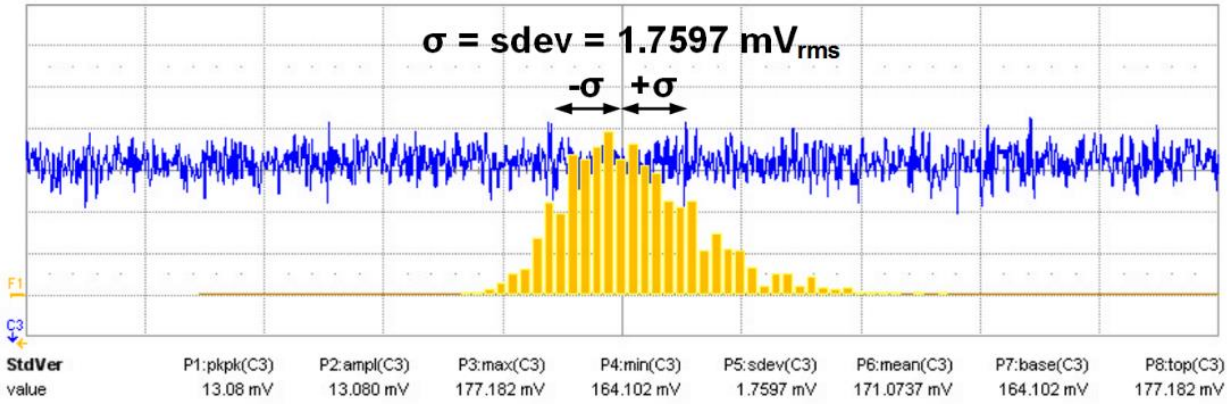

Figure 29 Amplifier integrated output noise *[1]*

Figure 30 depicts the setup for the eye diagram measurement of the amplifier. An Agilent N4975A pseudo-random bit-sequence (PRBS) generator was used to apply the 2^{15}-1-bit pattern. A Keysight digital communication analyzer (DCA) 86100D with 86118A sampling head were used to measure the eye diagram. The PRBS data output was attenuated to fall within the dynamic range of the TIA. Both trigger and precision time-based inputs of the DCA were used for accurate synchronization of clock and data. The measured eye diagram is shown in Figure 31.

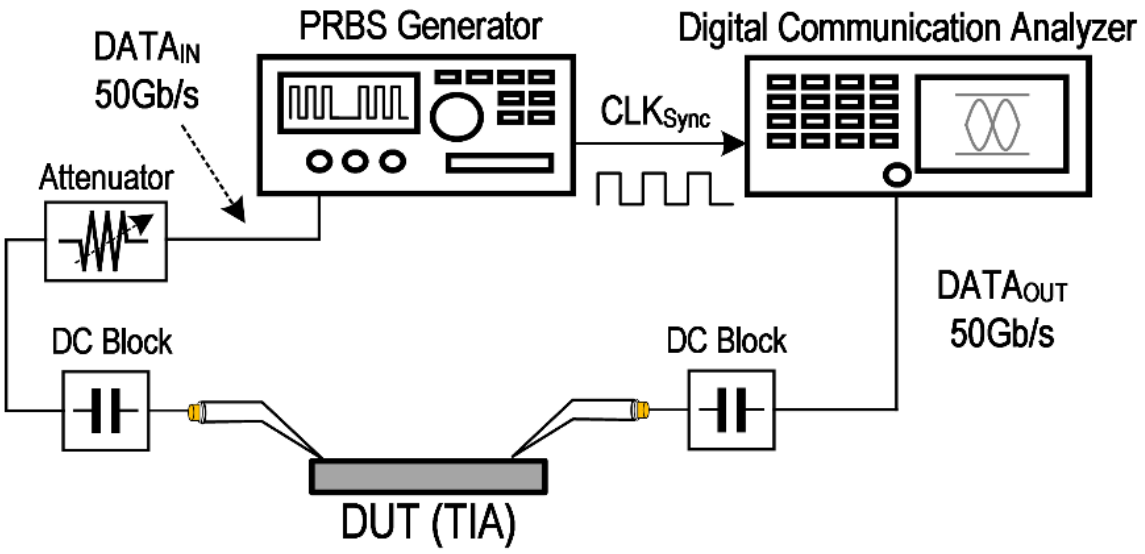

Figure 30 Eye diagram measurement setup *[31]*

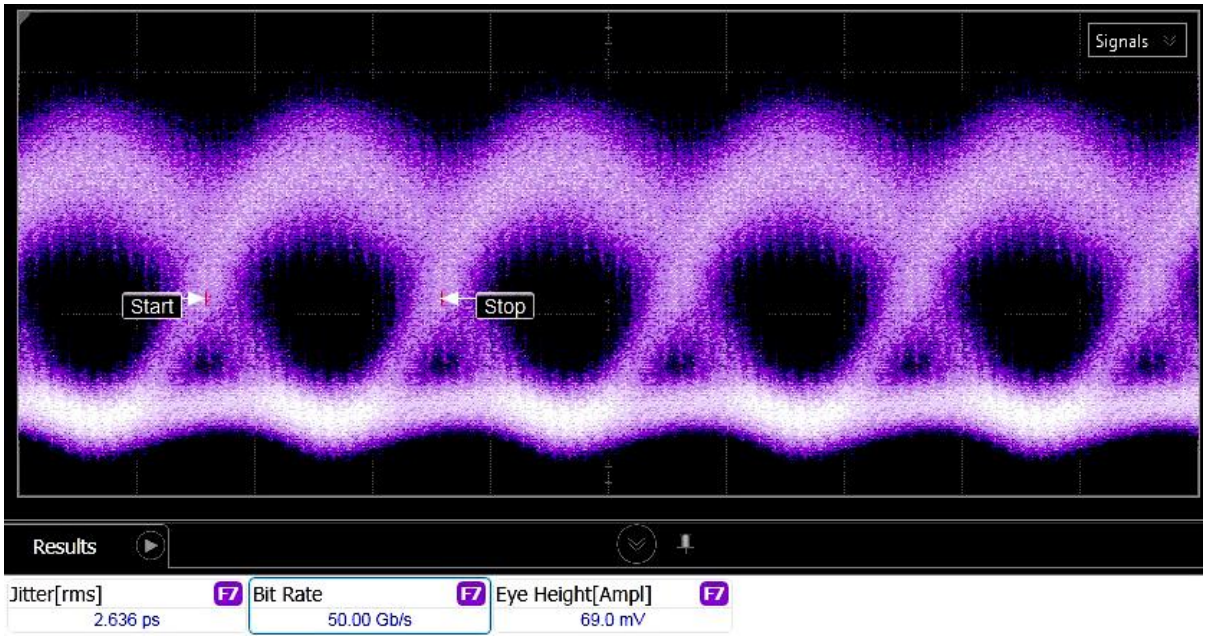

Figure 31 Measured eye diagram from a PRBS generator with 2^{15}-1 pattern and 350 µA input amplitude *[1]*

The test fixture contributed 1.1 ps rms jitter, resulting in an overall 2.34 ps rms jitter in the eye diagram. The measured eye appears to be more blurred around its high logic level. The main reasons for this phenomenon are attributed to the imperfect input/output matching and

process variation effects. In fact, simulations verify that the shape of the eye and high- and low-level voltages become asymmetric at the process corners.

The TIA performance summary is presented in Table 1. The TIA in this work shows a figure-of-merit (defined as FoM=BW×Gain/P_{DC}) of 233.7 Ω/pJ. This FoM has been calculated based on 50 GHz bandwidth which can be reported with the spectrum analyzer with limited bandwidth.

This TIA provides a low-power, broadband amplification solution for high speed optical link front-ends with data rates exceeding 50 Gb/s.

Table 1 Performance summary and comparison with prior art

	JSSC [18]	TCAS I [36]	JSSC [37]	TCAS I [19]	This work [31]
Measured Bit-rate (Gb/s)	27	40	40	N/A	50
f_{-3dB} (GHz)	28	29	30.5	8	50[4]
Gain (dBΩ)	53.6	50	51	53	41
Power (mW)	110	45.7	60.1	13.5	24
Noise (pA/√Hz)	36.5	51.8	55.7	18	39.8
Supply	2.5	1.5	1.8	1.8	2
C_{PD} (fF)	150	50[3]	50	250	100
GDV (ps)	13	16	45[1]	40	12
Area (mm^2)	0.75	0.4	0.54	0.36	0.58
FoM[2] (Ω/pJ)	121.8	200.7	180.1	264.7	233.7[4]
Technology	0.25 µm BiCMOS	0.13 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.13 µm BiCMOS
Process f_T (GHz)	137	85	~60	N/A	240

[1]Value reported up to 22GHz. GDV is 130ps across the whole bandwidth.
[2]BW×Z_T/P_{DC}. [3] Not included in the measurement, simulation only.
[4] Measured value limited by the spectrum analyzer bandwidth.

Conclusion

In this thesis, a brief overview of high-speed optical links was shown and a novel transimpedance amplifier with a staggered frequency response across three amplification stages was introduced. Performance specifications of broadband transimpedance amplifiers were discussed and a systematic link budget were derived to specify the design targets. Each stage in the proposed TIA was analyzed in detail and was further verified through simulations.

The design utilized a transformer-based shunt-series input stage to enhance the bandwidth, while providing additional degrees of freedom to control the jitter peaking in the frequency response. The middle stage provides additional gain plus a zero-pole cancellation using a capacitive-peaking technique. In the last stage emitter-follower, inductive series-peaking was used to increase the bandwidth. At the same time, the inductively-degenerated bias current provides another means to control the peaking in the overall frequency response. All the stages were designed as one entity to consider all non-ideal effects and optimize the performance. The TIA prototype was implemented in TowerJazz 0.13 μm BiCMOS process and was measured across 50 GHz of bandwidth. The chip showed open-eye diagram with minimal peaking in the frequency response. This TIA compares favorably with prior works, showing superior data rate.

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APPENDIX: Derivation of the input-referred noise for the first amplification stage

The equivalent model of the first stage alongside the noise sources for the dual-feedback transformer-based TIA is shown in Figure 32. For simplicity of the analysis, we assume IRNoise voltage is negligible compared to the IRNoise current and ignore the Early effect. The noise current of B_4 is parallel with the input current source. Noise transimpedance transfer functions for B_1 and B_2 are shown in (36) and (37) at the bottom of the page, respectively. Output noise due to R_2 is given by:

$$V_{n,R2} = \overline{i_{n,R2}} \frac{R_2}{1 + R_2 C_L} \tag{35}$$

Finally, the output noise due to the equivalent IRNoise current is given by (38). Inductor L_1 is not included in these equations as it unnecessarily complicates the equations (replacing R_1 with $R_1 + L_1 s$ gives the full transfer function). By equating the sum of (36), (37), noise current of B_4 and (35) with (38), the IRNoise spectral density in (25) is derived.

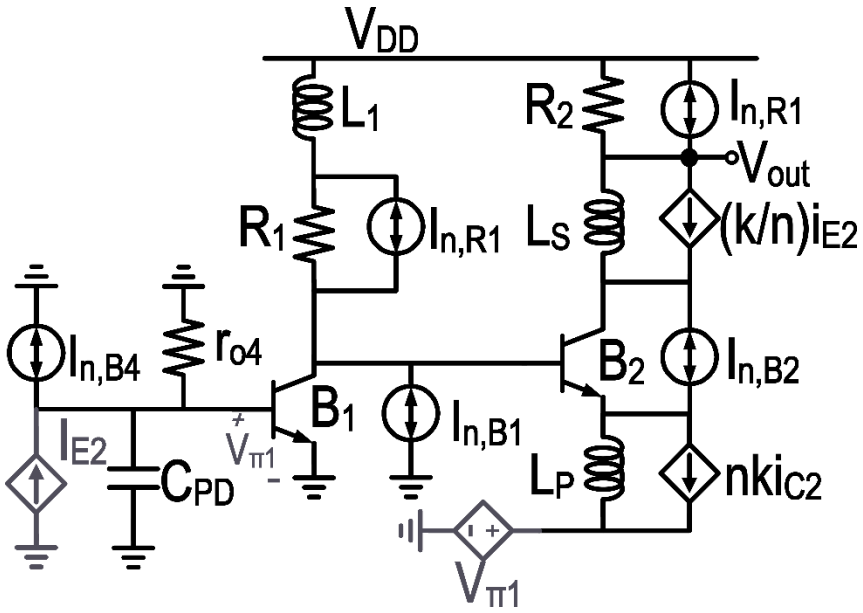

Figure 32 First stage of amplification equivalent noise model

$$V_{n,B1} = \frac{R_2\overline{i_{n,B1}}}{1+R_2C_L s} \times \frac{g_{m2}R_1(1+R_{in}C_{in}s)}{(1+R_{in}C_{in}s)[1+R_1C_{\pi 2}s+L_P s(g_{m2}(1-nk)+C_{\pi 2}s)]+R_{in}(1+g_{m1}R_1)(g_{m2}+C_{\pi 2}s)} \quad (36)$$

$$V_{n,B2} = \frac{R_2\overline{i_{n,B2}}}{1+R_2C_L s} \times \frac{R_{in}(1+g_{m1}R_1C_{\pi 2}s)+(1+R_1C_{\pi 2}s+L_PC_{\pi 2}s^2)(1+R_{in}C_{in}s)}{(1+R_{in}C_{in}s)[1+R_1C_{\pi 2}s+L_P s(g_{m2}(1-nk)+C_{\pi 2}s)]+R_{in}(1+g_{m1}R_1)(g_{m2}+C_{\pi 2}s)} \quad (37)$$

$$V_n = \frac{R_2\overline{i_{n,eq}}}{1+R_2C_L s} \times \frac{g_{m2}R_{in}(1+g_{m1}R_1)}{(1+R_{in}C_{in}s)[1+R_1C_{\pi 2}s+L_P s(g_{m2}(1-nk)+C_{\pi 2}s)]+R_{in}(1+g_{m1}R_1)(g_{m2}+C_{\pi 2}s)} \quad (38)$$