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A Multi-Phase Cascaded Series-Parallel (CaSP) Hybrid Converter for Direct 48 V to Point-of-Load Applications

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***Abstract*—The rapid growth in data-center electricity consumption has created an imperative need for more energy-efficient solutions to data center power delivery. This work proposes a multi-phase hybrid switched-capacitor (SC) converter for direct 48 V to point-of-load (PoL) conversion with high performance. The proposed topology can be viewed as a 6-to-1 cascaded series-parallel (CaSP) converter merged with a three-phase interleaved buck converter with automatic current balancing. Due to multi-phase operation, the CaSP stage is able to achieve a higher conversion ratio compared to two-phase SC converters with the same number of components as well as lower turn-on voltage for switching devices. Moreover, the proposed CaSP-PoL topology benefits from the frequency multiplication effect similar to that in flying capacitor multilevel converters, which allows for lower frequency operation of higher voltage rated switches and doubled frequency operation of buck inductors, contributing to a further reduction in switching loss and inductor size. A 48 V-to-PoL hardware prototype was built in vertical assembly structure for compact packaging and tested up to 90 A output current, achieving 94.1% peak efficiency (93.2% including gate drive loss) and 702 W/in^3 power density (by box volume) at 2.0 V output voltage.**

I. Introduction

Data-center electricity consumption accounted for about 1% of global electricity demand in 2018 and is forecasted to increase to 8% of projected global demand by 2030 [1], [2]. This rapid growth of computationally intensive information industry has made it imperative to develop more energy-efficient solutions for data center power delivery. Compared to the conventional 12 V bus, the 48 V bus has been demonstrated to be capable of achieving higher overall efficiency due to lower rack distribution loss [3] and therefore has received increased attention in modern data centers. This means that the 48 V bus then needs to be stepped down to the Point-of-Load (PoL) which requires extreme low voltage (e.g. 1.0-2.0 V) and high current (e.g. 100 A and higher).

To achieve such a high step-down conversion ratio, the most straightforward approach is the two-stage architecture [4]–[6] in which the 48 V bus is first stepped down to an intermediate bus (e.g. 12 V) with a bus converter and then regulated down to the load with a PoL converter. Compared to the two-stage approach, direct 48 V-to-PoL conversion has been demonstrated in recent works [7]–[13] to be promising for higher overall system efficiency and power density. These works can be classified into two categories: transformer-based solutions [7], [8] and hybrid switched-capacitor (SC) solutions [9]–[13]. The former comprises an optimized LLC converter with high step-down ratio and customized magnetics merged with a buck converter, whereas the latter comprises a fixed-ratio SC converter merged with a buck converter. Compared to transformer-based solutions, hybrid SC converters demonstrate more efficient utilization of switches [14] and can leverage the superior energy density of capacitors compared to inductors and transformers [15]. By merging the SC and buck stages, the total number of components can be reduced in comparison to the two-stage cascading structure. More importantly, the addition of the buck inductors allows for soft-charging operations of the SC stage, enabling highly efficient conversion [16], [17].

This paper proposes a multi-phase hybrid SC converter that can achieve direct 48 V-to-PoL conversion with high efficiency and high power density. The proposed topology comprises a 6-to-1 *cascaded series-parallel* (CaSP) stage and a three-phase interleaved buck stage with automatic current balancing. Due to multi-phase operation, the CaSP stage is able to achieve a higher conversion ratio compared to two-phase SC converters with the same number of capacitors and switches and enable lower turn-on voltage for the switching devices. The proposed CaSP-PoL topology also benefits from the frequency multiplication effect similar to that in flying capacitor multilevel (FCML) converters, which allows for lower frequency operation of higher voltage rated switches and doubled frequency operation of the buck inductors, further contributing to a reduction in switching loss and inductor size. A 48 V-to-PoL hardware prototype was built in vertical assembly structure to achieve compact packaging and tested up to 90 A output current. At 48-to-2.0 V conversion, the prototype achieved 94.1% peak efficiency (93.2% including gate drive loss) and 702 W/in^3 power density (by box volume).

II. Proposed Topology and Operating Principles

Fig. 1 shows the schematic of the proposed CaSP-PoL converter, with the voltage rating and operating frequency of the main active and passive components listed in Table I. Fig. 2 illustrates the key current waveforms and control signals, with the equivalent circuit model for each phase shown on the right. The proposed topology can be viewed as a 6-to-1 CaSP converter merged with a three-phase interleaved buck converter. The CaSP structure, on the one hand, can be regarded as a 2-to-1 front-end stage followed by a 3-to-1

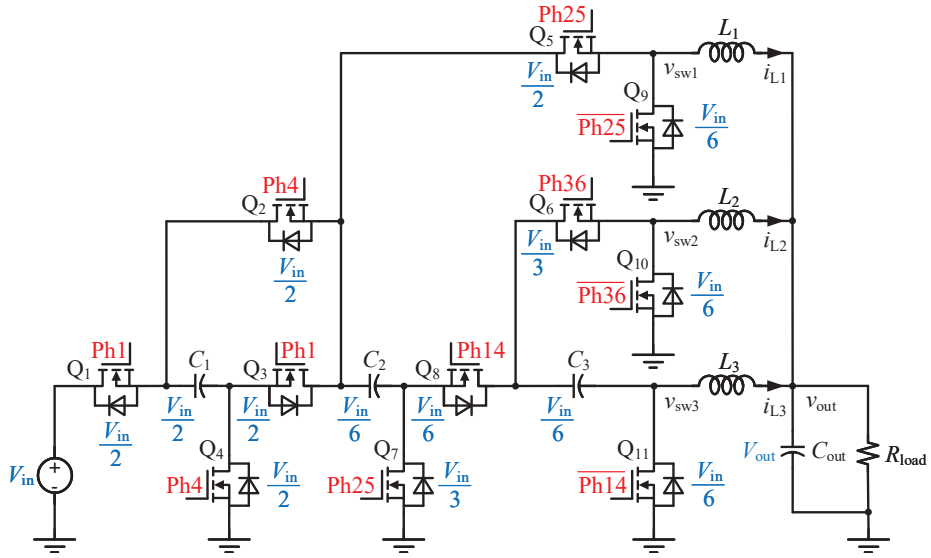


Fig. 1: Schematic of the proposed CaSP-PoL converter with device ratings labeled in blue and control signals labeled in red.

TABLE I: Voltage rating and operating frequency of the main components

	V_{blocking}	f_{sw}
Q_1-Q_4	$\frac{V_{\text{in}}}{2}$	f_0
Q_5	$\frac{V_{\text{in}}}{2}$	$2f_0$
Q_6-Q_7	$\frac{V_{\text{in}}}{3}$	$2f_0$
Q_8	$\frac{V_{\text{in}}}{6}$	$2f_0$
Q_9-Q_{11}	$\frac{V_{\text{in}}}{6}$	$2f_0$ (ZVS)
C_1	$\frac{V_{\text{in}}}{2}$	f_0
C_2-C_3	$\frac{V_{\text{in}}}{6}$	$2f_0$
L_1-L_3	$\frac{V_{\text{in}}}{6} - V_{\text{out}}$	$2f_0$

series-parallel stage. On the other hand, it can also be derived from the classic 4-to-1 series-parallel topology, by moving the source terminals of Q_2, Q_5 and Q_6 from the left-side of L_3 to the positive-side of C_2 and the left-sides of L_1 and L_2, respectively, and removing the switch between the negative-side of C_3 and the left-side of L_3.

As illustrated in Fig. 2, each switching cycle of the proposed converter is divided into multiple phases. The charge and discharge of C_2 and C_3 each takes two phases. C_1 is charged in phase 1 and discharged in phase 4, whereas C_2 and C_3 are charged in phases 1 and 4. C_2 is discharged in phases 2 and 5, and C_3 is discharged in phases 3 and 6. Due to the high conversion ratio of the CaSP stage, the conversion burden on the buck stage is reduced. Another advantage of multi-phase operation is lower turn-on voltage of switching devices. As can be seen in Fig. 2, although Q_7's peak blocking voltage is $\frac{V_{\text{in}}}{3}$, its drain-to-source voltage $V_{\text{ds,Q7}}$ naturally drops to a lower level before it turns on, contributing to reduced switching loss.

In the proposed CaSP-PoL topology, the CaSP stage and the three-phase buck stage are merged together without additional switches or flying capacitors. This helps not only minimize the number of components but also reduce the conduction loss compared to a two-stage approach, contributing to both higher power density and higher efficiency. The operation of the CaSP and buck stages is merged seamlessly to ensure interleaved inductor currents. Each inductor is energized twice in a switching cycle in two different phases by the source or flying capacitors and de-energized twice in the freewheeling phase 7.

The three-phase buck stage has an automatic current balancing capability that is similar to that of the series capacitor buck converter [18], [19]. There is a negative feedback mechanism that keeps the average currents through L_1 and L_2 the same as that through L_3, so that the three inductor currents are naturally balanced. For example, if the average current through L_1 is higher than that through L_3 (i.e. $\langle i_{\text{L1}} \rangle > \langle i_{\text{L3}} \rangle$), then the net charge flowing into C_2 in phases 1, 2, 4 and 5 will be negative, meaning C_2 will be discharged. Therefore, the voltage across L_1 in phases 2 and 5 in which L_1 is energized will decrease while the voltage across L_3 in phases 1 and 4 will increase, so that i_{L1} will decrease and i_{L3} will increase correspondingly until $\langle i_{\text{L1}} \rangle = \langle i_{\text{L3}} \rangle$. A similar analysis can be applied to i_{L2} and i_{L3}. If $\langle i_{\text{L2}} \rangle < \langle i_{\text{L3}} \rangle$, then the net charge flowing into C_3 in phases 1, 2, 3 and 6 will be positive, meaning C_3 will be charged. Therefore, the voltage across L_2 in phases 3 and 6 in which L_2 is energized will increase while the voltage across L_3 in phases 1 and 4 will decrease, so that i_{L2} will increase and i_{L3} will decrease until $\langle i_{\text{L2}} \rangle = \langle i_{\text{L3}} \rangle$. In summary, such a negative feedback mechanism naturally ensures $\langle i_{\text{L1}} \rangle = \langle i_{\text{L3}} \rangle$ and $\langle i_{\text{L2}} \rangle = \langle i_{\text{L3}} \rangle$ so that the three-phase interleaved inductor currents can be naturally balanced.

In addition, the abovementioned automatic current balancing capability can also be explained with a more quantitative analysis. Due to the triangular shape of the inductor currents, the average inductor current in the rising and falling stages will be the same as the average current over one switching cycle in the periodic steady state (PSS). Therefore, in PSS, the average currents through the flying capacitors can be given as

$$\begin{cases} \langle i_{\text{C1}} \rangle = \frac{D}{6} \langle i_{\text{L3}} \rangle - \frac{D}{6} \langle i_{\text{L3}} \rangle \\ \langle i_{\text{C2}} \rangle = \frac{D}{3} \langle i_{\text{L3}} \rangle - \frac{D}{3} \langle i_{\text{L1}} \rangle \\ \langle i_{\text{C3}} \rangle = \frac{D}{3} \langle i_{\text{L3}} \rangle - \frac{D}{3} \langle i_{\text{L2}} \rangle \end{cases}. \tag{1}$$

In PSS, the average currents through the flying capacitors should be zero, i.e.

$$\langle i_{\text{C1}} \rangle = \langle i_{\text{C2}} \rangle = \langle i_{\text{C3}} \rangle = 0. \tag{2}$$

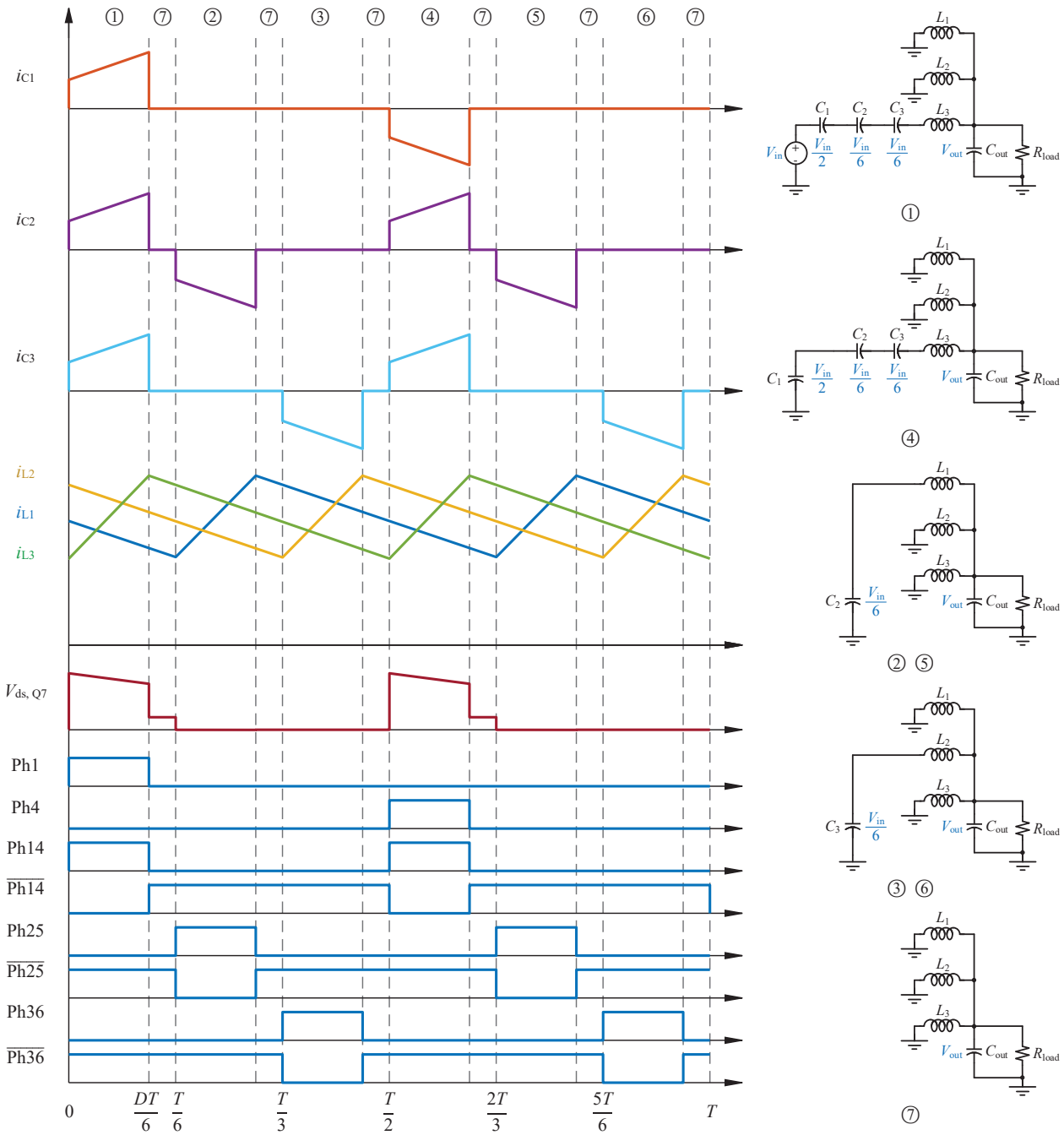


Fig. 2: Key current waveforms and control signals of the proposed hybrid SC converter. The equivalent circuit model for each phase is shown on the right.

Substituting (2) into (1) yields $\langle i_{L1}\rangle = \langle i_{L3}\rangle$ and $\langle i_{L2}\rangle = \langle i_{L3}\rangle$, which means well-balanced inductor currents can be automatically achieved in PSS.

Moreover, the proposed CaSP-PoL converter benefits from the frequency multiplication effect similar to that in FCML converters. If C_1 and Q_1-Q_4 operate at a frequency f_0, then the other main components operate at a frequency $2f_0$. As listed in Table I, the switches with higher voltage ratings (Q_1-Q_4) operate at lower switching frequency than those with lower voltage ratings, which is favorable to switching loss reduction. Since the operating frequency of the inductors is doubled due to multi-phase operation, lower inductance can be chosen while maintaining the same inductor current ripple. Also, due to the reduced switch voltage stress in the CaSP stage, low-voltage MOSFETs with lower $R_{ds(on)}$ and lower switching loss can be used. In addition, Q_9-Q_{11} operate with zero-voltage switching (ZVS) turn-ON.

The conversion ratio of the proposed converter can be de-

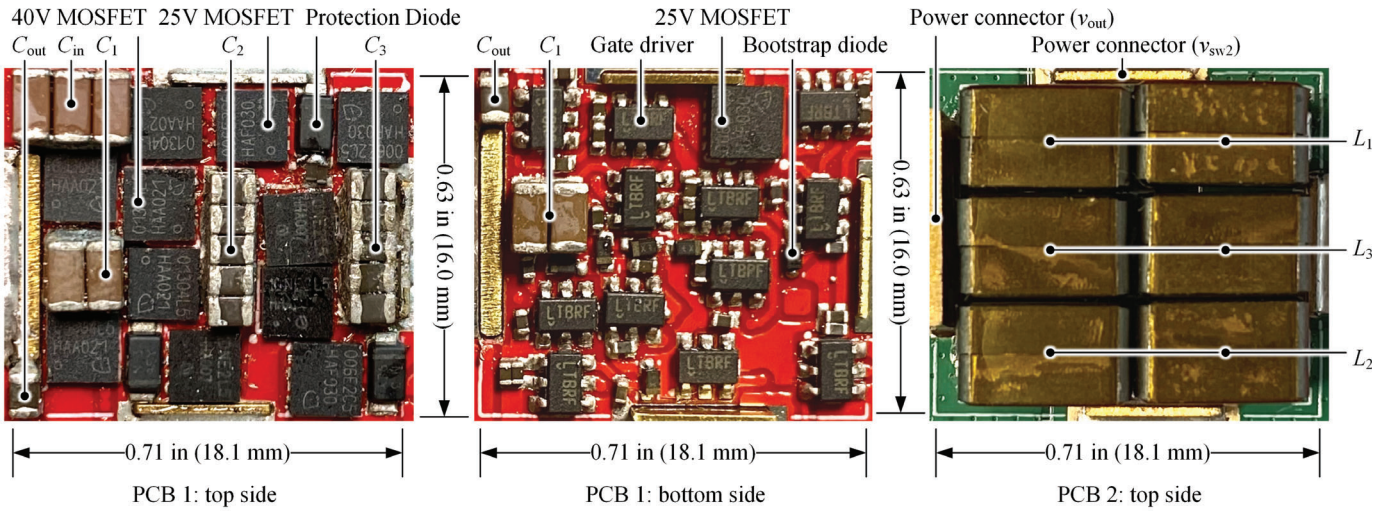


Fig. 3: Photograph of the hardware prototype. Dimensions: PCB 1: $0.71 \times 0.63 \times 0.24$ inch ($18.1 \times 16.0 \times 6.2$ mm); PCB 2: $0.71 \times 0.63 \times 0.33$ inch ($18.1 \times 16.0 \times 8.3$ mm).

rived based on the volt-second balance of the buck inductors:

$$\begin{aligned} &(\frac{V_{\text{in}}}{6} - V_{\text{out}}) \cdot \frac{DT}{6} + (-V_{\text{out}}) \cdot (\frac{T}{2} - \frac{DT}{6}) = 0 \\ &\Rightarrow \quad V_{\text{out}} = \frac{D}{18} V_{\text{in}} \end{aligned} \tag{3}$$

where D is the duty ratio of phases $1-6$ with respect to $\frac{T}{6}$, as illustrated in Fig. 2. Therefore, the output voltage can be regulated by adjusting the duty cycle.

III. Hardware Implementation and Experimental Results

Figures 3 and 4 show the annotated photograph and 3D assembly drawing of the converter prototype, with the key parameters and component list tabulated in Tables II and III, respectively.

As illustrated in Fig. 4, the prototype consists of two vertically stacked PCBs connected via nodes v_{sw1}, v_{sw2}, v_{sw3} and v_{out} (labeled in Fig. 1) with thick copper sheets (0.5 mm thick for v_{sw1}, v_{sw2} and v_{sw3}, and 1.0 mm thick for v_{out}). PCB 1 contains the switches, flying capacitors and gate drive circuitry while the inductors are placed on PCB 2.

This vertical structure can not only ease the layout design since it offers an addition dimension for component placement but also facilitate full utilization of the box volume of the converter. Commercial inductors with the desired parameters and the small footprint required in this design are typically high-profile with a height of more than 7 mm and are significantly taller than the other components (e.g. MOSFETs and capacitors) that are lower than 2 mm. If the inductors are placed on the same board with the other components, it would be difficult to achieve the smallest possible box volume since the large space above the low-profile components could not be utilized. Instead, by stacking the high-profile inductors and the other low-profile components in the way illustrated in Fig. 4, all main components are tightly packaged within a $0.71 \times 0.63 \times 0.57$ inch box with most space inside the box effectively utilized.

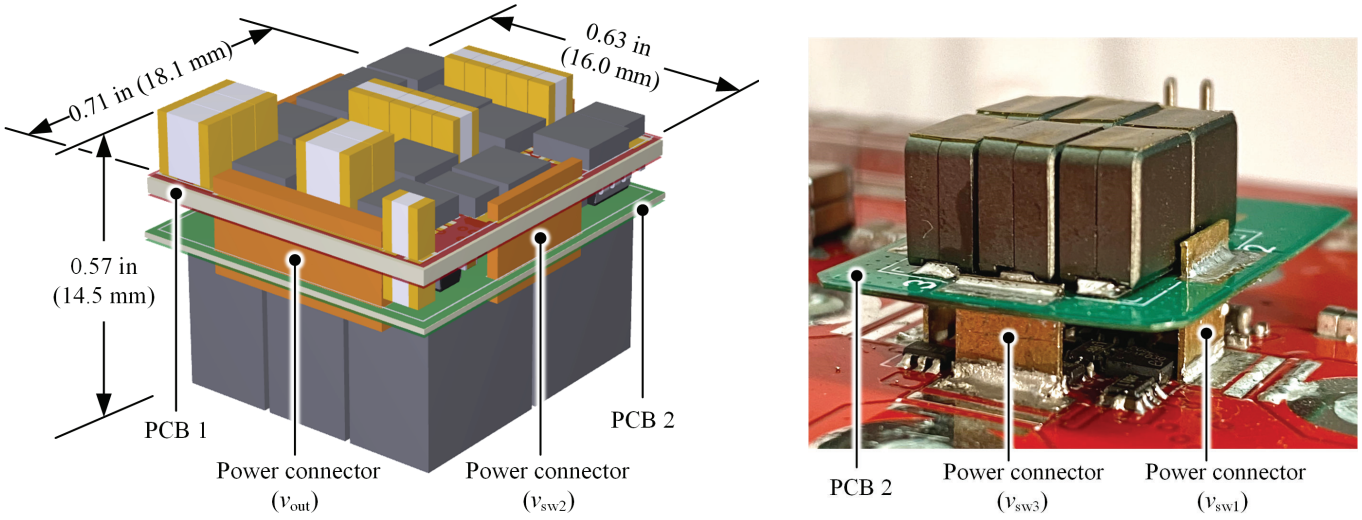
TABLE II: Key parameters of the prototype

Parameter	Value
Input voltage	48 V
Output voltage	1.2-2.0 V*
Output current	90 A
Switching frequency f_0	160 kHz
Inductor operating frequency $2f_0$	320 kHz
Prototype box volume	0.256 in^3
Power component volume+	0.136 in^3
Current density	351 A/in^3

* The converter prototype is able to operate at 1.0 V and lower output voltages but was only tested to 1.2 V due to the limited capability of the electronic load.

+ The power components included in the volume calculation are switching devices, capacitors and inductors.

In this prototype, efficiency is slightly traded for higher power density. Therefore, the selection of inductor is first based on the suitable footprint size that can be packaged with the other components in a rectangular box. Additionally, to achieve high efficiency, inductors with high inductance and low DCR should be selected. Finally, the TDK VLBU805080T-R18L with 5×8 mm footprint, 180 nH inductance and 0.2 mΩ DCR was selected. For each inductor (L_1-L_3 in Fig. 1), two TDK VLBU805080T-R18Ls are connected in series. As for the selection of flying capacitors, the capacitance design in this regulated converter is largely relaxed compared to the resonant converters [20] in which the L and C values have to be precisely tuned. Relatively small flying capacitors can be employed as long as they can ensure sufficiently small capacitor voltage ripples that will not cause overvoltage



(a) (b)

Fig. 4: Vertical assembly of the prototype. (a) 3D assembly drawing. Dimensions: $0.71 \times 0.63 \times 0.57$ inch ($18.1 \times 16.0 \times 14.5$ mm). (b) Photograph of the power connectors in the prototype.

TABLE III: Component list of the prototype

Component	Part number	Parameters
MOSFET Q_1-Q_5	Infineon IQE013N04LM6	40 V, 1.35 mΩ
MOSFET Q_6-Q_8	Infineon BSZ010NE2LS5	25 V, 1.0 mΩ
MOSFET Q_9-Q_{10}	Infineon IQE006NE2LM5CG	25 V, 0.65 mΩ
MOSFET Q_{11}	Infineon IQE006NE2LM5CG	25 V, 0.65 mΩ ×2 (in parallel)
Flying capacitor C_1	TDK C3216X5R1V226M160AC	X5R, 35 V, 22 μF*×6 (in parallel)
Flying capacitor C_2-C_3	TDK C2012X6S1C226M125AC	X6S, 16 V, 22 μF*×10 (in parallel)
Inductors L_1-L_3	TDK VLBU805080T-R18L	180 nH, 0.2 mΩ ×2 (in series)
Input capacitor C_{in}	TDK C3216X7S2A335K160AB	X7S, 100 V, 3.3 μF*×6 (in parallel)
Output capacitor C_{out}	TDK C2012X5R1A476M125AC	X5R, 10 V, 47 μF*×3 (in parallel)
Gate driver	Analog Devices LTC4440-5	80 V, high-side
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V, Schottky diode

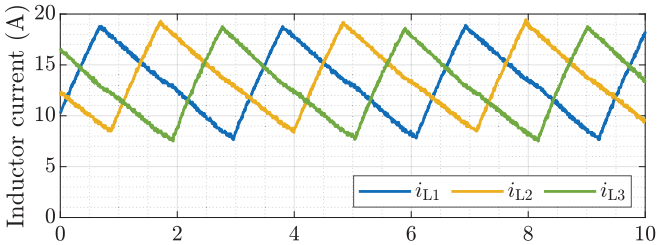
* The capacitance listed in this table is the nominal value before DC derating.

breakdown of switching devices and imbalanced inductor currents. Choosing larger flying capacitors can help reduce total capacitor ESR and hysteresis loss [21], [22] and ensure well-balanced inductor currents.

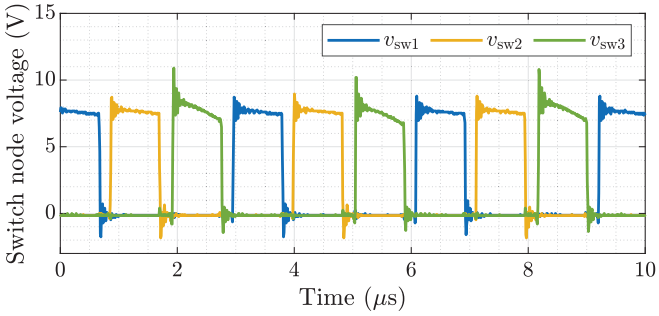
As listed in Table I, due to the reduced switch voltage stress in the CaSP stage, low-voltage MOSFETs with lower $R_{\text{ds(on)}}$ and lower switching loss can be used (40 V for Q_1-Q_5 and 25 V for Q_6-Q_{11}). An additional switch is added in parallel to Q_{11} to reduce the conduction loss since it carries two-times higher peak current than Q_9 and Q_{10}. The floating switches are driven by high-side gate drivers with internal level-shifters that are powered by a cascaded bootstrap circuit [23]. The gate drive voltage is 7.0 V in this prototype. The output voltage is regulated with a hysteretic control on the duty cycle D in which D will be increased by a step ΔD if the measured output voltage is lower than the reference value and will be reduced by ΔD if the measured output voltage is higher than the reference value. More advanced control techniques can be employed for desired transient response and control bandwidth, but are not the focus of this work. PCB 1 has 6 layers and is fabricated with 3 oz copper on the outer layers and 2 oz in the inner layers. PCB 2 has 2 layers and is fabricated with 3 oz copper. Thicker outer copper can be used to help further reduce the PCB trace loss.

Figs. 5(a) and (b) show the measured waveforms of the inductor currents and switch node voltages, respectively. As can be seen in Fig. 5(a), the three-phase interleaved inductor currents are naturally well-balanced which verifies the automatic current balancing capability explained in Section II. Fig. 6 presents the measured ZVS turn-ON waveforms of Q_{11}. These waveforms are also representative of Q_9 and Q_{10}.

Figs. 7(a) and (b) show the measured power stage efficiency



(a)



(b)

Fig. 5: Experimental waveforms of the proposed CaSP-PoL converter (V_{out} = 2.0 V, I_{out} = 40 A). (a) Balanced interleaved inductor currents. (b) Switch node voltages.

TABLE IV: Measured efficiency and power density of the prototype at various output voltages

Output voltage	Power stage efficiency	System efficiency (including gate drive loss)	Power density*
2.0 V	Peak: 94.1% Full load: 90.2%	Peak: 93.2% Full load: 89.9%	702 W/in^3 401 W/in^2
1.8 V	Peak: 93.8% Full load: 89.8%	Peak: 92.8% Full load: 89.5%	632 W/in^3 361 W/in^2
1.5 V	Peak: 93.3% Full load: 88.8%	Peak: 92.1% Full load: 88.5%	527 W/in^3 301 W/in^2
1.2 V	Peak: 92.5% Full load: 87.6%	Peak: 91.1% Full load: 87.2%	421 W/in^3 241 W/in^2

* The volumetric power density listed here is calculated based on the prototype box volume in Table II. The areal power density listed here is calculated based on the prototype box area 0.71 × 0.63 inch (18.1 × 16.0 mm) shown in Fig. 3.

and system efficiency (including gate drive loss) of the prototype at various output voltages, with the peak and full-load efficiency and power density (by box volume) summarized in Table IV. The efficiency of the prototype was measured with the following equipment: the input voltage and current were measured with digital multimeters Keysight 34401A and 34405A, respectively, and the output voltage and current were measured with electronic loads Rigol DL3021 and DL3031. Note that although Table IV only lists the measured efficiency at 1.2-2.0 V output voltages, the converter prototype is able to operate at 1.0 V and lower output voltages but was only

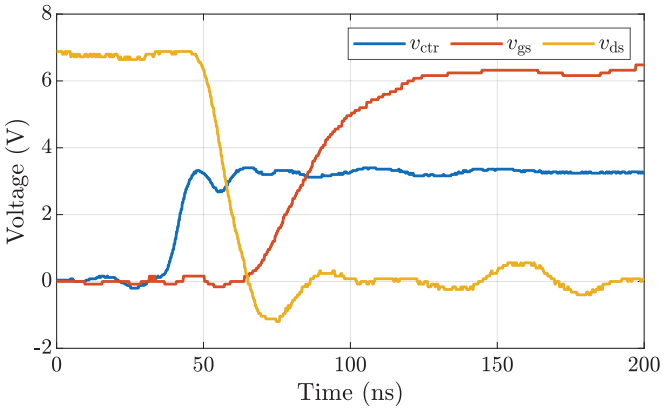
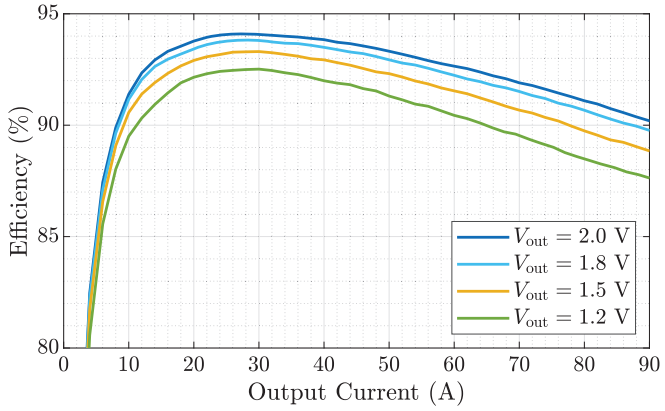
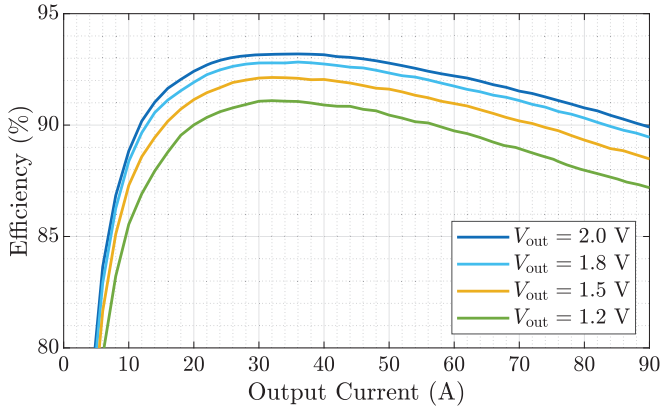


Fig. 6: ZVS turn-ON of Q_{11}. v_{ctr}: PWM control signal, v_{gs}: gate-to-source voltage, v_{ds}: drain-to-source voltage.



(a)



(b)

Fig. 7: Measured efficiency of the prototype at various output voltages. (a) Power stage efficiency. (b) System efficiency (including gate drive loss).

tested to 1.2 V due to the limited capability of the electronic load Rigol DL3031 whose minimum operating voltage is 1.3 V at 60 A. The prototype was tested up to 90 A output current and achieved a current density of 351 A/in^3. At 48-to-2.0 V conversion and f_0 = 160 kHz switching frequency (320 kHz seem by the inductors), the prototype achieved 94.1% peak

TABLE V: Comparison between this work and existing hybrid SC works

Reference	Conversion Ratio	Output Current	Power Density	Power Stage Efficiency
This work	48-to-2.0 V	90 A (30 A/phase)	702 W/in^3 (by box volume) 1328 W/in^3 (by power component volume$^+$)	Peak efficiency: 94.1% Full load efficiency: 90.2%
	48-to-1.5 V	90 A (30 A/phase)	527 W/in^3 (by box volume) 996 W/in^3 (by power component volume$^+$)	Peak efficiency: 93.3% Full load efficiency: 88.8%
MLB-PoL [11]	48-to-2.0 V	65 A (32.5 A/phase)	395 W/in^3 (by box volume)	Peak efficiency: 95.1% Full load efficiency: 91.3%
	48-to-1.5 V	65 A (32.5 A/phase)	296 W/in^3 (by box volume)	Peak efficiency: 94.4% Full load efficiency: 89.9%
MIH [9]	48-to-2.0 V	40 A (13.3 A/phase)	426 W/in^{3*} (by power component volume$^+$)	Peak efficiency: 94.6%* Full load efficiency: 87.2%* (including calculated gate charge loss)
DP-MIH [10]	48-to-2.0 V	100 A (25 A/phase)	304 W/in^3 (by estimated box volume)	Peak efficiency: 93.6% Full load efficiency: 87.1% (including gate drive loss)
7-level FCML [24]	48-to-2.0 V	10 A (10 A/phase)	N/A	Peak efficiency: 85.0% Full load efficiency: 81.5%
LEGO-PoL [12]	48-to-1.5 V	300 A (25 A/phase)	171 W/in^{3*} (by box volume)	Peak efficiency: 96.0%* Full load efficiency: 87.7%*
Crossed-coupled QSD buck [13]	48-to-1.5 V	40 A (20 A/phase)	150 W/in^3 (by power component volume$^+$)	Peak efficiency: 95.1%* Full load efficiency: 92.7%*

* According to direct correspondence with the author.

$^+$ The power components included in the volume calculation are switching devices, capacitors and inductors.

efficiency (93.2% including gate drive loss) and 90.2% full load (89.9% including gate drive loss), and 702 W/in^3 power density (by box volume).

Fig. 8 shows the thermal image of the prototype at equilibrium with fan cooling only at $V_{\rm out} = 1.2$ V, $I_{\rm out} = 90$ A, and 27.8 °C ambient temperature. As shown in Fig. 8, the maximum temperature on the board is 91.8 °C. Note that better thermal performance can be achieved by adding heat sinks on the MOSFETs without increasing the box volume since there is still room above the MOSFETs as illustrated in Fig. 4(a).

Table V compares this work with several best existing hybrid SC works with similar voltage conversion ratios. It can be seen that the proposed CaSP-PoL converter achieves a very high power density, while maintaining excellent peak and full-load efficiency. Note that some power density numbers in Table V are calculated by box volume, while others are by power component volume which can be much smaller than the real box volume of the converter. For reference, the power density by power component volume of our design is also provided in Table V. As explained above, the vertical assembly structure is adopted in this prototype to help package all main components in a rectangular box, which necessitates the use of power connectors to join the two PCBs. Since the power connectors at switch nodes $v_{\rm sw1}$, $v_{\rm sw2}$ and $v_{\rm sw3}$ conduct inductor currents $i_{\rm L1}$, $i_{\rm L2}$ and $i_{\rm L3}$ that ripple at 320 kHz, the addition of the power connectors incurs not only additional DC conduction loss but also AC conduction loss that cannot be easily reduced by increasing the thickness of the copper sheets due to the skin effect. Therefore, this prototype is designed to trade efficiency for relatively better power density. This can be seen in Table V as this prototype achieved 1.8 times higher power density at the cost of around 1% lower efficiency compared to the MLB-PoL converter proposed in [11]. For further optimization, low-profile customized inductors and board cutouts for recessing inductors can be used so that the inductors in this converter could be placed on the same board with the rest of the components without increasing the overall height of the converter, which could remove the need for power connectors and help achieve higher efficiency.

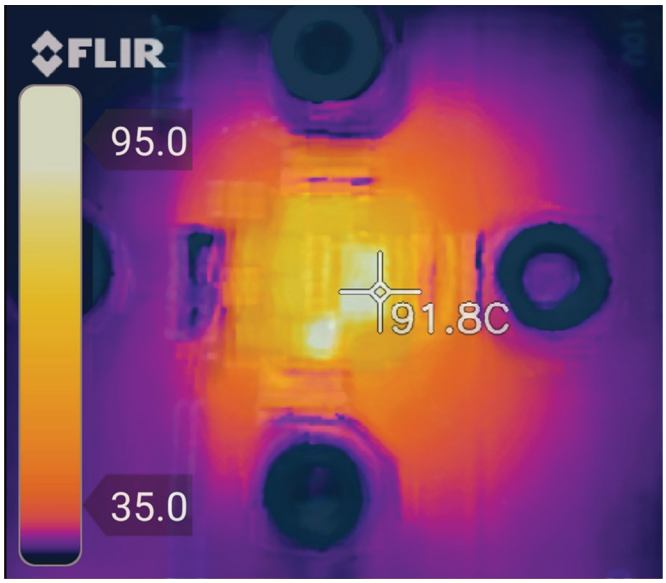


Fig. 8: Thermal image at equilibrium with fan cooling only ($V_{\text{out}} = 1.2$ V, $I_{\text{out}} = 90$ A, ambient temperature: 27.8 °C).

IV. Conclusion

This paper presents a multi-phase hybrid SC converter for direct 48 V-to-PoL conversion with high efficiency and high power density. The proposed topology comprises a 6-to-1 cascaded series-parallel (CaSP) stage and a three-phase interleaved buck stage with automatic current balancing. It benefits from the multi-phase operation and frequency multiplication effect which help decrease the number of components, reduce the switching loss, and shrink the inductor size. A 48 V to 2.0-1.2 V hardware prototype was built and assembled vertically to facilitate compact packaging and achieve high power density. The prototype was tested up to 90 A output current, achieving 94.1% peak efficiency (93.2% including gate drive loss) and 702 W/in^3 power density (by box volume) at 2.0 V output voltage.

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