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An 8-Level Flying Capacitor Multi-Level Boost Converter for High-Voltage Power Distribution in Electric Aircraft

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Abstract—Aviation is a rapidly growing transportation sector that has been seeing a shift towards more-electric and fully electric propulsion systems. Lightweight onboard DC-DC converters play a critical role in this transition by managing the varying DC voltages associated with battery charge and discharge, enabling the integration of diverse battery technologies onto a common DC bus, reducing high-voltage insulation mass by allowing lower battery voltages, and embedding fault protection directly within the converters. To support these applications, this work demonstrates an 8-level flying capacitor multilevel (FCML) converter designed and tested to boost an input battery voltage of 500-786 V to a 1000 V DC bus. The demonstrated system integrates embedded control, sensing, startup, and output disconnect. It achieves over 99.0% peak efficiency, as well as a gravimetric power density exceeding 100 kW/kg for the power stage.

I. INTRODUCTION

The rapidly growing aviation sector is experiencing a shift towards more-electric and fully electric propulsion systems [1], [2]. Key obstacles to the realization of more-electric and fully electric aircraft are the size and weight of the electric motor, power source, and power converters. Because these components are tightly coupled, advancements in power electronics directly impact overall system mass and performance. This work focuses on the use of an ultra-light high-voltage boost system to interface the battery pack to the DC bus, as shown in Fig. 1. This offers several key advantages in reducing overall system size and weight. First, operation at higher voltages – particularly at high altitudes – demands robust electrical insulation, which contributes significantly to overall system mass [3], [4]. By enabling the use of lower-voltage batteries, the boost system reduces insulation requirements within the

battery pack. Second, the architecture facilitates integration of different battery technologies (and, if desired, alternative energy sources such as fuel cells) on a common DC bus. Finally, this DC-DC conversion system regulates the varying voltages associated with battery charge and discharge, while embedding fault protection within the converters themselves.

Realization of these advantages necessitates power converters with exceptionally high performance, with literature projecting specific power density targets of 50 kW/kg for future aerospace power converters [5], [6]. This work presents the design of a power converter exceeding this specification within the high-voltage boost system that steps up a range of battery voltages to a shared 1000 V DC bus for the electrical propulsion system, as shown in Fig. 1.

The flying capacitor multi-level (FCML) converter [7] is an excellent candidate for electric aviation applications because it enables high power density and high efficiency simultaneously [8]–[12]. The multi-level topology enables the use of high figure-of-merit switches [13], [14] rated for voltages far lower than the maximum port voltage of the converter. In addition, the FCML converter minimizes passive component volume and mass by relying on high-density capacitive energy storage [15]. Fig. 2 shows the circuit schematic for a generalized N -level FCML boost converter. The converter's switching signals s_k are generated with symmetric phase-shifted pulse-width modulation (PS-PWM) [16]. The reduced amplitude of v_{sw} , along with its increased frequency, allows the use of an $(N - 1)^2$ times lower filter inductance compared to a 2-level converter for a given ripple current specification.

This work explores optimization of the FCML converter design to maximize specific power density, notably by exploring

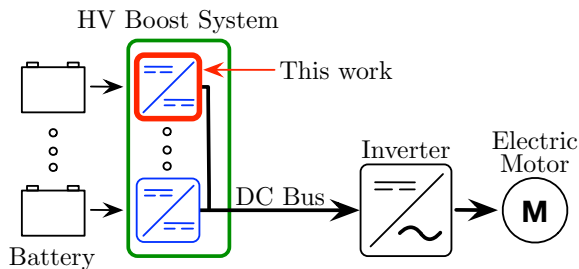


Fig. 1: The HV boost system consists of several converters that interface battery voltages with the propulsion DC bus. This work demonstrates one such converter.

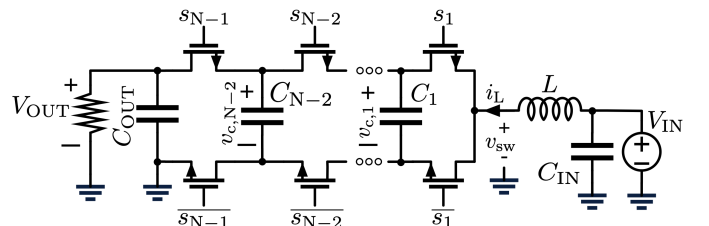


Fig. 2: Schematic of an N -level FCML converter with $N - 1$ complementary switch pairs and $N - 2$ flying capacitors. The input voltage is boosted from V_{IN} to V_{OUT} .

Table I
CONVERTER OPERATING PARAMETERS

Parameter	Value
Input Voltage	500–786 V
Output Voltage	1000 V
Output Power	10 kW
Switching Frequency	65 kHz
Peak Efficiency	99.1%
Power Stage Gravimetric Density	103 kW/kg
System Gravimetric Density	50.3 kW/kg
Power Stage Volumetric Density	117 kW/L
System Volumetric Density	32.2 kW/L

the loss redistribution between the switches and the inductor, shifting some of the dominant turn-on loss to inductor core losses. Additionally, this work demonstrates a fully contained system integrating startup, output disconnect, sensing, and embedded control, while also achieving state-of-the-art power density.

Section II outlines the hardware design for this work, including the converter optimization and startup circuitry. Section III describes the performance evaluation of the hardware prototype, highlighting efficiency versus output power and input voltage, as well as capacitor balancing during startup. Section IV concludes the paper.

II. HARDWARE DESIGN

To demonstrate the benefits of the FCML converter for high-voltage power distribution in electric aircraft, the converter in this work is designed to boost an input voltage between 500 V and 786 V to an output voltage of 1000 V. Table I outlines the converter’s operating parameters and realized performance.

As shown in Fig. 1, each converter within the HV boost system shares the battery input voltage and the high voltage DC bus. While this work focuses on the demonstration of a single converter, multiple units can be paralleled or interleaved to increase the system power handling capacity and realize the system in Fig. 1.

A. Converter Optimization

Passive components represent a key obstacle to increasing power density in conventional power converters [17]. The $(N - 1)^2$ reduction of the inductance, enabled by the FCML converter, provides a pathway for significant size and weight reduction [18], [19]. At very high level counts, the marginal gains in further reduction of the filter inductance are outweighed by the additional required switches and gate drive circuitry. An 8-level converter is used in this work, which allows the use of 200 V gallium nitride high-electron-mobility transistors (GaN HEMTs) in a 1000 V application, including consideration for flying capacitor voltage ripple and overshoots at switching transitions. To minimize commutation loop inductance, each switching cell in this design utilizes a lateral commutation loop with plane [20], [21] and local decoupling capacitors [22].

For converter designs relying on forced air cooling without heat sinking, losses in the transistors often limit the converter’s

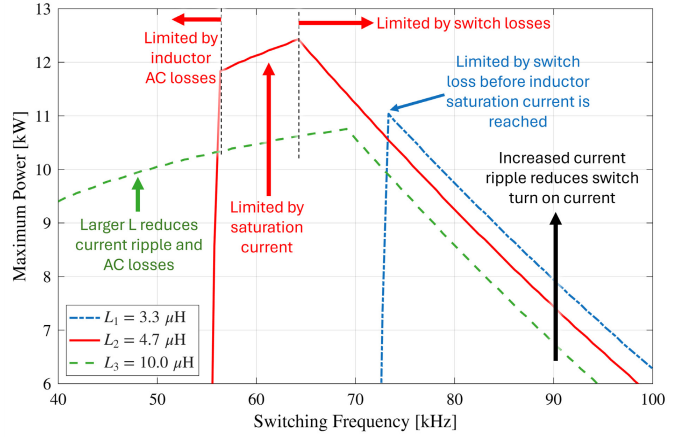


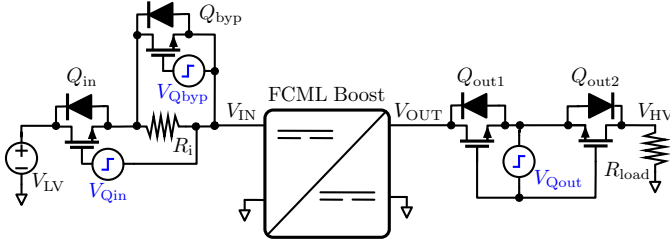
Fig. 3: Maximum output power capacity of the converter as a function of switching frequency for select inductances from Vishay’s IHL8787MZ-5A family. Maximum loss is allowed to be 4 W per paralleled pair of EPC2307 switches.

maximum power rating. Despite the fact that we use very high figure-of-merit [13], GaN HEMTs in this work, this continues to be the case. These transistors exhibit substantially greater thermal resistance than the inductor, owing to their much smaller physical size. Therefore, an exchange of increased inductor losses for decreased switch losses will result in improved power density. This may be achieved by adjusting the inductance and switching frequency. Both parameters impact the switching losses of the hard-switched GaN devices (switches gated by $\overline{s_1} \dots \overline{s_7}$ in this work), which is a significant contributor to overall switch losses [9], [10], [18]. Fig. 3 illustrates the impact on the converter’s maximum output power when the inductance and switching frequency are adjusted. The maximum output power is plotted against frequency for three different inductances $L_1 = 3.3 \mu\text{H}$, $L_2 = 4.7 \mu\text{H}$, $L_3 = 10 \mu\text{H}$ within the same package from Vishay’s IHL8787MZ-5A family. The inductor core losses are estimated using the improved generalized Steinmetz equation (iGSE) [23], [24] based on manufacturer-provided data [25]. Each switch in the FCML converter is realized with two parallel GaN devices. The parallel devices are driven with a common gate driver and thus it is assumed that both switching and conduction losses [26] are equally distributed between the two switches.

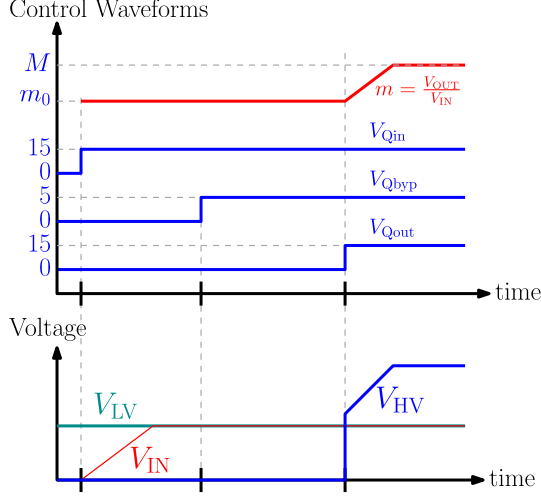
At high frequencies, the output power is constrained by the GaN devices’ switching losses. At low frequencies, the output power is constrained by the inductor’s thermal limit. In between, the inductor’s saturation current limit must be considered. As the inductance and frequency are varied, there is a tradeoff in losses between the inductor and the GaN switches. As shown in Fig. 3, a switching frequency of roughly 65 kHz and a 4.7 μH inductance represents the optimal tradeoff in this application, yielding the maximum output power.

B. Startup

When the FCML boost converter is powered up, the flying capacitors are initially discharged. Under PS-PWM, the flying capacitor voltages reach their nominal steady-state values $v_{C,k} = \frac{k}{N} V_{\text{OUT}}$ via natural balancing [16], [27],



(a) Startup and output disconnect circuits. Q_{in} , Q_{out1} , and Q_{out2} are implemented with 1200 V SiC MOSFETs. Q_{byp} is implemented with a 25 V Si MOSFET.



(b) Control waveforms and associated voltage waveforms for startup sequence.

Fig. 4: Startup and output disconnect circuitry.

[28]. However, the startup transient is characterized by slow underdamped oscillations [29] which can result in excessive voltage stress on the switches, which are not rated to block the full output voltage. Thus, a startup circuit that ramps the input supply voltage is used in prior work [10], [30]–[32].

Fig. 4a demonstrates the startup and output disconnect circuit used in this design. Switches Q_{out1} and Q_{out2} are used to disconnect the load from the FCML boost converter, notably under two conditions: startup and fault.

- **Startup:** The load resistance is isolated from the startup circuitry to allow the input of the FCML converter V_{IN} to ramp up to the input source voltage V_{LV} . When turned off, Q_{out1} prevents current from flowing to the load through reverse conduction of the high-side switches $s_1 \dots s_7$ in the FCML boost converter.
- **Fault:** The converter is isolated from the load, and is thus isolated from the shared HV bus in the overall boost system in the event of a fault. Under such a condition, it is possible for the output V_{HV} to remain charged at a voltage higher than V_{IN} . When turned off, Q_{out2} prevents current from back feeding the converter input port through reverse conduction of the high-side switches $s_1 \dots s_7$ in the FCML boost converter.

Fig. 4b illustrates the key waveforms involved in the startup process. The startup sequence is initiated by turning on Q_{in} , which sources constant current, determined by R_i , to the input

Table II
KEY COMPONENT VALUES

Component	Value
GaN HEMT	$2 \times$ parallel EPC2307
Input Inductor	IHLP8787MZER4R7
Derated Flying Capacitance	$1.6 \mu\text{F}$
Bulk Flying Capacitor C_1	C5750X7S2A226M280KB
Bulk Flying Capacitor C_2 – C_6	C5750X6S2W225K250KA
Decoupling Flying Capacitor	$8 \times$ C1206C103KFRACU
GaN Switch Gate Driver	LM5114
Power and Signal Isolator	ADUM5240
Startup Switch	IMBG120R008M2H
Output Disconnect Switch	IMBG120R008M2H
Startup Bypass Switch	BSZ013NE2LS5IATMA1
SiC Switch Gate Driver	TPSI3052
DSP	TMS320F28379D

of the FCML converter V_{IN} . While V_{IN} ramps linearly up to V_{LV} , the FCML boost converter is initialized to a conversion ratio, m_0 , slightly higher than one such that switching action balances the flying capacitor voltages.

The startup ramp rate is a trade-off between startup time, power dissipation in R_i and Q_{in} , and natural balancing dynamics. Since the system is designed to be connected to a static battery in this application, there is no strict startup time requirement.

Q_{byp} is turned on to bypass the startup resistor R_i , presenting a low-impedance connection to the source. The placement of Q_{byp} across R_i allows the use of a low-voltage device. When the load is connected by turning on Q_{out1} and Q_{out2} , there is a step change in the output current. However, this does not disrupt the operation of the converter and capacitor balance. The converter then ramps up its output voltage to the target 1000 V.

C. Onboard Controller

The control signals for startup, output disconnect and the FCML boost converter are generated by an on-board microcontroller unit (MCU) that utilizes the TI TMS320F28379D DSP. The controller also contains differential serial communication to output telemetry and to receive external commands to operate as a subsystem alongside other converters within the larger HV boost system. The MCU interfaces with onboard voltage and current sensors. This would allow the controller to implement active balancing with this hardware, [33] using all or a reduced subset of capacitor voltage sensors [34]–[36]. However, the experimental results presented in this paper are focused on the power stage performance and are obtained using natural balancing.

D. Hardware Design

An annotated photograph of the hardware prototype, designed in this work, is shown in Fig. 5. The FCML boost converter is outlined as the power stage. Converter operating parameters are listed in Table I, highlighting the density metrics for both the power stage and the full system. Both exceed the targets outlined in [5], [6] for future aerospace applications. The key components are outlined in Table II. For each of

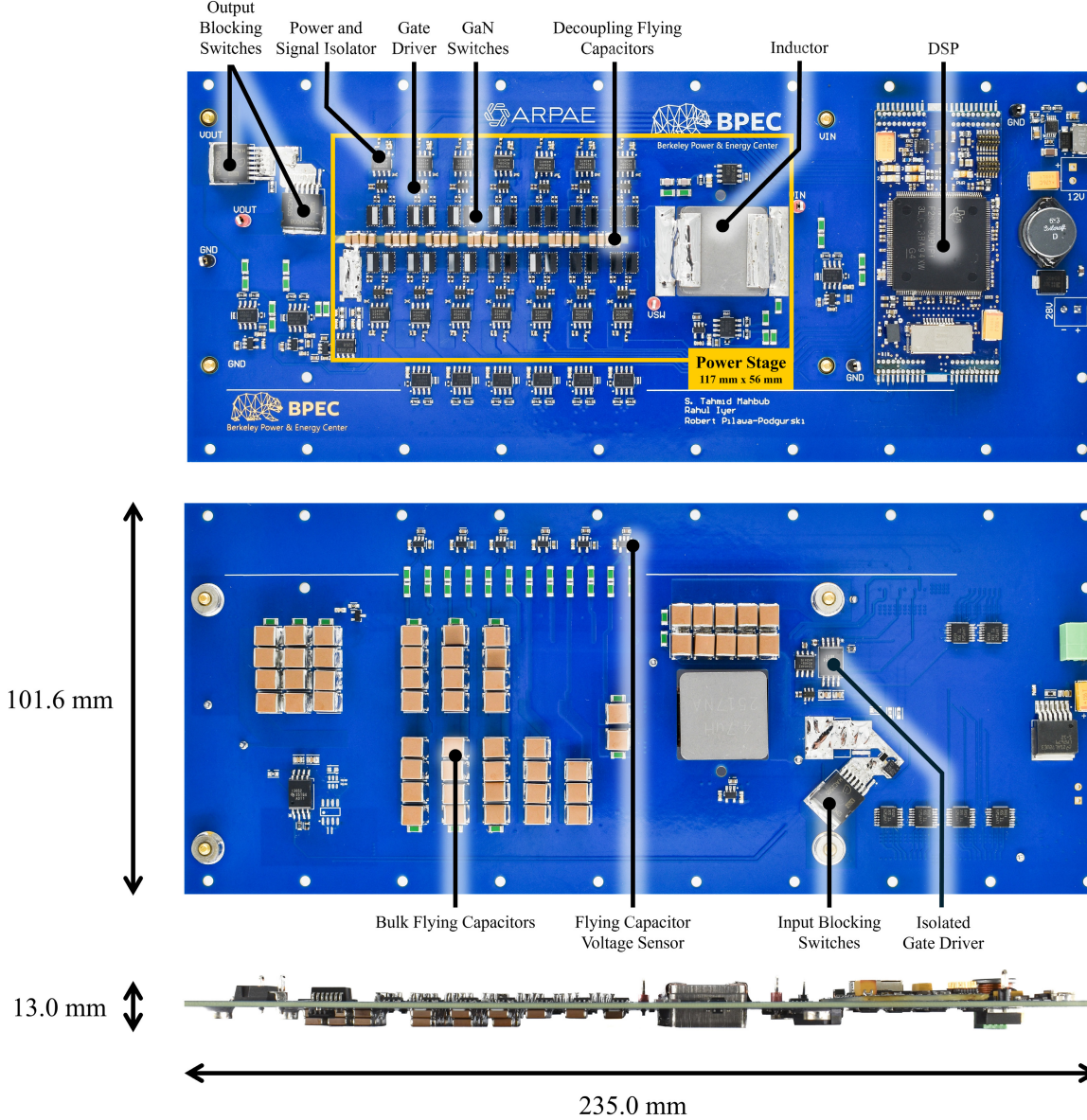


Fig. 5: Prototype hardware demonstrated in this work. Key components are annotated, and values are listed in Table II.

the flying capacitors $C_1 \dots C_6$, the target derated capacitance is obtained by connecting series-parallel combinations of the components listed in Table II.

A mass breakdown for the hardware prototype is given in Fig. 6. The power stage represents about 49% of the overall hardware mass. The largest contributors to the prototype mass are the bare PCB and the inductor. The flying capacitors and the MCU board also yield significant mass contributions.

III. EXPERIMENTAL RESULTS

The hardware prototype is tested across input supply voltages that reflect the range of battery voltages outlined in Table I and various output resistances to simulate different loads

on the aircraft high-voltage DC bus. A Keysight PA2201A IntegraVision Power Analyzer is used for efficiency characterization. Measurements are taken with forced air cooling applied across the GaN switches in the FCML converter.

Fig. 7 shows the efficiency sweeps for the converter power stage at battery voltage corners, peaking at 99.1%. Fig. 8 shows the thermal results when operating the converter at its maximum power. Fig. 7b shows how the efficiency varies as the input voltage is varied. Since the design optimization relies on large inductor current ripple, the inductor AC losses contribute significantly to the total losses. This drives the shape of the efficiency curve, which has local maxima at nominal

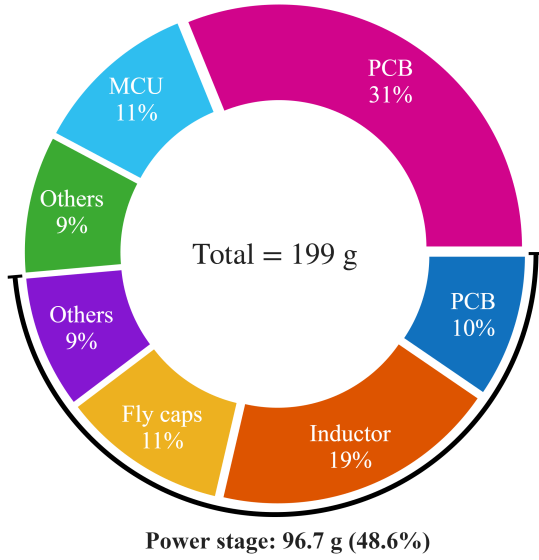
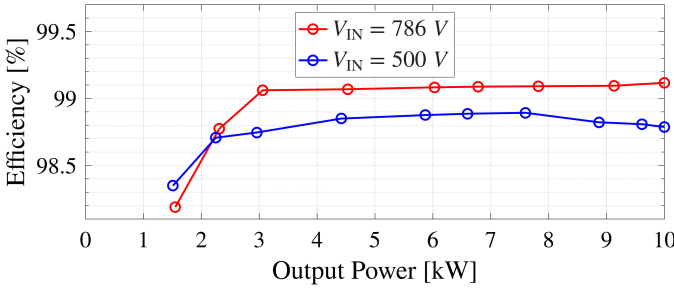
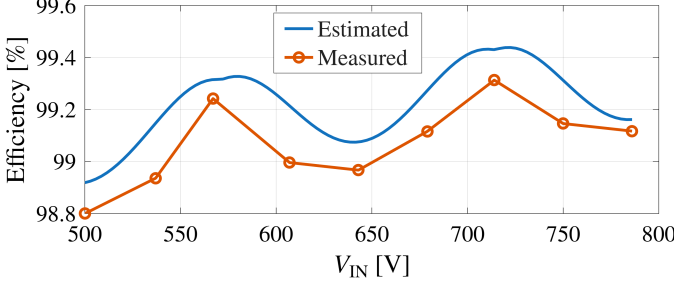


Fig. 6: Breakdown of key components in the overall design. The power stage represents about 49% of the overall hardware mass.



(a) Converter efficiency measurements with input voltages 500 V and 786 V. The output voltage is 1000 V.



(b) Efficiency measurements with varying input voltage at 10 kW output power, and a fixed 1000 V output voltage. The shape of the curve follows the inductor core loss pattern. The local maxima occur at nominal duty ratios where the ripple tends to zero. Inductor losses are estimated using the improved generalized Steinmetz equation (iGSE) [23], [24] based on manufacturer provided data [25].

Fig. 7: Efficiency characterization against output power and input voltage.

duty ratios of the FCML converter where the inductor current ripple tends to zero.

Fig. 9 demonstrates the startup behavior in action for the hardware prototype in this work. In this demonstration, the input to the FCML converter V_{IN} is ramped up to its maximum rating of 786 V. The output of the converter V_{HV} is ramped up to 1000 V. Upon completion of the startup phase, the converter powers a 2.5 kW load at 1000 V.

The flying capacitor voltages, shown in Fig. 9b are measured

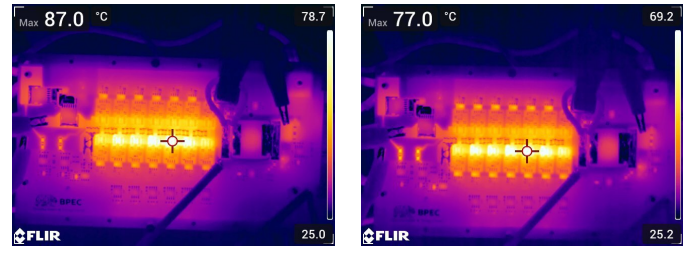
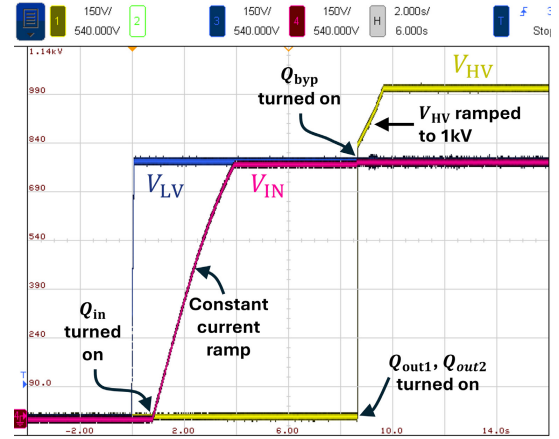
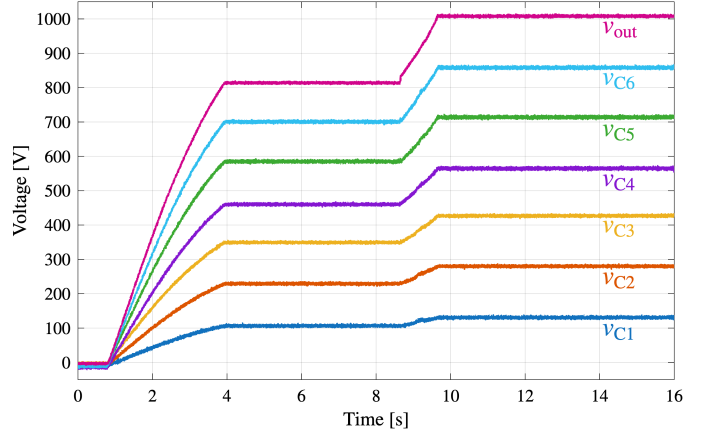


Fig. 8: Thermal results of pulse power testing at 1 kV output voltage and 10 kW output power. The hottest components are the hard-switching low-side switches in the FCML boost converter $s_1 \dots s_7$.



(a) Startup circuit ramps V_{IN} till it reaches $V_{LV} = 786 \text{ V}$ and then ramps V_{HV} till it reaches the target 1000 V. The yellow trace shows V_{HV} , the red trace shows V_{IN} and the blue trace shows the input supply V_{LV} . The time between V_{IN} reaching V_{LV} and the output V_{HV} being ramped up is exaggerated here to illustrate the two phases clearly.



(b) Measured capacitor voltages during startup. Capacitor voltages are fractions of the output voltage, as expected. The test is performed with $v_{IN} = 786 \text{ V}$ and $v_{OUT} = 1000 \text{ V}$ with a 2.5 kW output load.

Fig. 9: Startup testing results.

with high-voltage differential probes on multiple oscilloscopes, and plotted together on a single set of axes via post-processing in MATLAB. The capacitor voltages are equally spaced out at fractions of the output voltage, as required to prevent excessive voltage stress on the transistors in the FCML converter. This is observed at each phase of the startup process: during the startup ramp, when the load is first connected, as well as when the output voltage is ramped up to its final target 1000 V.

Table III
COMPARISON OF DC-DC CONVERTERS FOR AIRCRAFT APPLICATIONS

Specification	[10]	[9]	[8]	This Work
Input Voltage [V]	100–700	480–800	500–720	500–786
Output Voltage [V]	1000	450–720	400	1000
Peak Output Power [kW]	2.5	15	3	10
Peak Efficiency [%]	99.5	98.9	99.5	99.1
Power Stage Density [kW/kg]	28.2	94.3	15.0	103

Table III compares the performance of this work to other state-of-the-art high-voltage DC-DC converters for aircraft applications. This work achieves very high gravimetric power density, particularly considering its output rating of 1000 V.

IV. CONCLUSION

This paper demonstrates the design, optimization, and validation of an 8-level FCML boost converter for electric aircraft power distribution applications. The hardware prototype integrates the necessary embedded controller, as well as circuits for sensing, startup and output disconnect to demonstrate an integrated solution. The prototype achieves 99.1% peak efficiency and 103 kW/kg power-stage density, surpassing both projected aerospace targets identified as long-term goals in recent literature, as well as those of other state-of-the-art works in literature.

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