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INFLUENCE OF LOW TEMPERATURE-GROWN GaAs ON LATERAL THERMAL OXIDATION OF $Al_{0.98}Ga_{0.02}As$

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ABSTRACT

The lateral thermal oxidation process of $Al_{0.98}Ga_{0.02}As$ layers has been studied by transmission electron microscopy. Growing a low-temperature GaAs layer below the $Al_{0.98}Ga_{0.02}As$ has been shown to result in better quality of the oxide/GaAs interfaces compared to reference samples. While the later have As precipitation above and below the oxide layer and roughness and voids at the oxide/GaAs interface, the structures with low-temperature have less As precipitation and develop interfaces without voids. These results are explained in terms of the diffusion of the As toward the low temperature layer. The effect of the addition of a SiO_2 cap layer is also discussed.

INTRODUCTION

Lateral oxidation of $Al_xGa_{1-x}As$ layers is a very attractive technology for the fabrication of isolating oxide layers in optoelectronic devices because of their stability, high resistivity and near planar topology. They have been used in forming self-aligned dielectric layers in the fabrication of semiconductor laser diodes and on vertical cavity surface emitting laser (VCSEL) applications due to the excellent carrier confinement provided by the oxidized layer. These methodcan also be used attention in metal-oxide-semiconductor (MOS) devices. The high quality of the oxide is attributed to the formation of stable AlO(OH) and Al_2O_3 compounds [1]. However some problems related to the excess As created during the process, and weakness of the oxide interfaces, due to structural changes in the $Al_xGa_{1-x}As$ layers, remain unsolved [2,3].

The influence of parameters, such as temperature, layer thickness or composition, on the oxidation process has been the subject of recent studies. In this work we study the structural changes resulting from the inclusion of a low-temperature (LT) GaAs layer. The effects of the presence of a LT-GaAs on the oxidation rates was reported previously [4] indicating a higher oxidation rate for samples including LT-GaAs layers. The influence of the incorporation of a SiO_2 capping layer on the quality of the oxide layer is also discussed.

EXPERIMENTAL

Samples were grown by molecular beam epitaxy (MBE) on a (100) semi-insulating GaAs substrate. Two similar structures (shown in Fig.1) were grown to be oxidized. The only difference between the two types of sample is that in one the central 300 nm thick layer is standard GaAs grown at 580°C whereas in the other sample it is low temperature GaAs, grown at 210°C. The low temperature GaAs was annealed at 600°C for two minutes in-situ and received further annealing during growth of the subsequent layers at 590°C: 100 nm of n-GaAs(Si:10^{18} cm^{-3}), 30 nm of $Al_{0.98}Ga_{0.02}As$, and a capping layer of 35 nm GaAs. In addition thin layers (0.5-10nm) of AlAs were grown on either side of the LT. The reference and the LT samples were processed simultaneously. Mesas were formed in the top of the samples by patterning and

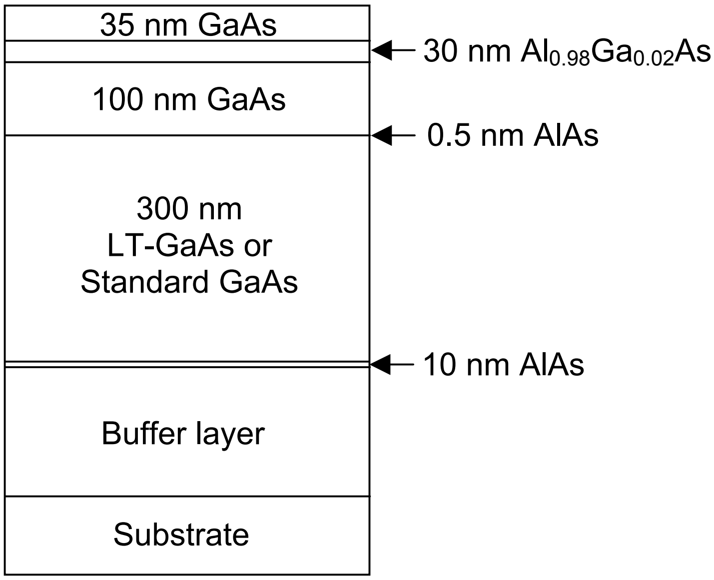

Fig. 1. Sample structure. LT GaAs is substituted by standard GaAs in reference sample.

etching in H_3PO_4:H_2O_2:H_2O (3:3:100). The etch extended past the AlGaAs but not the LT GaAs, exposing only the AlGaAs and part of the n-GaAs sidewalls to the oxidizing ambient. One more sample with LT-GaAs include a PECVD SiO_2 cap. Oxidation was carried out in a water vapor with a N_2 carrier gas, which was bubbled through water heated to 80°C and flowed over the sample, placed in a furnace held at a constant temperature of 450°C. Samples were prepared for transmission electron microscopy (TEM) observation by conventional mechanical polishing and Ar ion milling in a cooled stage until perforation. Topcon 002B and JEOL ARM microscopes were used for these studies.

RESULTS

Annealing of the LT-GaAs layers during the subsequent growth causes the formation of As precipitates that can be recognized as dark spots in Fig. 2. Previous investigations [5,6] show that LT-GaAs as grown is non-stoichiometric, containing excess As in amounts up to 1.5%. The annealing leads to a decrease of the concentration of As_{Ga} antisite defects with simultaneous formation of hexagonal As The average size of the precipitates prior to oxidation is about 4.3 nm, consistent with our previous studies [6]. A slight increase in precipitate average size, about 2%, is detected after oxidation.

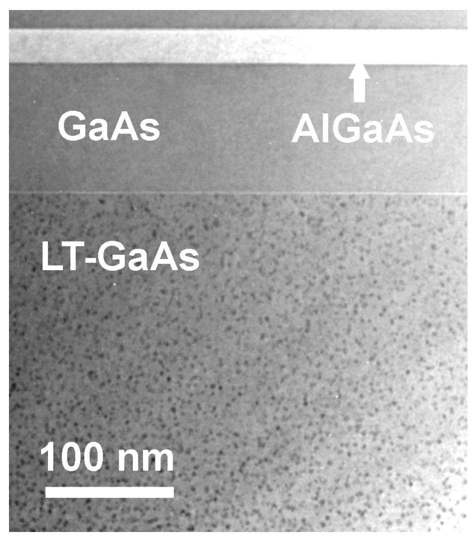

Fig. 2. Top region of the sample containing LT-GaAs. Note the As precipitates in LT layer as dark spots.

After oxidation of samples with a single GaAs capping layer, both standard and LT-GaAs samples developed a homogeneous oxide layer. However in the case of the sample with standard GaAs (Fig. 3.a), As precipitates were formed above and below the original $Al_{0.98}Ga_{0.02}As$ layer as a product of the oxidation. Furthermore, the interface between the oxide and the surrounding GaAs was rough and degraded by the presence of voids that may cause delamination.

It has been proposed [1] that the products of the oxidation reaction of AlAs are mainly Al oxides and hydroxides, and AsH_3. AsH_3 is a material which was assumed to escape to the surface:

$$2AlAs + 3H_2O \rightarrow Al_2O_3 + AsH_3 \quad (1)$$

$$AlAs + 2H_2O \rightarrow AlO(OH) + AsH_3 \quad (2)$$

$$AlAs + 3H_2O \rightarrow Al(OH)_3 + AsH_3 \quad (3)$$

However our results show that a significant amount of As remains in the sample after oxidation suggesting that either arsine decomposes [7]:

$$2AsH_3 \rightarrow 2As + 3H_2 \quad (4)$$

Or that direct formation of As and H_2 takes place by substitution of reaction (4) in (1), (2) and (3).

Conversely, the sample that includes a 300 nm LT GaAs layer, instead of standard GaAs, developed higher quality oxide/GaAs interfaces (Fig. 3.b). Arsenic precipitates in the vicinity of the oxide layer are only occasionally found in this case, and the interfaces were smoother, with no voids along the interfaces. Another interesting feature is the faster oxidation rate of the sample with the LT GaAs layer (21 µm in 10 min.) compared to the standard sample (10 µm in the same time) [4].

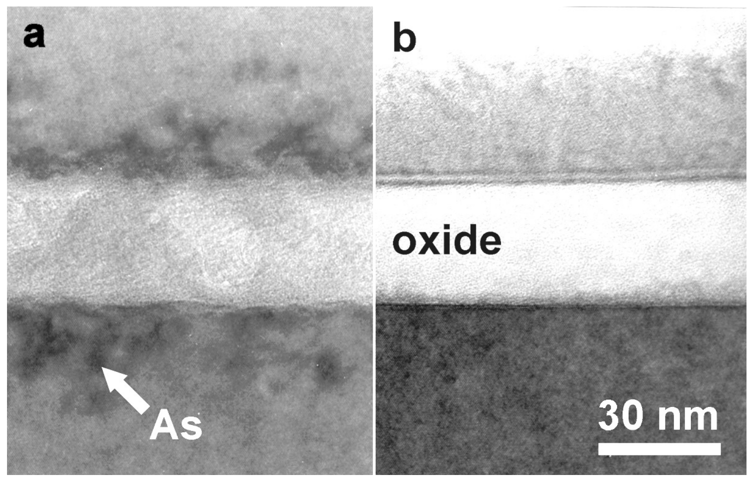

Fig. 3. Oxidized $Al_{0.98}Ga_{0.02}As$ layer in standard sample (a) and in sample with LT-GaAs (b). Arsenic segregated from the oxide and voids are found at the interfaces in (a). Interface quality is greatly improved in (b).

It is not yet clear what is the reason for reduced As precipitation near the oxidized layer when an underlying layer of annealed LT-GaAs is present. One possible explanation is that the presence of As precipitates in the annealed low-temperature layer acts as a sink for excess As so that near the oxidized layer the excess As concentration never reaches the critical value for precipitate nucleation. Another factor that could play a role is introduction of some excess Ga vacancies during annealing at of the low temperature GaAs into the layers above the low temperature layer which could facilitate As diffusion away from the oxide layer. Migration of excess As away from the oxidation front to the As precipitates in the low temperature layer is also consistent with the observed small increase in size of the As precipitates after the oxidation treatment.

Finally, we present the results for the sample that includes a top SiO_2 capping layer. The micrographs (Fig. 4) show again sharp interfaces and clean from As, like in the case that no capping layer is included.

Future work involves the capping of the sample with Si_3N_4 which is known to be non-permeable to As, acting as a barrier to outdiffusion. This will allow us to assess whether the arsenic accumulations diffuse mostly towards the LT-layer or leave the sample through the surface.

CONCLUSIONS

The influence of a low-temperature-grown GaAs layer, on the oxidation behavior of an $Al_{0.98}Ga_{0.02}As$ layer, has been investigated by TEM observations. Results show an improvement of the quality of the oxide/GaAs interfaces when a LT GaAs layer is included.

The exact reason for this improvement is not yet clear but it appears that the presence of As precipitates in the annealed low temperature layer may be acting as a sink for As thus reducing its build up near the oxidation front.

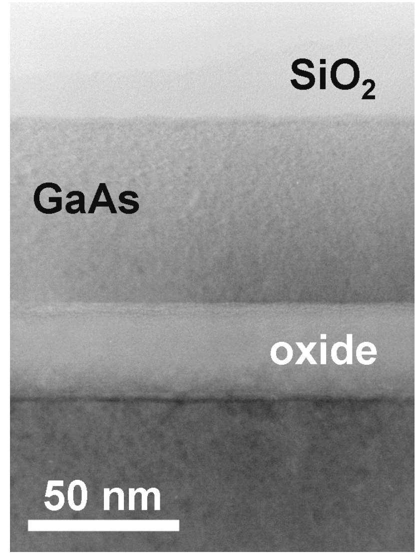

Fig. 4. Sample including a SiO_2 capping layers and LT GaAs. It exhibits clean, sharp oxide/GaAs interfaces.

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