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Analysis and Operation of Flying Capacitor Multilevel Converters: Single-Phase
Applications and Fundamental Electromagnetic Interference Scaling

By

Francesca Rose Giardine

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Robert Pilawa-Podgurski, Chair
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Professor Katherine A. Kim

Spring 2026

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Abstract

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Professor Robert Pilawa-Podgurski, Chair

Continuous advancements in power electronics are essential to meet the demands of an increasingly electrified future. This dissertation explores the application and operation of a multilevel power converter topology in two parts. In the first part, the flying capacitor multilevel (FCML) converter is assessed as a promising topology for high-density hardware designs in applications ranging from renewable grid integration to electrified transportation. In this part, high-density prototypes utilizing gallium nitride switching devices are described alongside modulation techniques used to increase efficiency. In the second part of this dissertation, conducted electromagnetic interference (EMI) is explored for the FCML converter. A discussion of differential-mode EMI is provided, and an analytical model for common-mode EMI is presented and detailed for the FCML converter. Using this hardware-validated common-mode EMI model, the first evidence of the FCML converter having intrinsically better conducted EMI than a conventional two-level solution is identified. Through the parallel efforts presented in this dissertation, the FCML converter is shown to be a superior topological alternative to conventional power converter topologies for a broad range of application spaces.

To Jessica N. Keast

With respect and admiration in equal parts.

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This thesis is dedicated to Jessica Keast, who will become my wife later this month. During the first Christmas we celebrated, we exchanged books. Inscribed in the front cover of the one I gave Jessica, was “To Jessica, with respect and admiration in equal parts.” After further reflection, this inscription is one that you give to someone you either like a lot, or someone you’ve worked with for a long time at their retirement party. I’ve reused this inscription here because, firstly, in choosing a person to create a life with, respect is a fundamental requirement. My respect for her never stops growing. I never fail to be amazed by her courage. From a cross-country move, to facing her fear of heights to hike to new ones, she reminds me constantly that it is always better to try. Secondly, I admire Jessica immensely. She is a fiercely intelligent woman who continuously challenges me to be better than I was yesterday. She is always ready with a question, a joke, and a laugh. Our home is filled with light and joy. There is no one I would rather go on an adventure with. Jessica, this one is for you.

Chapter 1

Introduction: Multilevel Power Converters to Meet the Power Challenges of Today

1.1 Background

Power electronics are used to transform voltages and currents from one form or magnitude to another. These circuits employ a combination of semiconductor switching devices and passive energy storage elements to precisely convert electrical energy for a specified end use. Power electronics enable households to not only draw power from the grid to use appliances and telecommunication devices [1] but also enable households to participate in a more sustainable future. With the development of new forms of residential-scale renewable energy generation and at-home electric vehicle charging, household engagement with the grid is changing [2, 3]. Power converters are required as an interface between these renewable resources and dynamic loads, to convert between the direct current (dc) present at a battery input or solar panel output and the alternating current (ac) present at the grid.

New and dynamic large-scale loads such as large-scale electric vehicle charging [4, 5] and power-hungry data centers are creating opportunities for advancement in power electronics. It is anticipated that data centers will account for up to 12% of electricity demand in the United States by 2028 [6]. In these large-scale systems, power is lost in a cascading effect as it moves through each stage, necessitating continuous innovation in power electronic architectures.

This dissertation considers power converters as pieces of larger systems. Fig. 1.1 highlights these systems conceptually, as well as some of the objectives that may be considered in the development of a converter for a given application. In this dissertation, a multilevel power converter topology is explored in pursuit of high efficiency and low volumetric sizes to enable modularity in different system implementations. Emphasis is placed on both the residential grid-connection application space and on innovations in electrified transporta-

tion. In both these systems, and in any system containing electronics, one concern for power converter implementation is conducted electromagnetic interference (EMI). Conducted EMI describes the frequency content present in the voltages and currents at the converter input or output. Because EMI can damage connected electronics and equipment, it is a stringently regulated phenomenon [7–11]. This dissertation explores conducted EMI in the selected multilevel power converter topology as a way to encourage more widespread adoption of the converter and as an acknowledgment that power conversion is one piece of a larger whole.

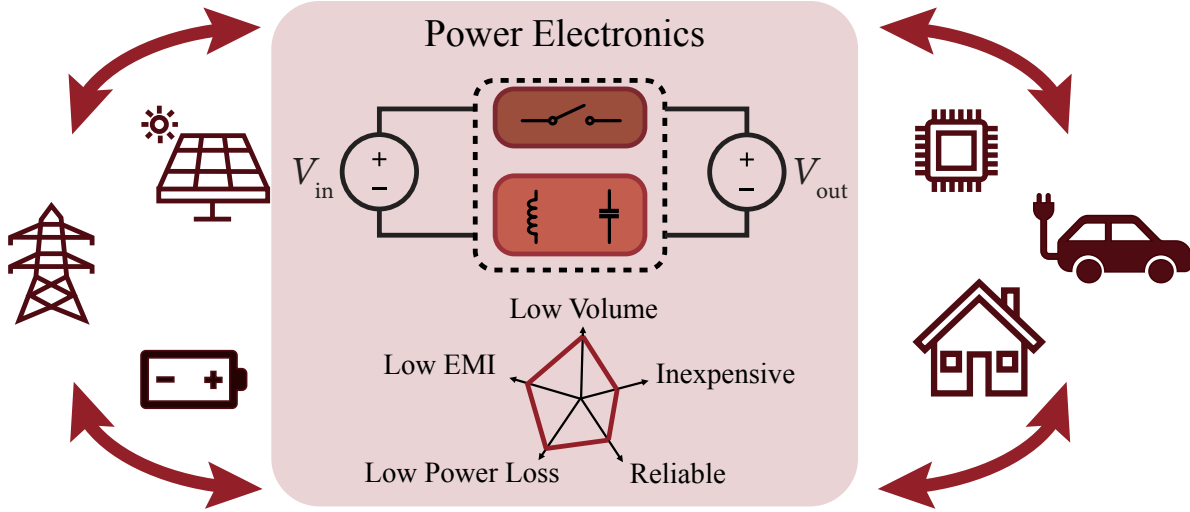


Figure 1.1: Conceptual diagram outlining the role that power electronics plays in electrifying a wide range of systems, as well as some considerations and objectives for power converter development.

1.2 Multilevel Power Converters

In circuit applications where both high efficiency and high power density are desirable, power converters are limited by the choices of appropriately rated state-of-the-art semiconductor switches and energy storage elements. A buck converter, used to convert from a higher voltage to a lower voltage, is shown in Fig. 1.2. The complementary gating signals are also shown for one switching period T_{sw} , as are the switch-node voltage (v_{sw}) and the inductor current (i_L). The buck converter produces an output voltage that is a fraction D of the input voltage V_{in} . In a buck converter, each semiconductor device is rated to block the full input voltage. The inductor, which handles the energy storage burden for the converter, must be rated to conduct both the average current and the current ripple imposed by the volt-seconds across the inductor.

It is possible to achieve the same conversion ratio as the buck converter using other circuit topologies. To improve efficiency and power density over the conventional buck converter, it

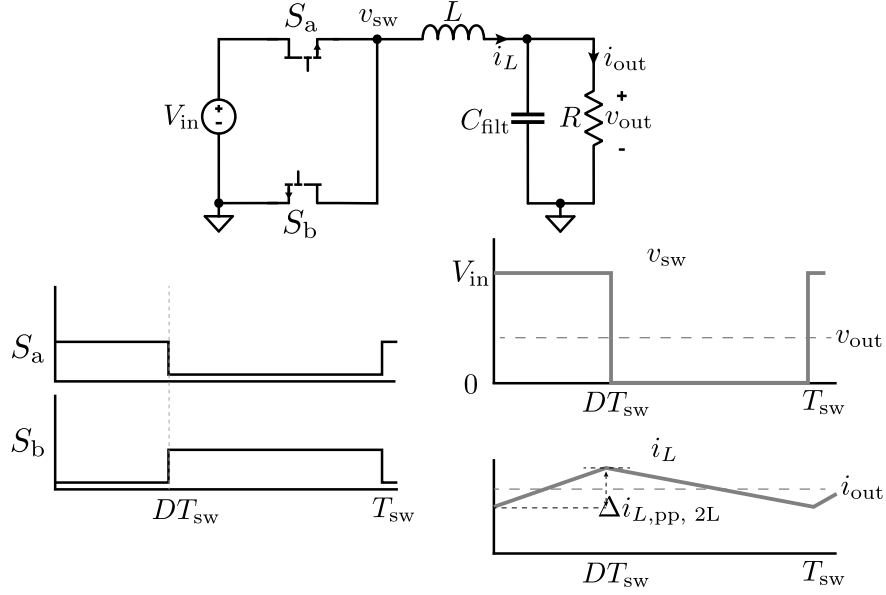


Figure 1.2: 2-level buck converter.

Figure 1.3: Schematic drawing of a buck converter gating signals, the switch-node voltage waveforms, and inductor current.

is worth considering how energy storage elements (inductors and capacitors) and semiconductor devices scale. Comparing these converter building blocks enables the evaluation of topological alternatives.

In terms of converter power density, the inductor is typically the largest physical element in a buck converter. In general, favorable volumetric scaling of magnetic components is difficult [12]. As inductor size is reduced achievable efficiencies become quite limited, which necessitates a “precipitous” reduction in achievable power density. A recent survey of commercially available capacitors and inductors revealed that the most volumetrically energy-dense capacitors are roughly $1000\times$ more energy-dense than the most energy-dense inductors [13]. Thus, implementing circuit topologies that place a larger energy conditioning burden on capacitors should theoretically improve system volume.

In addition, it has been shown that lower voltage semiconductor devices have more favorable loss scaling than high-voltage devices [14]. In fact, using a set of series-connected low-voltage devices in lieu of one high-voltage device has favorable loss scaling in a power converter. This finding incentivizes the use of circuit topologies that have reduced switch blocking voltages to improve efficiency.

The combination of passive component and semiconductor scaling trends motivates the use of converters that place more energy storage burden in capacitors than inductors and that utilize low-voltage semiconductor devices. One converter that merges these objectives

well is the flying capacitor multilevel (FCML) converter. The FCML converter is comprised of a switched-capacitor network and an LC filter [15], and it may also be classified as a hybrid switched-capacitor converter [16]. Hybrid switched-capacitor converters are a class of power converters with a switched-capacitor stage and an inductive element that enables soft charging of the capacitors.

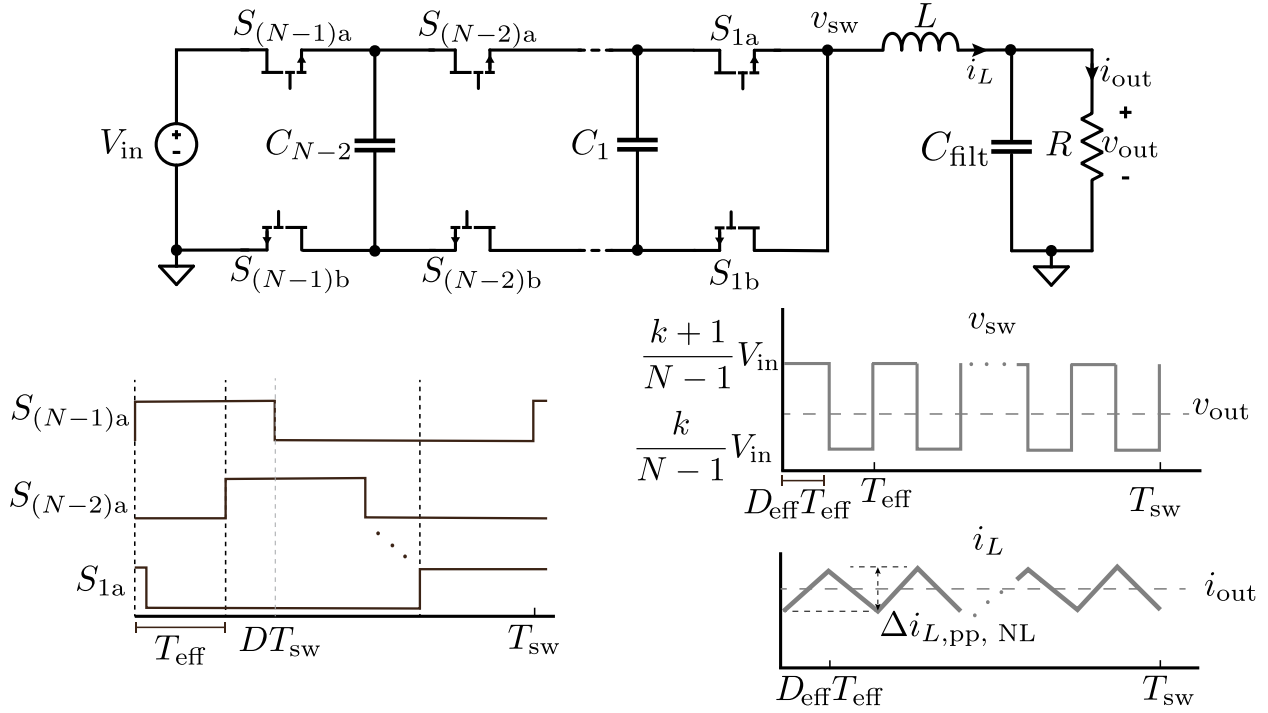


Figure 1.4: Schematic drawing of an FCML converter with gating signals, switch-node voltage waveforms, and inductor current.

The general N -level FCML converter is shown in Fig. 1.4. The converter has $N - 1$ switch pairs and $N - 2$ flying capacitors. The gate signals for the high-side switches are shown in Fig. 1.4 and highlight that each switch pair is circularly phase shifted from the preceding switch pair. The switch pairs are gated with signals generated by carriers that are separated by $\frac{2\pi}{N-1}$ radians, which is referred to here as phase-shifted pulse width modulation (PS-PWM) [17]. In the time domain, these phase shifts result in an effective switch-node period that is a fraction of the switching period

$$T_{eff} = \frac{1}{N-1} T_{sw}. \quad (1.1)$$

In the frequency domain, PS-PWM operation of the FCML converter results in a fundamental switch-node frequency

$$f_{eff} = (N-1)f_{sw}. \quad (1.2)$$

The switch-node voltage, v_{sw} , is also shown in Fig. 1.4. The multiplied effective frequency is highlighted here, as well as the fractional switch-node voltage values. The switch node alternates between $k V_{in}/(N - 1)$ and $(k + 1) V_{in}/(N - 1)$ where

$$k = \lfloor (N - 1)D \rfloor, \quad k = [0, 1, 2 \dots N - 2], \quad (1.3)$$

and $\lfloor \cdot \rfloor$ is the floor function [18].

The fractional switch-node voltage and effective frequency work together to substantially reduce the volt-seconds across the inductor. Compared to the inductor current ripple for the buck, or “2-level” converter, which is given by

$$\Delta i_{L,pp, 2L} = \frac{V_{in} \cdot D(1 - D)}{f_{sw}L}, \quad (1.4)$$

the N-level FCML converter has an inductor current ripple given by

$$\Delta i_{L,pp, NL} = \frac{V_{in} \cdot D_{eff}(1 - D_{eff})}{(N - 1)^2 f_{sw}L}, \quad (1.5)$$

where $D_{eff} = (N - 1)D - \lfloor (N - 1)D \rfloor$.

For the same inductor current ripple as the buck converter, the FCML converter reduces the required inductance L by a factor of $(N - 1)^2$, which is highly effective at miniaturizing this generally high-volume magnetic component.

The FCML converter benefits from having a cellular structure characterized by equal blocking voltages across each semiconductor device. This enables straightforward and symmetric printed circuit board design. Combined with the reduced filter inductance, the converter is a competitive choice in many application spaces that prioritize power density and efficiency [19–23].

This dissertation explores how the FCML topology enables high efficiencies and power densities, using hardware results for dc-ac applications. After establishing the circuit topology as a competitive alternative to conventional solutions, this dissertation tackles fundamental conducted electromagnetic interference behavior for the FCML converter. Both modeling and EMI measurements enable the conclusion that the FCML converter has superior EMI when compared to the 2-level solution.

1.3 Organization of Dissertation

This is a dissertation in two parts. In the first part, applications of the flying capacitor multilevel converter are examined with a particular emphasis on residential grid connection and electrified transportation. Chapters 2-5 detail the use of the FCML converter in dc-ac/ac-dc converters for residential grid ties, as well as an isolated FCML converter implementation for 800 V EV systems.

The second part of this dissertation, encouraged by the power densities and efficiencies observed in the first part of this dissertation, undertakes an exploration of electromagnetic interference generated by the FCML topology. Chapters 6-9 detail differential-mode EMI and common-mode EMI for the FCML converter. It is shown here that the FCML converter has superior EMI to the conventional 2-level buck converter despite the added complexity of more semiconductor switching cells.

Each chapter is described briefly in the following subsections as a guide for the reader.

Chapter 2: A Hybrid Switched-Capacitor Microinverter

Widespread adoption of solar energy at the residential scale is creating opportunity in the advancement of dc-ac power converters. This chapter details the development of a two-stage microinverter architecture. Each of the conversion stages are comprised of hybrid-switched capacitor converter topologies. The boost stage, which is a dc-dc resonant hybrid-switched capacitor converter, also has an intrinsic startup capability that can be used to energize the system. The inverting stage is made up of a flying capacitor multilevel inverter. The use of a two-stage solution also enables the utilization of an energy-dense capacitor to buffer the 120 Hz ripple at the dc link separating the boost and the inverter stages. Hardware results are provided and highlight the possibility of more power-dense conversion in this application space.

Chapter 3: Variable Switching Frequency Control for DC-AC FCML Converters to Improve Efficiency

In Chapter 2, it was observed that the flying capacitor multilevel inverter suffered efficiency penalties as a result of hard-switching losses. The need for a cleanly filtered sinusoidal output voltage in an inverter incentivizes faster switching speeds, but these losses are worsened by fast switching frequencies. In this chapter, a variable switching frequency scheme is proposed to leverage special properties of the FCML converter to reduce switching frequency in regions of the ac line cycle where inductor current ripple is intrinsically lower. This scheme enables substantial reductions in hard switching losses and subsequent improvements in efficiency. A safe set of operating conditions are derived, and the scheme can be implemented in a conventional microcontroller unit.

Chapter 4: A Totem-Pole DC-AC FCML Converter for Improved Power Density

While performance improvements can be enabled through modulation and control, as detailed in Chapter 3, this chapter highlights a topological change to the dc-ac converter architecture. Here, a totem-pole topology is applied to the FCML converter. The 3kW converter prototype developed by Yayun Zhao, which is demonstrated in this chapter, has

only two grid-frequency switches used to create an ac voltage, enabling high power density and efficiency.

Chapter 5: Applications of FCML Converters: Meeting Future Power Conversion Challenges

In this chapter, the FCML converter is merged with a dual active bridge converter to convert between 800 V and 53.3 V for electrified transportation applications. The GaN-based hardware prototype was collaboratively co-designed with Sahana Krishnan, and it features a 6-level FCML inverter, a planar transformer, and a rectifier with parallelized switches.

Chapter 6: An Overview of Differential-Mode Electromagnetic Interference in FCML Converters

This chapter provides an introduction to conducted electromagnetic interference and measurement before detailing the generation of differential-mode EMI in the FCML converter. Notably, some nuances regarding output-side differential-mode EMI in the FCML converter are explored. This analysis is enabled through the use of a model of the FCML converter that incorporates flying capacitor voltage ripple. We show and formalize that flying capacitor voltage ripple and imbalance create unexpected harmonics at the switching frequency.

Chapter 7: Improvements to Differential-Mode EMI in DC-AC FCML Converters

The variable switching frequency scheme presented in Chapter 3 has additional benefits beyond the improvement in converter efficiency. In this chapter, the switching frequency scheme is adapted as a spread-spectrum frequency modulation technique specific to the FCML converter. The variable frequency scheme is applied to an 8-level converter, and results in a substantial reduction in EMI peaks at both the input and output of the converter.

Chapter 8: Modeling Common-Mode EMI in the FCML Converter

Common-mode EMI, which results from unwanted parasitic capacitances throughout a converter, can be inherently challenging to characterize. In this chapter, a general model of CM EMI for the FCML converter is developed. Using a 6-level prototype, the required level of model detail is verified in both the time and frequency domains. Excellent matching highlights the feasibility of using this model to compute EMI signatures for the FCML converter.

Chapter 9: On the Scaling of Common-Mode EMI in the FCML Converter

Using the model presented in Chapter 8, it is possible to explore how EMI scales across FCML converter level counts. Simplifying assumptions enable the rapid computation of the fundamental component magnitude, and semiconductor device scaling is used here to compare among FCML converter level counts. This chapter shows that the FCML converter has improved CM EMI compared to a conventional 2-level buck converter through the use of smaller semiconductor die areas.

Chapter 10: Concluding Remarks

At the end of this dissertation, this chapter provides a brief overview of the full body of work and discusses future research directions.

Part I

Applications of Flying Capacitor Multilevel Converters: Residential Single-Phase Power Conversion and Electrified Transportation

Chapter 2

A Hybrid Switched-Capacitor Microinverter

2.1 Introduction

Executive Summary

This chapter details the development of a fully hybrid switched-capacitor microinverter. The two-stage solution enables each stage to be independently designed for optimal performance, and this is used as a way to explore the benefits of placing the dc-link capacitor at a high-voltage intermediate bus. The step-up stage is a multi-resonant hybrid switched-capacitor converter capable of soft-switching. Furthermore, this topology has an intrinsic soft-start capability that enables system-level startup. The inverter stage is realized with a flying capacitor multilevel converter, which enables the use of lower-voltage GaN switching devices. The power stages achieve a high volumetric power density and demonstrate the feasibility of a hybrid switched-capacitor design in the microinverter application space.

This chapter is based on collaborative work appearing in both [24] and [25].

Widespread adoption of renewable energy systems at the residential scale has increased the market for inverters to convert the low-voltage dc output of solar photovoltaic (PV) modules to the ac voltage required by the distribution grid [26, 27]. Microinverters are conventionally classified as being either two-stage or single-stage. The general architectures for each are shown in Fig. 2.1. A two-stage solution has a distinct boost conversion stage from the output voltage of a solar panel, an intermediate high-voltage dc bus, and an inverter stage [2, 28]. In contrast, a single-stage solution does not have a distinct intermediate dc-bus voltage; instead, the twice-line-frequency buffer capacitance is placed at the low-voltage PV input [29]. Single-stage solutions typically benefit from high efficiencies. In this work, we consider the development of a two-stage solution with an emphasis on developing

volumetrically dense power stage solutions. The two-stage architecture enables convenient placement of the dc-link capacitor used to buffer the twice-line frequency ripple at the high voltage (HV) bus. The placement of the buffer at the higher voltage dc bus enables a significant reduction in dc link capacitor volume, as discrete options for electrolytic capacitors offer the highest energy densities around 400 V [30, 31].

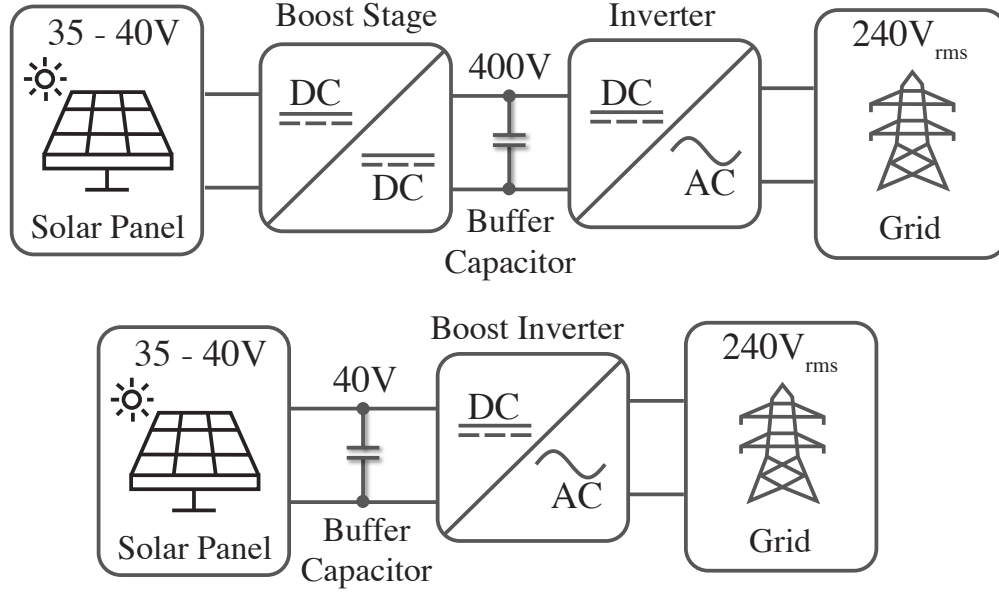


Figure 2.1: Two-stage (top) and single-stage (bottom) microinverter architectures. In this work we consider a two-stage solution.

A two-stage microinverter architecture allows for a decoupled design strategy, where the dc-dc and dc-ac stages are optimized independently. Hybrid switched-capacitor [16] and multilevel converter topologies [15] are seeing increased adoption [32, 33], as they allow for significant reduction in passive component volume by utilizing energy-dense capacitors [13, 34] and increased efficiency via the use of high figure-of-merit low-voltage switches [14, 19, 35–37]. This work proposes a novel two-stage architecture in which a fixed-ratio 1-to-10 cascaded series-parallel (CaSP) converter steps up a 35 – 40 V photovoltaic (PV) module input to a 350 – 400 V unregulated intermediate bus, which feeds a flying capacitor multilevel (FCML) inverter with a 240 V_{rms} ac output [25]. The CaSP converter is a multi-resonant switched-capacitor converter (ReSC) that has been used in the low-voltage (LV) step-down space [38–40]. Its competitively low passive volume, reduced component count compared to other hybrid switched-capacitor converters, and ability to achieve zero current switching (ZCS) make it an attractive option for a dc-dc step-up stage, particularly at high conversion ratios [41]. However, ensuring that the CaSP converter can be successfully used as a fixed-ratio step-up input to an inverter is essential in validating its potential for adoption in renewable energy applications.

An FCML inverter is implemented for the second microinverter stage, as this topology has demonstrated competitive efficiencies and low volumes in a wide array of applications [19, 20, 23, 32, 35, 42]. In this two-stage conversion scheme, the FCML inverter produces a well-filtered rectified sine-wave output of the desired ac-side voltage magnitude, which is then converted to a full-wave ac waveform through an H-bridge unfolded. Because the FCML converter is a switched-capacitor network merged with an inductive energy storage element, it is also considered to be a hybrid switched-capacitor converter. Combined, the two stages form a fully hybrid switched-capacitor converter architecture, making use of multilevel hybrid switched-capacitor topologies from input to output.

2.2 System Architecture

An illustration of the system architecture with detailed labeling of the dc blocking voltages of each switch and the dc voltages across the capacitors is provided in Fig. 2.2. The first converter in the system is the 1-to-10 CaSP stage that steps up the low 35–40 V input voltage to a 350 – 400 V dc voltage. A buffer capacitor (C_{buff}) is placed at the high-voltage dc bus to provide twice-line frequency buffering required for dc-ac operation to ensure that the ac ripple induced by the inverter is decoupled from the dc-side input. The 6-level FCML converter converts the high dc voltage at the intermediate bus to a 240 V_{rms} output at the grid frequency.

CaSP Boost Stage

The CaSP converter is a multi-resonant hybrid-switched capacitor topology, meaning that during a given switching period, there are LC tanks with different resonant frequencies that are formed across sub-period intervals. The CaSP converter was selected over other hybrid-switched capacitor topologies as it enables very low passive volume with relatively low switch stresses [25]. Compared to conventional two-phase resonant converters, the multi-phase control scheme within each switching period enables extreme conversion ratios with reduced active and passive components [39]. In a given switching period, the CaSP converter has three separate sub-period intervals that can be modeled as separate LC tanks [38]. In these LC tanks, capacitors $C_{1-4, \text{CaSP}}$, as labeled in Fig. 2.2, are defined by a nominal capacitance C_o , and capacitor $C_{5, \text{CaSP}}$ is obtained as $C_{5, \text{CaSP}} = \frac{C_o}{12}$ for the 1-to-10 CaSP converter. The three sub-period circuit models are shown in Fig. 2.3, as is the resulting inductor current.

In [25, 41], each sub-period's duration is derived according to the equivalent LC tank impedance such that ZCS is achieved in the converter. In this multi-resonant operation, a fraction of the switches will operate with ZVS. Even when the CaSP converter is operated above its resonant frequency, some switches can still achieve ZVS [38]. The resonant

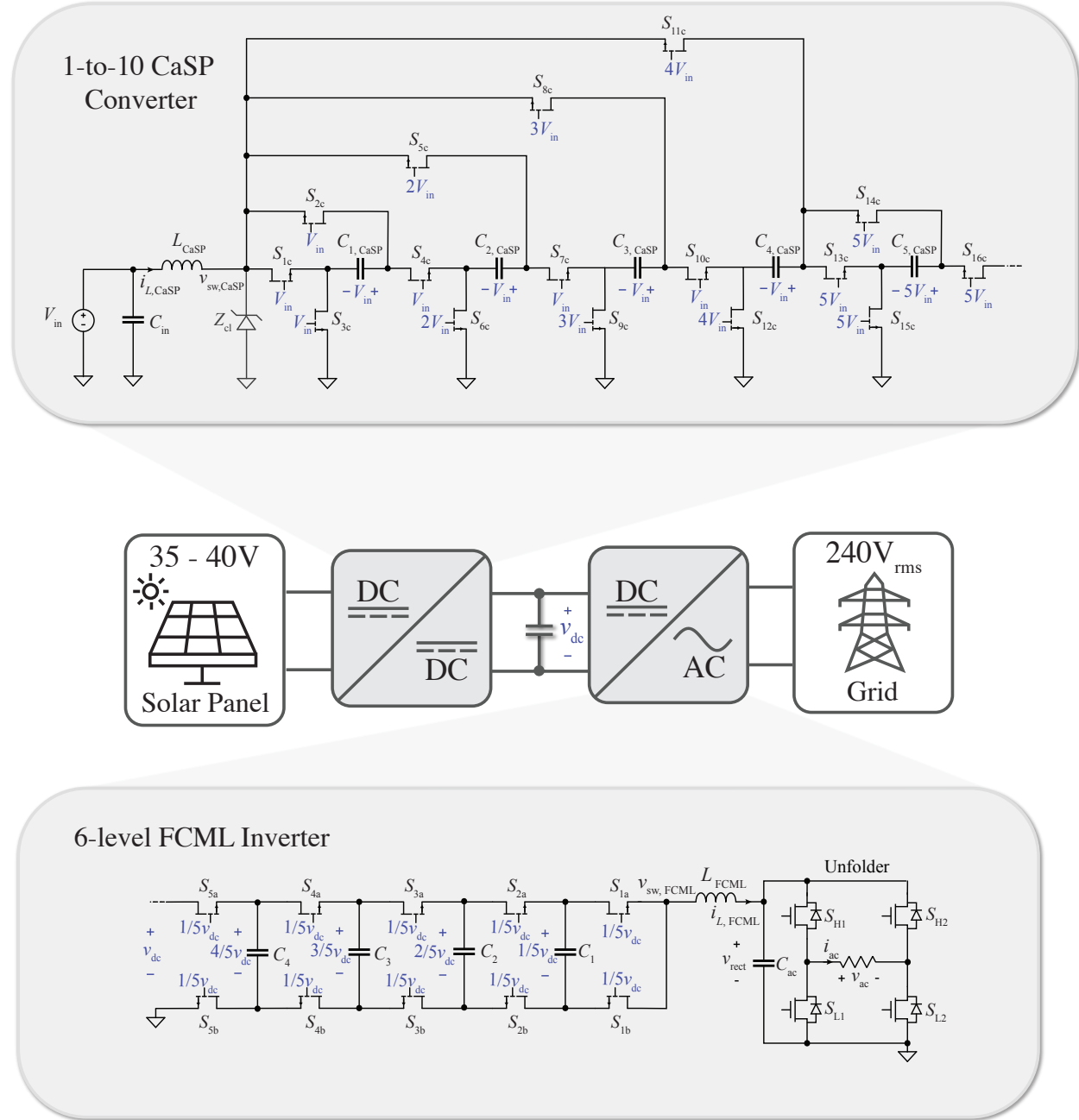


Figure 2.2: Schematic drawing of the proposed fully hybrid switched-capacitor architecture for converting LV PV power to grid power. A CaSP converter is used to step up the LV dc input to the HV dc bus, where the dc-link capacitor buffers the twice-line frequency power pulsation in the inverting stage. The second stage is composed of a 6-level FCML converter with an unfoldr.

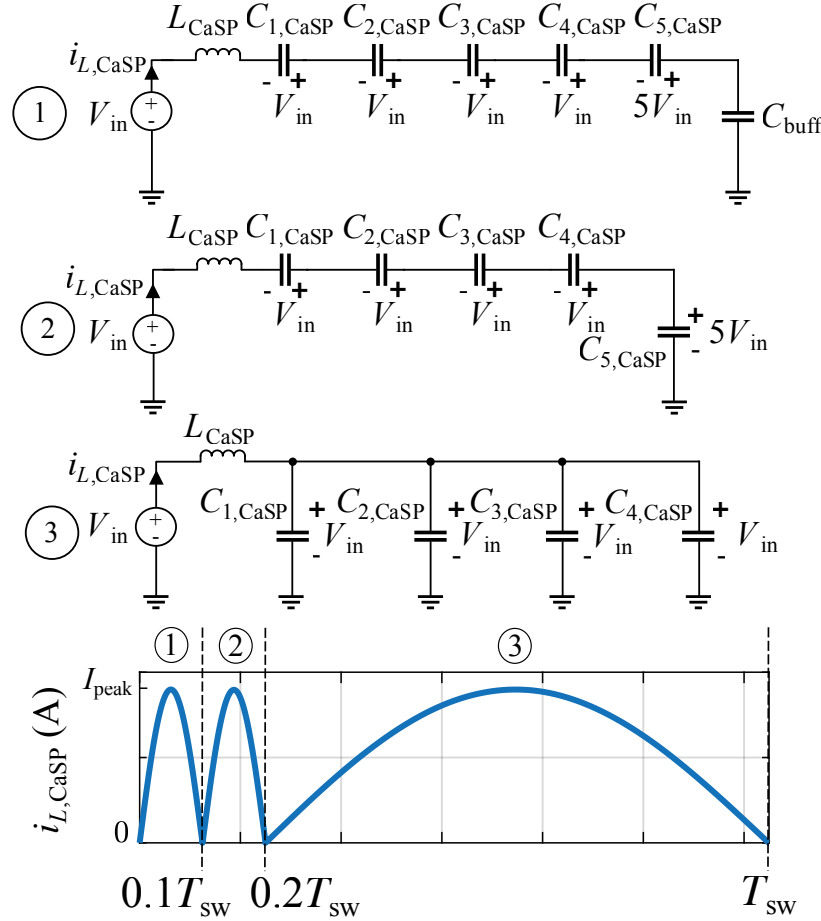


Figure 2.3: The three sub-period circuit models of the CaSP converter and the corresponding inductor current $i_{L,\text{CaSP}}$ for each stage over the period T_{sw} . Figure credit: Kelly Fernandez.

frequency for each sub-period is given by (2.1) and (2.2)

$$\omega_{\text{res},1} = \omega_{\text{res},2} = \frac{1}{\sqrt{L_{\text{CaSP}} \frac{C_o C_{5,\text{CaSP}}}{C_o + 4C_{5,\text{CaSP}}}}} = \frac{4}{\sqrt{L_{\text{CaSP}} C_o}} \quad (2.1)$$

$$\omega_{\text{res},3} = \frac{1}{\sqrt{4L_{\text{CaSP}} C_o}}. \quad (2.2)$$

The conducting switches of the CaSP converter during sub-periods ① and ② must carry inductor current $i_{L,\text{CaSP}}$, while during sub-period ③ the conducting switches are in parallel and must carry $\frac{i_{L,\text{CaSP}}}{4}$. The average value of the CaSP inductor current $i_{L,\text{CaSP}}$ is the same for each of the three sub-periods, which makes it possible to derive the peak inductor current

based on the input power and voltage, which is described by (2.3).

$$I_{\text{peak}} = \frac{\pi}{2} \cdot \frac{P_{\text{in}}}{V_{\text{in}}} \quad (2.3)$$

At high power, the peak value of the resonant current I_{peak} becomes large, which requires sufficient filter capacitance at the input and output buses of the CaSP converter to mitigate current ripple at the switching frequency.

In non-ZCS operation, is possible for the inductor current in the CaSP stage, $i_{L, \text{CaSP}}$, to not be fully discharged during a switching transition. When the inductor current is not fully discharged, current may conduct through the switch body diodes via the parasitic output capacitances of the switches. These diodes create a direct path to the HV dc bus from the switched node of the CaSP $v_{\text{sw, CaSP}}$, causing the switches to be over-voltaged. To mitigate high-voltage exposure to the FETs and protect the converter, a Zener diode Z_{cl} may be placed on the switched node of the CaSP stage to provide a low-impedance path for the current $i_{L, \text{CaSP}}$ to flow. This diode is shown in gray in Fig. 2.1. Additionally, this diode clamps the switched-node voltage to a value that does not exceed the rated blocking voltage of the switches [25].

CaSP Stage Enabled Startup

The CaSP stage has an innate soft-start functionality that eliminates the necessity for any additional startup circuitry. The switches of the CaSP step-up converter are rated to block a minimum of V_{in} so that when the full dc voltage is instantaneously applied to the converter while the system is not fully energized, the FETs will not experience an overvoltage condition. Under regular switching operation, in part due to the resonant nature of the CaSP converter, the charge flow in each sub-period enables a gradual ramp-up of the full output voltage. During this time, the FCML inverter will also experience an input voltage ramp. Fig. 2.4 shows the simulated direct application of $V_{\text{in}} = 40 \text{ V}$, with a terminal power level of $P_{\text{in}} = 400 \text{ W}$. The flying capacitors of the CaSP stage ramp up to their rated voltages on a time scale in the tens of milliseconds, resulting in the desired output voltage of $10 \cdot V_{\text{in}}$.

Buffer Capacitor Selection

It is worth noting that the buffer capacitor for the two-stage system is placed on the high-voltage dc bus that separates the CaSP stage from the FCML inverting stage. The buffer is sized to sufficiently store and release the energy associated with the rated twice-line frequency ($f_{2\text{Grid}} = 2f_{\text{Grid}}$) input power to the inverter stage [43]. The required capacitance for the buffer can be calculated using (2.4),

$$C_{\text{buff}} = \frac{P_{\text{in}}}{2\pi f_{\text{Grid}} \cdot v_{\text{dc}} \cdot \Delta v_{\text{dc}}}, \quad (2.4)$$

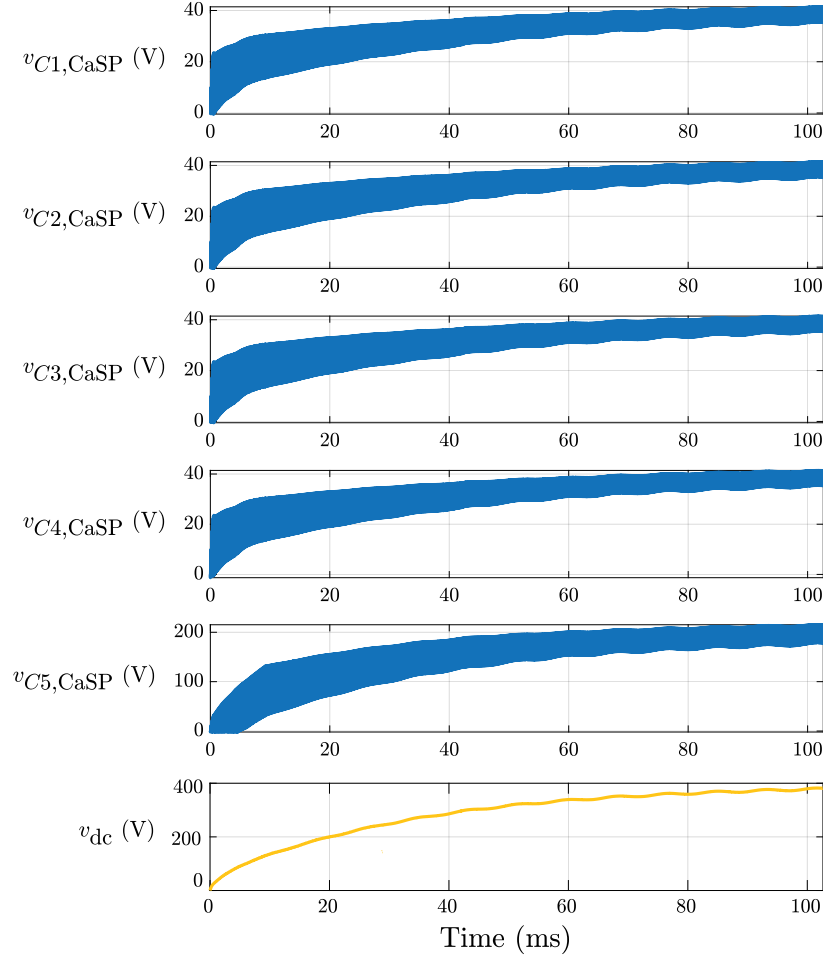


Figure 2.4: Simulated CaSP converter flying capacitor ($C_{1, \text{CaSP}} - C_{5, \text{CaSP}}$) voltage waveforms during startup from $V_{\text{in}} = 0$ V to 40 V at a rated power of $P_{\text{in}} = 400$ W. Figure credit: Kelly Fernandez.

where v_{dc} describes the HV dc-voltage bias the capacitor must be rated for and Δv_{dc} captures peak-to-peak voltage ripple. The placement of the buffer capacitance at the HV bus enables the use of the most energy-dense aluminum electrolytic capacitors available.

The selected capacitor used in the hardware described in Section 2.3 is rated for 500 V and is $2.5\times$ more energy dense than the most energy dense capacitor at 50 V. Fig. 2.5 shows the selected capacitor on a plot of volumetric energy densities at each voltage compared to the other aluminum electrolytic capacitors available on Digikey [13, 30]. For a ripple ratio of $\alpha = \Delta v_{\text{dc}}/v_{\text{dc}} = 0.025$, we can compare the required capacitance for a two-stage and single-stage solution, where the dc voltages are 40 V and 400 V respectively. In Table 2.1, we showcase this comparison and highlight the substantial volumetric benefit of moving the capacitor to the HV intermediate bus. The 50 V Nichicon capacitor is a very energy-

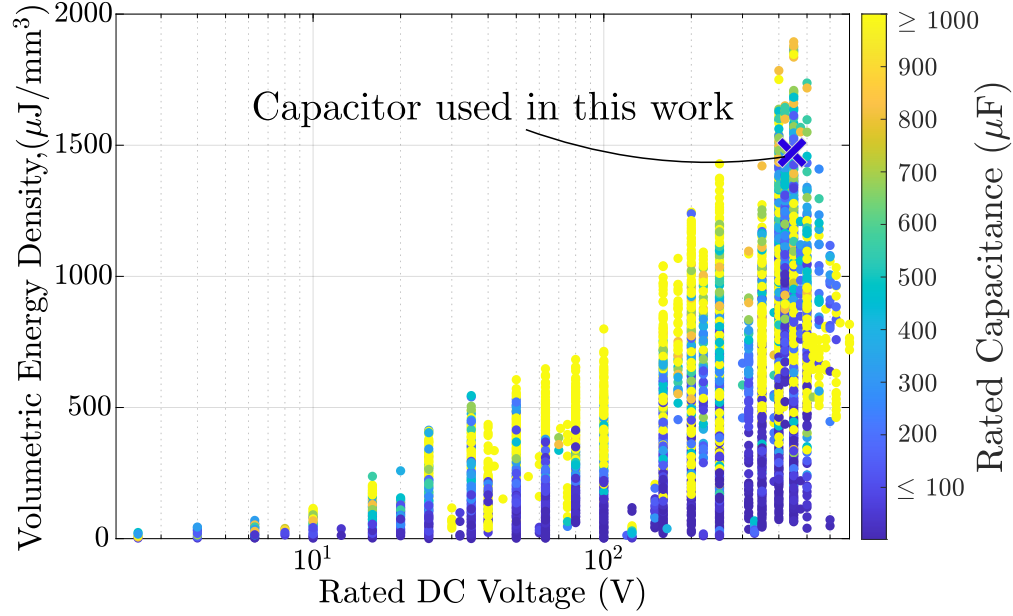


Figure 2.5: Plot of volumetric energy densities of commercially available aluminum electrolytic capacitors compared to their rated voltage. The data and analysis methods used to generate this plot are from [13, 30].

Table 2.1: Example buffer capacitance comparison of single-stage and double-stage designs.

Parameter	Single-stage	Double-stage
Required Capacitance	$> 33.2 \text{ mF}$	$> 332 \text{ } \mu\text{F}$
Capacitance Voltage Rating	$> 40 \text{ V}$	$> 400 \text{ V}$
Manufacturer	Nichicon	Rubycon
Part number	UVZ1H332MHD	500USK180MEFCSN25X30
Voltage Rating	50 V	500 V
Capacitance	$10 \times 3300 \text{ } \mu\text{F}$	$2 \times 180 \text{ } \mu\text{F}$
Volume	90.3 cm^3	31.4 cm^3
Volumetric energy density	$456.6 \text{ } \mu\text{J/mm}^3$	$1433 \text{ } \mu\text{J/mm}^3$

dense option at both its voltage and capacitance ratings. The 500 V capacitor, however, is approximately $3\times$ more energy dense, leading to a substantial reduction in volume for a 500 W buffer solution.

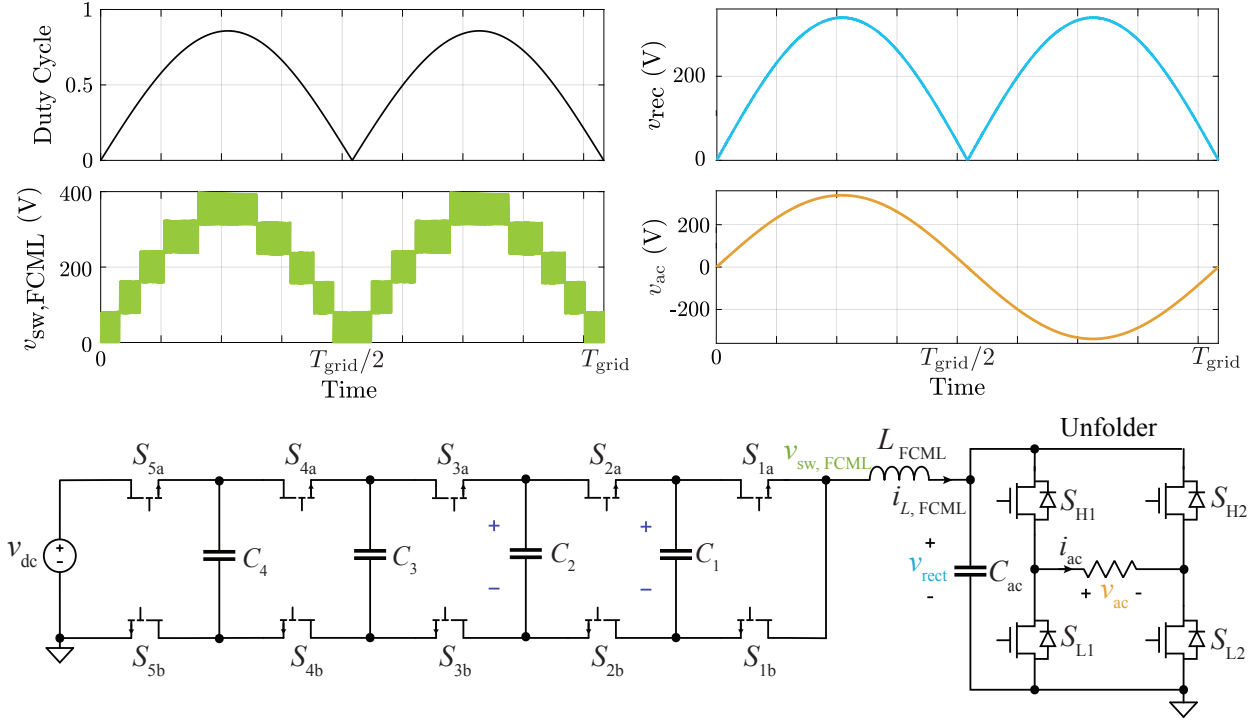


Figure 2.6: Simulation waveforms showing the rectified sinusoidal duty cycle D , the switch node voltage $v_{\text{sw,FCML}}$, the filtered rectified output voltage v_{rec} , and the ac output voltage v_{ac} for a dc input voltage $v_{\text{dc}} = 400$ V. The associated signals are labeled in the FCML inverter diagram shown directly below the key waveforms.

The Flying-Capacitor Multilevel Converter

The second stage of the microinverter is realized as a 6-level FCML inverter. An N -level FCML converter has $N - 1$ switch pairs and $N - 2$ flying capacitors. The dc voltage across each flying capacitor is given by (2.5),

$$v_{C,k} = v_{\text{dc}} \frac{k}{N-1}, \quad k = 1, \dots, N-2 \quad (2.5)$$

while each switch must block only $\frac{v_{\text{dc}}}{N-1}$. This feature makes the FCML converter an attractive option for converters operating in the hundreds of volts range while enabling it to still benefit from the high performance of low-voltage (e.g., < 200 V) GaN power transistors. Each switch is operated at a frequency of f_{sw} , and the effective frequency at the switch node is $f_{\text{eff}} = (N - 1) \cdot f_{\text{sw}}$. This frequency multiplication is achieved by phase-shifted pulse width modulation (PS-PWM) [17]. The notable implication of this is the inductor current ripple reduction on the order of $(N - 1)^2$ in comparison to a conventional buck converter. The effective switching frequency enables the production of a very well-filtered sinusoidal output with a small filter inductor compared to the conventional 2-level solution.

The duty cycle D used to generate the PWM signals for the FCML inverter is a rectified sinusoid and is shown in Fig. 2.6. The resulting switch-node voltage waveform v_{sw} generated in PS-PWM operation is filtered by the LC filter to produce v_{rec} . This voltage waveform requires unfolding by an H-bridge on the output of the converter. Example simulation voltage waveforms of the switch node voltage ($v_{sw,FCML}$), the filtered rectified sinusoid voltage (v_{rec}), and the ac output voltage (v_{ac}) are shown in Fig. 2.6 for one line cycle.

It is worth noting that a dc-ac/ac-dc converter can be realized with a totem-pole leg or the replacement of the H-bridge unfolders with a half-bridge leg [44–49]. Because the number of the low-frequency switches is reduced in the totem-pole configuration, both conduction losses and volume can be further reduced for the inverter stage. However, we choose to use a full H-bridge. This choice minimizes circuit implementation complexity, as the rectified sinusoid unfolded by the H-bridge shares the same ground voltage reference as seen at the input of the converter. The totem-pole configuration, rather, requires a change in common-mode voltage that results in large dv/dt events. Subsequently, additional control is required to handle the zero-crossing event [50].

2.3 Hardware Implementation

The complete microinverter system comprises two cascaded prototypes that are each rated for 500 W. The full developmental prototype for the CaSP stage and the affixed buffer capacitors is shown in Fig. 2.7, while the labeled power stage is provided in Fig. 2.8. The FCML inverting stage is placed on its own developmental board, and the power stage is shown with labels in Fig. 2.9.

The selected power components for both prototypes are shown in Table 2.3. Both prototypes make use of high-performance GaNFETs, which are placed on the top side of the board adjacent to the flying capacitors. The flying capacitors are multi-layer ceramic capacitors placed in parallel and are an energy-dense choice for this hardware design. A cascaded bootstrap technique is used to deliver power to the gate drive circuits in both the FCML and CaSP converters, and the required circuitry is placed on the bottom side of each of the hardware prototypes [51].

Operating conditions for the converters during hardware testing are shown in Table 2.2. Both converters are switched at 120 kHz to enable lower capacitor volumes for the CaSP converter and to enable synchronization in control between the two converters. The FCML inverter components are sized with this switching frequency in mind. A Keysight MSOX4024A oscilloscope was used to monitor critical voltage and current behavior during testing and to validate theoretical converter performance. First, ZCS operation is verified in the CaSP stage and is shown in Fig. 2.10. After each sub-period, the inductor current resonates to 0 A, which enables the switches in the CaSP converter to have soft switching, thereby reducing voltage-current overlap losses and contributing to an increase in efficiency.

Key operating waveforms for the CaSP and FCML converters are shown in Fig. 2.11. These waveforms include the HV dc bus, the inductor current for the CaSP converter, and

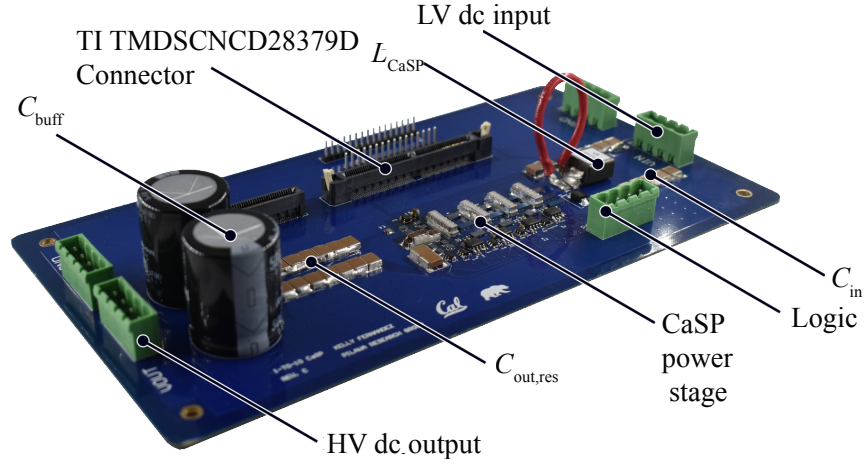


Figure 2.7: Developmental prototype of the 1-to-10 CaSP stage showing the placement of the buffer capacitors. Figure made in collaboration with Kelly Fernandez.

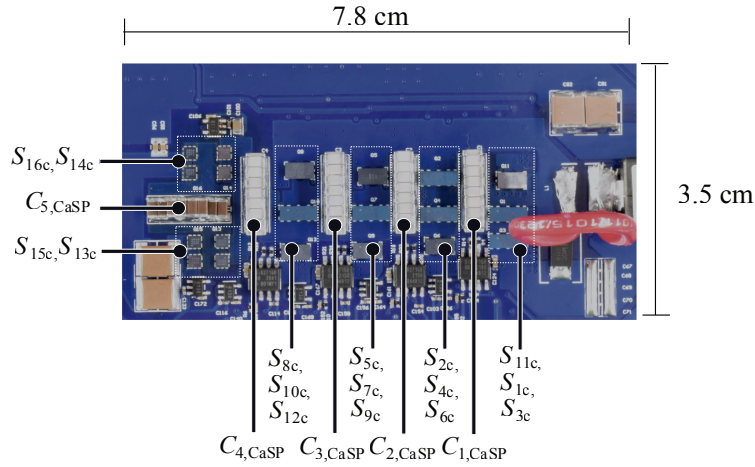


Figure 2.8: Annotated photograph of the power stage of a 1-to-10 CaSP hardware prototype. Figure made in collaboration with Kelly Fernandez.

the switch-node voltage of the FCML inverter at 500 W operation with $V_{in} = 38$ V and $v_{ac} = 240$ V_{rms}. The ac output and low-voltage dc input are shown in the measured high-precision Keysight PA2201A power analyzer waveforms in Fig. 2.12.

System efficiency for a power output between 50 W and 500 W is shown in Fig. 2.13. The CaSP stage achieves a peak efficiency of 96.1% at 340 W, and the FCML inverter achieves a peak efficiency of 98.3% at an output power of 500 W. For the merged system, the peak efficiency at $P_{out} = 340$ W is 94.3%, while the efficiency at full load is 93.8%. An estimated loss breakdown is shown in Fig. 2.14. The CaSP stage is dominated by conduction losses,

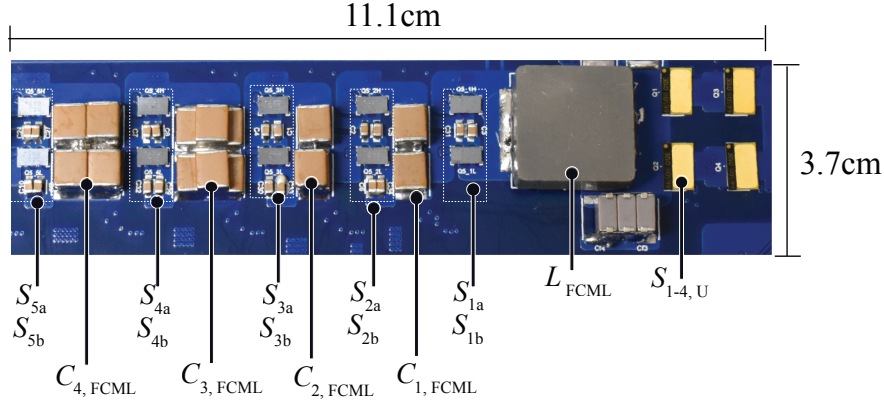


Figure 2.9: Annotated photograph of power stage of the FCML converter hardware prototype.

Table 2.2: Converter Operating Conditions

Parameter	Nominal	Range
V_{in}	38 V	35 V - 40 V
f_L	60 Hz	60 Hz
v_{ac}	240 V _{rms}	240 V _{rms}
Measured P_{out}	500 W	50 - 500 W
CaSP f_{sw}	120 kHz	100 kHz - 120 kHz
FCML f_{sw}	120 kHz	100 kHz - 120 kHz

while the FCML inverter stage is dominated by hard switching losses. Hard switching losses are a function of f_{sw} and are composed of losses generated by switch parasitic output capacitance C_{oss} and overlap losses.

It should be noted that in this work, no additional control techniques were used to increase the light-load efficiency. If desired, conventional light-load techniques such as pulse frequency modulation (PFM) or on/off control could be utilized. Other research proposes the use of variable switching frequency techniques in the FCML inverter stage to improve the efficiency of this stage [52].

In many grid-tied applications, total harmonic distortion (THD) is required to be below 5% [53]. The FCML inverter has a multiplicative switching frequency at the switched node that enables well-filtered sinusoids with a comparatively low inductance when juxtaposed against conventional 2-level designs. We show the measured THD in Fig. 2.15 across the rated power range and observe that THD is approximately 1% across the measured load range. The slight increase in THD with output power is attributed here to the increase in the HV dc bus voltage ripple, which begins to cause ac distortion at higher loads. Nevertheless,

Table 2.3: Component listing of the microinverter system hardware prototype

Subsystem	Component	Part No.	Parameters
1-to-10 CaSP	$S_{1c} - S_{4c}, S_{7c}, S_{10c}$	EPC2022	100 V, 3.2 m Ω
	S_{5c}, S_{6c}	EPC2033	150 V, 7 m Ω
	$S_{8c}, S_{9c}, S_{11c}, S_{12c}$	EPC2034C	200 V, 8 m Ω
	$S_{13c} - S_{16c}$	EPC2050	350 V, 80 m $\Omega \times 2$ (parallel)
	$C_{1,CaSP} - C_{4,CaSP}$	Murata GRM31C5C1H224JE02L	0.22 μ F $\times 15$ (parallel), C0G
	$C_{5,CaSP}$	Murata GCM31C5C2E223JX03L	0.022 μ F $\times 12$ (parallel), C0G
	L_{CaSP}	Coilcraft SLC1480-321MLD	320 nH
6-level FCML	GaN FETs	EPC2033	150 V, 7 m Ω
	Flying Capacitors	TDK C5750X6S225K250KA	2.2 μ F $\times 2-8$ (parallel, $\sim 2.6 \mu$ F effective)
	L_{FCML}	Vishay IHLP6767GZER150M8A	15 μ H
Unfolder	GaN FETs	GS66508T-MR	650 V, 30 A
Capacitors	C_{in}	Cal Chip Electronics GMC55X7R226M50NT	22 μ F $\times 20$ (parallel)
	$C_{buff,line}$	Rubycon 500USK180MEFCSN25X30	180 μ F, 500 V $\times 2$ (parallel)
	$C_{out,res}$	TDK C5750X6S225K250KA	2.2 μ F $\times 26$ (parallel)
Control	Microcontroller	TI F28379D controlCARD	C2000 Series Microcontroller

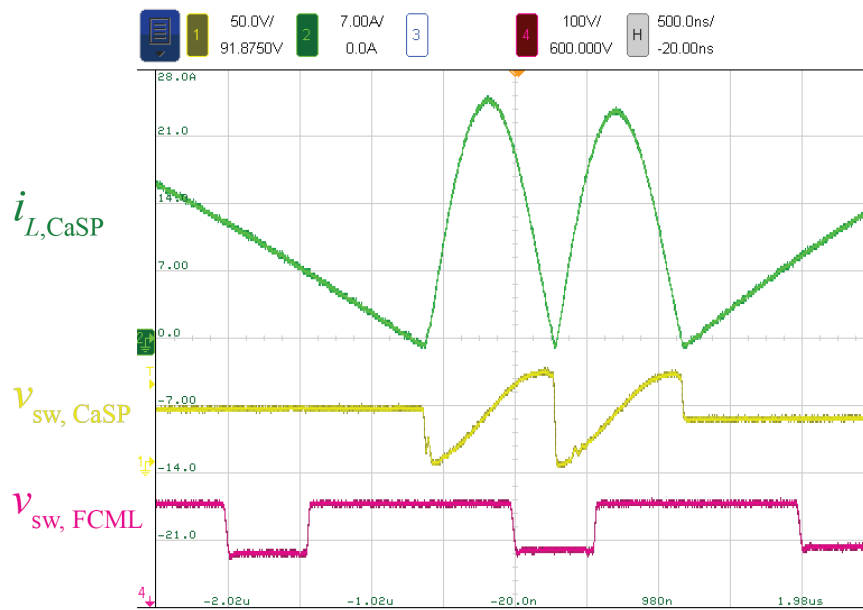


Figure 2.10: ZCS operation with waveforms of $i_{L,CaSP}$, $v_{sw,CaSP}$, and $v_{sw,FCML}$. Figure made in collaboration with Kelly Fernandez.

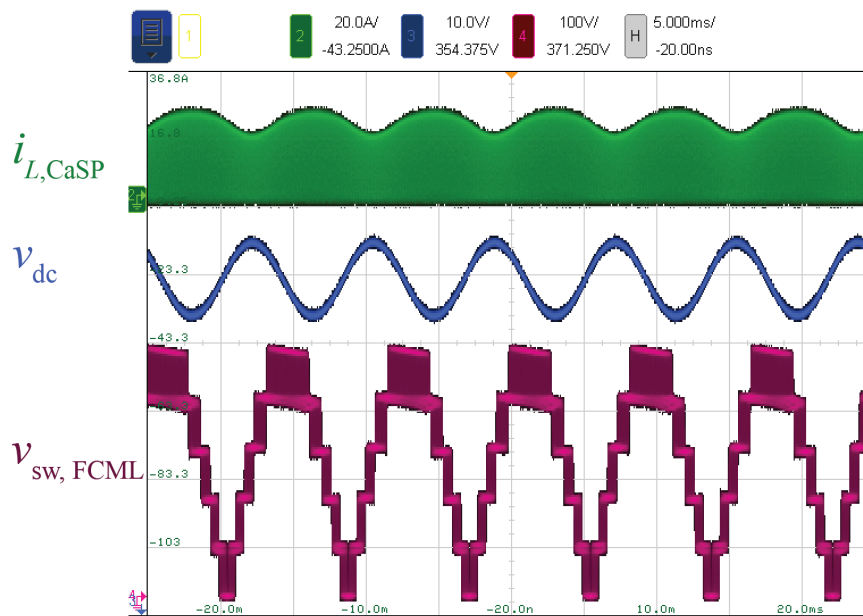


Figure 2.11: Plot of converter waveforms $i_{L,CaSP}$, v_{dc} , and $v_{sw,FCML}$ at 500 W. Figure made in collaboration with Kelly Fernandez.

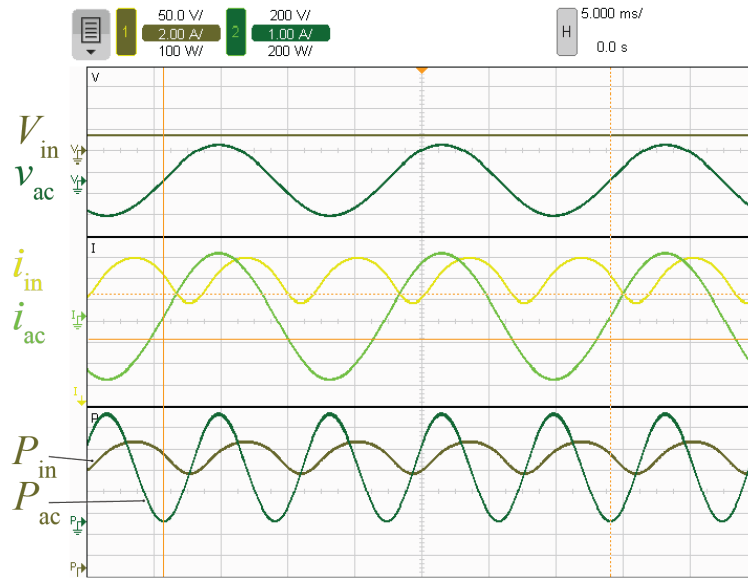


Figure 2.12: A power analyzer screenshot showing the low-voltage dc input and the ac outputs. Figure made in collaboration with Kelly Fernandez.

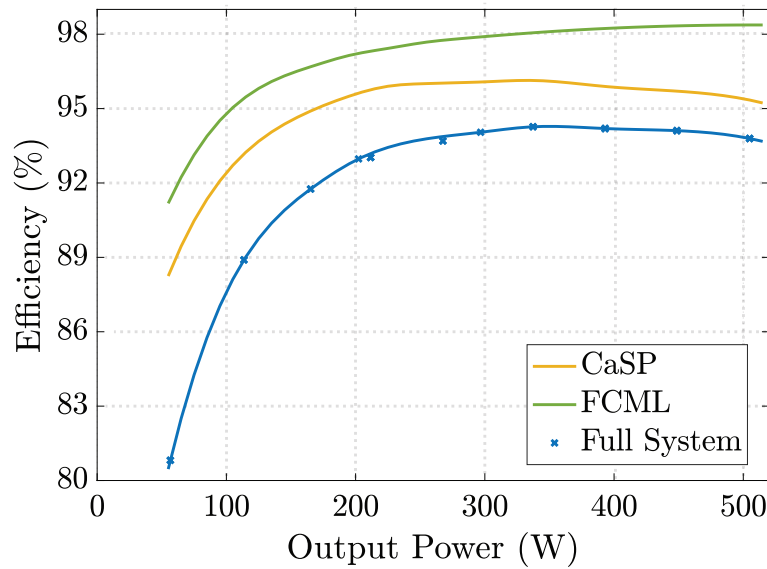


Figure 2.13: Efficiency of the two-stage converter across a load condition of 50 W to 500 W. Figure made in collaboration with Kelly Fernandez.

Table 2.4: Volumetric breakdown of each key converter stage.

Stage	Volume cm^3
CaSP Step-Up	27.3
FCML Inverter	35.6
Buffer Capacitance	31.4

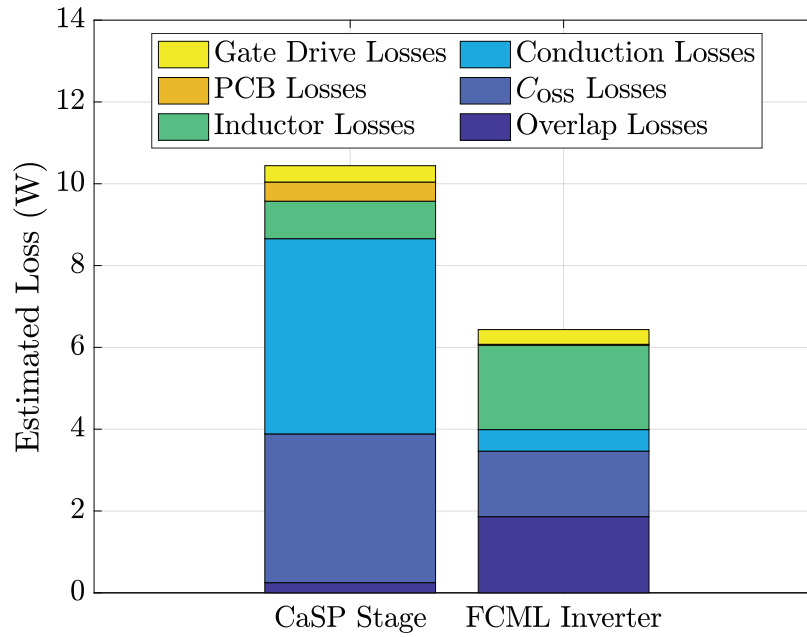


Figure 2.14: Estimated loss breakdown for each converter stage at an output power of 340 W. The loss breakdown is composed of hard switching losses, conduction losses, inductor losses, and PCB losses.

the sinusoid is well-filtered overall by the 600 kHz switched-node frequency.

Successful startup transient waveforms are shown for the CaSP converter in Fig. 2.16a and for the full system in Fig. 2.16b. The full system startup as demonstrated in this work is appropriate for a single grid-forming inverter, where the output is not connected to an energized grid. The CaSP stage can softly charge up its capacitors to their nominal dc offsets and provide a ramped input voltage to the FCML inverter stage. This intrinsic converter ability further incentivizes the use of the proposed two-stage architecture, as it removes the need for additional startup circuitry and control.

The overarching purpose of this work was to validate a completely hybrid switched-

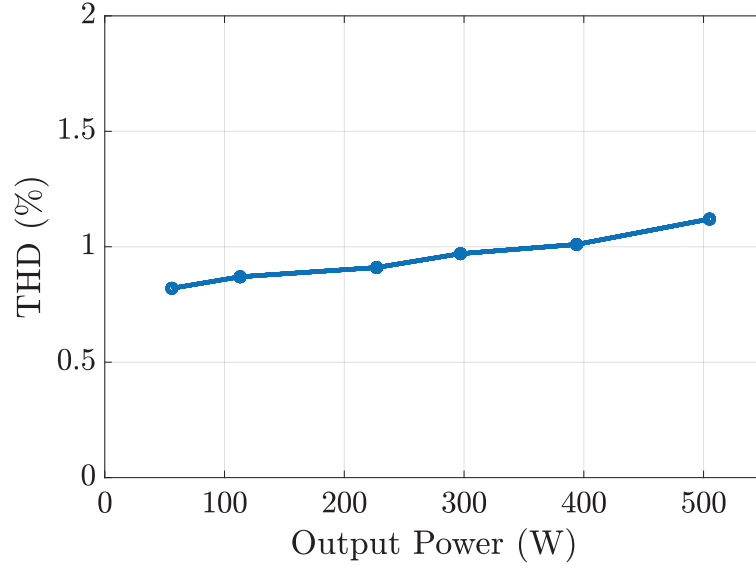
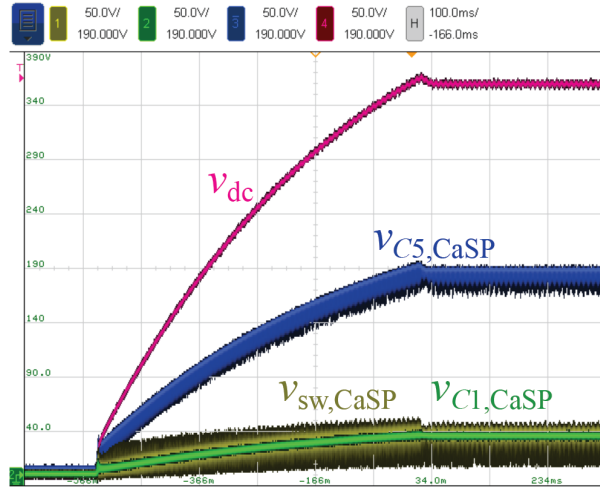
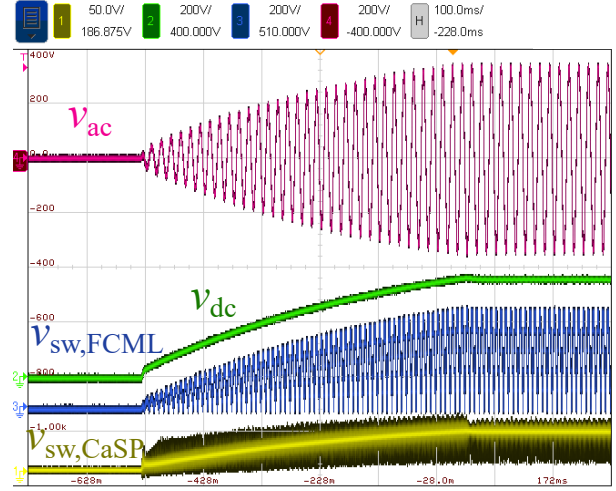


Figure 2.15: Plot of THD vs. power output across the full load range.



(a) Voltage waveforms for v_{dc} , $v_{C5, CaSP}$, $v_{C1, CaSP}$, $v_{sw, CaSP}$ during startup at $V_{in} = 36$ V and $P_{out} = 110$ W. Figure made in collaboration with Kelly Fernandez.



(b) Waveforms for v_{ac} , v_{dc} , $v_{sw, FCML}$, and $v_{sw, CaSP}$ for the full system during startup at $V_{in} = 36$ V and $P_{out} = 110$ W. Figure made in collaboration with Kelly Fernandez.

Figure 2.16: Startup waveforms for the CaSP and full system cases.

capacitor microinverter implementation, and to use of a two-stage converter to improve the twice-line frequency buffer volume. The total power density could be improved by further system packaging. In Table 2.4, we show the breakdown of volumes for each converter stage. Excluding the buffer capacitor, the volume of the power conversion stages is 62 cm^3 , amounting to a power density of 8.2 kW/L . The two aluminum electrolytic buffer capacitors have a combined volume of 32 cm^3 , contributing to a total system power-conversion density of 5.5 kW/L . One observation here is that the combined volume of the converter stages and the discretely summed buffer capacitance is approximately the same volume as the equivalent buffer capacitance for the single-stage microinverter solution from Table 2.1 (90 cm^3). The reduced conversion volume would enable a substantial reduction in total system volume using this architecture, providing contrast to previous literature advocating for single-stage solutions to maximize power density.

2.4 Conclusion

This work demonstrates the successful implementation of a PV microinverter architecture comprising a fixed ratio 1-to-10 CaSP boost stage followed by an FCML inverter. This chapter outlines the fundamental theory of operation for each stage, evaluates the merits of placing the twice-line frequency power pulsation buffer at a high-voltage intermediate dc bus, and showcases a full solution in hardware. The proposed solution is a fully hybrid switched-capacitor-based design and leverages these high-performance converters uniquely for microinverter applications. Hardware results at full power and voltage are shown, including the use of the CaSP stage for a full startup sequence. The full system demonstrates a conversion-stage power density of 8.2 kW/L and a peak efficiency of 94.3% .

One observation from the shape of the efficiency waveform in this work, and from the loss breakdown in Fig. 2.14, is that the FCML inverter stage is limited by hard switching losses. While the converter was designed around a 120 kHz switching frequency, this resulted in efficiency limitations, especially for the selected GaNFETs. This observation evokes questions as to how fast we *should* switch the FCML converter. In Chapter 3 we implement variable switching frequency control to improve the efficiency of this FCML inverter hardware prototype.

Chapter 3

Variable Switching Frequency Control for DC-AC FCML Converters to Improve Efficiency

Executive Summary

The use of GaN devices in the FCML converter enables further miniaturization of the converter through efficient switching in the hundreds of kilohertz. However, as identified in the previous chapter, these devices still incur hard switching losses across the load range. The research in this chapter presents a set of constraints that can be used to develop a set of safe operating conditions for the FCML inverter to be operated with a variable switching frequency under nominal PS-PWM operation. By intentionally lowering the switching frequency during portions of the line cycle where the FCML converter has low passive component ripple, we can improve system efficiency by mitigating these losses. Using the same hardware prototype presented in Chapter 2, we show that this switching frequency scheme can be used to reduce losses by up to 35%. Furthermore, the control can be implemented in a conventional microcontroller, which enables the application of this technique to pre-existing hardware prototypes.

This chapter is based on work appearing in both [54] and [52].

3.1 Introduction

The increased adoption of hybrid switched-capacitor and multilevel converter topologies such as the FCML converter is a direct result of the comparative passive component volume reduction and increased efficiency they boast. This is accomplished via the use of high figure-of-merit low-voltage switches [23, 35, 42, 55] and the use of energy-dense capacitors [13]. For dc-ac applications such as renewable energy conversion or electric vehicle charging,

where efficiency and power density are critical design objectives, the FCML converter is an attractive solution [21, 56–58].

While the FCML converter leverages the power density of capacitors to reduce overall converter volume, the inductor remains a large and lossy component in the circuit, owing to its comparatively poor energy density. In dc-ac operation, the inductor is typically sized to limit the current ripple at a set switching frequency f_{sw} . However, the peak-to-peak inductor current ripple $\Delta i_{L,\text{pp}}$ is a strong function of the duty cycle in the dc-ac FCML converter, and the resulting converter has both over-rated passive components at many operating conditions and increased losses at a higher than needed switching frequency. Under constant f_{sw} , the inductor volt-seconds vary over the line cycle. Thus, to meet a maximum current ripple specification, the inductance L and a constant f_{sw} must be chosen for the worst operating point in the line cycle.

Previous work in the dc-dc space has investigated modulation techniques for inductor current ripple control in the multilevel buck-boost transition region as well as modulation schemes to change the effective level count of the FCML [59, 60]. For dc-ac FCML converters, variable frequency control has been specifically used to limit the voltage ripple on flying capacitors [61–63], to mitigate capacitor ripple during overload conditions [64], and to achieve boundary conduction mode in FCML inverters to reduce switching losses [65].

This work develops guidelines for a variable switching frequency scheme that maintains constant inductor current ripple ($\Delta i_{L,\text{pp}}$) in dc-ac FCML converters. The required switching frequency is derived based on the dependency of the inductor current ripple on the instantaneous duty cycle and switching frequency. Further constraints are set for the lower switching frequency limits based on the allowable flying capacitor voltage ripple $\Delta v_{C,\text{fly}}$ and the LC filter on the output of the converter. These limits create a set of guidelines that ensures that all passive ripple conditions are achieved, even when the switching frequency is reduced beyond its nominal rating. The overall reduction in switching frequency enables the realization of higher efficiencies by reducing switching-related losses.

3.2 Overview of Theory and Control

Conventional FCML Inverter Operation

In this work, we consider an FCML converter operated under phase-shifted pulse-width modulation (PS-PWM) [17]. In comparison to a conventional buck converter, the inductor current ripple of an FCML converter is reduced by a factor of $(N - 1)^2$ for a given switching frequency and inductance value and is described by

$$\Delta i_{L,\text{pp}} = \frac{V_{\text{in}} D_{\text{eff}} (1 - D_{\text{eff}})}{L f_{\text{sw}} (N - 1)^2}, \quad (3.1)$$

where the effective duty cycle at the switch node is given by

$$D_{\text{eff}} = D(N - 1) - \lfloor D(N - 1) \rfloor. \quad (3.2)$$

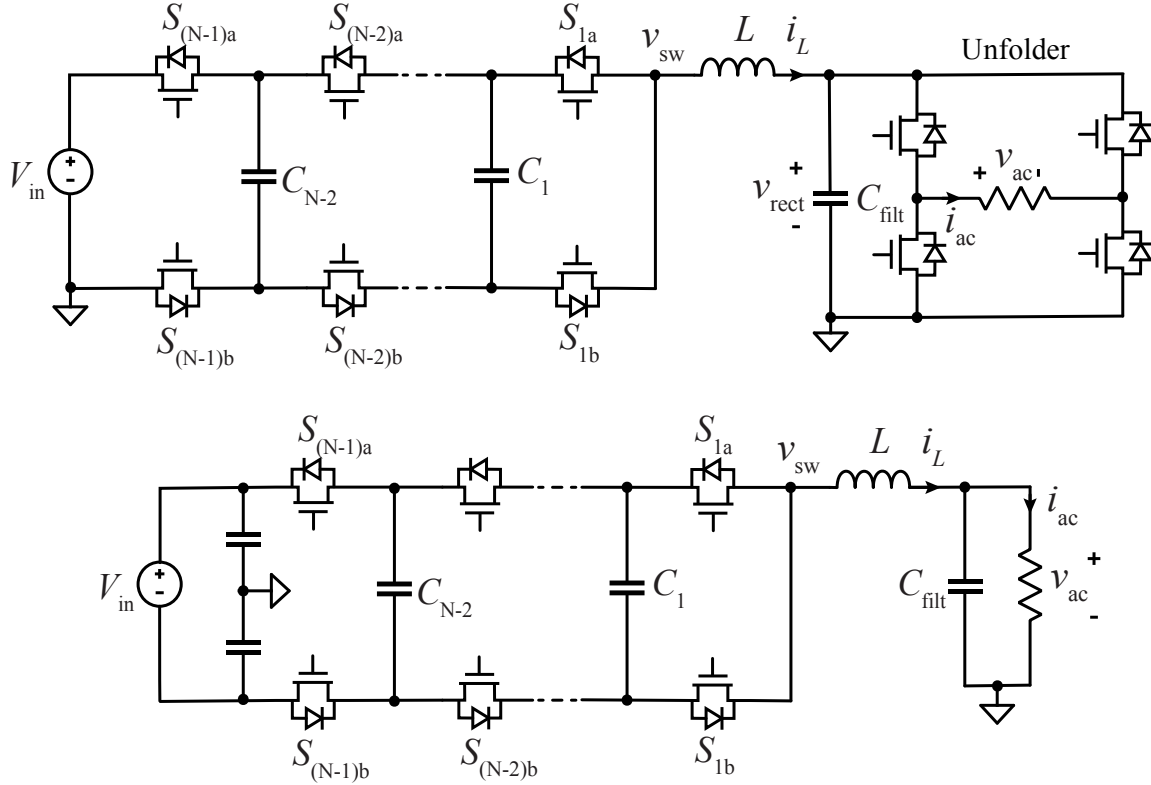


Figure 3.1: a) An N -level FCML converter with an H-bridge unfolded for dc-ac operation. b) An N -level FCML inverter configured with a split-bus input. Each configuration has $N - 1$ switch pairs and $N - 2$ flying capacitors.

There are a few conventional ways of realizing a dc-ac (or ac-dc) FCML converter. The first solution is through the inclusion of an unfolded at the output of the converter. This translates the rectified and filtered sinusoidal voltage at the output of the converter to be an ac voltage at the output terminals. Because the rectified sinusoid can have a peak voltage of V_{in} , the ac output voltage has a maximum ac voltage peak of $\pm V_{in}$ in this configuration. The other distinct way to conventionally realize the ac output voltage is to place a neutral point at the midpoint of the dc input of the converter. This split-bus configuration enables the generation of an ac output voltage with a maximum modulation depth of $\pm V_{in}/2$. The split-bus configuration is similar to the typical implementation of one phase in a three-phase dc-ac application. In a single-phase application, there are tradeoffs between these two approaches in terms of the peak magnitude of the ac output voltage that can be generated.

Fig. 3.1a shows an N -level FCML converter with an H-bridge unfolded at the output used to convert the filtered rectified sinusoid at the v_{rect} node into the ac output waveforms. The duty cycle over a half of a modulation cycle used to generate the ac output is shown in Fig. 3.2a.

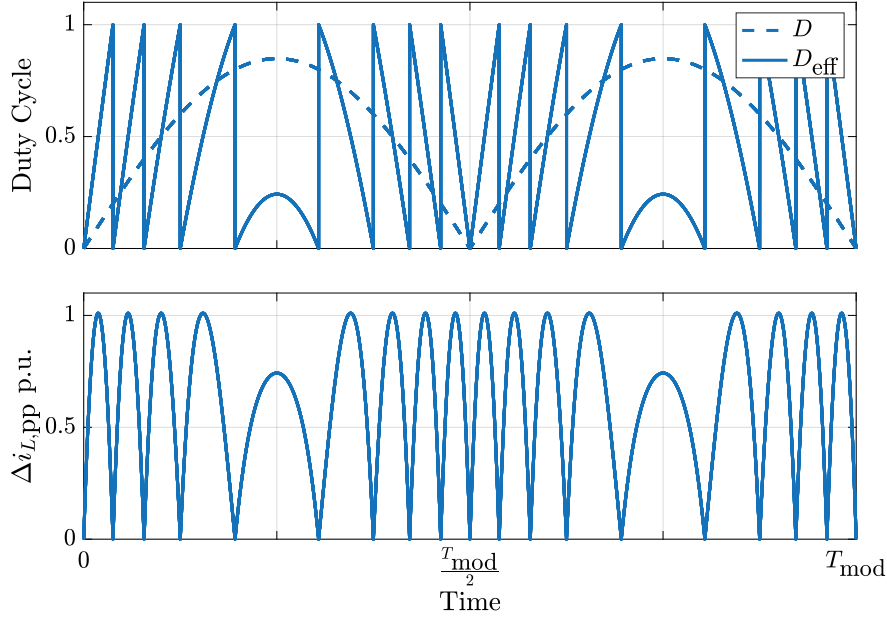


Figure 3.2: a) Duty cycle D and corresponding D_{eff} across a modulation cycle for the FCML converter with an unfolded such as the one in Fig. 1a. b) Normalized inductor current ripple at each duty cycle for a 6-level FCML inverter during an ac cycle showing the impact of the duty cycle D on inductor current ripple.

Subsequently, for a dc-ac FCML converter with an unfolded, the inductor current ripple $\Delta i_{L,\text{pp}}$ varies since the duty cycle is a rectified sinusoid. At certain duty cycles $D = \frac{k}{N-1}$, $k \in [1, N-2]$, the effective duty cycle D_{eff} is 0, and $\Delta i_{L,\text{pp}} = 0$ A as per the expression in (3.1). Fig. 3.2b also shows the normalized inductor current ripple across half of a modulation cycle and how D_{eff} corresponds with $\Delta i_{L,\text{pp}} = 0$ A at these nominal duty cycles. These signals result in the voltages and inductor current in Fig. 3.3.

For a split-bus FCML inverter such as the one in Fig. 3.1b, the duty cycle varies as a function of $D = \frac{1}{2} + M \sin(2\pi f_{\text{mod}} t)$ for carrier voltages between 0 and 1. The following component ripple relationships are functionally the same.

While the inductor in an FCML inverter might be sized for the ripple at the peak of the ac cycle, the maximum inductor current ripple occurs when $D_{\text{eff}} = \frac{1}{2}$ and is calculated as

$$\Delta i_{L,\text{pp}, \text{max}} = \frac{V_{\text{in}}}{4L f_{\text{sw}} (N-1)^2}. \quad (3.3)$$

Thus, regarding this rated current ripple, the resulting switching frequency f_{sw} is higher than necessary around the low-ripple duty cycles. This results in unnecessarily high losses, particularly in the switches.

The primary energy-conditioning elements in the FCML converter are the flying capacitors. In addition to the nominal dc voltage offsets these capacitors have, there is an additional

ripple component with peak-to-peak magnitude Δv_C , and the capacitor voltage is nominally bounded by

$$v_{C,k} = V_{C,k} \pm \Delta v_C/2. \quad (3.4)$$

The capacitor voltage ripple Δv_C is load-current dependent and is a piecewise expression with ranges set by the duty-cycle regions. This piecewise behavior is a result of the different capacitor charging behaviors near the duty-cycle extrema, and the ripple is given by

$$\Delta v_C = \begin{cases} \frac{|i_{ac}| \cdot D_{\text{eff}}}{(N-1) \cdot f_{\text{sw}} \cdot C_{\text{fly}}} & D \leq \frac{1}{N-1} \\ \frac{|i_{ac}|}{(N-1) \cdot f_{\text{sw}} \cdot C_{\text{fly}}} & \frac{1}{N-1} < D < \frac{N-2}{N-1} \\ \frac{|i_{ac}| \cdot (1-D_{\text{eff}})}{(N-1) \cdot f_{\text{sw}} \cdot C_{\text{fly}}} & \frac{N-2}{N-1} \leq D \end{cases} \quad (3.5)$$

The flying capacitor voltage ripple Δv_C is conventionally constrained as a fraction α_C of the switch blocking voltage, which is nominally described as $\Delta v_C = \alpha_C 2V_{\text{in}}/(N-1)$. In recent designs, the normalized ripple is often somewhere between 5 and 30%, where ripples closer to and exceeding 30% appear in high power-density applications [66, 67].

Variable Switching Frequency Constraints

The goal of this work is to decrease converter losses. Here, we outline the constraints imposed by passive component current/voltage ripples that create the basis for the deterministic switching frequency scheme across the ac voltage modulation cycle. Ultimate lower limits

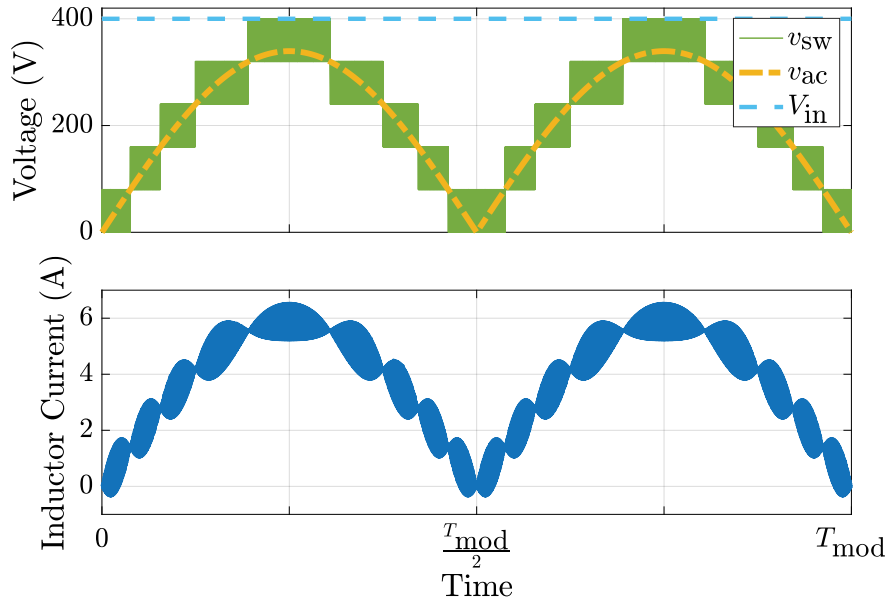


Figure 3.3: Calculated waveforms at $V_{\text{in}} = 400 \text{ V}$, $v_{\text{ac}} = 240 \text{ V}$, $P_{\text{out}} = 1 \text{ kW}$, $L = 22 \mu\text{H}$, $f_{\text{sw}} = 100 \text{ kHz}$.

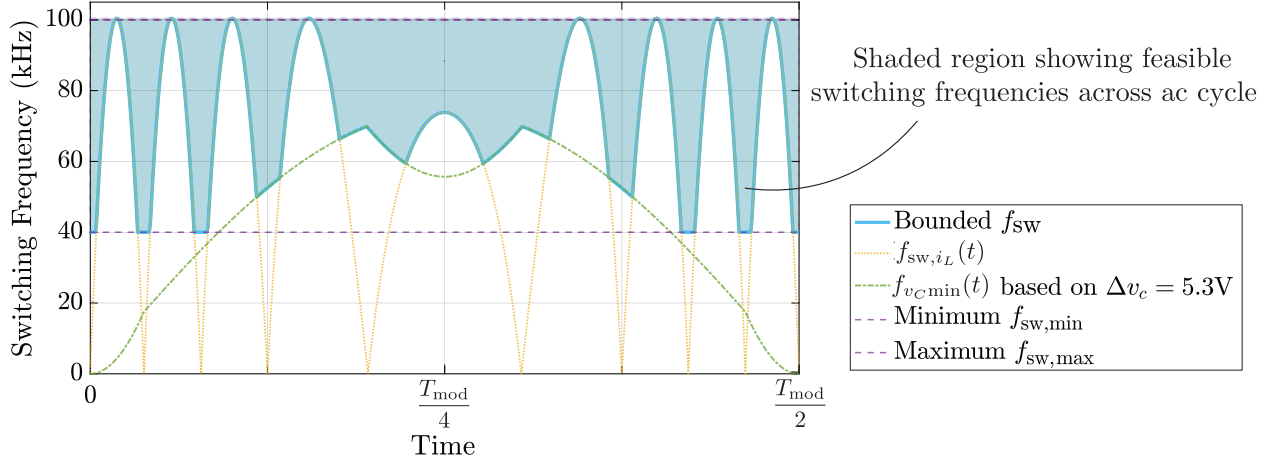


Figure 3.4: Variable switching frequency f_{sw} computed across half of a modulation cycle showing the minimum constraints set by the capacitor voltage ripple and the LC filter. The shaded region shows feasible switching frequencies at each point along half of the ac modulation cycle.

for the switching frequency are set by the LC filter and practical considerations for discrete implementation for a generalized ac output frequency. The constraints set forth generate a safe operating region for the FCML converter switching frequency across the ac modulation cycle, which is conceptually captured as the shaded region in Fig. 3.4.

Inductor Current and Flying Capacitor Voltage Ripple

By rearranging the expression in (3.1), it is possible to derive an expression for achieving a fixed inductor current ripple. This work proposes varying the switching frequency along the ac modulation cycle using (3.6) to reduce converter losses. Here, the effective duty cycle D_{eff} is a time-varying function of the ac duty cycle.

$$f_{sw,i_L}(t) = \frac{V_{in} D_{eff} (1 - D_{eff})}{\Delta i_{L,pp, \max} L (N - 1)^2} \quad (3.6)$$

Assuming a fixed maximum allowable voltage ripple $\Delta v_{C,\max}$, a lower switching frequency limit $f_{vC, \min}$ is derived from (3.5) as a function of the flying capacitance C_{fly} and the instantaneous load current i_{ac} . The function $f_{vC, \min}$ in (3.7) is piecewise, as the flying capacitor voltage ripple has different duty-cycle-dependent charging times due to PS-PWM operation [68, 69].

$$f_{vC, \min}(t) = \begin{cases} \frac{|i_{ac}| \cdot D_{eff}}{(N-1) \cdot \Delta v_{C,\max} \cdot C_{fly}} & D \leq \frac{1}{N-1} \\ \frac{|i_{ac}|}{(N-1) \cdot \Delta v_{C,\max} \cdot C_{fly}} & \frac{1}{N-1} < D < \frac{N-2}{N-1} \\ \frac{|i_{ac}| \cdot (1 - D_{eff})}{(N-1) \cdot \Delta v_{C,\max} \cdot C_{fly}} & \frac{N-2}{N-1} \leq D \end{cases} \quad (3.7)$$

Resonant LC Tank Frequency

An absolute lower switching frequency $f_{\text{sw},\text{min}}$ is set based on the LC filter at the output. The effective switching frequency at the switch node is f_{eff} , and must be sufficiently higher than the corner frequency of the LC filter given by $f_{\text{corner}} = \frac{1}{2\pi\sqrt{LC_{\text{flt}}}}$ to avoid resonant behavior. For a given converter, both L and C_{flt} are sized to meet a predefined output voltage ripple rating [23, 64, 70], and to achieve sufficient frequency attenuation of f_{eff} . Thus, the switching frequency needs to satisfy the expression described by

$$f_{\text{sw},\text{min},LC} = \alpha_{LC} \frac{1}{(N-1)2\pi\sqrt{LC_{\text{flt}}}} \quad (3.8)$$

where α_{LC} is a user-defined scaling factor. This scaling factor can be used to achieve

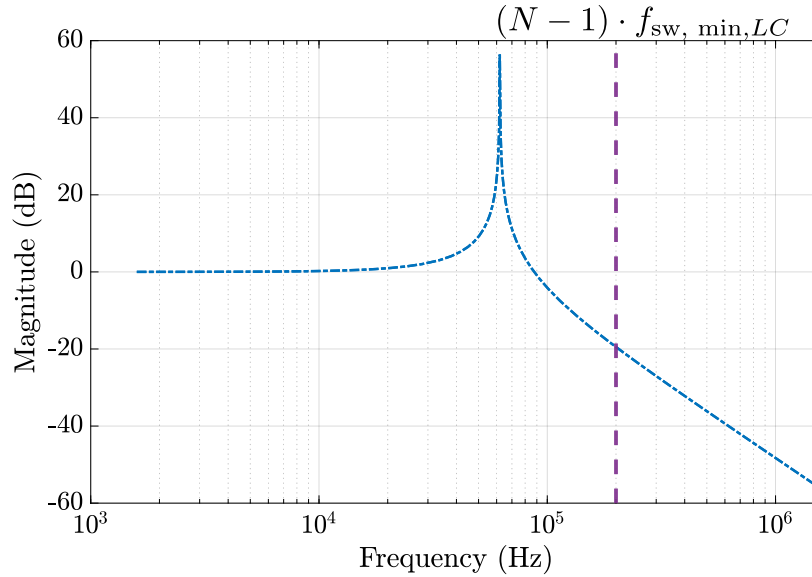


Figure 3.5: Plot of transfer function magnitude of the LC filter and $5 \cdot f_{\text{sw},\text{min},LC} = 200$ kHz showing good expected attenuation of f_{eff} .

adequate second-order filter attenuation and to avoid resonance with the LC filter. Because the filter capacitance C_{flt} in the dc-ac FCML converter is generally smaller than the flying capacitance, the higher frequency of the two resonant LC tanks that can be formed is captured.

For example, for the 6-level grid-tied prototype presented in Section 2.3, $f_{\text{sw},\text{min},LC} = 40$ kHz is an absolute lower limit, which corresponds to a minimum effective switching frequency of $f_{\text{eff}} = 200$ kHz for the 6-level FCML inverter. In this instance, f_{eff} is separated from f_{corner} by $\alpha_{LC} = 3.2$, and the filter attenuates the minimum effective switching frequency $f_{\text{eff}} = 200$ kHz by 19.5 dB. Fig. 3.5 shows a line for $f_{\text{eff}} = 200$ kHz in relation to the LC filter transfer function, corresponding to high attenuation.

Limitations Imposed by Discrete Control Implementation

This work further considers the role and limitations imposed by the modulation frequency (f_{mod}) and by the level count in generating the possible sequence of switching-frequency events. For a low modulation frequency such as the common grid frequencies (50-60 Hz), updating the period after each switching instance results in a frequency sequence with very granular steps across the ac cycle.

However, as the period length T_{mod} decreases with higher modulation frequencies, the number of possible switching frequency updates across the ac cycle is diminished for the same band of switching frequencies. For a higher modulation frequency, depending on the sampling instant, the limited updates to switching frequency might result in a dithering scheme that appears pseudo-random.

The simulated discrete switching-frequency steps for different modulation frequencies are shown for a portion of T_{mod} in Fig. 3.6. For the 60 Hz grid frequency, the switching-frequency waveform is smooth, as it is updated at a rate much faster than f_{mod} . For a modulation frequency of 1 kHz, the switching frequency may jump from the maximum switching frequency to the minimum in some portions of the ac cycle.

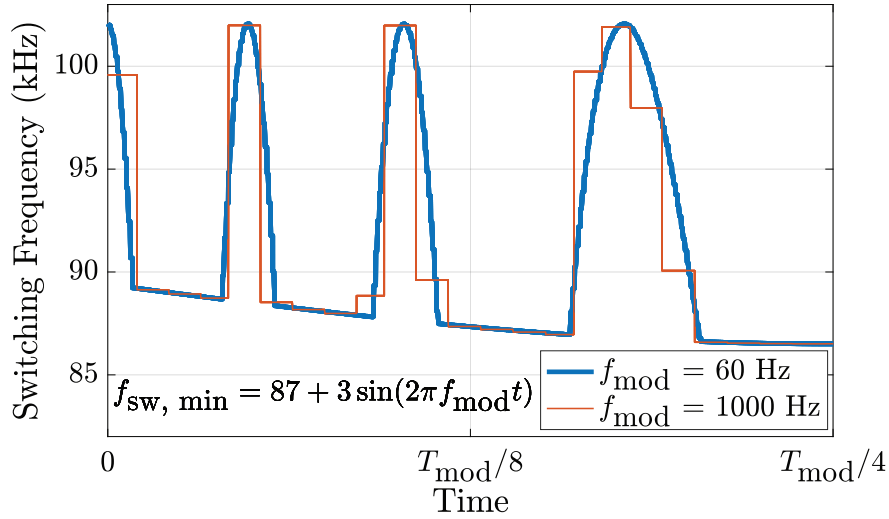


Figure 3.6: Discrete frequency envelopes from simulation for both 60 Hz and 1 kHz modulation frequencies showing the impact of sizing f_{mod} for an 8-level converter with a split-bus input. Note that here, the lower limit for $f_{\text{sw, min}}$ is set as a sinusoid with a frequency of f_{mod} to avoid the switching frequency hitting a hard limit over much of the ac cycle.

To better understand the impacts of level count and modulation frequency on the ideal discrete switching-frequency sequence, the shortest sub-duration between nominal duty ratios within the ac cycle is considered. For an even-level split-bus FCML where the duty cycle is given by $D = \frac{1}{2} + M \sin(2\pi f_{\text{mod}} t)$, this sub-duration is between $D = \frac{1}{2} + \frac{1}{2(N-1)}$ and $D = \frac{1}{2} - \frac{1}{2(N-1)}$. For an odd level count, this sub-duration occurs between $D = \frac{1}{2} + \frac{1}{N-1}$ and

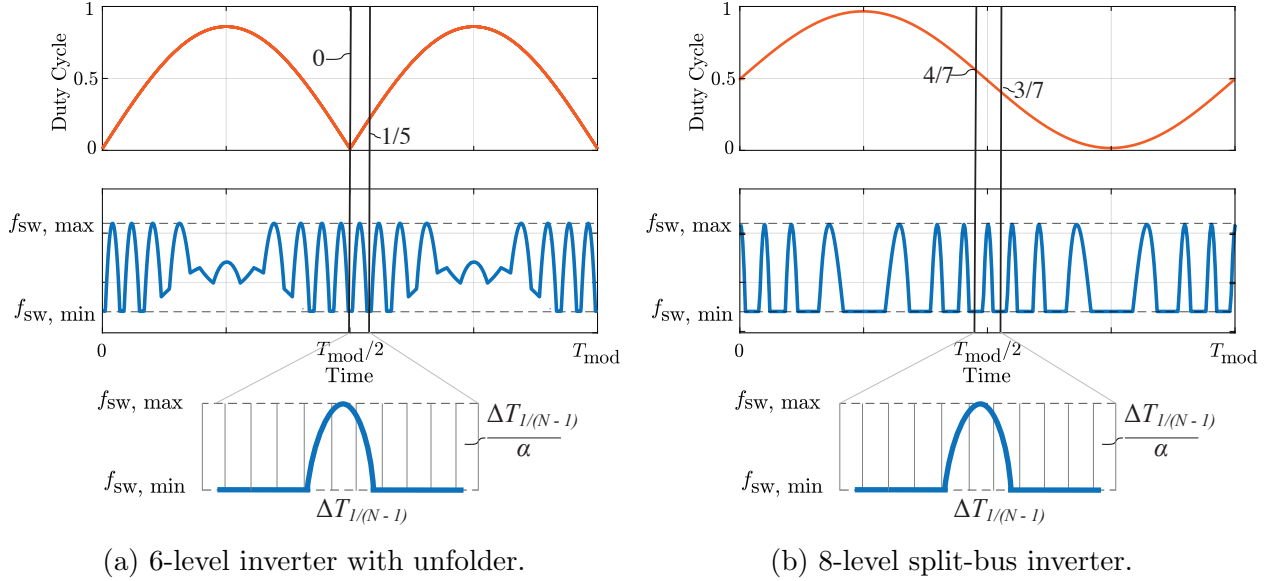


Figure 3.7: Comparison of $\Delta t_{1/(N-1)}$ relationship to sinusoidal duty cycle for (a) a 6-level topology with an unfold and (b) an 8-level split-bus FCML topology. In both cases, the minimum number of steps during the shortest sub-duration is constrained by $f_{sw, \min}$.

$D = \frac{1}{2}$. The time duration for these two cases is computed as $\Delta t_{1/(N-1)}$ and is given in (3.9) for a split-bus FCML and in (3.10) for an unfold-based converter, where the duty cycle is defined as $D = |M \sin(2\pi f_{\text{mod}} t)|$.

$$\Delta t_{1/(N-1)} = \begin{cases} \frac{\arcsin\left(\frac{1}{2M(N-1)}\right)}{\pi f_{\text{mod}}} & N, \text{ even, split bus} \\ \frac{\arcsin\left(\frac{1}{M(N-1)}\right)}{2\pi f_{\text{mod}}} & N, \text{ odd, split bus} \end{cases} \quad (3.9)$$

$$\Delta t_{1/(N-1)} = \frac{\arcsin\left(\frac{1}{M(N-1)}\right)}{2\pi f_{\text{mod}}} \quad N, \text{ even, odd, unfold} \quad (3.10)$$

To guarantee a user-specified minimum number of steps during this time window to achieve a more continuous frequency envelope in hardware, a minimum required switching-frequency cutoff is obtained as

$$f_{\text{disc, cutoff}} \geq \alpha_d \frac{1}{\Delta t_{1/(N-1)}} \quad (3.11)$$

where α_d is the minimum number of discrete steps in $\Delta t_{1/(N-1)}$.

Fig. 3.7a shows how this sub-duration $\Delta t_{1/(N-1)}$ relates to the duty cycle for the 6-level converter with an unfold examined in this chapter. Fig. 3.7b shows how this sub-duration $\Delta t_{1/(N-1)}$ relates to the duty cycle for the split-bus 8-level converter examined in Chapter 7 of this work. The sub-duration is visually divided into a minimum number of possible steps.

The upper limits for switching frequency are determined in this case by the peak inductor current ripple.

In Fig. 3.8, we examine how an increase in modulation frequency makes it challenging to set a low switching frequency limit while still enabling the variable switching frequency scheme. Illustratively, for the 6-level inverter used in Chapter 2, with $f_{\text{mod}} = 60$ Hz, we see that to guarantee at least 50 steps in $\Delta t_{1/(N-1)}$, a switching frequency of at least 39 kHz is required.

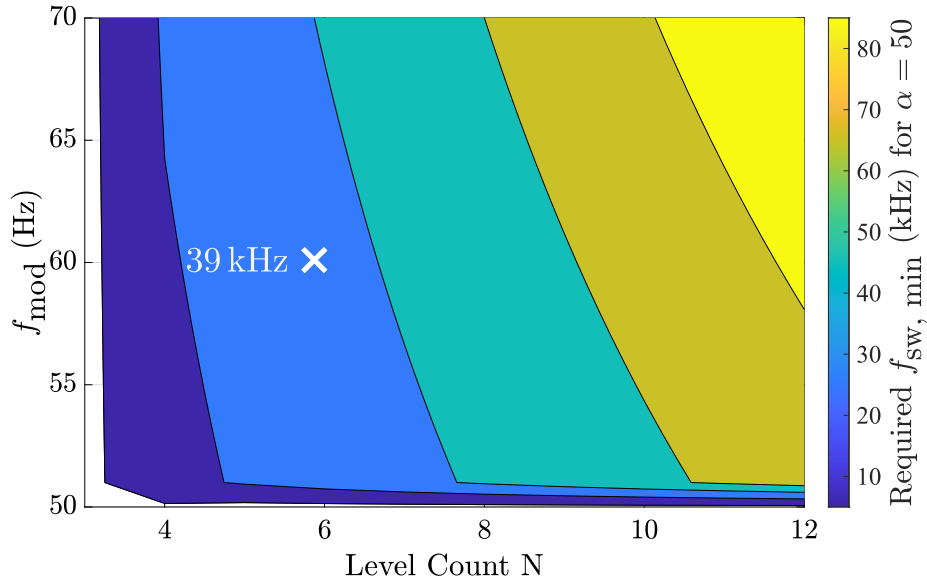


Figure 3.8: Contour plot showing how $f_{\text{sw}, \text{min}}$ scales across both level count N and ac modulation frequency f_{mod} to ensure that at least 50 steps ($\alpha \geq 50$) are generated across the brief sub-duration defined by $\Delta t_{1/(N-1)}$. For the 6-level FCML with an unfold and $f_{\text{mod}} = 60$ Hz, this limit is computed to be at least 39 kHz.

Constrained Operating Conditions

Considering the four constraints detailed above, a compact operating space for the switching-frequency envelope across the ac cycle can be defined as

$$\begin{aligned} f_{\text{sw}}(t) &= \max[f_{\text{sw}, i_{L_{\text{pp}}}}(t), f_{\text{sw}, v_{C_{\text{pp}}}}(t)], \\ \max(f_{\text{sw}, \text{LC}}, f_{\text{disc, cutoff}}) &\leq f_{\text{sw}}(t) \leq f_{\text{sw}, \text{max}}. \end{aligned} \quad (3.12)$$

The shape of the envelope waveform is strongly determined by the duty-cycle-dependent functions $f_{\text{sw}, i_{L_{\text{pp}}}}(t)$ and $f_{\text{sw}, v_{C_{\text{pp}}}}(t)$. The resulting switching frequency scheme over half of a modulation cycle for a 6-level FCML converter with an unfold is shown in Fig. 3.9. The simulated resulting inductor current waveform is captured in Fig. 3.10.

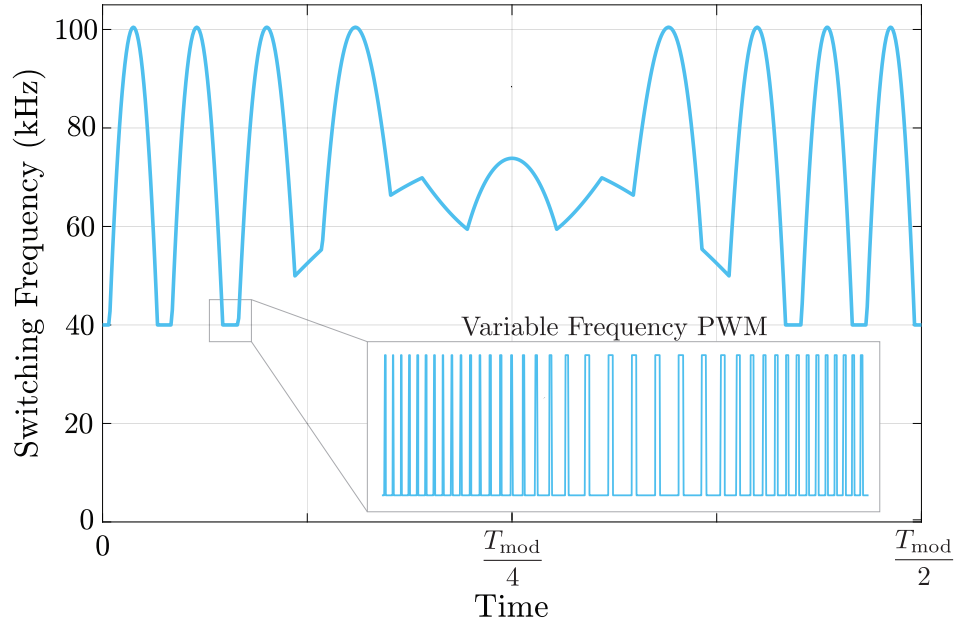


Figure 3.9: Variable frequency pattern over half of an ac modulation cycle set by (3.12) showing low ripple regions, and the corresponding variable frequency PWM concept during a low ripple region.

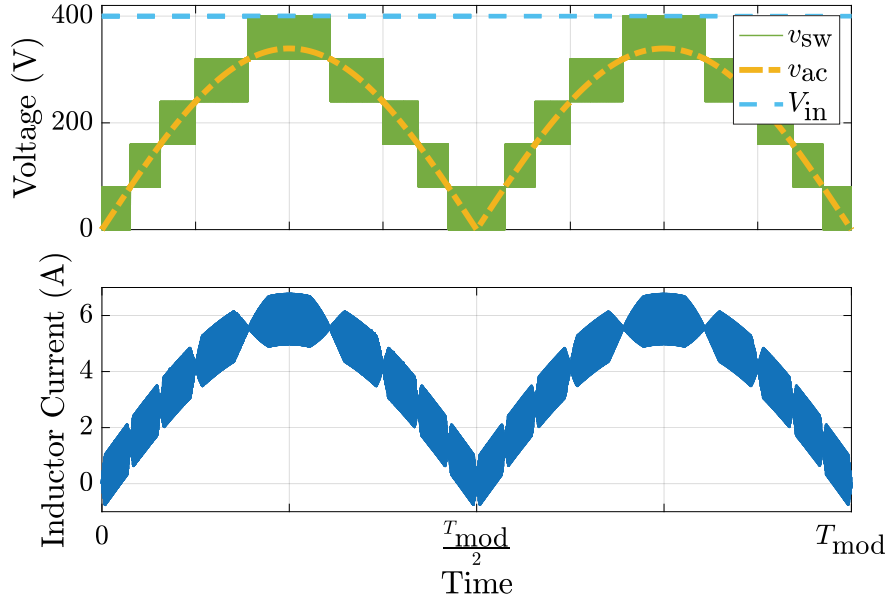


Figure 3.10: Calculated waveforms with the proposed technique at $V_{in} = 400$ V, $v_{ac} = 240$ V, $P_{out} = 1$ kW, $C_{fly} = 3$ μ F, $L = 22$ μ H, $C_{flt} = 300$ nF for an FCML with an unfold.

3.3 Hardware Implementation: Efficiency Monitoring

The experimental hardware prototype shown in Fig. 2.9 was used to validate the variable switching frequency implementation for $V_{\text{in}} = 400 \text{ V}$ and $v_{\text{ac}} = 240 \text{ V}_{\text{rms}}$ at 60 Hz up to 1450 W. The output inductor with inductance $L = 22 \mu\text{H}$ was chosen to achieve a maximum peak-to-peak current ripple of $\Delta i_{L,\text{pp}, \text{max}} = 1.81 \text{ A}$ at a switching frequency of 100 kHz. The converter parameters are described in Table 3.1.

The proposed variable switching frequency technique can be implemented with a digital signal processor (DSP). A TI C2000 MCU is used to generate the PS-PWM signals to control the FCML converter using the rated power level and modulation index D in open-loop operation. As shown in Fig. 3.11, the switching frequency is updated at the end of every switching cycle, and the phase shifts and duty cycle comparisons are synchronized concurrently. The C2000 code is detailed in Appendix B. Careful attention must be paid to ensure proper phase shifting between each switch pair.

In this work, the switching frequency was updated every switching period, making it possible to examine the full improvements achievable by operating at the lowest possible switching frequency while satisfying ripple constraints. In other applications it may be desirable to update the switching frequency more intermittently along the ac modulation cycle to minimize sampling and control complexity.

Fig. 3.12 shows measured conventional fixed switching frequency operational waveforms at an output power $P_{\text{out}} = 1 \text{ kW}$. The measured inductor current is consistent with the theoretical waveform in Fig. 3.3. Fig. 3.13 shows excellent matching between theory and the experimental waveforms for variable switching frequency operation at $P_{\text{out}} = 1 \text{ kW}$.

Table 3.1: Converter Operating Conditions

Parameter	Value
V_{in}	400 V
v_{ac}	240 V _{rms}
Measured P_{out}	55 - 1450 W
f_{sw}	40 kHz - 100 kHz
Grid frequency f_{line}	60 Hz
Derated C_{fly}	$\approx 3 \mu\text{F}$, paralleled 2.2 μF 450 V, C5750X6S225K250KA
FCML GaNFETs	150 V, 7 m Ω , EPC 2033
Unfolder GaNFETs	650 V, 50 m Ω , GS66508T
L	22 μH , IHLP8787MZER220M51
C_{flt}	300 nF, 630 V, CAA573C0G2J304J
Microcontroller	TI C2000 TMDSCNCD28379D

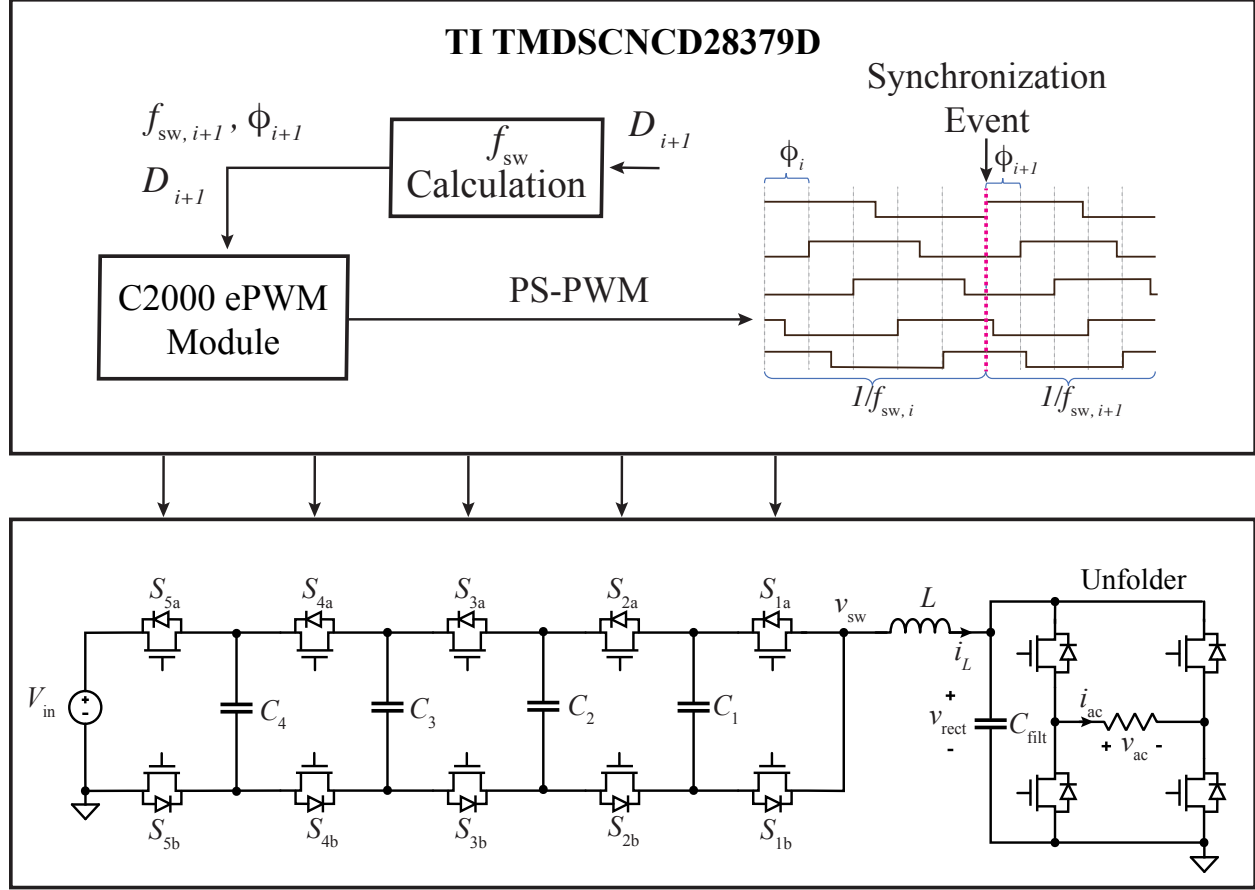


Figure 3.11: High-level diagram of microcontroller implementation. The output of the C2000 microcontroller is used to gate the FCML switches. In this figure, we show a single-ended 6 level FCML inverter with an unfolder such as the one in Fig. 2.9.

Flying capacitor voltage balancing according to the nominal dc voltage biases is required for converter operation. When the flying capacitor voltages are balanced, the switch-node voltage (v_{sw}) has a constant amplitude. For a dc-ac FCML converter, the switch-node voltage has distinct voltage steps as the duty cycle varies, but within each step this constant amplitude is maintained. Excellent balancing is observed in the clearly delineated voltage steps of v_{sw} in Fig. 3.13, and no imbalance is observed at any point across the measured load range.

Most notably, when f_{sw} is reduced during much of the ac modulation cycle, the overall efficiency of the converter improves. Efficiency measurements excluding gate-drive losses were taken with a Keysight IntegraVision PA2201A power analyzer. As shown in Fig. 3.14, the peak efficiency under fixed $f_{sw} = 100$ kHz operation was 98.8% at 1.009 kW. Under variable switching frequency operation with a minimum allowable switching frequency of 40 kHz, the

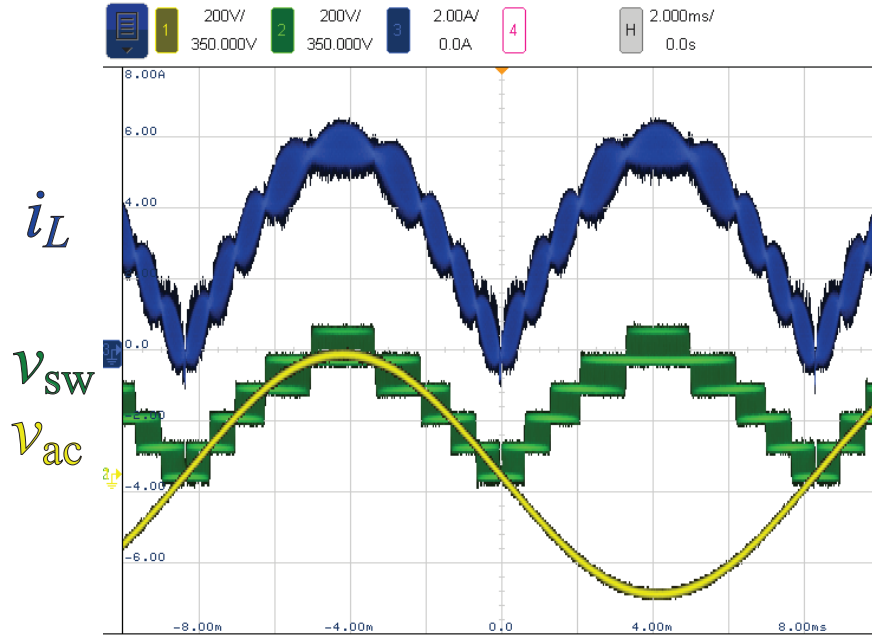


Figure 3.12: Oscilloscope plot of i_L , v_{sw} , and v_{ac} for fixed $f_{sw} = 100$ kHz.

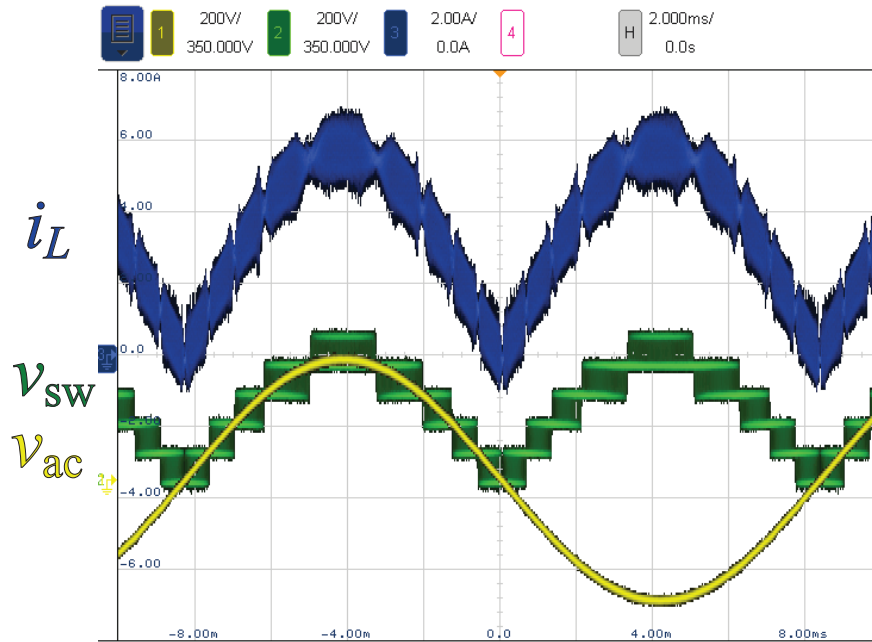


Figure 3.13: Oscilloscope plot of i_L , v_{sw} , and v_{ac} for variable $f_{sw} \in [40, 100]$ kHz].

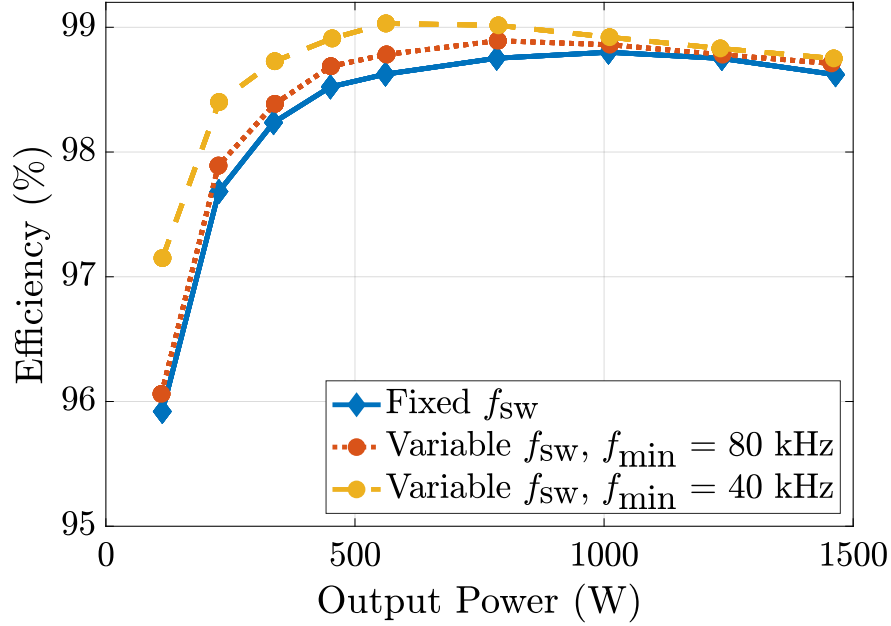


Figure 3.14: Plot of efficiencies for both fixed frequency and variable frequency operation.

peak efficiency reached 99.03% at 562 W. When the minimum switching frequency was limited to 80 kHz, the peak efficiency was 98.89% at 787 W. At the peak measured power, 1.45 kW, the efficiency was increased from 98.62% to 98.75% using the variable switching frequency scheme with a minimum limit set to 40 kHz. This corresponds to a 9.5% reduction in losses. At light load the improvements are even more dramatic. At an output power of 60 W, the efficiency increased from 91.86% to 94.73%, translating to a 35% reduction in losses.

An estimated loss breakdown for both operational modes at an output power of 1 kW is provided in Fig. 3.15 and shows that GaNFET switching overlap losses contribute significantly to the improvement in efficiency. Switching overlap losses were approximated using an average of the time-varying switching frequency and output current waveforms across half of an ac modulation cycle to capture the ac cycle variation in current. The expression for this approximation is given by (3.13), where v_{ds} is the nominal blocking voltage $\frac{V_{in}}{(N-1)}$ and the turn-on and turn-off times are denoted as t_{on} and t_{off} . These times are calculated according to manufacturer guidance [71].

$$P_{\text{overlap}} = \frac{2}{T_{\text{mod}}} \int_0^{T_{\text{mod}}/2} v_{ds} \cdot i_{ac}(t) \cdot f_{sw}(t) dt \cdot \frac{t_{on} + t_{off}}{2} \quad (3.13)$$

Conduction losses throughout the circuit are more simply captured by

$$P_{\text{cond}} = i_{ac, \text{rms}}^2 \cdot R. \quad (3.14)$$

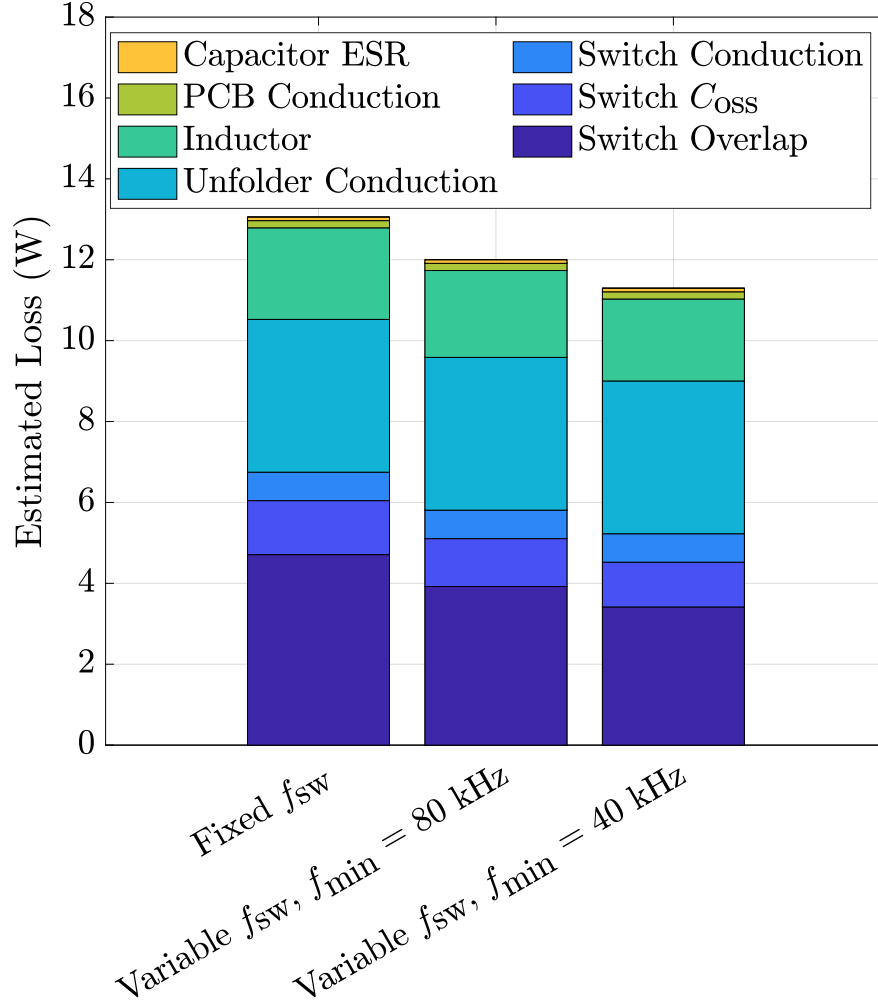


Figure 3.15: Estimated loss breakdown for operation at 1 kW. Results are broken down for a minimum switching frequency limit of both $f_{min} = 40$ kHz and $f_{min} = 80$ kHz. As expected, switching losses are substantially improved for the lower switching frequency case.

Inductor losses were approximated using manufacturer-provided models [72]. A key observation is that the reduction in average switching frequency does not drastically change the overall converter conduction losses. Subsequently, the control scheme is particularly impactful at lighter loads, resulting in the achievement of a peak efficiency at a lower power level than in the fixed switching frequency case. We also observe that as the lower limit for the switching-frequency scheme is increased, the power level at which the peak efficiency occurs is pushed upward. For a high-voltage, relatively low-current application, this would be a useful technique to recoup switching losses at lower power.

In Table 3.2, we compare this work to a few other variable switching frequency FCML inverter works. Loss reductions are afforded by these techniques compared to switching at

Table 3.2: Comparison of Variable Frequency Multilevel Inverter Works

Work	Constraints	Topology	Switching Freq.	Operating Conditions	Performance
This work	$\Delta i_L, \Delta v_c$	6-level FCML (1 ϕ)	40–100 kHz	$V_{dc} = 400$ V $V_{ac} = 240$ V _{rms}	Loss: 10–35% $\eta = 99\%$
[65]	i_L	3-level FCML (1 ϕ)	30–160 kHz	$V_{dc} = 400$ V $V_{ac} = 240$ V _{rms}	$\eta = 98.2\%$
[61]	Δv_c	3-level FCML (3 ϕ)	2.5–7.5 kHz	$V_{dc} = 500$ V V_{LN} not reported	Not reported
[62]	Δv_c	3-level FCML (3 ϕ)	7.8–10 kHz	$V_{dc} = 200$ V $V_{LN} = 77$ V _{rms}	Loss: 12.8%
[73]	Δv_c	3-level FC-NPC (3 ϕ)	4–10 kHz	$V_{dc} = 200$ V $V_{LN} = 70$ V _{rms}	Not reported

the maximum rated switching frequency. Notably, the 6-level FCML inverter in this work can achieve high efficiencies while switching faster than most of the other FCML inverter implementations. Some other prototypes in this table are 3-phase FCML inverter systems that switch much more slowly in part because they utilize different semiconductor devices, and thus have larger passive volumes. One other work uses a broad range (30 – 160 kHz) of switching frequencies to achieve ZVS across a wide load range [65].

Total Harmonic Distortion

There are additional considerations for grid-tied converters beyond efficiency, and power density. For many grid-tied applications, total harmonic distortion (THD) is required to be below 5% [53]. Moreover, many non-grid-tied inverters generally benefit from outputting well-filtered sinusoidal voltages. This is typically accomplished through a combination of operation with a small inductor current ripple and a relatively large output capacitance on the ac-side. To achieve small current ripple operation, it is required to employ either a large filter inductor or a high switching frequency. The measured output current at an output power of 1 kW is shown in Fig. 3.16 for both fixed- and variable-frequency operation. This current waveform was obtained through the measurement of the output voltage across a known resistive load of $R = 55.5 \Omega$ using a Keysight N2791A 25 MHz differential voltage probe. This measurement technique reveals a small change in high-frequency ripple magnitude between the two illustrated currents. The THD was computed from this measured current for comparative purposes. As shown in Fig. 3.17, which displays measured THD performance across the output power range, the variable switching frequency scheme does

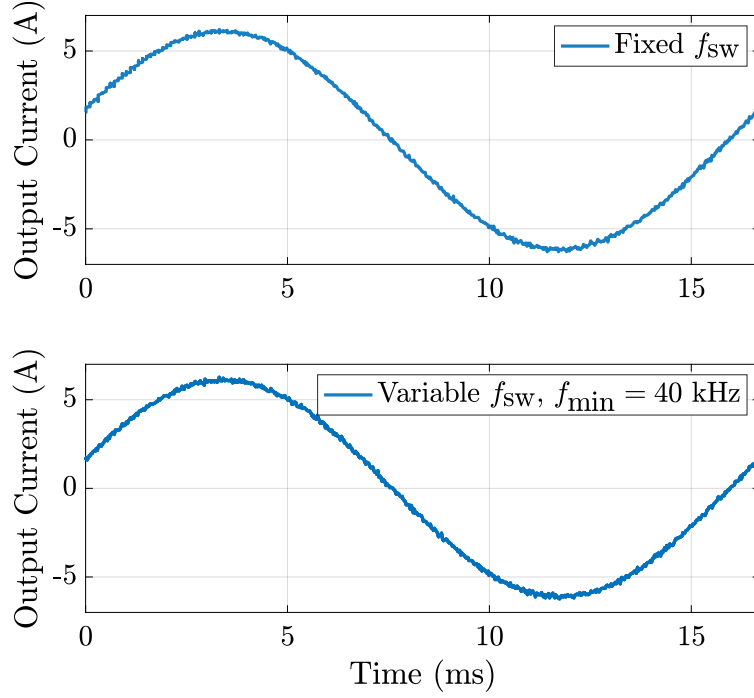


Figure 3.16: Output currents at 1 kW obtained by measuring output voltage across the same known resistive load of $R = 55.5\Omega$. This method enables the capture of high-frequency ripple content.

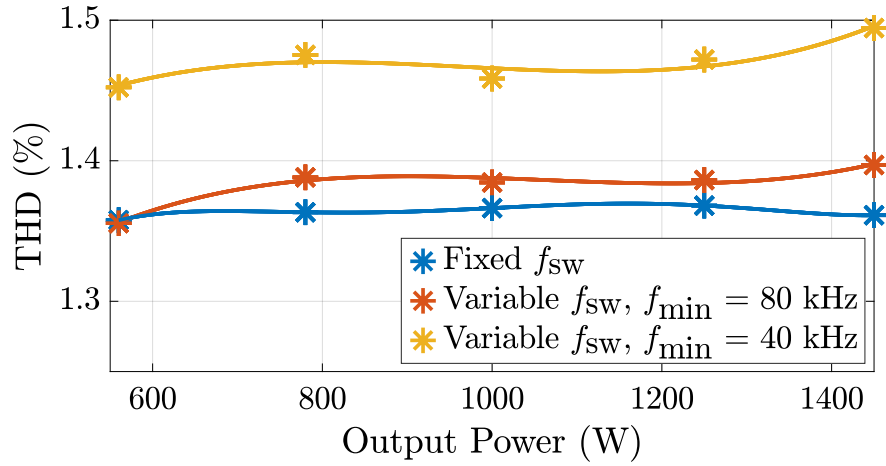


Figure 3.17: THD measurements at five points across a load range of 560 W – 1450 W for variable frequency operation with $f_{sw} \in [40, 100$ kHz], $f_{sw} \in [80, 100$ kHz], and fixed frequency operation at $f_{sw} = 100$ kHz.

incur a small THD penalty for the 6-level FCML prototype. However, this impact is marginal and more than offset by the efficiency improvements as outlined here.

3.4 Conclusion

This chapter outlines the theory and constraints for a variable frequency switching scheme for FCML inverters to enforce a constant inductor current ripple, along with a description of how to implement the theory in practice. The technique can be applied to any FCML dc-ac converter using common control inputs, and it can ultimately be used to drastically increase converter efficiency by lowering the average switching frequency input to each switch without violating passive component ripple ratings. A 6-level FCML inverter hardware prototype validates the approach and demonstrates significant efficiency improvements over conventional fixed switching frequency techniques. A peak efficiency of 99.03 % was achieved using the variable switching frequency technique. Efficiency improvements were observed across the measured load range of 60 W – 1.45 kW, where loss reductions on the order of 10 % – 35 % were measured.

Chapter 4

A Totem-Pole DC-AC FCML Converter for Improved Power Density

Executive Summary

This chapter introduces the use of an alternative dc-ac/ac-dc flying capacitor multilevel converter topology that reduces conduction losses in the low-frequency unfolded leg required of dc-ac converters. The “totem-pole” structure halves the number of grid-frequency switches in the converter. This is done at the expense of increased control complexity. The 400 V_{dc} to $240\text{ V}_{\text{rms}}$ converter presented in this chapter achieves a power density of 151 kW/L through the use of a 6-level FCML converter stage, two low-frequency FETs, and a compact PCB layout by Yayun Zhao. This collaborative project provides valuable insight through state-of-the-art hardware as to how multilevel converter structures and topological adjustments can push the limits of power density.

This chapter is based on collaborative work appearing in [74].

4.1 Introduction and Theory

In a conventional dc-ac/ac-dc circuit using a buck or boost stage, a grid-frequency rectifier or unfolded stage is required to convert between the sinusoid expected by the grid and a rectified sinusoidal voltage. In Chapter 2 and Chapter 3 the unfolded is realized as a full-bridge circuit operating at the line frequency. In this chapter, a collaborative piece of work that uses a topological change to improve system power density is highlighted.

In a conventional inverter with a low-frequency H-bridge leg, the switches operating at the grid frequency must be rated for the full grid voltage, resulting in the use of larger switches with higher on-state resistances [75]. One way to manage this trade-off is through the use

of a half-bridge circuit in lieu of the full-bridge leg to reduce both volume and MOSFET conduction loss. This “totem-pole” structure has been shown to improve power densities and efficiencies, but it requires additional considerations to operate [21, 45].

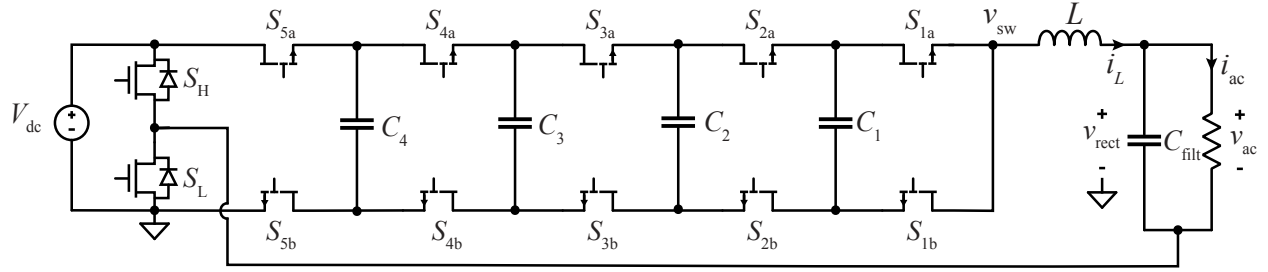


Figure 4.1: A 6-level FCML totem-pole inverter.

The FCML converter is configured as a totem-pole dc-ac converter, as shown in Fig. 4.1. The neutral line of the ac voltage input is connected at the midpoint of the half-bridge. The duty cycle and resulting voltage signals are shown in Fig. 4.2. The common-mode voltage transition between V_{dc+} and V_{dc-} at the zero crossing of the ac line voltage is showcased. It is useful to measure the rectified voltage waveform referenced to V_{dc-} , as this measurement highlights the large dv/dt events at the zero-crossing.

The design optimization framework presented in [67] was used to select the optimal converter level count. This framework considers the capacitor voltage ripple rating, inductor volt-seconds, the switching losses and volume, and the line-frequency switching devices. Using the resulting sweep of possible designs, converter volume and efficiency are predicted. From these generated designs, a Pareto front is developed to examine the tradeoffs between efficiency and power density, and a 6-level FCML totem-pole converter is shown to be the most promising solution.

This work builds on previous totem-pole FCML converter works [44–46, 48, 49, 76], but specifically emphasizes the achievement of a state-of-the-art power density for an FCML converter utilizing a totem-pole leg to convert between dc-ac/ac-dc.

4.2 Hardware Results

A hardware prototype of the bidirectional totem-pole FCML converter was designed and constructed by Yayun Zhao to evaluate its performance. The prototype, shown in the annotated photograph in Fig. 8.9, was designed for a 350 - 400 V dc bus and a 240 V_{rms} ac port, and it achieves a full-load power of 3.24 kW. This prototype uses a compact layout suitable for GaN-based power conversion. The silicon MOSFETs used for the low-frequency leg have an on-state resistance $R_{ds,on} = 10 \text{ m}\Omega$ and are chosen to limit conduction losses compared to 650 V GaN devices, which typically have on-state resistances $\geq 25 \text{ m}\Omega$. Table 4.2 details the selected components of the converter.

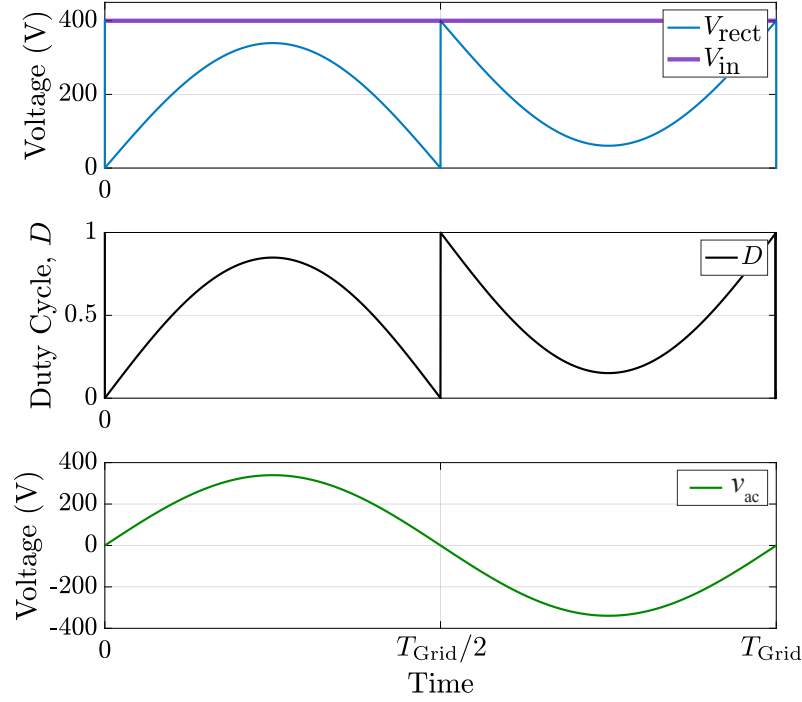


Figure 4.2: Key voltage waveforms for the totem-pole FCML inverter. Here, S_L conducts from 0 to $T_{\text{grid}}/2$ and S_H from $T_{\text{grid}}/2$ to T_{grid} .

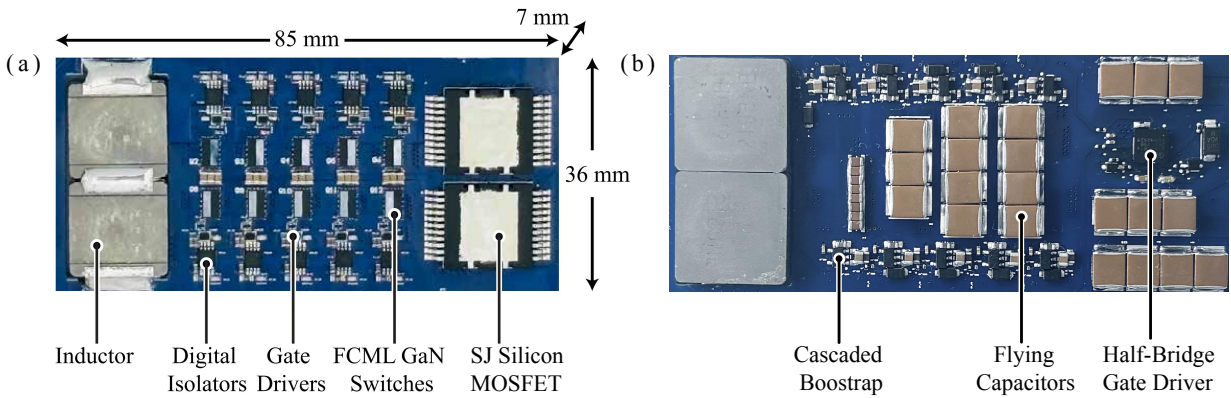


Figure 4.3: (a) Top side and (b) bottom side of the hardware prototype. Figure credit: Yayun Zhao.

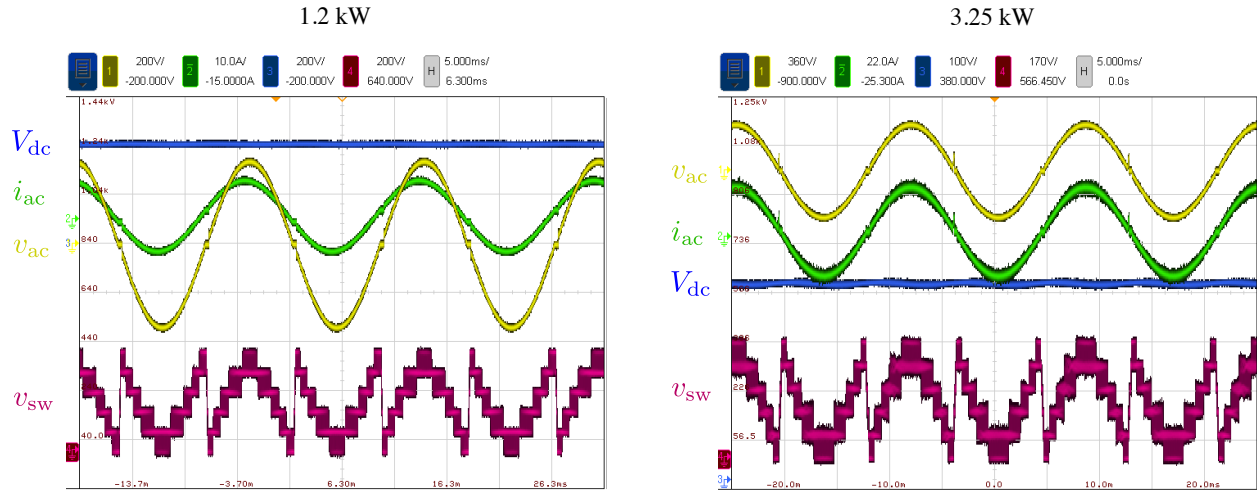


Figure 4.4: a) Inverter operating waveforms at $V_{dc} = 400$ V and $v_{ac} = 240$ V_{rms} showcasing the switch-node voltage waveform as well as the clean ac-side voltage and current at 1.2 kW. b) Inverter operating waveforms at $V_{dc} = 400$ V and $v_{ac} = 240$ V_{rms} showcasing the switch-node voltage waveform as well as the ac-side voltage and current at 3.25 kW.

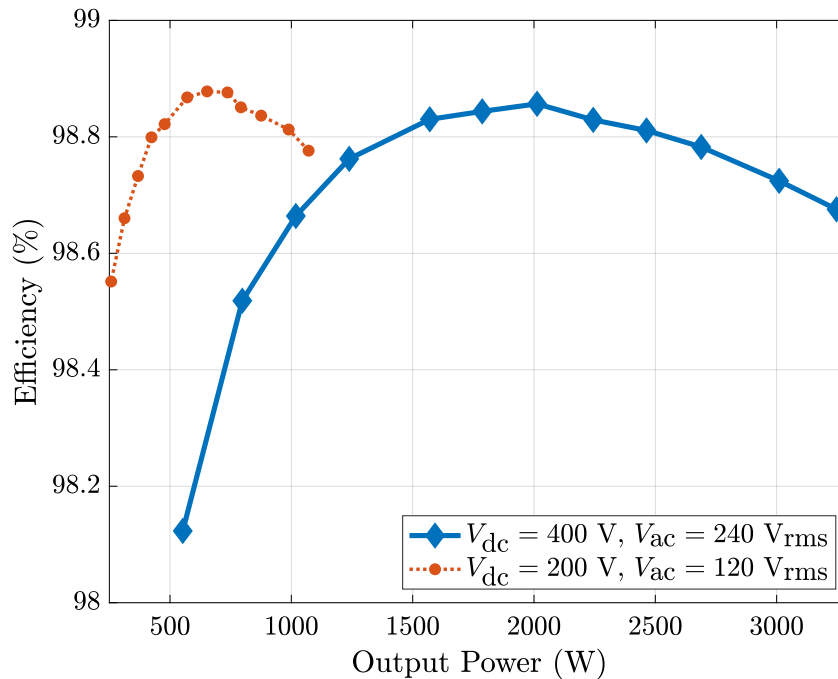


Figure 4.5: Measured efficiency curve under both 240 V_{rms} and 120 V_{rms} ac output conditions. A peak efficiency of 98.86% is recorded in the 240 V_{rms} case. At the full load of 3.24 kW, the converter achieves an efficiency of 98.67%. Figure credit: Yayun Zhao.

Table 4.1: Converter Operating Parameters

Parameter	Value
V_{dc}	350–400 V
v_{ac}	240 V _{rms}
P_{ac}	3.24 kW
f_{sw}	100 kHz
C_{fly}	2 μ F
L	13.6 μ H

Table 4.2: 6-Level FCML Totem-Pole DC-AC Hardware Prototype Component Listing

Component	Part Number	Parameters
Controller	TI TMS320F28379D	
GaN Switches ($\times 10$)	EPC2305	150 V, 2.2 m Ω
SJ Silicon MOSFET ($\times 2$)	Infineon IPDQ60R010S7	600 V, 10 m Ω
Flying Caps – 100 V ($\times 8$)	TDK C2012X5R2A475K125AC	4.7 μ F
Flying Caps – 450 V ($\times 11$)	TDK C5750X6S2W225K250KA	2.2 μ F
Decoupling Caps ($\times 15$)	TDK C2012X7T2W473K125AA	47 nF, 450 V
Inductor ($\times 2$)	Vishay IHL6767	6.8 μ H
Bootstrap Diode ($\times 9$)	Vishay 2EQH02HM3/H	200 V
LDO ($\times 10$)	TI LP2985AIM5X-5.0	5 V, 150 mA
GaN Gate Driver ($\times 10$)	TI LMG1020	5 V, 7A/5A
MOSFET Gate Driver ($\times 1$)	Infineon 2EDF7275K	
Operational Amplifier ($\times 2$)	TI OPA2350UA/2K5	
Current Sense Amplifier ($\times 1$)	ADI LT1999CS8-20PBF	

Measured inverter operating waveforms at $P_{out} = 1.2$ kW are shown in Fig. 4.4. We see that the switch-node voltage waveform has clearly delineated steps indicating balanced operation. The THD across the load range was measured to be below 2.5%. The converter efficiency, including gate drive losses, is presented in Fig. 4.5 at a conversion from both 200 V to 120 V_{rms} and 400 V to 240 V_{rms}. Efficiency measurements were taken using a Keysight PA2201A power analyzer. A peak efficiency of 98.86% is recorded in the 240 V_{rms} case. At the full output power of 3.24 kW, the converter achieves an efficiency of 98.67%. The converter achieves a state-of-the-art power density of 151 kW/L.

Compared to the hardware prototype in Chapter 2, this prototype uses substantially reduced flying capacitance to achieve a higher volumetric power density. It should be noted that the peak flying capacitor voltage ripple can be estimated by (4.1).

$$\Delta v_{C,pp} = \frac{|i_{ac}| \big|_{D=(N-2)/(N-1)}}{(N-1)f_{sw}C_{fly}} = \frac{17.9 \text{ A}}{5 \cdot 100 \text{ kHz} \cdot 2.2 \mu\text{F}} = 16.3 \text{ V}. \quad (4.1)$$

From (4.1), this design can be identified as one that has a moderate ripple, especially considering that each switch must block 80 V. At heavy load, we observe that the switch-node voltage waveform has higher ripple content in Fig. 4.1b. In Chapter 6, we discuss some implications for this capacitor ripple design decision and how it relates to expected electromagnetic interference performance.

4.3 Conclusion

This chapter briefly presents a 6-level flying capacitor totem-pole dc-ac/ac-dc converter that can achieve a power density exceeding 2480 W/in³ or 151 kW/L, and a peak efficiency of 98.86%. Hardware results taken for dc-ac operation experimentally validate the proposed converter and establish a state-of-the-art power-density benchmark. The prototype achieves an efficiency of 98.67% at a 3.24 kW full load, while achieving 2483 W/in³ power density and 98.86% peak efficiency. The presented prototype achieves higher power density and efficiency than the inverter presented in Chapters 2 and 3, and highlights how topological adjustments can improve hardware performance.

Chapter 5

Applications of FCML Converters: Meeting Future Power Conversion Challenges

Executive Summary

In this chapter, the FCML converter is merged with an isolated converter topology for a high-step-down conversion from 800 V to 53 V. This converter achieves a peak efficiency of 96.5% at 550 W, highlighting the applicability of the FCML converter to systems requiring isolation [77]. This chapter highlights the effective design of the rectifier in the converter topology, which includes parallelized GaN devices used to reduce conduction losses while switching at 200 kHz. The overall converter topology is a timely exploration, as an 800 V dc bus is a recent update in both automotive and data center applications.

This chapter is based on collaborative work spearheaded by Sahana Krishnan, and appears in [77].

5.1 The Burgeoning 800 V Bus

Although the 400 V dc bus has been a long-standing element in the automotive industry and in the dc-link of data centers, new levels of demand require a shift to a higher voltage input. Moving to a higher voltage can reduce conduction losses in the cabling for a given power level through a reduction in current, enabling the delivery of higher power to demanding loads at higher efficiencies. Subsequently, the 800 V bus has begun to appear in passenger electric vehicles [78, 79], and data centers [80, 81].

In 800 V step-down applications, isolation is typically required to ensure safety for those working on low-voltage systems in the electrical environment and to prevent damage to the

low-voltage electrical system. Galvanically isolated topologies leverage transformers for the isolation barrier. These magnetic structures are often large and lossy, incentivizing the use of switching stages that are compact and efficient to compensate [12, 82, 83].

The efficiency and power-density benefits of the FCML converter have previously been applied to some isolated power converter topologies [84]. The use of the multilevel converter structure enables the use of high FOM, low-voltage semiconductor devices [75], and can offer improvements in a topology using galvanic isolation. In this chapter, the FCML converter is merged with a dual active bridge (DAB) converter, which is a galvanically isolated dc-dc converter. Under typical operation in single-phase-shift modulation, the DAB converter comprises a high-frequency square-wave inverter, a transformer, and a high-frequency square-wave rectifier. This merged topology provides isolation and leverages the benefits of a multilevel power converter architecture.

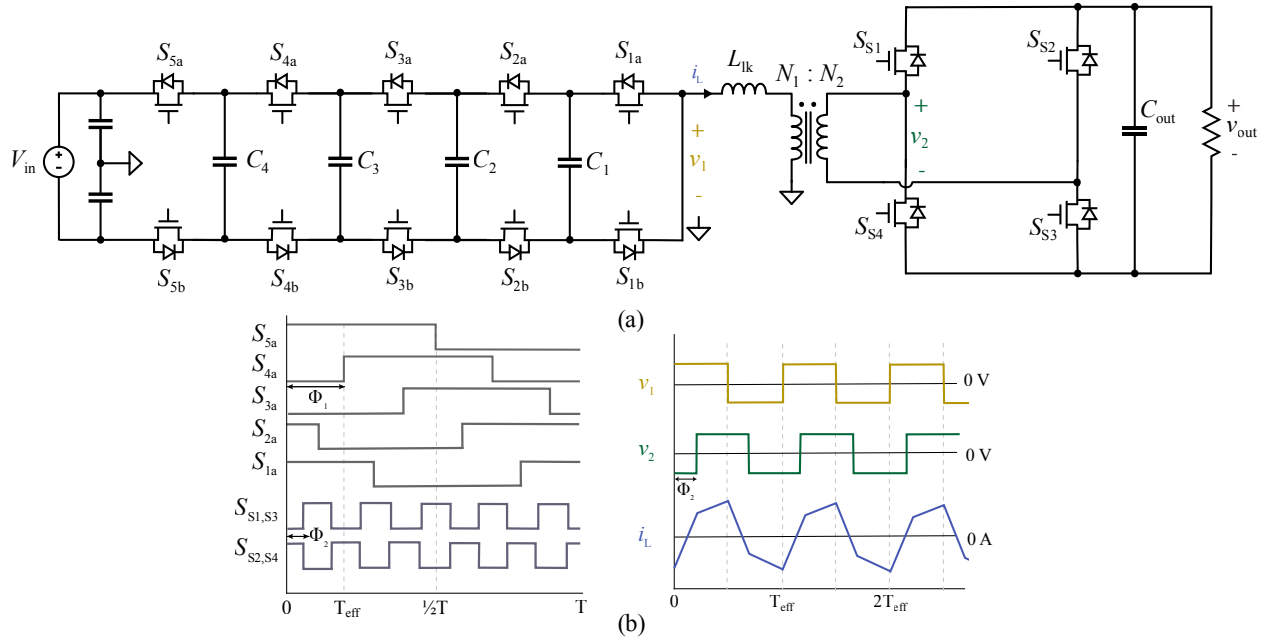


Figure 5.1: Schematic of the proposed 6-level FC-DAB topology. Gating signals are shown for the switches, and key voltage and current waveforms are also shown. Figure made in collaboration with Sahana Krishnan.

5.2 An Isolated FCML Converter Topology

The proposed topology is shown in Fig. 5.1. The circuit consists of a split-bus 6-level FCML converter on the primary side of the transformer, which generates a square wave at a frequency of $f_{eff} = (N - 1)f_{sw}$ under nominal PS-PWM operation. With a duty cycle

of $D = 0.5$, the FCML stage creates a primary-side voltage that is a square wave with magnitudes defined by $v_1 = \pm \frac{V_{in}}{2(N-1)}$.

On the secondary side of the transformer, a rectifier converts the square wave voltage v_2 to a dc voltage. The rectifier in the FC-DAB converter is switched at the FCML converter's effective frequency f_{eff} . Under single phase-shift operation, the secondary side gate signals are shifted by a phase shift ϕ_2 from the primary side switch-node waveform. This enables the flow of power, which is controlled by the magnitude of the leakage inductance of the transformer. The magnitude of this power for the FC-DAB topology is defined by (5.1).

$$P_{out} = \frac{V_{out} \frac{V_{in}}{2(N-1)}}{2\pi^2 L_{lk} f_{eff}} \cdot \frac{N_1}{N_2} \cdot \phi_2(\pi - \phi_2) \quad (5.1)$$

From (5.1), a relationship between level count, the effective frequency, and the turns ratio is observed that makes it imperative to develop an understanding of the tradeoffs between FCML level counts and feasible output powers. This tradeoff was considered in [77], and the 6-level FCML converter was shown to provide an optimal balance between efficiency and power density.

5.3 Hardware Implementation

The switching stages of the 800-to-53.3 V prototype is shown in Fig. 5.2 with labeled components. Each of the power stages was designed with GaNFET switches on separate PCBs to enable modularity in testing the overall high-voltage system. All major components are described in Table 5.1.

Table 5.1: Key Components of the FC-DAB Hardware Prototype

Component	Mfr. & Part Number	Parameters
Primary Side: FCML		
Switches $S_{1a}-S_{5b}$	EPC EPC2304	GaN, 200 V, 5 mΩ
Flying Capacitance C_1-C_4	TDK C5750X6S2W225K250KA	2.2 μF, 450 V
Decoupling Capacitance	Kemet C1206C103KFRACU	10 nF, 1500 V
Level Shifter	Texas Instruments SN74LV4T125PWR	Buffer, non-inverting
Isolator	Analog Devices ADuM5240ARZ	2-channel, unidirectional
Gate Driver	Texas Instruments LM5114	Low-side driver
Secondary Side: Rectifier		
Switches $S_{S1}-S_{S4}$	EPC EPC2302	GaN, 100 V, 1.8 mΩ
Digital Isolator	NVE IL711-3E	2-channel, unidirectional
Gate Driver	Texas Instruments LM5114	Low-side driver
Bootstrap Diode	Diodes Inc. MBR0580S1-7	Schottky, 80 V, 500 mA

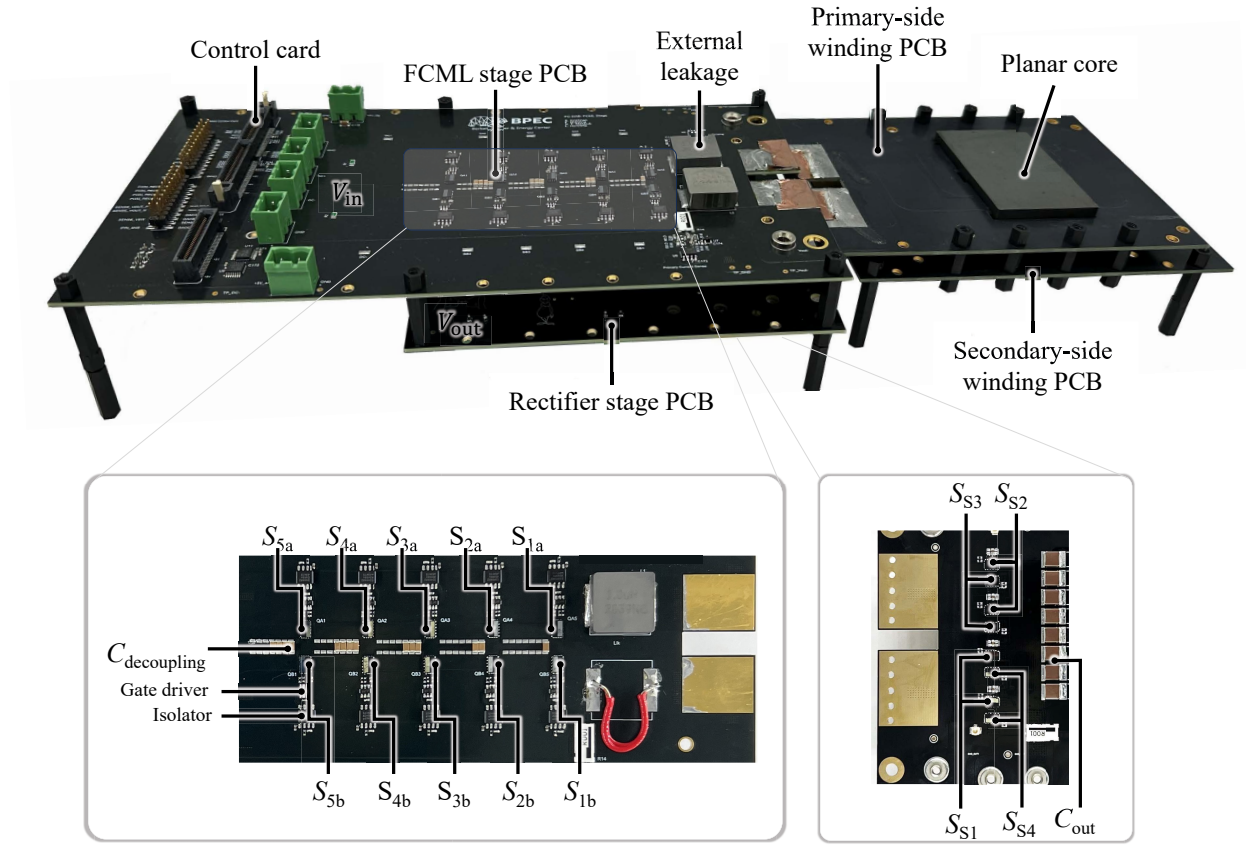


Figure 5.2: Hardware prototype showing the full system assembly, including the planar transformer. Insets with each of the labeled switching stages are shown. Figure made in collaboration with Sahana Krishnan.

My contribution to the system-level prototype was the full design of the secondary-side rectifier. This prototype uses parallelized 100 V GaN switches. A tight decoupling strategy is employed to reduce commutation-loop inductance for parallelized GaN devices. This decoupling is essential, as ringing from rectifier switching will be reflected via the transformer to the primary-side switch node. Moreover, the rectifier is switched at $f_{\text{eff}} = 200 \text{ kHz}$, a frequency that incentivizes tight PCB layout.

To achieve a tight commutation loop, each parallel device is placed in its own half-bridge circuit with the complementary switch. In this configuration, four identical half-bridges are designed, similar to the approach in [85]. The concept behind this split commutation loop is shown in Fig. 5.3 for a parallelized half-bridge. Measured voltages for v_1 and v_2 are shown in Fig. 5.6, and highlight the importance of mitigating ringing in the rectifier. The fast switching transitions excite parasitic inductance and capacitance in the transformer, which results in some ringing on the primary side of the converter [86]. A secondary-side power

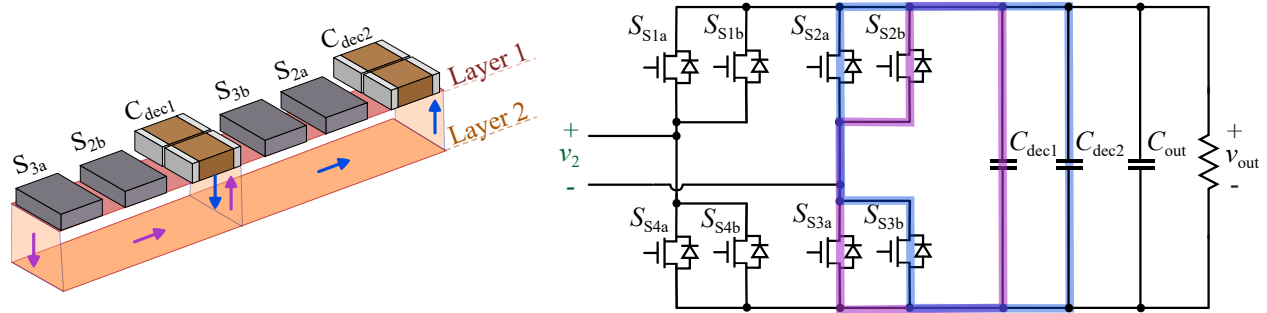


Figure 5.3: Secondary-side rectifier with parallel GaNFETs and the intended commutation loops for each pair of switches. Figure credit: Sahana Krishnan.

stage with a poor layout and high commutation loop inductances will have higher ringing and overshoot, which can worsen parasitic excitations and, subsequently, the ringing observed on the primary side. However, this ringing was sufficiently managed by the converter design choices.

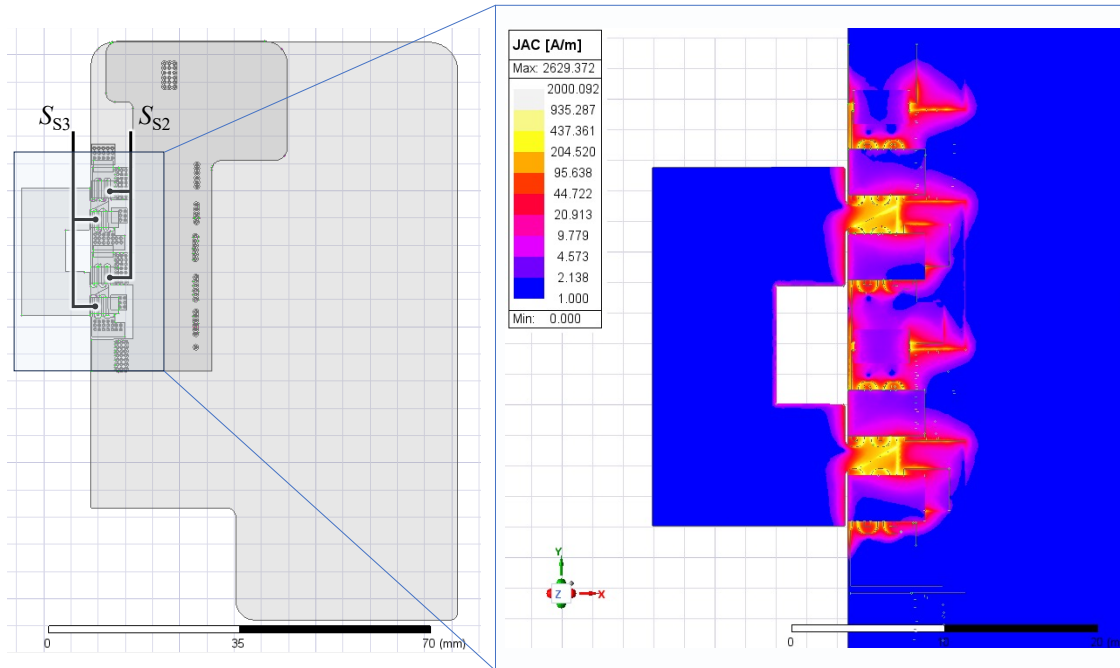


Figure 5.4: Simulation of one half-bridge in ANSYS Q3D. An inset is shown for the computed current density, and highlights good symmetry between each parallel switch.

To verify the effectiveness of the proposed decoupling strategy, parasitic extraction for a single half-bridge was performed in ANSYS Q3D to ensure that each half-bridge with

decoupling capacitors had evenly matched parasitic resistance and inductance. Furthermore, the full commutation-loop inductance and resistance are estimated for the parallel system. The PCB design in the ANSYS Q3D environment is shown in Fig. 5.4. Parallel switches S_{S2} and S_{S3} are labeled as well. An inset showing the current-density plot highlights good symmetry and expected circuit behavior. The commutation-loop inductance is plotted against frequency in Fig. 5.5. This design highlights a commutation-loop inductance below 0.6 nH per paralleled half-bridge in the rectifier. Good matching is observed between the self-inductances and resistances of each parallel branch, which is critical in ensuring current sharing.

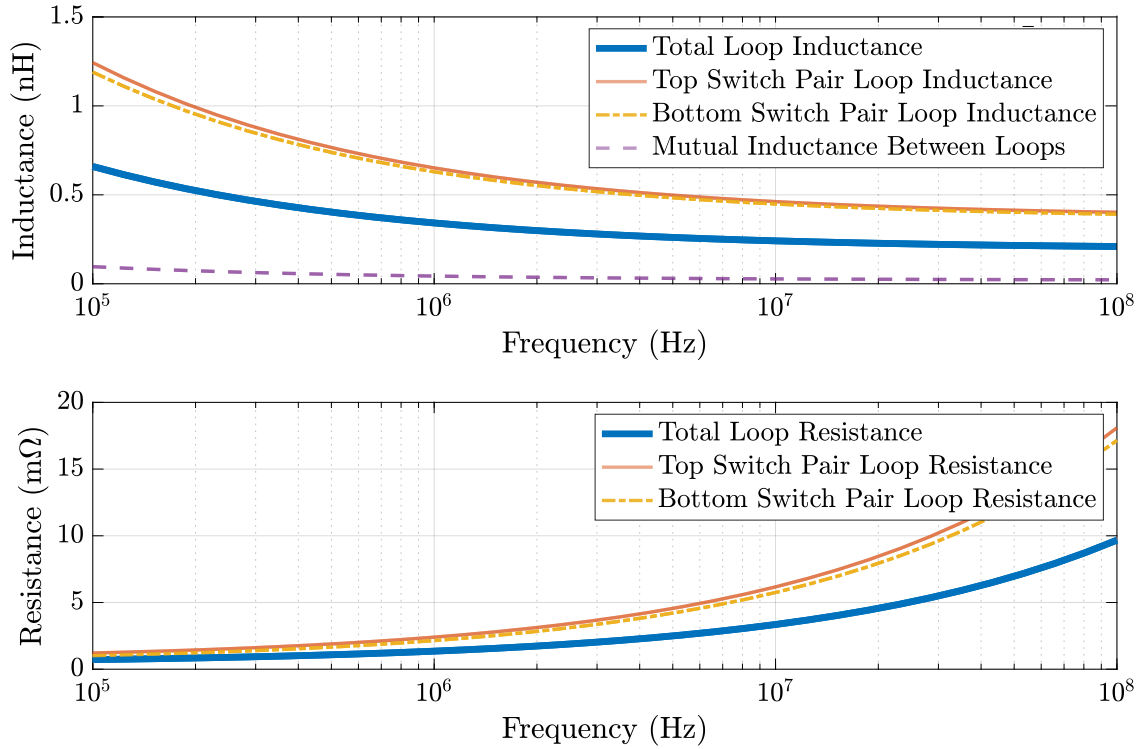


Figure 5.5: The top plot shows the estimated commutation-loop inductance, as well as the inductance measured in each half-bridge leg. The full half-bridge has a commutation loop inductance between 0.2 nH and 0.6 nH. The bottom plot shows the estimated parasitic resistance present in the layout, which is below 10 mΩ across the frequency range.

As shown in Fig. 5.2, the hardware prototype places the high-performance rectifier below the FCML converter stage. The hardware achieves a peak efficiency of 96.5% at 550 W, and a peak power of 700 W. Efficiencies across the load range were above 95%, which is very competitive for a step-down ratio of 15 : 1. These hardware results highlight the usefulness of the multilevel architecture applied to an isolated topology.

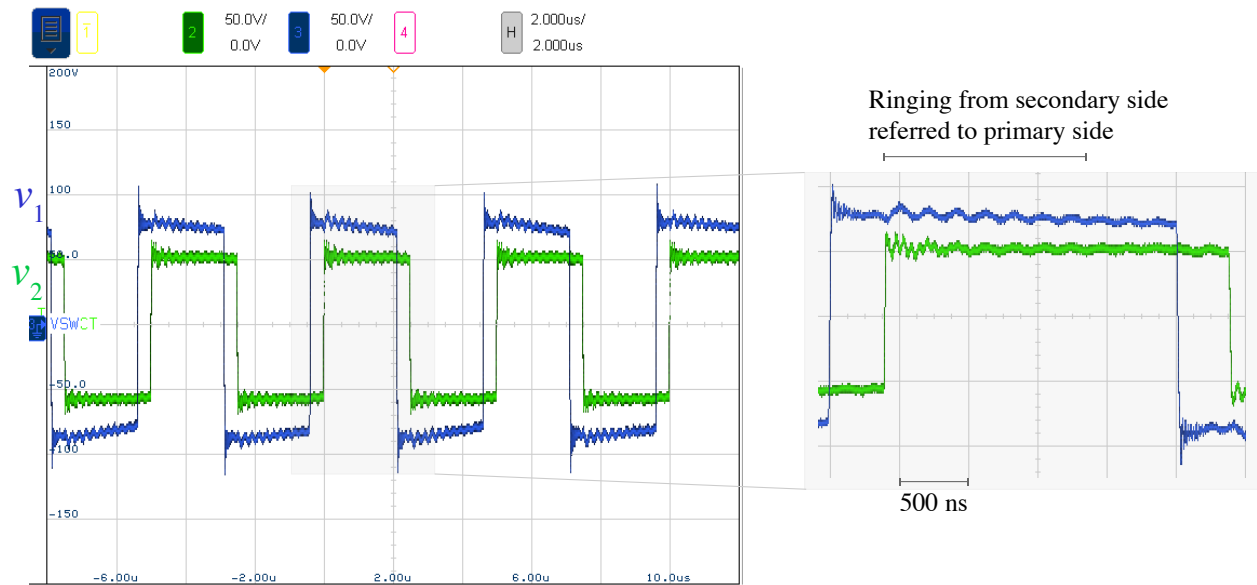


Figure 5.6: Oscilloscope voltage waveforms for v_1 and v_2 at 800 V in, and 53.3 V out at 700 W, showcasing the importance of good commutation-loop design on the secondary-side rectifier.

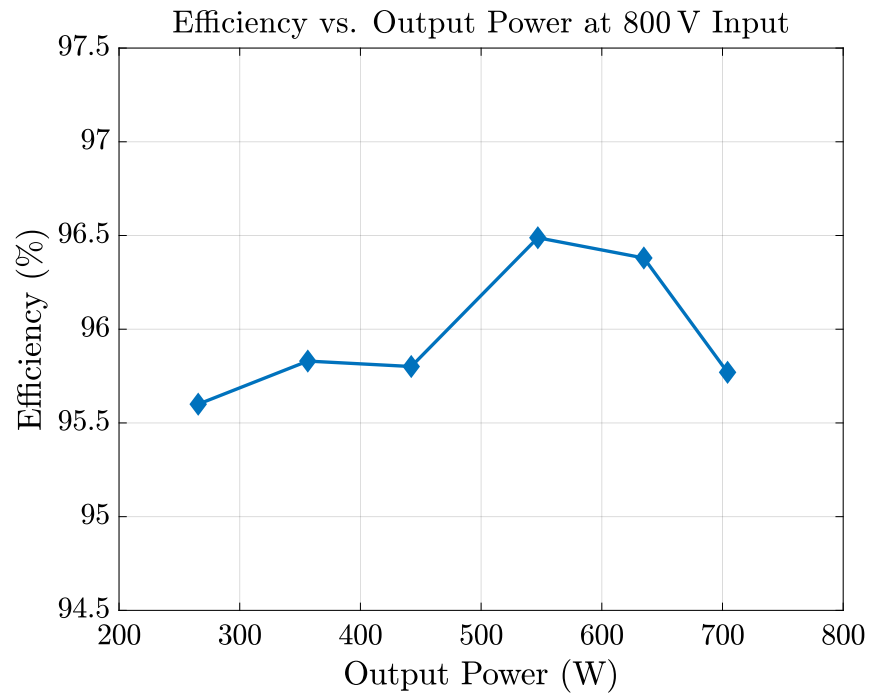


Figure 5.7: Efficiency measurements across the load range of the FC-DAB hardware prototype at an input voltage of 800 V. Figure made in collaboration with Sahana Krishnan.

5.4 Concluding Remarks

This chapter highlights the product of a collaborative project. Here an 800 V to 53.3 V FC-DAB converter is proposed and validated in hardware. The converter achieves high efficiencies, and creates new opportunities for innovation in the isolated multilevel converter design space. Each converter stage was designed on a separate PCB, enabling development of competitive solutions for each.

Part II

Conducted Electromagnetic Interference in the Flying Capacitor Multilevel Converter

Chapter 6

An Overview of Differential-Mode Electromagnetic Interference in FCML Converters

Executive Summary

This chapter provides an introduction to conducted electromagnetic interference (EMI) in power converters. EMI can result in system-level damage of connected equipment, and is an important consideration in power converter design and deployment. First, this chapter provides a general introduction to EMI and how it is measured. Then, this chapter characterizes differential-mode EMI for the FCML converter, which is the type of conducted EMI that is intrinsic to converter operation. We conclude by identifying the unique EMI signatures that differentiate FCML converter operation from standard two-level architectures, and how these signatures may influence design decisions.

This chapter references work and a model presented in [87] to better explain differential-mode EMI on the output side of an FCML buck converter.

6.1 Conducted Electromagnetic Interference Background

Conducted electromagnetic interference (EMI) describes the frequency content flowing at either the input or output of the converter. While it is intrinsic to converter operation, conducted EMI can damage connected equipment if not properly mitigated. Conducted EMI is split into two components: differential- and common-mode EMI. Differential-mode (DM) EMI describes the frequency content resulting from power flow around the main power path of the circuit, and is intrinsic to converter operation. DM EMI arises predominantly as a result of di/dt events and is worsened by stray inductances in the circuit. Common-mode

(CM) EMI occurs as a result of parasitic capacitances throughout the circuit—in particular, capacitances to ground, which are frequently encountered in converters with power-device heatsinks to a grounded chassis. These capacitances provide leakage paths for common-mode currents, which are driven by dv/dt switching events. Because these capacitances are formed by unavoidable non-idealities such as semiconductor devices with non-zero die area or large high-frequency copper planes in a PCB, CM EMI cannot be avoided in practical converter implementations. Both CM and DM EMI are shown conceptually in Fig. 6.1. In this figure, we highlight the power path that generates DM EMI, and the leakage paths from the power stage that result in CM EMI.

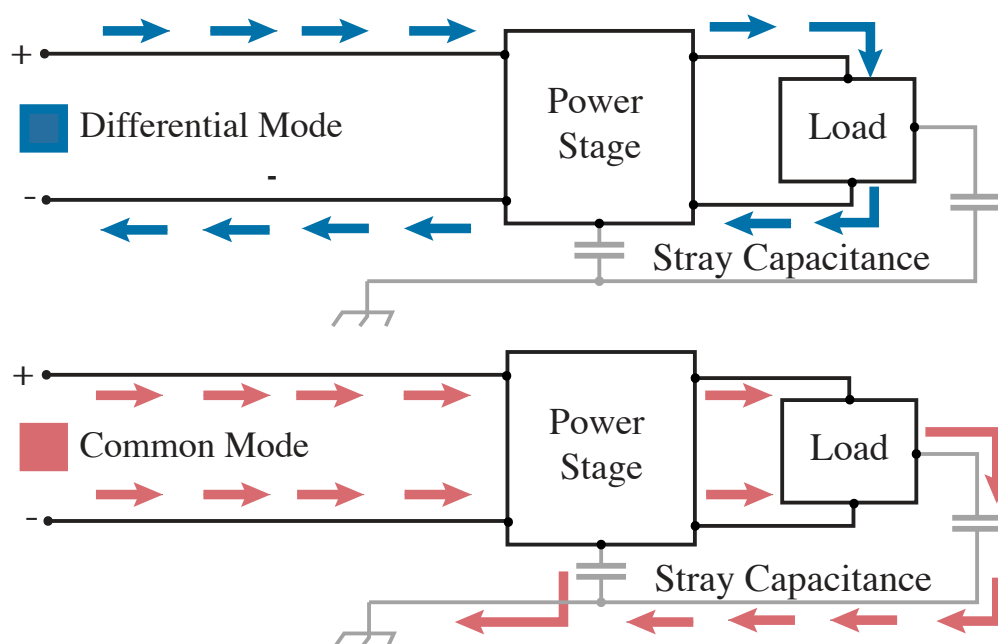


Figure 6.1: Schematic showing the generation of differential-mode and common-mode EMI in a converter stage.

For a 2-level buck converter, we show the generation of common-mode and differential-mode EMI in Fig. 6.2. The line impedance stabilization networks (LISNs) used to measure EMI are shown in this diagram as well. These LISNs provide a consistent impedance that we can reference this frequency content to. In this circuit schematic, differential-mode EMI is shown to flow around the main power path of the converter. Common-mode EMI is shown here to be generated from parasitic capacitance referenced to the source of the high-side FET. This capacitance may be generated as the result of a heat sink placed on the switch [88–94]. Illustratively, top-cooled switches are electrically connected to the source or drain on the top of the device. The placement of a gap pad and a heat sink on top creates a plate capacitance referenced from the device to the heat sink ground. This capacitance is proportional to the conductive external area of the device, as shown in Fig. 6.3. This

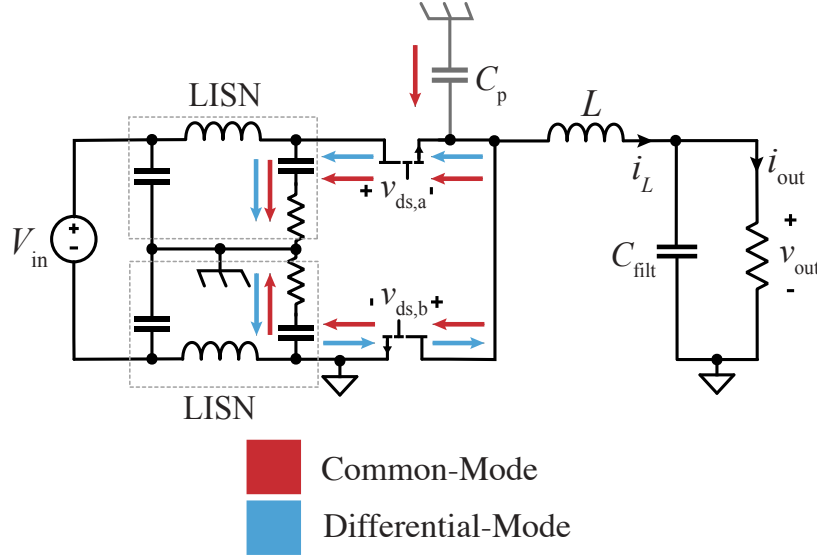


Figure 6.2: Schematic of a buck converter showing the parasitic capacitance at the switch node resulting from the die area. Common-mode and differential-mode EMI are shown via arrows.

capacitance can be estimated as

$$C_p \approx \frac{\epsilon_o \epsilon_r A_{device}}{d}, \quad (6.1)$$

where A_{device} is the thermal cooling area, ϵ_o is the permittivity of free space, ϵ_r is the specific permittivity of the thermal interface material (TIM), and d is the distance between the FET and the heat sink, and is determined by the TIM or gap pad thickness.

Because conducted EMI resulting from converter operation poses a threat to connected equipment, it is a stringently regulated phenomenon. In Table 6.1, we showcase a subset of EMI standards with conducted emissions limits. This table includes where these standards apply geographically, as well as the corresponding application space. The frequency range in the table refers to the frequency range associated with conducted EMI limits.

In Figure 6.4, we showcase the major components of a pre-compliant benchtop setup for EMI measurements. In this diagram, input-side EMI is being measured. The converter is placed on metal ground shields, to which the LISN ground is referenced. A circuit schematic for conventional 5 μ H LISNs is shown. The voltage across the 50 Ω terminals for each LISN is measured and fed through the through-capacitance to a spectrum analyzer. The two-LISN setup does enable the simultaneous measurement of conducted emissions on both the high- and low-side inputs to the converter. However, to distill the DM and CM spectra, an additional step is required. A TBLM1 LISN Mate from Tekbox is connected to both LISNs, and the signals from the two LISNs are either directly summed for CM EMI or subtracted (phase-shifted then summed) for DM EMI. The spectrum analyzer is then directly connected

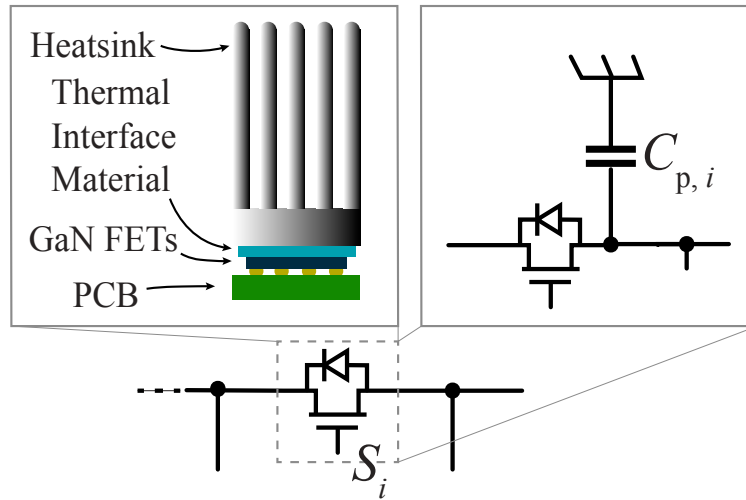


Figure 6.3: Diagram showing the generation of a parasitic capacitance as a result of the addition of a grounded heatsink.

Table 6.1: Common EMI Standards for Power Electronics Systems

Standard	Region	Application	Conducted Freq. Range
FCC Class A/B [95]	USA	Consumer electronics in industrial (Class A) and residential (Class B) environments (equivalent to CISPR 32)	150 kHz–30 MHz
CISPR 32 [96]	Intl./EU	Multimedia equipment (replaces CISPR 22)	150 kHz–30 MHz
CISPR 11 [7]	Intl./EU	Industrial, scientific, medical equipment	150 kHz–30 MHz
CISPR 14 [8]	Intl./EU	Household appliances and tools	9 kHz–30 MHz
CISPR 25 [10]	Intl./EU	Vehicles, boats, and internal combustion engines	150kHz–108 MHz
IEC 61000-6-3 [97]	Intl./EU	Emissions standard for residential environments	150 kHz–30 MHz
IEC 61000-6-4 [9]	Intl./EU	Emissions standard for industrial environments	150 kHz–30 MHz
MIL-STD-461 [98]	USA	Military equipment EMI requirements	30 Hz–10 MHz

to the desired CM or DM port on the TBLM1 LISN Mate, while the other port is terminated with 50Ω . The key measurement tools are shown in Table 6.2.

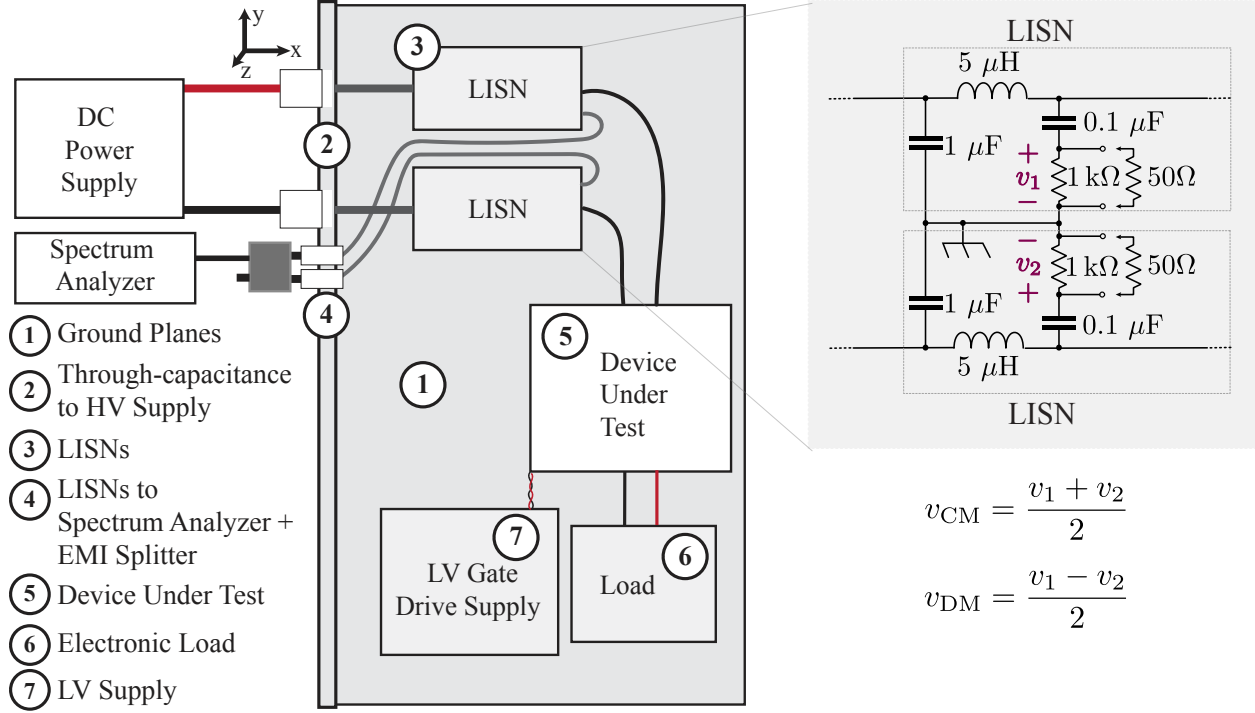


Figure 6.4: Diagram of a pre-compliant EMI test bench. Here, example $5\mu\text{H}$ LISN passive component values are defined [99], as are the expressions for CM and DM EMI from the measured LISN voltages.

Table 6.2: Key Components of EMI Benchtop Setup Used in This Work

Component	Part Number
LISNs	Solar Electronics Company 21702-5-TS-50-N
EMI Splitter	Tekbox TBLM1 LISN Mate
Spectrum Analyzer	Tektronix RSA306B

In this work, we do not seek EMI compliance as a specific outcome, but are more concerned with scaling trends, and the relative impact of various EMI mitigation techniques. The available test bench and equipment are only appropriate for pre-compliant testing. The overarching goal of the work presented in this section is 1) the fundamental characterization of EMI in the FCML converter and 2) the demonstration of effective EMI peak mitigation

by variable frequency control. For this reason, the hardware validations for EMI in this work do not include additional attenuation via passive filtering.

6.2 Differential-Mode EMI in the FCML Converter

We begin the discussion of EMI in the FCML converter by investigating DM EMI. Because DM EMI is intrinsic to converter operation, understanding it in the FCML converter is a matter of describing the input/output voltages and currents of the converter.

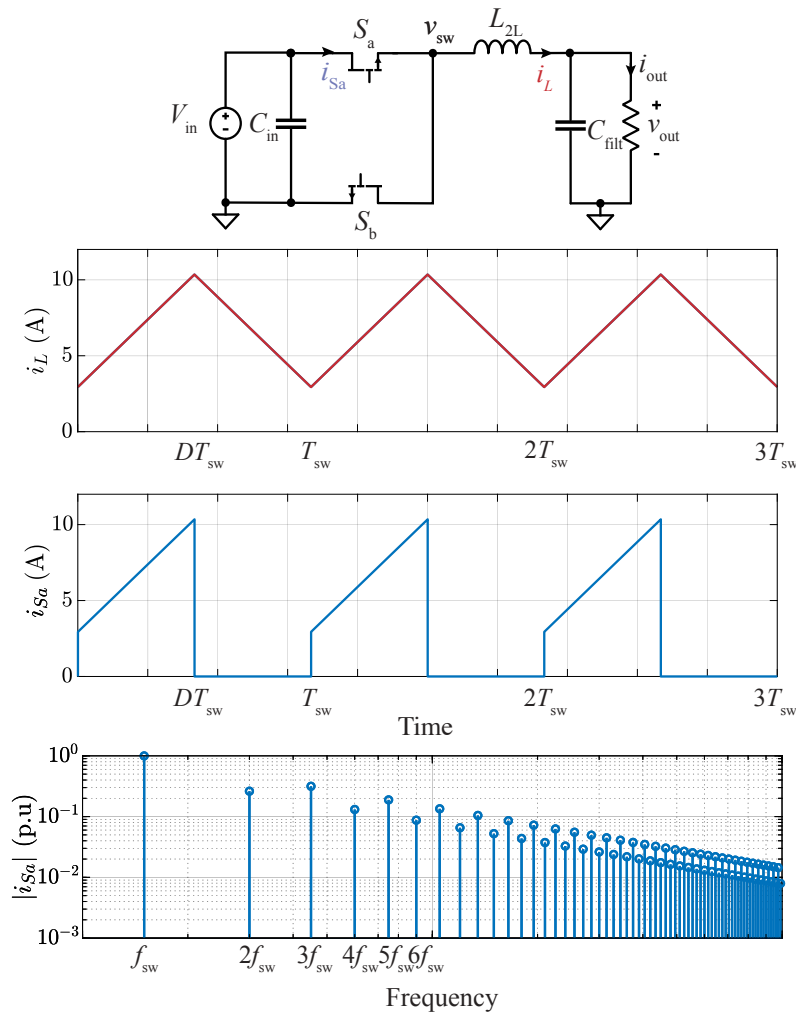


Figure 6.5: Labeled schematic of a 2-level buck converter and plots of the pertinent currents i_L and i_{Sa} obtained from simulation in PLECS. The magnitudes of the harmonic spectra for i_{Sa} are also shown, highlighting a fundamental component at f_{sw} .

Input-Side DM EMI

In the 2-level buck converter, input side EMI arises due to switching actions at the switching frequency f_{sw} . Fig. 6.5 shows a buck converter with waveforms for the inductor current i_L , and the current through the high-side switch i_{S_a} . The resulting harmonic spectrum, normalized to the fundamental harmonic at f_{sw} is also shown. When the switch S_a is on, it conducts the inductor current i_L , and the periodicity of these switching actions creates a fundamental component at f_{sw} .

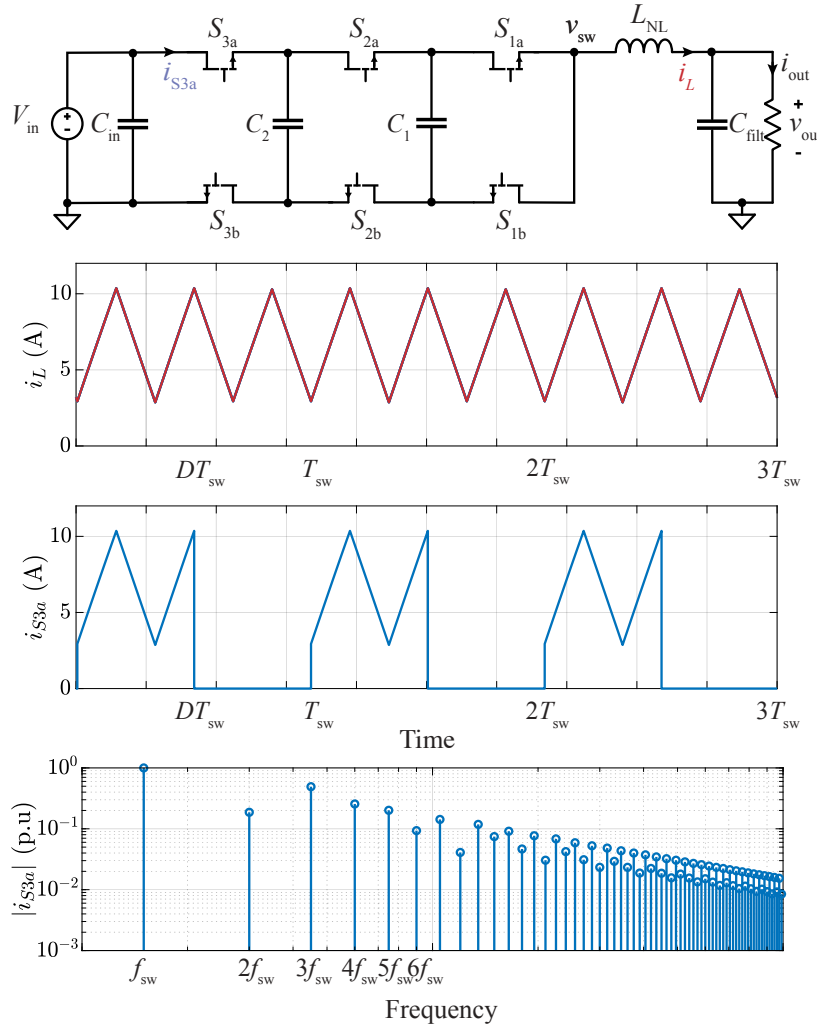


Figure 6.6: Labeled schematic of a 4-level FCML converter and plots of the pertinent currents i_L and i_{S3a} obtained from simulation in PLECS. The magnitudes of the harmonic spectra for i_{S3a} are also shown, highlighting a fundamental component at f_{sw} . For the same switching frequency as the buck converter, the FCML inductor is sized for the same current ripple such that $L_{NL} = L_{2L}/9$.

To describe DM EMI in the FCML converter, we will investigate a 4-level converter for simplicity. To understand the frequency content at the input side of the FCML converter, let us inspect the current through the high-side switch S_{3a} . Fig. 6.6 shows the schematic for a 4-level FCML converter, the inductor current i_L , and the current through the first switch $i_{S_{3a}}$. When the switch S_{3a} is conducting, it carries the inductor current. Here, we have sized the inductor of the FCML converter such that it has the same peak-to-peak ripple as the buck converter in Fig. 6.5 for the same f_{sw} . This is accomplished by decreasing the filter inductance by a factor of $(N - 1)^2$ such that $L_{NL} = L_{2L}/9$.

The harmonic spectrum of the input current, normalized to the fundamental harmonic at f_{sw} is also shown in Fig. 6.6. Much like the 2-level buck converter, the fundamental component at f_{sw} is the largest harmonic. The third harmonic, corresponding to $f_{eff} = 3f_{sw}$ is proportionally slightly larger than the third harmonic in the buck converter case in Fig. 6.5. Subsequently, we see that the effects of PS-PWM operation are shown to not substantially impact the input-side spectra, even in this example with high inductor current ripple. The fundamental harmonic is very much determined by the switching actions of the first switch pair.

Input-side DM EMI of the FCML converter has been previously documented in [100] for an inverter system. In that work, the sidebands generated by dc-ac operation are also described via the computation of a formal Double Fourier transform using techniques from [101]. In [100], the inductor current is also assumed to be a uniform periodic function, which is an assumption we relax in this work as we consider output-side EMI later in this section. Thus, in lieu of the analytically rigorous Fourier transform, we opt to use the Fast Fourier Transform (FFT) to describe both input- and output-side DM EMI in this chapter.

Output-Side DM EMI

In PS-PWM, the frequency observed at the switch node of the FCML converter is a multiple of the switching frequency, $f_{eff} = (N - 1)f_{sw}$. In most of the FCML converter literature, f_{eff} has traditionally informed output-side EMI filter design. This design insight is particularly pertinent for grid-tied FCML converters [23], where the LC filtered voltage interacts with the grid. However, some recent work [21, 87] showcases that additional harmonics at f_{sw} may occur. These “intra-harmonics” arise as a result of two key mechanisms: flying capacitor imbalance, and flying capacitor voltage ripple. Moreover, the work in [87] provides concrete evidence that these two mechanisms are coupled, which may further worsen the generation of these intra-harmonics.

To investigate these intra-harmonics, we seek to describe the output current of the converter. For a resistive load

$$i_{out} = \frac{v_{out}}{R_{load}} \quad (6.2)$$

by Ohm’s law. We can describe the current i_{out} in the frequency domain by considering the cascading impacts of the LC filter on the v_{sw} signal transformed into its harmonic

magnitudes.

In the frequency domain, we can represent the switch-node voltage as a series of harmonic magnitudes by taking the Fast Fourier Transform (FFT) of this voltage signal. Here, we choose the FFT over the computation of an analytical Fourier series, as this enables us to evaluate different switch-node voltages. We define a frequency-dependent function $V_{\text{sw}}[k]$ as

$$V_{\text{sw}}[k] = \text{FFT}(v_{\text{sw}}). \quad (6.3)$$

The switch-node voltage $V_{\text{sw}}[k]$ is filtered by an LC filter with a transfer function $H[k]$ that is approximated by

$$H[k] = H(j\omega_k) = \frac{1}{1 - \omega_k^2 LC_{\text{filt}}}, \quad \omega_k = 2\pi f_k. \quad (6.4)$$

We can estimate the frequency-domain output voltage as

$$V_{\text{out}}[k] = H[k] V_{\text{sw}}[k] \quad (6.5)$$

and the output current for a purely resistive load as

$$I_{\text{out}}[k] = V_{\text{out}}[k] / R_{\text{load}}. \quad (6.6)$$

Now, we have a way to describe the differential-mode currents in the frequency domain, and can evaluate the impacts of different flying capacitor balancing and ripple scenarios. In the following analysis, the converter operating parameters in Table 6.3 are used.

Table 6.3: Converter Operating Parameters

Parameter	Value
V_{in}	100 V
v_{out}	56 V
L	10 μH
C_{filt}	4 μF
R_{load}	10 Ω
f_{sw}	150 kHz

The Zero-Ripple, Balanced Case:

We first consider an ideal case, in which the flying capacitors of the FCML converter are considerably large, such that their peak-to-peak voltage ripple $\Delta v_{\text{pp}} = 0$. Since we often size our flying capacitors such that this ripple is a fraction of the switch blocking voltage $\Delta v_{\text{pp}} = \alpha V_{\text{in}} / (N - 1)$, we are considering the scenario where $\alpha = 0$. In this case, we also assume that the flying capacitors have perfectly balanced dc voltage offsets, meaning their

mid-range voltage is a fraction of the input voltage $V_{C,k} = kV_{\text{in}}/(N - 1), k \in [1, N - 2]$. For a perfectly balanced FCML converter with $\alpha = 0$, we generate a switch-node voltage v_{sw} that switches between different fractions of the input voltage. In Fig. 6.7, for $V_{\text{in}} = 100 \text{ V}$, $D = 0.56$, and $f_{\text{sw}} = 150 \text{ kHz}$, we show the generation of the switch-node voltage from the perfectly dc flying capacitor voltages that measure $V_{C1} = 33.33 \text{ V}$ and $V_{C2} = 66.67 \text{ V}$. From v_{sw} , we compute $V_{\text{sw}}[k]$, and apply the LC filter transfer function for $L = 10 \mu\text{H}$ and $C_{\text{flt}} = 10 \mu\text{F}$, and a resistive load of $R_{\text{load}} = 10 \Omega$ to find $I_{\text{out}}[k]$. In the bottom plot of Fig. 6.7, we show the normalized harmonic magnitudes of I_{out} . The fundamental component here is f_{eff} , rather than f_{sw} . The harmonic content is consistent with literature for perfectly balanced FCML converters with no flying capacitor voltage ripple [23].

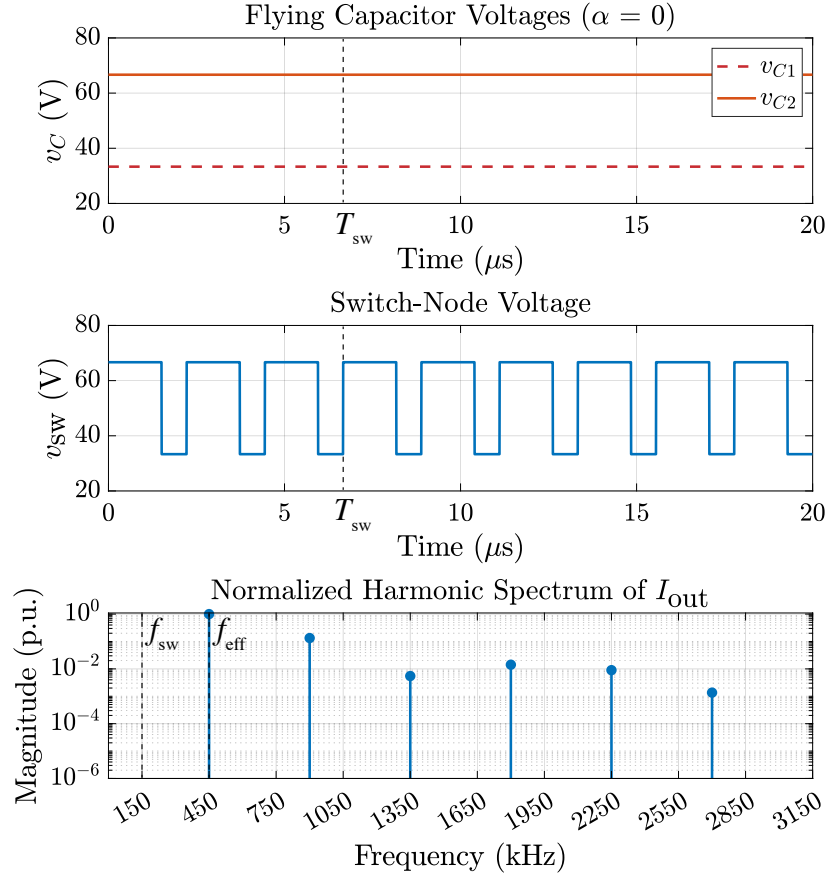


Figure 6.7: The top plot shows two perfectly balanced flying capacitor voltages with no ripple. The middle plot shows the generation of the switch-node voltage waveform, and the bottom plot shows the harmonic magnitude of the output current, as estimated by the FFT of the switch-node voltage. Here, $V_{\text{in}} = 100 \text{ V}$, $D = 0.56$, and $f_{\text{sw}} = 150 \text{ kHz}$.

The Zero-Ripple, Imbalanced Case:

We next consider the (improbable) case where the FCML converter has no flying capacitor voltage ripple, but there are small deviations in the mid-range voltages of the capacitors. As an example here, the flying capacitor voltages are deviated by just -0.67 V from their nominal values for the 4-level converter, corresponding to a 2% voltage imbalance. In this scenario, we have a switch-node voltage with a component at a switching frequency periodicity. In Fig. 6.8, we can see this in the switch-node voltage waveform, where the pulse heights at different times in the switching sequence can vary by as much as ± 0.67 V. In the frequency domain, this results in harmonics at f_{sw} that may be similar in size to the harmonic at f_{eff} . As voltage imbalance is worsened, these harmonics will be exacerbated.

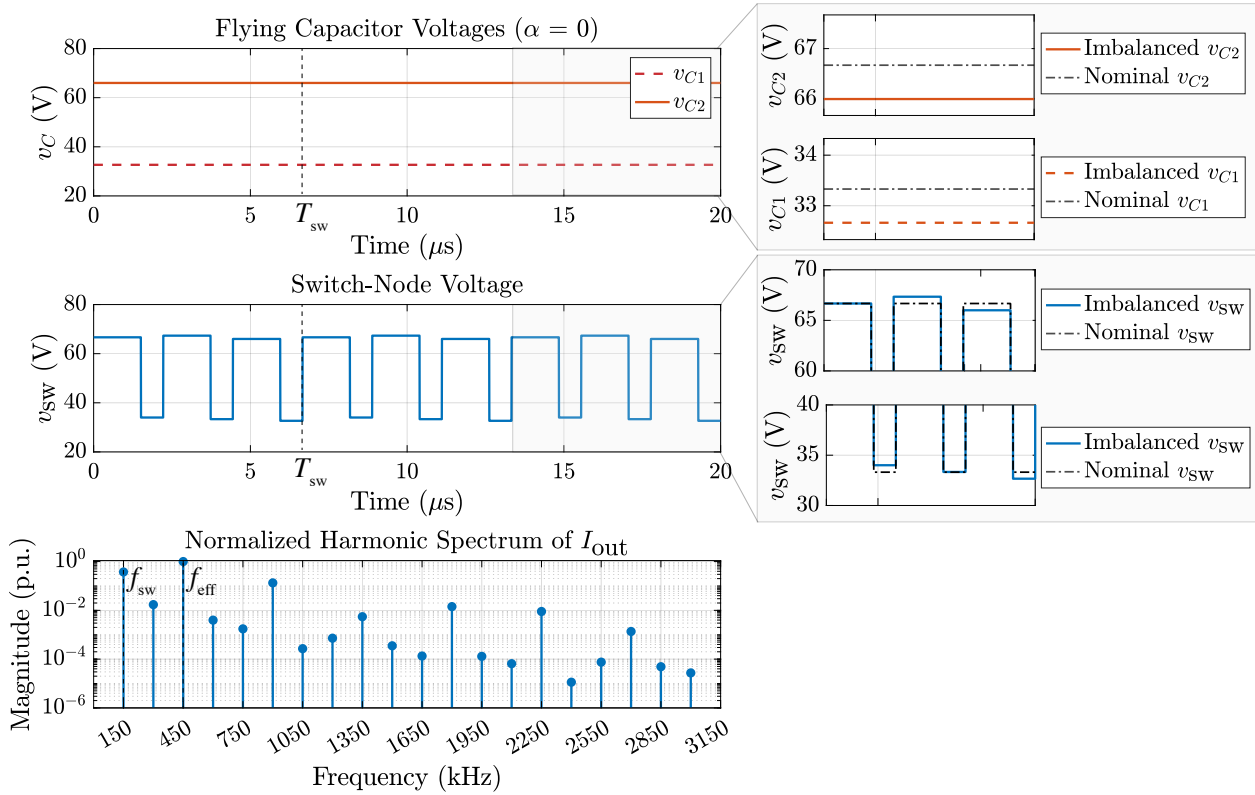


Figure 6.8: The top plot shows two flying capacitor voltages with no ripple content. In this plot, $V_{C,1} = 32.67$ V, and $V_{C,2} = 66.00$ V. An inset shows the small deviations (0.67 V) from the nominal midrange capacitor voltages. The middle plot shows the generation of the switch-node voltage waveform, with an inset showing deviations from the nominal switch-node voltage waveform. The bottom plot shows the harmonic magnitude of the output current, as estimated by the FFT of the switch-node voltage. Here, $V_{in} = 100$ V, $D = 0.56$, and $f_{sw} = 150$ kHz.

Natural flying capacitor voltage balancing is determined by a number of physical con-

verter mechanisms. While parasitic output capacitance of semiconductor devices incurs hard-switching losses, C_{oss} in the FCML converter also serves a critical function in rebalancing charge in the flying capacitors [102]. Flying capacitor voltage balancing is also strongly influenced by level count. It has also been shown that even level counts have better natural balancing dynamics than odd level count converters [103]. Operation of the converter at a nominal duty ratio $D = k/(N - 1)$, $k \in [1, N - 2]$ also contributes to imbalanced operation.

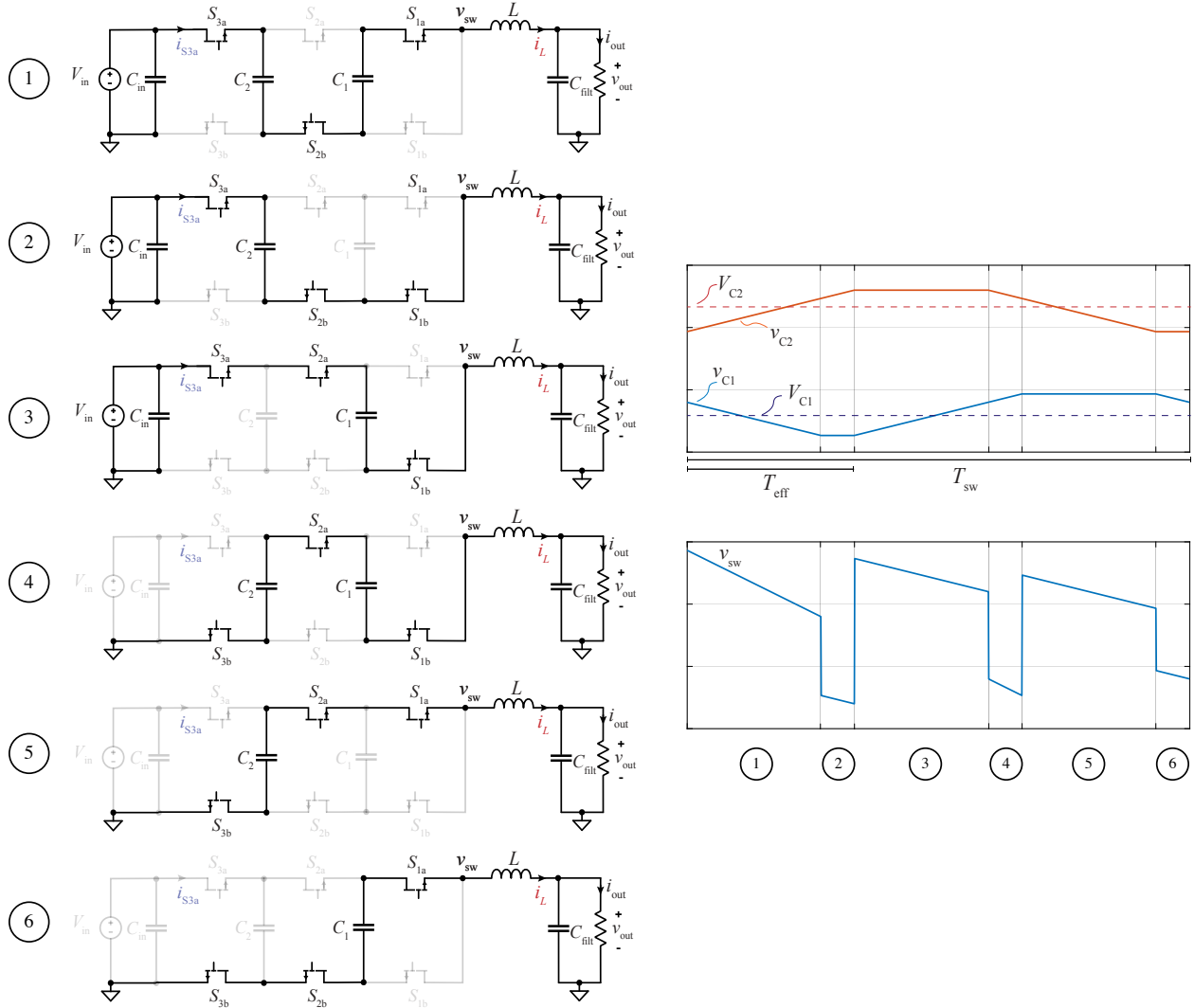


Figure 6.9: Each switching state of a 4-level FCML converter. The flying capacitor voltages with ripple are shown, along with their mid-range voltages $V_{C,k}$, as is the constructed switch-node voltage waveform v_{sw} .

The Nonzero-Ripple, Balanced Case:

Lastly, we consider the case where the flying capacitors are balanced, but have voltage ripple resulting from finite flying capacitance. In Fig. 6.9, we explicitly highlight the generation of the switch-node voltage during each circuit state, where either one or two flying capacitors are connected in series by the conducting switches. This switch-node voltage highlights different voltage ripple slopes as a result of the charging of either C_{fly} or $C_{\text{fly}}/2$. In Fig. 6.10, we observe that the converter with flying capacitor voltage ripple generates intra-harmonics at f_{sw} . While in this particular case, f_{eff} is still the largest harmonic, the 1st and 2nd harmonics are close in magnitude.

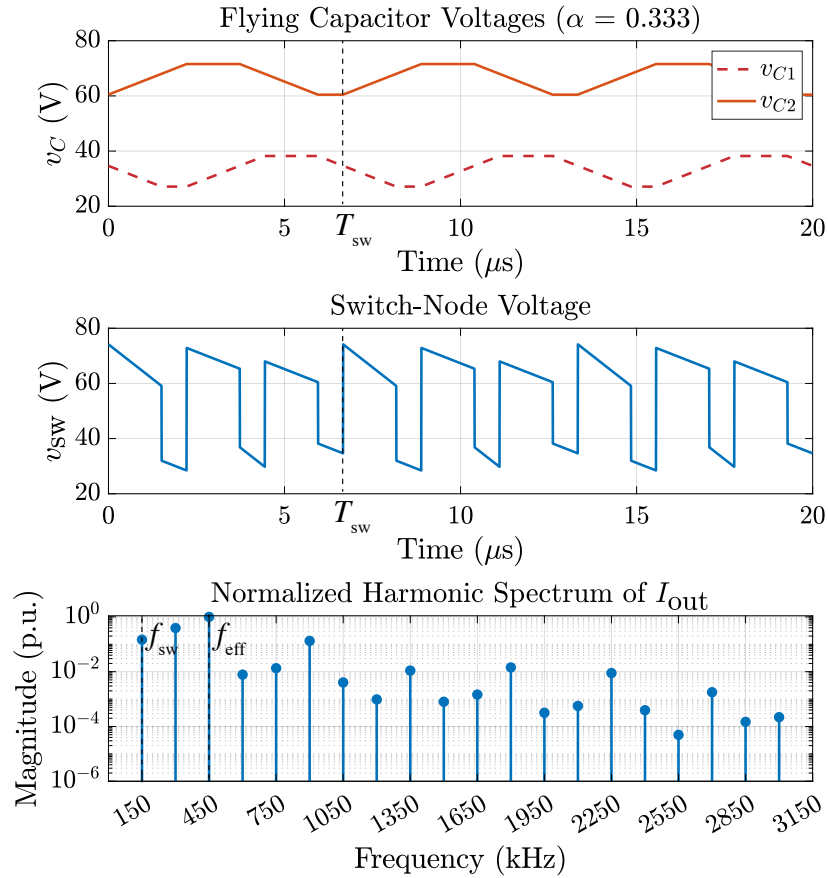


Figure 6.10: The top plot shows two flying capacitor voltages with $\alpha = 0.4$. In this plot, $V_{C,1} = 33.33 \text{ V}$, and $V_{C,2} = 66.67 \text{ V}$ correspond to balanced mid-range voltages. The middle plot shows the generation of the switch-node voltage waveform, and the bottom plot shows the harmonic magnitude of the output current, as estimated by the FFT of the switch-node voltage. Here, $V_{\text{in}} = 100 \text{ V}$, $D = 0.56$, and $f_{\text{sw}} = 150 \text{ kHz}$.

One nuance that we would like to capture here, is that flying capacitor voltage ripple also plays a part in flying capacitor voltage imbalance. In [87], flying capacitor voltage

ripple is incorporated into a closed-form model for steady-state operation of the converter. This model describes the generation of a switch-node voltage with varying slopes, which in turn generates an inductor current waveform with ripple that is parabolic as a result of the integration of the volt-seconds across L . The model can capture and describe deviation from the mid-range voltages as a function of capacitor voltage ripple, and it shows that high-ripple designs present poorer natural balancing of the flying capacitors.

Thus far, there is not substantial literature documenting the generation of harmonics on the LC filter side of the converter as a result of flying capacitor voltage ripple. In [87], the harmonics are documented alongside their relationship with ripple ratio α . In [21], these intra-harmonics are documented and described on the ac side of an FCML totem-pole PFC circuit. In [52], intra-harmonics are shown for an 8-level FCML inverter through hardware measurements.

With the establishment of capacitor imbalance and voltage ripple being contributors of intra-harmonics in the output-side EMI spectra, we can further consider that these two mechanisms are inherently coupled. To explore the dual impact of these mechanisms, the model in [87] is employed. Because this piecewise parabolic model considers flying capacitors with voltage ripple and enables the assessment of flying capacitor voltage balancing at different operating conditions, we can use it to gain insight into the generation of output-side EMI via the construction of the switch-node voltage from model outputs.

In Fig. 6.11 we show the mid-range voltages for a 4-level FCML converter across the full range of duty cycles computed using the modeling approach in [87]. Near the nominal duty ratios (1/3 and 2/3 here), these mid-range voltages deviate further from their ideal values. If we increase the flying capacitor voltage ripple, the deviation of the mid-range voltage worsens. Concrete evidence is shown here that capacitor voltage ripple has a strong relationship with natural balancing of the FCML converter.

Table 6.4: 4-Level FCML Converter Operating Conditions and Components

Parameter	Value
V_{in}	100 V
V_{out}	10-90 V
I_{out}	3 A
f_{sw}	150 kHz
C_{fly}	150 nF, 630 V, C3225X7T2J154K200AC
L	10 μ H, IHLP6767GZER100M01
Input and Output Capacitor	2.2 μ F, 450 V, C5750X6S2W225K250KA

By evaluating the model in [87], we can compute both flying capacitor imbalance and harmonic magnitudes at different capacitor voltage ripple conditions. In Fig. 6.12a, the percent imbalance of the flying capacitors are plotted on the left y-axis for ripple ratio

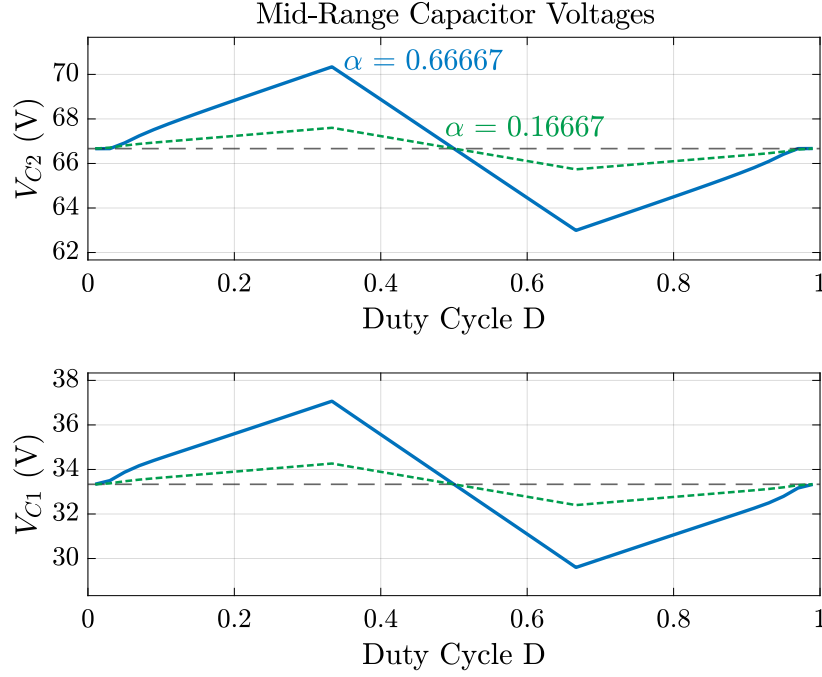
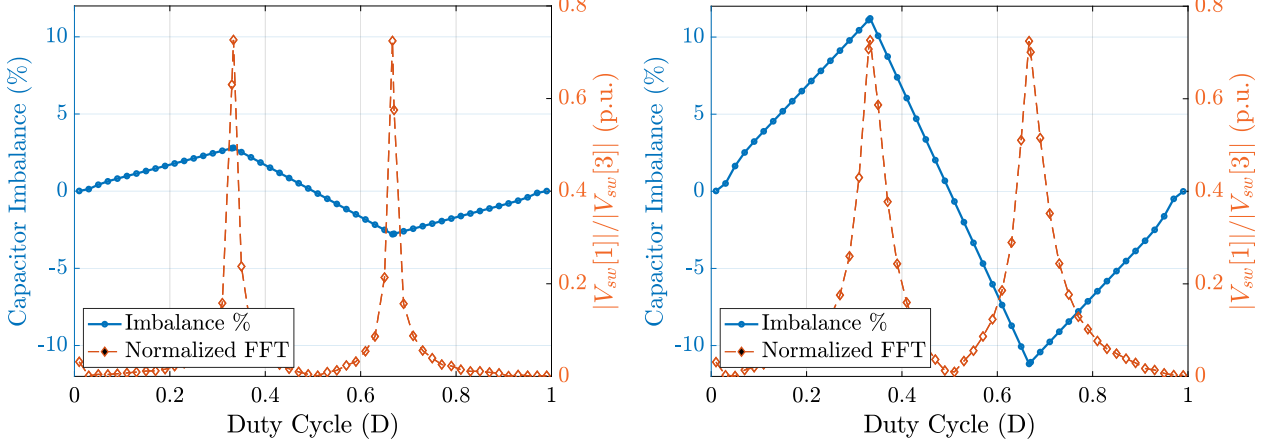


Figure 6.11: For both $\alpha = 0.1667$ and $\alpha = 0.6667$, we show the deviation of the mid-range voltages for a 4-level FCML at $V_{in} = 100$ V, $f_{sw} = 150$ kHz across the full range of duty cycles.

$\alpha = 0.1667$. Note that α here is computed for duty cycles in the middle bins, defined as $1/(N-1) < D < (N-2)/(N-1)$. In this duty cycle region, flying capacitor voltage ripple is maximized. On the right y-axis, the first harmonic of $V_{sw}[k]$ normalized to the $(N-1)^{th}$ harmonic, which here is $V_{sw}[3]$ for the 4-level FCML converter. Because these voltage magnitudes are normalized, we do not need to apply the LC filter transfer function, as normalization would result in its cancellation. We observe that small deviations in mid-range capacitor ripple result in large first harmonic content relative to the expected fundamental component at f_{eff} . In Fig. 6.12b, the same parameters are shown for $\alpha = 0.6667$. The relative magnitudes of the harmonic at f_{sw} normalized to the magnitude at f_{eff} are invariant between the low and high ripple cases at the nominal duty ratios ($D = 1/3$ and $D = 2/3$).

In addition to the first harmonic, we also consider the harmonic at $2f_{sw}$ for both $\alpha = 0.1667$ and $\alpha = 0.6667$, normalized again to $3f_{sw}$. This is shown in Fig. 6.13a and Fig. 6.13b. One notable observation is that the second harmonic has a substantial magnitude even when the converter is operating at a balanced operating condition. At $D = 0.5$, the 4-level FCML converter should exhibit minimal deviation in flying capacitor mid-range voltage magnitude. At this operating point, as ripple is increased, notable second harmonics are generated.

This analysis shows that regardless of the FCML converter being well balanced, the existence of flying capacitor voltage ripple results in harmonics below f_{eff} that require mitigation

Imbalance and Harmonics vs. Duty Cycle ($\alpha = 0.16667$) Imbalance and Harmonics vs. Duty Cycle ($\alpha = 0.66667$)


(a) Imbalance and relative harmonic magnitude for the low ripple case where $\alpha = 0.1667$. (b) Imbalance and relative harmonic magnitude for the low ripple case where $\alpha = 0.6667$.

Figure 6.12: On the left-hand axis, we plot the percent imbalance of the flying capacitor mid-range voltage. On the right-hand axis, the first harmonic of $V_{sw}[k]$ normalized to the $(N - 1)^{th}$ harmonic, which here is $V_{sw}[3]$ for the 4-level FCML converter. Normalizing to $V_{sw}[3]$ enables the examination of the magnitude of the first harmonic relative to the *ideal* fundamental component at f_{eff} .

to achieve EMI compliance. The model in [87] is validated in hardware to demonstrate the accurately predicted deviation in flying capacitor mid-range voltages. However, here we also showcase DM EMI measurements taken for the 4-level hardware prototype in this work to validate the claims made here about the existence of intra-harmonic frequency content in the switch-node of the FCML converter.

The EMI measurement bench in Fig. 6.4 was used to validate output-side DM EMI in the 4-level FCML converter in [87]. Hardware parameters are shown in Table 6.4. The results for both $\alpha = 0.1667$ and $\alpha = 0.6667$ are shown in Fig. 6.14. The first harmonic here is enlarged by LISN mismatch, which is characterized further in Chapter 8. The second harmonic enables us to make relative comparisons to the third harmonic and our modeled comparisons. Since we measure EMI here in $\text{dB}\mu\text{V}$, we can compute the harmonic magnitudes in μV as $|v_{DM}| = 10^{\text{DM EMI (dB}\mu\text{V})/20}$. The ratio of $|v_{DM,2}|/|v_{DM,3}| = 0.05$ for $\alpha = 0.1667$ and $|v_{DM,2}|/|v_{DM,3}| = 0.25$ for $\alpha = 0.6667$ is consistent with the normalized values in Figs. 6.13a and 6.13b.

From this analysis, we can draw a few conclusions: Flying capacitor voltage imbalance creates much worse intra-harmonics than the existence of ripple alone, so designing a converter for naturally balanced operation will manage these harmonics effectively. Future research opportunities exist in the assessment of control techniques that promote the balancing of flying capacitors for improved EMI performance. There are digital active balancing

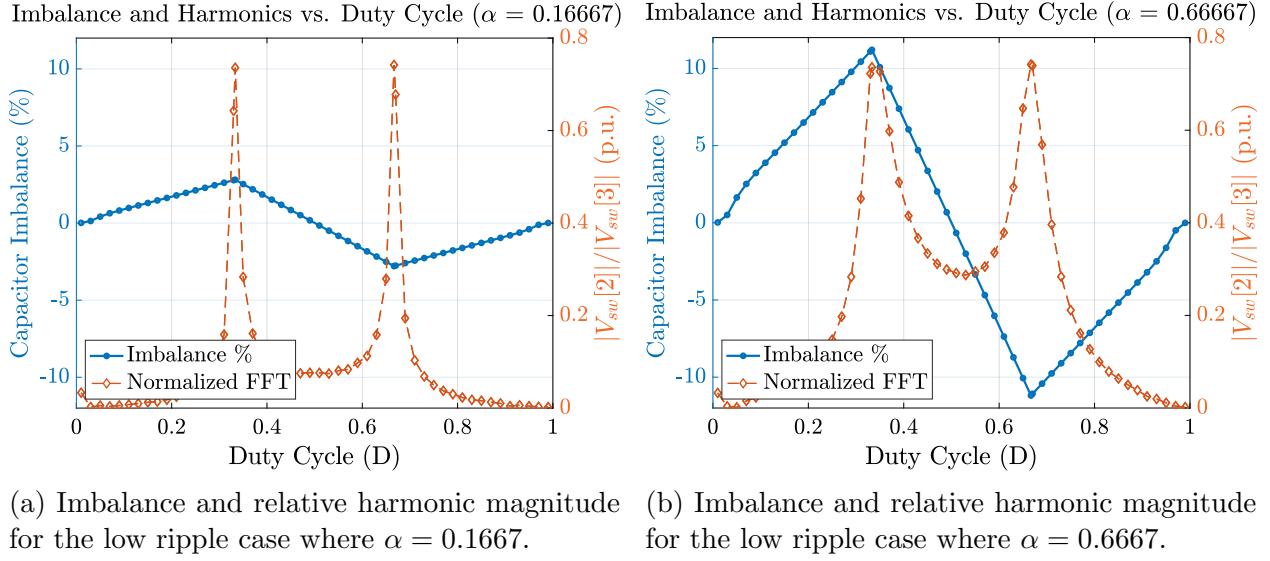


Figure 6.13: On the left-hand axis, we plot the percent imbalance of the flying capacitor mid-range voltage. On the right-hand axis, the second harmonic of $V_{sw}[k]$ normalized to the $(N - 1)^{th}$ harmonic, which here is $V_{sw}[3]$ for the 4-level FCML converter. Normalizing to $V_{sw}[3]$ enables the examination of the magnitude of the first harmonic relative to the *ideal* fundamental component at f_{eff} .

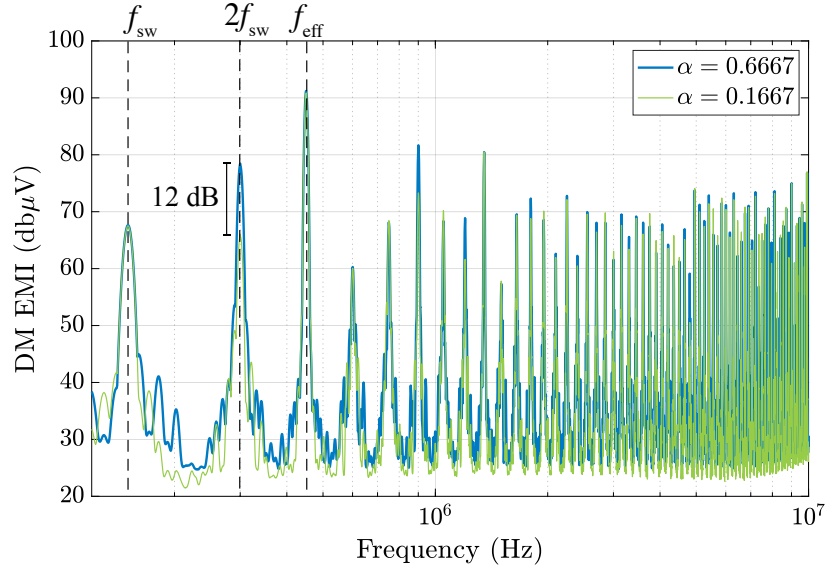


Figure 6.14: For both $\alpha = 0.1667$ and $\alpha = 0.6667$, we show the hardware measurements of output-side EMI for the 4-level converter in [87]. Figure made in collaboration with Elisa Krause.

[104] and current-programmed modulation techniques [105] that enable better capacitor balancing, which may mitigate the magnitude of intra-harmonics. Lastly, since voltage ripple results in intra-harmonics even in a perfectly balanced FCML converter, it is worthwhile to compute the impacts of the addition of more flying capacitance in intra-harmonic mitigation. While high-ripple designs enable a movement to higher power density [22], the increase in EMI filtering may result in system-level power density tradeoffs.

6.3 Conclusion

This chapter provides an introduction to conducted EMI and its characterization. Then, an overview of DM EMI is provided for the FCML converter. For the input side of the FCML converter operated in a buck configuration, we describe the fundamental magnitude at f_{sw} using simulation results. However, for the output side of the converter, we provide a lengthier discussion of the generation of harmonics below f_{eff} . These harmonics are generated as a result of two coupled mechanisms, flying capacitor voltage imbalance and ripple. A piecewise parabolic model detailed in [87] is used to investigate the impact of these mechanisms further, and hardware results corroborate the generation of these harmonics in a 4-level converter with good natural balancing and finite flying capacitance. Since very few papers document these intra-harmonics [21, 52, 87, 106], it is worthwhile to have further characterized their cause.

Chapter 7

Improvements to Differential-Mode EMI in DC-AC FCML Converters

Executive Summary

In Chapter 6, differential-mode EMI was characterized for the FCML converter. This chapter builds on the previous EMI characterization by addressing EMI mitigation. Here, we assess the use of the variable switching frequency scheme presented in Chapter 3 specifically designed for an FCML converter in dc-ac operation to spread out the peaks of conducted electromagnetic interference (EMI) while still improving efficiency. Ripple constraints of the flying capacitor voltages and inductor current set the basis for a deterministic switching frequency pattern, which can also be considered a targeted dithering scheme. Furthermore, by leveraging the constraints set by the passive components of the designed prototype and reducing the switching frequency, switching losses are mitigated and efficiency is increased. Hardware results are provided for a 2 kW 8-level FCML inverter and showcase improved conducted EMI peaks and efficiency for the high performance, high level count prototype.

This chapter is based on work appearing in both [107] and [52].

7.1 Introduction

The use of high figure-of-merit gallium nitride high-electron-mobility transistors (GaN HEMTs) enables increasingly high switching frequencies for multilevel converters [108, 109]. An important consideration is the generation of unwanted conducted electromagnetic interference (EMI) and how this propagates in the system as the frequency increases [10, 23, 110, 111]. The input side of an FCML converter operated as a step-down inverter has a current flow with a fundamental harmonic at the switching frequency f_{sw} , much like the 2-level buck converter equivalent. This poses possible EMI challenges at a lower frequency [112] rather

than at the multiplied effective frequency at the ac output of the inverter [21, 23], which can have detrimental effects on the equipment attached to the dc bus [113–115].

Beyond the inclusion of a passive EMI filter at the converter input port, there are modulation techniques that can be used to improve the conducted emissions at harmonics of the switching-frequency fundamental by spreading out the characteristic peaks [62, 116–121]. For these spread-spectrum frequency modulation (SSFM) techniques, however, the passive components must be sufficiently sized for the lowest frequency used in the modulation scheme, which may further penalize power density.

This work analyzes and demonstrates in hardware how a technique previously used to improve the efficiency of an FCML inverter can be leveraged more strategically to improve EMI performance as well [54]. In the work presented in Chapter 3, the observed efficiency improvement was accomplished by reducing the switching frequency in low-ripple regions of the ac cycle for a grid-frequency inverter. Regarding EMI mitigation, the ripple constraints here create feasible operating conditions that make it possible to generate a deterministic switching pattern sequence that effectively functions as a spread-spectrum frequency modulation technique. In this work, we assess the efficacy of this approach for a higher level count converter, which is less frequently characterized for EMI. Hardware results are provided for a high performance 8-level FCML inverter with GaN switches. Improved measured conducted EMI at the input and output of the converter and improved efficiency results demonstrate the merits of this technique.

7.2 Methodology

The methods presented in Chapter 3 are used to develop the set of feasible operating constraints for the hardware prototype presented in Section 7.3. The schematic for an 8-level FCML inverter with a split-bus input is shown in Fig. 7.1. The hardware prototype parameters are shown in Table 7.1. We use these hardware parameters to compute absolute lower limits for switching frequency operation.

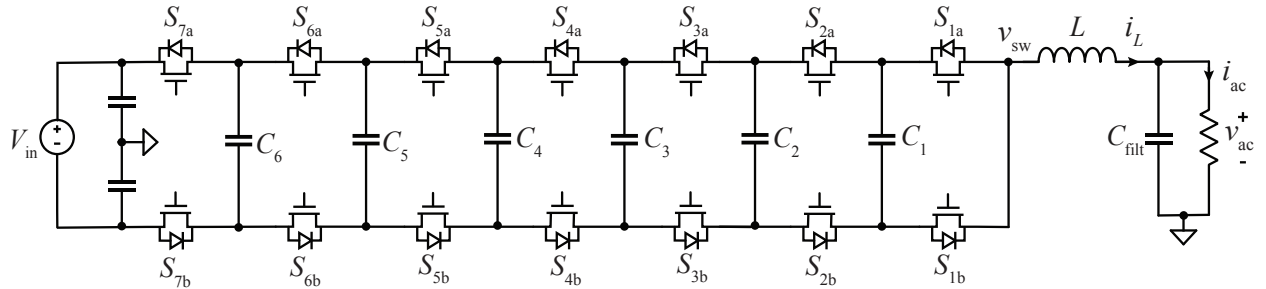


Figure 7.1: Simplified schematic for an 8-level FCML converter with a split input bus.

To generalize to different converter use-cases, we can consider the EMI at both the input and output ports of the converter. At the input side, the first switch pair (i.e., $S_{(N-1),a}$ and

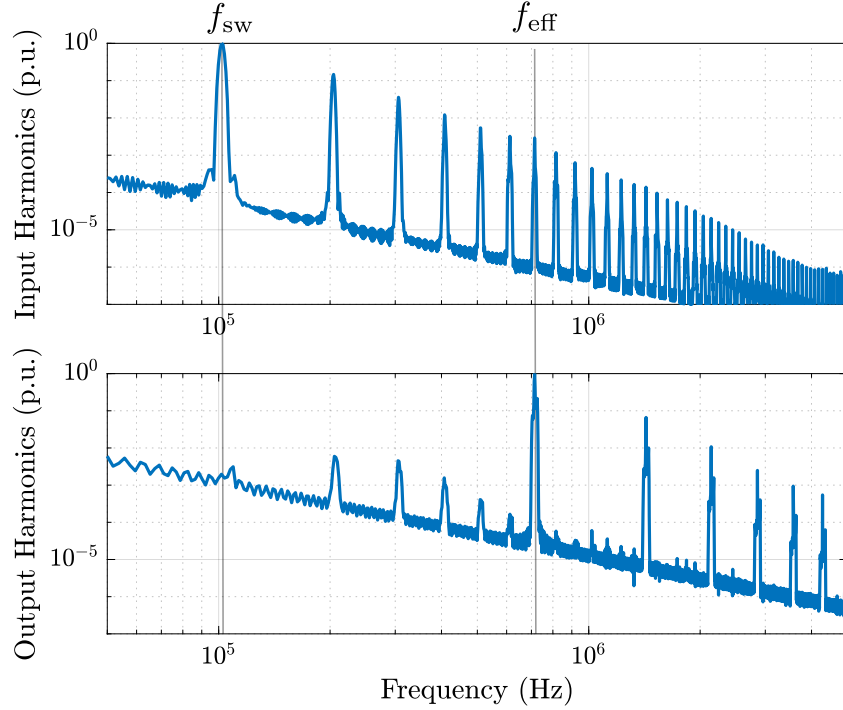


Figure 7.2: a) Harmonics for the input current of an 8-level FCML converter from PLECS simulation normalized to the harmonic magnitude at f_{sw} . b) Harmonics for the output inductor current of an 8-level FCML converter from PLECS simulation normalized to the harmonic magnitude at f_{eff} .

$S_{(N-1),b}$ in Fig. 3.1) carries the inductor current while on, creating frequency content with a fundamental component at the switching frequency. The resulting EMI spectrum can be readily observed in Fig. 7.2a, which displays normalized simulated harmonics for an 8-level FCML converter.

At the output of the converter, the load current (for a resistive load) is proportional to the voltage across the filter capacitor C_{flt} [23] which is a function of inductor current ripple. This has a predominant component at the effective switching frequency f_{eff} , which is well documented [23]. In this work, we found in hardware that there are additional “intra-harmonics” at harmonics of f_{sw} , which is a direct result of flying capacitor voltage ripple [21, 87]. The impact of the flying capacitor voltage ripple on the output-side harmonics can be observed in simulation, as shown in the inductor current spectra of Fig. 7.2b, which displays the result of a simulated 8-level FCML converter. Additional harmonics of the switching frequency are clearly visible.

The LC filter imposes a design constraint such that we should size $f_{sw, min, LC}$ with a reasonably large scaling factor α_{LC} to attenuate f_{eff} using (3.8).

We size this corner frequency scaled by α_{LC} as

Table 7.1: 8-Level FCML Converter Operating Conditions

Parameter	Value
V_{in}	400 V
f_{mod}	60 Hz - 600 Hz
f_{sw}	84 kHz - 102 kHz
v_{ac}	135 V _{rms}
P_{out}	350 - 2000 W
$\Delta v_{C_{\text{pp}}, \text{max}}$	10.5 V
$\Delta i_{L_{\text{pp}}, \text{max}}$	3.0 A
Derated C_{fly}	$\approx 3 \mu\text{F}$, paralleled 2.2 μF 450 V, C5750X6S225K250KA
GaN HEMT	100 V, 1 m Ω , EPC 2361
L	6.6 μH $2 \times$ IHLP6767GZER3R3M01
C_{flt}	$6 \times 150 \text{ nF}$ 250 V, TDK 5750C0G2E154J230KE

$$\begin{aligned}
 f_{\text{sw}, \text{min}, LC} &= \alpha_{LC} \frac{1}{(N-1) 2\pi \sqrt{LC_{\text{flt}}}} \\
 &= \alpha_{LC} \frac{1}{7 \cdot 2\pi \sqrt{13.2 \mu\text{H} \cdot 900 \text{ nF}}} \\
 &= \alpha_{LC} \cdot 6596 \text{ Hz}.
 \end{aligned} \tag{7.1}$$

To achieve 20 dB of attenuation, we would want to size $\alpha_{LC} = 3.2$, and would subsequently set $f_{\text{sw}, \text{min}, LC} = 21.1 \text{ kHz}$.

The other limit to consider is set by the desired number of discrete frequency steps and the shortest duration between nominal duty ratios of the FCML converter. Since this is a split-bus FCML converter, we evaluate (3.9) and (3.11). For $\alpha_d = 10$ steps for $f_{\text{mod}} = 400 \text{ Hz}$, we would find for an 8-level converter with $f_{\text{disc}, \text{cutoff}} = 84 \text{ kHz}$. In Fig. 7.3, we showcase values of $f_{\text{disc}, \text{cutoff}}$ computed for a range of modulation frequencies f_{mod} for the 8-level inverter. This cutoff frequency can be tuned by ac application space.

Using the defined converter parameters in Table 7.1, and the practical limit set by discrete switching frequency operation, we derive the switching frequency pattern shown in Fig. 7.4. On this diagram, we have labeled the shortest duration between nominal duty ratios used to compute $f_{\text{disc}, \text{cutoff}} = 84 \text{ kHz}$.

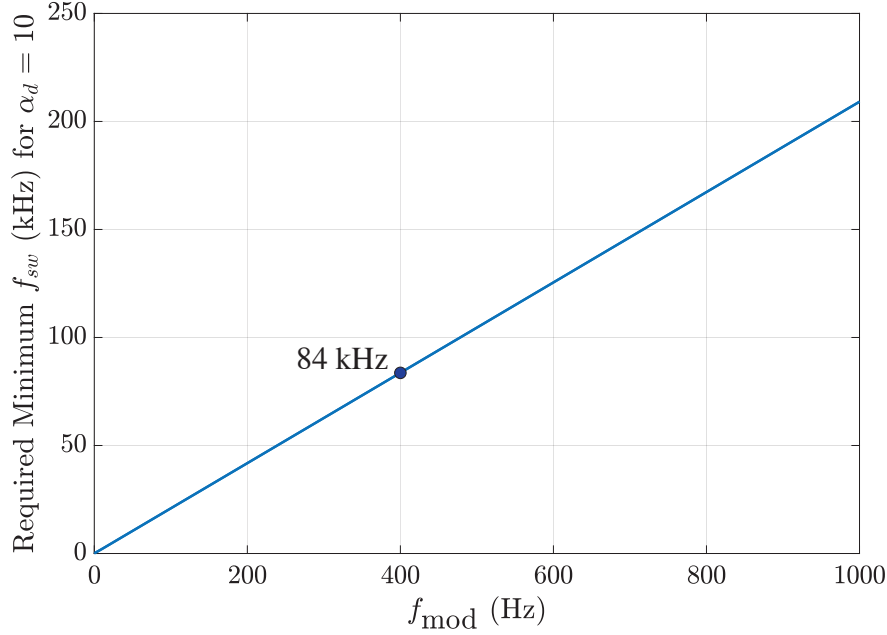


Figure 7.3: Plot showing how $f_{\text{sw}, \text{min}}$ scales across ac modulation frequency f_{mod} to ensure that at least 10 steps ($\alpha \geq 10$) are generated across the brief sub-duration defined by $\Delta t_{1/(N-1)}$. For the 8-level FCML converter operating with $f_{\text{mod}} = 400$ Hz, this is computed to be at least 84 kHz.

7.3 Hardware Results

To ensure the extension of this work to a higher level-count FCML inverter and to a split-bus prototype, an 8-level converter was used to validate the possible improvements to conducted EMI. This converter was designed with minimal parasitic inductance in the power path, which helps to reduce differential-mode conducted EMI [66], and was originally designed for operation at $f_{\text{sw}} = 102$ kHz. The operating conditions for this prototype are in Table 7.1.

In Fig. 7.5, we highlight the functionality of the converter operating under variable switching frequency operation at 700 W. No difference in flying capacitor voltage balancing was observed in the switch-node voltage waveform v_{sw} for both fixed and variable switching frequency operation. Like the 6-level converter in Chapter 3, efficiency improvements were also observed for the 8-level converter. In Fig. 7.6, we see improved efficiency measurements across the full load range. A peak efficiency of 98.85 % was observed at 1080 W for the fixed frequency case, compared to 98.9 % at 1190 W for the variable switching frequency operation. The substantial efficiency improvements are primarily attributed to an improvement in overlap losses, as the particular GaN HEMTs used featured very low on-state resistances.

The EMI test bench and hardware prototype are shown in Fig. 7.7. In this work, EMI measurements are shown for both the input and output side EMI, so that this work can be used to advance the informed mitigation of EMI at either port for FCML inverters.

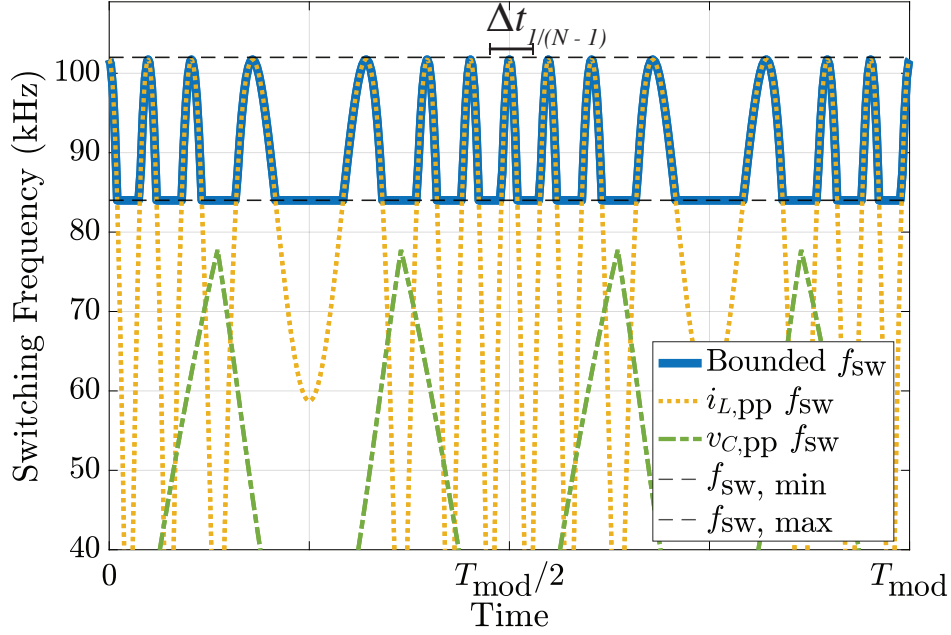


Figure 7.4: Example continuous variable switching frequency limits for an 8-level FCML inverter with a nominal switching frequency of 102 kHz, and low modulation frequency f_{mod} . Here, the lower switching frequency limit is set by $f_{\text{disc, cutoff}} = 84$ kHz.

In this work we are most concerned with DM EMI, as the converter does not have a heat sink and thus has limited stray capacitance to ground. As seen in Fig. 7.8, which shows measured DM and CM EMI, this is a reasonable assumption for the converter considered in this work. However, this particular distinction will vary by hardware prototype and packaging.

EMI measurements are taken for both the fixed frequency case and the variable switching frequency case at 700 W. CISPR average measurements are provided in this work to capture the impact of the variable switching frequency scheme over the slower ac frequency behavior. Substantial EMI improvements are shown in Fig. 7.9 for the $f_{\text{mod}} = 400$ Hz case. For fixed frequency operation, the peak of the fundamental is at the 102 kHz switching frequency, and the subsequent peaks are at harmonics of this frequency. The application of the variable switching frequency scheme reduces the peak of the fundamental by 7 dB. A spread sub-peak forms around 91.2 kHz in this case.

Additional measurements taken at $f_{\text{mod}} = 600$ Hz validate that this scheme is still effective at higher modulation frequencies when there are fewer switching frequency updates per ac cycle. As discussed in Section II, fewer discrete time steps are available for the same switching frequency limits. As shown in Fig. 7.10, the increasingly discretized switching frequency envelope for the 600 Hz case remains an effective mechanism to reduce the EMI peaks, with improvements on the order of 5 dB. Like the 400 Hz case, the sub-peak occurs at 91.9 kHz,

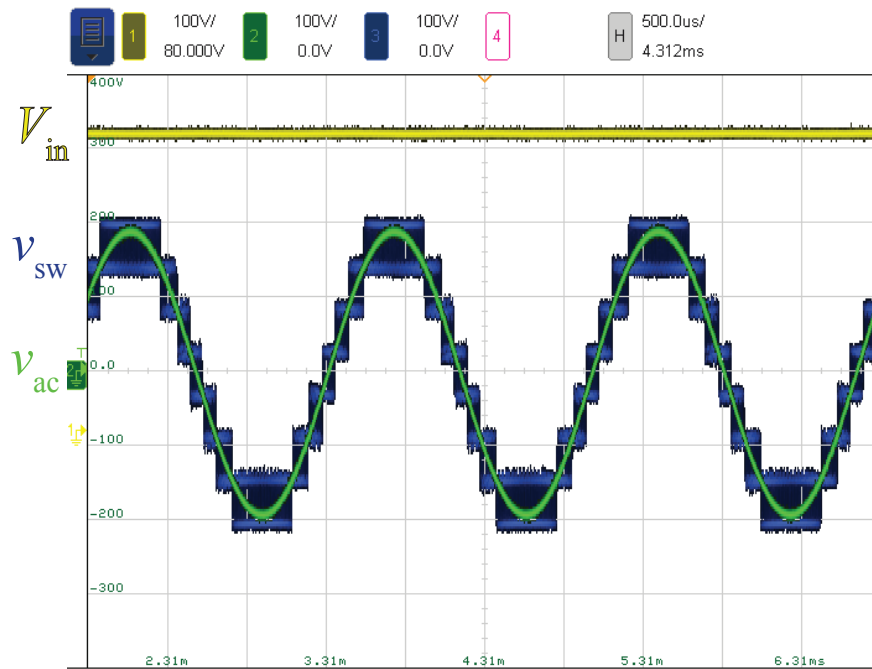


Figure 7.5: Measured waveforms of the input voltage V_{in} , the switch-node voltage v_{sw} , and the ac output voltage v_{ac} at 700 W and $f_{mod} = 600\text{Hz}$.

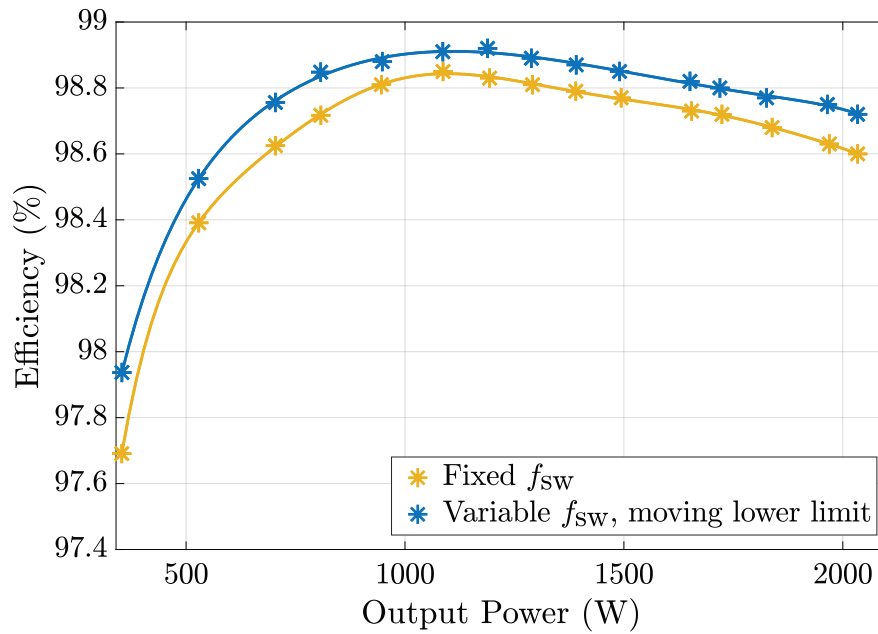
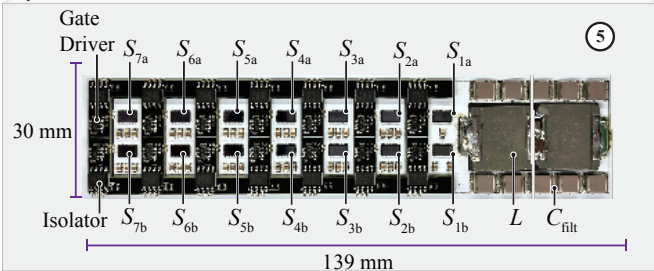


Figure 7.6: Plot of efficiencies for both fixed frequency and variable frequency operation for $f_{mod} = 600\text{ Hz}$.



which consists of an FCML inverter with a split-bus input such as the one in Fig. 7.1.

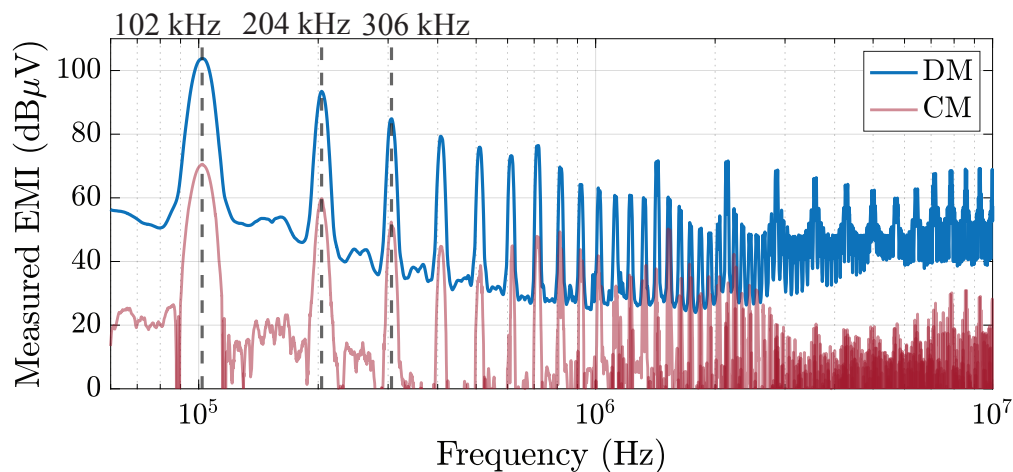


Figure 7.8: Measured input EMI for $f_{\text{mod}} = 600$ Hz showing split CM and DM data.

showing consistency between both modulation frequencies. This congruity suggests that this technique can be applied at higher modulation frequencies for the same limits of $f_{\text{sw, min}}$ and

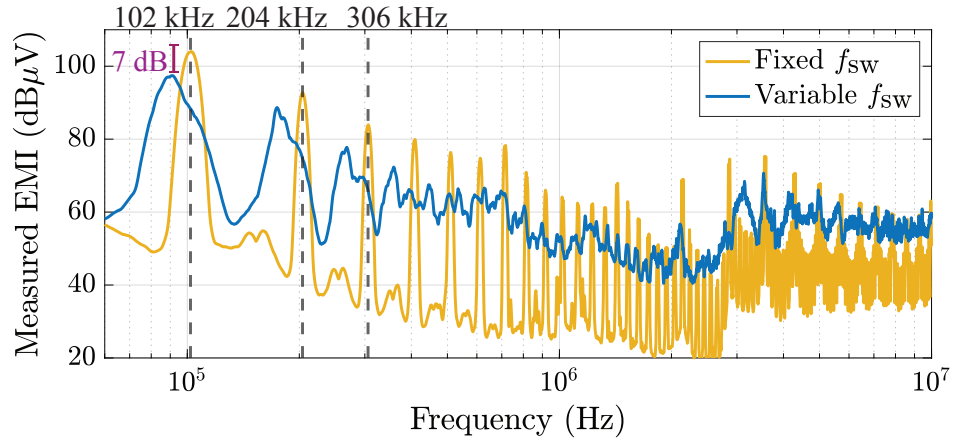


Figure 7.9: Measured input EMI for $f_{\text{mod}} = 400$ Hz.

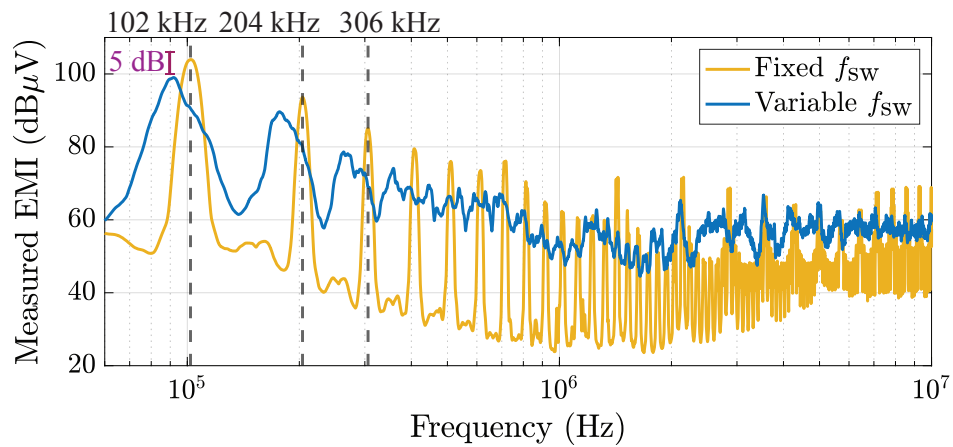


Figure 7.10: Measured input EMI for $f_{\text{mod}} = 600$ Hz.

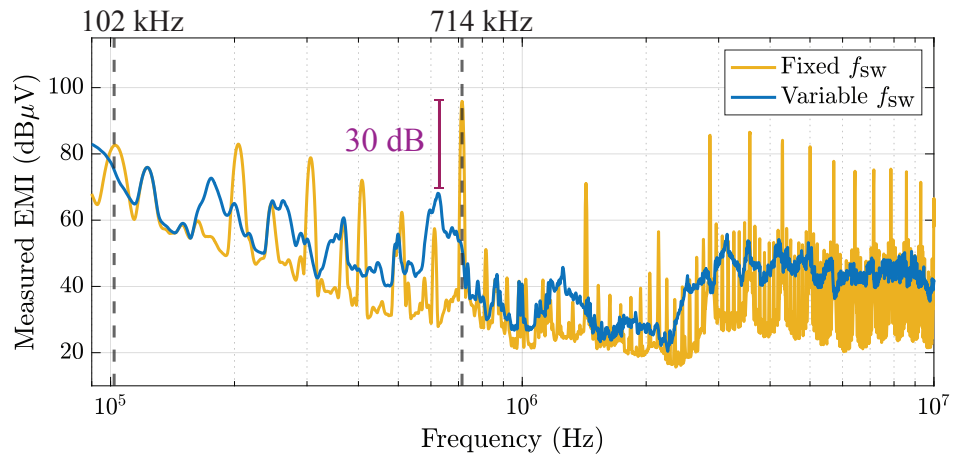


Figure 7.11: Measured output-side EMI for $f_{\text{mod}} = 60$ Hz at 250 W.

$f_{\text{sw}, \text{max}}$ without loss in functionality.

Output-side EMI measurements are shown at 250 W, 120 V_{rms} and $f_{\text{mod}} = 60$ Hz in Fig. 7.11. The first observation is that the largest harmonics occur as expected at $f_{\text{eff}} = 714$ kHz. However, as expected, smaller peaks are observed at harmonics of f_{sw} . For a grid-tied converter, this would necessitate considering these lower-order harmonics in the EMI mitigation strategy. The lower-order harmonics would possibly increase the EMI filter size of the converter, although the spreading of these peaks from the variable switching frequency technique is still an effective approach to reduce their impact. For the measured converter prototype, the variable frequency technique reduced the harmonic content at f_{eff} by ≈ 30 dB. At harmonics of f_{eff} , this method also provides substantial peak mitigation, indicating that this would be a highly effective technique for applications in which the ac-side harmonics must be mitigated.

7.4 Conclusion

This chapter demonstrates a variable frequency switching scheme that can be used for peak EMI spreading in dc-ac FCML converters. The approach is generalized to handle a range of modulation frequencies and level counts such that a deterministic and sufficiently granular pattern is generated. Hardware results showcase a substantial reduction in input-side and output-side EMI peaks for an 8-level FCML inverter at different ac modulation frequencies. In outlining the possible switching frequency conditions that the converter is rated for, this work opens up the possibility of creating other FCML converter specific spread-spectrum frequency routines. Furthermore, the efficiency of the high-performance prototype is increased, as the average switching frequency in this case is reduced.

Chapter 8

Modeling Common-Mode EMI in the FCML Converter

Executive Summary

This chapter derives and validates a model for common-mode EMI in the FCML converter. Common-mode EMI is generated by parasitic capacitances throughout the circuit and the currents arising through them as a result of large dv/dt switching events. The mechanisms by which the FCML converter generates conducted common-mode EMI are an underexplored area of research, despite the critical nature of EMI. This chapter proposes modeling a parasitic capacitance for each switch to understand how common-mode currents are generated in multilevel operation. Common-mode EMI scaling behavior from first principles for an FCML converter is derived, and hardware validation with a 6-level converter prototype provides concrete evidence in both the time and frequency domains that the level of modeled detail is sufficient to capture power-stage CM behavior for this converter topology.

This chapter is based on work appearing in [122].

8.1 Introduction

Chapters 6 and 7 have focused on DM EMI propagation and mitigation in the FCML converter. This chapter investigates the core behavior of common-mode (CM) EMI at the input side of the FCML buck converter operated under nominal phase-shifted pulse width modulation (PS-PWM) [17]. Common-mode EMI is predominantly generated by parasitic capacitances to ground throughout the circuit, which can be particularly challenging in a converter with a chassis-mounted enclosure [88–94]. A grounded heat sink mounted on a bare-die field effect transistor (FET) generates a parasitic capacitance with respect to the heat sink ground reference that is proportional to the source or drain referenced pad/tab

of the device [123–126]. Current through a capacitor is given by $i_C = C \frac{dv_C}{dt}$, and the high dv/dt events within each switching cell result in the generation of these unwanted currents from each FET through the heat sink. Since each switch in the FCML converter will have a parasitic capacitance associated with it, modeling CM EMI in the FCML converter is nontrivial.

Much of the work addressing fundamental EMI behavior in the FCML converter [21, 23] has been limited to commentary on conducted differential mode (DM) EMI, which is correlated to the currents observed at either the input or output of the converter. Thorough work has been done to derive a frequency-based model describing aggregate EMI with both CM and DM components for a boost FCML converter at both the input and output ports [127, 128], but there is limited commentary about implications for CM EMI in higher level count converters. Finally, EMI modeling for the FCML converter at the port with the LC filter has been previously performed [129]. Comparatively, this work presents a comprehensive analysis of common-mode EMI behavior in the FCML converter as seen at the input port and highlights the unique CM EMI behavior associated with the various circuit states. The inclusion of a parasitic capacitance for each switch is shown to be a necessary level of modeling detail for describing the CM EMI signatures for the power stage of the converter.

This work provides a systematic way to analyze the generation of common-mode currents in an FCML converter. One major finding is that the switch pair closest to the converter input port is a key contributor in the generation of CM EMI for this multilevel topology. Furthermore, a general mathematical description of the CM EMI sources is presented, which enables the rapid calculation of both time- and frequency-domain EMI signatures for the general N -level case. A compact expression for the frequency-domain behavior is presented, creating future opportunities in strategizing EMI mitigation.

This chapter presents the augmented converter model, as well as the derivation of the analytical model. A specially designed 6-level hardware prototype with “quiet” gate drive circuitry is used to validate the model. Hardware results are shown in both the time and frequency domains and show excellent matching. Sources of measurement error are discussed in this chapter, and provide strong corroboration that this model is useful in describing fundamental CM EMI behavior.

8.2 Derivations of the Analytical Model

Common-Mode EMI Scaling in the DC-DC FCML Converter

The N -level FCML converter, shown in Fig. 8.1 has $N - 1$ switch pairs and $N - 2$ flying capacitors. Under conventional phase-shifted PWM (PS-PWM), each switch pair is symmetrically phase-shifted from its adjacent switch pairs by $\phi_k = \frac{2\pi}{N-1}$, which results in an effective frequency at the switch node of $f_{\text{eff}} = (N - 1)f_{\text{sw}}$ [15]. In this mode of operation, each switch pair must block just $V_{\text{in}}/(N - 1)$, enabling the use of lower voltage FETs with higher figures-of-merit [75].

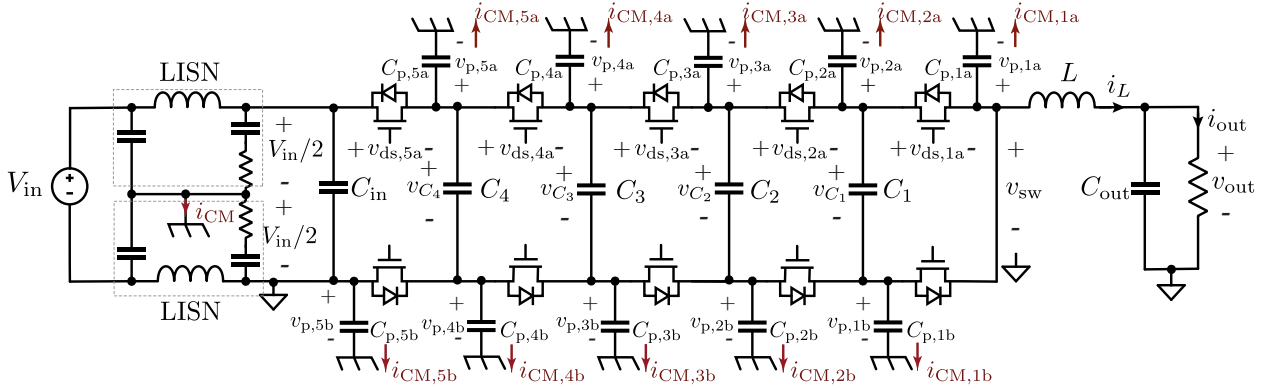


Figure 8.1: A 6-level FCML converter showing the generation of parasitic capacitances through a heat sink grounded to chassis.

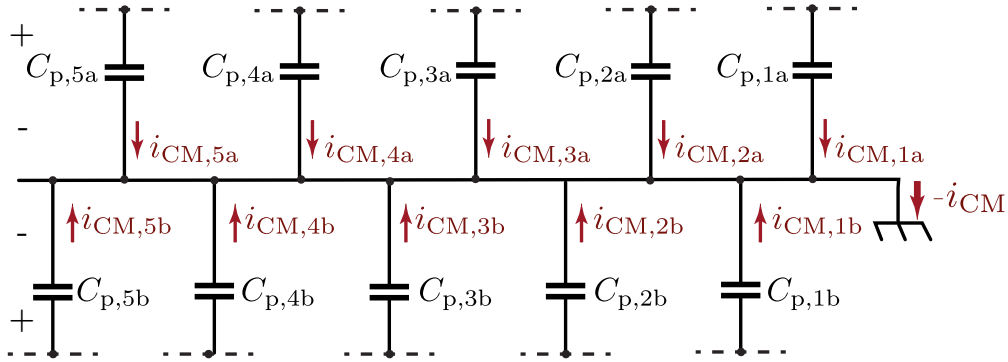


Figure 8.2: Common-mode currents flowing into LISN-referenced chassis ground as a result of parasitic capacitances throughout the circuit. The direction of current is consistent with Fig. 8.1.

For many power MOSFETs, top-side cooling is employed to increase thermal performance. The exposed metal typically has an internal electrical connection to either the source or drain potential of the FET. To maintain electrical insulation between the metal pad and the heat sink, a thin layer of electrically insulating (and ideally highly thermally conductive) thermal interface material (TIM) is typically used. Even with optimal packaging, this connection creates an undesirable capacitance when a grounded heat sink/chassis is used, with the capacitance given by: $C_p \approx \frac{\epsilon A_{\text{die}}}{d}$, where ϵ is the dielectric constant, A_{die} is the area of the die, and d is the thickness of the TIM. It should also be noted that in cases of ungrounded heat sinks, the heat sink itself will have stray capacitance to ground, thereby still providing paths for parasitic ground currents to flow.

In this work, a capacitance for each FCML switch is included in the converter model to gain insight into the generation of CM EMI in the power stage of the FCML converter. This

simple approach makes it possible to explore how these capacitances and their relative magnitudes influence total CM EMI generation in the power stage of the converter as observed at the converter input. For power transistors with the source terminal as the exposed metal used for cooling, these parasitic capacitances are shown in Fig. 8.1 for the 6-level FCML converter.

Each capacitance creates a path to the chassis with a finite impedance, which is a direct path for leakage currents to flow. These currents are generated as a result of the fundamental relationship $i_C = C \frac{dv_C}{dt}$. In other words, the differentiated voltage across each parasitic capacitance generates an unwanted CM current through that capacitor, and the total CM current as observed at the input side of the converter arises from the sum of these currents. As shown for the 6-level converter in Fig. 8.1, the common way to measure the CM EMI current, i_{CM} , is to place line impedance stabilization networks (LISNs) at the terminal of interest (in this case, the converter input). These LISNs share a common ground at the midpoint of the converter input, and the total CM current at the LISNs is measured as the sum of currents in (8.1). This sum of currents is also represented visually in Fig. 8.2.

$$\begin{aligned} i_{CM} &= - \sum_{i=1}^{(N-1)} i_{CM,ia} + i_{CM,ib} \\ &= - \sum_{i=1}^{(N-1)} C_{p,ia} \frac{dv_{C,p,ia}}{dt} + C_{p,ib} \frac{dv_{C,p,ib}}{dt} \end{aligned}$$

To characterize the voltages across each capacitor, we can systematically perform Kirchhoff's Voltage Law analysis for each parasitic capacitance in Fig. 8.1. The voltages across the top-side parasitic capacitances $v_{p,ia}$, and the low-side parasitic capacitances $v_{p,ib}$ where $i \in [1, (N-1)]$ are given in the system of equations in (8.1) as a function of the adjacent parasitic capacitor voltages, the input voltage, and the flying capacitor voltages $v_{C,i}$.

$$\begin{aligned} v_{p,(i)a} &= v_{p,(i+1)a} - v_{ds,(i)a} \\ v_{p,(i)b} &= v_{p,(i)a} + v_{ds,(i)a} - v_{C(i)} \\ &\vdots \\ v_{p,(N-1)a} &= V_{in}/2 - v_{ds,(N-1)a} \\ v_{p,(N-1)b} &= V_{in}/2 \end{aligned} \tag{8.1}$$

The interdependency of these node voltages makes it possible to distill the total CM current as a linear combination of each current in terms of the effective node capacitance, $C_{p,i}$, and the drain-to-source voltages $v_{ds,i}$. For an FCML converter operating in steady-state with sufficiently large flying capacitance, as it is customary to maintain small capacitor voltage ripple and switch voltage stress, we can approximate $\frac{dv_{C,i}}{dt} = 0$. Furthermore, with an adequately sized input capacitor, we can approximate $\frac{dV_{in}}{dt} = 0$. This eliminates these terms from the capacitor voltage derivatives. A smaller flying capacitance would increase voltage ripple on each flying capacitor C_i and add a ripple component to each $v_{ds,i}$.

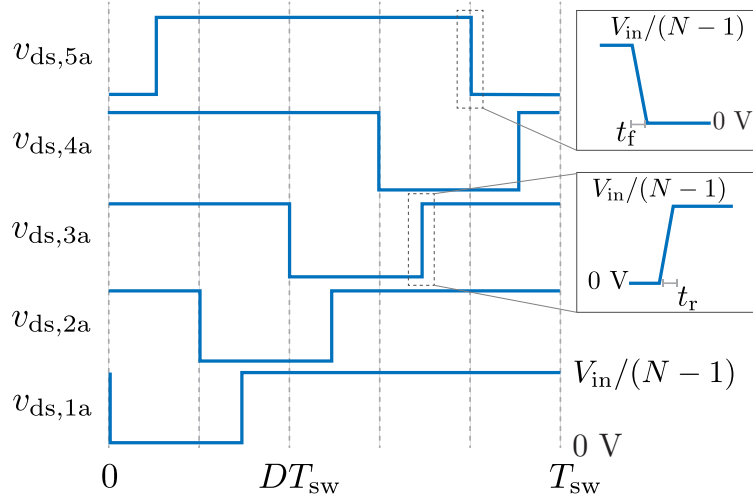


Figure 8.3: Phase-shifted v_{ds} waveforms for the high-side switches showcasing the simplified trapezoidal modeling approach for the drain-to-source voltages.

A linear combination of the sum of the capacitor currents is given in (8.2). This is given in a matrix composed of parasitic capacitances $C_{p,i}$ and the top-side drain-source voltages $v_{ds,ia}$.

$$\begin{aligned}
 i_{CM} = & \begin{bmatrix} C_{p,1a} \\ C_{p,2a} \\ \vdots \\ C_{p,(N-1)a} \\ C_{p,1b} \\ C_{p,2b} \\ \vdots \\ C_{p,(N-1)b} \end{bmatrix}^T \begin{bmatrix} 1 & 1 & \dots & 1 \\ 0 & 1 & \dots & 1 \\ \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \dots & 1 \\ 0 & 1 & \dots & 1 \\ 0 & 0 & \dots & 1 \\ \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \dots & 0 \end{bmatrix} \begin{bmatrix} \frac{dv_{ds,1a}}{dt} \\ \frac{dv_{ds,2a}}{dt} \\ \vdots \\ \frac{dv_{ds,(N-1)a}}{dt} \end{bmatrix} \quad (8.2)
 \end{aligned}$$

From this linear combination, there are several observations that can be made. First, the turn-on and turn-off of the first (leftmost) switch pair is integral to the generation of common-mode EMI in the FCML converter. During these switching transitions, the voltage change of the input-side top switch $\frac{dv_{ds(N-1)a}}{dt}$ occurs across $2N - 3$ parasitic capacitors as given in the vertical matrix dimension in (8.2). For a practical converter with identical parasitic capacitors $C_{p,ia} = C_{p,ib} = C_p$, there is a linear scaling in the contribution of each switch pair to the overall CM current, such that the switching transitions of the first pair contribute CM current in $2N - 3$ capacitors, the second pair in $2N - 5$ capacitors, and so

forth.

Each drain-to-source voltage is modeled as a phase-shifted periodic trapezoidal voltage with a distinct rise time t_r , and fall time t_f between 0 V and $V_{in}/(N - 1)$. This is shown in Fig. 8.3. Real phenomena such as ringing and overshoot are neglected here, as they are assumed to be identical in each switching cell. The derivative of these drain-to-source voltages appearing in the CM current is a set of periodic rectangular pulses, as shown in Fig. 8.4.

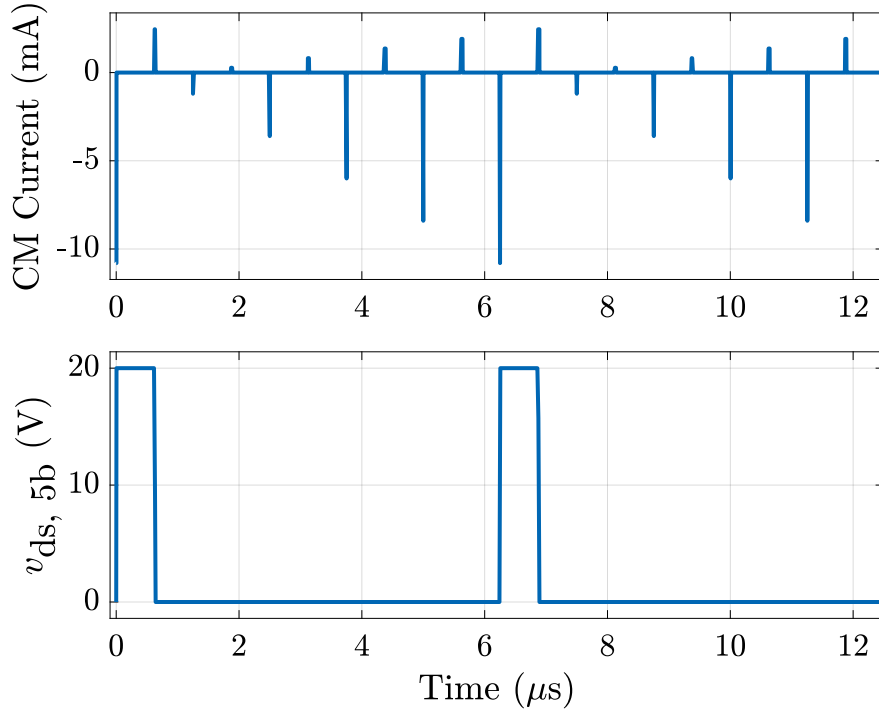


Figure 8.4: Common-mode currents under PS-PWM for identical parasitic capacitances for a 6-level FCML with $V_{in} = 100$ V (top). Drain-source voltage of switch 5b, illustrating the relationship between the dv/dt and the generation of CM currents (bottom).

The periodic CM current in Fig. 8.4 is formulated as a sum of $N - 1$ distinct positive rectangular waveforms and a sum of $N - 1$ negative rectangular waveforms associated with the rising and falling edges, respectively, of the high-side drain-source voltages $v_{ds,ia}$. To find a compact analytical model of CM EMI for the FCML converter operated in PS-PWM, we consider the translation of the time-domain model to the frequency domain via the Fourier transform. The periodic rectangular pulses make it possible to find the frequency-domain behavior using straightforward properties of the Fourier transform. A periodic rectangular pulse waveform with a period T centered about time $t = t_0$ in the time-domain has a Fourier

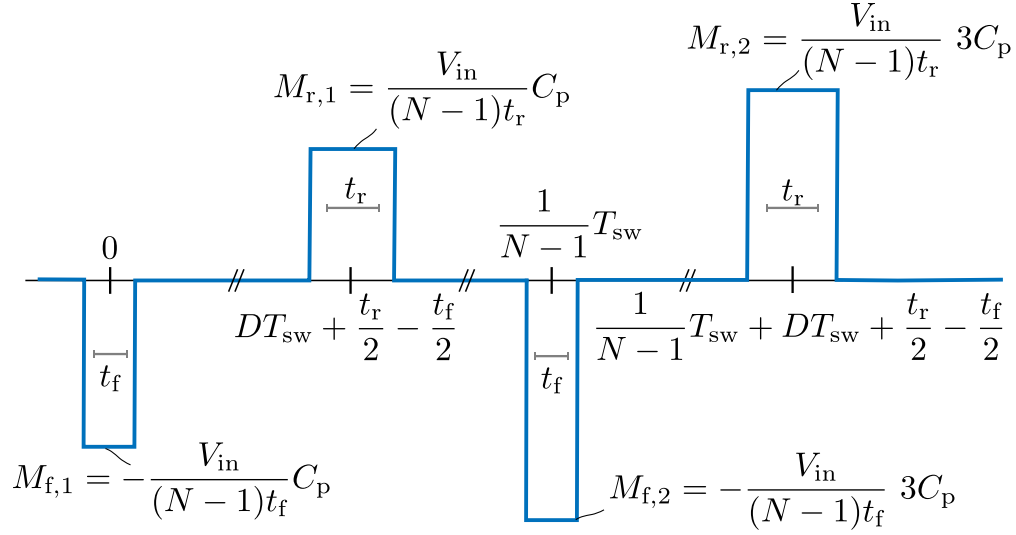


Figure 8.5: Example CM currents for two phase-shifted switching events (corresponding to $v_{ds,1}$, and $v_{ds,2}$), showcasing both magnitude and timings.

harmonic component a_k (corresponding to the cosine terms in the series) equal to

$$a_k = \frac{2}{\pi} \frac{M}{k} \sin\left(\pi k \cdot \frac{\tau}{T}\right) e^{(-j \frac{2\pi k}{T})t_0} \quad (8.3)$$

where M is the amplitude of the pulse, τ is the width of the pulse, and $k \geq 1$ is the harmonic number. The complex exponential in (8.3) comes from the time-shifting property of the Fourier transform, $\mathcal{F}(x(t - t_0)) = \mathcal{F}(x(t)) e^{(-j \frac{2\pi k}{T})t_0}$. This creates a general way to describe the time-shifted nature of the waveform. The linearity of the Fourier transform is then leveraged to find a single harmonic of the full CM current considering the sum of the rectangular waveforms. This linearity makes it possible to construct the Fourier coefficients a_k as a summation of the contributions of each rectangular waveform.

For each rectangular CM current, we need to find both its magnitude M and its relative time shift t_0 . We can define the CM current peak magnitudes associated with rise times as M_r , and the magnitudes associated with fall times as M_f . Because we assume linear rise/fall regions in the trapezoidal construction of $v_{ds,i}$, we approximate $\frac{dv}{dt_r} \approx \frac{V_{in}}{t_r(N-1)}$ and $\frac{dv}{dt_f} \approx -\frac{V_{in}}{t_f(N-1)}$. To factor in the linearly scaling number of parasitic capacitors with capacitance C_p subjected to each drain-to-source voltage, we consider the i^{th} switching cell counting up from the switch node of the converter. Combining the scaled capacitances and the dv/dt

events, we formulate these magnitudes in (8.4).

$$\begin{aligned} M_{r,i} &= \frac{V_{in}}{t_r(N-1)} \cdot C_p(2i-1) \\ M_{f,i} &= \frac{V_{in}}{t_f(N-1)} \cdot C_p(2i-1) \\ i &\in \mathbb{Z}, \quad 1 \leq i \leq N-1 \end{aligned} \quad (8.4)$$

With the magnitudes addressed, the remaining step is to find the relative time-shift associated with each rectangular waveform. This is easiest to do geometrically for a few cases. Fig. 8.5 shows the rectangular pulses associated with the switching events of $v_{ds,1a}$ and $v_{ds,2a}$. The pulses associated with t_f are centered about times $t = \frac{i-1}{N-1}T_{sw}$, $i \in [1, N-1]$ that capture the phase shifts associated with PS-PWM operation. The rectangular waveforms occurring as a result of t_r are shifted by the converter duty cycle D , which is assumed to be gated by a signal that is triggered at the start of t_f .

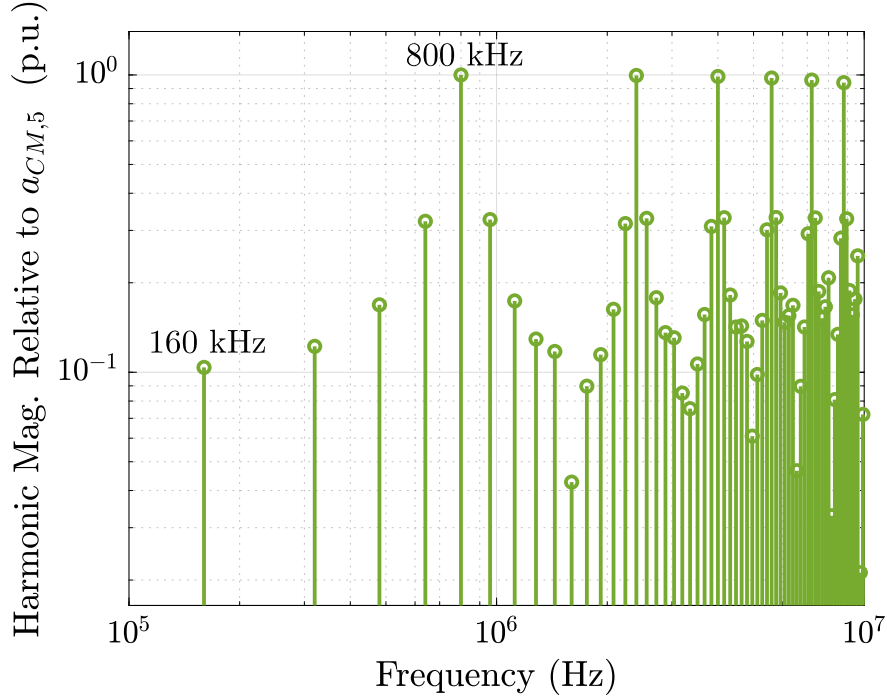


Figure 8.6: Harmonic content of calculated common-mode currents normalized to $a_{CM,5}$ at a switching frequency of 160 kHz and duty cycle $D = 0.1$ for a 6-level FCML converter. The fundamental harmonic is at f_{sw} .

Combining the magnitudes in (8.4) with the associated time shifts, the analytical harmonic decomposition of the Fourier coefficients of the continuous-time CM current in (8.5)

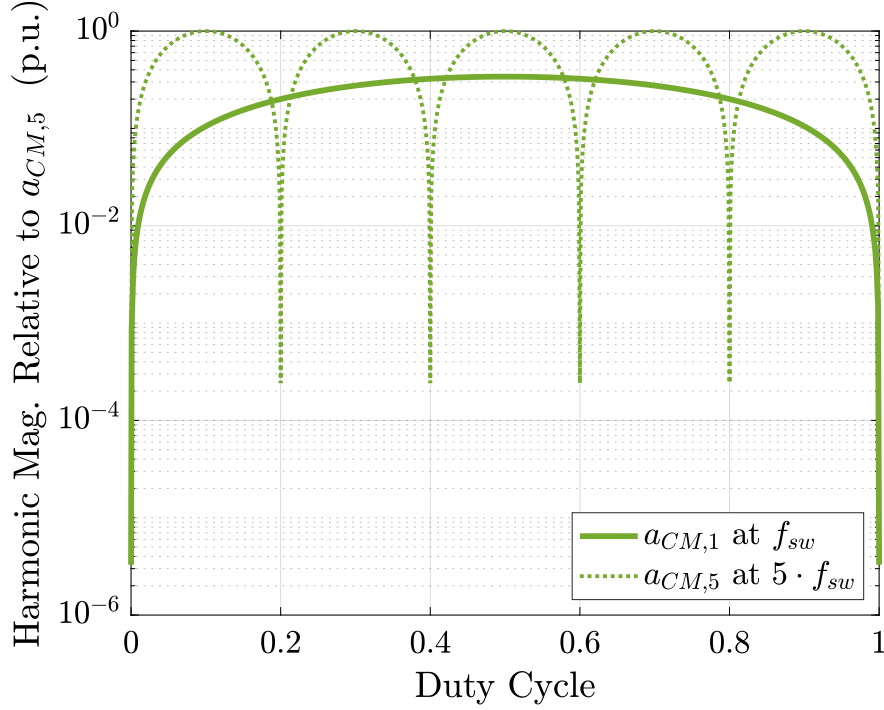


Figure 8.7: For a 6-level FCML converter, the magnitude $a_{CM,1}$ of the fundamental harmonic, and the harmonic at the effective switching frequency $a_{CM,5}$ normalized over $a_{CM,5}$ across the full range of duty cycles.

is constructed for each harmonic ($a_{CM,k}$) as a sum of all the common-mode current peaks. This decomposition reveals a fundamental ($k = 1$) at the switching frequency f_{sw} .

$$\begin{aligned}
 a_{CM,k} = & \sum_{i=1}^{(N-1)} -\frac{2 \cdot M_{f,i}}{k\pi} \sin\left(k\pi \frac{t_f}{T_{sw}}\right) e^{-j\frac{i-1}{N-1}2\pi k} \\
 & + \frac{2 \cdot M_{r,i}}{k\pi} \sin\left(k\pi \frac{t_r}{T_{sw}}\right) e^{-j(D+\frac{i-1}{N-1}+\frac{t_r}{2T_{sw}}-\frac{t_f}{2T_{sw}})2\pi k}
 \end{aligned} \tag{8.5}$$

The summation in (8.5) physically translates to the replacement of each high-side device as a frequency-domain voltage source placed in parallel with different numbers of parallelized parasitic capacitors.

For some duty cycles, maximum harmonic peaks occur at multiples of $(N-1)f_{sw}$ as shown in the visual representation of Fig. 8.6, which shows the normalized (to the maximum value) Fourier components for a duty cycle $D = 0.1$ used in a 6-level FCML converter. With this harmonic decomposition, it is possible to quickly ascertain frequency domain CM behavior for the FCML converter.

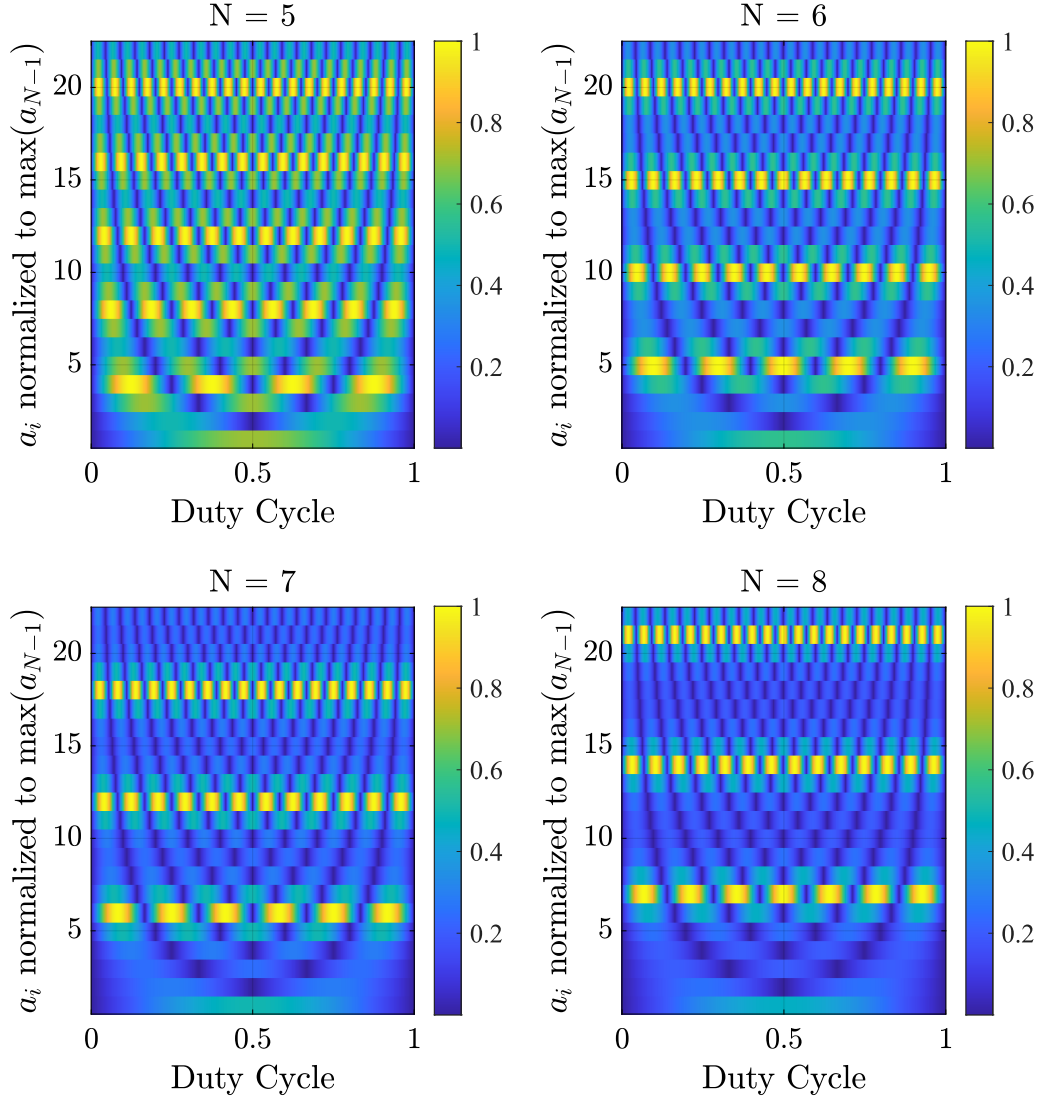


Figure 8.8: For a range of level counts, the magnitude of each harmonic $a_{\text{CM},i}$ for $i \in [1, 22]$ normalized to the maximum harmonic at $a_{\text{CM},N-1}$ for $N \in [5, 8]$. This shows more specifically that duty cycle is the primary contributor to relative harmonic magnitude, but each FCML level count has its own unique footprint centered around harmonics of the effective frequency, $a_{\text{CM},N-1}$.

To better understand the role of duty cycle and level count on harmonic content, the magnitude of the harmonics at the frequency $f_{\text{eff}} = (N - 1)f_{\text{sw}}$ is further explored. The harmonic magnitudes in (4) are computed for $a_{\text{CM},1}$ and $a_{\text{CM},N-1}$ for the full range of duty cycles and normalized over the maximum case for $a_{\text{CM},N-1}$. This is shown in Fig. 8.7 for a 6-level converter, and showcases that as the duty cycles approach the midpoints between fractional phase-shift values used to gate the FCML converter switches, these harmonics are substantially maximized.

To more generally explore this effect for other level counts, harmonic magnitudes are calculated and normalized to the $a_{\text{CM},N-1}$ case. From this, there are a few observations. Harmonics are minimized for specific duty cycles, irrespective of level count. However, maximum harmonic magnitudes occur at harmonics of $(N - 1)f_{\text{sw}}$ for duty cycles at $D = \frac{k}{2(N-1)}, k \in [1, N - 2]$. This phenomenon is shown in Fig. 8.8. This plot shows that while the global shape of the spectrum is the same across level counts, the relative harmonic magnitudes create a unique frequency domain signature for each level count of the FCML converter. From the plot in Fig. 8.8, we also can use the observation that $a_{\text{CM},1}$ is maximized at $D = 0.5$ across all level counts to investigate how the fundamental harmonic changes as we increase level count.

8.3 Hardware Validation of Model

Hardware Design

Thus far, we have provided analytical expressions for the CM EMI generated in the switching stage of the FCML converter. Hardware validation requires care, as CM EMI is primarily associated with parasitic effects in the hardware itself. To isolate the noise created at each switching node, careful attention was paid to the design of the overall converter to eliminate CM noise from the gate drive circuitry, and to minimize uncontrolled and asymmetric parasitic capacitances. The hardware prototype on the pre-compliant EMI test bench is shown in Fig. 8.9. Design details for the PCB are provided in Appendix A. To validate the scaling trends presented in this work, a 6-level FCML converter was designed to be easily outfitted with a grounded heat sink. Each switching cell was designed to be symmetric to the adjacent one. Each commutation loop was designed with decoupling capacitors placed in a lateral configuration, a common choice for FCML converter designs [130]. A copper plane in the PCB layer below the commutation loop provided sufficient overshoot management but incorporated enough typical circuit parasitics to be representative of other FCML converter designs.

Gate Drive Considerations

The gate drive design was powered through a cascaded bootstrap circuit with low EMI footprint gate drivers and isolators to avoid high-frequency noise stemming from the gate drive circuitry [51]. The LMG1020 gate drivers are in a ball grid array package with a small

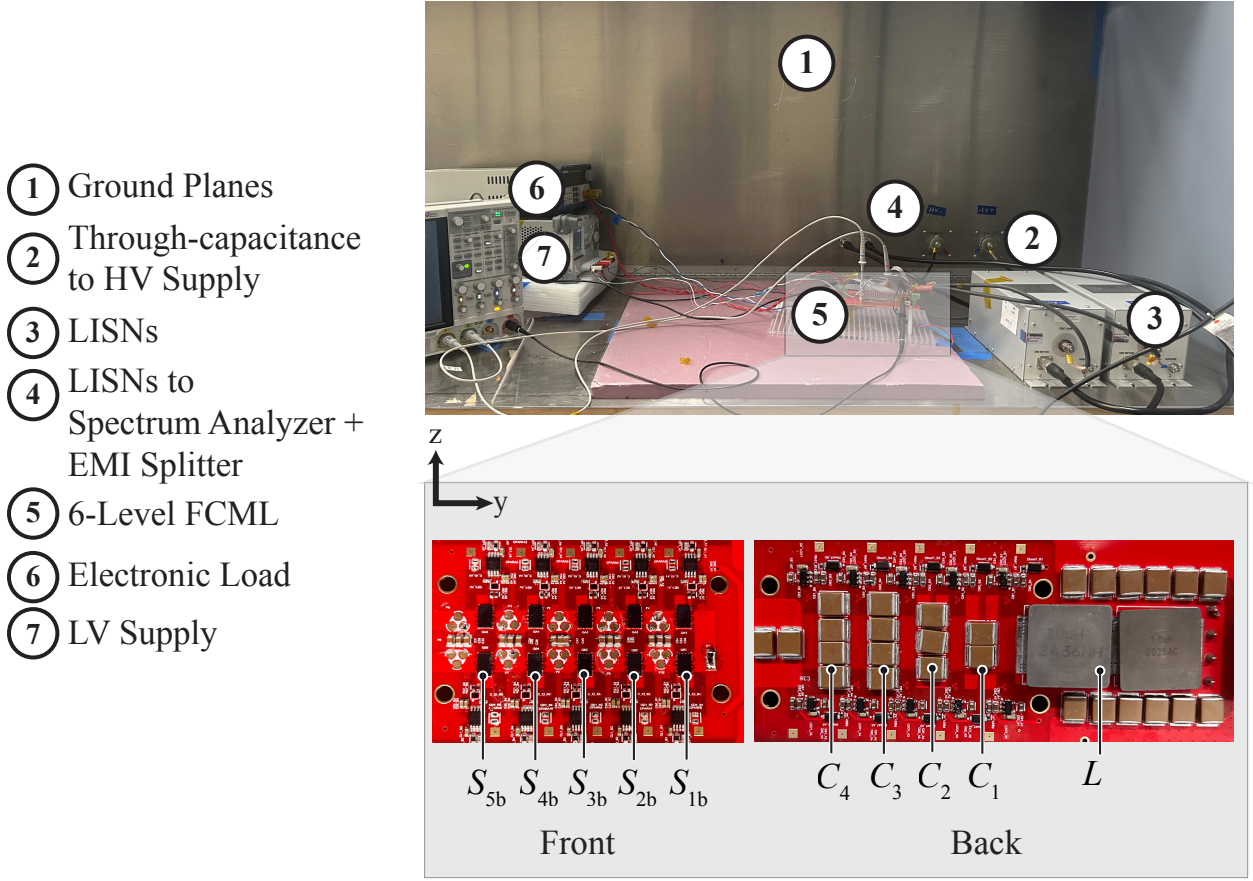


Figure 8.9: Labeled EMI test bench setup and associated hardware prototype.

Table 8.1: 6-Level FCML Converter Operating Parameters

Parameter	Value
V_{in}	100 V
v_{out}	10 - 90 V
i_{out}	2 A
f_{sw}	160 kHz

footprint. Paired with good layout, these enable high switching transitions with minimal insertion parasitics. The required digital isolators for each switching cell are realized with IL710 high-speed single-channel digital isolators. These devices are characterized by having low EMI, as they do not have a carrier or clock. They use an alternative magnetoresistive technology [131]. The intentional choice of the active gate drive components to minimize EMI contributions from the gate drive circuit combined with the decision to utilize a boot-

Table 8.2: Component Listing of the Hardware Prototype

Component	Mfr. & Part Number	Parameters
FCML Power Stage		
Switches	EPC 2305	GaN, 150 V, 2.2 m Ω
Flying Capacitance C_{fly}	TDK C5750X6S225K250KA	2.2 μF , 450 V
Local Decoupling Capacitance	TDK C2012X7T2W473K125AA	47 nF, 450 V
Inductance L	Vishay IHL6767GZER100M1A, IHL6767DZER1R0M01	11 μH , 9.7 m Ω
Gate Drive		
Gate Drivers	TI LMG1020	7 A / 5 A, single channel
LDO	TI LP2985AIM5X-5.0	5 V, 150 mA
Digital Isolators	NVE IL710	2500 V _{rms} isolation
Bootstrap Diode	Vishay 2EQH02HM3	200 V, 2 A
Controller Board		
Microcontroller	TI TMDSCNCD28379D	C2000 MCU

strap power supply enabled minimal gate drive noise to couple into the power stage. The components used for the power stage and the gate drive are provided in Table 8.2.

Heatsink Design and Mounting

The heatsink in this work, designed by Marrin Nerenberg, was designed to cover just the transistors, as those were determined to be the key thermal limiting factors for the FCML converter designed. The heatsink along with relevant parameters are shown in Fig. 8.10. The heatsink was attached to the converter with a 0.5 mm thermal interface material (TIM) ($\epsilon_r = 2 - 4$) placed between the top of the GaNFET (EPC 2305) package (source potential) and the grounded heatsink. The heatsink was mounted using the four through-holes at the corners of the sink and in the PCB. Using 3 mm diameter screws, a nut was used on the bottom side of the board to affix the heatsink to the PCB. We were careful to ensure that the nut placement on each screw was the same on each corner, so that the distance between each device and the heatsink was uniform for the 6-level converter. The selected GaNFETs have a bare-die area of 11.6 mm² which results in an estimated parasitic capacitance to chassis of $C_p \approx 0.4$ pF per FET source.

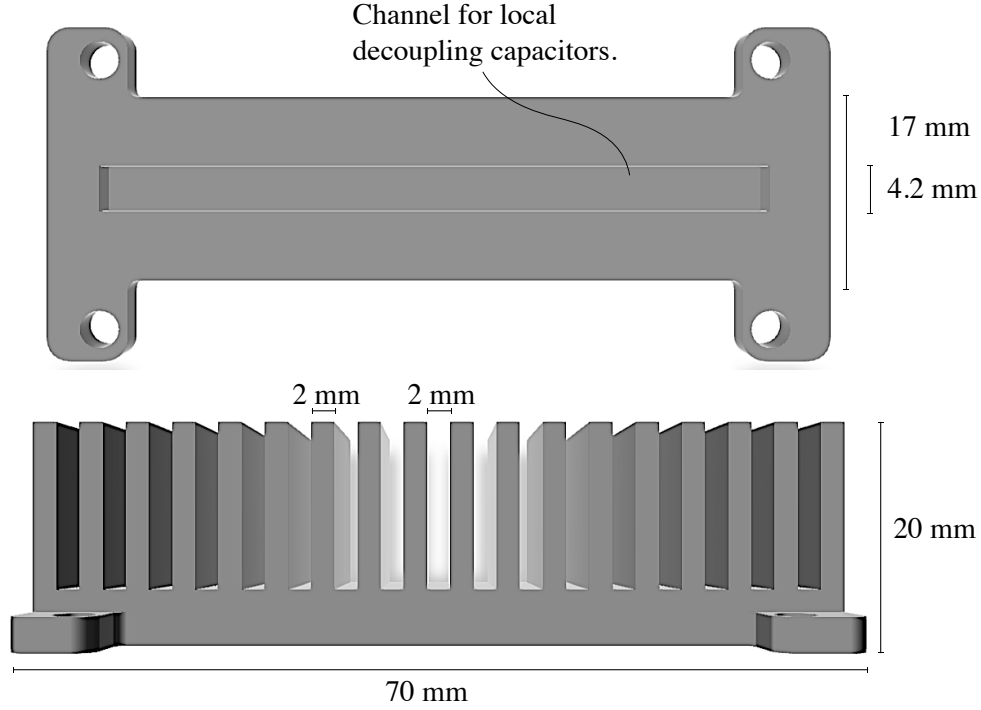


Figure 8.10: 3-D rendering of heatsink with relevant dimensions shown. The heat sink is attached to the converter via 3 mm screws.

Time-Domain Hardware Results

For the time-domain hardware validation, the outputs of the LISNs were supplied to a EMI signal splitter (TBLM1 LISN Mate) and a $50\,\Omega$ probe terminal on a 200 MHz Keysight MSOX4024A oscilloscope. The drain-to-source voltage of low-side switch S_{5b} was measured to identify the timing of the first switch-pair turn on. The necessary rise and fall times of the drain-to-source voltages needed to evaluate (8.5) were extracted from this measurement.

The rise and fall times are conventionally varied by the choice of external gate resistances R_g used to control t_r and t_f . These rise and fall times may be estimated, respectively, as

$$t_r \approx \frac{R_{g, \text{off}} Q_{gd}}{v_{pl}}. \quad (8.6)$$

and

$$t_f \approx \frac{R_{g, \text{on}} Q_{gd}}{v_{gs} - v_{pl}}. \quad (8.7)$$

Based on the gate resistances of $R_{\text{off}} = 5\,\Omega$ and $R_{\text{on}} = 22\,\Omega$ respectively, we compute rise and fall times of 6.75 ns and 22 ns based on the expressions in (8.6) and (8.7). For the EPC 2305 at $v_{ds} = 20\,\text{V}$, the gate-to-drain charge is approximated as $Q_{gd} = 3\,\text{nC}$. The Miller

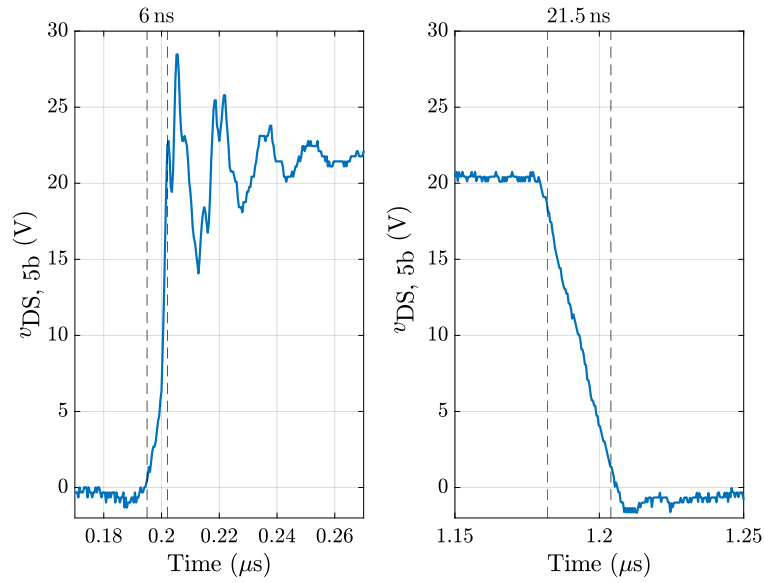


Figure 8.11: Measured rise and fall times of the low-side drain-to-source switch S_{5b} .

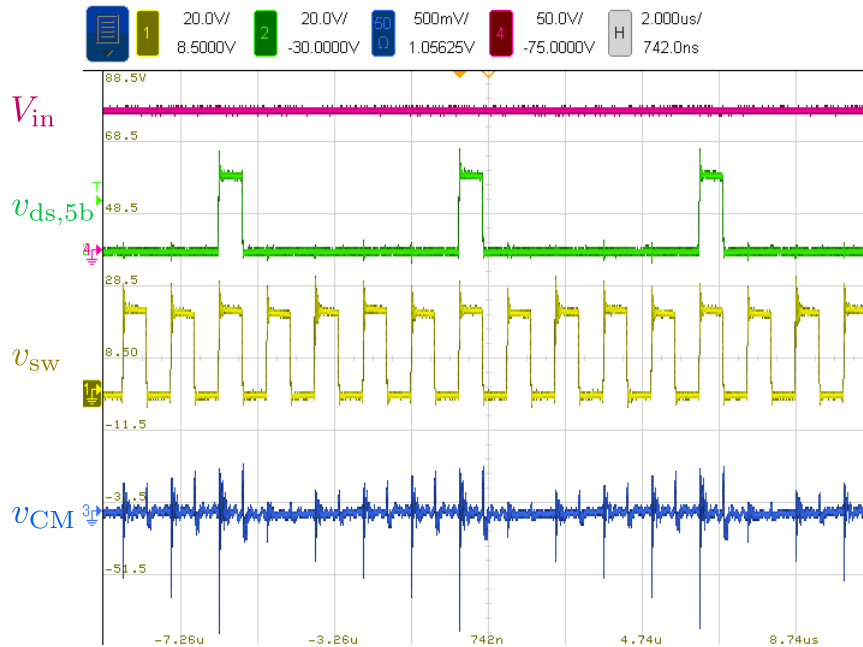


Figure 8.12: Oscilloscope waveforms showing the measurement of the common-mode voltage across the $50\ \Omega$ terminal of the EMI splitter.

plateau voltage is $V_{pl} \approx 2\text{ V}$. In Figure 8.11, we showcase measured rise and fall times of 21.5 ns and 6 ns corresponding to 2.3 % and 11 % errors between measured and calculated values.

The time-domain measurements are shown in Fig. 8.12. Excellent theoretical matching is observed, confirming that the parasitic capacitances that generate common-mode currents can be modeled at the switching cell level. Furthermore, the unique linear FCML converter CM current peak scaling is observed across each full period. Calculated currents are compared to measured currents in Fig. 8.13 and show that the proposed approach captures the full CM behavior for the FCML converter in the time domain.

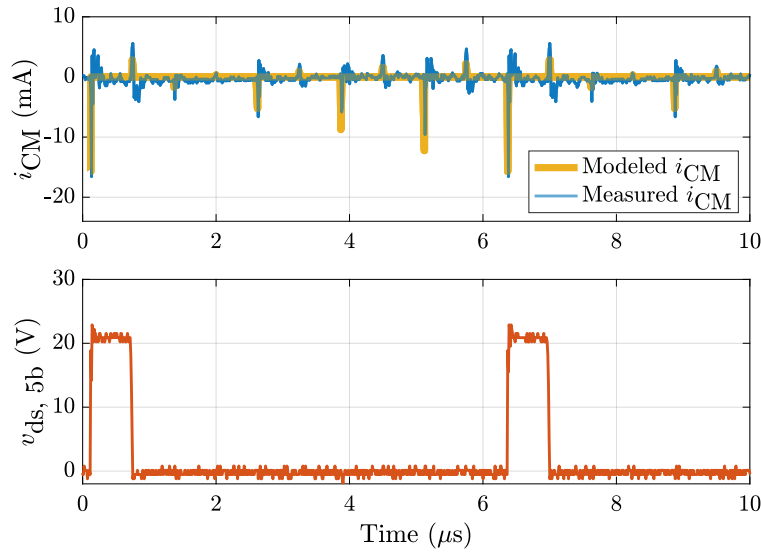


Figure 8.13: Comparison of measured and calculated time domain CM currents for $D = 0.1$. Clear matching is observed.

Frequency-Domain Results

In addition to time-domain data, hardware results were obtained in the frequency domain using the EMI test setup in Fig. 8.9 and a Tektronix RSA306B digital spectrum analyzer. In Fig. 8.15 and Fig. 8.17, EMI results at $D = 0.2$ and $D = 0.8$ respectively are shown for both a 2 A load and a no-load condition. This shows the condition when the converter is operating at a nominal duty ratio, which results in the cancellation of the 5th harmonic for the 6 level converter. In Fig. 8.14 and Fig. 8.16, EMI results at $D = 0.1$ and $D = 0.5$ are shown. We see the maximization of the 5th harmonic in these cases. In the case for $D = 0.5$, we also note the expected cancellation of even harmonics.

Since CM EMI is predominately generated as a result of unwanted parasitic capacitances and dv/dt events, there is not a substantial difference between loaded and non-loaded converter operation with respect to total capacitive leakage currents. One observation in the

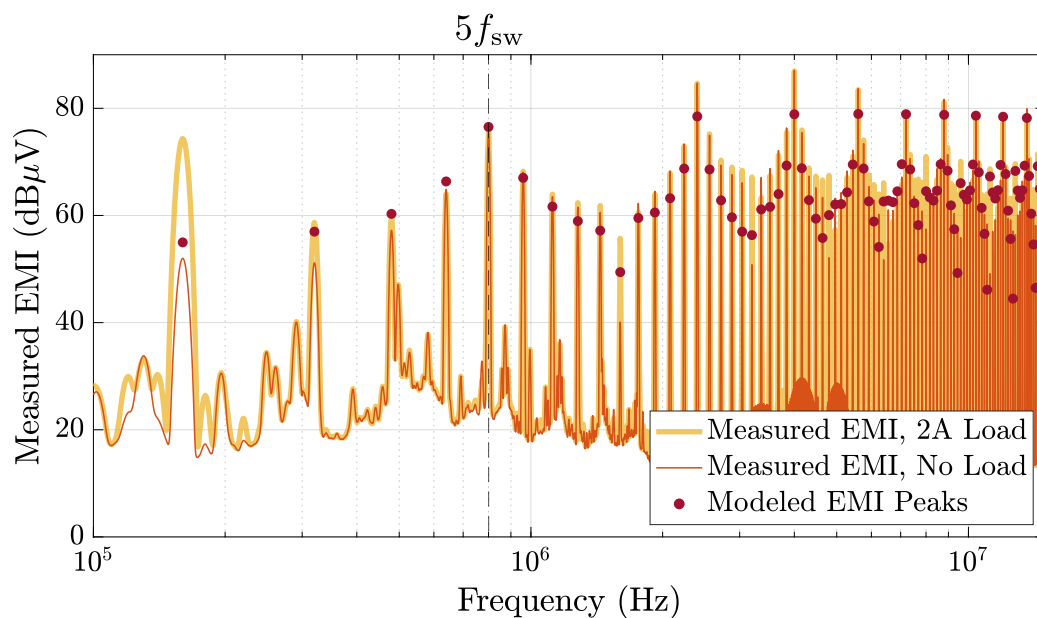


Figure 8.14: Frequency domain data for $D = 0.1$ showing spectrum for a 2 A load and for the unloaded circuit, compared to modeled peaks.

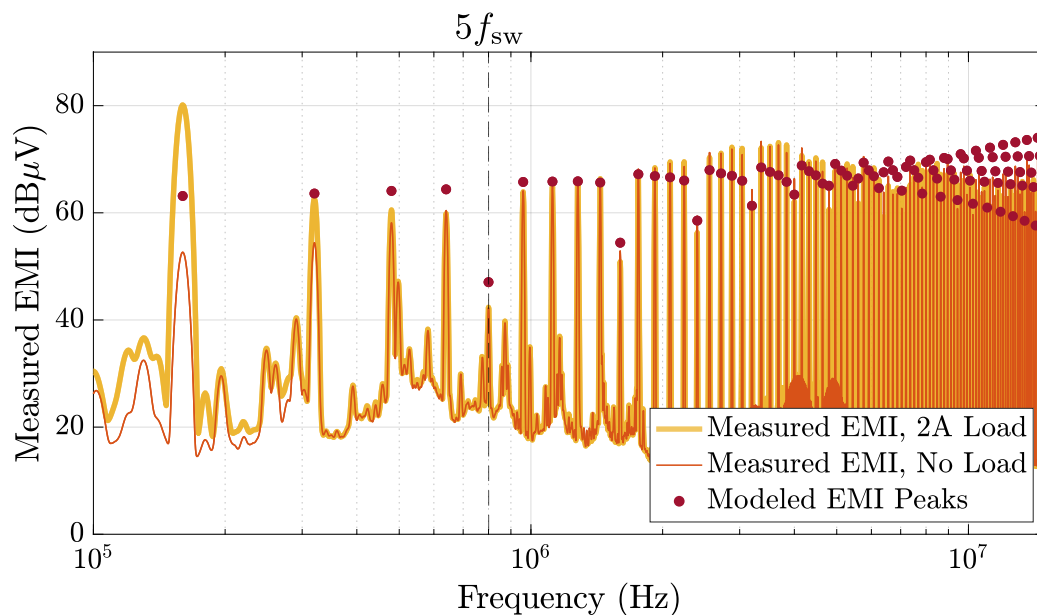


Figure 8.15: Frequency domain data for $D = 0.2$ showing spectrum for a 2 A load and for the unloaded circuit, compared to modeled peaks.

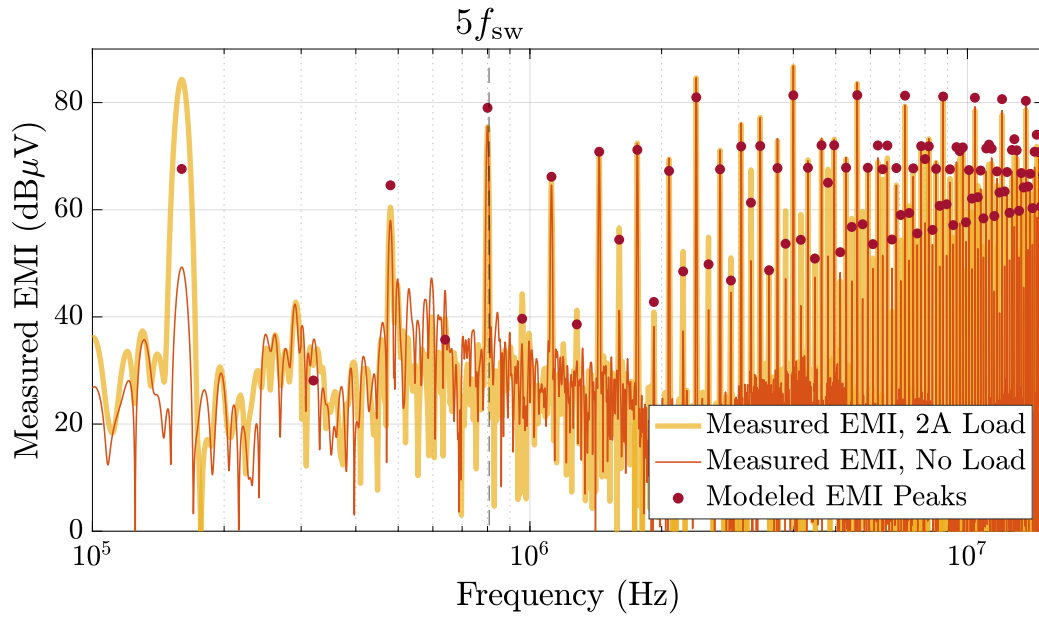


Figure 8.16: Frequency domain data for $D = 0.5$ showing spectrum for a 2 A load and for the unloaded circuit, compared to modeled peaks.

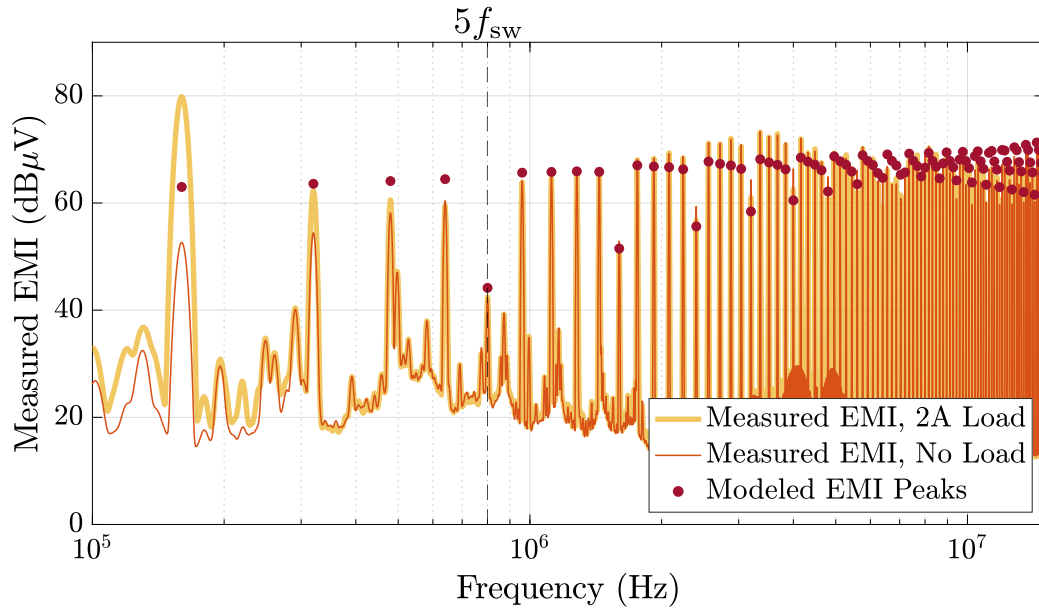


Figure 8.17: Frequency-domain data for $D = 0.8$ showing spectrum for a 2 A load and for the unloaded circuit, compared to modeled peaks.

time domain was a small triangular voltage waveform present in v_{CM} at the terminals of the LISNs. This is visible in Fig. 8.12, and results from current draw through mismatched LISN and cabling parasitics. The outcome of this triangular current is additional frequency content dominating the first harmonic at f_{sw} when the converter is loaded.

The modeled common-mode current magnitudes at each frequency were multiplied by corresponding points in the frequency-dependent LISN impedance curve to ascertain matching between measured and theoretical results. These scaled points are added to the measured noise floor in Fig. 8.14, Fig. 8.15, Fig. 8.16, and Fig. 8.17. The inclusion of data for the duty cycle of $D = 0.8$ in Fig. 8.16 showcases harmonic cancellation for the nominal duty cycle $D = 0.8 = \frac{4}{5}$, as predicted in the plot in Fig. 8.7. The global shape of the frequency content in both plots matches the theoretical results very well, particularly in the unloaded case. In the higher frequency domain, there is less overlap between the theoretical model and the measured spectra. This is likely a combined result of the measurement setup and unmodeled parasitics changing the frequency envelope shape. Since higher-frequency content is generally easier to remove with a low-pass filter, good matching in the lower range offers sufficient information to devise a CM EMI mitigation strategy.

Sources of Measurement Error

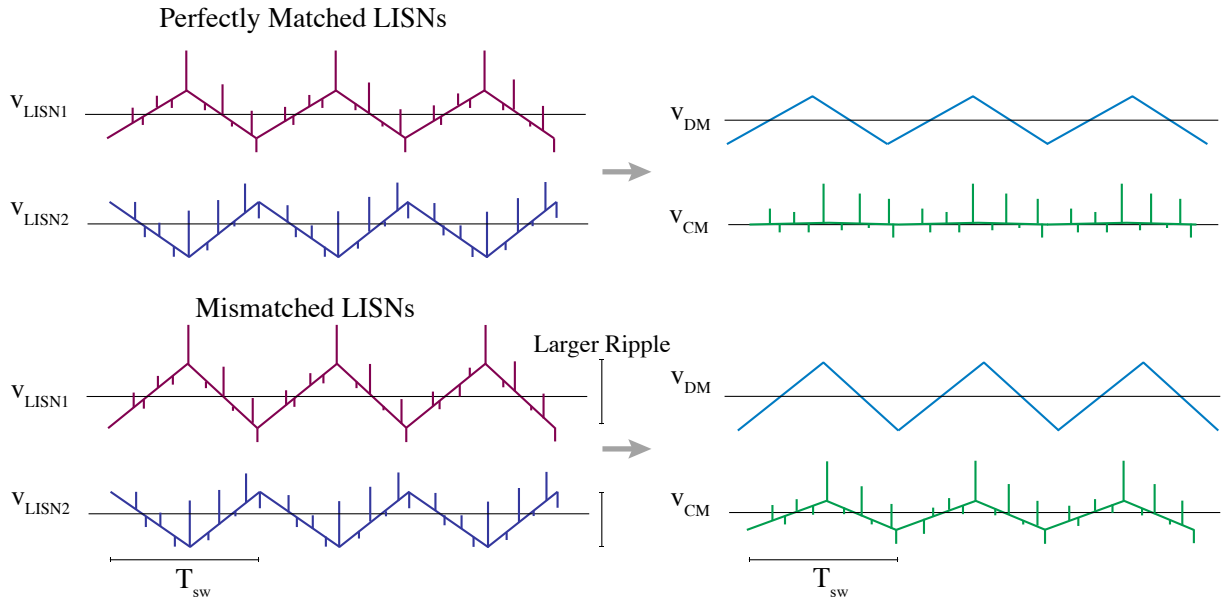


Figure 8.18: Qualitative diagram showing the measured LISN voltages across the 50Ω terminations and the resulting CM and DM components. If the LISNs have mismatched impedances, they will ripple with different magnitudes, resulting the presence of a triangular waveform in the CM voltage measurement.

We noted that the unloaded converter had a substantially smaller measured fundamental CM harmonic compared to the loaded converter case. When the circuit is unloaded, parasitic mismatches in the LISNs, cabling, and PCB do not substantially impact the CM spectrum, as only CM current spikes generated by voltage events are present [132]. To better understand the large fundamental magnitude occurring in the loaded circuit, we took additional measurements in the time and frequency domains under different loading scenarios.

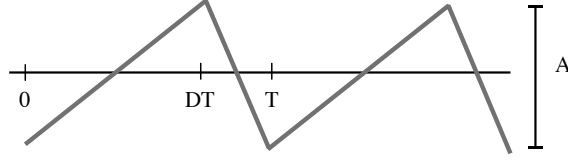


Figure 8.19: Periodic triangular waveform with asymmetric rising and falling edge slopes defined by the duty cycle D , and amplitude A .

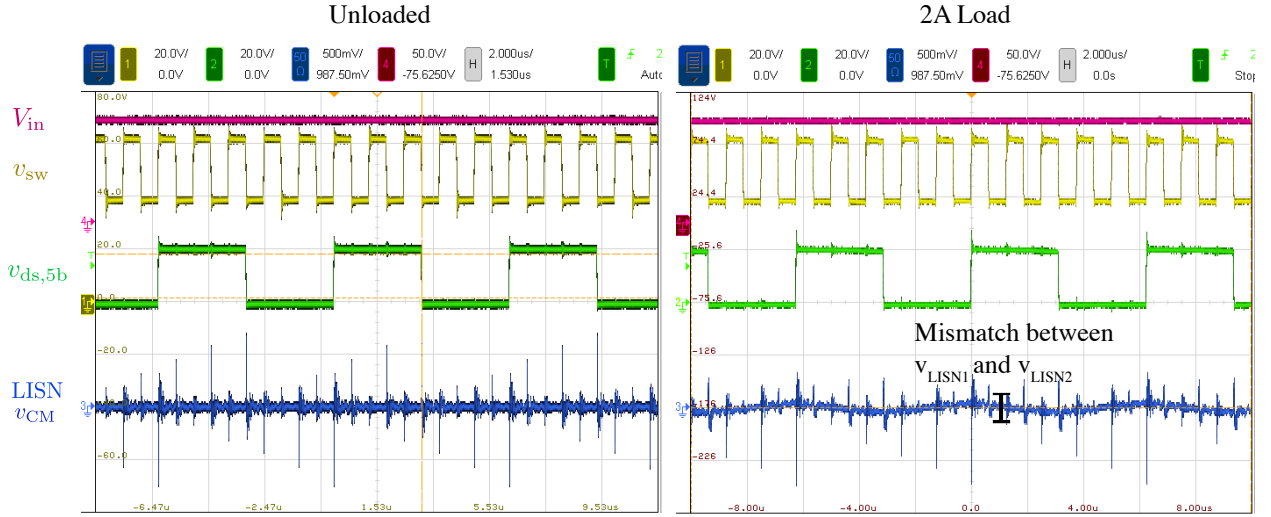


Figure 8.20: Oscilloscope plots showing the measured CM voltage. On the left, we view the unloaded case, showing no additional triangular waveform in the CM voltage measurement. On the right, we can see that parasitic mismatches result in a small triangular component in the CM voltage measurement when the converter is loaded with 2 A.

A key source of error we consider is an impedance mismatch between the two LISN paths. If the off-the-shelf LISNs, and connected cables are perfectly matched, the voltages across their $50\,\Omega$ terminations, when summed, will result in a sequence of periodic CM spikes centered around zero. If either the LISNs, or the cables feeding the LISNs have mismatched impedances, they will conduct different currents [133], and the sum of the voltages across the $50\,\Omega$ terminations will result in a CM voltage with a triangular component. This will be

further exacerbated with current flowing through the converter [134]. Fig. 8.18 conceptually shows the sum of LISN output voltages, and how a triangular voltage may form in the CM EMI measurement. Because the amplitude of the triangular waveform in v_{LISN1} is larger than the triangular component in v_{LISN2} , we observe an unwanted triangular component in v_{CM} .

To understand the expected impacts of this LISN path mismatch in the frequency domain, we can incorporate the fundamental components of the resulting triangular waveform derived from the time-domain CM measurement. For a periodic triangular waveform with asymmetric rising and falling edge slopes defined by the duty cycle D , as shown in Fig. 8.19, the Fourier coefficients for a given harmonic k associated with the sine term are given by

$$a_{\text{tri},k} = \frac{A}{\pi^2 k^2 D(1-D)} \sin(k\pi D). \quad (8.8)$$

Using the hardware prototype, we verify the existence of the triangular voltage present in v_{CM} . For the case where $D = 0.2$, if we use the time-domain oscilloscope data, we find that the amplitude of the current across the 50Ω termination is estimated to be 1 mA.

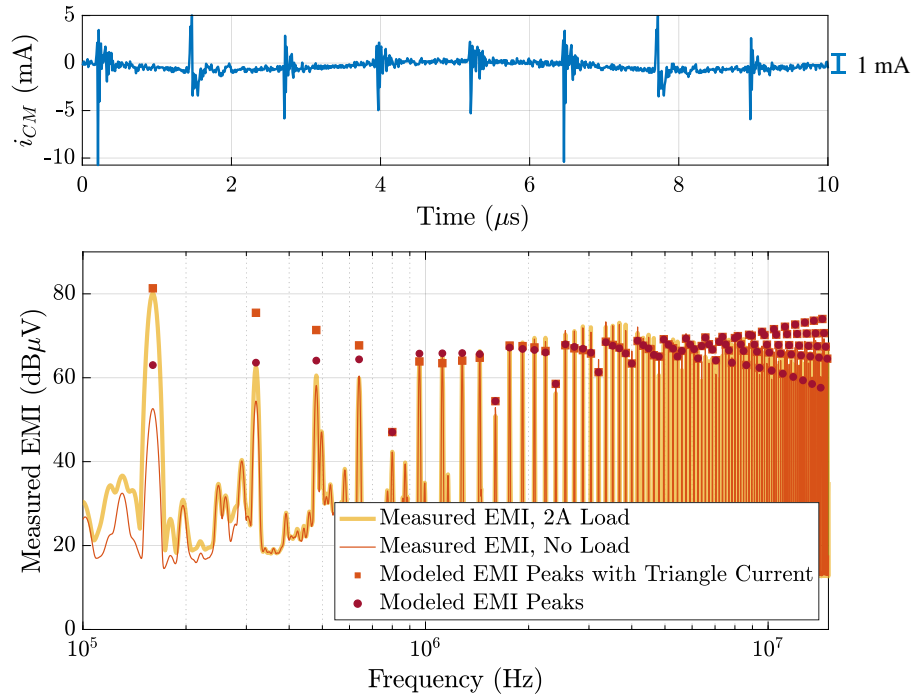


Figure 8.21: Top: Common-mode current showing presence of dominant triangular waveform at the switching frequency. The estimated amplitude of 1 mA is labeled. Bottom: We include the impact of affiliated harmonics from this current added to the modeled results. We see that when the converter is loaded, that low-frequency harmonics resulting from this triangular current dominate the fundamental magnitude.

This is shown and labeled in the measured time-domain waveform of i_{CM} in Fig. 8.21. Using (8.8), we can compute and add these harmonic magnitudes to the modeled CM EMI peaks. The resulting points are shown in the bottom EMI plot in Fig. 8.21. We see that these dominate the lower-order harmonic magnitudes, resulting in the measurements differing quite drastically for the loaded converter case. Because of the k^2 term in the denominator of (8.8), the impact of this current rolls off quickly. After the 5th harmonic or so, the computed harmonics with this error incorporated overlap with the modeled CM harmonics.

The other possible source of measurement error is the “noise floor” present in the EMI measurement test setup. This slightly variable baseline may further exacerbate the mismatch between modeled and measured results. We measured the noise floor both when the gate drive circuit was powered and when it was not. As shown in the top plot in Fig. 8.22. When the gate drive is powered, we see some harmonic content at the switching frequency in the noise floor. However, when we add each noise floor to the modeled results, we see that there are not ample differences between the two cases. We thus conclude, that both the noise floors and the gate drive noise do not contribute large discrepancies between modeled and measured results.

Considering possible sources of measurement error enables us to determine with more confidence that this model provides a good estimate of CM EMI in the FCML converter. EMI is inherently challenging to quantify with a pre-compliant test bench. Between the variable noise floor and parasitic mismatches in the LISN and cabling, there are many challenges

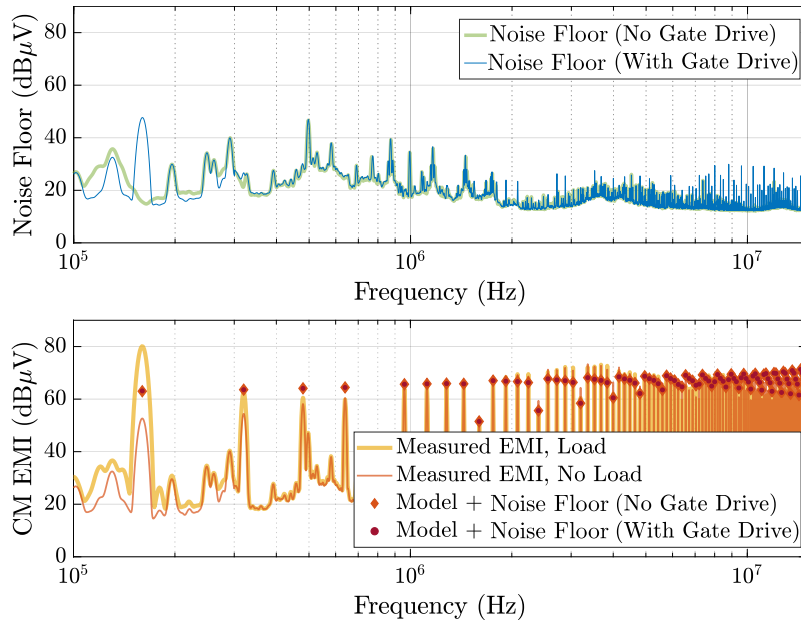


Figure 8.22: Top: Measured noise floor with and without gate drive power. Bottom: We add the impact of each noise floor to the modeled frequency-domain results for $D = 0.2$ and compare this to the measured EMI.

presented. The hardware results match quite well in this section, and provide sufficient validation of model accuracy in both the time and frequency domains.

8.4 Concluding Remarks

In this chapter, we defined the assumptions and level of detail required to model CM EMI effectively in the FCML converter. An analytical model was developed and validated in a 6-level FCML converter prototype. This model provides sufficient information to investigate how CM EMI scales with level count, and ascertain if there are benefits or drawbacks of the topology compared to a conventional 2-level converter design. In the next chapter, we perform this comparison, and develop a greater understanding of how the FCML converter propagates CM EMI.

Chapter 9

On the Scaling of Common-Mode EMI in the FCML Converter

Executive Summary

This chapter uses the model presented in Chapter 8 to analyze the impact of FCML level count on CM EMI in the FCML converter. The model in Chapter 8 enables the rapid calculation of harmonic signatures, which is used here to assess CM EMI as a function of semiconductor die area. We find that the FCML converter has superior EMI compared to the 2-level buck converter, even as the level count is increased. This improvement is enabled through the availability of superior semiconductor switches at lower voltage ratings.

9.1 General Level Count Exploration

Generalized Harmonic Scaling

To begin comparing CM EMI between FCML converter level counts, we contextualize and describe CM EMI for GaN-based N-level converters. Because EMI filters often must be designed around the fundamental component magnitude at the switching frequency, we use this fundamental component magnitude as a basis for comparison. This chapter begins with the evaluation of (8.5) for the harmonic $k = 1$.

The 2-Level Converter

The 2-level converter has a peak fundamental harmonic at the switching frequency $f_{sw, 2L}$. The magnitude of this fundamental harmonic can be ascertained by substituting $N = 2$ and

$k = 1$ into (8.5). We define the 2-level converter switching period as $T_{\text{sw},2\text{L}}$.

$$a_{\text{CM},1} = -\frac{2 \cdot M_{\text{f},1}}{\pi} \sin\left(\pi \frac{t_{\text{f}}}{T_{\text{sw},2\text{L}}}\right) e^0 + \frac{2 \cdot M_{\text{r},1}}{\pi} \sin\left(\pi \frac{t_{\text{r}}}{T_{\text{sw},2\text{L}}}\right) e^{-j(D + \frac{t_{\text{r}}}{2T_{\text{sw},2\text{L}}} - \frac{t_{\text{f}}}{2T_{\text{sw},2\text{L}}})2\pi} \quad (9.1)$$

We can further simplify the magnitude in (9.1) if we assume that the rise and fall times t_{r} and t_{f} are a relatively small percent of the switching period. For a GaN HEMT with rise/fall times in the range of 5 - 100 ns and switching speeds in the hundreds of kHz or slower (i.e., switching periods on the order of thousands of ns), this assumption is reasonable. By the small angle approximation, for a small x , we can assume that $\sin(x) \approx x$. Here this translates to a drastic simplification for the two-level case in (9.2) where expressions for $M_{\text{f},i}$ and $M_{\text{r},i}$ from (8.4) are used.

$$a_{\text{CM},1}^{2\text{-level}} \approx \frac{2}{T_{\text{sw},2\text{L}}} V_{\text{in}} C_{\text{p}} (e^{-j2\pi D} - 1) \quad (9.2)$$

The magnitude of this expression can be further simplified as (9.3), and is maximized for $D = 0.5$. In this chapter, we consider this worst-case fundamental magnitude.

$$|a_{\text{CM},1}^{2\text{-level}}| \approx \left| \frac{4}{T_{\text{sw},2\text{L}}} V_{\text{in}} C_{\text{p}} \sin(\pi D) \right|. \quad (9.3)$$

The N-Level Converter

We can repeat the same simplification procedure for the N-level case to facilitate straightforward comparisons between level counts. For $k = 1$, and defining the switching period as $T_{\text{sw,NL}}$, we begin the simplification process to find

$$a_{\text{CM},1} = \sum_{i=1}^{(N-1)} -\frac{2 \cdot M_{\text{f},i}}{\pi} \sin\left(\pi \frac{t_{\text{f}}}{T_{\text{sw,NL}}}\right) e^{-j \frac{i-1}{N-1} 2\pi} + \frac{2 \cdot M_{\text{r},i}}{\pi} \sin\left(\pi \frac{t_{\text{r}}}{T_{\text{sw,NL}}}\right) e^{-j(D + \frac{i-1}{N-1} + \frac{t_{\text{r}}}{2T_{\text{sw,NL}}} - \frac{t_{\text{f}}}{2T_{\text{sw,NL}}})2\pi}. \quad (9.4)$$

Next, assuming that the rise and fall times t_{r} and t_{f} are a relatively small percent of the switching period, we can further simplify the above to

$$a_{\text{CM},1}^{\text{N-level}} \approx -\frac{2 \cdot V_{\text{in}} C_{\text{p}}}{T_{\text{sw,NL}}(N-1)} \sum_{i=1}^{(N-1)} (2i-1) e^{-j \frac{i-1}{N-1} 2\pi} + \frac{2 \cdot V_{\text{in}} C_{\text{p}}}{T_{\text{sw,NL}}(N-1)} e^{-j2\pi D} \sum_{i=1}^{(N-1)} (2i-1) e^{-j \frac{i-1}{N-1} 2\pi}. \quad (9.5)$$

For $N > 2$, the summation in this equation can be generally evaluated as

$$\sum_{i=1}^{(N-1)} (2i-1)e^{-j\frac{i-1}{N-1}2\pi} = \frac{2(N-1)}{e^{-2\pi j/(N-1)} - 1}, \quad (9.6)$$

which enables further simplification

$$a_{\text{CM}, 1}^{\text{N-level}} \approx \frac{4 \cdot V_{\text{in}} C_{\text{p}}}{T_{\text{sw}, \text{NL}}} \frac{e^{-j2\pi D} - 1}{e^{-j2\pi/(N-1)} - 1}. \quad (9.7)$$

Finally, for $N > 2$, we define

$$|a_{\text{CM}, 1}^{\text{N-level}}| \approx \left| \frac{4}{T_{\text{sw}, \text{NL}}} V_{\text{in}} C_{\text{p}} \frac{\sin(\pi D)}{\sin\left(\frac{\pi}{N-1}\right)} \right|. \quad (9.8)$$

Harmonic Simplification Summary

We can then summarize the magnitude of the worst-case fundamental harmonic in (9.9) for both the $N > 2$ and $N = 2$ cases.

$$|a_{\text{CM}, 1}^{\text{N-level}}| \approx \begin{cases} \left| \frac{4}{T_{\text{sw}, \text{NL}}} V_{\text{in}} C_{\text{p}} \frac{\sin(\pi D)}{\sin\left(\frac{\pi}{N-1}\right)} \right|, & N > 2 \\ \left| \frac{4}{T_{\text{sw}, 2\text{L}}} V_{\text{in}} C_{\text{p}} \sin(\pi D) \right|, & N = 2 \end{cases} \quad (9.9)$$

From (9.9), we see a fundamental magnitude that is highly dependent on the parasitic capacitance C_{p} . This capacitance is a function of the die area of the switch, with larger die areas yielding larger CM EMI.

In this analysis, we also consider the magnitude of the harmonic at the effective frequency f_{eff} of the FCML converter, or the $k = N - 1$ harmonic. In Section 8.3, we observed that the harmonics at $k = N - 1$ may be much larger than the fundamental harmonic, which may impact filter design. By extending the method used to obtain (9.9) for the $k = 1$ case, we 1) evaluate (8.5) for $k = N - 1$, and 2) apply the assumption that $t_{\text{r}}, t_{\text{f}} \ll T_{\text{sw}}$. This assumption enables the small angle approximation for all sinusoids, and eliminates fractions of $t_{\text{r}}, t_{\text{f}}$ to T_{sw} in the complex exponential terms. From these simplifications, we find the following:

$$|a_{\text{CM}, N-1}^{\text{N-level}}| \approx \begin{cases} \left| \frac{4(N-1)}{T_{\text{sw}, \text{NL}}} V_{\text{in}} C_{\text{p}} \sin(\pi D(N-1)) \right|, & N > 2 \\ \left| \frac{4}{T_{\text{sw}, 2\text{L}}} V_{\text{in}} C_{\text{p}} \sin(\pi D) \right|, & N = 2 \end{cases} \quad (9.10)$$

where the $N > 2$ case is maximized when $D = 1/(2(N-1))$. From (9.10), and as shown in the hardware validation in Section 2.3, this sinusoidal term in the approximation has the power to also eliminate the $k = N-1$ harmonic case for nominal duty ratios $D = \frac{l}{(N-1)}$, $l \in (1, N-2)$. Combined with a strategic choice in switching frequency, this fact can be used to further reduce EMI filter size.

In both (9.4) and (9.10), it can be observed that the harmonic magnitudes have an inverse linear relationship with the switching periods $T_{sw,2L}$ and $T_{sw,NL}$. To verify this linear scaling, the 6-level FCML hardware prototype presented in Chapter 8 was operated at a 50 V input and 25 V output. The converter was evaluated at three discrete switching frequencies: 160, 180, and 200 kHz. To visualize the expected linear magnitude scaling, absolute magnitude results for the common-mode voltage measured at the output of the EMI splitter are shown in Fig. 9.1 in millivolts for the first few harmonics. Clear positive linear trends are observed for each harmonic as the switching period is reduced, following the expected scaling behavior.

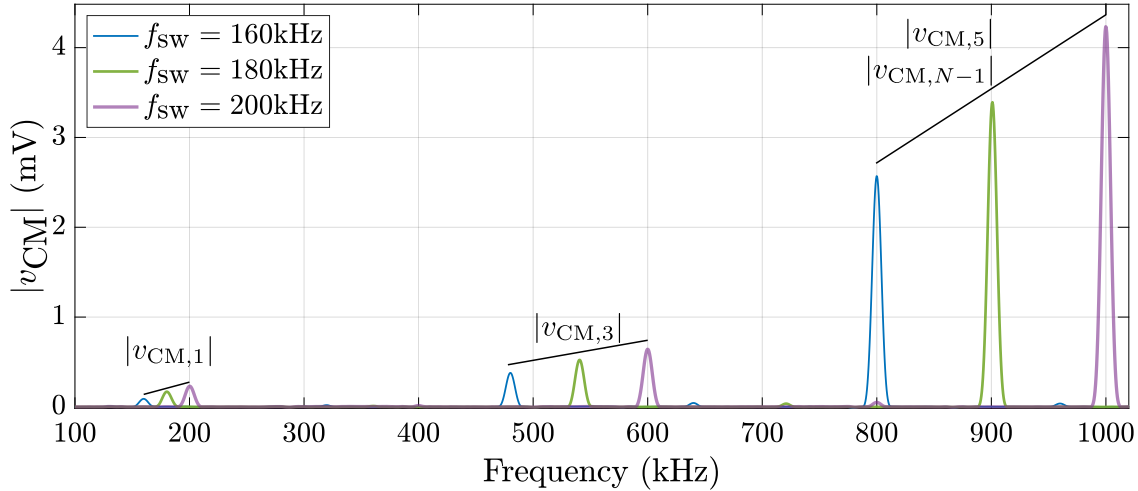


Figure 9.1: Measured CM voltage harmonics using the 6-level prototype from Chapter 8 at switching frequencies of 160 kHz, 180 kHz and 200 kHz showing a linear increase in harmonic magnitude as frequency increases. This scaling is consistent with the expectations set by the equations in (9.4) and (9.10).

The mathematical simplifications made to the low-frequency CM harmonics in this part enable a direct comparison between level counts. Rise and fall times have been decoupled from these calculations, which is consistent with the expectation that the logarithmic CM spectrum is relatively flat below the rise/fall time frequency $1/(\pi t_r)$, at which point the spectrum begins rolling off at -20 dB/dec [135]. Our simplifications reveal that only switching period and parasitic capacitance substantially impact low-frequency CM EMI results. Since parasitic capacitance can be approximated by semiconductor die area, it is now straightforward to make comparisons using available semiconductor data.

9.2 FCML Converter Level Count Comparisons

To better explore a possible relationship between level count and EMI performance, we investigate a set of possible FCML converter hardware configurations. We compare FCML converters that can be realized using surface-mount GaN switches to limit the possible semiconductors to one material. A dataset was aggregated using the datasheets of commercially available GaN devices. For the devices rated from 80 V to 200 V, Efficient Power Corporation devices are used, as these are typically packaged as bare die devices, or in Power Quad Flat No-Lead packages [136, 137], meaning the die area is synonymous with the cooling area of the package. For devices ≥ 650 V, devices from different manufacturers were purchased from Digikey/Mouser, common distributors of off-the-shelf components. These high voltage switches have larger physical packages and larger dedicated conductive cooling areas. To explore the theoretically ideal parasitic capacitances generated by 650 V devices, distilling the die area from external packaging allows for a fairer comparison to the lower voltage GaN devices used in this work. To obtain the die area, the external packaging was removed from the purchased devices. Once the package was opened, the total die area footprint was measured using digital calipers. Because the full length and width of the visible die were measured, these die area estimates are possibly conservative.

Table 9.1: Datasheet parameters and descriptions extracted for $n = 90$ GaN devices.

Parameter	Description
Manufacturer	EPC (< 650 V), Multiple Vendors (≥ 650 V)
V_B	Rated drain-to-source blocking voltage of the device.
I_{ds}	Rated continuous drain-to-source current of the device.
$R_{ds,on}$	Nominal on-state resistance of the device.
C_{oss}	Output capacitance of the device.
Q_{oss}	Output charge of the device.
Q_g	Total gate charge of the device.
Q_{gd}	Rated gate-to-drain charge of the device.
V_{pl}	Plateau voltage found by interpolating the voltage plateau in datasheet plots of gate-to-source voltage v_{gs} vs. Q_g .
A_{die}	Die area.
A_{cool}	Cooling area.

Later in this analysis, we examine discrete implementations of FCML converters where

the full package cooling area is used, as the die area is much smaller than the full package for the high voltage GaN devices. Analyzing discrete converter implementations enables a comparison that can be made using just datasheet parameters. Pertinent parameters are included in Table 9.1.

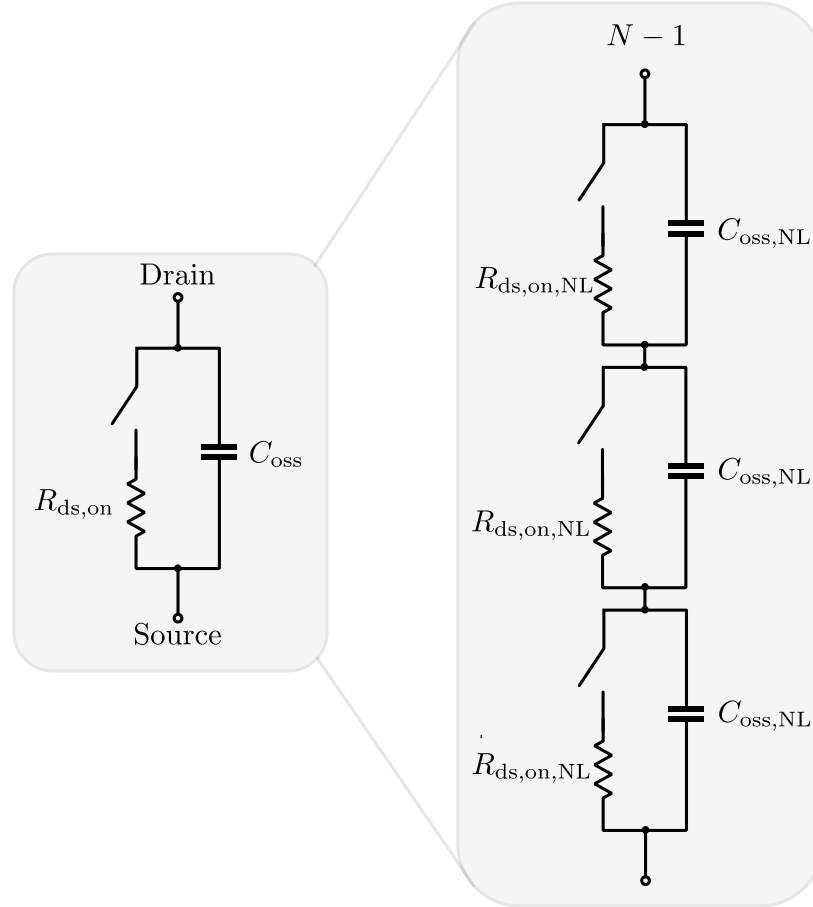


Figure 9.2: $N - 1$ serialized devices demonstrating the series connection of parasitic resistances and capacitances.

Die Area Informed CM EMI Scaling

To begin this analysis, die area must be related to the switch voltage rating. A canonical model of a switch is shown in Fig. 9.2 with two parasitic elements: on-state resistance $R_{ds,on}$ and output capacitance C_{oss} . A series-equivalent set of $N - 1$ switches is shown as an inset, which describes the replacement of the single switch with a multilevel series configuration of switches. Since both $R_{ds,on}$ and C_{oss} are dependent on the die area, we can use these parameters to relate die area to blocking voltage rating for GaN devices.

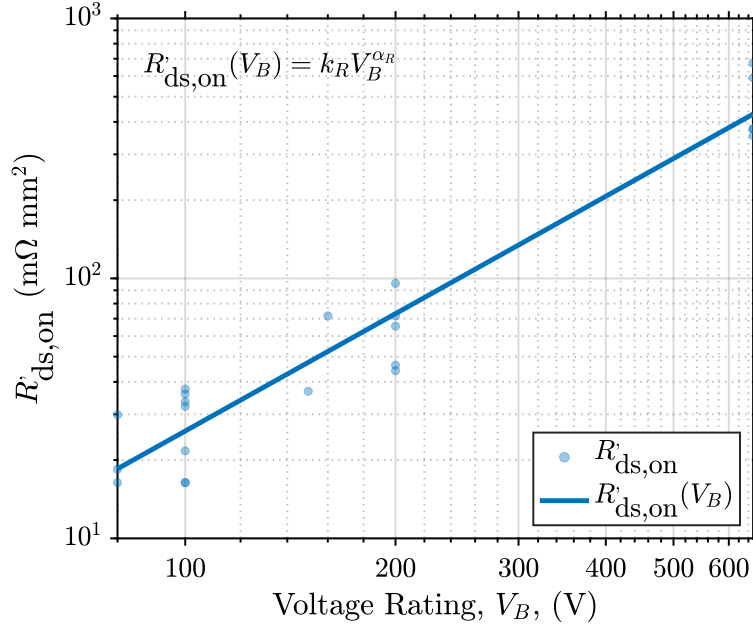


Figure 9.3: Plot of GaN specific on-resistance as well as fitted curve $R'_{\text{ds, on}}(V_B) \approx k_R V_B^{\alpha_R}$.

Area-specific on-state resistance, $R'_{\text{ds, on}}$, has a distinct relationship with blocking voltage [14]. For lateral GaN-on-Si HEMTs, the ideal on-resistance is approximated by

$$R'_{\text{ds, on}} = \frac{L_{\text{drift}}^2}{q\mu Q_s} = \frac{V_B^2}{q\mu Q_s E_{C,L}^2} \quad (9.11)$$

where L_{drift} is the drift region, $E_{C,L}$ is the critical electric field, μ is the free carrier mobility, and Q_s is the sheet carrier density [138, 139]. Because the ideal $R'_{\text{ds, on}} \propto V_B^2$, we can use device data to fit

$$R'_{\text{ds, on}}(V_B) \approx k_R V_B^{\alpha_R} \quad (9.12)$$

where the coefficient k_R is a constant, and we have a voltage scaling factor α_R , which we expect to be fairly close to 2 based on (9.11). In Fig. 9.3, we show this numerical fit evaluated for numerous commercial GaN devices between 80 V and 650 V. The rated continuous drain-to-source current is limited to being between 30 A and 60 A, which is set by the current ratings of the commercially available 650 V devices surveyed in this work. Here, we find $\alpha_R = 1.5$, which is lower than our theoretical expectation due to the very low on-state resistances of high voltage lateral GaN [14, 138].

As a device-informed scaling trend between specific on-state resistance and blocking voltage has been well established, we can then distill die area from this fit of specific on-resistance as

$$A_{\text{die}} \approx \frac{R'_{\text{ds, on}}(V_B)}{R_{\text{ds, on}}}. \quad (9.13)$$

Table 9.2: Extracted coefficients for the power-law fits of the form $R'_{\text{ds, on}}(V_B) \approx k_R V_B^{\alpha_R}$.

Fit	k	α	R^2
$R'_{\text{ds, on}}(V_B)$	0.0259	1.5	0.93

Using (9.12) and (9.13), for a given on-state resistance $R_{\text{ds, on}}$, we can compute A_{die} . For the design of a 400 V buck converter using GaN devices, we would use 650 V GaN switches. Among the commercially available GaN devices, an on-state resistance of approximately 50 m Ω is a fairly common choice, so it is used here as a baseline comparison number to which we compare multi-level converters. It should be noted here that the exact choice of this baseline resistance is not critical, as what we are after is the relative change to this number by the introduction of higher level count designs. We thus define $R_{\text{ds, on, 2L}} = 50 \text{ m}\Omega$. Subsequently, for an N-level FCML converter, we would want each device to have an on-state resistance of

$$R_{\text{ds, on, NL}} \leq \frac{R_{\text{ds, on, 2L}}}{N - 1} \quad (9.14)$$

so that when $N - 1$ devices are series-connected, we have the same (or less) equivalent on-state resistance as a 2-level converter. For a given power rating, this is the equivalent of fixing switch conduction losses.

Assessing the CM EMI performance of FCML converters with different level counts necessitates the use of appropriately rated switch blocking voltages for each design. For a given input voltage, we need to use switches with blocking voltage V_B rated for

$$V_B \geq \beta \frac{V_{\text{in}}}{N - 1} \quad (9.15)$$

where β is a term describing the overrate factor of the switch. Thus, for the multilevel converter case, we can compute the die area of a single switch:

$$\begin{aligned} A_{\text{die, NL}} &\approx \frac{k_R \left(\beta \frac{V_{\text{in}}}{N-1} \right)^{\alpha_R}}{\frac{R_{\text{ds, on, 2L}}}{N-1}} \\ &\approx \frac{k_R (\beta V_{\text{in}})^{\alpha_R}}{R_{\text{ds, on, 2L}}} (N - 1)^{1-\alpha_R}. \end{aligned} \quad (9.16)$$

The parasitic capacitance per switch for an N-level FCML converter is approximated as

$$C_p \approx \frac{A_{\text{die, NL}} \epsilon_r \epsilon_0}{d}, \quad (9.17)$$

where we assume the use of the same thermal interface material (fixed d and ϵ_r) for these surface-mount devices.

The Fundamental Harmonic

There are several informed choices of switching frequency, $f_{\text{sw, NL}}$, we can use to compare the fundamental CM magnitude of the FCML converter to the 2-level converter. If we hold the magnetic volume of the two converters constant, we should consider the volt-seconds across the main filter inductor. For the same inductance as a 2-level converter, L , the FCML converter has a switching frequency equal to

$$f_{\text{sw, NL}} = \frac{f_{\text{sw, 2L}}}{(N-1)^2}. \quad (9.18)$$

We start this analysis by inserting (9.18) and (9.17) into (9.9). In this analysis, we consider switches that are overrated by $1.25 \leq \beta \leq 1.63$. Here, the upper limit $\beta = 1.63$ is derived from the overrating of the 650 V GaN for a converter with $V_{\text{in}} = 400$ V. These parameters are summarized in Table 9.3.

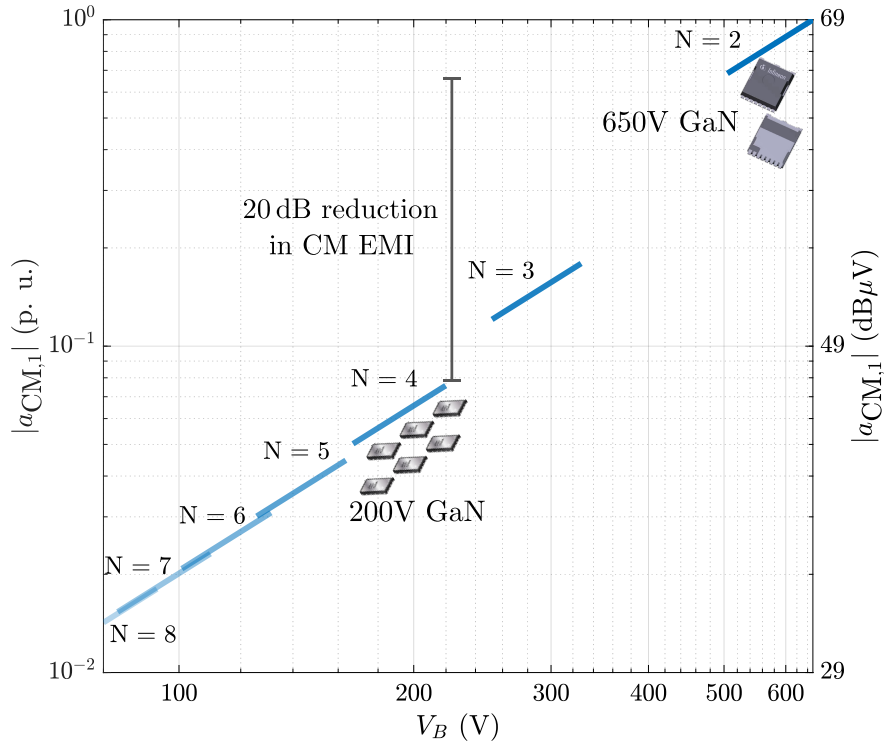


Figure 9.4: Plot of maximum fundamental harmonic magnitude for level counts between $N = 2$ and $N = 8$ computed by predicting $C_p \approx \frac{A_{\text{die}}(V_B)\epsilon_r\epsilon_0}{d}$ for $f_{\text{sw, 2L}} = 160$ kHz and $f_{\text{sw, NL}}$ is found by (9.18). We showcase these magnitudes computed relative to the maximum value for the 2-level case, but also in terms of $\text{dB}\mu\text{V}$. We highlight the 20 dB reduction in fundamental harmonic magnitude between the best 2-level converter and the worst 4-level FCML converter realized with high performance GaN devices.

Table 9.3: Key Parameters for CM Harmonic Magnitude Predictions

Parameter	Description
V_{in}	400 V
N	$N \in [2, 8]$
$f_{\text{sw}, 2\text{L}}$	160 kHz
β	$1.25 \leq \beta \leq 1.63$
C_{p}	Predicted as a function of $R'_{\text{ds,on}}$ when $R_{\text{ds,on}, 2\text{L}} = 50 \Omega$

The maximized fundamental harmonic magnitude is approximated for level counts between $N = 2$ and $N = 8$ in Fig. 9.4. For each level count, the range of allowable blocking voltages set by β are shown as a continuous line. Here, the fundamental harmonic magnitude is normalized to the maximum magnitude for the 2-level converter case. We see drastic improvements for the multilevel converter case, even as the level count is increased. While the total number of switches is increased, the reduced required die area per device, the distributed switching behavior, and the reduction in $f_{\text{sw,NL}}$ all result in an improved CM EMI scaling with level count when evaluating (9.9).

While a fixed magnetic volume is often a metric for comparison between different level-count FCML converters, we expand this analysis by considering two other feasible switching frequency cases for FCML converter design. Many high-density FCML converter designs that utilize wide-bandgap devices can switch in the hundreds of kilohertz. It is possible to switch many of these devices fast while still achieving high efficiencies. Subsequently, the inductor volume may be decreased as the frequency of the switch node is defined as $f_{\text{eff}} = f_{\text{sw}} \cdot (N - 1)$. We thus consider the fundamental harmonic of CM EMI for the cases where the FCML converter is switched at 1) $f_{\text{sw}, \text{FCML}} = \frac{f_{\text{sw}, 2\text{L}}}{(N-1)}$ and 2) $f_{\text{sw}, \text{FCML}} = f_{\text{sw}, 2\text{L}}$. When $f_{\text{sw}, \text{FCML}} = \frac{f_{\text{sw}, 2\text{L}}}{(N-1)}$, the inductor is reduced by a factor of $(N - 1)$ compared to the 2-level converter, and when $f_{\text{sw}, \text{FCML}} = f_{\text{sw}, 2\text{L}}$, the inductor is reduced by a factor of $(N - 1)^2$.

For a 400 V converter, we evaluate the cases when $f_{\text{sw}, \text{FCML}} = \frac{f_{\text{sw}, 2\text{L}}}{(N-1)}$ and $f_{\text{sw}, \text{FCML}} = f_{\text{sw}, 2\text{L}}$ in Fig. 9.5. The findings here are substantial. Even if the FCML converter is switched at the same frequency as a 2-level buck converter, the FCML converter can be designed to have slightly better CM EMI through the use of semiconductor devices with smaller die areas. For the comparative case of a buck converter and an FCML converter design with the same switch-node frequency f_{eff} , the FCML converter enables substantial improvements in the fundamental CM EMI component.

Considering these different switching frequency scenarios can practically inform CM filter design. While CM EMI fundamentals at lower frequencies may be smaller, sizing a low-pass

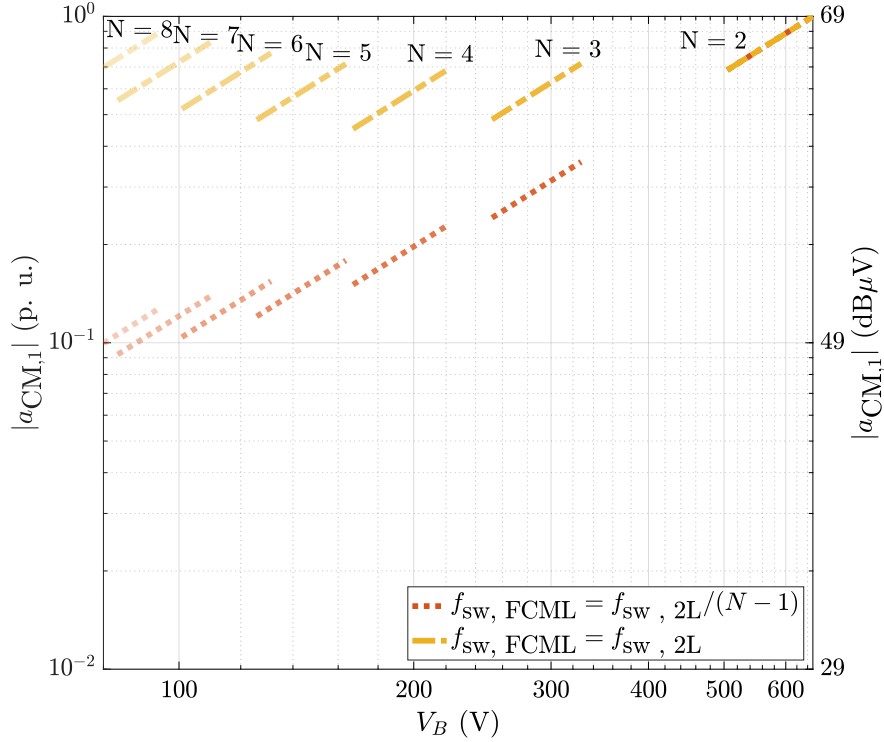


Figure 9.5: Plot of maximum fundamental harmonic magnitude for level counts between $N = 2$ and $N=8$ computed by predicting $C_p \approx \frac{A_{die}(V_B)\epsilon_r\epsilon_0}{d}$. We showcase that for both 1) $f_{sw, FCML} = \frac{f_{sw, 2L}}{(N-1)}$ and 2) $f_{sw, FCML} = f_{sw, 2L}$, CM EMI reductions are enabled by the multilevel circuit topology.

CM EMI filter for a lower switching frequency may result in a larger common-mode choke. However, many EMI standards (e.g. CISPR 25) do not require attenuation below 150 kHz [10]. Thus, it may be desirable to introduce a fundamental harmonic at < 150 kHz. Another consideration here, is that for the FCML converter, the harmonic at $k = N - 1$ may be even larger than the fundamental. Thus, the switching frequency should be chosen strategically.

The Effective Switching Frequency Harmonic

When considering higher-order harmonics, in Fig. 9.6, we showcase the **maximum** harmonic at $k = N - 1$ for $f_{sw, FCML} = f_{sw, 2L}$, $f_{sw, FCML} = f_{sw, 2L}/(N - 1)$, and $f_{sw, FCML} = f_{sw, NL} = f_{sw, 2L}/(N - 1)^2$ using the expression in (9.10). We find that this harmonic magnitude is reduced in the cases where the switching frequency of the multilevel converter is reduced by a factor of either $(N - 1)$ or $(N - 1)^2$. In the case where the FCML converter is switched at $f_{sw, FCML} = f_{sw, 2L}$, we observe that the higher-order harmonic ($k = N - 1$) is similar in size to the 2-level case. Since an EMI filter is conventionally a low-pass filter, the magnitudes in Fig. 9.6 when $f_{sw, FCML} = f_{sw, 2L}$ are not a source of concern, as we know from Fig. 9.5

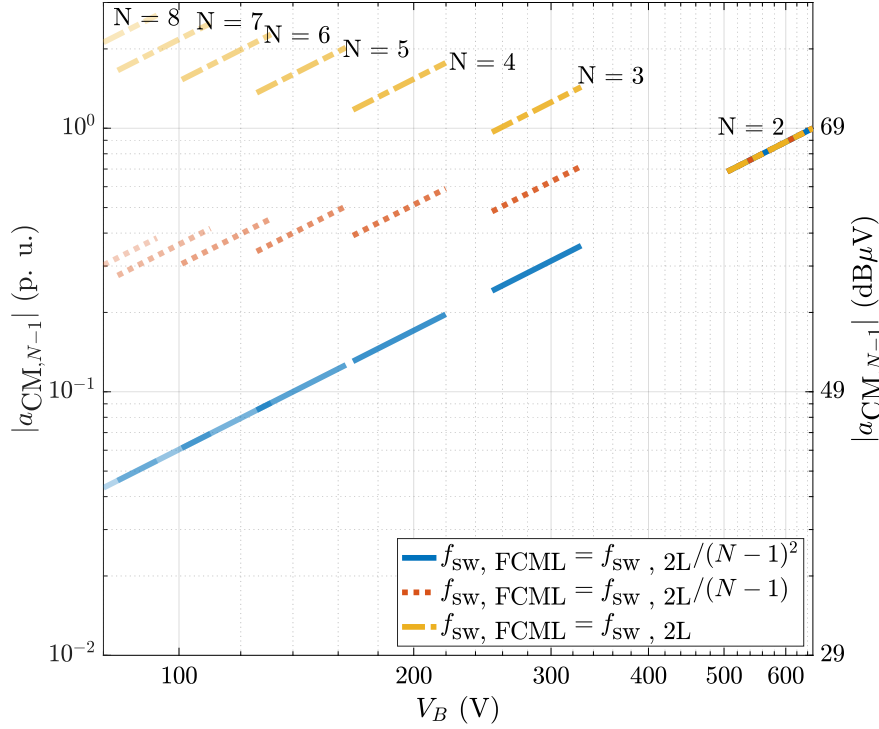


Figure 9.6: Plot of the maximum $k = N - 1$ harmonic magnitude for level counts between $N = 2$ and $N=8$ computed by predicting $C_p \approx \frac{A_{die}(V_B)\epsilon_r\epsilon_0}{d}$.

that the fundamental magnitude ($k = 1$) has been reduced in the multilevel case. If the fundamental harmonic when $f_{sw, FCML} = f_{sw, 2L}$ is within the range of frequencies regulated by an EMI standard, the higher order harmonic $k = N - 1$ should be well captured by the filter design.

Summary of Die Area Informed CM EMI Scaling

Thus far, we have established that the use of switches with smaller die areas in multilevel configurations enables a reduction in CM EMI. This analysis has been agnostic to power rating and converter efficiency, which amplifies the impact of its findings. From this analysis, we know that:

- The fundamental harmonic magnitude $k = 1$ is reduced in multilevel configurations even as level counts are increased and as we consider different FCML converter switching frequency scenarios.
- The effective frequency harmonic magnitude $k = N - 1$ is also reduced in multilevel configurations. This provides useful insight into the choice of switching frequency when considering frequency cutoffs imposed by different EMI standards.

- The FCML converter offers substantially reduced CM EMI characteristics compared to conventional 2-level solutions through die area scaling alone.

In the next subsection, we consider a more holistic view of the FCML converter, where loss and power rating is factored into our CM EMI discussions.

Loss-Sensitive Analysis

The comparison between level counts can be further strengthened by considering the influence of power rating on our device-level and multilevel converter investigation. This analysis considers the scaling of specific on-resistance and charge-equivalent output capacitances for different devices. From these, an optimally calculated die area for both 2-level and multilevel solutions is derived. We apply this procedure in our analysis to inform the optimal balance between CM EMI and efficiency performance. An excellent loss/efficiency analysis for FCML converters was done in [14], including detailed device scaling trends. Over the last six years, many new GaN devices have appeared on the market, which are included in the analysis here. The two main sources of semiconductor device losses are conduction losses, P_{cond} , and hard switching losses, P_{coss} . Conduction losses resulting from the parasitic on-resistance of a device are generally given by

$$P_{\text{cond}} = i_{\text{rms}}^2 R_{\text{ds,on}}. \quad (9.19)$$

We developed the ability to estimate and compute $R_{\text{ds,on}}$ in (9.12). A key takeaway is that in the design of multilevel converters, it is more desirable to use low-voltage devices to minimize total on-resistance.

The other major source of device loss is hard switching loss, which is nominally described by

$$P_{\text{coss}} = C_{\text{oss,Q}} v_{\text{ds}}^2 f_{\text{sw}}, \quad (9.20)$$

where $C_{\text{oss,Q}}$ is the charge-equivalent output capacitance.

In this work we fit a curve to the collected set of data to better describe the area-specific capacitance $C'_{\text{oss,Q}}$ as

$$C'_{\text{oss,Q}}(V_B) \approx k_C V_B^{\alpha_C}. \quad (9.21)$$

Table 9.4: Extracted coefficients for the power-law fits of the form $C'_{\text{oss,Q}}(V_B) \approx k_C V_B^{\alpha_C}$.

Fit	k_C	α_C	R^2
$C'_{\text{oss,Q}}(V_B)$	$4.71 \cdot 10^4$	-1.3	0.936

This capacitance scaling is atypical in deriving voltage-dependent scaling laws in semiconductors. Commercial GaN-on-Si are lateral devices, and inherently 2D. Unlike 1D devices, this makes it challenging to derive a physical relationship between blocking voltage and C_{oss} [14, 140]. A full physical derivation is beyond the scope of this work; we use the empirical

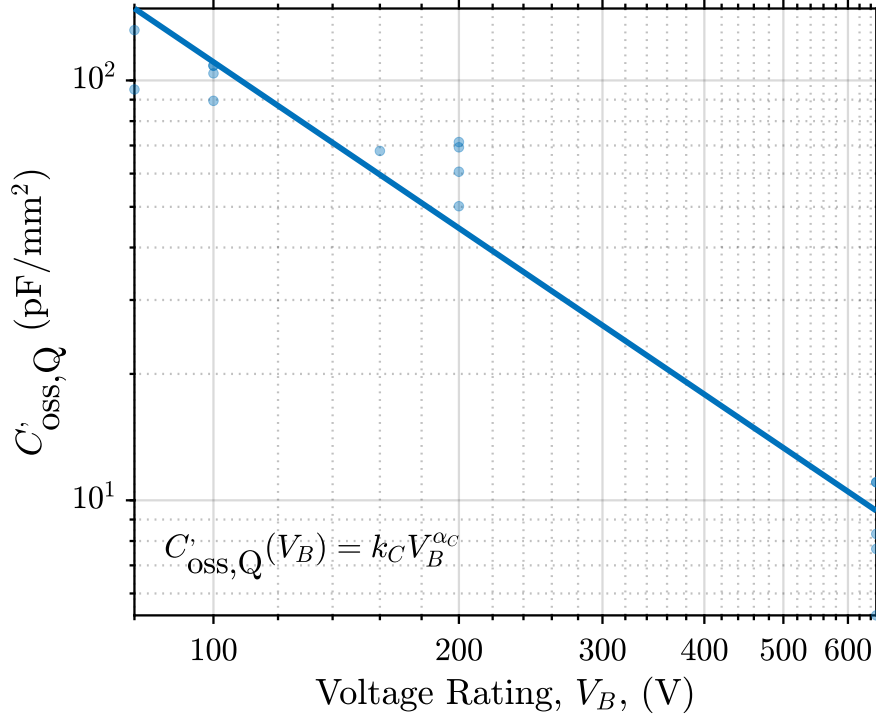


Figure 9.7: Plot of GaN specific output capacitance as well as fitted curve $C'_{oss,Q} \approx k_C V_B^{\alpha_C}$.

fit as a practical tool for comparing devices across voltage ratings. The data points and the empirical fit describing $C'_{oss,Q}$ from (9.21) are shown in Fig. 9.7. Here, $\alpha_C = -1.3$ for this collected set of data, when considering the full voltage range. The empirical fit in Fig. 9.7 indicates a strong relationship with blocking voltage, which is confirmed by $R^2 = 0.936$.

Excluding overlap losses, the major semiconductor device losses for a 2-level solution are given as the sum of P_{cond} and P_{coss} by

$$P_{semi,2L} = i_{rms}^2 \frac{R'_{ds,on}(V_B)}{A_{die}} + C'_{oss,Q}(V_B) \cdot V_{in}^2 f_{sw,2L} A_{die}. \quad (9.22)$$

Recall that both $C'_{oss,Q}(V_B)$ and $R'_{ds,on}(V_B)$ are functions of the rated switch blocking voltage. The multilevel losses for a general N-level case are similarly represented by

$$\begin{aligned} P_{semi,NL} = & (N-1) i_{rms}^2 \frac{R'_{ds,on}(V_B)}{A_{die}} \\ & + (N-1) C'_{oss,Q}(V_B) \cdot \left(\frac{V_{in}}{N-1}\right)^2 f_{sw,NL} A_{die}. \end{aligned} \quad (9.23)$$

In [14], the optimal total die area is computed under the loss minimization assumption that

$\frac{dP_{\text{semi}}}{dA_{\text{die}}} = 0$, which leads to the computed optimal 2-level total die area

$$A_{\text{die, opt, tot., 2L}} = 2 \frac{i_{\text{rms}}}{V_{\text{in}}} \sqrt{\frac{R'_{\text{ds,on}}(V_B)}{C'_{\text{oss,Q}}(V_B) f_{\text{sw, 2L}}}} \quad (9.24)$$

and

$$A_{\text{die, opt., tot., NL}} = 2(N-1)^2 \frac{i_{\text{rms}}}{V_{\text{in}}} \cdot \sqrt{\frac{R'_{\text{ds,on}}(V_B)}{C'_{\text{oss,Q}}(V_B) f_{\text{sw,NL}}}} \quad (9.25)$$

for the multilevel converter case.

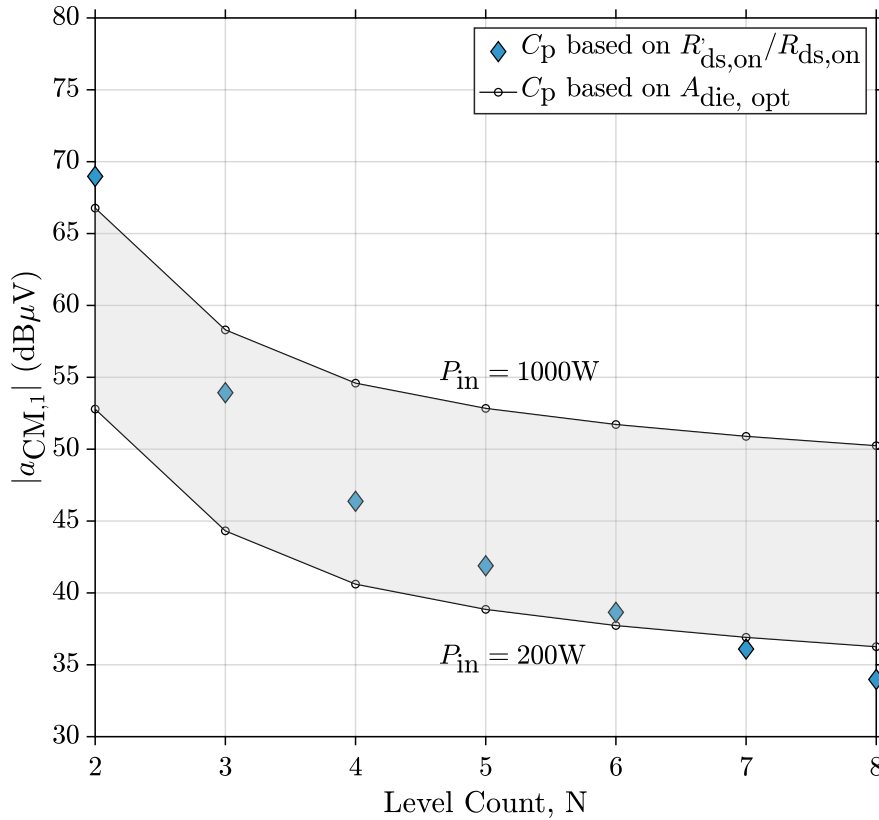


Figure 9.8: Plot of $|a_{\text{CM},1}|$ computed for a 400 V converter where we predict $C_p(A_{\text{die}})$ using the expression in (9.13), and also the cases where we substitute (9.25) into (9.17) for a 200 W and a 1000 W converter. We see that the fundamental magnitudes based on the optimal die area case increase as power rating is increased.

From (9.25), which describes the total optimal die area for a multilevel converter at a given power rating, we can compute a singular switch die area as

$$A_{\text{die, opt.}} = \frac{A_{\text{die, opt., tot., NL}}}{2(N-1)}. \quad (9.26)$$

Using (9.26), we can compute now $C_p(A_{\text{die}})$ and evaluate (9.9).

In Fig. 9.8, we first consider the fundamental magnitudes $|a_{\text{CM}, 1}|$ computed for the case where we predict $C_p(A_{\text{die}})$ using the expression for die area in (9.13) for a 400 V converter switched at $f_{\text{sw, NL}}$. In this case, only conduction losses are accounted for, as we are using $R'_{\text{ds, on}}$ to predict die area. In the second case, we predict the magnitudes $|a_{\text{CM}, 1}|$ for the case where the computed optimal die area (9.25) is substituted into (9.17) for 400 V converters rated for 200 W and 1000 W. Each switch is overrated by $\beta = 1.63$. The parameters used in these calculations are summarized in Table 9.5. Considering the optimal die area allows us to account for the impact of power rating on expected die area. In Fig. 9.8, we observe that as we increase power rating, the total harmonic magnitudes for the FCML converter cases increase in magnitude, as semiconductor devices with larger die areas are needed to conduct more current, as given by (9.25). This subsequently results in larger parasitic capacitances for CM EMI generation.

Table 9.5: Key Parameters for CM Magnitude Prediction Considering Losses

Parameter	Description
V_{in}	400 V
N	$N \in [2, 8]$
$f_{\text{sw, NL}}$	$f_{\text{sw, NL}} = f_{\text{sw, 2L}}/(N-1)^2$
P_{in}	200 W and 1000 W
β	1.63
C_p	Predicted as a function of 1) $R'_{\text{ds, on}}$ when $R_{\text{ds, on, 2L}} = 50 \text{ m}\Omega$ and 2) $A_{\text{die, opt.}}$

9.3 Considering Discrete Hardware Designs

The previous analysis assumed the commercial availability of switches at any desired blocking voltage. The analysis moves beyond that assumption to consider three additional practical constraints of FCML converter design.

1. **Discrete Semiconductor Device Ability:** The availability of discrete semiconductor devices limits the possible design combinations for FCML converters at different

level counts. For example, a 3-level FCML converter for an input voltage of 400 V must have switches rated to block > 200 V. There are presently very few GaN devices rated for < 650 V and > 200 V. Practically, this GaN-based 3-level FCML converter would be realized using 650 V GaN devices.

2. **Package Cooling Footprint and Die Area Differ Widely:** We have previously identified that the parasitic capacitance C_p is a function of die area. For bare-die devices, such as the GaN FETs produced by EPC, this assumption holds true. However, the 650 V GaN devices are available in a range of packaging, often featuring plastic bodies with metal connections to the source/drain for cooling purposes. In these cases, the die area is smaller than the conductive thermal plate and, subsequently, smaller than the “cooling area.” For example, some lateral GaN devices are available in a the Transistor Outline Leded Top-side (TOLT) package [141–143]. These packages have enhanced thermal dissipation through a tab on the top side of the package [144]. Figure 9.9 shows a very simplified diagram of a TOLT-packaged device showing the electrical connection of the die to the cooling plate on top. This plate determines the area of the parasitic capacitance to the chassis in a system with a heat sink.

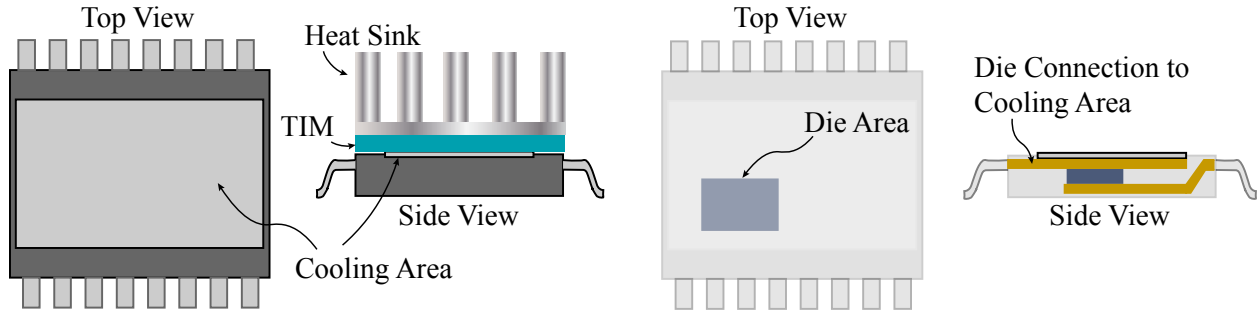


Figure 9.9: Simplified figure of a FET in a Transistor Outline Leded Top-side (TOLT) package with a heat sink placed on top of the cooling area. A transparent view of the FET on the right shows the die, and how it is electrically bonded to the cooling area.

In generating discrete hardware designs, we can highlight this increased area, and the resulting increase in parasitic capacitance. For each design, C_p is defined as

$$C_p \approx \frac{\epsilon_r \epsilon_0 A_{\text{cooling}}}{d}. \quad (9.27)$$

Because the die area is typically not readily available from datasheet parameters, but the cooling area is, we survey some additional 650 V GaN devices to inform possible designs. For these devices, only the dimensions of the cooling tab on top-cooled devices are considered.

3. **Overlap Losses Impact System Efficiency:** In [14], the only considered sources of semiconductor losses are P_{cond} and P_{coss} . High-performance FCML converter works

may additionally consider the role of overlap losses in designing for a specific power converter efficiency condition. The framework presented in [145] includes these overlap losses P_{ovl} to optimize an FCML inverter from a discrete set of generated designs and the resulting Pareto front. We posit that while overlap losses contribute to converter efficiency and should be considered in design optimizations, they do *not* directly correlate to CM EMI performance predictions in the low-frequency spectrum of interest, as the pulse widths of the common-mode current that correspond to both t_r and t_f are a minimal percent of the total switching period for these GaN-based designs.

Overlap losses may be estimated by

$$P_{\text{overlap}} \approx v_{\text{ds}} i_{\text{ds}} \frac{t_{\text{on}} + t_{\text{off}}}{2} f_{\text{sw}}. \quad (9.28)$$

Using the collected data parameters in Table 9.1, we can now consider the inclusion of these losses in the generation of discretized FCML converter designs. While the actual magnitudes of t_f and t_r minimally impact the fundamental harmonic magnitude, they may strongly influence total converter efficiency. We showed in Section 8.3 that we have the capacity to predict these rise/fall times with reasonable accuracy using datasheet parameters. Using the same loss calculations in [145, 146], which achieved strong accuracy when validated in GaN-based FCML hardware prototypes, we connect this analysis to bodies of work considering semiconductor overlap losses.

To make comparisons between FCML converters, we generate a set of designs capable of realizing a 400 V input at a 50% duty cycle and an output power of 1 kW. Total semiconductor losses are computed as

$$P_{\text{sw}} = P_{\text{coss}} + P_{\text{overlap}} + P_{\text{cond}}. \quad (9.29)$$

To compare designs, the semiconductors are given a total loss budget of 20 W that would correspond to an efficiency of $\eta_{\text{semi}} = 98\%$, assuming that the rest of the converter is lossless. To account for overlap losses, we fix one of the gate resistors to constrain the problem sufficiently. Here, $R_{\text{g, off}} = 4 \Omega$. To enable the generation of a 3-level FCML converter using the available GaN devices, switches are overrated by 125–325 % of $V_{\text{in}}/(N-1)$. Because rise and fall times are computed to calculate the overlap losses, we evaluate the full expression in (8.5). The parameters used in these calculations are summarized in Table 9.6.

The averaged fundamental magnitudes $\langle |a_{\text{CM}, 1}| \rangle$ for discrete FCML converter realizations, as well as error bars extending to the minimum and maximum computed fundamental magnitudes, are shown in Fig. 9.10. Notably, we see that the jump in CM EMI performance between a 3-level and a 4-level converter is large, as the 3-level must use 650 V GaN. The higher level count converters have a much lower harmonic profile, as there are many low-voltage GaN devices available. These low voltage devices are the bare-die EPC GaN switches, and have small cooling areas and switch very efficiently, making an efficiency of 98% easy to achieve.

A key finding in this work that impacts the results shown in Fig. 9.10 is that the computed rise/fall times have little to no impact on $|a_{\text{CM}, 1}|$. The switching period is a much stronger

Table 9.6: Constraints for CM EMI comparison calculations.

Parameter	Description
V_{in}	400 V
P_{in}	1000 W
$f_{sw, NL}$	$f_{sw, NL} = f_{sw, 2L}/(N - 1)^2$
η_{semi}	98 %
Min. V_{ds}	125 – 325 % of $V_{in}/(N - 1)$

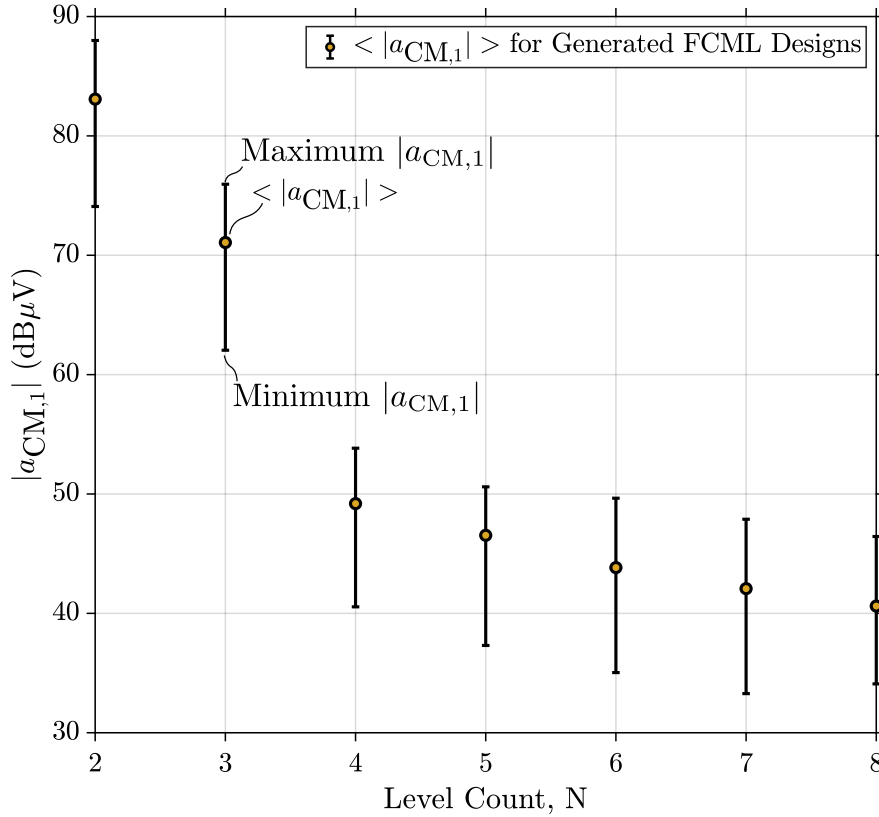


Figure 9.10: Plot of $|a_{CM,1}|$ computed for different discrete hardware prototypes for the FCML converter at 400 V converter rated for 1 kW. Here, we hold efficiency fixed and incorporate overlap losses. The average fundamental magnitude $\langle |a_{CM,1}| \rangle$ is shown for each level count, and error bars extend to the maximum and minimum computed harmonic values.

predictor of harmonic magnitude. In Fig. 9.10, the computed fundamental harmonics are in the same magnitude range as earlier estimates that do not account for overlap losses or explicitly computed rise/fall times. This similarity tells us that while overlap losses may impact total converter efficiency, they do not directly correlate to predictions of $|a_{\text{tot},1}|$, while parasitics that scale with die area, such as $R_{\text{ds,on}}$ and $C_{\text{oss,Q}}$ are much better predictors of CM EMI fundamental harmonic magnitudes for the FCML converter.

9.4 Conclusion

This chapter used the model presented in Chapter 8 to analyze CM EMI in the general N-level FCML converter. Rise and fall times are decoupled from this analysis, as we consider the low-frequency spectrum. First, using the area-specific on-resistance, we predict die area and subsequently the parasitic capacitance from source to chassis. From these calculations, we find that **for a fixed equivalent on-state resistance, the FCML converter has better CM EMI than the 2-level converter**. In this initial framework, we also consider the possibility of using different switching frequencies and showcase that $|a_{\text{CM},1}|$ is lower in the FCML converter than in the conventional 2-level solution, even at the same switching frequency. Second, we consider how CM EMI scales as a function of power rating, by considering both semiconductor conduction and hard switching losses. We find that using the computed optimal die area for a given power rating, **CM EMI scales favorably in the FCML converter, even as power is increased**. Lastly, we consider that the semiconductor die area and package area are distinct, particularly in commercially available high-voltage GaN. We generate a set of discrete FCML converter designs for a fixed efficiency, with device overlap losses incorporated. Reintroducing this complexity confirms that the FCML converter **has substantially better CM EMI than the 2-level converter considering device packaging constraints**. By gradually increasing analysis complexity in this chapter, it is shown that multilevel converter architectures offer opportunities for improved CM EMI performance.

Chapter 10

Concluding Remarks

This dissertation has focused on the implementation and benefits of the FCML converter compared to a conventional buck or boost converter. This final chapter focuses on summarizing the findings presented in this dissertation and commenting on future avenues of research.

Hybrid Switched-Capacitor Converters for DC-AC Systems

In Part I of this dissertation, FCML converters are evaluated as a strong choice for dc-ac/ac-dc conversion. Their ability to generate a well-filtered sinusoid at high efficiencies and power densities results in them being competitive choices in this application space. However, there are still ways to augment the performance of the FCML converter in dc-ac/ac-dc application spaces.

Future Work: One practical challenge that was discussed is system start-up for a microinverter. The flying capacitors in both stages of the microinverter in Chapter 2 were successfully ramped up to their nominal dc voltages. As a multi-resonant hybrid switched-capacitor circuit was used to provide a startup routine in lieu of additional circuitry, it would be interesting to evaluate other similar circuit topologies that can provide this capability to a system. Understanding the start-up rate for different topologies would be a useful metric for comparison.

FCML Converters in Isolated Applications

The FCML converter is merged with a dual active bridge converter in Part I of this dissertation to create a competitive high-step-down isolated converter for automotive or data center applications. The transformer in the DAB converter provides necessary galvanic isolation, while the replacement of the high voltage switches on the primary side of the DAB with the low voltage devices enabled by the FCML converter translates to high efficiencies and power densities.

Future Work: In general, assessing the use of different hybrid switched-capacitor derived topologies for isolation is a useful area of investigation, and capacitively isolated hybrid switched-capacitor solutions are also an active area of research [83, 147–150]. Continued investigation into galvanically isolated converters with switched-capacitor stages is worthwhile.

Conducted EMI in the FCML Converter

Differential-Mode EMI

Part II of this dissertation explores conducted EMI in the FCML converter. In this work, DM EMI is characterized for FCML converters with flying capacitor voltage ripple. It is shown that a combination of capacitor voltage imbalance and ripple creates harmonics at frequencies other than the effective switch-node frequency. In dc-ac/ac-dc FCML converters, the grid-side voltage and current will have these intra-harmonics, which was noted in [21, 106]. Characterizing the impact of these harmonics on EMI filter design would be an interesting way to explore the co-optimization of FCML converter and filter design. The existence of these harmonics are nuanced, and filter optimization would be a practically motivating way to explore this further.

Future Work: As flying capacitor voltage imbalance worsens the magnitude of observed intra-harmonics, it is worth investigating the impacts of active balancing or other current programmed modulation techniques that improve capacitor balancing [104, 105, 151] on output-side DM EMI in the FCML converter. While imbalance is only one driver of intra-harmonics, it is a substantial contributor to these magnitudes. Eliminating imbalance should theoretically improve these harmonics, although more analysis is needed to assess the extent to which this is true.

Common-Mode EMI

Common-mode EMI is modeled for the FCML converter in this work. Both the time-domain and frequency-domain measurements verify that the model encompasses the required level of detail to accurately predict CM EMI in the topology. Finally, CM EMI is shown to be better in the FCML converter than in the buck converter.

Future Work: The CM EMI modeling approach could be applied to other hybrid switched-capacitor topologies. For topologies using fewer switching phases than the FCML converter operated under PS-PWM operation, the suggested approach would be fairly straightforward in both the time and frequency domain.

This dissertation demonstrates that the FCML converter is superior to the 2-level buck converter, but how it compares to other converter topologies remains unknown. Comparing CM EMI performance between hybrid switched-capacitor circuit topologies would enable a new exploration of practical trade-offs between circuits in this converter class. For example, a Dickson-based circuit topology was used to achieve automotive EMI pre-compliance in [152], but the specific EMI benefits of the Dickson converter over other hybrid switched-

capacitor topologies remain unknown. Using the framework presented in this thesis would be a starting point to begin making these practical topology comparisons.

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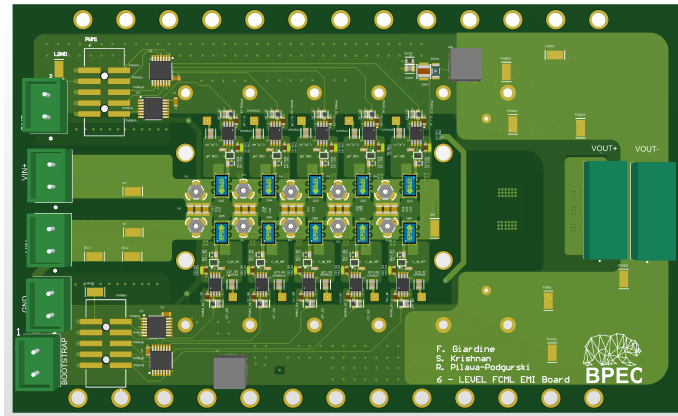
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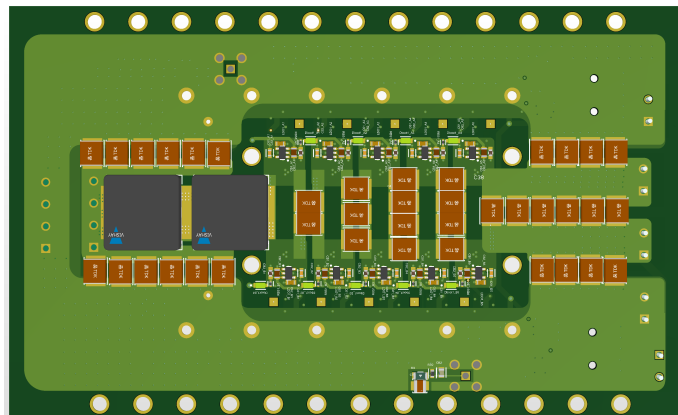
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Appendix A

PCB Design of an FCML Converter



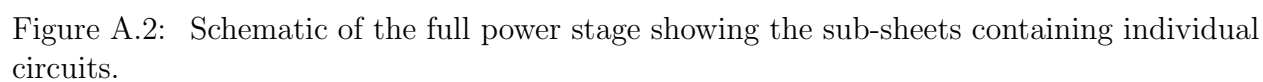
(a) Top of PCB.

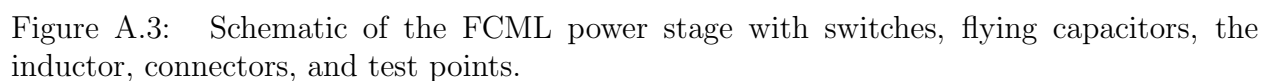


(b) Bottom of PCB.

Figure A.1: The figure shows a 3D rendering generated in Altium PCB Designer of the PCB designed for the 6-level FCML converter in Chapter 8.

Figure A.2: Schematic of the full power stage showing the sub-sheets containing individual circuits.





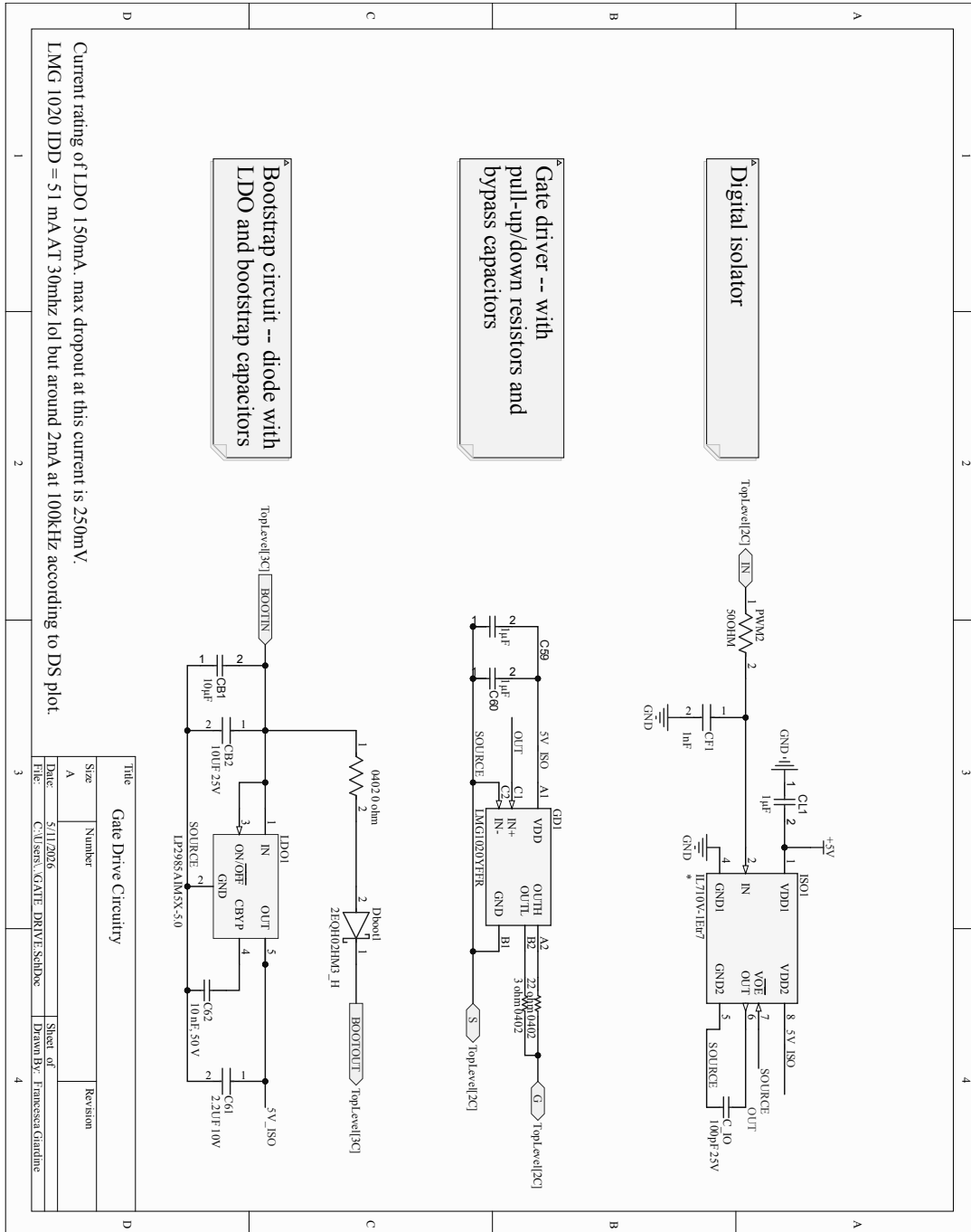


Figure A.4: Schematic of a single gate drive circuit powered with cascaded bootstrap. Each switch has an individual gate drive circuit.

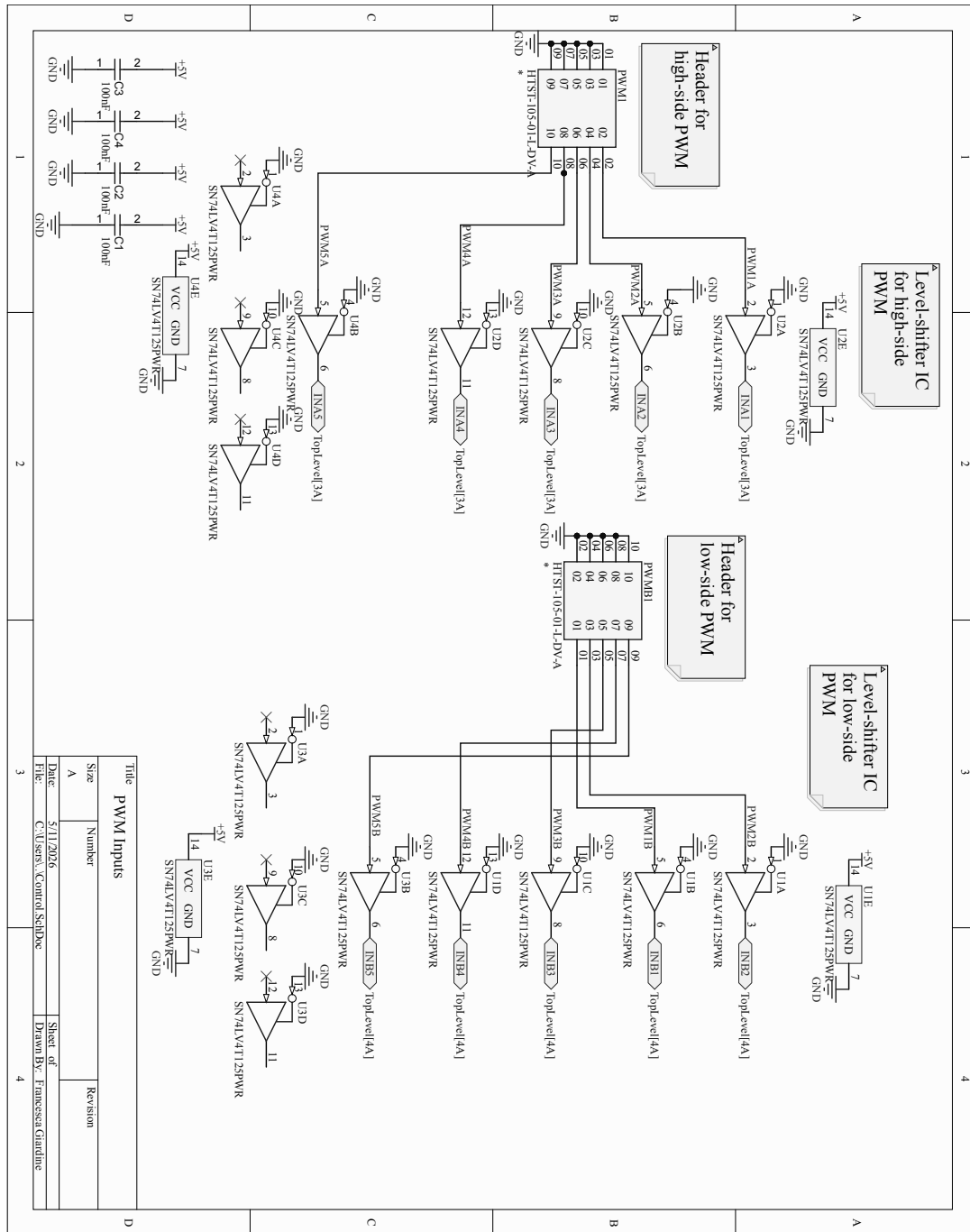


Figure A.5: Schematic with headers used for off-board PWM generation, as well as level shifters to create a 5 V input to the isolators.

A.2 Copper Layers

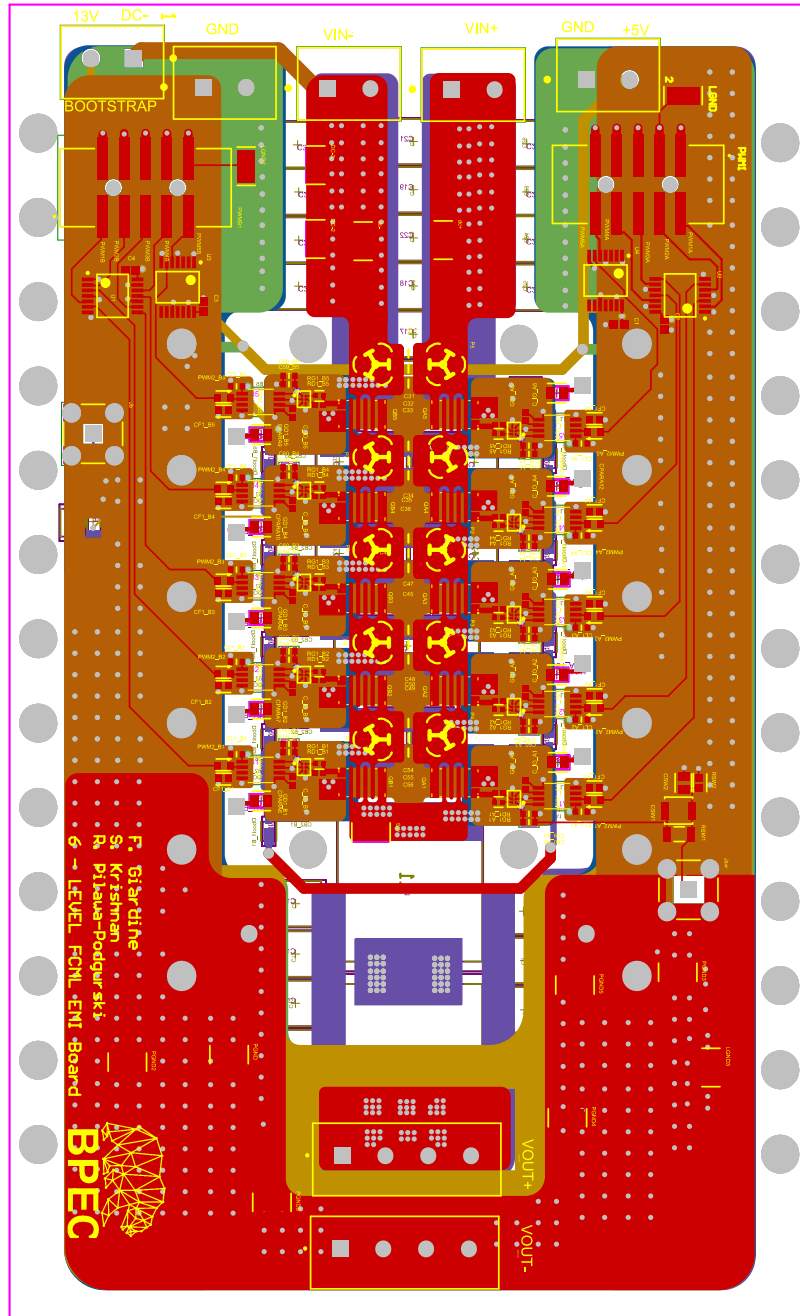


Figure A.6: The full PCB layer copper layer stack as shown from the top layer.

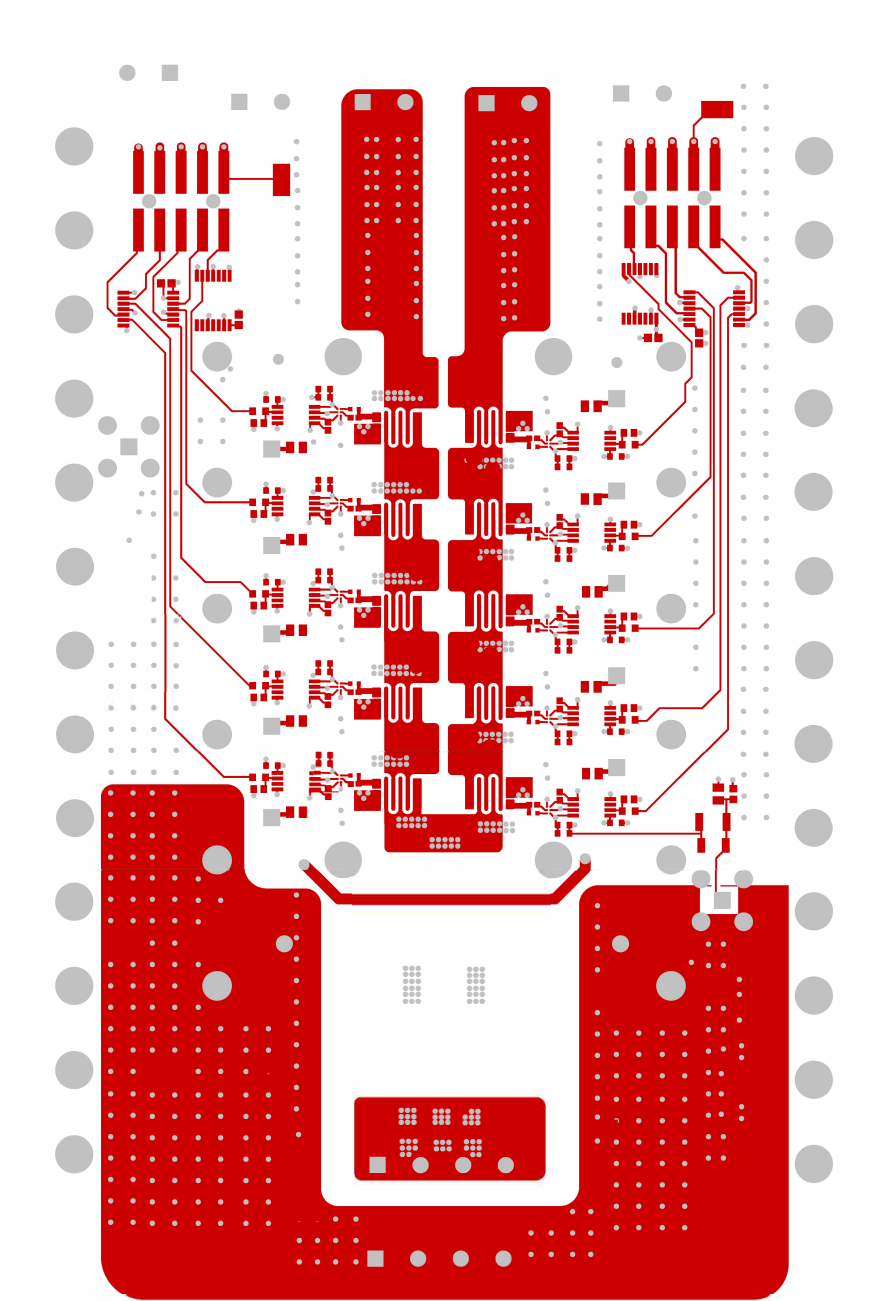


Figure A.7: PCB top layer. Switches, local decoupling capacitors, and gate drivers/isolators are placed on this layer.

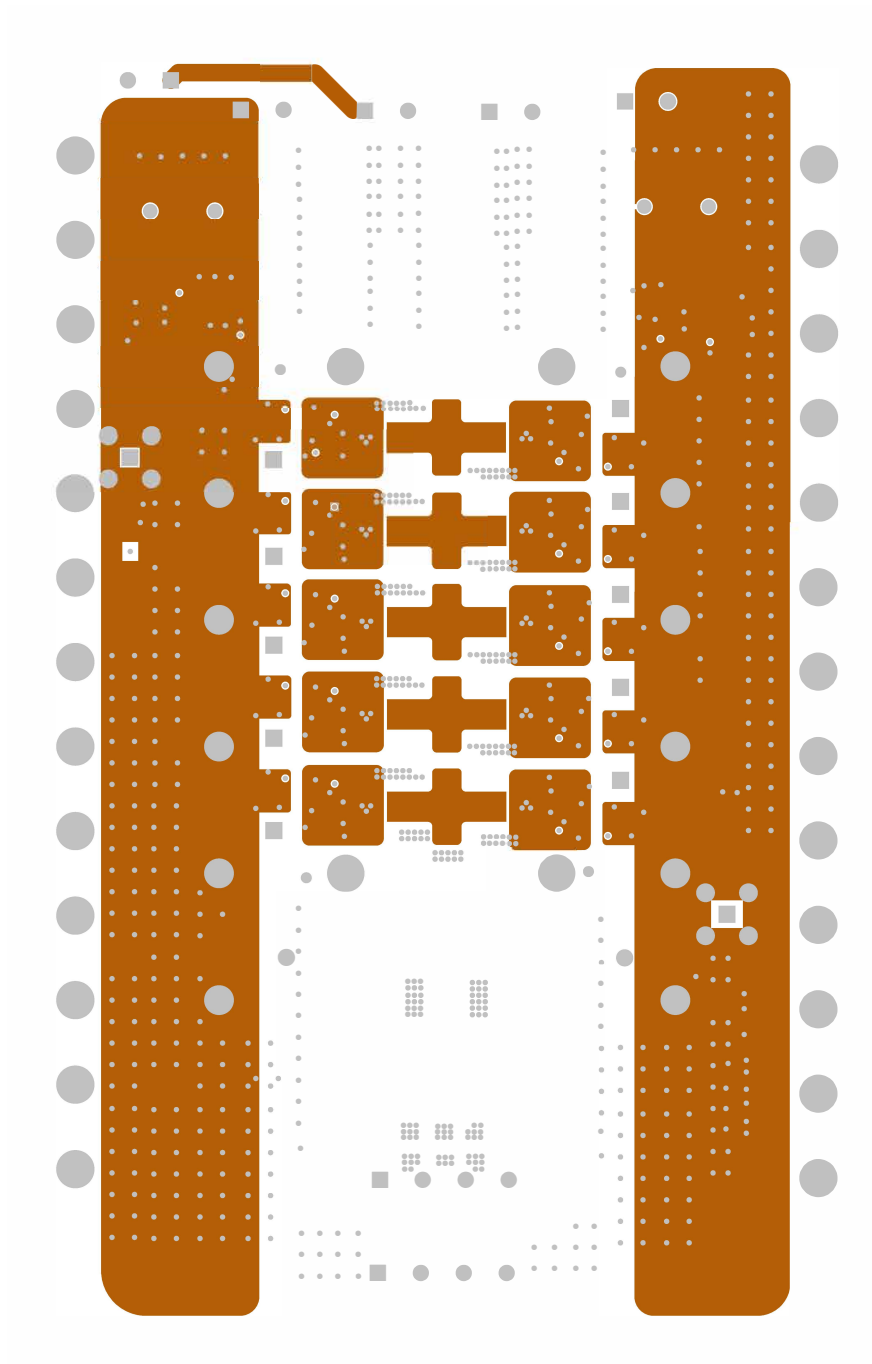


Figure A.8: PCB layer 2. This layer contains copper shielding planes below switches and decoupling capacitors, and shielding below the gate drive circuitry.

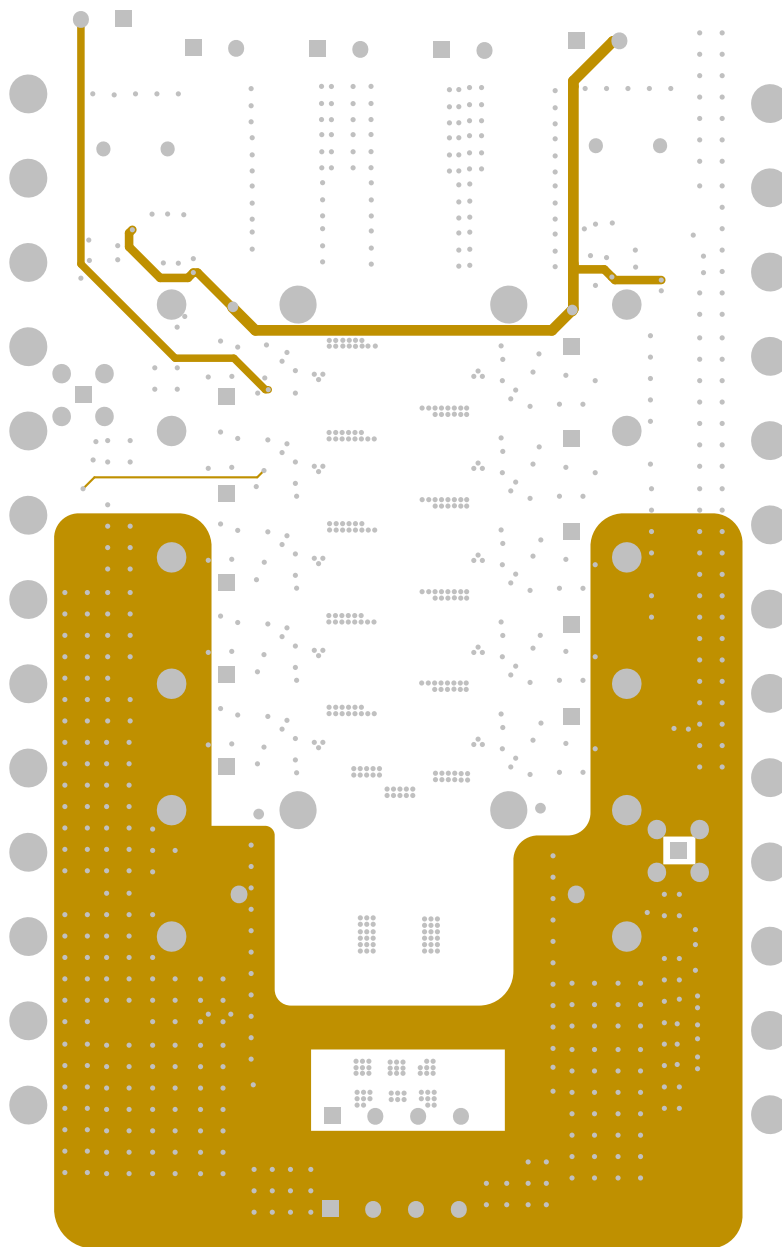


Figure A.9: PCB layer 3. This layer contains some logic voltage power routing and more ground pours.

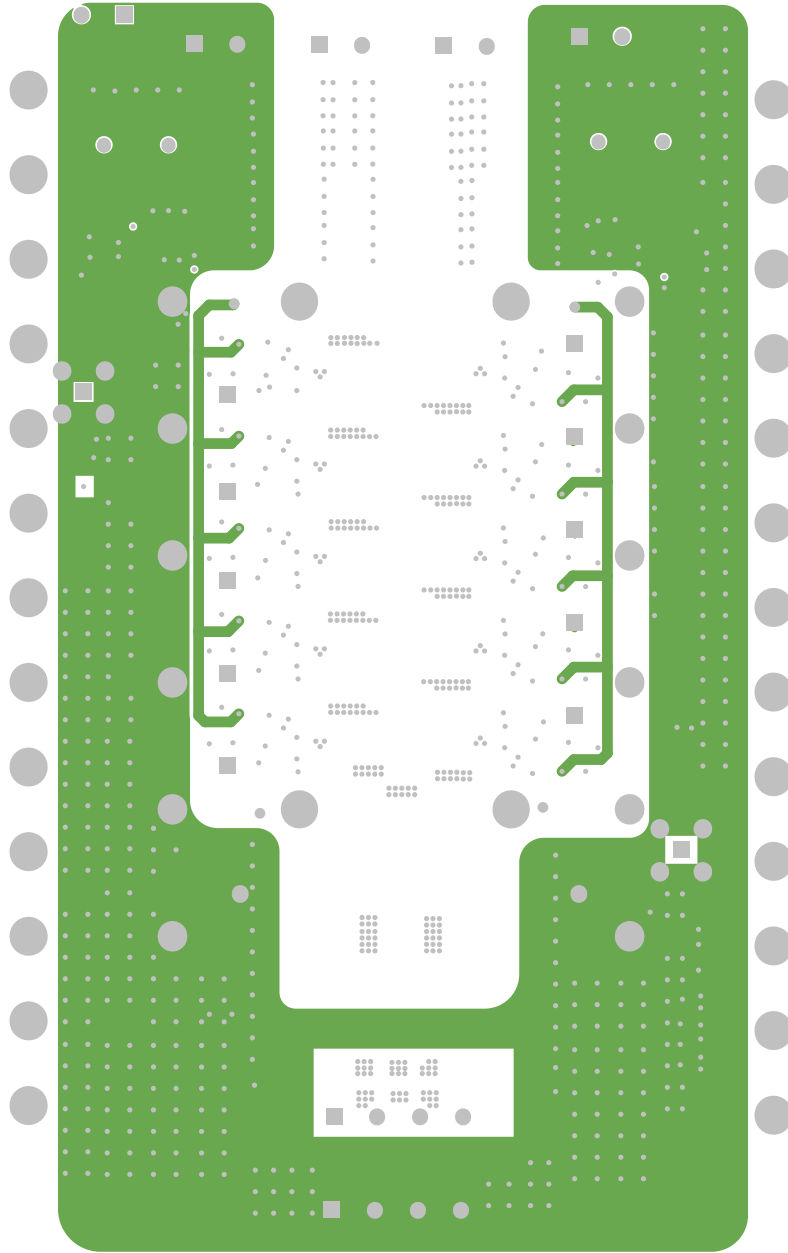


Figure A.10: PCB layer 4. This layer contains some logic voltage power routing and more ground pours.

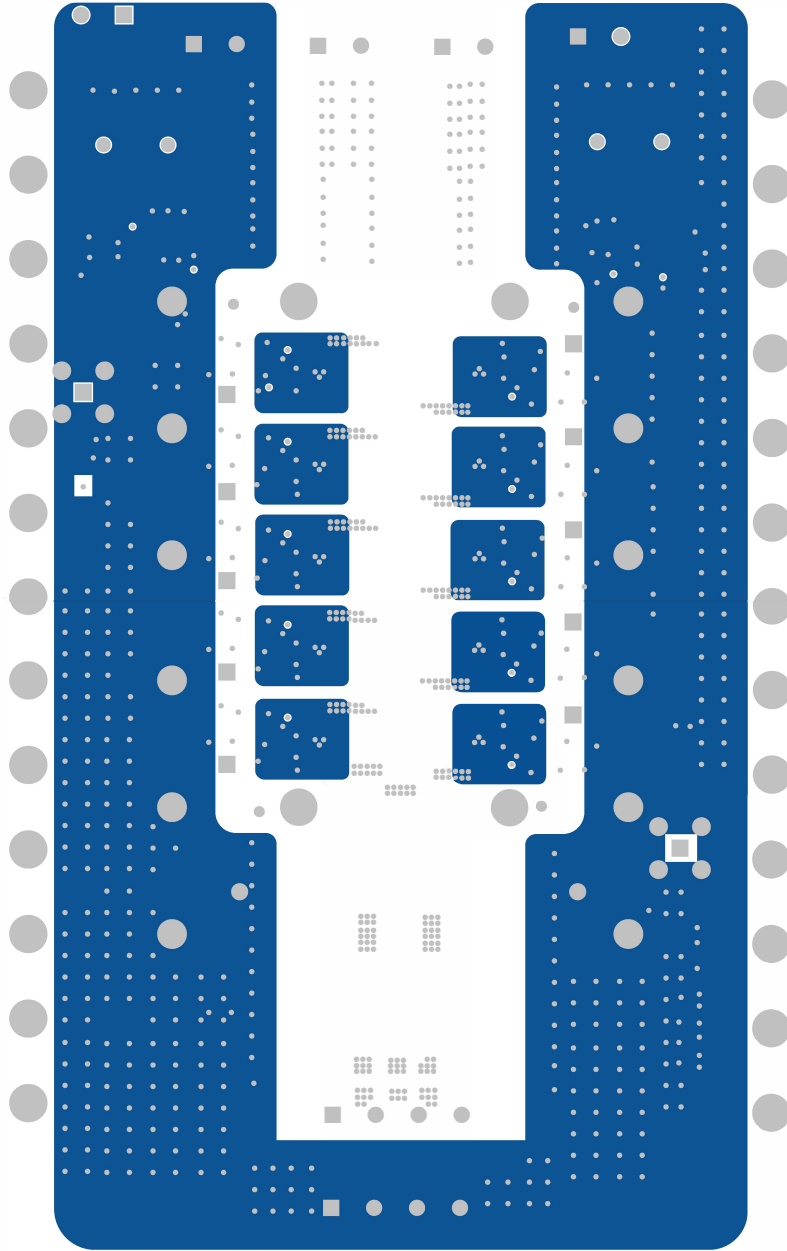


Figure A.11: PCB layer 5. This layer contains copper shielding planes below bootstrap circuitry, and more ground pours.

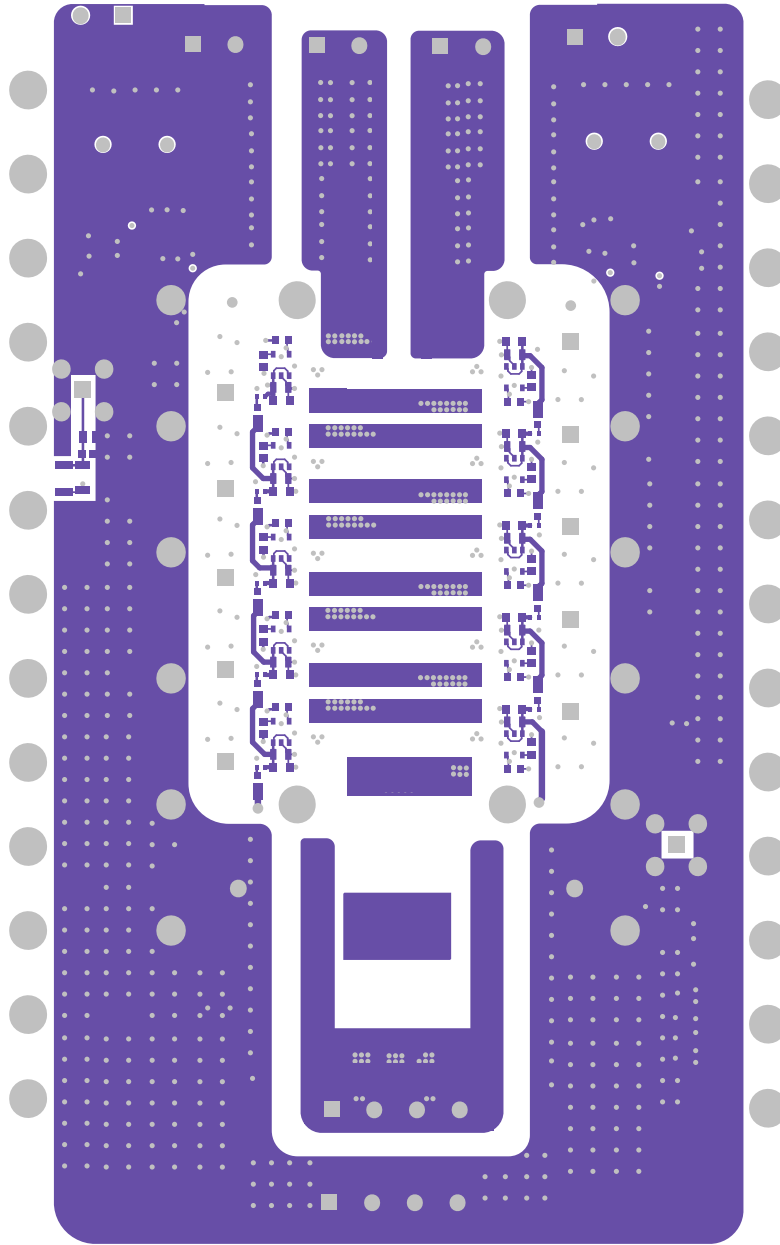


Figure A.12: PCB bottom layer. This layer contains the flying capacitors, and the bootstrap circuitry. Bootstrap power is delivered to the gate drivers through vias.

Appendix B

Variable Frequency C2000 Code

The C2000 code in this appendix was used in Chapter 3 and adapted for the converter in Chapter 7. The project structure was adopted from a project originally authored by Nathan Brooks, and substantially altered by Yixuan Wu and me to operate with a variable switching frequency.

```

1
2 //#####
3 // $TI Release: F2837xD Support Library v160 $
4 // $Release Date: Mon Jun 15 13:36:23 CDT 2015 $
5 // $Copyright: Copyright (C) 2013-2015 Texas Instruments Incorporated -
6 //           http://www.ti.com/ ALL RIGHTS RESERVED $
7 //#####
8
9 // Device Headerfile and Examples Include File
10 #include "F28x_Project.h"
11 #include "globalvariables.h"
12 #include "globaldefine.h"
13 #include "initialize.h"
14 #include "math.h"
15
16
17 void main(void)
18 {
19     // Step 1. Initialize System Control:
20     // PLL, WatchDog, enable Peripheral Clocks
21     // This example function is found in the F2837xD_SysCtrl.c file.
22     InitSysCtrl();
23
24     // Step 2. Initialize GPIO:
25     InitGpio(); // set the GPIO to it's default state (i.e., high
impedance input)
26     CpuSysRegs.PCLKCR2.bit.EPWM1=1;
27
28     // Step 3. Clear all interrupts and initialize PIE vector table:
29     Init_interrupts();

```

```

30
31 // Step 4. Initialize the Device Peripherals:
32 EALLOW;
33 // make PWM clock the same as SYSCLK
34 ClkCfgRegs.PERCLKDIVSEL.bit.EPWMCLKDIV = 0x0;
35 //disable synchronization of all ePWMs to the TBCLK
36 CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 0;
37 EDIS;
38
39 Init_EPwms(); // Initialize ePWMs
40
41 EALLOW;
42 //enable synchronization of all ePWMs to the TBCLK
43 CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;
44 // this will start ADC conversion since ADC are triggered by ePWM1
45 EDIS;
46
47 // Initialize global variables. Includes some ADC conversion
48 // calculations so must be called after ADC_bias().
49 Init_globalvariables();
50 Configure_GPIO();
51
52 EALLOW;
53 GpioCtrlRegs.GPBDIR.bit.GPIO32 = 1;
54 // Configure pins for PWM3 to be regular output pins
55 EDIS;
56 GpioDataRegs.GPASET.bit.GPIO32 = 1;
57
58 // Step 5. User specific code, enable interrupts:
59 // Initialize all interrupts
60 Enable_interrupts();
61
62 // Step 6: Infinite loop, let ISR (interrupt service routines) handle
63 // the rest
64 while(1)
65 {
66 }
67
68 //-----
69 // Yixuan Wu wrote this ISR for variable switching frequency
70 //-----
71
72 interrupt void variable_f_sw_ISR(void)
73 {
74 //Calculate relative angle
75 ac_step = ((float)period_sw / (float) AC_PERIOD);
76 theta = theta + ac_step;
77 if ((theta) >= 1)

```

```

78     {
79         theta = theta - 1;
80     }
81     else if (theta < 0)
82     {
83         theta = theta + 1;
84     }
85
86
87 //Calculate duty cycle as a sine wave of the relative angle
88     ac_dutyopen = m_ref*(__sinpuf32(theta));
89 //Toggle unfold switches at 60Hz, set by GPIO 4, 5
90     if (ac_dutyopen > 0)
91     {
92         GpioDataRegs.GPASET.bit.GPIO4 = 1;
93         GpioDataRegs.GPASET.bit.GPIO5 = 1;
94     }
95     else if (ac_dutyopen < 0)
96     {
97         GpioDataRegs.GPACLEAR.bit.GPIO5 = 1;
98         GpioDataRegs.GPACLEAR.bit.GPIO4 = 1;
99     }
100 //Calculate absolute value of duty cycle ratio - double humps
101     period_sw = Update_period_sw(fabs(ac_dutyopen));
102 //Update period_sw on leader ePWM
103     ePWM[EPwm_CH1]->TBPRD = (uint16_t) (period_sw-1);
104
105 // Update duty cycle
106     cmpa_ctr = (uint16_t)(period_sw*fabs(ac_dutyopen));
107     ePWM[EPwm_CH1]->CMPA.bit.CMPA = cmpa_ctr;
108 // might be needed with the linking
109
110 //Update phase shift of follower ePWMs
111     ph_1_ctr = (uint16_t)(period_sw*ph_1);
112     ph_2_ctr = (uint16_t)(period_sw*ph_2);
113     ph_3_ctr = (uint16_t)(period_sw*ph_3);
114     ph_4_ctr = (uint16_t)(period_sw*ph_4);
115     ph_5_ctr = (uint16_t)(period_sw*ph_5);
116
117     ePWM[EPwm_CH4]->TBPHS.bit.TBPHS = ph_1_ctr;           // Phase
118     ePWM[EPwm_CH5]->TBPHS.bit.TBPHS = ph_2_ctr;           // Phase
119     ePWM[EPwm_CH6]->TBPHS.bit.TBPHS = ph_3_ctr;           // Phase
120     ePWM[EPwm_CH7]->TBPHS.bit.TBPHS = ph_4_ctr;           // Phase
121     ePWM[EPwm_CH8]->TBPHS.bit.TBPHS = ph_5_ctr;           // Phase
122
123 // Phase shift direction for circularly shifted PS-PWM
124     ePWM[EPwm_CH4]->TBCTL.bit.PHSDIR = dir_1;
125     ePWM[EPwm_CH5]->TBCTL.bit.PHSDIR = dir_2;
126     ePWM[EPwm_CH6]->TBCTL.bit.PHSDIR = dir_3;
127     ePWM[EPwm_CH7]->TBCTL.bit.PHSDIR = dir_4;

```



```

128     ePWM[EPwm_CH8]->TBCTL.bit.PHSDIR = dir_5;
129
130 // Set action at EPWMxSYNCIN
131 //set PWM output to high or low as a manual comparison
132 // This helps against the glitch that happens when the phase offset is
    equal (or around equal) to the CMPA value
133     set_sync_aqa(EPwm_CH4, ph_1_ctr, cmpa_ctr);
134     set_sync_aqa(EPwm_CH5, ph_2_ctr, cmpa_ctr);
135     set_sync_aqa(EPwm_CH6, ph_3_ctr, cmpa_ctr);
136     set_sync_aqa(EPwm_CH7, ph_4_ctr, cmpa_ctr);
137     set_sync_aqa(EPwm_CH8, ph_5_ctr, cmpa_ctr);
138
139 // Clear and acknowledge interrupt
140 // Clear INT flag for this timer
141     EPwm1Regs.ETCLR.bit.INT = 1;
142
143 //Acknowledge this interrupt to receive more interrupts from group 3
144     PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
145 }
146
147 uint16_t Update_period_sw(float duty)
148 {
149 //Calculate effective duty ratio
150     float duty_eff = (N-1)*duty - floorf((N-1)*duty); // effective duty
    cycle
151
152 //calculate the switching frequency for a certain current ripple
153     float f_sw_ipp = V_IN * (duty_eff * (1-duty_eff)) * INV_1_L *
    INV_1_N_1 * INV_1_N_1 * INV_1_DELTA_I_PP;
154
155 // Calculate the minimum switching frequency for a certain voltage ripple
156     if (duty < 0.8)
157     {
158         f_sw_min = V_IN * duty * INV_R_LOAD * INV_1_C * INV_1_N_1 *
    INV_1_DELTA_V_PP;
159     }
160     else if (duty >= 0.8)
161     {
162         f_sw_min = V_IN * duty * INV_R_LOAD * (1 - duty_eff) * INV_1_C *
    INV_1_N_1 * INV_1_DELTA_V_PP;
163     }
164 // saturate the switching frequency
165 // too low - capacitor voltages diverging too much from ideal value
166 // too high - physically not possible
167     f_sw_ipp = f_sw_ipp < f_sw_min ? f_sw_min : f_sw_ipp;
168     f_sw_ipp = f_sw_ipp < F_SW_MIN ? F_SW_MIN : f_sw_ipp;
169     f_sw_ipp = f_sw_ipp > F_SW_MAX ? F_SW_MAX : f_sw_ipp;
170
171 //inversion for period instead of frequency
172     uint16_t period = (uint16_t) floorf(TBCLK/f_sw_ipp*500);

```

```

173     return period;
174 }
175
176 void set_sync_aqa(EPwm_Channel pwm_chan, uint16_t ph_x_ctr, uint16_t
    cmpa_ctr)
177 {
178     if (cmpa_ctr >= ph_x_ctr)
179     {
180         ePWM[pwm_chan]->AQCTLA2.bit.T1U = AQ_SET;
181     }else{
182         ePWM[pwm_chan]->AQCTLA2.bit.T1U = AQ_CLEAR;
183     }
184
185     if (cmpa_ctr >= ph_x_ctr)
186     {
187         ePWM[pwm_chan]->AQCTLA2.bit.T1D = AQ_SET;
188     }else{
189         ePWM[pwm_chan]->AQCTLA2.bit.T1D = AQ_CLEAR;
190     }
191 }

```

Listing B.1: Main C2000 file (**main.c**) with the variable frequency operation interrupts defined

```

1 #ifndef INITIALIZE_H_
2 #define INITIALIZE_H_
3 #include "F28x_Project.h"
4 #include "globaldefine.h"
5 #include "globalvariables.h"
6
7 extern struct EPWM_REGS *ePWM[];
8
9 void Init_globalvariables(void);
10
11 // Disable unused clocks to save power
12 void Disable_unused_clk(void);
13
14 // initialize ADCS
15 void Init_ADCs(void);
16 void InitADCa(void);
17 void InitADCb(void);
18 void InitADCc(void);
19 //void InitADCd(void);
20
21 // Clear interrupt flag for ISR "interrupt1"
22 void ADC_clear_interrupt1_flag(void);
23
24 void Init_DACs(void);
25
26 void Init_EPwms(void);

```

```

27 void InitEPwm_Leader(EPwm_Channel, int, float, float, int,
    EPwm_ModulationType, EPwm_ComplimentaryMode);
28 void InitEPwmA_X(EPwm_Channel, int, float, float, int, EPwm_ModulationType
    , EPwm_ComplimentaryMode, int);
29 void InitEPwmB_X(EPwm_Channel, int, float, float, int, EPwm_ModulationType
    , EPwm_ComplimentaryMode);
30
31 void InitEPwmADC(EPwm_Channel);
32
33 // Initialize the necessary interrupts (without enabling)
34 void Init_interrupts(void);
35
36 // Enable interrupts
37 void Enable_interrupts(void);
38
39 // interrupt functions
40 interrupt void ADC_interrupt1(void);
41 void Update_duty(float duty);
42 void Configure_GPIO(void);
43
44
45 //Variable switching frequency functions
46 interrupt void variable_f_sw_ISR(void);
47 uint16_t Update_period_sw(float duty);
48 void set_sync_aqa(EPwm_Channel pwm_chan, uint16_t ph_x_ctr, uint16_t
    cmpa_ctr);
49
50 #endif /* INITIALIZE_H_ */

```

Listing B.2: Initialization header file (**initialize.h**) initializing all functions/interrupts.

```

1 #include "F28x_Project.h"
2 #include "initialize.h"
3 #include "globaldefine.h"
4 #include "globalvariables.h"
5
6 /* Declare internal functions */
7 void ADC_conversion_wait(void);
8 void ADC_clear_all_interrupt_flags(void);
9
10 /* Define external functions */
11 // Initialize all global variables to their nonzero values.
12
13 void Configure_GPIO(void)
14 {
15 //CONFIGURE AS ORDINARY GPIO FOR UNFOLDER
16     GpioDataRegs.GPACLEAR.bit.GPIO4 = 1; //inv_pos_pwm
17     GpioDataRegs.GPACLEAR.bit.GPIO5 = 1; //inv_neg_pwm
18
19     GPIO_SetupPinMux(4, GPIO_MUX_CPU1, 0);
20     GPIO_SetupPinOptions(4, GPIO_OUTPUT, GPIO_PUSHPULL);

```

```

21     GPIO_SetupPinMux(5, GPIO_MUX_CPU1, 0);
22     GPIO_SetupPinOptions(5, GPIO_OUTPUT, GPIO_PUSHPULL);
23 }
24
25 void Disable_unused_clk()
26 {
27     EALLOW;
28     CpuSysRegs.PCLKCR0.bit.CLA1 = 0;
29     CpuSysRegs.PCLKCR0.bit.DMA = 0;
30     CpuSysRegs.PCLKCR0.bit.CPUTIMER0 = 0;
31     CpuSysRegs.PCLKCR0.bit.CPUTIMER1 = 0;
32     CpuSysRegs.PCLKCR0.bit.CPUTIMER2 = 0;
33
34     CpuSysRegs.PCLKCR1.bit.EMIF1 = 0;
35     CpuSysRegs.PCLKCR1.bit.EMIF2 = 0;
36
37     CpuSysRegs.PCLKCR2.bit.EPWM10 = 0;
38     CpuSysRegs.PCLKCR2.bit.EPWM11 = 0;
39     CpuSysRegs.PCLKCR2.bit.EPWM12 = 0;
40
41     CpuSysRegs.PCLKCR3.bit.ECAP1 = 0;
42     CpuSysRegs.PCLKCR3.bit.ECAP2 = 0;
43     CpuSysRegs.PCLKCR3.bit.ECAP3 = 0;
44     CpuSysRegs.PCLKCR3.bit.ECAP4 = 0;
45     CpuSysRegs.PCLKCR3.bit.ECAP5 = 0;
46     CpuSysRegs.PCLKCR3.bit.ECAP6 = 0;
47
48     CpuSysRegs.PCLKCR4.bit.EQEP1 = 0;
49     CpuSysRegs.PCLKCR4.bit.EQEP2 = 0;
50     CpuSysRegs.PCLKCR4.bit.EQEP3 = 0;
51
52     CpuSysRegs.PCLKCR6.bit.SD1 = 0;
53     CpuSysRegs.PCLKCR6.bit.SD2 = 0;
54
55     CpuSysRegs.PCLKCR7.bit.SCI_A = 0;
56     CpuSysRegs.PCLKCR7.bit.SCI_B = 0;
57     CpuSysRegs.PCLKCR7.bit.SCI_C = 0;
58     CpuSysRegs.PCLKCR7.bit.SCI_D = 0;
59
60     CpuSysRegs.PCLKCR8.bit.SPI_A = 0;
61     CpuSysRegs.PCLKCR8.bit.SPI_B = 0;
62     CpuSysRegs.PCLKCR8.bit.SPI_C = 0;
63
64     CpuSysRegs.PCLKCR9.bit.I2C_A = 0;
65     CpuSysRegs.PCLKCR9.bit.I2C_B = 0;
66
67     CpuSysRegs.PCLKCR10.bit.CAN_A = 0;
68     CpuSysRegs.PCLKCR10.bit.CAN_B = 0;
69
70     CpuSysRegs.PCLKCR11.bit.McBSP_A = 0;

```

```

71  CpuSysRegs.PCLKCR11.bit.McBSP_B = 0;
72  CpuSysRegs.PCLKCR11.bit.USB_A = 0;
73
74  CpuSysRegs.PCLKCR12.bit.uPP_A = 0;
75
76  CpuSysRegs.PCLKCR14.bit.CMPSS1 = 0;
77  CpuSysRegs.PCLKCR14.bit.CMPSS2 = 0;
78  CpuSysRegs.PCLKCR14.bit.CMPSS3 = 0;
79  CpuSysRegs.PCLKCR14.bit.CMPSS4 = 0;
80  CpuSysRegs.PCLKCR14.bit.CMPSS5 = 0;
81  CpuSysRegs.PCLKCR14.bit.CMPSS6 = 0;
82  CpuSysRegs.PCLKCR14.bit.CMPSS7 = 0;
83  CpuSysRegs.PCLKCR14.bit.CMPSS8 = 0;
84  EDIS;
85 }
86
87 void Clear_interrupts()
88 {
89 // Initialize the PIE control registers to their default state.
90 // The default state is all PIE interrupts disabled and flags
91 // are cleared.
92     InitPieCtrl();
93
94 // Disable CPU interrupts and clear all CPU interrupt flags:
95     EALLOW;
96     IER = 0x0000;
97     IFR = 0x0000;
98     EDIS;
99
100 // Initialize the PIE vector table with pointers to the shell
Interrupt
101 // Service Routines (ISR).
102 // This will populate the entire table, even if the interrupt
103 // The shell ISR routines are found in F2837xD_DefaultIsr.c.
104     InitPieVectTable();
105 }
106
107 void Init_DACs(){
108 // Enable DACOUTA
109     EALLOW;
110 //Use VDAC as the reference for DAC
111     DacARegs.DACCTL.bit.DACREFSEL = 1;
112 //Enable DAC output
113     DacARegs.DACOUTEN.bit.DACOUTEN = 1;
114 //Set DAC to some initial value
115     DacARegs.DACVALS.bit.DACVALS = 2048;
116
117 //Use VDAC as the reference for DAC
118     DacBRegs.DACCTL.bit.DACREFSEL = 1;
119 //Enable DAC output

```

```

120     DacbRegs.DACOUTEN.bit.DACOUTEN = 1;
121     //Set DAC to some initial value
122     DacbRegs.DACVALS.bit.DACVALS = 2048;
123
124     //Use VDAC as the reference for DAC
125     DaccRegs.DACCTL.bit.DACREFSEL = 1;
126     //Enable DAC output
127     DaccRegs.DACOUTEN.bit.DACOUTEN = 1;
128     //Set DAC to some initial value
129     DaccRegs.DACVALS.bit.DACVALS = 2048;
130     EDIS;
131 }
132
133 void Init_EPwms()
134 {
135     // Enable ePWM clocks
136     CpuSysRegs.PCLKCR2.bit.EPWM1=1;
137     CpuSysRegs.PCLKCR2.bit.EPWM2=1;
138     // CpuSysRegs.PCLKCR2.bit.EPWM3=1;
139     CpuSysRegs.PCLKCR2.bit.EPWM4=1;
140     CpuSysRegs.PCLKCR2.bit.EPWM5=1;
141     CpuSysRegs.PCLKCR2.bit.EPWM6=1;
142     CpuSysRegs.PCLKCR2.bit.EPWM7=1;
143     CpuSysRegs.PCLKCR2.bit.EPWM8=1;
144     CpuSysRegs.PCLKCR2.bit.EPWM9=1;
145
146     // Initialize GPIO mux for desired ePWM
147     // These functions are defined in F2837xD_EPwm.c
148     InitEPwm1Gpio();
149     InitEPwm2Gpio();
150     // InitEPwm3Gpio();
151     InitEPwm4Gpio();
152     InitEPwm5Gpio();
153     InitEPwm6Gpio();
154     InitEPwm7Gpio();
155     InitEPwm8Gpio();
156     InitEPwm9Gpio();
157
158     InitEPwm_Leader(EPwm_CH1, period_sw, duty, 0, 0,
159     EPwm_Mod_TrailingTriangle, EPwm_Comp_True);
160     // Leader pwm of epwm modules - Not connected to a physical switch
161
162     InitEPwmA_X(EPwm_CH4, period_sw, duty, ph_1, deadtime_1,
163     EPwm_Mod_TrailingTriangle, EPwm_Comp_True, dir_1); //Switch 1
164     InitEPwmA_X(EPwm_CH5, period_sw, duty, ph_2, deadtime_1,
165     EPwm_Mod_TrailingTriangle, EPwm_Comp_True, dir_2); //Switch 2
166     InitEPwmA_X(EPwm_CH6, period_sw, duty, ph_3, deadtime_1,
167     EPwm_Mod_TrailingTriangle, EPwm_Comp_True, dir_3); //Switch 3
168     InitEPwmA_X(EPwm_CH7, period_sw, duty, ph_4, deadtime_1,
169     EPwm_Mod_TrailingTriangle, EPwm_Comp_True, dir_4); //Switch 4

```

```

165     InitEPwmA_X(EPwm_CH8, period_sw, duty, ph_5, deadtime_1,
166     EPwm_Mod_TrailingTriangle, EPwm_Comp_True, dir_5); //Switch 5
167 }
168
169 // This function arbitrarily configures basic functionality for all ePWM
170 // modules -- PWM channel, period, duty cycle, deadtime, modulation type,
171 // complementary/not complementary
172 void InitEPwm_Leader(EPwm_Channel pwm_chan, int period, float duty_cycle,
173 float phase, int deadtime, EPwm_ModulationType pwm_modtype,
174 EPwm_ComplimentaryMode pwm_comp)
175 {
176     EALLOW;
177
178     ePWM[pwm_chan]->TBPRD = period; // Set timer period
179     ePWM[pwm_chan]->TBPHS.bit.TBPHS = 0; // Phase
180     ePWM[pwm_chan]->TBCTR = 0x0000; // Clear counter
181     ePWM[pwm_chan]->TBCTL.bit.PRDLT = TB_SHADOW;
182     ePWM[pwm_chan]->TBCTL.bit.PHSEN = TB_DISABLE;
183 // Disable phase loading
184 ePWM[pwm_chan]->TBCTL.bit.SYNCOSEL = TB_CTR_CMPB;
185 // output EPWMxSYNCO when TBCTR=0, configure pwm as a global (for syncing)
186 // (Note: the default is local)
187
188 ePWM[pwm_chan]->ETSEL.bit.INTEN = 1; // enable PWM
189 interrupt
190 ePWM[pwm_chan]->ETSEL.bit.INTSEL = ET_CTR_ZERO; // trigger
191 interrupt on TBCTR=0
192 ePWM[pwm_chan]->ETPS.bit.INTPRD = ET_1ST; // trigger
193 interrupt every time the above defined event happens
194
195 ePWM[pwm_chan]->TBCTL2.bit.PRDLDSYNC = 0x0; // update on
196 zero for the leader ePWM
197
198 // Set up TBCLK
199 switch(pwm_modtype) {
200     case EPwm_Mod_TrailingEdge :
201         ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_UP;
202         // Count up
203         ePWM[pwm_chan]->AQCTLA.bit.CAU = AQ_CLEAR;
204         ePWM[pwm_chan]->AQCTLA.bit.ZRO = AQ_SET;
205         break;
206     case EPwm_Mod_LeadingEdge :
207         ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_DOWN; // Count
208         down
209         ePWM[pwm_chan]->AQCTLA.bit.CAD = AQ_SET;
210         ePWM[pwm_chan]->AQCTLA.bit.PRDLT = AQ_CLEAR;
211         break;
212     case EPwm_Mod_TrailingTriangle :

```

```

204         ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count
        up then count down
205         ePWM[pwm_chan]->TBPRD = (ePWM[pwm_chan]->TBPRD)/2;
206         ePWM[pwm_chan]->AQCTLA.bit.CAU = AQ_CLEAR;
207         ePWM[pwm_chan]->AQCTLA.bit.CAD = AQ_SET;
208         break;
209     case EPwm_Mod_LeadingTriangle :
210         ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
211         ePWM[pwm_chan]->TBPRD = (ePWM[pwm_chan]->TBPRD)/2;
212         ePWM[pwm_chan]->AQCTLA.bit.CAU = AQ_SET;
213         ePWM[pwm_chan]->AQCTLA.bit.CAD = AQ_CLEAR;
214         break;
215     default :
216         break;
217 }
218
219     ePWM[pwm_chan]->TBCTL.bit.HSPCLKDIV = TB_DIV1;
220 // Clock ratio to SYSCLKOUT is equal to 1 (sysclock = epwm clock)
221     ePWM[pwm_chan]->TBCTL.bit.CLKDIV = TB_DIV1;
222     ePWM[pwm_chan]->CMPCTL.bit.SHDWAMODE = CC_SHADOW;
223 //configure pwm as a local (for syncing) (Note: the default is local),
    enable shadow mode
224     ePWM[pwm_chan]->CMPCTL.bit.SHDWBMODE = CC_SHADOW;
225     ePWM[pwm_chan]->CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
226     ePWM[pwm_chan]->CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;
227 // Setup compare (aka duty cycle)
228     ePWM[pwm_chan]->CMPA.bit.CMPA = duty_cycle; //(ePWM[pwm_chan]->TBPRD)*
    duty_cycle;
229 // Set up PWMxA and PWMxB, and setup the deadband
230     ePWM[pwm_chan]->DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
231     ePWM[pwm_chan]->DBCTL.bit.IN_MODE = DBA_ALL;
232     switch(pwm_comp) {
233     case EPwm_Comp_True :
234         ePWM[pwm_chan]->DBCTL.bit.POLSEL = DB_ACTV_HIC;
235 // Active high complimentary mode. ePWMxB is inverted.
236         break;
237     case EPwm_Comp_False :
238         ePWM[pwm_chan]->DBCTL.bit.POLSEL = DB_ACTV_HI;
239 // Active high mode. ePWMxA and ePWMxB are in phase.
240         break;
241     default :
242         break;
243     }
244     ePWM[pwm_chan]->DBRED.bit.DBRED = 0;
245     ePWM[pwm_chan]->DBFED.bit.DBFED = 0;
246     EDIS;
247 }
248
249 void InitEPwmA_X(EPwm_Channel pwm_chan, int period, float duty_cycle,
    float phase, int deadtime, EPwm_ModulationType pwm_modtype,

```



```

EPwm_ComplimentaryMode pwm_comp, int dir)
250 {
251     EALLOW;
252
253     ePWM[pwm_chan]->TBPRD = period;
254     ePWM[pwm_chan]->TBCTR = 0x0000;
255     ePWM[pwm_chan]->TBCTL.bit.PHSEN = TB_ENABLE;
256     ePWM[pwm_chan]->TBCTL.bit.HSPCLKDIV = TB_DIV1;
257     ePWM[pwm_chan]->TBCTL.bit.CLKDIV = TB_DIV1;
258     ePWM[pwm_chan]->TBCTL.bit.SYNCSEL = TB_SYNC_IN;
259     ePWM[pwm_chan]->TBCTL.bit.PRDL = TB_SHADOW;
260     ePWM[pwm_chan]->TBCTL2.bit.PRDLDSYNC = 0x2;
261
262     //YW - linking of ePWMmodule to another one - link to the leader one
263     ePWM[pwm_chan]->EPWMXLINK.bit.TBPRDLINK = 0x0;
264     ePWM[pwm_chan]->EPWMXLINK.bit.CMPALINK = 0x0;
265
266     // Setup TBCLK
267     switch(pwm_modtype) {
268         case EPwm_Mod_TrailingEdge :
269             ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_UP;    // Count up
270     // Set actions -- Note: these values are closely tied to the CTRMODE and
271     // POLSEL bits
272         ePWM[pwm_chan]->AQCTLA.bit.CAU = AQ_CLEAR;
273         ePWM[pwm_chan]->AQCTLA.bit.ZRO = AQ_SET;
274         // Set ePWMxA high when TBCTR = 0
275         ePWM[pwm_chan]->AQTSRCSEL.bit.T1SEL = 0x7;
276         ePWM[pwm_chan]->AQCTL.bit.LDAQASYNC = 0x1;
277
278         break;
279         case EPwm_Mod_LeadingEdge :
280             ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_DOWN;    // Count
281     down
282         ePWM[pwm_chan]->AQCTLA.bit.CAD = AQ_SET;
283         ePWM[pwm_chan]->AQCTLA.bit.PRDL = AQ_CLEAR;
284         break;
285         case EPwm_Mod_TrailingTriangle :
286             ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
287             ePWM[pwm_chan]->TBPRD = (ePWM[pwm_chan]->TBPRD)/2;
288             ePWM[pwm_chan]->AQCTLA.bit.CAU = AQ_CLEAR;
289             ePWM[pwm_chan]->AQCTLA.bit.CAD = AQ_SET;
290             ePWM[pwm_chan]->AQTSRCSEL.bit.T1SEL = 0x7;
291             ePWM[pwm_chan]->AQCTL.bit.LDAQASYNC = 0x1;
292         case EPwm_Mod_LeadingTriangle :
293             // Count up then count down
294             ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
295             ePWM[pwm_chan]->TBPRD = (ePWM[pwm_chan]->TBPRD)/2;
296             ePWM[pwm_chan]->AQCTLA.bit.CAU = AQ_SET;
297             ePWM[pwm_chan]->AQCTLA.bit.CAD = AQ_CLEAR;
298             ePWM[pwm_chan]->TBCTL.bit.PHSDIR = dir;

```

```

297         break;
298     default :
299         break;
300 }
301 // Setup compare register loading
302 //YW: Set shadow mode, compare value is NOT loaded immediately
303 ePWM[pwm_chan]->CMPCTL.bit.SHDWAMODE = CC_SHADOW;
304 ePWM[pwm_chan]->CMPCTL.bit.SHDWBMODE = CC_SHADOW;
305 //Load on synchronization EVENT
306 ePWM[pwm_chan]->CMPCTL.bit.LOADASYNC = 0x2;
307 ePWM[pwm_chan]->CMPCTL.bit.LOADBSYNC = 0x2;
308
309 // Setup compare (aka duty cycle)
310 ePWM[pwm_chan]->CMPA.bit.CMPA = (ePWM[pwm_chan]->TBPRD)*duty_cycle;
311 ePWM[pwm_chan]->TBPHS.bit.TBPHS = (ePWM[pwm_chan]->TBPRD)*phase;
312
313 // Set up PWMxA and PWMxB, and setup the deadband
314 ePWM[pwm_chan]->DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
315 ePWM[pwm_chan]->DBCTL.bit.IN_MODE = DBA_ALL;
316
317 switch(pwm_comp) {
318     case EPwm_Comp_True :
319         ePWM[pwm_chan]->DBCTL.bit.POLSEL = DB_ACTV_HIC;           //
320         Active high complimentary mode. ePWMxB is inverted.
321         break;
322     case EPwm_Comp_False :
323         ePWM[pwm_chan]->DBCTL.bit.POLSEL = DB_ACTV_HI;           //
324         Active high mode. ePWMxA and ePWMxB are in phase.
325         break;
326     default :
327         break;
328 }
329
330 ePWM[pwm_chan]->DBRED.bit.DBRED = deadtime; //deadtime;
331 ePWM[pwm_chan]->DBFED.bit.DBFED = deadtime; //deadtime;
332 EDIS;
333 }
334
335 void InitEPwmB_X(EPwm_Channel pwm_chan, int period, float duty_cycle,
336 float phase, int deadtime, EPwm_ModulationType pwm_modtype,
337 EPwm_ComplimentaryMode pwm_comp)
338 {
339     EALLOW;
340     // Setup TBCLK
341     switch(pwm_modtype) {
342         case EPwm_Mod_TrailingEdge :
343             ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_UP;           //
344             Count up
345             ePWM[pwm_chan]->AQCTLB.bit.CBU = AQ_CLEAR;
346             ePWM[pwm_chan]->AQCTLB.bit.ZRO = AQ_SET;

```

```

342         break;
343     case EPwm_Mod_LeadingEdge :
344         ePWM[pwm_chan]->TBCTL.bit.CTRMODE = TB_COUNT_DOWN;        //
    Count down
345         ePWM[pwm_chan]->AQCTLB.bit.CBD = AQ_SET;
346         // Set ePWMxB low when TBCTR = CMPB (and TBCTR is decremting
    )
347         ePWM[pwm_chan]->AQCTLB.bit.PRD = AQ_CLEAR;
348         // Set ePWMxB low when TBCTR = TBPRD
349         break;
350     case EPwm_Mod_TrailingTriangle :
351         ePWM[pwm_chan]->AQCTLB.bit.CBU = AQ_CLEAR;
352         // Set ePWMxB low when TBCTR = CMPB (and TBCTR is incrementing
    )
353         ePWM[pwm_chan]->AQCTLB.bit.CBD = AQ_SET;
354         // Set ePWMxB high when TBCTR = CMPB (and TBCTR is
    decremting)
355         break;
356     case EPwm_Mod_LeadingTriangle :
357         ePWM[pwm_chan]->AQCTLB.bit.CBU = AQ_SET;
358         // Set ePWMxB high when TBCTR = CMPB (and TBCTR is
    incrementing)
359         ePWM[pwm_chan]->AQCTLB.bit.CBD = AQ_CLEAR;
360         // Set ePWMxB low when TBCTR = CMPB (and TBCTR is decremting
    )
361         break;
362     default :
363         break;
364 }
365 // Setup compare (aka duty cycle)
366 ePWM[pwm_chan]->CMPB.bit.CMPB = (ePWM[pwm_chan]->TBPRD)*duty_cycle;
367 EDIS;
368 }
369
370 // This function configures the specified EPwm channel for triggering ADC
    events
371 void InitEPwmADC(EPwm_Channel pwm_chan)
372 {
373     // Disable phase loading, already disabled in InitEPwm_X()
374     ePWM[pwm_chan]->TBCTL.bit.PHSEN = TB_DISABLE;
375     ePWM[pwm_chan]->TBCTL.bit.SYNCSEL = TB_CTR_ZERO;
376         ePWM[pwm_chan]->ETSEL.bit.SOCAEN = 1; // enable SOC on A
    group
376     ePWM[pwm_chan]->ETSEL.bit.SOCASEL = ET_CTR_PRD; // Select SOC on TBCTR
    = PRD
377     ePWM[pwm_chan]->ETPS.bit.SOCAPRD = ET_1ST; // Generate pulse on 1st
    event
378 }
379
380 void Init_interrupts()

```

```

381 { // Step 1: Disable interrupts globally, disable CPU interrupts
382     DINT;
383 // Initialize the PIE control registers to their default state.
384     InitPieCtrl();
385 // Disable CPU interrupts and clear all CPU interrupt flags:
386     EALLOW;
387     IER = 0x0000;
388     IFR = 0x0000;
389     EDIS;
390 // Step 2: Enable the PIE by setting the ENPIE bit of the PIECTRL register
    . //Initialize the PIE vector table with pointers to the shell
    Interrupt
391 // Service Routines (ISR).
392 // Enable the PIE
393     PieCtrlRegs.PIECTRL.bit.ENPIE = 1;
394 // Step 3: Write the ISR vector for each interrupt to the appropriate
    location in the PIE vector table, which can be found in Table 2-2.
395     EALLOW;
396 // Step 4: Set the appropriate PIEIERx bit for each interrupt. The PIE
    group and channel assignments can be found in Table 2-2.
397 //Enable PIE interrupt (see Table 2.2 of Technical Reference Manual)
398     PieCtrlRegs.PIEIER3.bit.INTx1 = 0x0001; //Enable epwm1 interrupt
399 // Step 5: Set the CPU IER bit for any PIE group containing enabled
    interrupts.
400     IER |= M_INT3; //Enable group 1 interrupts
401     EDIS;
402 }
403
404 void Enable_interrupts()
405 { // Enable global Interrupts and higher priority real-time debug events:
406     EINT; // Enable Global interrupt INTM
407     ERTM; // Enable Global realtime interrupt DBGM
408 }
409
410 void Init_ADCs()
411 { // Initialize ADC sampling
412     InitADCa();
413     InitADCb();
414     //InitADCc();
415     //InitADCd();
416 }
417
418 void InitADCa(void)
419 {
420     EALLOW;
421     AdcaRegs.ADCCTL2.bit.PRESCALE = 6; //set ADCCLK divider to /4, So
    running at 50 MHz
422     AdcSetMode(ADC_ADCA, ADC_RESOLUTION_12BIT, ADC_SIGNALMODE_SINGLE);
423     AdcaRegs.ADCCTL1.bit.INTPULSEPOS = 1;
424 //interrupt at end of the conversion

```

```

425     AdcaRegs.ADCCTL1.bit.ADCPWDNZ = 1;
426     AdcaRegs.ADCSOC0CTL.bit.CHSEL = 0;
427     AdcaRegs.ADCSOC0CTL.bit.ACQPS = 50;
428     AdcaRegs.ADCSOC0CTL.bit.TRIGSEL = 5;
429     EDIS;
430 }
431
432 void InitADCb(void)
433 {
434     EALLOW;
435     AdcbRegs.ADCCTL2.bit.PRESCALE = 6; //set ADCCLK divider to /4, So
    running at 50 MHz
436     AdcSetMode(ADC_ADCB, ADC_RESOLUTION_12BIT, ADC_SIGNALMODE_SINGLE);
437     AdcbRegs.ADCCTL1.bit.INTPULSEPOS = 1;
438     AdcbRegs.ADCCTL1.bit.ADCPWDNZ = 1;
439     AdcbRegs.ADCSOC0CTL.bit.CHSEL = 0;
440     AdcbRegs.ADCSOC0CTL.bit.ACQPS = 50;
441     AdcbRegs.ADCSOC0CTL.bit.TRIGSEL = 5;
442     AdcbRegs.ADCINTSEL1N2.bit.INT1SEL = 0; //end of SOCO (i.e. EOC0) will
    set INT1 flag
443     AdcbRegs.ADCINTSEL1N2.bit.INT1E = 1; //enable INT1 flag
444     AdcbRegs.ADCINTSEL1N2.bit.INT1CONT = 0; //No further ADCINT1 pulses
    are generated until ADCINT1 flag is cleared by user
445     AdcbRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //make sure INT1 flag is
    cleared
446     EDIS;
447 }
448
449 void InitADCC(void)
450 {
451     EALLOW;
452     AdccRegs.ADCCTL2.bit.PRESCALE = 6; //set ADCCLK divider to /4
453     AdcSetMode(ADC_ADCC, ADC_RESOLUTION_12BIT, ADC_SIGNALMODE_SINGLE);
454     AdccRegs.ADCCTL1.bit.INTPULSEPOS = 1;
455     AdccRegs.ADCCTL1.bit.ADCPWDNZ = 1;
456     AdccRegs.ADCSOC0CTL.bit.CHSEL = 2;
457     AdccRegs.ADCSOC0CTL.bit.ACQPS = 50; //sample window (# of SYSCLK,
    needs to corresponds to at least 75ns)
458     AdccRegs.ADCSOC0CTL.bit.TRIGSEL = 5; //trigger on ePWM1a SOCA
459     EDIS;
460 }
461
462 void InitADCd(void)
463 {
464     EALLOW;
465     //write configurations
466     AdcdRegs.ADCCTL2.bit.PRESCALE = 6;
467     AdcSetMode(ADC_ADCD, ADC_RESOLUTION_12BIT, ADC_SIGNALMODE_SINGLE);
468     AdcdRegs.ADCCTL1.bit.INTPULSEPOS = 1;
469     AdcdRegs.ADCCTL1.bit.ADCPWDNZ = 1;

```

```

470     AdcdRegs.ADCS0C0CTL.bit.CHSEL = 1;
471     AdcdRegs.ADCS0C0CTL.bit.ACQPS = 50;
472     AdcdRegs.ADCS0C0CTL.bit.TRIGSEL = 5;
473     EDIS;
474 }
475     DELAY_US(700000);
476 }
477 // This function waits until all enabled ADC conversions are finished.
478 void ADC_conversion_wait(void)
479 { // Make sure all ADC conversions are finished (check interrupt flag)
480     while (AdcbRegs.ADCINTFLG.bit.ADCINT1 != 1);
481 }
482 void ADC_clear_all_interrupt_flags(void)
483 { // Call all interrupt clear flag functions
484     ADC_clear_interrupt1_flag();
485 }
486 void ADC_clear_interrupt1_flag(void)
487 {
488     AdcbRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //clear INT1 flag on ADCB
489 }

```

Listing B.3: Initialization C file (**initialize.c**) initializing all functions/interrupts.

```

1  #ifndef globalvariables_H_
2  #define globalvariables_H_
3
4  #include "F28x_Project.h"
5  #include "globaldefine.h"
6  typedef enum
7  {
8      EPwm_CH1,
9      EPwm_CH2,
10     EPwm_CH3,
11     EPwm_CH4,
12     EPwm_CH5,
13     EPwm_CH6,
14     EPwm_CH7,
15     EPwm_CH8,
16     EPwm_CH9,
17     NUM_EPWM_CH
18 } EPwm_Channel;
19
20 typedef enum
21 {
22     EPwm_Mod_TrailingTriangle,
23     EPwm_Mod_LeadingEdge,
24     EPwm_Mod_TrailingEdge,
25     EPwm_Mod_LeadingTriangle
26 } EPwm_ModulationType;
27
28 typedef enum

```

```

29 {
30     EPwm_Comp_True ,
31     EPwm_Comp_False
32 } EPwm_ComplimentaryMode;
33
34 extern int dummy_read;
35
36 extern float ph_1;
37 extern float ph_2;
38 extern float ph_3;
39 extern float ph_4;
40 extern float ph_5;
41 extern float d;
42
43 extern int dir;
44 extern int dir_1;
45 extern int dir_2;
46 extern int dir_3;
47 extern int dir_4;
48 extern int dir_5;
49
50 extern int count_1;
51 extern int count_2;
52 extern int count_12;
53 extern int count_3;
54
55 extern int increase_1;
56 extern int increase_2;
57 extern int increase_3;
58
59 extern int deadtime_1;
60 extern float duty;
61
62 extern float theta;
63 extern float m_ref;
64 extern float ac_step;
65 extern float ac_dutyopen;
66 extern float theta;
67 extern float f_sw_min;
68
69 // for dynamic update of switching periods
70 extern uint16_t period_sw;
71
72 extern uint16_t ph_1_ctr;
73 extern uint16_t ph_2_ctr;
74 extern uint16_t ph_3_ctr;
75 extern uint16_t ph_4_ctr;
76 extern uint16_t ph_5_ctr;
77 extern uint16_t cmpa_ctr;

```

Listing B.4: Global variables definition header file (globalvariables.h)

```

1 #include "F28x_Project.h"
2 #include "globaldefine.h"
3 #include "globalvariables.h"
4
5 // Construct an array of EPWM_REGS structures (see "F2837xD_epwm.h")
6 volatile struct EPWM_REGS *ePWM[NUM_EPWM_CH] =
7     { &EPwm1Regs, &EPwm2Regs, &EPwm3Regs, &EPwm4Regs, &EPwm5Regs,
8       &EPwm6Regs, &EPwm7Regs, &EPwm8Regs, &EPwm9Regs};
9 float ph_1 = 0.8;
10 float ph_2 = 0.4;
11 float ph_3 = 0;
12 float ph_4 = 0.4;
13 float ph_5 = 0.8;
14
15 float d = 0;
16 int dir_1 = 0;
17 int dir_2 = 0;
18 int dir_3 = 0;
19 int dir_4 = 1;
20 int dir_5 = 1;
21 int count_1 = 0;
22 float duty = 0.5;
23 float m_ref = 0.85;
24 float theta = 0;
25 float ac_step = 60/100e3;
26 float ac_dutyopen = 0;
27
28 float f_sw_min = 40000;
29
30 int deadtime_1 = DEFAULT_DEADTIME;//+5
31 uint16_t period_sw = 2000; // variable switching period, will be updated
    continuously
32
33 uint16_t ph_1_ctr = 0;
34 uint16_t ph_2_ctr = 400;
35 uint16_t ph_3_ctr = 800;
36 uint16_t ph_4_ctr = 1200;
37 uint16_t ph_5_ctr = 1600;
38 uint16_t cmpa_ctr = 1000;
39 #endif /* GLOBAL_DEFINE_H_ */

```

Listing B.5: Global variables definition C file (globalvariables.c)

```

1 #ifndef globaldefine_H_
2 #define globaldefine_H_
3
4 #define SYSCLK          200000 // kHz, period is 5 ns
5 #define SWITCHING_FREQ  100 // kHz 1000
6 #define DEADTIME_NS     50 //ns
7 #define PERIOD           (int32) SYSCLK/SWITCHING_FREQ // 200MHz
    /160kHz = 1250

```



```

8 #define DEFAULT_DUTY          0.5
9 #define DEFAULT_DEADTIME      10      // DEFAULT_DEADTIME*5ns = 50ns, 5
    ns is period of sysclk, 2* takes into account updown count
10
11 #define EPWMCLK                SYSCLK
12 #define TBCLK                  EPWMCLK
13
14 #define AC_PERIOD              1666666 // HALF OF 3333333 FOR UPDOWN MODE
15 #define F_SW_MAX              120000 //kHz
16 #define F_SW_MIN              40000  //kHz
17 #define DELTA_I_PP            2.22    // target output inductor current
    ripple (A)
18 #define L                      0.000015 // output filter inductor size (
    H)
19 #define N                      6      // number of levels in the FCML
20 #define V_IN                  400    // input DC voltage
21
22 #define INV_1_N_1              0.2    // 1/(N-1)
23 #define INV_1_L                66666.66666666667 // 1/L
24 #define INV_1_DELTA_I_PP      0.4505 // 1/DELTA_I_PP
25
26 #define INV_1_C                333333.333333333 // 1/C C=3uF
27 #define INV_1_DELTA_V_PP      0.333333333 // 1/DELTA_V_PP 0.641 for 1.56
    Vpp 0.333333333 for 3Vpp use 3Vpp for >500W
28 #define INV_R_LOAD            0.01   //1/Rload
29 #endif /* GLOBAL_DEFINE_H_ */

```

Listing B.6: Global variables values definition header file (**globaldefine.h**)