UNIVERSITY OF CALIFORNIA

Santa Barbara

Development of Long-Cavity III-Nitride Vertical-Cavity Surface-Emitting Lasers

A dissertation submitted in partial satisfaction of the requirements for the degree

Doctor of Philosophy
in
Materials

By

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Committee in charge:

Professor Shuji Nakamura, Chair
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Professor James S. Speck
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June 2024

The dissertation of Nathan C. Palmquist is approved.

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Professor Shuji Nakamura, Committee Chair

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This dissertation is dedicated to my wife

Sydney Harmon

my parents

Bruce and Rhonda Palmquist

and my brother

Matt Palmquist

Acknowledgements

I am incredibly blessed by the many people in my life who have gotten me to this point in my career. First, I would like to thank Prof. Shuji Nakamura for giving me the opportunity to pursue this research, and for being so patient and optimistic especially throughout the disruptive COVID shutdown and leading up to my first VCSEL. I am particularly grateful for Dr. Dan Cohen, whose near daily support during the challenging development process kept me focused and motivated. I am also thankful for Prof. Steven Denbaars and Prof. Jim Speck for the many conversations we had about material characterization, applications, and industry perspectives. I would also like to thank the cleanroom staff, including Demis John, Biljana Stamenic, Brian Thibeault, and Mike Silva, for debugging processing issues, fixing tools last minute, and encouraging me to continue pushing forward. The 1000's of hours I spent in the cleanroom forged me into the scientist that I am today.

Next, I want to thank the educators who mentored me during formative periods of my life. I am thankful for influential high school teachers, including Don May, Jeff Hashimoto, and Debbie Rowden, who encouraged me to take risks and pursue a college degree far from home. Thank you to my mentors during my undergraduate years, including Prof. Orla Wilson, Dr. Stephen Farias, Dr. Ebuka Arinze, and Dr. Botong Qiu, for cultivating my love for science and discovery. A huge thank you to my undergraduate research advisor, Prof. Susanna Thon, for teaching me foundational research skills, and for giving me the confidence to attempt difficult projects. Your guidance as my first research advisor was invaluable throughout my PhD experience at UCSB.

Last, but certainly not least, I am so grateful for my family, friends, and colleagues who helped me in many ways, either directly with my research or by supporting and doing fun activities with me. To the SSLEEC students, past and present, thank you for the insightful conversations. To my family, Bruce, Rhonda, and Matt, thank you for your love and constant encouragement. Finally, I would like to thank my wife Sydney for her unwavering support throughout the PhD. Your encouragement, presentation edits, and enthusiasm for life helped me push through to the finish line. Thank you for always being there for me.

Curriculum Vitae

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EDUCATION

University of California, Santa Barbara *Aug 2018 - Feb 2024*

- Ph.D. – Materials
- Advisor: Shuji Nakamura
- Research focus: nonpolar vertical-cavity surface-emitting lasers

Johns Hopkins University *2012 – 2016*

- B.S. Materials Science and Engineering
- Concentration: Nanotechnology

PROFESSIONAL EXPERIENCE

UCSB Solid State Lighting and Energy Electronics Center *Aug 2018 - Present*

- Graduate student researcher
- Demonstrated CW electrically injected nonpolar GaN vertical-cavity surface-emitting lasers (VCSELS) using a topside monolithic GaN lens
- 1st demonstration of a GaN VCSEL with a topside lens and 1st demonstration of a nanoporous GaN distributed Bragg reflector (DBR) from UCSB, 1st topside GaN lens demonstration in the world

Johns Hopkins University, Thon NanoEnergy Lab *Feb 2014 - May 2016*

- Undergraduate student researcher
- Optimized performance properties of thin-film colloidal quantum dot solar cells by developing a computational method based on thin-film interference and particle swarm optimization and then fabricating devices based on results

Central Washington University, Jackson Lab *Summer 2013*

- Research assistant
- Discovered 28 new far infrared laser emissions from several isotopic forms of methanol via optical pumping with a Class IV CO_2 laser

MATERIALS FABRICATION & CHARACTERIZATION

Growth & Deposition	Processing	Characterization	Software
- Metal-organic chemical-vapor deposition - Ion beam deposition - Sputtering - Thermal & e-beam evaporation - PECVD - RIE/ICP dry etching - Atomic layer deposition	- Photolithography (contact, stepper, and Heidelberg MLA) - Ion implantation - Electrochemical etching - Rapid thermal annealer - Chemical-mechanical polishing - Flip-chip bonding	- SEM/FIB - Photoluminescence - LIV - AFM - Single-crystal XRD - SIMS - UV-Vis spectroscopy - Ellipsometry - IR thermal microscopy	- MATLAB - L-Edit - Lumerical FDTD - Klayout - ImageJ - Ilastik - SiLENSe - SRIM - COMSOL

PUBLICATIONS

1. **Palmquist, N. C.**; Kearns, J.; Gee, S.; Juan, A.; Gandrothula, S.; Lam, M.; Denbaars, S. P.; Nakamura, S. Demonstration of III-Nitride Vertical-Cavity Surface-Emitting Lasers with a Topside Dielectric Curved Mirror. *Appl. Phys. Express* **2023**.
2. **Palmquist, N. C.**; Anderson, R.; Kearns, J. A.; Back, J.; Trageser, E.; Gee, S.; Denbaars, S. P.; Nakamura, S. Long-Cavity M-Plane GaN-Based Vertical-Cavity Surface-Emitting Lasers with a Topside Monolithic Curved Mirror. *Photonics* **2023**, *10* (6), 646.
3. Wong, M. S.; Raj, A.; Chang, H.-M.; Rienzi, V.; Wu, F.; Ewing, J. J.; Trageser, E. S.; Gee, S.; **Palmquist, N. C.**; Chan, P.; Kang, J. H.; Speck, J. S.; Mishra, U. K.; Nakamura, S.; DenBaars, S. P. Improved Wall-Plug Efficiency of III-Nitride Tunnel Junction Micro-Light-Emitting Diodes with AlGaN/GaN Polarization Charges. *AIP Adv.* **2023**, *13* (1), 015107.
4. **Palmquist, N. C.**; Anderson, R.; Kearns, J. A.; Back, J.; Trageser, E.; Gee, S.; Denbaars, S. P.; Nakamura, S. Continuous-Wave Operation of Long-Cavity m-Plane GaN-Based Vertical-Cavity Surface-Emitting Lasers with a Topside Curved Mirror and Nanoporous GaN DBR. *Gallium Nitride Materials and Devices XVIII*; SPIE **2023**; Vol. 12421, pp 127–135.
5. Anderson, R.; Zhang, H.; Trageser, E.; **Palmquist, N.**; Wong, M.; Nakamura, S.; DenBaars, S. Green Edge Emitting Lasers with Porous GaN Cladding. *Opt. Express* **2022**, *30* (15), 27674–27682.
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7. Wong, M. S.; **Palmquist, N. C.**; Jiang, J.; Chan, P.; Lee, C.; Li, P.; Kang, J. H.; Baek, Y. H.; Kim, C. H.; Cohen, D. A.; Margalith, T.; Speck, J. S.; Nakamura, S.; DenBaars, S. P. Effects of Activation Method and Temperature to III-Nitride Micro-Light-Emitting Diodes with Tunnel Junction Contacts Grown by Metalorganic Chemical Vapor Deposition. *Appl. Phys. Lett.* **2021**, *119* (20), 202102.
8. Li, P.; Zhang, H.; Li, H.; Zhang, Y.; Yao, Y.; **Palmquist, N.**; Iza, M.; Speck, J. S.; Nakamura, S.; DenBaars, S. P. Metalorganic Chemical Vapor Deposition Grown N-InGaN/n-GaN Tunnel Junctions for Micro-Light-Emitting Diodes with Very Low Forward Voltage. *Semicond. Sci. Technol.* **2020**, *35* (12), 125023.
9. Li, P.; Zhang, H.; Li, H.; Iza, M.; Yao, Y.; Wong, M. S.; **Palmquist, N.**; Speck, J. S.; Nakamura, S.; DenBaars, S. P. Size-Independent Low Voltage of InGaN Micro-Light-Emitting Diodes with Epitaxial Tunnel Junctions Using Selective Area Growth by Metalorganic Chemical Vapor Deposition. *Opt. Express* **2020**, *28* (13), 18707.
10. Kearns, J. A.; Back, J.; **Palmquist, N. C.**; Cohen, D. A.; DenBaars, S. P.; Nakamura, S. Inhomogeneous Current Injection and Filamentary Lasing of Semipolar $(20\overline{2}1)$ Blue GaN-Based Vertical-Cavity Surface-Emitting Lasers with Buried Tunnel Junctions. *Phys. Status Solidi A* **2020**, *217* (7), 1900718.
11. Arinze, E. S.; Qiu, B.; **Palmquist, N.**; Cheng, Y.; Lin, Y.; Nyirjesy, G.; Qian, G.; Thon, S. M. Color-Tuned and Transparent Colloidal Quantum Dot Solar Cells via Optimized Multilayer Interference. *Opt. Express* **2017**, *25* (4), A101–A112.
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PRESENTATIONS

1. Laser Display and Lighting Conference (LDC), Yokohama, Japan, 2024, invited speaker.

2. International Conference on Nitride Semiconductors (ICNS), Fukuoka, Japan, 2023.
3. SSLEEC Review, Santa Barbara, USA, 2023.
4. SPIE Photonics West, San Francisco, USA, 2023.
5. SSLEEC Review, Santa Barbara, USA, 2022.

PATENTS

1. **Palmquist, N. C.**; [et al.], III-Nitride-Based VCSEL with Modified Emission Properties (patent pending).
2. **Palmquist, N. C.**; [et al.], Chemical Etch Assembly for Uniform III-Nitride Based Etching (patent pending).
3. **Palmquist, N. C.**; [et al.], III-Nitride Based VCSEL with Dielectric P-side Lens (patent pending).
4. Kearns, J.; [et al., including **Palmquist, N. C.**], WO2020243330A1, December 3, 2020.

FELLOWSHIPS & RECOGNITION

Heeger Fellowship	*Feb 2024*
Best Student Award, ICNS 14	*Nov 2023*
Graduate Certificate in Technology Management, UCSB	*July 2023*
SSLEEC Outstanding Researcher Award, UCSB	*Nov 2022, 2023*
Materials Department Service Award, UCSB	*July 2021*
Individualized Professional Skills Program, UCSB	*Mar. 2020*
Peter J. Frenkel Foundation Fellowship, IEE UCSB	*2019 - 2020*
Delegate (NanoDirect), 16th NanoBusiness Conference (NanoBCA)	*June 2017*
Best Nanotechnology Senior Presentation, Dept. Materials, JHU	*May 2016*
Huggins Fellowship, Dept. ECE, JHU	*Summer 2014/2015*
Dean's List, JHU	*Fall 2012, Fall 2013, Spring 2015*
5th Nationally, Management & Decision Making, FBLA	*Summer 2011*

Abstract

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GaN vertical-cavity surface-emitting lasers (VCSELs) show promise for numerous lighting, display, communications, and sensor applications due to their visible wavelength emission, low threshold current, high beam quality, and arraying capabilities. Primarily, research has been focused on short to medium cavity ($L<5\lambda$) VCSEL designs, prioritizing single longitudinal mode operation. However, GaN VCSELs struggle with thermal management due to self-heating from higher input power requirements, high optical losses from p-type GaN and current spreaders, and poor heatsinking from the typically low thermal conductivities of the bottomside distributed Bragg reflectors (DBRs). These issues result in a high thermal impedance, generally >1000 K/W, quick thermal rollover, and low device lifetimes. Recently, long cavity ($L>>5\lambda$) GaN VCSEL designs have shown significant promise towards addressing the issues of thermal stability and cavity length control but require substrate polishing and complex fabrication, limiting scalability for mass production.

To address these issues, a topside lens fabrication method is developed. Then, a 65λ GaN VCSEL with a topside lens, a buried tunnel junction current aperture, and bottomside epitaxial nanoporous GaN DBR was fabricated using standard microfabrication techniques. First, a topside GaN lens was demonstrated, with CW lasing achieved at lower current densities than comparable planar cavity VCSELs. However, the output power was limited by the high temperature regrowth required to fabricate the GaN lens as well as the high turn-on voltage. Next, a topside dielectric lens was developed which enabled CW lasing performance above 2mW for a GaN VCSEL with a partially etched porous DBR, and single

transverse mode operation for other VCSELs with fully etched porous DBRs. The devices show high thermal stability due to the long cavity, with an estimated thermal impedance of 600K/W measured on-chip.

Table of Contents

1 Introduction

Vertical-cavity surface-emitting lasers (VCSELs) are a unique class of semiconductor laser diode that emits a laser beam vertically from its top surface, setting it apart from conventional edge-emitting laser diodes which emit light from the sides of the device. This design gives VCSELs a combination of advantages, including low threshold currents, high-speed modulation, circular mode profiles with low divergence, and the ability to form 2D arrays[1]. The global VCSEL market, segmented into red (650-750nm), near-infrared or NIR (750-1400nm), and mid-wave infrared or MWIR (1400nm-3000nm), is currently valued at $2.4 billion, and is projected to grow at a compound annual growth rate (CAGR) of 18% until 2030[2]. Much of this demand is focused in automotive and sensing, with LIDAR and object recognition driving the projected forecast.

There is a high interest in industry for a robust, stable VCSEL platform that can emit across the visible spectrum (400-650nm). However, the current market is limited to red into the IR due to the maturity of the GaAs material systems. VCSELs spanning the visible spectrum would enable a new suite of applications in display, AR/VR, bio-sensing, and quantum photonics, while providing advantages to certain communications and sensing applications currently being serviced by IR VCSELs. For this wavelength range, gallium nitride (GaN) is the material system of choice, with emission options spanning ultraviolet, violet, blue, green, yellow, and red.

GaN VCSELs were first demonstrated in 2008, and have received significant research efforts from both industry and academic collaborators[3,4]. The University of California, Santa Barbara (UCSB) has been participating in the field since 2012, and has focused their efforts

on non-polar and semi-polar GaN VCSELs due to several advantages provided by the crystal orientation such as inherently polarized emission[5,6]. Until 2018, device demonstrations from UCSB were limited to pulsed operation (i.e. power was only injected intermittently, on the order of 0.5% each second) due to high thermal resistance and high threshold currents. For most practical applications, thermally stable continuous-wave (CW) operation is desired. In 2018, UCSB achieved its first demonstration of CW lasing by extending the cavity length of their design by a factor of 3, from 1,100nm to 3,500nm[7]. They accomplished this because longer cavities can dissipate heat more effectively than shorter cavities[8]. However, the thermal resistance was still incredibly high, attributed to the flip-chip process required to deposit the n-side dielectric distributed Bragg reflector (DBR).

Elsewhere in the field, a significantly longer cavity design was implemented which demonstrated high output powers, low threshold currents, and high wall plug efficiencies (WPE)[9,10]. In this work, the cavity length was extended significantly, to approximately 25,000nm. For long planar cavities with fixed mirror diameters, diffraction loss increases quickly with cavity length[10]. This effect has been used to suppress higher order transverse modes in other material systems, as higher order modes experience greater rates of diffraction loss[11]. Since the typical gain of GaN QWs is approximately 1% per pass, minimizing this source of loss is critical for long cavity designs. For the recent designs, lateral mode confinement was achieved by introducing a curved concave mirror on one side[12]. Converting one of the planar DBRs into a curved DBR mirror is a recognized method for establishing a stable resonator configuration. This configuration results in the formation of a beam waist on the planar side, effectively reducing diffraction losses. This approach confines the lateral mode, and as a consequence, the dimensions of the beam waist and its propagation within the

cavity are chiefly governed by two key parameters, the cavity length (L) and the radius of curvature (ROC) of the mirror.

The initial design demonstrated by Hamaguchi et al. prioritized low threshold conditions by placing the active region at the beam waist (100nm from the planar mirror) and minimizing aperture size[13]. Using this structure, they were able to demonstrate GaN VCSELs with record performances, all while achieving high device yields. However, the polished substrate introduces processing complexity, requiring handling of a thin, fragile substrate, and requiring backside alignment of the mirror. This approach has limited their demonstrations to only cm^2 substrates, and the pathway to scaling this design to larger substrates is unclear.

This dissertation builds on the long cavity design but with a focus on scalability and fabrication process efficiency. To gain the benefits of the ultra-long (L>10,000nm) cavity, a topside lens is developed, as described in section 2. To circumvent the thermally resistive flip-chip design, a nanoporous GaN DBR is also developed. Section 1 gives an overview of GaN optoelectronics and then into the specifics of GaN VCSEL design. Section 2 describes the growth of long cavity *m*-plane GaN VCSELs, as well as details the development process for the topside lens and nanoporous DBR. Section 3 and 4 detail the development of the topside GaN lens VCSEL and topside dielectric lens VCSEL, respectively. Section 5 may or may not exist.

1.1 Overview of GaN Optoelectronics

GaN-based optoelectronics have had a tremendous impact on the world. In 1993 Shuji Nakamura, with the help of colleagues Isamu Akasaki and Hiroshi Amano, invented the efficient GaN-based blue LED after years of intensive research efforts. This invention

revolutionized illumination technology and the three were awarded the 2014 Nobel Prize in Physics for their work[14]. White light can be efficiently generated by coating a blue GaN LED with a phosphor that converts a percentage of the incident blue light into yellow light. This method has led GaN LEDs to a 50% global market share for new residential lighting[15]. Incandescent light bulbs, with a low light output of ~16 lumens per watt, lose a majority of their energy to heat and have wall-plug efficiencies (WPE) on the order of 5%. By comparison, phosphor-converted GaN LEDs emit up to 300 lumens per watt with a WPE of 50%. The increasing market share of GaN LEDs thus represents a significant energy savings, up to 569 TWh of electrical energy globally by 2035[16].

While the device epitaxial structure shares similarities to LEDs, GaN edge-emitting laser diodes (EELDs) require significantly more complex fabrication steps to create the optical cavity and enable lasing. Compared to LEDs, laser diodes have several advantages, including higher power densities and higher efficiencies at high current densities. This has made GaN-based laser diodes attractive for high power and directional applications, such as automotive headlights, laser cutting, and directional projectors.

Of the three classes of optoelectronics, LEDs, EELDs, and VCSELs, GaN VCSELs are the only device type not commercially realized. Compared to LEDs, VCSELs share the surface-emission, small form factor, and mass manufactured array capabilities. Compared to EELDs, VCSELs share the stimulated emission, lower divergence angle, and stringent requirements for material quality, mirrors, and optical and current confinement. However, VCSEL requirements are even more stringent than EELDs. Due to the low overlap between the active region and the confined light, which is on the order of 1%, the top and bottom mirror reflectivities must both exceed 99% to reach the threshold for lasing. While GaN EELDs were

demonstrated back in 1996[17], only 3 years after the first GaN LED, the first GaN VCSEL wouldn't be demonstrated until over a decade later in 2008[3,4].

1.1.1 III-Nitride Materials System

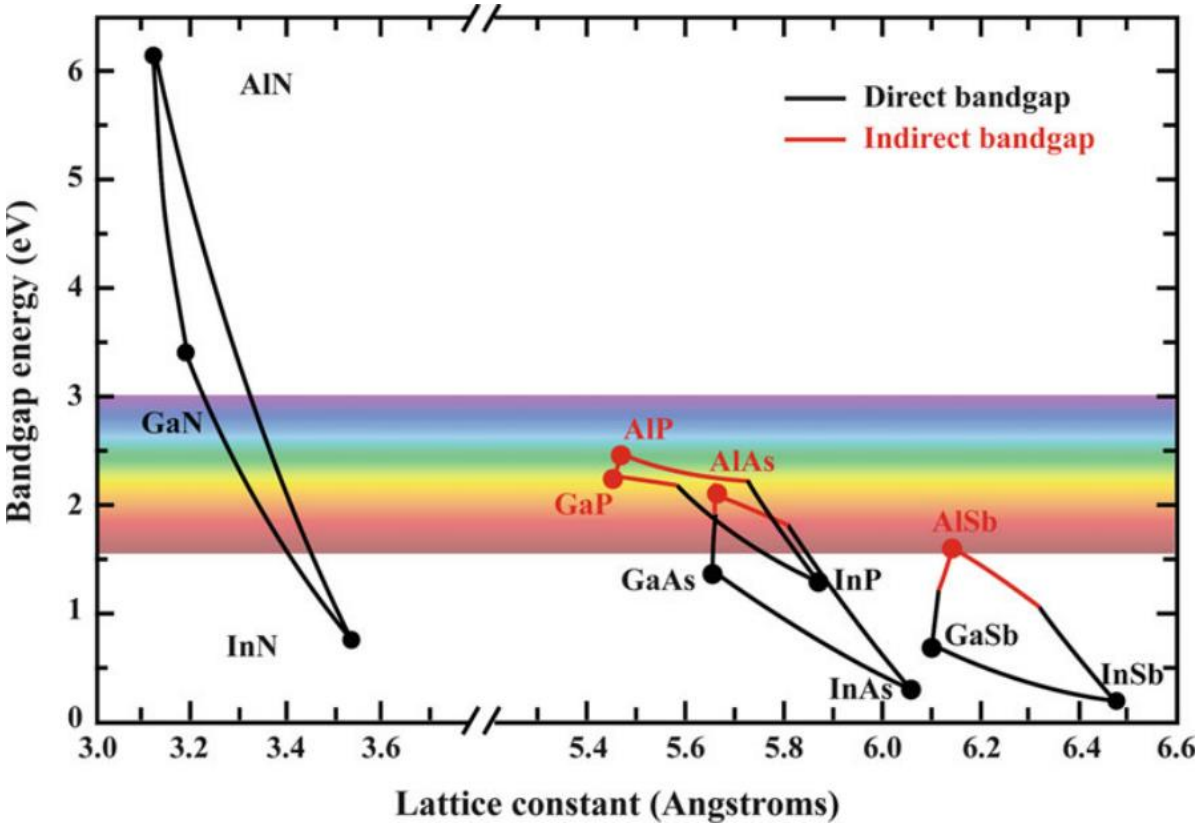

Figure 1.1. Band gap energy versus lattice constant at 300 K for several popular III-V compound semiconductors. The connecting lines indicate various alloys that can be formed between connecting materials. Reprinted from [Zhu D., Humphreys C.J. (2016) Solid-State Lighting Based on Light Emitting Diode Technology. In: Al-Amri M., El-Gomati M., Zubairy M. (eds) Optics in Our Time. Springer, Cham] under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/).

The group III-nitride materials system consists of both direct and in-direct bandgap compound semiconductors with emission wavelengths that range from the UV, through the entire visible spectrum, and into the NIR and MWIR. The bandgap energy versus lattice constant for various III-nitride semiconductor material systems is shown in Figure 1.1, with lines denoting available alloy pairings[18].

The emission wavelength can be calculated using the equation below,

$$E_g = \frac{hc}{\lambda} \approx \frac{1240\ eV \cdot nm}{\lambda} \tag{1.1}$$

where E_g is the bandgap energy in electron volts (eV), *h* is Planck's constant, *c* is the speed of light, and λ is the wavelength in nanometers (nm). The band gap energies listed above span from 207nm for AlN all the way to 3,500nm for InAs. Within the (In, Al, Ga)N family, the emission range spans from 207nm for AlN, 365nm for GaN, and 1771nm for InN. The emission wavelength can be approximately linearly tuned between these values by varying the composition of AlGaN or InGaN ternary alloys, as shown by the solid lines in Figure 1.1.

Unfortunately, while InGaN (AlGaN) has the same crystal structure as GaN, the larger (smaller) size and bonding strength of the In (Al) atoms relative to GaN leads to crystal lattice parameters that are larger (smaller) than GaN. This leads to compressive (tensile) stresses for films grown epitaxially on GaN. The relatively large lattice mismatch between AlN, InN, and GaN can lead to material defect formation and polarization electric fields. This makes expanding into green and red wavelengths difficult as the active region requires higher and higher indium compositions. Additionally, in order to incorporate these high compositions, the growth temperature of the InGaN quantum well structures must be decreased, which leads to increased impurity incorporation and growth defects[19].

GaN's most stable phase is a hexagonal wurtzite crystal structure with a 6mm point group and a C_{6v}^4-P6$_3$mc space group. GaN has six-fold rotation symmetry and two mirror planes[20]. Each atom of Ga or N is surrounded by four N or Ga atoms, respectively, in a tetrahedral orientation. As a result, the lattice is asymmetric in the (0001) direction, leading to spontaneous polarization fields. In asymmetrical directions, characterized by the inclination angle (Θ) with respect to basal c-plane, the spontaneous polarization field can be reduced or eliminated[21]. In the case where Θ=90^o, the crystal is oriented along the (1-100) (m-plane) or (11-20) (a-plane) directions and the crystal is symmetric (that is, there are an equal amount of Ga/N atoms above and below parallel planes). While both m-plane and a-plane are nonpolar, the devices that will be discussed in this dissertation are exclusively m-plane. As such, any

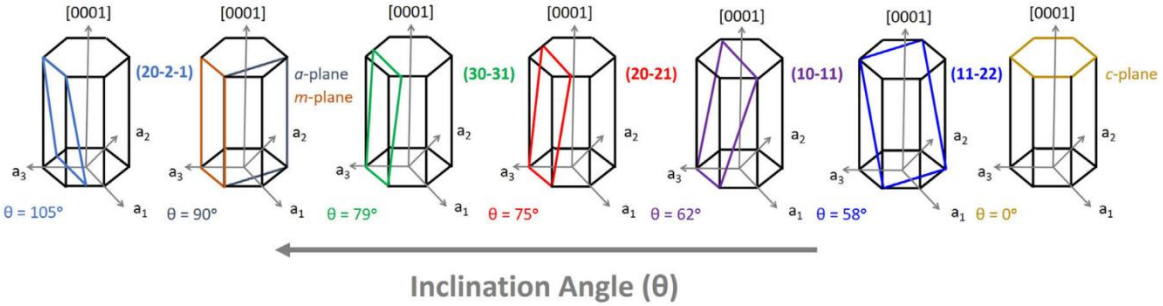

Figure 1.2. Schematics of selected crystal planes in a Wurtzite GaN latticed characterized by different inclination angles (θ) relative to the *c*-plane. Copyright © 2018 Wiley-VCH GmbH. Reprinted with permission.

reference to nonpolar refers to the m-plane. Any intermediate plane $0^o < \Theta \neq 90^o < 180^o$ is referred to as semipolar and exhibits a reduced spontaneous and piezoelectric polarization field relative to c-plane. A selection of typical nonpolar and semipolar planes are summarized in Figure 1.2.

In addition to spontaneous polarization, piezoelectric polarization occurs due to lattice-mismatch-induced strain. This effect in GaN VCSELs is most impactful at the InGaN/GaN QW interface, as the combined polarization effects can result in significant band

tilting and Quantum Confined Stark Effect (QCSE)[22]. However, these polarization effects are highly dependent on crystal orientation; for InGaN layers, total polarization becomes zero for nonpolar orientations and at Θ=45 ^{o}, and at off-angles exhibits varying degrees of polarization with magnitudes varying based on indium composition[23]. These varying degrees of polarization have different effects on the magnitude and direction of the QW tilt, which impact device performance.

In c-plane InGaN/GaN Ga-polar QWs, the built-in E-field (E_{bi}) and piezoelectric E-field (E_{pz}) are antiparallel, with E_{pz} being much larger, resulting in heavy QW tilt downward along the growth direction when the built-in field vanishes under forward bias that reduces overlap between electron/hole wavefunctions. In InGaN/GaN interfaces at all orientations, the spontaneous polarization (E_{sp}) has a comparably small impact on band tilting compared to E_{bi}/E_{pz}. This band tilting causes carrier separation, as holes crowd to one side of the tilted well in the VB and electrons in the CB crowd to the opposite side. This crowding reduces the effective band gap of the semiconductor and is referred to as the QCSE. This carrier separation leads to lower recombination and thus is considered detrimental to device performance. For comparison, the E_{sp}/E_{pz} in m-plane nonpolar InGaN/GaN QWs is zero, resulting in a flat band that is only influenced by the external bias. Interestingly, the semipolar (10-1-1) and (20-2-1) directions exhibit downward bending behavior similar to c-plane (albeit at reduced magnitude) while the (11-22) and (20-21) orientations exhibit upward bending due to E_{bi} and E_{pz} being parallel. Figure 1.3 shows simulated band diagrams for $In_{0.2}Ga_{0.8}N$/GaN single QWs grown at various crystal orientations.

A study by Feezell et al. found that the semipolar (20-2-1) was a special case amongst semipolar orientations with a nearly flat band in the QW similar to *m*-plane[24]. This was due to the aforementioned antiparallel nature of its E_{bi} and E_{pz} fields which caused them to all but cancel each other out and led to the highest overlap of any orientation up to current densities of ~100A/cm^2. This advantage likely decreases at higher current densities required for VCSEL lasing (~1 kA/cm^2) where Coulomb charges begin to shield the polarization-induced field.

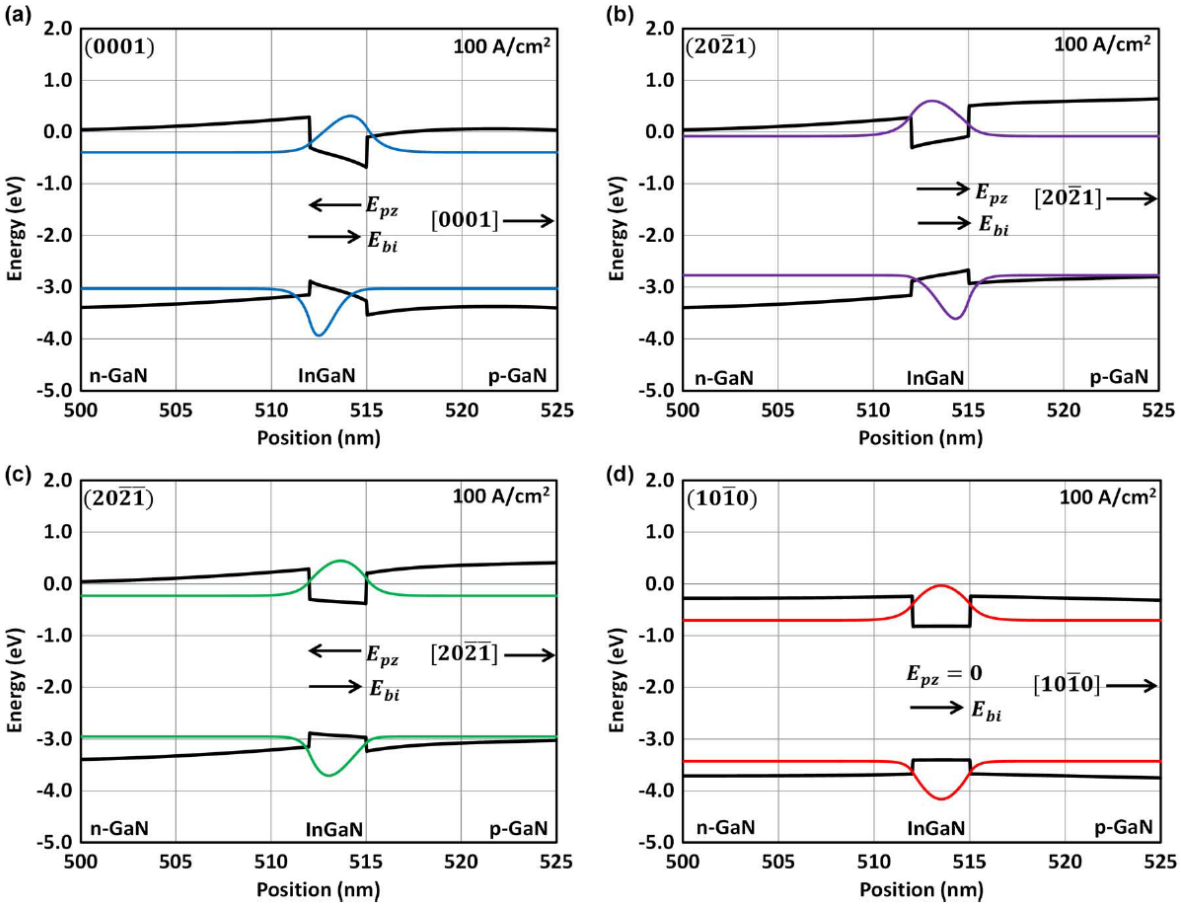

Figure 1.3. Simulated energy band diagrams for 3nm InGaN single QWs with GaN barriers at an injected current density of 100A/cm^2 for (a) polar *c*-plane, (b) semipolar (20-21), (c) semipolar (20-2-1), and (d) nonpolar *m*-plane (10-10). The ground-state electron and hole wavefunctions are shown as well as the direction of the piezoelectric and built-in field.

The main benefit of an increased wavefunction overlap comes from an increase in the recombination coefficients, which include the Shockley-Read-Hall recombination coefficient, A, the bimolecular recombination coefficient, B, and the Auger recombination coefficient, C,

which are all suggested to be proportional to the square of wavefunction overlap[20]. At high current densities, the current density is described as

$$J = qd(AN + BN^2 + CN^3) \quad (1.2)$$

where J is the current density, N is the carrier density, d is the active region thickness (QW thickness times the number of wells), and q is the electron charge. This means that, for a given carrier density, the result current density will be higher for semipolar/nonpolar orientations. This is important because it helps mitigate efficiency droop, which occurs when the internal quantum efficiency (IQE) decreases at high current densities. IQE is described by

$$\eta_{IQE} = \eta_i \frac{BN^2}{AN+BN^2+CN^3} \quad (1.3)$$

where η_i is the injection efficiency. It can be seen that as N increases, the denominator BN^2 and CN^3 components also increase, with CN^3 dominating at high N. Another advantage of increased wavefunction overlap in non-polar and semipolar GaN is an increase in recombination rates, as well as higher optical gain[20]. This is especially relevant to laser diode structures which operate at high current densities and rely on optical gain for performance and output.

Besides increased wavefunction overlap, the differences in electronic band structure between c-plane and nonpolar/semipolar orientations also leads to a near 50% reduction in calculated hole mass with increasing crystal angle[25]. This further increases the rate at which current density can improve optical gain, and is coupled with the benefits discussed previously.

A final important property of nonpolar and semipolar GaN comes from the emission anisotropy. The band structure of GaN consists of 4s orbitals in the conduction band from the Ga atom, and 2p orbitals in the valence band from the N atom. For c-plane, the px and py orbitals are degenerate in-plane, and both are equally effected by the compressive strain introduced by InGaN QWs. This means that, within the QW, carriers will relax into the orbitals at equal rates, and release photons polarized into either the x- or y- directions. For c-plane VCSEL arrays, this leads to random polarization states between neighboring VCSELs. However, for semipolar and nonpolar orientations, the compressive strain introduced is anisotropic in-plane. This asymmetry reflects itself in the band structure, as can be seen in Figure 1.4 for the valence band structure of a 3.5nm $In_{0.15}Ga_{0.85}N$/GaN QW on c-plane and m-plane. It can be seen that at the Γ-point (k=0), the separation between the A1 and B1 valence

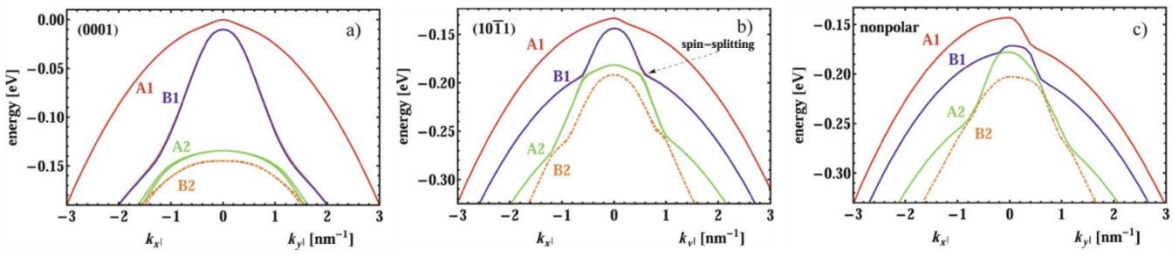

Figure 1.4. Valence band structure for (a) polar *c*-plane, (b) semipolar (10-11) and (c) nonpolar *m*-plane orientations. Copyright © 2011 Wiley-VCH GmbH. Reprinted with permission.

subbands, which are orientated along the a-direction and c-direction, respectively. Since the A1 subband has the closest energy separation to the conduction band, carriers will preferentially collapse into this subband, leading to emission that is largely polarized parallel to the a-direction. In LEDs, the spontaneous emission is approximately 70% polarized along the a-direction, and varies from 20-50% for various semipolar orientations, as can be seen in Figure 1.5 below[20]. The data is collected from the following references[26–29]. This high polarization fraction of spontaneous emission is what allowed for nonpolar VCSEL arrays

with 100% polarization along the a-direction[30], and similar behavior was demonstrated for (20-2-1) VCSELs[6].

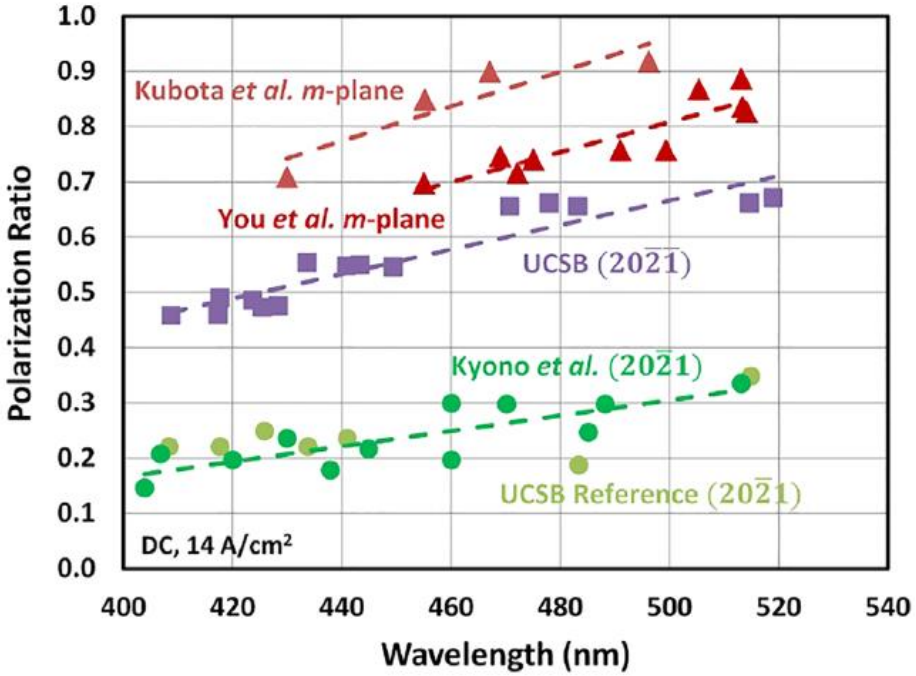

Figure 1.5. Polarization ratio as a function of emission wavelength for various nonpolar and semipolar orientations. Copyright © 2018 Wiley-VCH GmbH. Reprinted with permission.

1.2 VCSEL Applications

VCSELs have found many commercial applications due to their unique characteristics[1]. The VCSELs primary differentiator compared to the EELD is that the laser oscillation as well as the out-coupling of the laser beam occurs in a direction perpendicular to the epitaxial gain region as opposed to parallel to the gain region. This trait has cascading effects on the device design and behavior. First, the length of a VCSEL cavity is significantly smaller, generally micrometer-scale, compared to an EELD which can be millimeter-scale. This translates into a larger longitudinal mode spacing and a smaller overlap between the gain region and resonant electric field. In order to compensate for this, the light has to travel back and forth more times before being coupled out, requiring higher mirror reflectivities. Whereas a typical EELD can

operate with output facets that have a reflectivity of approximately 30%, calculated from the index of refraction contrast between the facet material and air, a VCSEL requires reflectivities exceeding 99%. To achieve this, VCSELs employ top and bottom superlattices of high refractive index contrasting materials. These superlattices are called distributed Bragg reflectors (DBRs) and are used ubiquitously throughout VCSEL industry.

The small size of VCSELs provides other advantages. Due to the small active volume and high mirror reflectivity, VCSELs have significantly lower threshold currents than EELDs, resulting in lower power consumption and reduced heating of the device. Additionally, the use of DBRs eliminates the risk of catastrophic optical damage in the mirrors, which can occur in EELDs when the active region near the facets becomes depleted of carriers and becomes light absorbing. Additionally, the larger longitudinal mode spacing leads to inherently single-mode operation that is well suited for wavelength engineering, including wavelength division multiplexing and tunable VCSEL applications.

The spatial mode properties of VCSELs are also favorable for commercial applications. Due to the circular symmetry of the VCSEL structure, the light is emitted with a circular beam and very low divergence. This results in efficient coupling into optical fibers and allows for relaxed tolerance in alignment. Combined with this ease of integration is the VCSEL's efficient manufacturing process. Because VCSELs are so small, and emit light normal to the substrate, it is straightforward to fabricate very dense 2-dimensional arrays of VCSELs. This allows for effective testing of VCSELs on-wafer, whereas EELDs need to be cleaved or diced in order to be properly characterized. This also allows for VCSELs to either be diced and packaged individually, or packaged as an array, depending on the application.

However, VCSELs have some significant drawbacks compared to EELDs. Due to the small overlap of the gain region with the resonant cavity mode, the mirror reflectivity tolerance is much tighter than for EELDs. A change in even 1% on either mirror reflectivity will significantly hurt VCSEL performance, if the device can lase at all. Additionally, for cavities with a large mode spacing, any deviation in the epitaxial growth will shift the resonant mode wavelength. Typical GaN VCSEL gain regions are on the order of 10-20nm full-width half-max (FWHM), so the margin for error is small. Additionally, while the circular spatial mode is desired for VCSEL applications, VCSELs have a strong tendency to operate in higher order spatial modes. This issue is exacerbated by current crowding, which can occur when the series resistance across the current confinement region is non-uniform, leading to an increase in current injection along the edge of the device. It is also exacerbated by larger apertures, which inject current into the larger higher order spatial modes.

The longitudinal and spatial mode behavior of VCSELs is incredibly sensitive to the structural and epitaxial design. A small change in the refractive index profile or epitaxial growth can have an outsized impact on device performance. Controlling every aspect of the VCSEL fabrication process is critical for realizing high power, single mode VCSELs.

1.2.1 Current Commercial III-V VCSEL Applications

The VCSEL was first proposed in 1979 by Iga et. al[31], and first commercialized by Honeywell in 1988. The most mature market for VCSELs uses NIR GaAs VCSELs as transceivers for data communication through optical fibers, taking full advantage of the high modulation speeds and single mode operation offered by VCSEL platforms. NIR VCSELs have achieved impressive speeds with data transfer rates ranging from 20 Gb/s to 40 Gb/s for

VCSELs emitting from 980nm to 1100nm[32,33]. Most of today's commercial datacom components are based on VCSELs that are either individually packaged or packaged in parallel 2- to 16-channel fiber modules[34]. Modules with 850nm VCSELs are commonly employed in short range <400m transmission schemes, finding use in data centers, office buildings, campuses, and more. Long-haul options utilizing longer wavelength VCSELs with transmission ranges up to 80km, are also available. VCSEL revenues for datacom applications are expected to reach $2.1 billion USD by 2027, and comprise approximately 50% of total VCSEL market revenues[35].

Another rapidly growing market for VCSELs is 3D depth sensing. Within the consumer electronics space, smartphones are the growth leader, with Apple as the lead player. Since the release of the iPhone X, all subsequent iPhones have integrated VCSEL technology into their phones to provide facial recognition capabilities to users. The system creates a 3D depth map of the primary phone user's face using an IR VCSEL which supplies IR light to an active diffractive optical element that splits the VCSEL beam into 30,000 dots for high resolution[36]. This process offers a 20x improvement to identification accuracy relative to the conventional fingerprint-based ID system, with a less than one in one million chance of a false positive ID. Aside from facial recognition, VCSELs are prominently used in a variety of consumer products, including as the positional tracking component in optical mice, the writer in laser printing, and for security recognition when making mobile payments. In total, the mobile and consumer electronics market enabled by VCSELs is expected to drive $1.9 billion in revenue, approximately 48% of the market.

Aside from facial recognition, optical coherence tomography, which enables 3D imaging of biological tissues and materials, is an emerging market for VCSELs[37]. For retinal scanning,

the current dominant technology is a wavelength tunable IR or NIR VCSEL. The emission wavelength is continuously tuned via a microelectromechanical system (MEMS) comprised of a DBR suspended to create an air gap over an epitaxial layer stack; the cavity length of the air gap is tuned by electrostatic actuation of the top DBR. Tunable MEMS VCSELs have achieved continuous tuning ranges of 150nm for a VCSEL emitting at 1310nm, and 65nm for

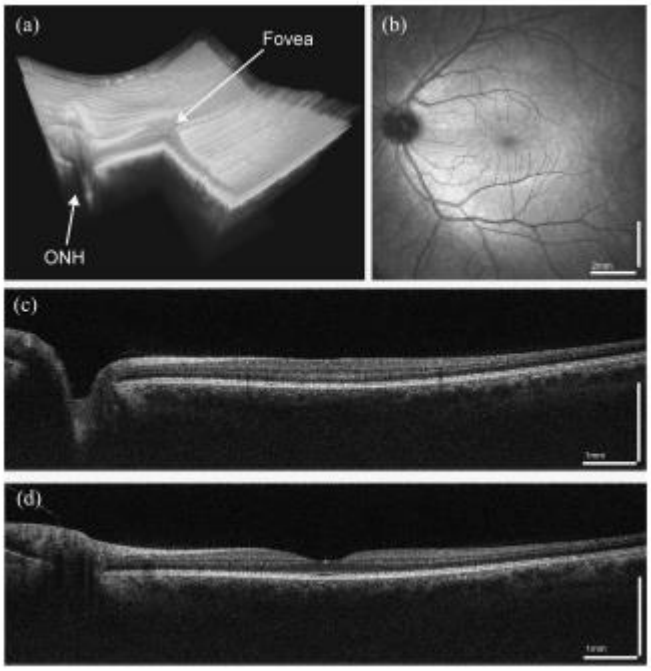

Figure 1.6. (a) Wide field 3-dimensional rendering of human retina data obtained with a tunable MEMS VCSEL source. (b) OCT Fundus image. (c) Wide field OCT cross sectional image intersecting the optic nerve head. (d) Wide field OCT cross sectional image intersecting the fovea. Copyright © 2015 IEEE. Reproduced with permission.

a VCSEL emitting at 1050nm[38,39]. Swept source OCT enables high contrast imaging to visualize and quantify blood circulation in tissue. This has found widespread application in optometry for diagnosis and study of retinal issues. Figure 1.6 shows a wide field 3D rendering of human retina data obtained with an early prototype tunable VCSEL source. Currently, the market revenues for medical technologies are approximately $5 million globally, with the amount expected to grow at a modest rate of 5.5% CAGR through 2030. However, with recent reports and spotlights from government agencies around the world on the trend of increasingly

poor eyesight in school-age children and young adults, VCSELs are poised to play an expanding role in the medical industry[40,41].

One final emerging application for VCSELs is in automotive sensing. The National Highway Traffic Safety Administration provides a framework for the 6 Levels of Automation, which are summarized in Table 1.1 below[42].

Table 1.1. Levels of vehicle automation as defined by the National Highway Traffic Safety Administration.

Level	Criteria	Examples
0	Driver fully attentive, assisted with warnings and notifications, no automated operation of any vehicle function	Lane departure or forward collision warning sensors
1	Driver fully attentive, assistance provided with either acceleration/braking OR steering	Adaptive cruise control, lane assistance
2	Driver fully attentive, assistance with acceleration/braking AND steering	Highway piloting
3	Driver available but not fully attentive to vehicle, all aspects of driving automated	Automation with prompts for driver participation during unexpected scenarios
4	Passenger only, all aspects of driving fully automated but within limited service area	Full automation but only within defined area
5	Passenger only, all aspects of driving fully automated with no restriction to service area	Automated travel available anywhere

Consumer demand for autonomous and semi-autonomous vehicles is increasing. However, all vehicles sold commercially in the United States today fall in Automation Levels 0-2. In order for a vehicle to achieve Level 5 automation, the computing system responsible for navigation will require a complex suite of sensors to manage every conceivable roadway scenario. Most sensing platforms utilize a mix of optical cameras and light detection and ranging (LIDAR) to inform the central operating system of its surroundings. VCSELs are well-suited for LIDAR systems due to their ability to generate 3D images, low power consumption, and narrow linewidth emission output. Additionally, the small form factor and mass producibility of

VCSEL arrays makes them a cost and weight effective solution for the consumer-oriented automotive industry. While current VCSEL revenues from the automotive industry are only $2 million, the sector is expected to grow the fastest of all sectors at an expected CAGR of 97%, with expected revenue exceeding $100 million by 2030.

1.2.2 GaN-Based VCSEL Applications

The current VCSEL market is primarily limited to red and IR emission due to the commercial availability of AlGaAs/GaAs- and InAlGaAs/InP-based VCSELs. However, GaN-based VCSELs share many of the same intrinsic properties of these more mature materials platforms, while offering a range of visible and near-UV emission wavelengths. The primary sectors for immediate GaN VCSELs include transceivers, sensors, medical imaging, and display technology.

Recently, visible light communications (VLC) has gained some interest in industry and academia[43]. VLC works by transmitting data optically via visible wavelengths, in a fashion comparable to existing IR VCSELs for datacom. However, visible light is attenuated by existing optic fiber infrastructure, and so the envisioned application would be for short distance communication, generally through free space within office buildings or to enable car-to-car or car-to-infrastructure communication. The main benefits of VLC are that the maximum theoretical data speed is higher due to the higher frequency of emitted light, and that the light is strongly attenuated by physical objects such as walls, increasing security for transmitted data. Furthermore, the existing bandwidth for traditional communications is incredibly crowded, with the issue becoming worse with the explosive growth of the IoT sector. However, this method comes with significant tradeoffs. For one, the maximum

permissible exposure (MPE) to be considered eye safe is significantly lower in the visible region, <1μJ/cm^2 for a 1μs pulse[44,45]. Compare this to a 1550nm laser, which has a MPE 1 million times higher at 1J/cm^2, and VLC appears to have an insurmountable safety disadvantage. However, this framing is somewhat disingenuous, as commercial LIDAR systems employ both 1550nm lasers and 905nm lasers, and the MPE of 905nm lasers are within an order of magnitude to the visible spectrum. All this is to say that VLC may provide a complement to existing optical datacom technologies.

So far, VLC demonstrations have utilized both LED and microLED devices and arrays, demonstrating up to 10Gb/s data rates for a 3 x 3 array of 20μm microLEDs[46]. However, the modulation bandwidth of LEDs is limited (2GHz for a single LED) compared to laser diodes due to longer carrier lifetimes. GaN EELD demonstrations have reached transmission rates of 4 Gb/s through direct modulation of a single laser diode[47].The benefits of the EELD are a reduction in carrier lifetimes compared to the LED. Since the modulation bandwidth is inversely proportional to the active region volume, GaN VCSELs have the potential to yield even higher modulation bandwidths than EELDs[48].

Beyond applications in VLC, GaN VCSELs integrated into a Doppler interferometry system could enable novel metrology applications. In this application, the shorter visible wavelength emission would allow for improved surface mapping and quality control analysis for semiconductor and biological material production lines. Additionally, the inherently polarized nature of nonpolar VCSEL arrays make GaN VCSELs well suited to Doppler interferometry applications which require a stable polarization state.

One exciting application for GaN VCSELs is in OCT systems for retinal imaging. While current OCT technologies were built on the pre-existing NIR VCSEL technology from

datacom, there are a number of medical issues that would directly benefit from a shorter wavelength laser source. For example, visible OCT enables higher axial resolution with a similar spectral bandwidth, a stronger back-scattered signal, and a higher lateral resolution[49]. For example, the optical reflectance of the retinal nerve fiber layer characteristic of glaucoma is more sharply reduced at short wavelengths (<560nm) compared to longer NIR wavelengths, providing increased spectral contrast and enabling earlier detection and treatment of glaucoma[50]. Generally, this increase in resolution comes with the tradeoff of increased absorption of light by biological tissue, compromising depth of penetration.

Arguably the most exciting application for GaN VCSELs from an industry standpoint is in display technologies like projectors and AR/VR. With current technologies, this would involve pairing blue and green GaN-based VCSELs with red AlGaInP-based VCSELs. The low threshold currents and power consumption make them a good fit for portable battery-powered devices, which could include laser pico-projectors and augmented reality headsets, potentially adopting a form factor similar to Google Glass, Meta Oculus, or Apple Vision Pro. The coherent, highly directional, and circular beam profile with low divergence of VCSELs makes them excellent candidates for displays and projectors utilizing diffractive optics technology. This characteristic is particularly advantageous for augmented reality headsets and heads-up displays.

1.3 GaN VCSEL Design

This section summarizes the results from the GaN VCSEL field from their first inception in 2008 until present. The design challenges facing GaN VCSELs are discussed in section 1.3.1. Specific aspects of GaN VCSEL design are discussed in section 1.3.2 onwards.

VCSELs share many of the same design goals as EELDs, such as minimizing the threshold current density and maximizing the output power. However, the significantly different device geometries, including vertical light emission and shorter cavity lengths, lead to some specific design considerations. A general schematic of a VCSEL is shown in Figure 1.7.

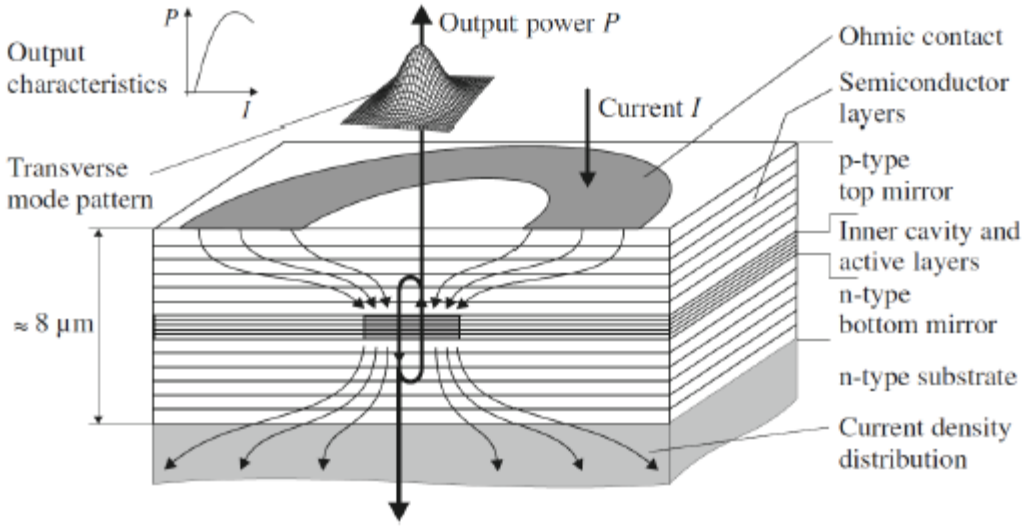

Figure 1.7. Schematic illustration and operating principle of a VCSEL.1 Reprinted by permission from [Michalzik, R. (2013). *VCSELs: Fundamentals, Technology and Applications of Vertical-Cavity Surface-Emitting Lasers* (1st ed.). Heidelberg: Springer. https://doi.org/10.1007/978-3-642-24986-0]. © Springer-Verlag Berlin Heidelberg 2013.

In an EELD, the optical cavity is arranged parallel to the active region, leading to a high overlap between the electric field and gain region. However, for VCSELs, the optical cavity is perpendicular to the gain region, leading a low overlap between the optical cavity and gain on the order of 1%[1]. Additionally, EELDs have cavity lengths on the order of ~1mm and threshold currents on the order of 100's of mA, while VCSELs have cavity lengths on the order of ~1-10µm and threshold currents on the order of 1-10mA.

The first electrically-injected GaN VCSEL was demonstrated simultaneously by two different research groups from National Chiao Tung University (NCTU)[4] and Nichia Corporation[3] in 2008. Since then, multiple research groups have achieved room temperature

CW operation of GaN VCSELs on a variety of different basal orientations, with wavelengths ranging from near UV into the green[7,51]. The threshold current densities of devices has ranged from 0.7kA/cm^2 to 141kA/cm^2[13,52], with peak powers ranging from 3μW up to 23.7mW[53,54]. While initial VCSELs were demonstrated on GaN-on-sapphire substrates, bulk GaN substrates have been increasingly utilized due to their improved thermal performance, higher output powers, and longer device lifetimes[55].

In general, GaN VCSELs struggle with self-heating due to higher input power requirements and high optical losses from p-GaN and current spreaders[8], as well as poor heatsinking due to the typically low thermal conductivities of the bottomside DBRs[56]. These issues result in lower thermal rollover and lower device lifetimes compared to GaAs-based VCSELs. Because of these issues, a variety of different device architectures have been demonstrated, all with the hope of addressing the issues presented. The discussion will start with the challenge in fabricating the bottomside DBR. Next, we will discuss the challenge of dealing with the low conductivity of p-GaN, and the various current spreading techniques employed. Following this, we will discuss mode control, and the challenges of mode control for GaN VCSELs. Finally, we will discuss the advantages of extending the cavity length for GaN VCSELs and describe our design goals for this thesis.

1.3.1 DBR Mirror Design

In order to emit vertically, VCSELs require top and bottom mirror that are parallel to the substrate. Due to the low overlap between the optical cavity and gain region, mirrors need to have a reflectivity >99% in order to ensure the mirror loss doesn't overcome the available cavity gain. This is accomplished using a distributed Bragg reflector (DBR), which consists

of several periods of quarter-wavelength (λ/4) alternating layers of high and low refractive index. The index contrast between the two layers, Δn, determines both the max reflectivity as well as the reflectance stopband of the DBR mirror. The peak reflectivity can be calculated using,

$$R = \left[\frac{1-\left(\frac{n_L}{n_H}\right)^{2m}}{1+\left(\frac{n_L}{n_H}\right)^{2m}}\right]^2 \tag{1.4}$$

where n_L and n_H are the refractive indices of the materials with lower and higher indices, respectively, and *m* is the number of layer pairs. The stopband width of a DBR mirror can be estimated as,

$$\Delta\lambda_{max} = \frac{4\lambda}{\pi} sin^{-1}\left(\frac{n_H - n_L}{n_H + n_L}\right) \tag{1.5}$$

where $\Delta\lambda_{max}$ is the full-width half-maximum (FWHM) of the reflectance of a DBR mirror with infinite layer pairs. Note that this is an upper bound, and the real stopband will be reduced due to index dispersion and having a finite number of mirror periods.

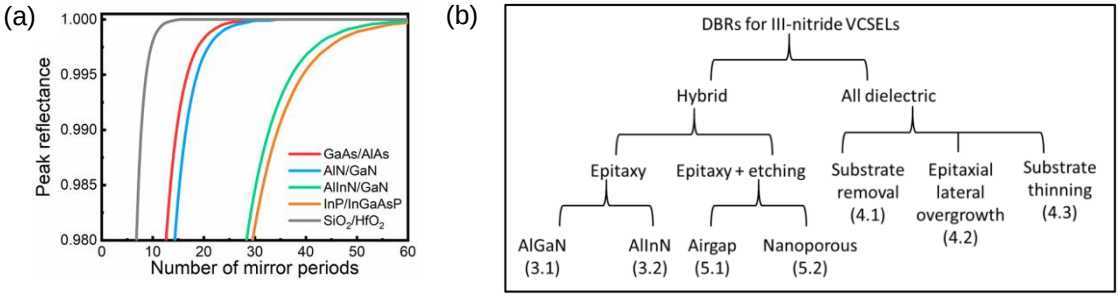

Figure 1.8. (a) Peak mirror reflectance, R, versus number of periods for SiO_2/HfO_2 (dielectric), AlAs/GaAs, InP/InGaAsP, AlN/GaN, and AlInN/GaN DBRs. (b) Chart depicting different approaches to incorporating the bottomside DBR into III-nitride VCSELs. Reprinted from [Zhang C. et al, (2019) Distributed Bragg Reflectors for GaN-Based Vertical-Cavity Surface-Emitting Lasers, Applied Sciences 9(8), 1593] under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/).

In the GaAs material system, there are several viable options for a bottomside DBR. One popular option is the AlAs/GaAs DBR, which provides a decent lattice contrast (Δn~0.5) and

is thermally and electrically conductive[57]. Not only does this DBR have favorable material characteristics, but it can also be grown in-situ with the rest of the epitaxial layers, allowing for precise monitoring of the cavity length using a laser monitor. Unfortunately, within the GaN material system there is not an equivalent epitaxial DBR option due to an unfavorably high lattice mismatch between AlN and GaN. This has posed a serious challenge to GaN VCSEL development, and a variety of different device structures have been demonstrated, roughly split into hybrid epitaxial designs and dual dielectric DBR designs. The demonstrated options have been summarized in Figure 1.8 (b)[56]. To date, the most promising device performances have been achieved with AlInN DBRs, and dual dielectric DBRs deposited via substrate thinning, so the next section will outline the device characteristics achieved for these DBR methods. Additionally, since this thesis pursued a nanoporous DBR, and the NP DBR is a relatively recent GaN DBR option, the final section will examine them. The general takeaway from this section is that while the epitaxial DBR configuration is clearly preferable within the mature IR VCSEL industry, the choice of bottomside DBR for GaN VCSELs remains a debatable subject and each option has significant tradeoffs amongst optical properties, thermal and electrical transport, and manufacturability.

1.3.1.1 Dual Dielectric DBR

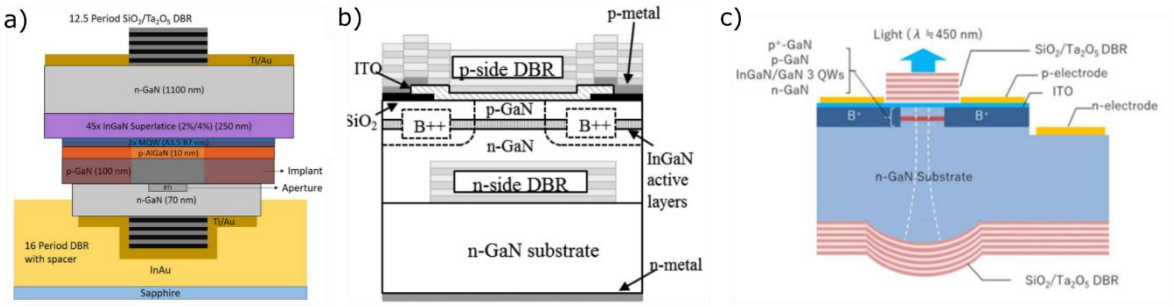

Figure 1.9. Device schematics for dual dielectric DBR VCSELs fabricated via (a) flip chip bonding with a photoelectrochemical etch, (b) epitaxial lateral overgrowth, and (c) chemical-mechanical polishing with a curved backside mirror. (a) Copyright © 2019 Wiley-VCH GmbH. (b) Copyright © 2016 Wiley-VCH GmbH. (c) [K. Hayashi et al, IEEE Photonics Journal **14**(4), 1–5 (2022).] Reprinted under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/).

The dual dielectric DBR structure has been a popular architecture due to the high index of refraction contrast between available dielectrics, including SiO_2, ZrO_2, HfO_2, and Ta_2O_5, as well as the ability to deposit lower stress films for visible light reflection due to the thinner layer thickness requirements. While this DBR configuration avoids any of the substantial growth difficulties associated with the epitaxial DBR options, the placement of the dielectric DBR on the bottomside generally necessitates flip chip bonding and substrate removal. A number of techniques for substrate removal of GaN VCSELs have been shown, including chemical-mechanical polishing (CMP)[10,58], photoelectrochemical etching (PEC)[5,6,30], and laser lift off[3]. There has been limited research efforts into epitaxial lateral overgrowth[59]. Figure 1.9 shows an overview of the device schematics for GaN VCSELs with (a) dual dielectric DBRs fabricated via flip chip bonding and photoelectrochemical etching[60], epitaxial lateral overgrowth[59], and CMP polishing without flip chip bonding[61].

One of the original VCSEL designs used a flip-chip architecture, where the sapphire substrate was removed with laser liftoff (LLO) followed by CMP to attain the desired cavity thickness. In this method, the device is partially processed and a topside dielectric DBR is

deposited before bonding to a handling wafer. One distinct downside of using CMP for substrate removal is the issue with thickness uniformity and cavity length control[55]. Due to this, a majority of subsequent flip chip architectures have utilized photoelectrochemical etching (PEC), in which the flipped device is removed from its native substrate when light photo-excites a chemical reaction (typically oxidation) between a sacrificial layer (typically a QW) and a suitable electrolyte (typically KOH). The biggest drawback of the PEC etch is that, on c-plane, the etch surface is highly roughened due to the presence of built-in polarization fields, as well as highly different etch rates between different crystal facets[62]. Since a majority of groups worldwide are pursuing GaN VCSELs on c-plane, this has limited its use outside of academic groups focused on non-basal orientations. Up until 2020, this was the dominant VCSEL fabrication method utilized at UCSB, with VCSELs demonstrated on both *m*-plane[5,7,63] and semipolar (20-2-1)[6,60] orientations.

Epitaxial lateral overgrowth (ELO) was utilized by Sony Corporation in 2015 to fabricate dual dielectric DBR VCSELs without needing substrate removal[59]. The ELO growth consisted of GaN growth around a dielectric DBR deposited onto a GaN template, resulting in a dielectric DBR buried beneath epitaxial material. Unfortunately, the drawbacks of this technique were that the resulting cavity had a high cavity thickness of 5-10μm, leading to increased diffraction loss. Additionally, the high MOCVD growth temperatures (600-1100°C) led to significant thermal stresses in the deposited dielectric film during epitaxial growth, causing cracking and reducing yield.

One final technique that has also been developed by Sony Corporation uses CMP to remove a majority of the substrate, resulting in a VCSEL cavity of roughly 20μm, followed by deposition of the dielectric DBR on a curved GaN lens etched into the thinned backside[13].

The curved lens minimizes the diffraction loss that would otherwise occur for large cavities, as well as offering tunability of optical confinement. The long cavity length provides significant thermal benefits, solving one of the biggest drawbacks to the dual dielectric DBR design. This method will be discussed in more detail in Section 1.3.4.

A representative summary of VCSEL devices utilizing a dual dielectric DBR are shown in Table 1.2 below. In the case where both pulsed and CW performance were reported, only the CW performance is included, and for results which report multiple CW VCSELs, only the highest output power VCSEL is included. The results are arranged by structure, and chronologically within each structure. For some structures, the thermal impedance values were taken from ref[64], which simulated the structures. The values are noted with the relevant citation. Generally, it can be seen that flip-chip VCSEL designs have struggled to lase under CW operation, which is largely attributed to the high thermal impedance from the bottom dielectric DBR (thermal conductivity <1 K/W[7]). It can also be seen that, for the dual dielectric DBR, the CMP/lens method offers excellent output powers and robust CW operation, attributed to the longer cavity lengths. While initial LLO VCSELs lased CW (in fact the first VCSEL demonstration in 2008 was LLO!), the technique was largely abandoned as the field transitioned from sapphire substrates to absorbing bulk GaN substrates.

Table 1.2. Summary of GaN VCSELs with dual dielectric DBRs.

Structure	**Orient.**	**Operation**	**Aperture (μm)**	**Cavity (μm)**	**λ (nm)**	**J_{th} (kA/cm^2)**	**P_{out} (mW)**	**R_{th} (K/W)**
PEC[65]	*m*-plane	Pulsed	10	1.2	412	90	0.02	6800[64]
PEC[66]	*m*-plane	Pulsed	12	1.1	417	3.5	0.55	4600[64]
PEC[67]	*m*-plane	Pulsed	12	1.1	417	22	0.18	
PEC[5]	*m*-plane	Pulsed	10	1.1	406	16	0.01	
PEC[68]	*m*-plane	Pulsed	10	1	408	10	0.32	
PEC[7]	*m*-plane	CW	6	3.8	420	40	0.14	
PEC[63]	*m*-plane	CW	8	1	430	10	0.72	
PEC[6]	(20-2-1)	Pulsed	12	1.1	445	4.6	1.85	1400
PEC[60]	(20-2-1)	CW	12	1.1	451	2.4	0.25	1150
ELO[59]	*c*-plane	CW	8	4.5	453	35.8	1.1	2900[64]
LLO/CMP[3]	*c*-plane	CW	8	1	414	13.9	0.15	4100[64]
LLO[69]	*c*-plane	Pulsed	10	1	414	8.9	0.02	710
CMP[70]	*c*-plane	CW	10	2.6	560	0.8	0.01	915
CMP[55]	*c*-plane	CW	8	1	410	16	0.6	
CMP[71]	*c*-plane	CW	7	0.88	525	0.051		842
CMP lens[13]	*c*-plane	Pulsed	8	25	454	141		
CMP lens[72]	*c*-plane	CW	3	20	445	3.5	0.3	
CMP lens[9]	*c*-plane	CW	8	20	443	7.95	15	
CMP lens[73]	*c*-plane	CW	4	20	443	13.5	2.5	
CMP lens[74]	*c*-plane	CW	4	20	515	14.4	0.08	

1.3.1.2 AlInN/GaN DBR

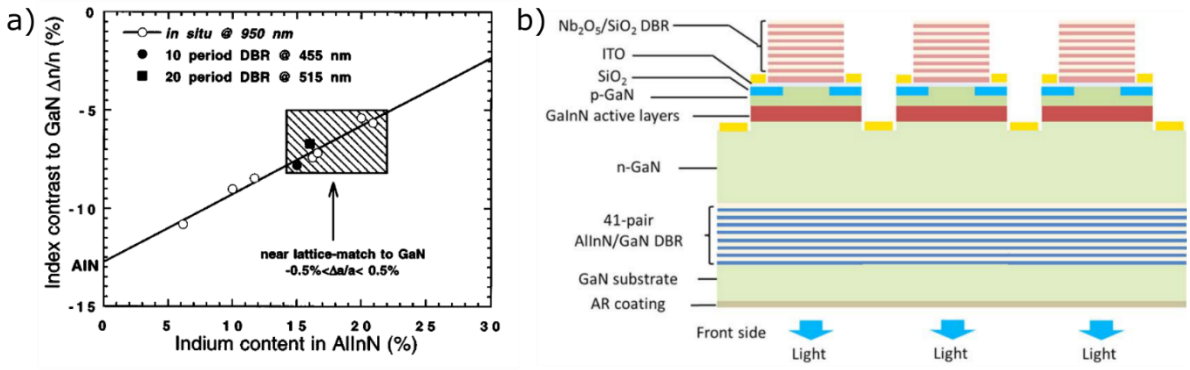

Figure 1.10. (a) AlInN/GaN refractive index contrast versus AlInN indium content, calculated from in situ reflectivity measurements (950nm wavelength) and from ex situ analysis of shorter wavelength DBRs (455nm and 515nm). The shaded square shows the approximate growth window for lattice matching to GaN, where the extent of the window denotes +/- 0.5% lattice mismatch. (b) Schematic of VCSEL array with AlInN/GaN DBRs. (a) Copyright © 2003 AIP Publishing. (b) Copyright © 2019 IOP Publishing [Masaru Kuramoto et al 2019 Appl. Phys. Express 12 091004] Reprinted with permission under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/).

The ternary $Al_{0.80}In_{0.20}N$ alloy has been gaining increasing research interest for GaN VCSELs due to its ability to completely lattice match to GaN[75] while introducing an index contrast of ~0.2 with GaN[76,77]. AlInN/GaN DBRs were first demonstrated in 2003[76], but due to the slow growth rate (~200nm/hr) and low index contrast, growth of a >99% reflective DBR took prohibitively long. The primary challenges with growing AlInN are due to the large mismatch between InN and AlN covalent bonds, vast differences in the optimal growth temperature between InN (600ºC) and AlN (>1100ºC) via MOCVD, and the narrow growth window to achieve lattice matching, seen in Figure 1.10 (a)[76]. A schematic of a recent GaN VCSEL with an AlInN/GaN DBR is shown in Figure 1.10 (b)[78]. The first GaN VCSEL with a bottom 41.5-period AlInN/GaN DBR was demonstrated in 2012 by École Polytechnique Fédérale de Lausanne (EPFL). Since then, continued development on GaN VCSELs with AlInN/GaN DBRs has been primarily performed by Meijo University in conjunction with Stanley Electric Corporation[79–81], as well as by Nichia Corporation[51,78]. In 2015, Otto-von-

Guericke-Universität Magdeburg identified a new growth window using a two-temperature growth procedure that allowed for a much higher growth rate (>500nm/hr)[82]. Recently, Meijo University and Otto-von-Guericke-Universität Magdeburg both demonstrated electrically conductive AlInN/GaN DBRs with vertical specific resistances as low as $5x10^{-4}$ Ωcm^2 through the DBR[83,84]. Perhaps most promising, it was also recently shown that the AlInN/GaN DBR can be used to provide in-situ feedback on epitaxial growth, providing a 0.5% growth rate accuracy[85]. These recent demonstrations show that AlInN/GaN DBRs have the potential to provide the epitaxial DBR solution that has been sorely missing from GaN VCSEL development.

The challenges with the AlInN/GaN DBR are considerable. First, the growth of AlInN is incredibly challenging, with a narrow growth window, low growth rates, and general difficulty maintaining control over the requisite 4:1 Al:In ratio for lattice-matching. This issue is compounded by AlInN's low index contrast with GaN, requiring 40-60 periods of AlInN/GaN, depending on the desired reflectivity. This represents a total thickness of roughly 4 - 6μm, depending on the number of periods and the desired wavelength, and almost 1 full day of growth even under the faster growth condition. The narrow stopband of the DBR also limits its utility in certain applications such as tunable VCSELs which need a suitably wide tuning range[86]. Finally, the thermal conductivity of AlInN is quite low, on the order of 5 W/mK[87], limiting its use in short cavity VCSEL structures[88].

A summary of VCSEL devices utilizing a bottom AlInN/GaN DBR are shown in Table 1.3 below, organized similarly as Table 1.2 above. Note that all demonstrations have been on c-plane, and without any substrate removal. As of writing, AlInN/GaN DBR GaN VCSELs hold the world record for CW output power, 23.7mW,[81] and peak wall-plug efficiency (WPE),

18.5%[51]. A 16 x 16 VCSEL array with bottom AlInN/GaN DBRs was achieved that had a total output power above 1W[80]. Finally, a lifetime study was performed on the highest efficiency GaN VCSELs to date and found stable CW operation above 1mW for 1000 hours[51].

Table 1.3. Summary of GaN VCSEL demonstrations utilizing a bottom epitaxial AlInN/GaN DBR.

Institution	Operation	Aperture (μm)	Cavity (μm)	λ (nm)	J_{th} (kA/cm^2)	P_{out} (mW)	R_{th} (K/W)
EPFL[89]	Pulsed	8	1.3	420	140	0.3	
Meijo[54]	CW	8	1.9	445	8.92	15.7	710
Meijo[90]	CW	8	0.85	441	6	6	
Meijo[91]	CW	8	1.9	441	6	15.7	
Meijo[88]	CW	8	0.75	445	14	1.8	2700
Meijo[79]	CW	8	1.9	442	15.9	15.7	
Meijo[81]	CW	7	1.9	450	21	23.7	
Meijo[92]	CW	10	0.9	411	18.3	2	
Nichia[78]	CW	4	0.85	442	3.2	3	
Nichia[78]	CW	5	1	515	14.3	1.5	
Nichia[51]	CW	5		445.9	9.7	12	

1.3.1.3 Nanoporous GaN DBR

The formation of nanoporous (NP) GaN DBRs will be described in greater detail in Section 2.3, and this section will mainly focus on previous VCSEL work.

The NP DBR is a recent epitaxial DBR option that has shown promise for GaN VCSELs[93]. Using a simple electrochemical cell, pores are formed by injecting holes into the surface layer of heavily doped n-GaN in order to oxidize the material. The resulting porous GaN structure has a refractive index that can be calculated using the volume average theory[94],

$$n_{por} \approx \sqrt{(1-\varphi)n_{GaN}^2 + \varphi n_{air}^2} \tag{1.6}$$

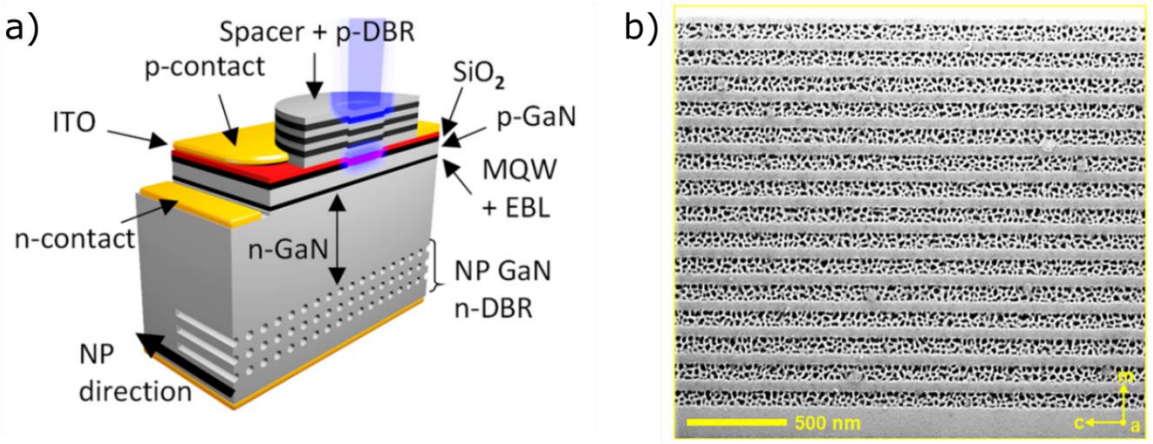

Figure 1.11. (a) Device schematics of a VCSEL with a top dielectric DBR VCSELs and bottom NP GaN DBR. (b) Cross-sectional SEM image of a 15-period *m*-plane GaN NP DBR. (a) Reprinted with permission from [R.T. Elafandy, J.-H. Kang, C. Mi, T.K. Kim, J.S. Kwak, and J. Han, "Study and Application of Birefringent Nanoporous GaN in the Polarization Control of Blue Vertical-Cavity Surface-Emitting Lasers," ACS Photonics 8(4), 1041–1047 (2021)]. Copyright © 2021 American Chemical Society. (b) Copyright © 2018 AIP Publishing. Reprinted with permission.

where φ is the ratio of air to GaN (porosity). By forming a superlattice of undoped or low-doped n-Gan and heavily doped n-GaN, a high reflectivity DBR can be formed. An example of this can be seen in Figure 1.11. The main advantage of the NP DBR is that the attainable index contrast is quite high, theoretically up to 1.5 for an airgap/GaN DBR[95]. Additionally, the epitaxy of undoped GaN/n+-GaN superlattices is quite straightforward, with growth times on the order of 1hr or less for a >99.9% reflective DBR structure that imposes negligible degradation on device epitaxial microstructure or morphology. The tunability of the porosity led to impressive early demonstrations of NP DBRs spanning the visible spectrum with stopbands ranging from 50nm at 450nm to almost 100nm at 650nm[96].

However, there are significant tradeoffs with the NP DBR. First, the thermal conductivity of the porous layers is low, with a 10% porous layer exhibiting a near 80% reduction in thermal conductivity when compared to un-porosified GaN[97]. For porosities exceeding 40%, a porosity which provides an index contrast of 0.43 at 450nm, the thermal conductivity of the

NP DBRs is comparable to a dielectric DBR. The significant thermal barrier posed by the NP DBR prevented CW lasing until 2023.

The first VCSEL with a NP DBR was demonstrated in 2019 on *m*-plane via optical pumping[98]. They observed that when they tuned the porosity too high, individual nanopores would collapse into each other and create larger macro voids. They observed that these voids created local variations in porosity which led to local variations in the effective cavity length. When the pump laser was pointed at these regions, multiple lasing peaks would appear, correlated to the different regions. Since then, this issue hasn't been reported again, but it highlights the necessity for pore control.

Since 2019, several electrically injected VCSELs were demonstrated. In 2020, Yale University succeeded in making a GaN VCSEL that was electrically injected through the NP DBR[99]. Injecting through the NP DBR led to a slight increase in the turn-on voltage (0.4V) and differential resistance (4Ω). They also showed that their NP DBR etch condition was highly uniform, with a <2nm shift in the stopband center wavelength across a 2-in wafer.

Perhaps the most compelling demonstration to date came in 2021, when Yale University showed that by taking advantage of the birefringence of the porous DBR layers, they were able to fabricate GaN VCSEL arrays on c-plane that were polarization pinned parallel to the pore direction[100]. They showed a maximum polarization suppression ratio (OPSR) of 17dB and 13dB along the [1-120] and [1-100] directions for a DBR porosity of 47%, respectively, and they expect this to increase with increased porosity. This is probably the strongest advantage of the NP DBR, as it enables a crucial feature that was thought to only be accessible via processing on non-basal orientations. The importance of this finding underscores the need

for a NP DBR VCSEL structure that can balance the high thermal impedance of the DBR layers.

A summary of VCSEL devices utilizing a bottom NP DBR is shown in Table 1.4 below. Note that there has only been one CW demonstration in the field, and the device experienced rollover at a current density of ~3.5kA/cm^2. However, the limited performance demonstrated thus far is largely a symptom of the NP DBR's time in the field, and the work being done shows great promise for future applications in GaN VCSELs. Excitingly, a startup company was recently founded with the goal of commercializing GaN VCSELs, and their bottom DBR of choice is the NP DBR[101].

Table 1.4. Summary of GaN VCSELs with a bottom epitaxial nanoporous DBR.

Institution	**Orient.**	**Operation**	**Aperture (μm)**	**Cavity (μm)**	**λ (nm)**	**J_{th} (kA/cm^2)**	**P_{out} (mW)**	**R_{th} (K/W)**
UNM[102]	*m*-plane	Pulsed	20	1.5	409	20	1.6	
Yale[99]	c-plane	Pulsed	15	1.1	434	42	0.18	
Yale[100]	c-plane	Pulsed	15	1.1	433	59		
Yale[52]	c-plane	CW	6	0.2	437	0.7		

In summary, the choice of bottom DBR has a large impact on the epitaxy, fabrication complexity, thermal impedance, and peak reflectivity of the emission or non-emission DBR. There are substantial tradeoffs with each DBR option. Figure 1.12 summarizes the refractive index contrast Δn, electrical conductivity (S/m), and thermal conductivity (W/m K) for AlInN/GaN, NP-GaN/GaN, and dielectric Ta_2O_5/SiO_2 DBRs. While there are valid reasons to

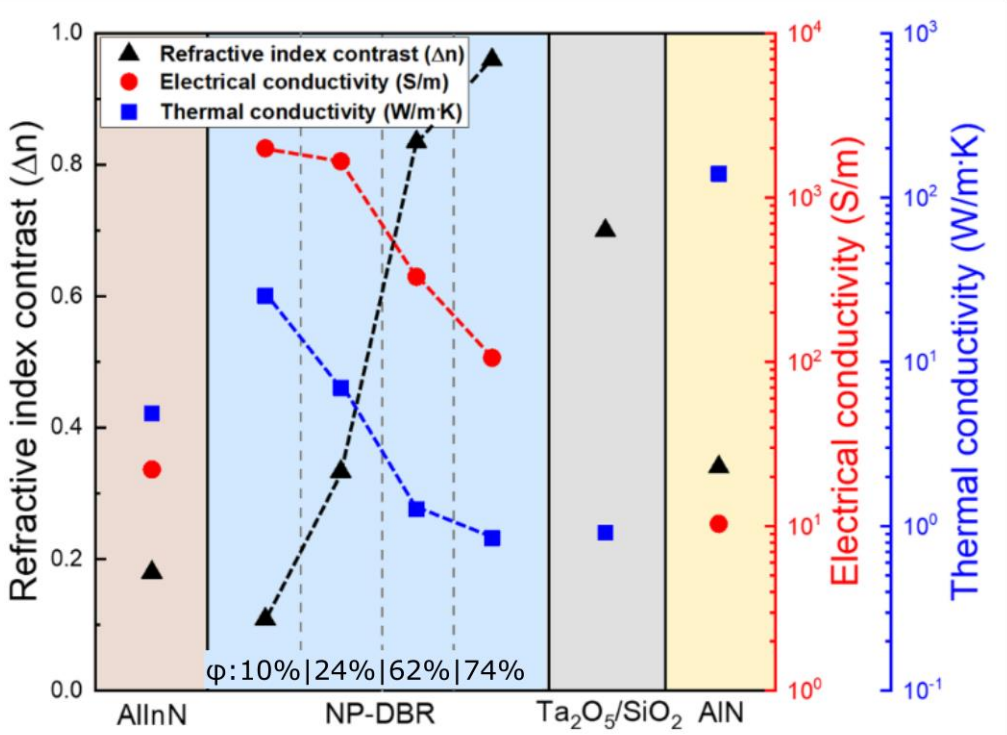

Figure 1.12. A parameter plot for NP GaN in comparison with other materials. Copyright © 2019 AIP Publishing. Reprinted with permission.

choose each DBR, for our devices we determined that the NP DBR offered the most in terms of ease of fabrication and DBR performance. It allowed us to achieve a higher index contrast than AlInN using a simpler fabrication process than the dielectric DBR. It also gave us an epitaxial solution that was significantly easier to control than the AlInN DBR. So, we chose to integrate this DBR into our device process. The development of the NP DBR is covered in Section 2.3.

1.3.2 Current Confinement

Lateral current confinement is an important factor to enable efficient laser operation of VCSELs with a low threshold voltage and enable uniform current spreading across the aperture. Often, the choice of current confinement also has ramifications on optical confinement. The goal of the current confining layer is to control the injection of current to

provide optimal overlap between the current and light confining regions of the device. In general, smaller diameter apertures enable single spatial mode operation due to the increased scattering loss experienced by wider spatial modes. By contrast, larger diameter apertures enable higher output powers and improved thermal performance, but suffer from current crowding around the edge of the aperture[103]. Current crowding is exacerbated by the low electrical conductivity of p-GaN, which prevents lateral current injection from the exterior metal contacts to the aperture. Because of this, a variety of current spreader techniques have been employed to address this issue. In this section, the primary current confinement apertures that have been used in GaN VCSELs will be presented. First, the various options for n-side current spreading will be discussed. Next, the different current aperture designs will be discussed, organized based on the impact of the aperture structure on the normalized effective index contrast ($\Delta n_{eff}/n_{cavity}=(n_{cavity}-n_{peripheral})/n_{cavity}$) between the cavity and exterior region: concave ($\Delta n_{eff}/n_{cavity} < 0$), planar ($\Delta n_{eff}/n_{cavity} \sim 0$), and convex ($\Delta n_{eff}/n_{cavity} > 0$).

1.3.2.1 Current Spreaders

Due to the low electrical conductivity of p-GaN, an intracavity contact is required to act as a current spreading layer. The current spreader allows for uniform current injection across the aperture and lowers the overall series resistance of the device. Uniform current injection reduces current crowding around the edge of the aperture, which reduces device lifetime, promotes higher order modes, and reduces overlap with the gain region. Lateral current spreading from the metal contacts to the aperture has most commonly been achieved by a transparent conductive oxide (TCO), with the most popular TCO being indium-doped tin oxide (ITO) due to its ability to make efficient low resistance contact with p-GaN and its industry precedent in LED production[104]. ITO is straightforward to deposit, and low roughness

(<0.5nm), low resistivity (~$2x10^{-4}$ Ω-cm) films are readily achievable[104]. The drawback of ITO is that it is absorbing in the blue-violet range. In initial VCSEL demonstrations, 50nm and 240nm ITO layers introduced significant absorption loss, 0.5% and 1.4%, respectively[3,4]. For these designs, the ITO layer was the dominant source of loss for the VCSELs, and in general, the thickness of the ITO needs to be 20nm or lower and it needs to be aligned to a null of the standing wave to ensure optimal device performance from a loss perspective[72]. However, decreasing the thickness of the ITO limits its ability to adequately spread current, and can limit its utility in larger current apertures at the high operating current densities in GaN VCSELs[103].

Another option for current spreading is the GaN tunnel junction[105]. A tunnel junction is comprised of a highly doped n-type and highly doped p-type layer. Due to the high doping, a narrow depletion region is formed, and under reverse bias, electrons can tunnel from the valence band of the p-type region into the conduction band of the n-type region. In GaN VCSELs, the TJ current spreader consists of p+-GaN, n+-GaN, and a top n-GaN spreading layer. The first demonstration of a GaN TJ in a VCSEL found that the threshold current density decreased by 56%, and the max output power increased by 690%, when swapping a λ/4-thick ITO layer with a GaN TJ for lasing emission at 417nm[66]. This performance increase was primarily attributed to the greatly reduced absorption loss from the TJ layers relative to the ITO, which has an absorption coefficient of 2000cm^{-1} around 410nm. However, the TJ introduced a significant voltage penalty of 1.5V relative to the ITO VCSEL. Due to the tendency of Mg to propagate with the growth surface[106], the TJ requires a removal and subsequent regrowth to ensure the quality of the p/n interface. In MOCVD-grown TJs, this creates a variety of challenges that, if not addressed, introduce excess voltage, including:

sidewall activation of the p-type dopant Mg[107], the formation of passivating Mg clusters for high [Mg][108], and challenges with controlling the interface quality between p+-GaN and regrown n+-GaN[109]. These issues increase the depletion width between the TJ layers, exponentially decreasing the tunneling probability and increasing the voltage penalty for band-to-band tunneling[110].

While there have been some alternative current spreading schemes proposed for GaN VCSELs, including thin intracavity metal contacts[103] and subwavelength gratings[111], ITO and TJs have been the dominant current spreaders in GaN VCSEL demonstrations to date.

1.3.2.2 Concave Aperture

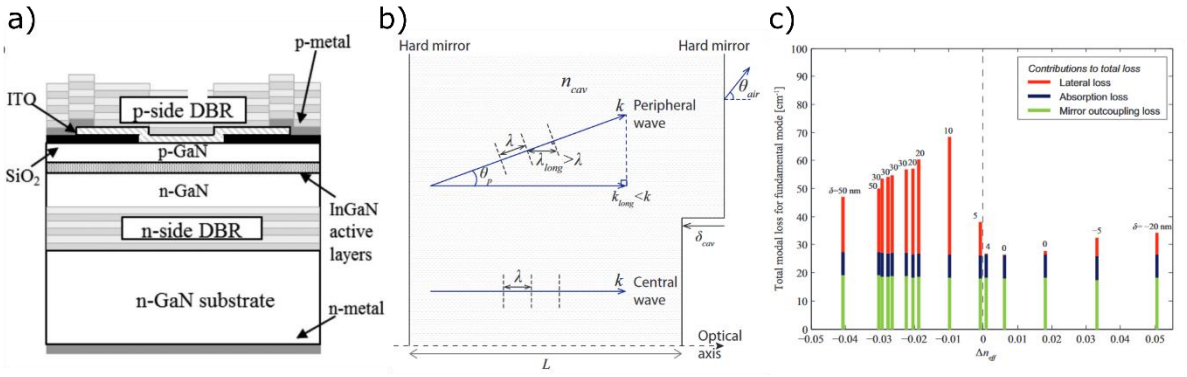

Figure 1.13. (a) Device schematic of GaN VCSEL with epitaxial bottom DBR and concave aperture. (b) Simplified model of laser cavity as a hard-mirror model with a central concave depression of thickness δ_{cav} and filled with a homogeneous medium of index n_{cav}. (c) Dependence of lateral, absorption, and mirror loss as a function of effective index contrast between aperture and peripheral cavity. (a) Copyright © 2016 Wiley-VCH GmbH. (b-c) Reprinted with permission.

Early GaN VCSEL demonstrations used an insulating layer, such as SiO_2, to create simple current confinement apertures[3,53,59,112,113]. A sample schematic of this design is shown in Figure 1.13 (a). Note that the dielectric layer is deposited first, followed by the TCO deposited into the hole and above the dielectric. The primary advantage of this technique was its ease of fabrication. However, the dielectric layer also increased the effective cavity length outside of

the aperture. It was shown by Hashemi et al. in 2013 that this increase in cavity length formed an anti-guiding cavity, generating a negative effective index gradient and leading to increased internal loss[114]. In an anti-guided cavity, the external or peripheral cavity is at resonance for an oblique angle of propagation, and the top and side TCO/SiO_2 interfaces facilitate lateral transport of optical power away from the current and optical confinement region. The mechanism of this is shown in Figure 1.13 (b). What is shown is the optical cavity of length L, with a depression of distance δ_{cav} created by the absence of the dielectric insulating layer in the optical aperture. Resonance within the cavity is determined by

$$k \cdot 2L = m_c \cdot 2\pi \tag{1.7}$$

where k is the wave vector $k=2\pi/\lambda$, and m_c is an integer. However, a field with the same oscillation frequency can also be resident in the longer peripheral cavity surrounding the aperture if it propagates at an angle, θ_p, with a slightly longer wavelength,

$$k_p \cdot 2L = m_p \cdot 2\pi \tag{1.8}$$

Figure 1.13 (c) shows the impact of the lateral loss on the total modal loss for the fundamental mode within cavities with concave, planar, and convex structures. It can be seen that even for very small negative Δn_{eff}, the lateral loss is of the same order of magnitude as the absorption loss, and for larger negative values, the dominant source of loss. Once thermal lensing effects are considered, the detrimental impact of lateral leakage is reduced, although it is still a prominent source of loss[115]. Interestingly, the anti-guiding effect is more pronounced for higher order spatial modes, due to their wider modal volumes and divergence, showing the potential utility of anti-guiding cavities for achieving single mode operation. However, the dramatic increase in modal loss for concave structures made them an unpopular choice, and

planar and convex structures, who had zero or significantly reduced leakage effects, became the dominant structures explored after 2014.

1.3.2.3 Planar Aperture

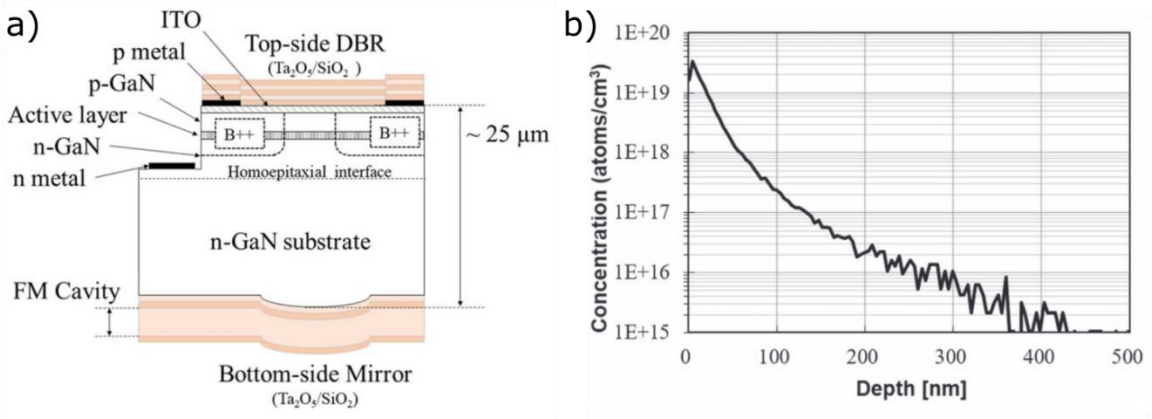

Figure 1.14. (a) Device schematic of GaN VCSEL with planar aperture defined by Boron ion implantation. (b) Boron depth profile in GaN as measured using SIMS. (a-b) [T. Hamaguchi et al, Jpn. J. Appl. Phys. **58**(SC), SC0806 (2019).] Reprinted under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/).

One alternative to the concave aperture is the planar aperture, an example schematic is shown in Figure 1.13 (a). In this approach, a thin p-GaN in conjunction with a TCO or tunnel junction structure is used to provide current injection and spreading. Instead of the current being confined by a dielectric layer, the current region is defined using ion implantation (IIA) of an ionic species[10]. Ion implantation is a commonly utilized technique in the fabrication of GaN semiconductor devices, offering advantages such as selective-area doping, precise control over doping profiles and concentrations, and device isolation[116]. Generally, ion implantation is employed for two purposes, either by introducing doped regions through implantation and activation of a dopant species, or by creating high resistance regions through the formation of deep traps or compensating centers. For doping purposes, Mg and Si are the most commonly used species, and have been demonstrated in high electron mobility transistors (HEMT)[117], current aperture vertical cavity transistors (CAVET)[118,119], and light-

emitting diodes (LED)[120]. For device isolation or aperture definition, a variety of ionic species (including C, Al, O, B, Ar, Zn, Fe, F, and others[121–125]) have been utilized, each providing different penetration depth profiles, thermal stabilities, surface damage, and trap state energies.

The implantation process involves bombarding the GaN epitaxy outside of the defined aperture region; at a high enough energy, the incident ions will locally damage the crystal structure and greatly decrease the electrical conductivity. Al ions[5,6] and B ions[10,126] have both been shown in GaN VCSELs. At proper implantation conditions, the surface of GaN behaves like an insulating layer, with reverse bias currents <10μA at -10V shown for B implantation[126].

I am being somewhat facetious by claiming that the "planar" aperture is defined as having an effective index contrast of 0 between the cavity and peripheral cavity. In fact, implanted GaN has a slightly reduced index of refraction relative to un-implanted GaN[5], attributed to the greatly increased density of vacancies and defects introduced by the implantation process. Generally, this is a benefit, as a slight positive index guiding will reduce the internal loss to lateral light leakage. However, this effect is quite small; for a VCSEL with a 1.2μm cavity, the effective index contrast is approximately 0.001. For 12μm cavity, the index contrast drops to ~0.0001. For this thesis, which primarily concerns long cavity (L>10μm) devices, this positive guiding is negligible relative to other guiding effects (e.g. thermal lensing).

There are several practical design challenges to consider with the ion implanted aperture. The ion implantation profile can be roughly calculated using Stopping and Range of Ions in Matter (SRIMS) simulations[127] to gain a general understanding of the expected penetration depth and final ion density within a particular material. Generally, an impacting ion will collide with atoms in the crystal and create vacancies. At certain angles, for example along

certain crystalline directions, ions will be much less likely to experience a collision and penetrate deep into the crystal in a process called channeling. This effect can be beneficial for dopant implantation, but for the purpose of GaN VCSEL, this effect can be minimized by implanting at a slight crystallographically irrelevant angle, e.g. 7°. Additionally, ions will have a certain amount of lateral straggle, meaning that they will implant laterally. This effect scales with the implant energy and is generally higher for smaller ions[128]. Since ions create vacancies and defects which can act as non-radiative recombination centers, lateral straggle is a potential source of absorption loss.[123,129,130] The risk of loss is highest for devices with modes that aren't properly confined to the center of the aperture, as was the case for ref. [6] and a general challenge for GaN VCSELs experiencing filamentary emission.

1.3.2.4 Convex Aperture

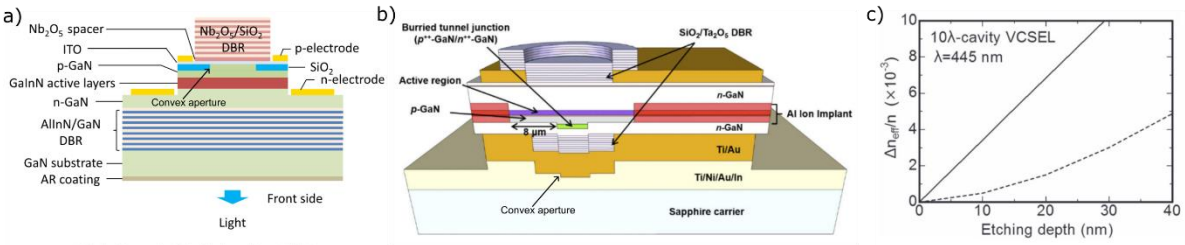

Figure 1.15. (a) Device schematic of GaN VCSEL with convex aperture defined by RIE. (b) schematic of GaN VCSEL with convex aperture defined by BTJ regrowth. (c) normalized effective difference as a function of buried SiO_2 waveguide (dashed) or GaN cylindrical waveguide (solid). (a) Copyright © 2018 AIP Publishing, (b) Copyright © 2019 (c) Copyright © 2020 The Japan Society of Applied Physics.

The final current confinement scheme to be discussed is the convex aperture. In this regime, Δn_{eff} between the cavity and external peripheral cavity is positive, leading to optical guiding. As has been previously discussed, the positively guided regime minimizes the effect of lateral loss up to a certain Δn_{eff}. However, a large Δn_{eff} can introduce some lateral loss due to diffraction. Additionally, high Δn_{eff} will provide stronger optical confinement, and can enable higher order modes to readily exist within the cavity. This is shown in the first

experimental demonstration of a convex aperture, which was a self-aligned SiO_2-buried layer[90]. The aperture, shown in Figure 1.15 (a), was formed by reactive ion etching (RIE) to a depth of 20nm, immediately followed by a self-aligned 20nm SiO_2 layer. The aperture was capped with ITO. Due to the self-aligned process and same thickness between dielectric and RIE p-GaN, the ITO deposition was planar, and the index contrast was between the SiO_2 and p-GaN. This led to an index contrast of 0.0026. The 8μm exhibited multi-mode lasing, attributed to both the wide aperture as well as the optical guiding provided by the buried dielectric. In 2019 – 2021, several buried tunnel junction (BTJ) VCSELs were demonstrated. The tunnel junction (TJ) acts as a hole injector for the p-GaN and allows n-GaN to be used for current spreading. In a BTJ, the highly doped n++-/p++-GaN layers are confined to the aperture such that current will only flow through that area. This confinement is achieved by growing a planar TJ and then dry etching the highly doped layers away from everywhere outside of the aperture before regrowing the current spreading layer. One interesting artefact of the current spreading layer regrowth is that the thickness difference from the BTJ eth is propagated into the upper epitaxial layer. This creates a positive guiding structure. The BTJ structure was first demonstrated in 2019, when CW operation was achieved for the second time at UCSB with a 40nm BTJ aperture[63]. The authors noted that the lasers exhibited filamentary emission, but that the mode order appeared highly structured. They attributed this structure to the high Δn_{eff}~0.04 which strongly encouraged higher order modes. Interestingly, in the second BTJ demonstration on semipolar (20-2-1), highly structured guiding was not observed despite the moderate Δn_{eff}~0.027[60]. However, this study also found a high correlation between the current injection and location of lasing modes, so it is possible the inhomogeneous current injection impact washed out the impact of the BTJ guiding.

Regardless, the step at the top of the regrowth was seen as a powerful tool for optical confinement, and one that naturally came with the BTJ current confining aperture.

Finally, recently it was shown that the cylindrical GaN waveguide could be directly fabricated by dry etching[81]. The authors showed that a meaningful positive guiding could be achieved by a very small dry etch into the upper p-GaN; the index contrast as a function of etch depth can be seen in Figure 1.15 (c). For their design, they used a dry etch depth of 5nm which corresponded to $\Delta n_{eff}/n_{cavity} \sim 0.0017$. Using this waveguide structure, they were able to achieve record-breaking output power of 23.7mW from a multi-mode 7μm current aperture VCSEL, and good single spatial mode performance from a 3.3μm aperture VCSEL. The relative ease of fabrication for this convex waveguide technique make it a promising design choice for future VCSEL development.

Since we were developing VCSELs in the violet emission range, ITO was a poor choice as a current spreader due to its high absorption coefficient at these wavelengths. We chose to use a GaN TJ as the n-side current spreader. We fabricated devices with both planar and convex apertures. More details can be found in Chapters 3 and 4 of this thesis.

1.3.3 Thermal Challenges

The performance of a VCSEL is heavily dependent on the device structure's ability to dissipate heat generated during operation. Ideally, above threshold, the optical power should increase linearly with injected current. However, as the device heats up, the rate of power increases decreases, until the power experiences rollover and the device turns off. There are several different heat sources such as joule heating, non-radiative recombination, Peltier

heating, and Thomson heating. Around threshold, the dissipated power, P_D, is roughly proportional to the input power P_{in},

$$P_D \sim P_{in} = I_{in} V_{in} \tag{1.9}$$

At this low injection level, the heating effects due to the optical output power can be neglected, although generally this contributing effect is small compared to the other power dissipation effects. The thermal impedance, R_{th}, is geometry dependent and allows for one to calculate the expected rise in temperature for a given input power,

$$\Delta T = P_D R_{th} \tag{1.10}$$

The optical spectrum of a VCSEL can be used to experimentally estimate the thermal resistance. By influencing the temperature of the laser in two independent ways, first by changing the ambient temperature and separately by changing the input power, one can derive a data set (ΔT, ΔP) for which the red shift is the same. These relationships can then be used to calculate the thermal resistance by[131],

$$R_{th} = \frac{T_j - T_{amb}}{P_{in-P_{out}}} \sim \frac{\frac{\Delta\lambda}{\Delta P_{in}}}{\frac{\Delta\lambda}{\Delta T_{amb}}} \tag{1.11}$$

In practice, the dependence of the wavelength on input power can be determined by increasing the pulse width or duty cycle of a pulsed measurement over a suitable range of input powers (P_{in} 0-100mW) at room temperature, and the dependence of the wavelength on ambient temperature can be determined by placing the VCSEL on a heat stage and taking measurements at a constant pulse width and duty cycle (500ns pulse, 0.5% duty cycle or lower).

There are several ways that elevated temperature contribute to rollover, including increased carrier leakage out of the active region, a red-shift of the gain spectra due to a thermally-induced reduction to the band gap, and a misalignment between the lasing mode and gain spectra due to thermal lensing. Increased carrier leakage results in a higher threshold current to reach the same carrier density within the quantum wells, reducing differential efficiency. A reduction in the gain spectra and misalignment between the gain spectra and lasing mode requires a higher input power to generate the same amount of modal gain to offset internal and mirror losses. All of these together results in a near exponential dependence of device performance on temperature effects. For GaN VCSELs, which have roughly 10-20x the input power requirements compared to GaAs VCSELs, understanding the sources and consequences of generated heat is critical to achieving good device performance.

Amongst the various GaN VCSEL designs, the selection of the bottom DBR is particularly impactful when evaluating thermal management implications. As can been seen from Tables 1.3 – 1.5, the thermal impedance values vary significantly by design. Dual dielectric DBR designs have generally reported the highest thermal impedances, with the average impedance well above 1000 K/W. NP DBR VCSELs have also been limited by the thermal impedance of the NP DBR, with only one CW demonstration reported. While AlInN DBR VCSELs have shown multiple high power CW demonstrations, and thermal impedance values below 1000 K/W, many of these designs have also employed longer cavity designs than the dielectric DBR and NP DBR designs which reported thermal impedances. The impact of long cavities on VCSEL performance will be discussed in Section 1.3.5.

1.3.4 Transverse Mode Control

As previously mentioned, many applications require a lasing source with stable, single longitudinal and spatial emission. For longitudinal modes, the wavelength is dependent on the optical cavity thickness. Which particular mode lases is determined by the modal overlap between the gain region and the modes, minus the internal loss. As mentioned previously, both single and muti-longitudinal mode VCSELs have been demonstrated with a variety of cavity lengths.

In discussions about lasing modes, it's crucial to consider transverse modes alongside longitudinal ones. Transverse modes denote the varied intensity profiles that a single longitudinal mode can adopt. To optimize laser performance, these modes should be confined within the aperture area to minimize diffraction loss. The selection of confined transverse modes hinges on the lateral index profile of the device design. Typically, as the index contrast between the core (aperture area) and cladding (outside aperture) increases, the number of viable transverse modes expands. The VCSEL designs using the positively gain-guided convex aperture feature an index step at the aperture edge to introduce optical guiding, potentially enabling multiple potential transverse modes. For planar designs the device is considered gain-guided, with index guiding occurring only during laser pumping due to the index's dependence on carrier density and temperature. During operation, the increased carrier density and temperature in the aperture both work to increase the refractive index, slightly confining the mode. However, these effects are dependent on current spreading and thermal management, and in general are difficult to precisely control. The best performing GaN VCSELs have all exhibited some form of index or optical confinement.

Transverse spatial mode shapes are commonly described by Laguerre-Gaussian (LG), Hermite-Gaussian (HG), or Ince-Gaussian (IG) modes depending on whether the geometry and symmetry of the cavity is circular, rectangular, or elliptical[132]. LG modes have rotational symmetry along their propagation axis, and as such higher order LG modes can be derived by modulating an amplitude function proportional to the wavevectors in the x and y direction, k_x and k_y, with an angular dependency defined by $\phi = tan^{-1}(\frac{y}{x})$. The electric field of the Laguerre-Gauss mode, $E_{l,p}^{LG}$, is described by the following (Equation 1.12)[132]:

$$E_{l,p}^{LG} = \frac{e^{-il\phi}}{w\left(\frac{z}{z_R}\right)}\left(\frac{\sqrt{x^2+y^2}}{w\left(\frac{z}{z_R}\right)}\right)^l L_p^l\left(\frac{2(x^2+y^2)}{w^2\left(\frac{z}{z_R}\right)}\right)\exp\left(ikz - \frac{x^2+y^2}{w_0^2\left(1+\frac{iz}{z_R}\right)} - i(l+2p+1)tan^{-1}\left(\frac{z}{z_R}\right)\right)$$

where *l* and *p* are integers ranging from 0 to infinity that denote the mode's angular momentum about the optical axis and radial distribution of intensity, respectively, and z_R is the Rayleigh length, defined by

$$z_R = \frac{\pi\omega_0^2}{\lambda} \tag{1.13}$$

The beam waist, ω_0, and beam at a distance z from the beam waist, $w\left(\frac{z}{z_R}\right)$, are both described in more detail in section 2.3.

Figure 1.16 (a) shows example calculated modes for the three symmetries, and Figure 1.16 (b) shows a selection of lower order Laguerre-Gaussian modes. Note that some general features of the fundamental mode are spatial symmetry, low beam divergence, efficient coupling, and higher gain, relative to all higher order modes, hence why it is the mode most desired for many industry applications. The intensity radial profile of the fundamental mode has a centrally symmetric bell-like form resembling a Gaussian. Therefore, for optimal excitation of this mode within a VCSEL cavity, a similarly shaped profile of the threshold optical gain would be the most preferable. However, this is only feasible for smaller VCSEL apertures, where current crowding effects are at a minimum. With an increase in the aperture size, current crowding will gradually change the injection profile into a more doughnut-like profile, encouraging generation of higher order modes. Note that as the mode order increases,

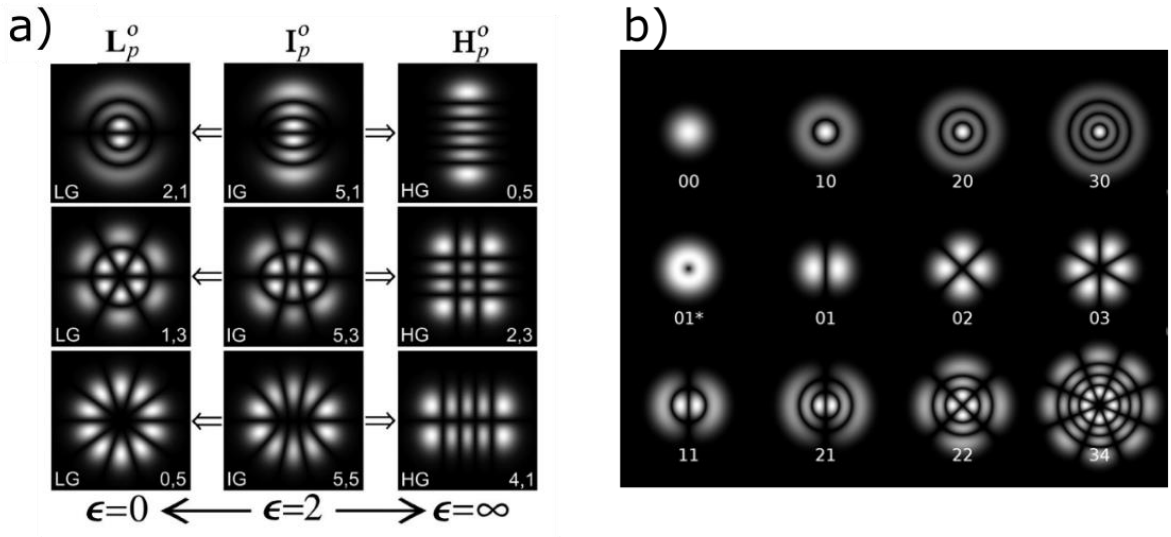

Figure 1.16. (a) Example higher order LG, IG, and HG modes. (b) The fundamental LG mode compared with the next highest LG modes. (a) Copyright © 2004 The Optical Society. Reused with permission (b) Ref 133.

the mode volume increases as well[133]. In general, GaN-based VCSEL designs, whether planar or with a curved lens, have struggled to realize single transverse mode operation for current apertures wider than 4μm, mainly for two reasons. First, GaN VCSEL transverse mode control

has struggled with filamentary lasing, defined as non-uniform emission across the current aperture[134]. The exact cause of filamentary lasing is unknown, but is believed to be partly due to non-uniformities or interfacial effects between the p-GaN and current spreading layer, or inefficiencies in the thermal activation process for p-GaN. This non-uniformity issue is worse for MOCVD-grown tunnel junctions, where hydrogen passivates Mg in the p++-layer (and underlying p-type layer), requiring a thermal activation post-growth. Hydrogen cannot diffuse through n-type GaN, so for TJ devices the hydrogen must move laterally out through the device sidewalls[107]. This result in incomplete activation, where Mg at the center remains passivated, and in general activation is less efficient compared to topside activation, introducing an additional resistance-related voltage penalty and impacting light uniformity. Filamentary lasing has been observed in a variety of VCSEL architectures, including ITO-current spreader[102], tunnel junction[135], and in both planar and non-planar demonstrations[136], and the effect gets worse for wider apertures. In practice, the filamentary lasing leads to messy mode behavior that is difficult to manipulate, including coupling into optic fiber, beam steering, and directional illumination[137]. Certain structures, such as mode posts or curved lens, appear to generate more symmetric and ordered modes[138], and in some cases, generate clean higher order transverse modes and even the fundamental transverse mode[81,136]. However, the control over the generation of either the fundamental mode or higher order modes using larger apertures has been inconsistent. Recently, the use of lenses with ultra-wide radius of curvatures (ROC) has shown single transverse mode operation for an 8μm aperture, but the large size of the lens limits VCSEL packing density and applicability to commercial products which require dense 2D arrays[61]. Figure 1.17 (a) and (b) show example topside nearfield patterns (NFPs) of GaN VCSELs with planar apertures ($\Delta n_{eff}/n_{cavity}$~0) exhibiting filamentary

lasing without any symmetry and GaN VCSELs with convex apertures ($\Delta n_{eff}/n_{cavity}>0$) exhibiting filamentary lasing with symmetry along the c-direction, respectively. Device structures detailed in ref[134]. Figure 1.17 (c) shows a topside NFP of a GaN VCSEL with a curved lens that is lasing in the fundamental mode, and Figure 1.17 (d) shows the FFP of a GaN VCSEL with a curved lens[136]. The apparent dependence of filamentary lasing on the optical elements within the cavity shows that mode structure is a complex combination between the waveguiding and current non-uniformity within the aperture.

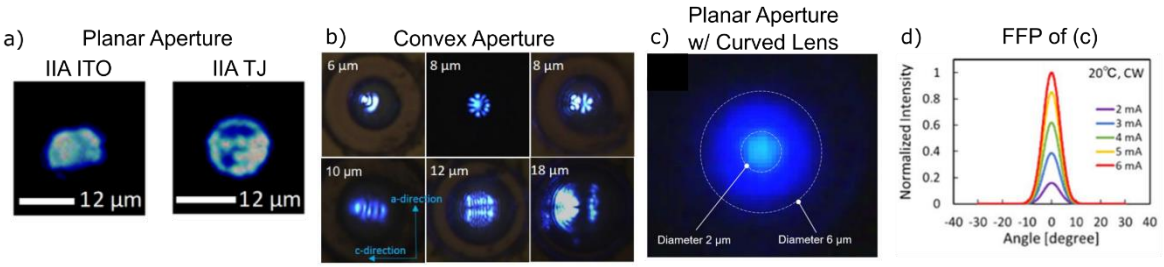

Figure 1.17. (a) Topside NFPs of planar aperture VCSELs with ITO or TJ current apertures. (b) VCSELs with GaN BTJ convex current apertures. (c) Planar aperture VCSEL with curved GaN lens. (d) Topside farfield pattern of VCSEL in (c). (a) Copyright © 2015 AIP Publishing, (b) Copyright © 2020 SPIE. (c) [Hamaguchi et al, (2019) A review on the latest progress of visible GaN-based VCSELs with lateral confinement by curved dielectric DBR reflector and boron ion implantation, JJAP 58, SC0806 (2019)] under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/). (d) [Nakajima et al, (2019) Single transverse mode operation of GaN-based vertical-cavity surface-emitting laser with monolithically incorporated curved mirror, Appl. Phys. Express 12 0840036 (2019)] under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/).

The second reason that mode control for GaN VCSELs apertures wider than 4µm is difficult is that for wider apertures, the overlap with higher order modes and the current aperture become higher, leading to laser output beams that are multi-lobed and multi-wavelength. This issue is material system agnostic, and is instead a symptom of current crowding, spatial hole burning, and thermal lensing, all of which are exacerbated for large VCSEL apertures. A particular transverse LP_{ij} cavity mode is excited in a laser cavity when its modal gain becomes equal to its modal losses. In the case of the fundamental mode, the intensity profile is in the form of a single central peak, and the intensity area is minimized.

All other organized higher order modes contain more peaks where at least some of them are shifted from the central active region position. To enhance stable single mode operation, modal gain of the fundamental mode and/or modal losses of all higher order modes should be as high as possible. This means that the radial profile of the optical gain should be approximately Gaussian, and the optical losses should be radially shifted from the central position. This is a fundamental challenge for wider aperture VCSELs, since current crowding around the edge of the aperture leads to the opposite of the desired effect. Fortunately, there are some applications which would prefer an organized higher order mode, such as in spatiotemporal mode locking, where higher order modes have a higher effective area compared to single modes, leading to higher and tighter energy per pulse[139]. Regardless, it is preferable to generate only one single mode, be it the fundamental spatial mode, or a selected higher orer mode. Focusing back on generating the fundamental spatial mode, and suppressing all higher order modes, a variety of techniques have been developed in the more mature GaAs-based VCSEL system as reviewed extensively by ref. [140]. Each technique either increases the modal gain of the fundamental mode or increases the modal loss for all higher order modes, and they will be summarized here.

To increase the modal gain of the fundamental mode, the most efficient method is to improve the uniformity of the current injection into the VCSEL active region[133]. However, this method alone is limited, as increasing current injection above threshold will lead to spatial hole burning, wherein stimulated carrier recombination in places of high mode intensity (the center of the active region) leads to lower carrier concentration in the center. Over time, this will lower the modal gain of the fundamental mode and increase the modal gains of the higher order modes. Additionally, as mentioned previously, uniform current injection is a general

challenge for larger apertures. Alternatively, the radial absorption loss can be adjusted using ion implantation. In this method, ions are implanted which heavily absorb incident light[141]. This approach relies on the fact that higher order modes have a wider distribution of light intensity compared to the fundamental mode, so they will interact more with the implanted region and experience higher absorption loss. The main limitation with this is that there is a tradeoff between higher mode selectivity and performance, since the fundamental mode will still have some overlap with the implanted region.

To increase the modal loss of higher order modes, one popular method is to use spatial mode filtering by modifying the reflectivity of the DBR. By taking advantage of the central confinement of the fundamental mode, the DBR can be designed to have higher reflectivity in the center, but lower outside, leading to exorbitant mirror losses for the higher order modes[142]. Another simple method is to increase the cavity length, as diffraction loss increases with cavity length and higher order modes suffer from higher diffraction losses compared to the fundamental mode[143]. However, this option is not available for VCSELs with a curve lens, as diffraction loss is prevented. Another option is to use a passive-antiguide-region, wherein the central VCSEL aperture is surrounded by a material with a higher index of refraction, again leading to higher diffraction losses of the higher order mode[144]. Finally, scattering loss can be radially introduced into the structure that interact with the higher order mode. In this method, the central aperture is surrounded by, or partly intersected by, a row of hole structures that selectively introduce loss. For GaAs-based VCSELs, the hole structure has been used to great effect, generating near record high output power and low divergence of the output beam[145,146]. Figure 1.18 (a-b) shows one example iteration of this structure, wherein triangle shapes were dry etched into the VCSEL structure. The choice of triangles was made to

increase the field penetration of higher order modes with the hole, taking advantage of the higher modal volumes of higher order modes[146]. Figure 1.18 (c) shows the topside NFP with yellow solid lines indicate the position of the triangle holes, and the red dashed line indicates the position of the aperture. Figure 1.18 (d) shows the topside FFP of the fundamental mode. This particular demonstration is of particular interest for GaN VCSELs due to its relative ease of fabrication and ability to fine tune mode control.

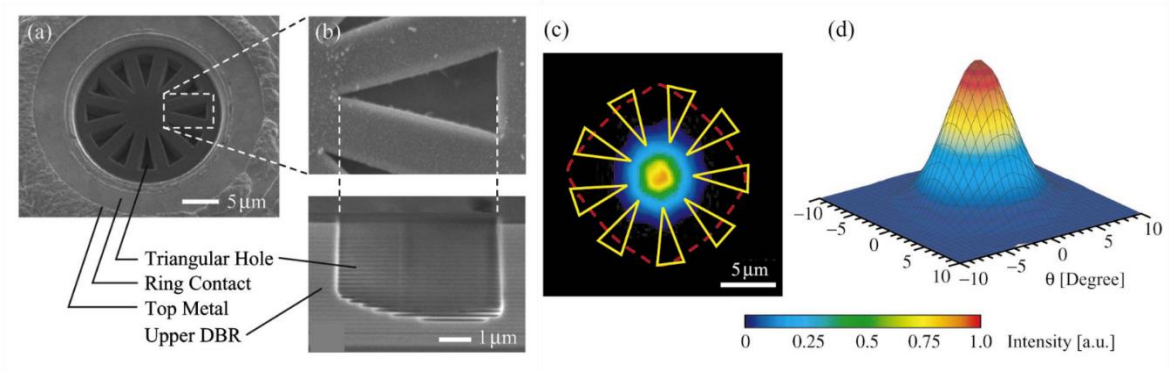

Figure 1.18. (a) SEM image of GaAs VCSEL with triangle shaped holes etched into the top DBR and cavity. (b) Magnified top view of triangular hole. (c) Topside NFP with yellow solid line to indicate location of triangles, and dashed red line to indicate position of oxide aperture. (d) Topside FFP of VCSEL under operation. Copyright © 2004 AIP Publishing. Reprinted with permission.

Many of these methods, such as passive anti-guiding[114], long monolithic cavities[13], spatial mirror filtering[81], ion implantation[5], and patterned apertures[79] have been employed in GaN VCSELs, some with the explicit goal of mode control. Of these, using a curved mirror or reducing the aperture size, or both, appears to be a consistent method for obtaining the fundamental spatial mode.

1.3.5 Advantages of the Long Cavity VCSEL

Long cavity designs have emerged as a crucial strategy in enhancing the thermal performance of GaN VCSELs. By extending the cavity length, these designs facilitate efficient heat dissipation through increased thermal spreading within the active region, thereby

mitigating the detrimental effects of thermal build-up, which include degradation in active region gain, threshold current, output power, and emission spectrum[147]. This is a pressing issue for GaN VCSELs, which have over twice the expected turn-on voltage, and between 7 – 70 times higher threshold currents than their III-AsP counterparts[8]. Extending the cavity length allows for better heat extraction from the device, reducing the operating temperature gradient across the structure and minimizing thermal-induced wavelength shifts and spectral broadening. Consequently, long cavity designs offer improved reliability, stability, and overall performance of GaN VCSELs.

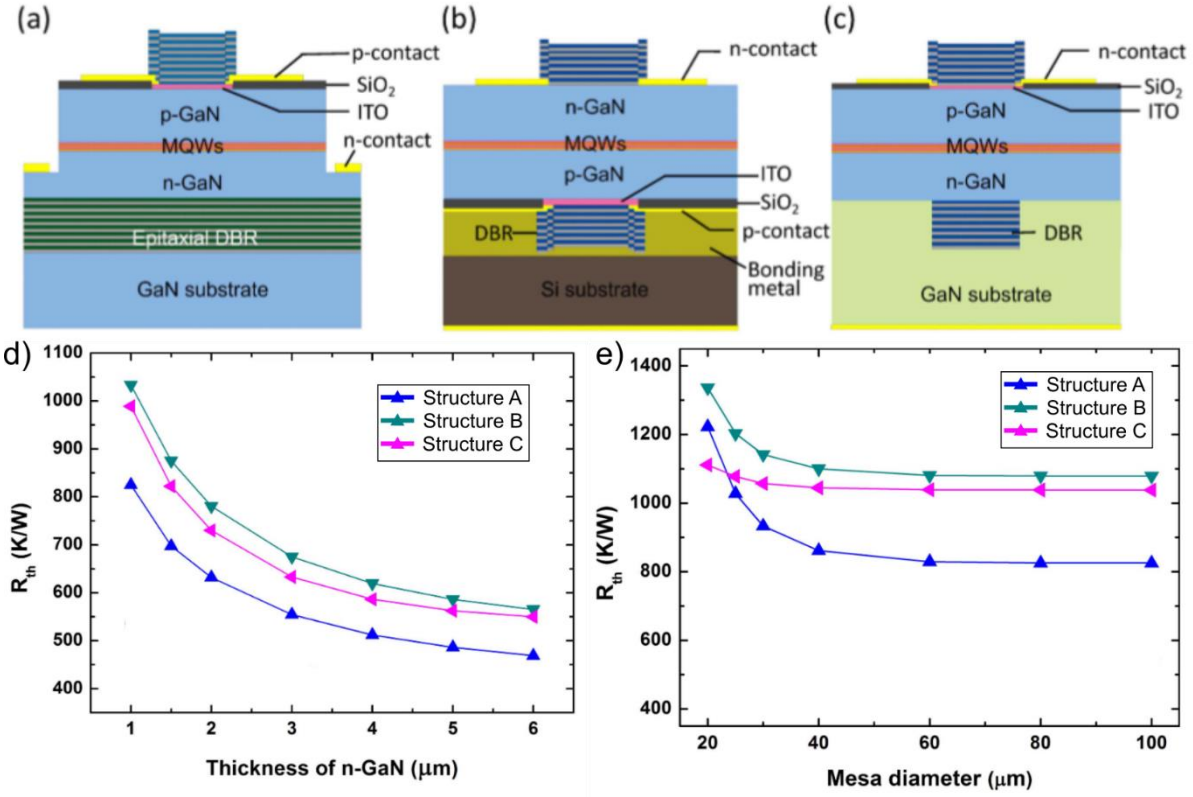

Figure 1.19. Three typical structures of GaN VCSELs. (a) hybrid bottom epitaxial AlInN/GaN DBR, (b) dual dielectric DBR fabricated via PEC flip chip bonding, (c) dual dielectric DBR fabricated through ELO. (d) Thermal resistance as a function of bottom n-GaN thickness. (e) Thermal resistance as a function of mesa diameter. Copyright © 2017 IOP Publishing. Reprinted with permission with minor edits.

In a study by Mei et al, the effect of extending the cavity length on three VCSEL structures, a hybrid bottom epitaxial AlInN/GaN DBR (Structure A), a flip chip dielectric DBR (Structure

B, and an ELO dielectric DBR (Structure C) design were studied. The design of each VCSEL structure can be seen in Figure 1.19 (a) - (c), and Structure A was simulated with different epitaxial DBR options. The thickness of the bottom n-GaN was varied and its effect on the overall calculated thermal impedance is shown in Figure 1.19 (d). It can be seen that for all three structures, increasing the n-GaN from 1μm to 6μm reduces the thermal impedance by >40%. This reduction is of the same magnitude whether or not the active region is placed next to the insulating DBR structure or far from it. The thicker n-GaN layer improved the thermal dissipation in all structures because GaN has a large thermal conductivity which benefits the out-diffusion of thermal energy from the active region. While the study only considered cavity lengths up to approximately 6μm, there are still potential reductions in thermal impedance for thicker cavities, although the added benefit is lower. The authors also showed that the device mesa diameter can also play a role in reducing thermal impedance, with the effect most pronounced for the epitaxial DBR structure, Structure A. This is because in Structure A, the epitaxial DBR covers the entire base of the mesa, so heat must always transfer vertically through the DBR. However, in Structure B and C, the dielectric DBR is only 12μm in diameter, so wider mesas allow for lateral as well as vertical heat spreading. However, the benefits of increasing mesa size only occur up to 60μm for all three designs. It is clear that the geometry of the device plays a large role in performance, and that besides the choice of bottom DBR, extending the cavity length has the largest impact on thermal impedance.

At the time of this study, the NP DBR had not yet been demonstrated within a GaN VCSEL and so it was not considered. However, a subsequent study calculated that the NP DBR structure outperformed a flip-chip dielectric DBR structure due to a higher lateral thermal conductivity of the porous GaN[97]. The takeaway here is that the thermal performance

of the NP DBR likely lies somewhere in between a dual dielectric DBR and AlInN/GaN DBR design.

Within the field, there have been several direct comparisons between VCSEL designs with short and long cavities. In 2018, Forman et al demonstrated the first *m*-plane VCSEL capable of CW operation[7]. They found that increasing the cavity length from 1.1μm to 3.8μm decreased the operating temperature at the active region from 270 °C down to 170 °C and enabled the longer cavity device to operate under CW operation. Kuramoto et al fabricated two VCSEL structures with identical current spreader and AlInN/GaN DBRs, but with different cavity lengths of 0.66μm (5λ) and 1.57μm (10λ)[91]. They found that doubling the cavity length reduced the thermal impedance from 1100 K/W to 710 K/W, increased the differential efficiency from 25.4% to 31%, and increased the peak output power before thermal rollover from 8.2mW to 15.7mW. Muranaga et al performed a similar study on shorter cavities, 0.25μm (1.5λ) versus 0.66μm (4λ), and observed similar behavior[88]. In this study, increasing the cavity length from 1.5λ to 4λ reduced the thermal impedance from 2700 K/W to 1300 K/W, increased the peak output power at thermal rollover from 0.03mW to 0.45mW, and increased the current at thermal rollover from 5.3mA to 15mA.

Sony Corporation has recently been pursuing a VCSEL design with a cavity length significantly longer than others, at around 20μm (100+λ)[10]. Their design utilizes the dual dielectric DBR architecture, and they use CMP to expose the bottom DBR. However, due to the long cavity, a planar cavity would exhibit high diffraction loss more than 1%. To adjust for this, the authors incorporated a curved monolithic GaN lens on the back of the substrate after CMP. The lens provides optical confinement and re-captures the loss that would otherwise have occurred due to diffraction. Sony has made a variety of record-breaking

demonstrations, and this VCSEL design has broken the record for output power[9], threshold current[72], and wall-plug efficiency[9]. Sony's long cavity design is incredibly robust to growth rate fluctuations and thermal energy generation, with demonstrations on substrates as large as 2-inch. Additionally, they have shown that they can reliably generate a single spatial mode in the farfield (FFP) with a low divergence angle using a lens with a large radius of curvature[61], and that they can achieve longitudinal mode control using external cavity structures[73]. One notable drawback of Sony's long cavity design is the CMP process that forms the cavity, as the resulting epitaxial wafer is only around 20μm thick. This poses a significant scalability challenge, as the thin wafer is prone to cracking during processing and during integration onto non-native wafers (for example, using an automated pick-and-plance machine). A more detailed discussion on the lens can be found in Section 2.3, but suffice to say here that there are significant advantages to ultra-long cavity structures.

Besides the benefit to thermal performance, increasing the cavity length has consequences on the spontaneous emission coupling factor (β)[71] and longitudinal mode spacing (Δλ). β can be defined as the fraction of spontaneous emission coupled into a cavity mode with respect to the spontaneous emission into all modes, and depends on the Purcell factor of the cavity[148,149]:

$$\beta = \frac{F_p}{1+F_p} \tag{1.14}$$

where the Purcell Factor F_p is:

$$F_p \propto \frac{1}{[\ln(R)+L_c\alpha_i]} \tag{1.15}$$

where R, L_c, and α_i are the mirror reflectivities, effective cavity length, and calculated absorption loss in the VCSEL, respectively. By decreasing the cavity length, β is increased,

meaning more spontaneous emission is incorporated into the lasing mode and the threshold current is reduced.

Additionally, increasing the cavity length will decrease Δλ, the spacing between adjacent longitudinal modes. Δλ is defined as:

$$\Delta\lambda = \frac{\lambda^2}{2\bar{n}L_c} \tag{1.16}$$

where λ is the lasing wavelength and $\bar{n}$ is the effective group index. For a typical 5λ GaN VCSEL cavity structure, Δλ is approximately 30nm for modes around 405nm. For the 10λ design explored above, Δλ reduces to around 16nm. For Sony's long cavity design, assuming the design thickness of 20μm or 120λ at 405nm, the mode spacing is around 1.64nm. The average InGaN QW emission bandwidth is approximately 10-30nm FWHM for emission ranging from 405nm – 450nm, which means that long cavity VCSELs are more likely to exhibit multi-longitudinal mode operation. Additionally, the emission is prone to mode-hopping, wherein the lasing mode abruptly hops to an adjacent mode. For certain applications which need stable emission at a specific wavelength, for example in cold atom trapping where emission at a specific wavelength is required to hit a specific energy transition state, this lack of longitudinal mode control is a detriment. However, for certain other applications, for example in directional lighting or displays, the thermal benefits gained from extending the cavity length outweigh the downsides.

The advantages of the long cavity VCSEL with a curved lens were appealing for a variety of reasons. First, there have been several high power, high efficiency CW demonstrations, attributed to the superior thermal management over short cavity designs. Second, single longitudinal[73] and low divergence single spatial mode[61] control have both been

shown using this design, showing its potential to suppress filamentary lasing for larger apertures. However, the existing method for lens fabrication is incredibly complex, requiring CMP polishing and subsequent handling of a thin 20µm thick wafer. Not only does this introduce challenges when scaling this process or when integrating it into a broader product line, but it also limits the flexibility of the cavity design; the minimum demonstrated cavity thickness is 20µm, and post-patterning of the lens, i.e. introducing holes, is limited. Additionally, the only lens material that has been demonstrated is GaN, mainly due to the convenience of how the lens is fabricated onto the backside. Therefore, we developed a topside lens method that addresses these issues: we've removed the need for CMP, we demonstrate VCSELs with cavity lengths on the order of 10µm - 12µm, we show that we can manipulate the lens shape by introducing holes for improved activation and mode control, and we show that we can fabricate VCSELs with lenses made of either GaN or a dielectric.

2 Methods

This chapter delves into the major design elements for VCSELs with an epitaxial nanoporous DBR and lens design. First, the complete process flow will then be presented. Next, the development of the NP DBR at UCSB will be discussed, as well as the unique electrochemical etch setup that we employed. Finally, the topside lens design and incorporation into a VCSEL are considered, with a focus on the epitaxial regrowth of the thick topside GaN required for the topside GaN lens.

2.1 Process Overview

This section outlines the growth and fabrication process to create *m*-plane long cavity GaN VCSELs with a nanoporous (NP) DBR with a topside GaN lens. Please note that this fabrication process is a work-in-progress, and the fabrication process should be treated as malleable.

Table 2.1. Epitaxial structure grown via MOCVD, including thickness, approximate doping concentration, and absorption coefficients.

Growth Step	Layer	Thickness (nm)	Doping Conc. (cm^{-3})	Abs. Coeff. (cm^{-1})
	GaN	1700	UID	**2**
3rd	n-GaN	1810	$8x10^{18}$	**2**
2nd	n++-GaN	8	$1.5x10^{20}$	**235**
1st	p++-GaN	10.5	$2.5x10^{20}$	**180**
	p-GaN	80	$1x10^{19}$	**80**
	p-AlGaN EBL	10	$1x10^{19}$	**27**
	GaN barrier	5	UID	**2**
	GaN/InGaN QW (2x)	3/8	UID	**0**
	n-GaN	2500	$8x10^{18}$	**2**
	GaN	3860	UID	**2**
	n+-GaN/ GaN DBR (24x)	48.4/40.4	$5x10^{19}$/UID	**0/0**

The first step is MOCVD growth on freestanding *m*-plane GaN substrates to grow a majority of the epitaxial layers. The growth required from each of the three growth steps is shown below in Table 2.1, with the approximate thicknesses, doping levels, and absorption coefficients used for fabrication of the initial GaN lens VCSEL. Absorption coefficients estimated from ref[150]. Before growth, a series of MOCVD growths are performed for each of the layers to calibrate the growth rate using x-ray diffraction (XRD). The growth rate for n-GaN, for example, is calibrated by performing MOCVD on an *m*-plane GaN template substrate to grown a GaN template, 15nm AlGaN, and a 50-200nm n-GaN layer. Using XRD to perform a 2-theta/omega scan, the interference fringes created by phase differences between AlGaN and n-GaN layer are inversely proportional to the layer thickness. By modeling the scan in a software and comparing to the MOCVD growth time, the growth rate can be

obtained. This method can be used to calibrate the growth rates of every layer; in practice, the thinner InGaN QWs can be difficult to accurately measure because of the relatively thick growth requirement for the calibration sample. Additionally, for the long cavity VCSEL design, accurate control of every growth rate is not required due to the close longitudinal mode spacing. For example, a deviation of -10% in a 10μm GaN cavity thickness will only increase the resonant mode spacing from 3.36nm to 3.74nm for modes around 410nm. Therefore, within this thickness regime there will always be a number of resonant modes available in the cavity regardless of the gain bandwidth. However, the thickness of certain layers is critical to proper device performance. Of these, the growth rates of the n++-GaN and UID-GaN layers that make up the NP DBR are critical to control as precisely as possible, as the reflectance spectrum is directly dependent on those layers. Any deviation in the layer thicknesses will blueshift or redshift the NP DBR. Since the expected stopband around 410nm is roughly 25nm, and the expected FWHM of the gain region is roughly 15nm, even a small deviation in the growth rate can destroy the resonant cavity condition. Besides the thickness of the NP DBR layers, the spacing between the active region and TJ layers is also of interest. The optimal VCSEL epitaxial structure is one where the active region is aligned to an antinode of the electric field intensity, and any layers with a high absorption loss are aligned to a node of the electric field intensity. Within the long cavity VCSEL structure being discussed, the layers with the highest absorption loss are the p++-GaN/n++-GaN TJ layers, therefore the spacing between them and the active region needs to be controlled to ensure the lowest loss. As there are multiple resonant modes within the structure, this condition is impossible to hit for every mode. Rather, the growth is designed to align one of the modes, generally the one expected to be at the peak gain bandwidth. Therefore, the growth rates for the p-AlGaN EBL and p-GaN

layers should be calibrated to match the design thickness as closely as possible. If substrate availability is limited, just calibrating the p-GaN should work well enough. Note that for a shorter cavity design, for example cavities with only a single resonant mode, every layer needs to be calibrated and prayers should be said.

After calibrating the growth rates of relevant layers, the 1st growth step of the epitaxial structure is grown, the p-GaN is activated (625 °C for 15min), and electroluminescence (EL) is performed to check the quality of the growth and ensure the emission wavelength is near the target wavelength. This is performed using the "quick-test" method in which indium metal is pressed through a metal shadow mask to create circular p-contacts on the top surface, and indium metal is soldered on the side of the GaN substrate to create the n-contact. For emission around 410nm or 450nm, the FWHM should be 10-12nm and 18-25nm, respectively. Note that the spectrometer can display an offset emission spectrum if it hasn't been calibrated in a while, so one optional step is to calibrate the spectrometer before testing. Depending on the substrate used, the quick-test power can vary. It is important to have a reference sample to properly relate the power to prior quick-test performance metrics. After quick-testing the calibration sample, the MOCVD growth temperature of the active region can be adjusted accordingly to shift the emission wavelength to re-align with the design condition.

After calibrating the growth rates and emission wavelength, MOCVD is performed on the actual VCSEL samples. In addition to the VCSELs, a NP DBR calibration sample is grown. This sample will be used to calibrate the porous etch condition as best as possible. The growth condition is identical to the VCSEL condition, but the growth ends after the last NP DBR period is grown. It is processed only during the relevant processing steps to expose and porosify the NP DBR. After growth, the quick-test process is repeated on each sample, and

samples are ranked based on their performance. At a current of 20mA, an *m*-plane VCSEL epitaxial stack emitting at 410nm should have a voltage ~5V and an output power of ~5-7mW. Any significant deviation may trigger a regrowth; however, due to the shift in growth rates across GaN substrates grown in UCSB MOCVD reactors, many samples should have a region that shows good performance.

Next, samples are submerged in boiling aqua regia (3:1 $HCl:HNO_3$ at 120 °C) for 30min to remove the indium contacts. Next, the samples are treated with 2-3 cycles of 10min UV ozone followed by 2min concentrated HF. The UV ozone helps to remove any organic particulates and the concentrated HF removes Mg that propagates to the top of the growth surface[106] as well as removes the native oxide that quickly forms when GaN samples are exposed to atmospheric conditions. After, samples are reloaded and n++-GaN is regrown via MOCVD. Note that both surface Mg and native oxide can affect the TJ performance, as the interface is incredibly sensitive. Therefore, it is recommended to do the last concentrated HF dip as close as possible to loading the samples into the reactor.

For each processing step involving a photolithography going forward, there will be a side-cut of the epitaxial stack along with a top-down image of the VCSEL mask. After the regrowth, there are two photolithography steps to perform before the second regrowth. The 1st lithography step is to etch alignment marks that will be used throughout the rest of the fabrication process. The epitaxial layers after the first regrowth and alignment mark pattern can be seen in Figure 2.1.

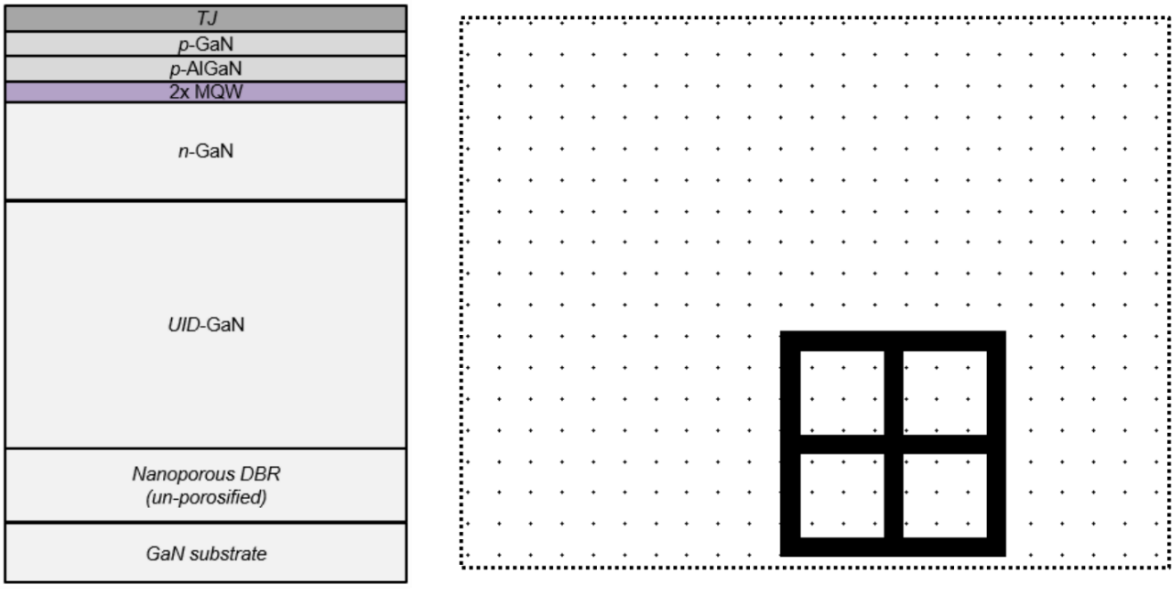

Figure 2.1. (Left) Schematic illustration of the epitaxial structure after the first regrowth. (Right) Image of mask showing an alignment mark.

The alignment marks must be precisely aligned relative to the a-direction and c-direction. This is done so that the trench etch to the NP DBR layers is aligned to be parallel to the a-direction. This allows for uniform porosification etch rates on both sides of the trench, as it was known that the c+ and c- directions react with the porosification etch at different rates. The alignment mark is etched with reactive ion etching (RIE) using Cl_2. The precise depth for this layer is not important as anything greater than 400nm will be easily resolvable in subsequent processing steps using the Heidelberg maskless aligner. Note that these alignment marks may be affected by the thick n-GaN regrowth later in the process. For example, when performing the 3µm regrowth on *m*-plane GaN, the facets defined by the etch created lateral growth fronts that grew at different rates. The a-direction facets grew at the same rate, but the c+ and c- directions grew differently. This effect distorted the alignment marks and made alignment to the BTJs difficult. Figure 2.2 (a) and (b) show the designed alignment mark and the alignment mark after regrowth. The horizontal cross-bar, which was aligned parallel to the

c-direction, is slightly widened. That is because the c- direction regrows at a slight angle, distorting the alignment mark in that direction. However, the cross-bar that is parallel to the a-direction grows inward at a relatively constant rate. The degree of misalignment for the 3µm regrowth was approximately 1.5µm. To resolve this, I included a dielectric hard mask surrounding the alignment mark that prevented any GaN growth, seen in Figure 2.2 (c). After regrowth, seen in Figure 2.2 (d), the hard mask is covered by roughened poly-GaN that can be removed by RIE etching, seen in Figure 2.2 (e). While this added process minimized the misalignment due to regrowth, it added several processing steps that are only necessary for certain regrowth conditions and substrate orientations. If, for example, the regrowth was relatively thin, ~300nm, then the added misalignment would only be ~150nm. This is smaller than Heidelberg's alignment tolerance (500nm), so protection is likely unnecessary.

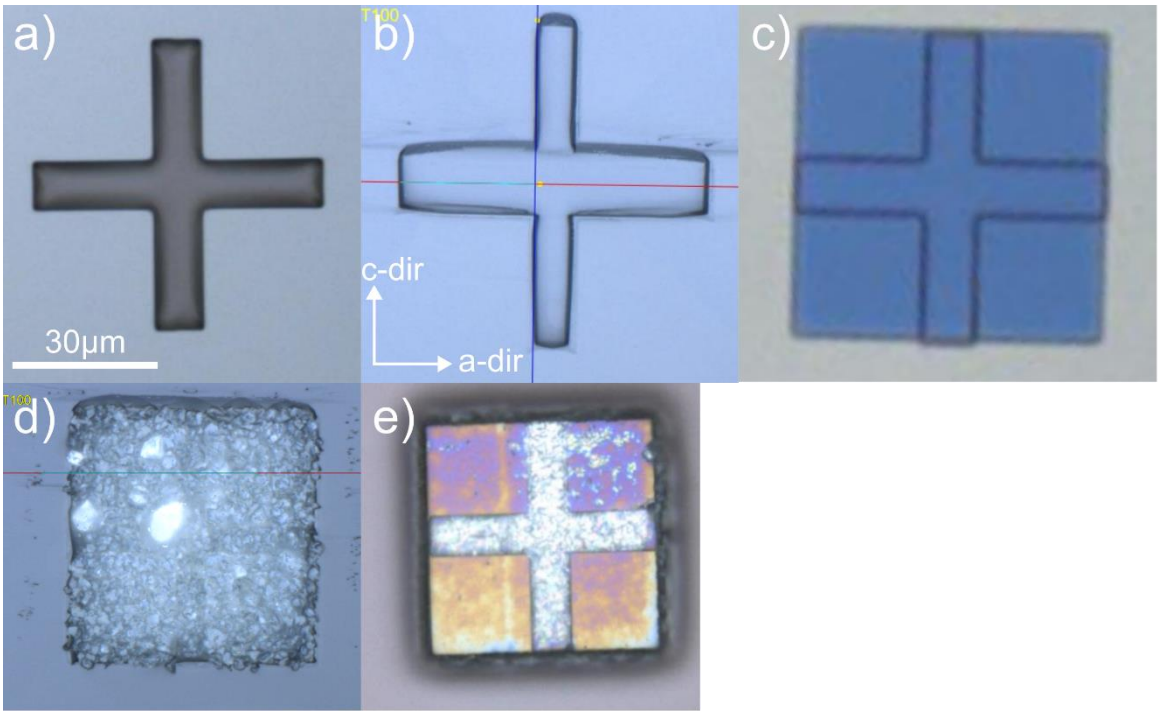

Figure 2.2. Optical microscopy image of (a) photoresist mask pattern, (b) mask pattern after exposure to lens MOCVD regrowth. Note the deviation from the optimal mask shape after regrowth. (c) Alignment mark covered by square SiO_2 pattern. (d) alignment mark after MOCVD regrowth covered in poly-GaN. (e) alignment mark and SiO_2 mask after 45min RIE etch.

After this, the BTJ pattern is defined, and BTJ apertures are etched in RIE using $SiCl_4/Ar/BCl_3$. This etch chemistry was chosen because of its low, controllable etch rate of approximately 18nm/min. Here, the BTJ etch depth is much more important, as the target etch depth is small, ~30nm, and the margin for error is lower. The relevant process step can be seen in Figure 2.3.

Following the BTJ etch, the samples are cleaned with a piranha solution (3:1 H_2SO_4:H_2O_2) for 15min to remove remaining photoresist scum, followed by a 2-cycle loop of 10min UV ozone and 2min concentrated HF. Then, the BTJs are activated at 720 °C for 20min. Finally, the long n-GaN regrowth is performed via MOCVD.

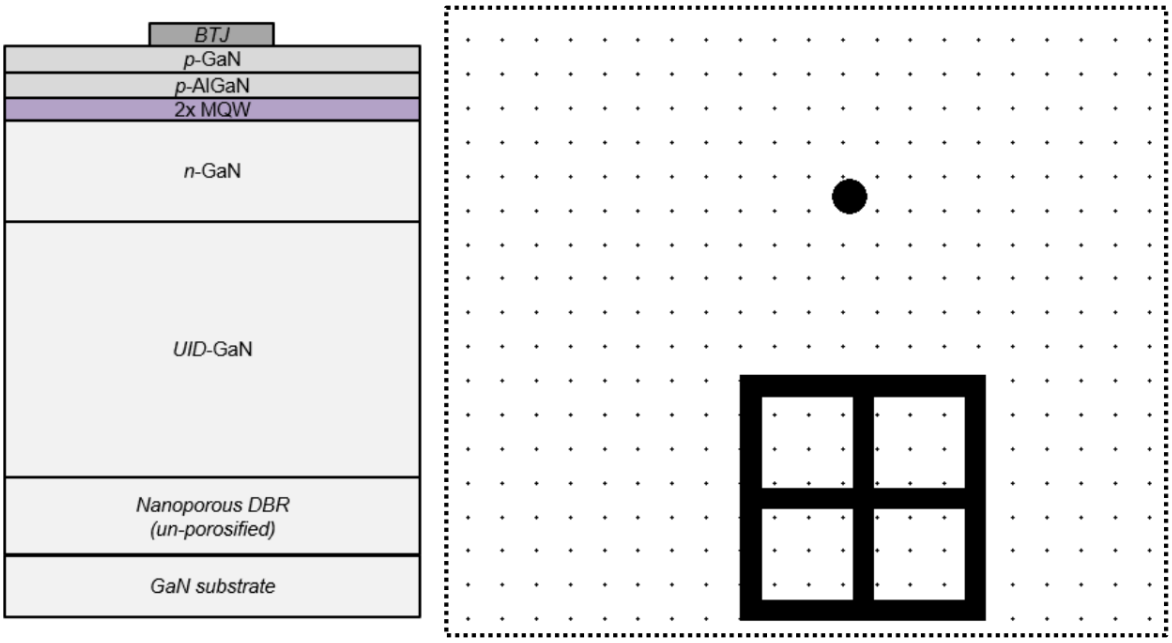

Figure 2.3. (Left) Schematic illustration of device after BTJ RIE etch. (Right) Image of mask showing BTJ aperture.

Before continuing the process, the issue of photoresist scum on regrowth quality will be discussed. During early iterations of this VCSEL process, we often noticed that after the final regrowth, there were serious morphology issues across the surface with a repeating pattern that corresponded to the BTJ apertures. An example SEM image can be seen in Figure

2.4 (a) of a particular die post regrowth. Zooming in, the regrowth showed crystalline facets surrounding a central opening, as can be seen in Figure 2.4 (b). While it was expected that the regrowth would not fully planarize, the n-GaN was expected to coalesce on top of the BTJ apertures. It was apparent that something was disrupting the coalescence above the BTJ. We initially suspected the regrowth condition but found no obvious dependence on the regrowth

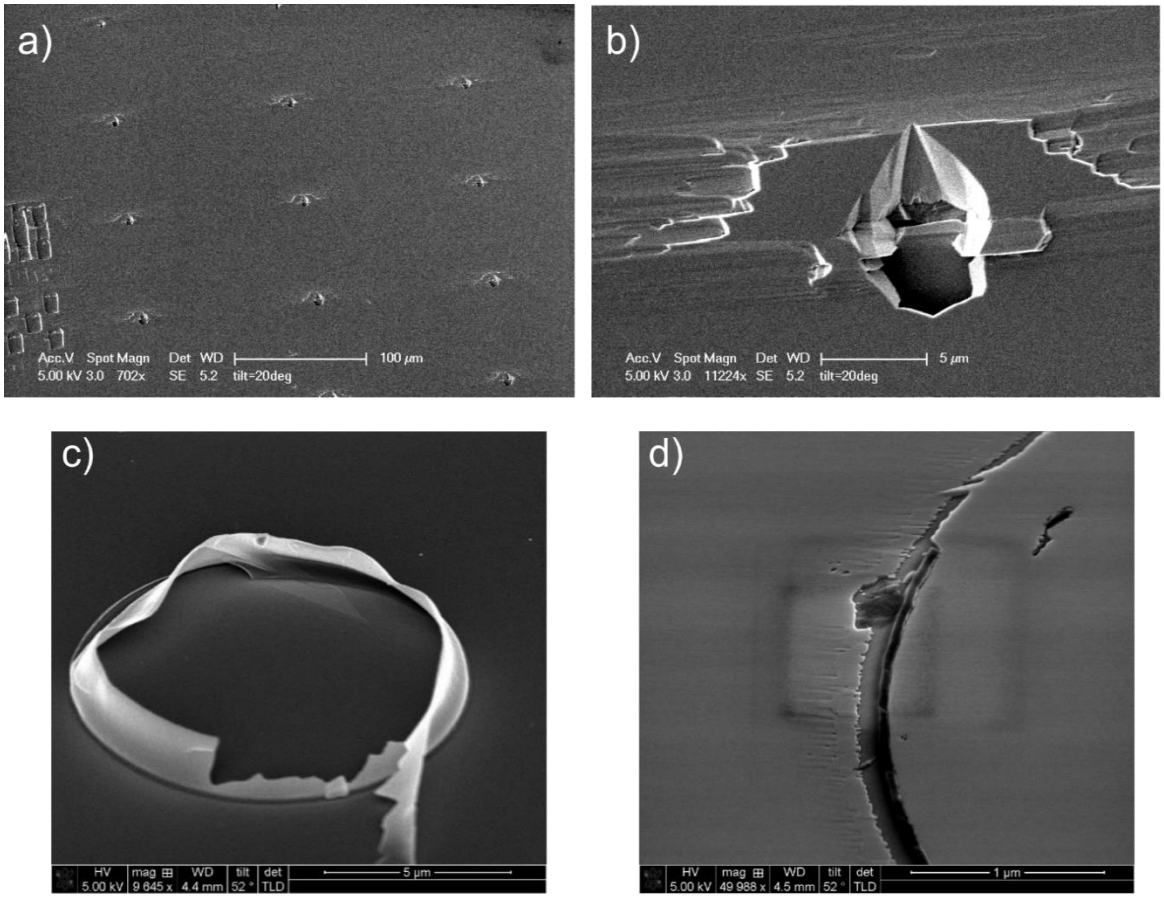

Figure 2.4. SEM image of a VCSEL sample after regrowth. (b) Magnified SEM image of regrowth issue. (c) SEM of BTJ aperture directly following the RIE etch. After cleaning, the BTJ aperture appears to be free of residue (not shown). (e) SEM image of the edge of a BTJ aperture after a 50nm regrowth in MOCVD.

condition with the appearance of this anomalous growth. Eventually, attention was turned to the BTJ etch and cleaning process. Figure 2.4 (c) shows an SEM image of a BTJ aperture directly after the RIE etch. A thin white film can be seen around the diameter of the aperture. The exact composition of this film is unknown, but it is believed to be a mix of organic

photoresist residue, back-sputtered Ga, and potentially Si-Ga-photoresist composite material. Originally, our cleaning process consisted of n-methyl-2-pyrrolidone (NMP) and buffered HF to remove the photoresist and scum.

After 10min in each solution, the film was no longer visible. However, as can be seen in Figure 2.4 (d), after loading a test BTJ sample into MOCVD and performing a 50nm regrowth, a black substance can be seen around the BTJ aperture and the regrowth surface on top of and directly next to the aperture is roughened. This black residue is likely photoresist scum that carbonized under the high regrowth temperatures of MOCVD and disrupted the coalescence of the two growth fronts. We were able to reduce this issue by modifying the post-BTJ etch cleaning process, including adding the piranha etch, and swapping buffered HF for concentrated HF. However, it was very difficult to completely suppress this regrowth issue. Recently, some colleagues have found success with AZ 300T stripper in conjunction with the other cleaning steps.

After the regrowth, the next photolithography step is the curved lens etch. The process is shown below in Figure 2.5. The lens formation is covered in more detail in Section 2.3. In brief, the sample is patterned with a photoresist cylinder with a diameter matching the desired lens diameter. Then, the photoresist is subject to a temperature above its glass transition temperature, 135 °C bake for 120s. This bake makes the cylinder reflow into a droplet with a radius-of-curvature that is based on width and height of the photoresist. Many different types

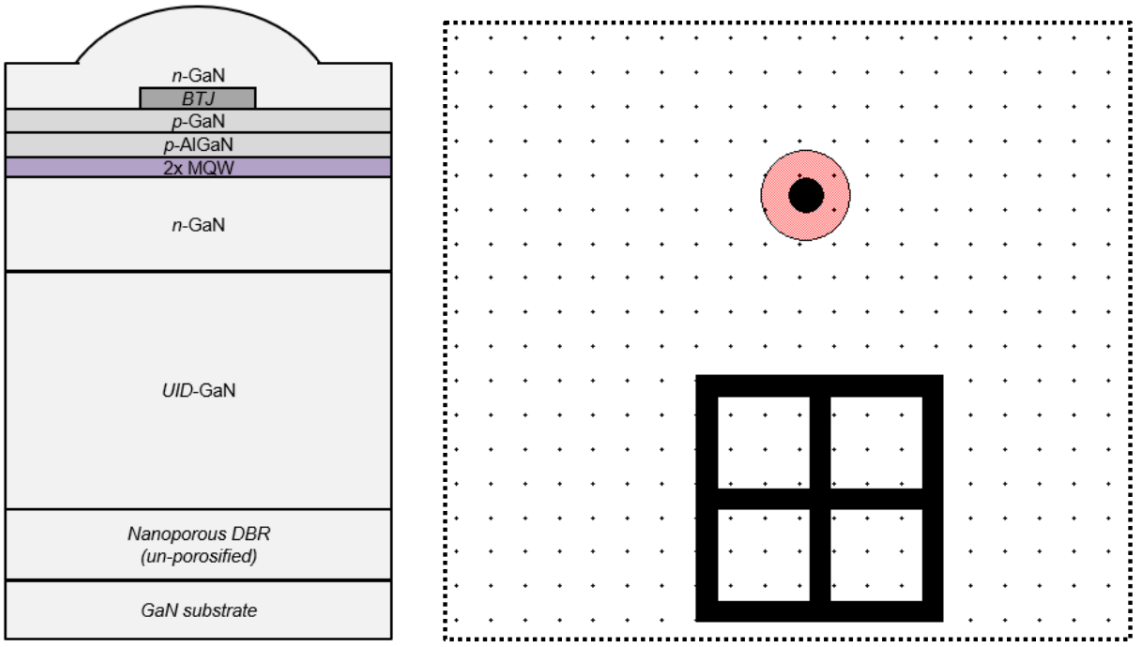

Figure 2.5. (Left) Schematic illustration of VCSEL after ICP lens etch. (Right) Mask view after lens etch.

of photoresists can make lenses but note that the optimal etch condition will vary for each one. After reflow, the lens is projected into the top n-GaN surface using an inductively-coupled plasma (ICP) dry etch in Cl_2 and O_2. It was found that RIE is a poor choice of dry etch when forming a curved lens, as the etch had a high tendency to flatten the photoresist lens and project the distorted shape into the GaN. The exact mechanism here is unknown but suffice to say that curved shapes etch better in ICP. Additionally, it is difficult to maintain a 1:1 etch ratio between GaN:photoresist due to the extreme difference in material properties. Generally,

the etch rate of the photoresist will be higher, and attainable etch ratios were around 1:1.4. A deviation from the 1:1 etch ratios results in lens shapes that are non-parabolic, and can even create non-uniform curvature profiles across the lens[151]. This may affect the mode structure or prevent lasing entirely, depending on the overlap between the spatial mode with structural non-uniformities. This can be solved by ensuring that the lens profile is close to the ideal shape near the region where the mode is expected to be. For me, I ensured that the top lens profile was close to the optimal condition out to a distance of approximately 5μm from the center, as a majority of the mode was contained within this.

When etching the lens, it is very important that the photoresist lens is entirely consumed during the etch process. Any leftover photoresist will always be at the very top of the lens. If it is removed prematurely, the lens will have a flat top and be of no use. To check if there is any leftover photoresist at the top of the lens, laser confocal microscopy or optical microscopy can be used to study the top of the lens. If using laser confocal microscopy, slowly raster the laser z-position through the lens. Near the tip of the lens, interference fringes should appear if there is some leftover photoresist. If using optical microscopy, search for a color contrast near the tip of the lens. If unsure, compare the profile of lenses near the center of the sample with lens profiles near the edge of the sample; generally, photoresist is thicker at the edge of the sample and so there is a higher likelihood of leftover photoresist. If it is determined that there is remaining photoresist, then the sample should be re-loaded and etched for additional time until the photoresist is consumed. This is a suboptimal solution, as the photoresist will etch at a slightly different rate and leave a discontinuity in the lens due to the rapid change in etch rate. However, a suboptimal VCSEL is better than a dead one.

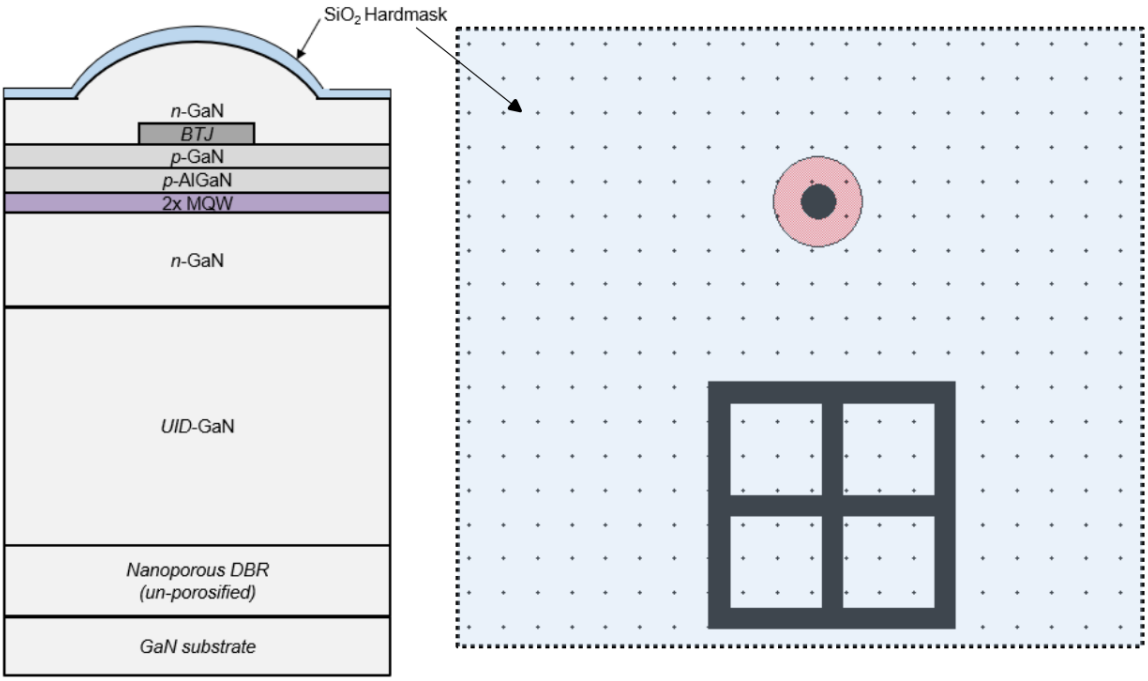

Figure 2.6. (Left) Schematic illustration of VCSEL after deposition of SiO_2 hard mask. (Right) Mask view.

Before continuing the process, a SiO_2 hard mask is deposited across the entire sample using plasma enhanced chemical vapor deposition (PECVD). The point of the hard mask is to protect the lens from getting damaged in the upcoming dry etch steps that form the mesa and NP DBR trench. The required thickness of the SiO_2 hard mask can be estimated by taking the approximate etch times required for the mesa and trench etch and multiplying them by the approximate etch rate for PECVD-deposited SiO_2. Generally, that thickness comes out to approximately 1,000nm. Of course, the photoresist pattern will be consumed first, so this is an upper limit and the most conservative approach. In principle, any dielectric can be used as a hard mask, but PECVD-deposited SiO_2 provided the optimal blend of: high etch selectivity with GaN (GaN:PECVD SiO_2 ~7:1), high deposition rate, decent film density, and high wet etch rate in BHF. If using PECVD, make sure to take out the sample after every 300nm SiO_2 deposition and dip in DI water to reduce the propagation of defects through the film.

Next, the mesa was etched, as can be seen in Figure 2.7. The central square shape surrounding the BTJ and lens is the p-mesa, whereas the adjacent square shape denoted the n-mesa that will be etched in the following step.

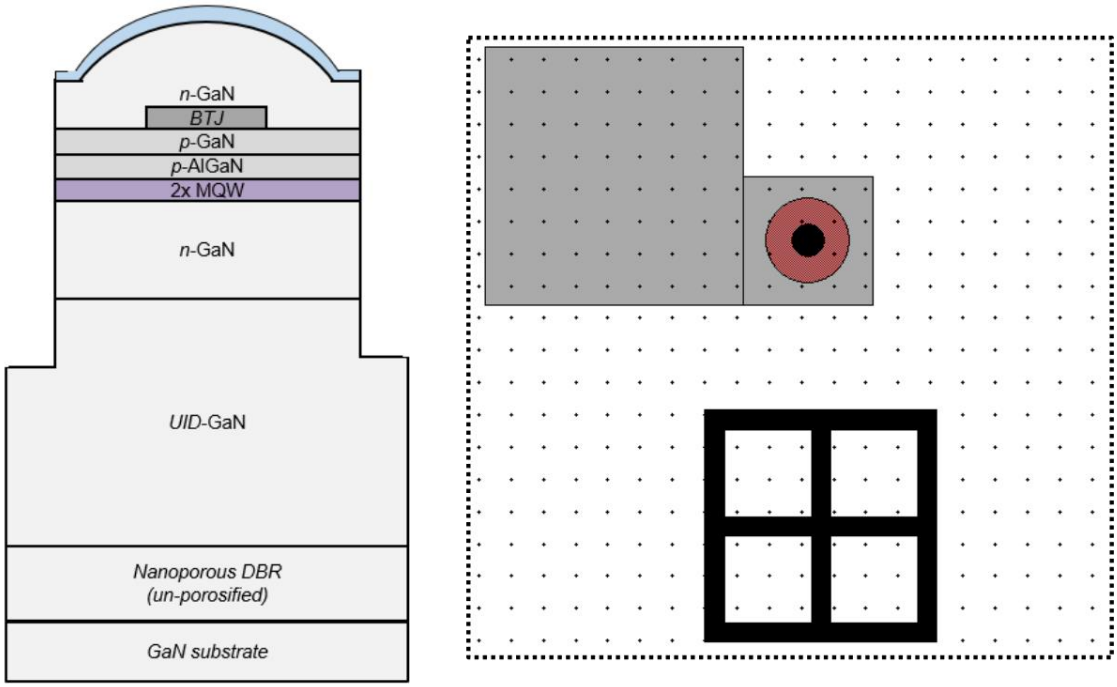

Figure 2.7. (Left) Schematic illustration of VCSEL after ICP mesa etch. (Right) Mask view after mesa etch.

The etch depth for the mesa is set to be 250-500nm deeper than the base of the bottom n-GaN layer. The purpose of the mesa is to expose the sidewalls for lateral hydrogen diffusion from the BTJ during thermal activation, and to set up the doped epitaxial layers for isolation from the nanoporous electrochemical etch. A p-mesa diameter of 40μm was chosen because this was expected to provide a low penalty to lateral heat dissipation[152] while minimizing the path length for lateral hydrogen diffusion during the BTJ activation[107]. For the topside GaN lens VCSEL, the etch depth of the mesa is approximately 4,000nm. The etch is performed in ICP with a Cl_2/N_2 mixture, and GaN etch rates as high as 500nm/min are attainable.

Following the mesa etch is the trench etch. The purpose of the trench etch is to expose the sidewall of the DBR layers for the upcoming porosification etch. The depth of the etch

should be carefully calibrated, and the required etch depth is approximately the cavity length minus the mesa etch depth and lens etch depth from previous steps. For the long cavity GaN lens VCSEL, the required etch depth was approximately 5,000nm, and the etch was performed using the same ICP condition as the mesa. For the trench, it is important to overshoot the trench relative to undershooting. An example of what happens when the trench etch depth is not properly calibrated is discussed in Section 4.2.1, but essentially the porous etch proceeds non-uniformly and can affect device performance.

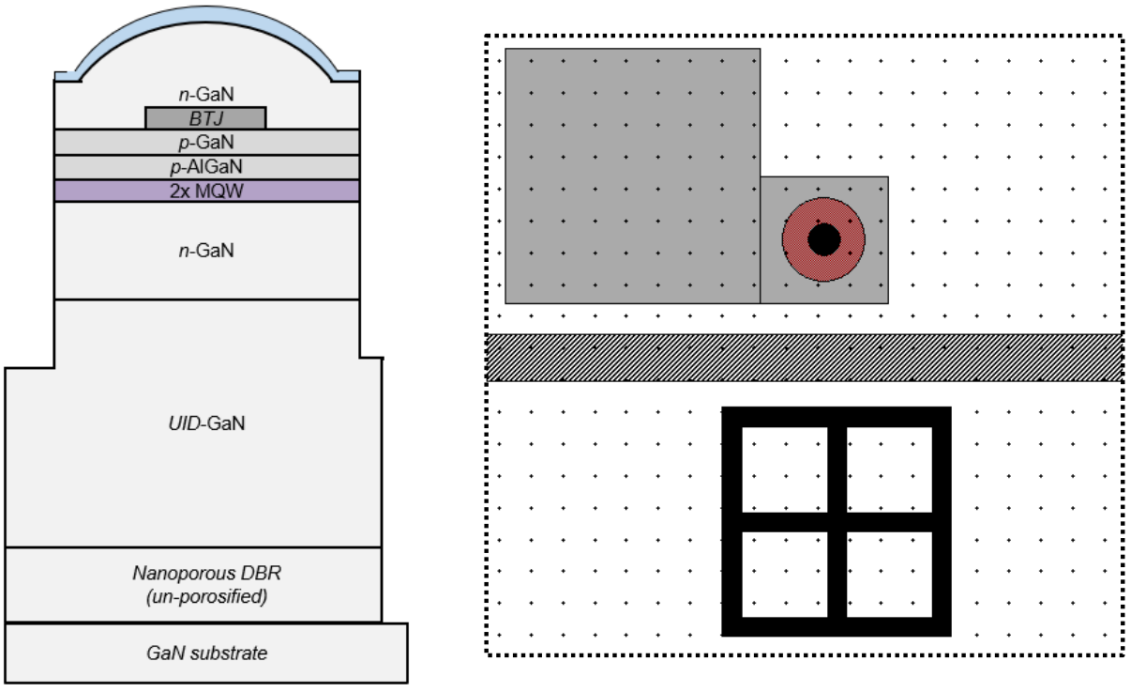

Figure 2.8. (Left) Schematic illustration of VCSEL after ICP trench etch. (Right) Mask view after trench etch.

Next up is the n-contact etch. This etch creates the n-mesa by exposing the bottom n-GaN. This etch is done in RIE using Cl_2, as the etch rate is more controllable. If this etch goes past the n-GaN into the UID GaN, then there will be a significant voltage penalty introduced. If possible, it is ideal to have several hundred nanometers of n-GaN beneath the n-mesa for optimal spreading. However, it can be difficult to precisely control this due to difficulties in predicting growth fluctuations, and precisely controlling the GaN lens etch. The margin of

error can be made larger by extending the thickness of the n-GaN region, at the expense of increased absorption loss from the dopants.

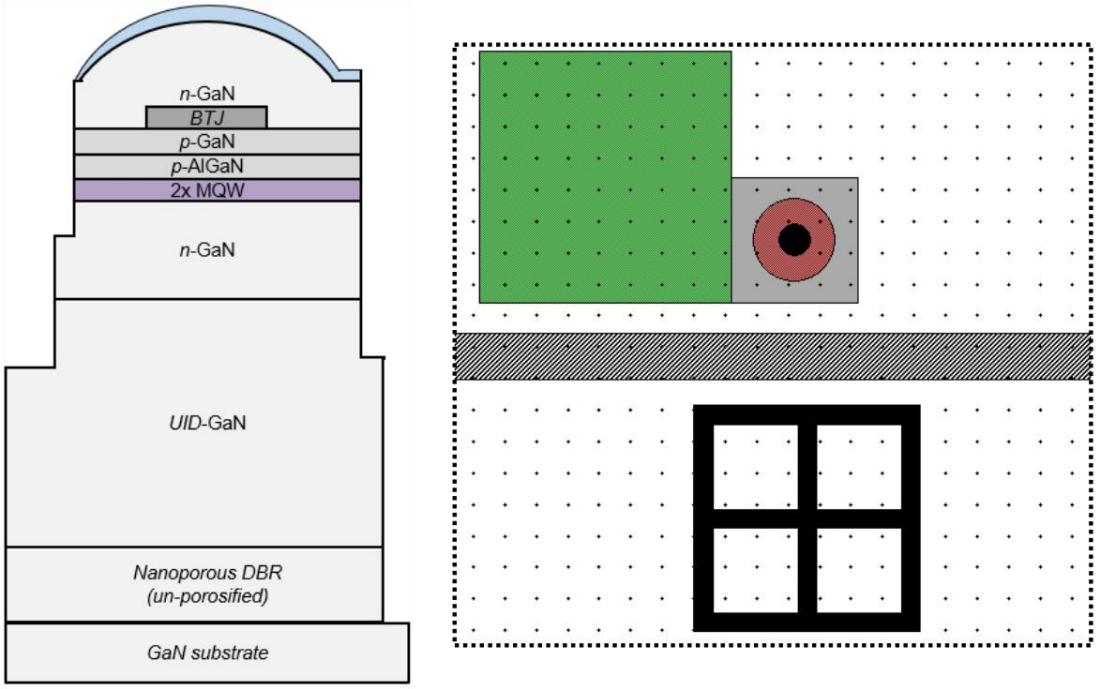

Figure 2.9. (Left) Schematic illustration of VCSEL after RIE n-contact etch. (Right) mask view.

Next, the BTJ apertures are thermally activated using the rapid thermal annealer. The anneal condition is 730 °C for 30min in a 1:1 N_2:O_2 environment. After, atomic layer deposition (ALD) is performed to conformally deposit 25-30nm SiO_2 across the entire sample. Early iterations of the VCSEL design used sputter-deposited SiO_2 to attempt to protect the sidewalls, taking inspiration from previous demonstrations[102]. However, due to the much larger 4,000nm tall mesas required for our process, sputter deposition was not conformal enough to adequately coat the sidewalls and protect the mesa from unintentional etching. More details can be found in Section 2.2. The advantage of ALD-deposited SiO_2 is that it is highly conformal, able to coat high aspect ratio structures like our mesas[153]. However, the ALD film also covers the sidewall, preventing the porous etch from working properly. Therefore, The

trench etch lithography step is repeated, protecting the device structure with photoresist, and a 30s BHF dip re-exposes the sidewall. Both steps are shown in Figure 2.10 below.

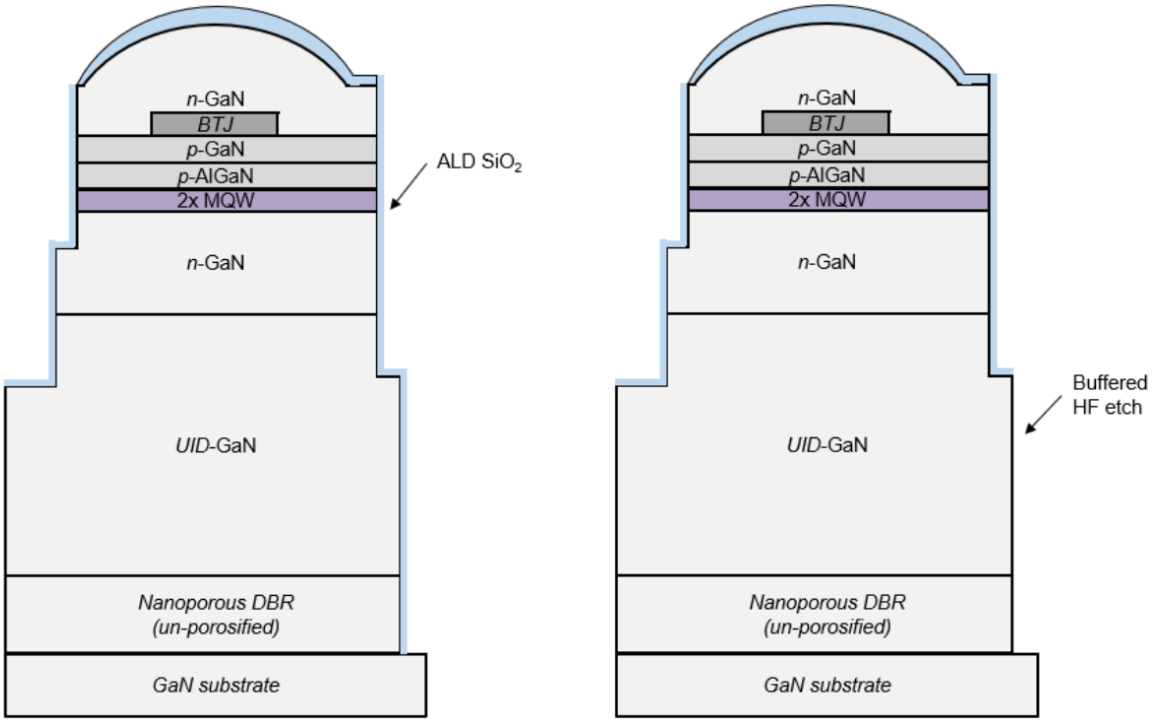

Figure 2.10. (Left) Schematic illustration of VCSEL after ALD SiO_2 deposition, and (Right) after BHF dip using the trench photolithography condition as mask.

Next, the sample is flipped over and Ti/Au 10nm/550nm is deposited via electron beam evaporation, as can be seen with Figure 2.11 below. The backside metal facilitates electrical contact with the NP DBR etch setup. Since the metal will need to be removed after porosification due to the devices being bottomside emitting, the Ti thickness is kept to a minimum to enable liftoff. Note that the porous structure will be destroyed in aqua regia, so it cannot be used. In fact, after the porous etch is performed, the sample cannot be subject to sonication or solutions with vigorous bubbling, or else the porous structure will be destroyed. Following metal deposition, the calibration sample is loaded into the NP DBR etch setup, and the NP DBR is porosified. The goal with the NP DBR calibration is to determine the approximate position of the stopband of the DBR and measure its reflectivity across the

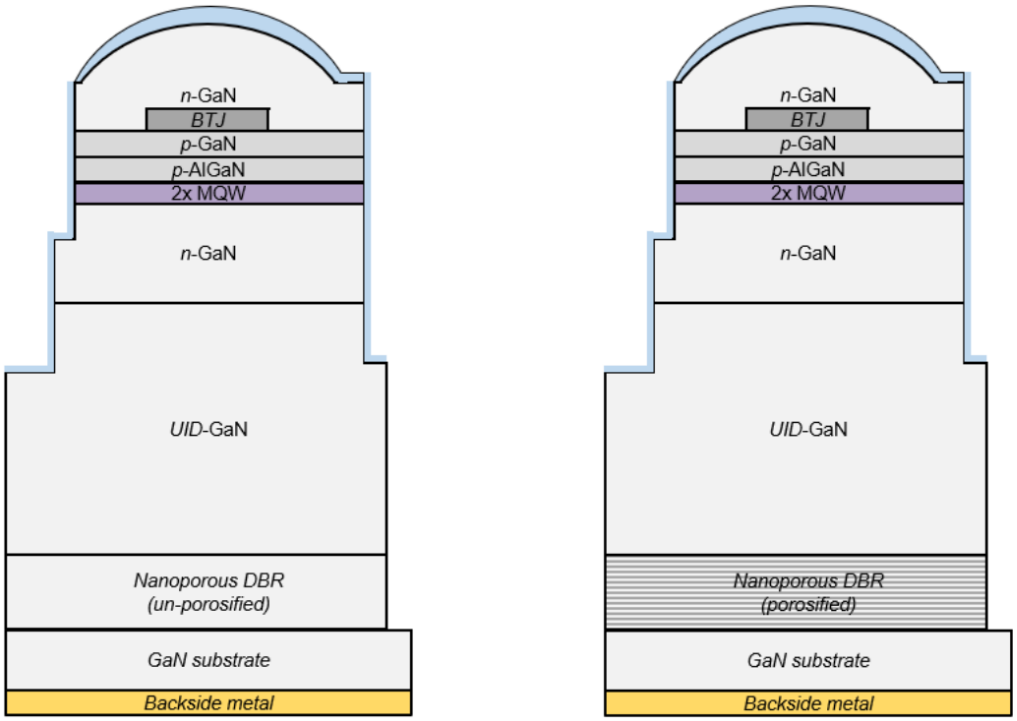

Figure 2.11. (Left) Schematic illustration of VCSEL after backside metal deposition, and (Right) after nanoporous electrochemical etch.

substrate surface. If needed, cross-sectional SEM images can be taken of the calibration DBR sample to determine if the applied voltage is yielding the expected porosity. There are a variety of reasons that the porosity can change run-to-run, including shifts in the n+-GaN doping due to reactor drift, changes in the conductivity between different batches of commercial bulk GaN substrates, changes in the surface profile of the trench sidewall due to the etch condition, etc. We also found that once porous etching was started at a certain voltage setting, it was only possible to reduce the applied voltage to decrease the porosity. When the voltage was increased, the porous structure was destroyed. Therefore, the real purpose of the NP DBR calibration sample was to ascertain the upper voltage limit for optimal pore formation. More details are available in Section 2.2.

Once the porosification etch is completed, the sample is removed from the etch setup and the backside metal is removed by placing the metal face onto a piece of Kapton tape. The next

photolithography step is the contact accessibility step. Currently, the entire sample surface outside of the trenches is covered by a dielectric material, either PECVD-deposited SiO_2, ALD-deposited SiO_2, or both. To finish the device fabrication process, both the optical cavity and metal contact regions need to be cleared of dielectric material. To that end, this step involves patterning followed by a BHF dip to remove the dielectric. The resulting device profile and pattern can be seen in Figure 2.12.

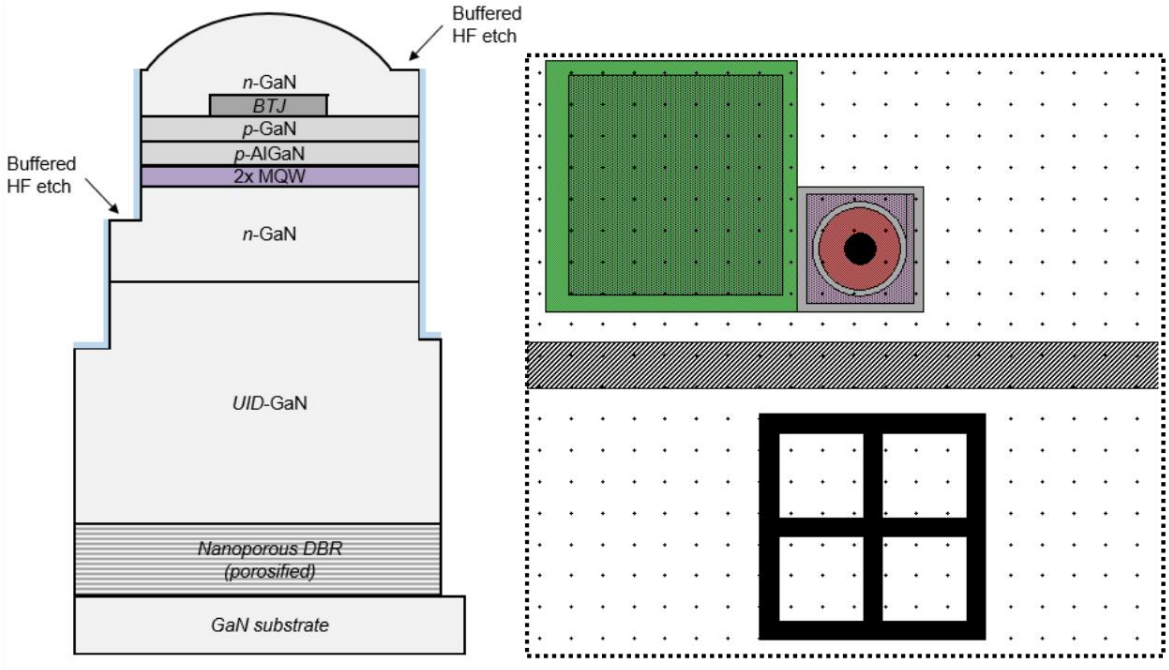

Figure 2.12. (Left) Schematic illustration of VCSEL after wet etch removal of SiO_2 around lens and contact regions. (Right) mask view.

Once this step is complete, there are two open regions for metal to make electrical contact with the sample, one on the p-mesa and one on the n-mesa. Note that a majority of the metal contacting the p-side will be off the p-mesa but on top of SiO_2, highlighting the multi-functional utility of the SiO_2 layers as hard mask, electrochemical isolation, and electrical isolation. Synergy.

The next lithography step is to deposit the p-DBR, a 16-period SiO_2/Ta_2O_5 dielectric superlattice, via ion beam deposition, as shown in Figure 2.13. The p-DBR consists of quarter-

wavelength-thick alternating layers of SiO_2 and Ta_2O_5 with respective thicknesses of 69.2nm and 46.6nm, assuming $n_{SiO2} \sim 1.48$ and $n_{Ta2O5} \sim 2.2$ at $\lambda = 410$nm. Prior to DBR deposition, the optical growth rates of the SiO_2 and Ta_2O_5 films need to be properly calibrated to ensure a high peak reflectivity of the final DBR. This is accomplished by first depositing single layers of SiO_2 and Ta_2O_5 onto Si wafers and using ellipsometry to calculate the approximate IBD

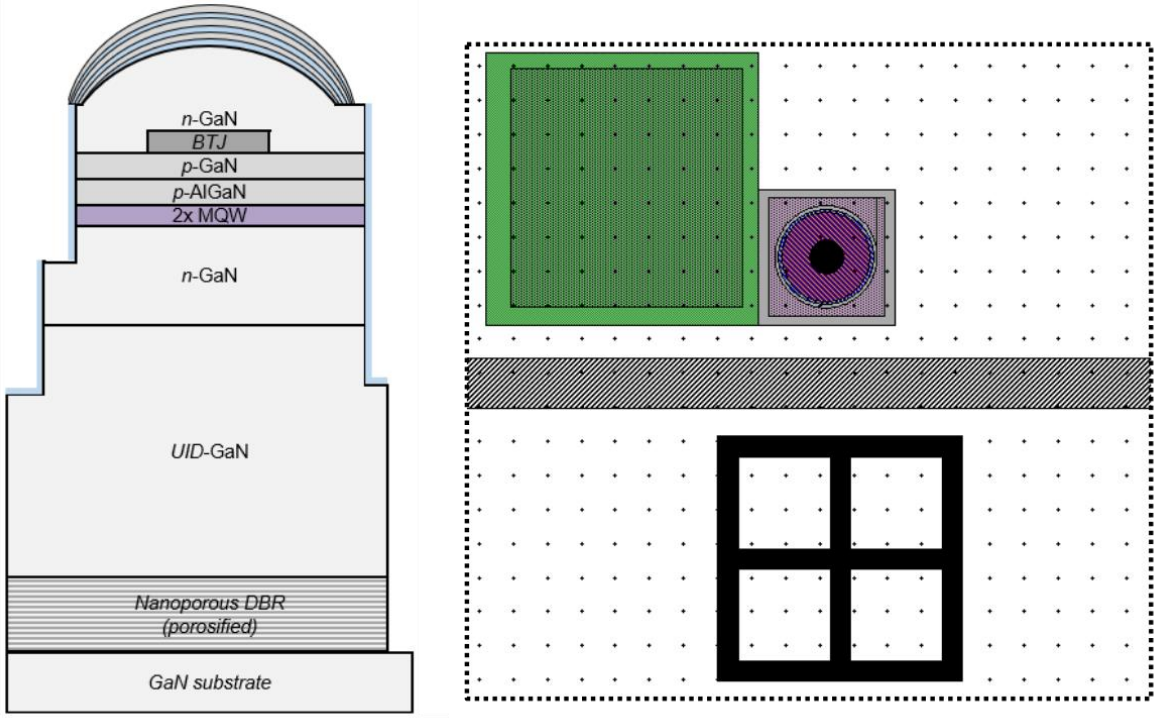

Figure 2.13. (Left) Schematic illustration of VCSEL after p-DBR deposition. (Right) mask view.

deposition rates. Then, a series of SiO_2/Ta_2O_5-based Fabry-Perot cavities are deposited on sapphire wafers and a UV-Vis spectrometer is used to measure the reflectance spectrum. Each Fabry-Perot cavity is comprised of four periods of dielectric sandwiching an extra quarter-wavelength-thick layer of SiO_2 or Ta_2O_5. The extra layer creates an optical cavity with a reflectance minimum that corresponds to the optical thickness of the deposited film. The reflectance nulls from a SiO_2 and a Ta_2O_5 Fabry-Perot cavity can be used to correctly adjust

the independent growth rates of the SiO_2 and Ta_2O_5 deposition condition. For more information on this, please read Section 4.4.2 in Charles Forman's thesis (UCSB, 2018).

Finally, the last step is to deposit the metal contacts. This design uses a common contact architecture, so both the n- and p-side contacts are deposited at the same time. The

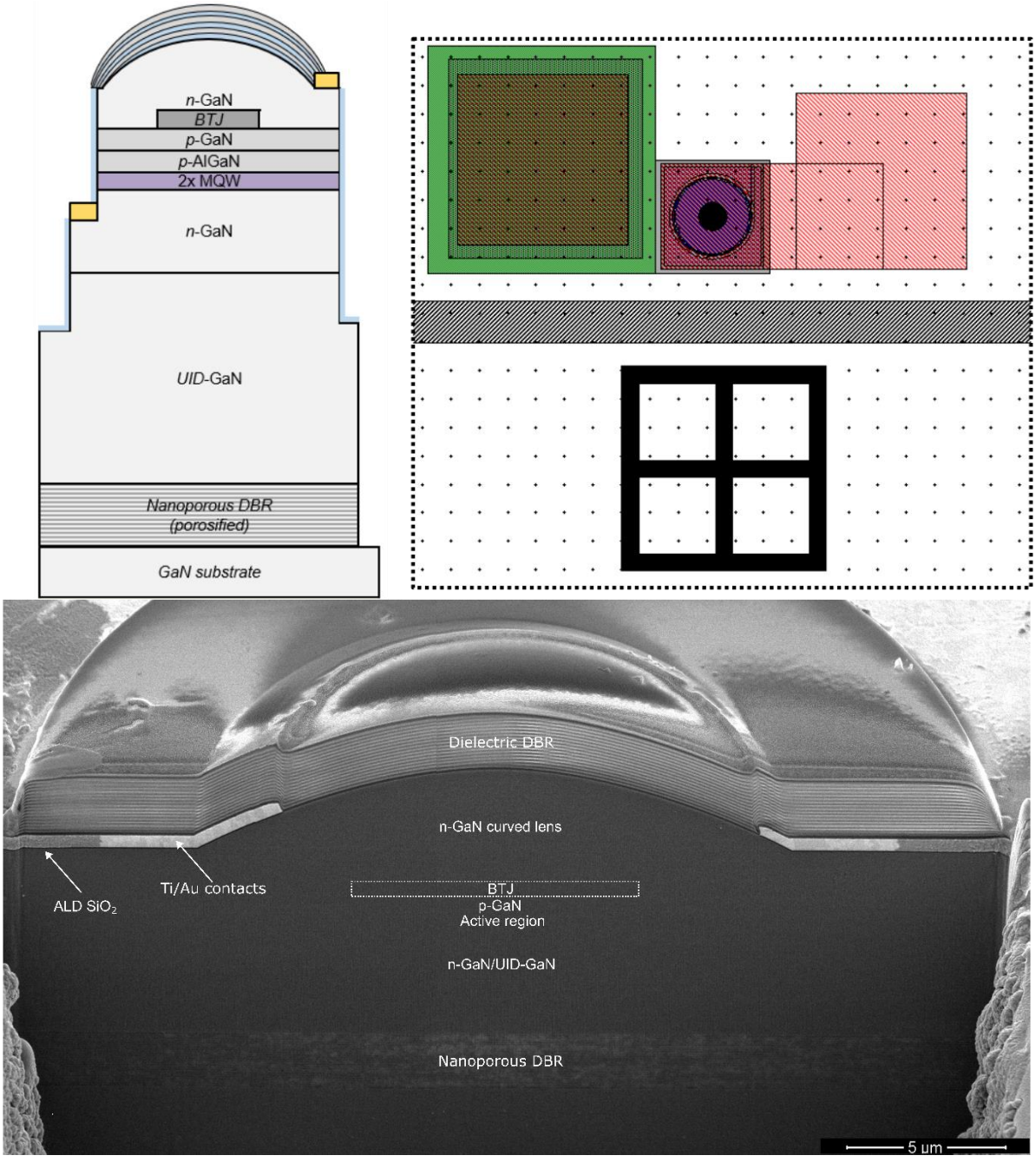

Figure 2.14. (Left) Schematic illustration of completed VCSEL after contact metal deposition. (Right) mask view of completed VCSEL. (Bottom) cross sectional SEM image of fabricated VCSEL.

metal is deposited using electron beam evaporation, and the metal deposited is Ti/Au 40nm/650nm. The final step is shown below.

After liftoff, the VCSELs are ready for testing! In Figure 2.14, a cross-section SEM image of a long cavity GaN VCSEL fabricated using the above process flow is shown. The photo was taken perpendicular to the a-direction.

2.2 Designing the Nanoporous GaN DBR

Nanoporous GaN DBRs (NP-DBRs) have shown promise in GaN VCSELs due to their lattice match to GaN, relative ease of growth and fabrication, and high refractive index contrast. The formation of NP-GaN has been studied extensively, and the mechanism of etching is well understood[154]. Electrochemical (EC) etching of GaN in oxalic acid is conductivity selective, meaning that at a given applied bias, the size and shape of pores is

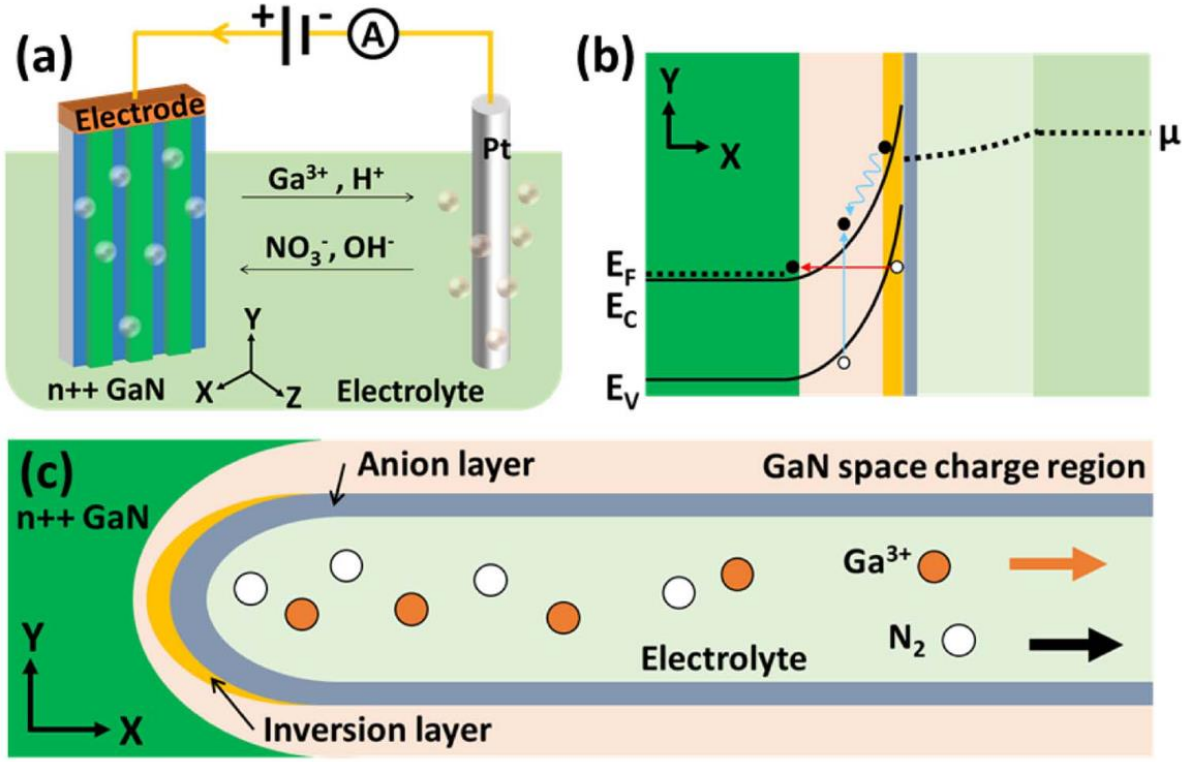

Figure 2.15. Schematic diagrams of GaN anodic etching. (a) Experiment setup of GaN electrochemical etching in nitric acid (HNO_3) electrolyte, with ion/mass transport denoted by arrows. Nitrogen and oxygen gases are generated near the anode and hydrogen gas at the cathode, denoted by bubbles. (b) Energy band diagram of the GaN/electrolyte interface. Electrons and holes are shown as small black and white circles at the conduction and the valence band, respectively. Holes generate at the inversion layer (orange) by either band-to-band tunneling (red arrow) or impact ionization (blue arrows). (c) Schematic cross-sectional image of a single nanopore structure. The nanopore structure is illustrated with full depletion approximation and consists of an anion layer, an inversion layer and a GaN space charge region. The anion layer is due a negative charge accumulation near the GaN/electrolyte interface caused by applied voltage bias. Within the GaN material, the positive charges are supplied by ionized dopants. Ga3+ ion and N2 gas are generated by the oxidation of GaN, and they transport away from the etching front driven by diffusion and electrolyte flow. Reproduced from ref 154 with permission from IOP Publishing (copyright 2018).

directly related to the n-type doping and the crystal orientation of the layers exposed to the solution. Figure 2.15 shows an overview of the chemical etch process in the case of nitric acid, HNO_3. For our process, oxalic acid, $C_2H_2O_4$, was utilized due to safety and handling concerns regarding HNO_3. During the etching reaction, four continuous processes occur: (1) the negative applied bias creates a hole inversion layer at the electrolyte/n-GaN interface, (2) the n-GaN surface is oxidized due to the presence of holes at the inverted surface, (3) oxidized GaN dissolves into Ga^{3+} and nitrogen gas products, which (4) migrate freely into the electrolyte, leaving behind mesoporous or nanoporous voids. The void size grows with applied voltage and is limited by the n-doping of the n-GaN layer, which determines the required depletion width of the formed hole inversion layers.

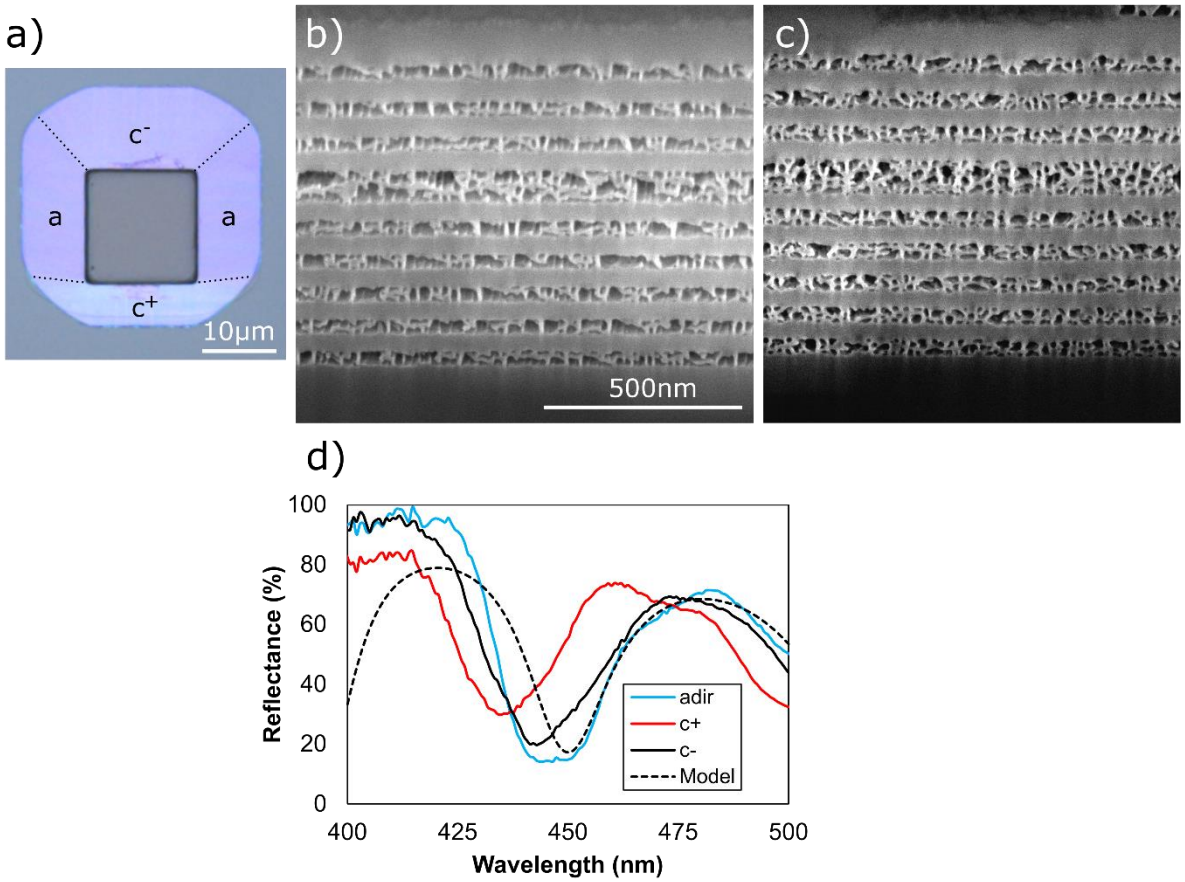

Figure 2.16. (a) Optical microscope image of nanoporous FP cavity after etching in oxalic acid. Cross sectional SEM images of FP cavity with pores aligned along (b) the a-direction and (c) c^--direction. (d) Reflectance of nanoporous FP cavities.

While etching in c-plane is spatially isotropic, for *m*-plane GaN the etch proceeds differently in the a- and c-directions. Fabry-Perot (FP) cavities were fabricated on single crystalline m-plane GaN substrates with a miscut of 1° in the [0001] direction to study the differences in etch behavior. The FP structure consisted of 4 periods of λ/4 UID-GaN/n+-GaN surrounding a λ/2 layer of n+-GaN, with a design wavelength of 450nm. Figure 2.16 (a) shows a top-down optical microscope image of the completed Fabry-Perot structure after etching in oxalic acid. It can be seen that the etch proceeds uniformly along the a-direction, but differently along the c^+ and c^- directions, and that this applies to both the porosity (reflected by the change in color) and the etch rate. Figure 2.16 (b) and (c) shows cross-section SEM

images of a FP cavity etched along the a- and c⁻- direction, respectively. The porosity of the c⁻-direction FP is approximately 33%, and the pore structure is organized with only scatter macro voids throughout. By contrast, the FP cavity etched in the a-direction has a porosity of nearly 50% and is nearly electropolished, with a majority of the nanopores collapsed into voids. This behavior shifts the optical cavity length of the center λ/2 spacer, with the resonance wavelength of the FP moving from 436nm for the c⁻direction to 446nm for the a-direction. The shift is primarily due to a reduction in the refractive index of the spacer layer, which can be approximated using the volume average theory (VAT), where the porous GaN layer is assumed to form an "alloy" between GaN and air:

$$n_{por} \approx \sqrt{(1-\varphi)n_{GaN}^2 + \varphi n_{air}^2} \tag{2.1}$$

Here, φ is the porosity, n_{GaN}, and n_{air} are the refractive index of GaN and air, respectively[96]. Note that the resonance minimum for the a-direction is broader than the c+ and c⁻ FPs, indicating that the macro voids are causing scattering within the FP structure[155]. The dependence of scattering on pore size can be estimated using the following equation[96]

$$\frac{I_{scatter}}{I_0} = A\left(\frac{\pi d_{max}}{\lambda}\right)^4 \frac{\varphi}{\pi d_{avg}^2} \tag{2.2}$$

where the factor $\left(\frac{\pi d_{max}}{\lambda}\right)^4$ is the classic Rayleigh scattering dependence from a single scatterer, $\frac{\varphi}{\pi d_{avg}^2}$ describes the density of the scattering nanopores, and A is a fitting parameter. This equation is valid for the case when πd/λ is much less than 1. For our VCSEL structures, we chose to align the sidewalls parallel to the c-direction to ensure that the etch would proceed uniformly on both side of the trench and optimized the voltage for the a-direction with the goal of pore uniformity.

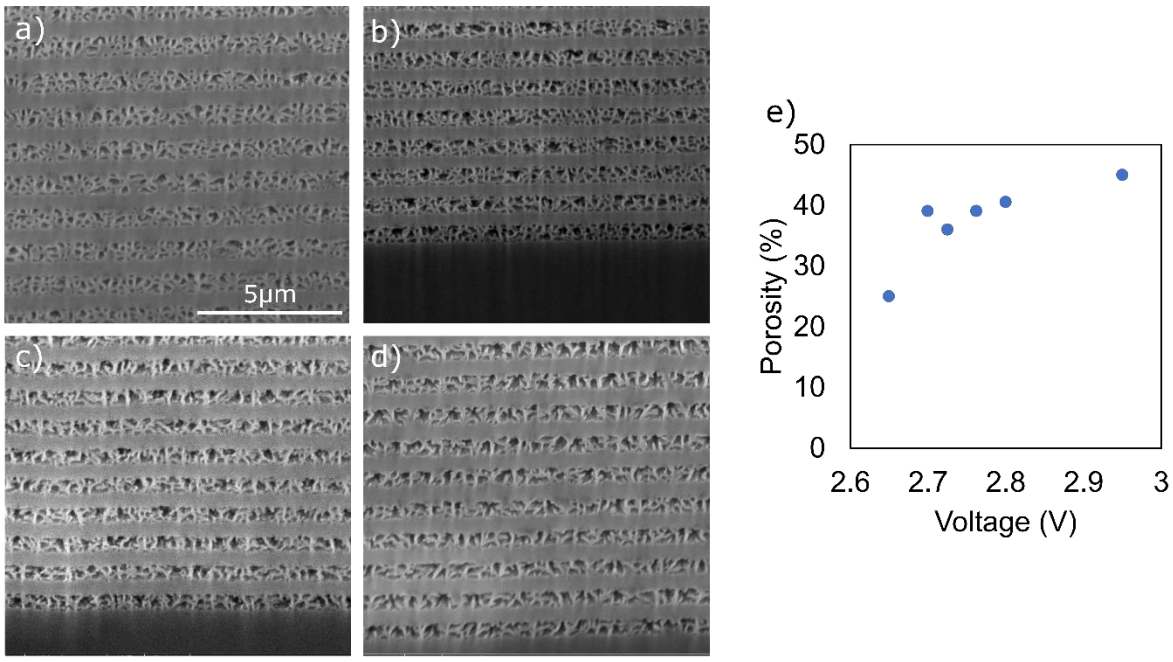

Figure 2.17. Cross-sectional SEM images taken perpendicular to the etch interface of NP DBRs etched at a voltage of (a) 2.5V, (b) 2.65V, (c) 2.8V, (d) 2.95V. (e) plot of porosity versus applied voltage.

Figure 2.17 (a-d) shows various m-plane NP-DBRs etched at UCSB for different voltages along the a-direction, [Si]~$5x10^{19}cm^{-3}$. Figure 2.17 (e) shows the relationship between applied bias and porosity and pore size. The porosity of each NP DBR was extracted by binarizing the cross-sectional SEM images and calculating the porous fraction from the known thicknesses of the individual layers. For the current etch setup at UCSB, porosity levels off with increasing voltage, but average pore size grows rapidly as small pores combine into larger voids. The ratio between the size of the pores and the surrounding walls is determined by the depletion width between the surrounding n-GaN and the inverted hole tip. At a given doping and voltage, charge equilibrium is reached between the depleted sidewalls and hole-rich pore center, influencing pores to etch in a unified direction. As the voltage increases, the depletion region between neighboring pores decreases, until the sidewalls collapse and the nanopores become a large void. These voids can increase scattering loss from the NP-DBR[156], and so the etch voltage is chosen to minimize the presence of macro-voids. To consistently match the

NP-DBR stopband to the active region emission, several substeps were added to the process flow, including same-day XRD growth rate calibrations of the NP-DBR layers, Ti/Au backside coating prior to the etch to increase spreading and minimize variation in the contact resistance between the substrate and test fixture, and a two-step etch process that allows for analysis of the etch in-progress. Figure 2.18 shows an optimized NP-DBR compared to a 1D transmission matrix model, where the refractive index (n_{por}) of the porous layer is calculated using VAT. The optimal condition was determined to be 33-35%, which maximized the index

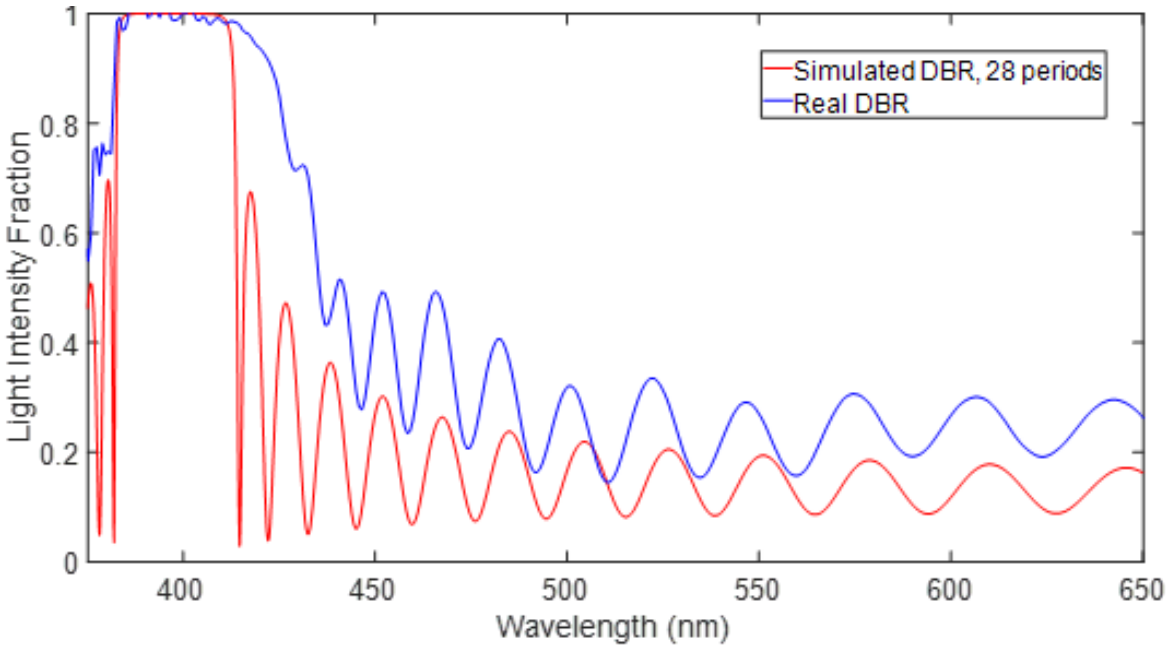

Figure 2.18. Optimized NP DBR structure compared to 1D transmission matrix model.

contrast and gave the widest stopband, while minimizing the generation of macro-voids. The maximum of the optimized porosity range yields an effective nanoporous refractive index as low as 2.094 at 410nm, leading to an index contrast of 0.41 (approximately double the index contrast of a lattice-matched AlInN/GaN layer) and a full-width half-percent max (FWHPM) of 26nm for a 22-period DBR.

2.2.1 Device Structure Considerations

There are several important design issues that need to be resolved when integrating the NP DBR etch into a full VCSEL process flow. The etch is selective in terms of n-doping, but for even low n-doping, some etching is inevitable. R. Anderson et. al. experienced this unintentional etching in their EELD with nanoporous cladding; unintentional etching into the n-GaN above the intentioned NP cladding modified the mode in unexpected ways, and introduced additional loss due to scattering from pores overlapped with the mode[157]. Similar issues were faced fabricating our initial VCSEL structures. When the device mesas were uncovered, the etch readily penetrated the mesa through the various n-GaN sublayers in the device. Coating with sputtered SiO_2 was proposed to encapsulate the mesas and has been utilized for previous VCSEL designs with NP DBRs[102]. However, the sidewall coverage proved unsuitable for the thick cavity design, which required a mesa sidewall height of over 4μm. Several deposition techniques were explored, and it was experimentally determined that atomic layer deposition (ALD) provided the necessary conformal coverage. Figure 3-5 (a) – (b) shows optical microscopy images of a mesa covered with 300nm sputtered SiO_2 (Figure 3-5 (a)) compared with 25nm SiO_2 deposited by ALD (Figure 3-5 (b)), after both samples were submerged in oxalic acid for 24 hours and held at a bias of 2.5V. The blue coloring in the image is the reflection from the bottomside NP DBR. Around the edge of the sputter SiO_2-coated mesa in Figure 2.19 (a), the foamy white regions indicate the presence of scattering pore structures within the mesa itself. The inset of Figure 2.19 (a) shows a nearby device where the porous etch penetrated all the way to the highly doped n+-GaN of the BTJ, fully electropolishing it. Figure 2.19 (c) – (d) show laser confocal microscopy images of the two sample sets, where in each image the laser depth of focus is placed within the device mesa.

The white contrast seen within the mesas in Figure 2.19 (c) corresponds to the foamy regions highlighted in Figure 2.19 (a). By contrast, the mesas in Figure 2.19 (d) that are covered by ALD SiO_2 show minimal discoloration, with the majority of mesas only faintly illuminated by unintentional reflection from the bottomside NP DBR. There is a small region visible on one mesa, indicating that the ALD coverage wasn't fully present. This issue may improve with improvements to substrate cleaning. The effectiveness of ALD SiO_2 is corroborated by Figure 2.19 (e) – (f), which show a cross section of each mesa taken using a focused ion beam (FIB) and imaged by scanning electron microscopy (SEM). It can be seen that the sputter SiO_2-covered mesa in Figure 2.19 (e) has significant unintentional porous etching in both of the top

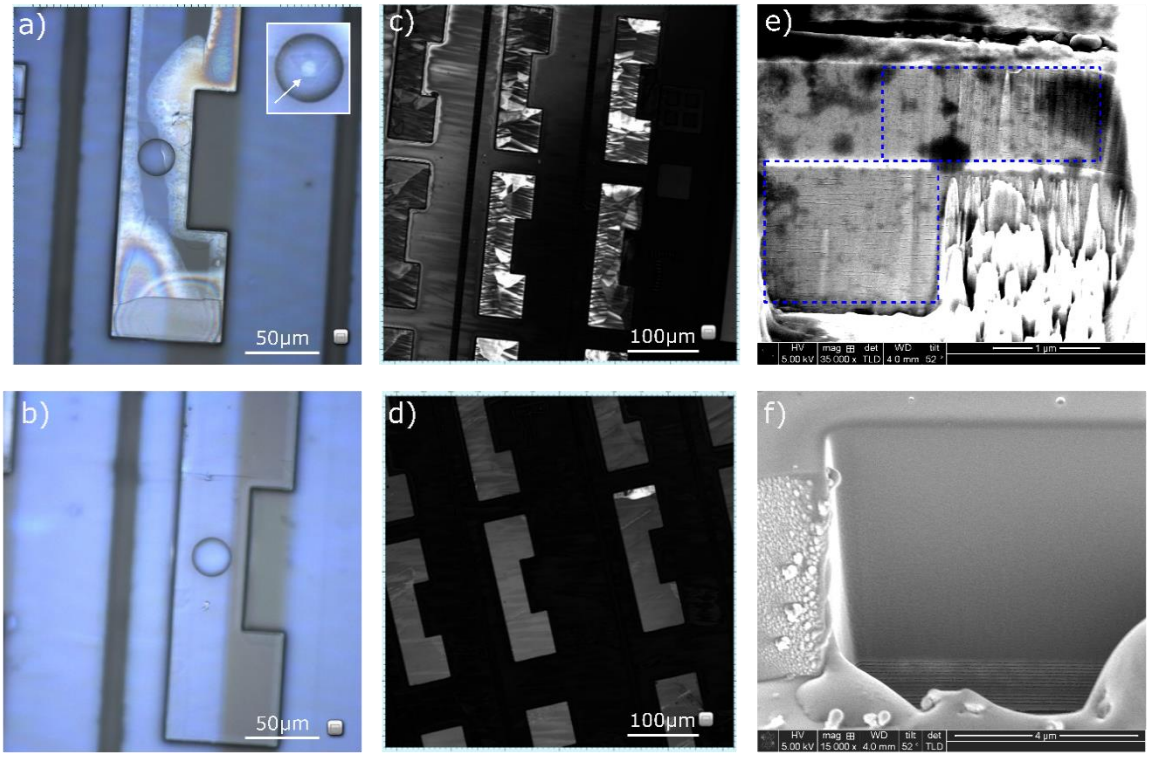

Figure 2.19. (a-b) Optical microscopy image of a VCSEL mesa coated with (a) 300nm sputter deposited SiO_2 or (b) 25nm ALD deposited SiO_2 after 24 hours of electrochemical etching in oxalic acid. The inset of (a) shows a nearby device where the BTJ has been electropolished, denoted by a white arrow. (c-d) laser confocal microscopy scans through device mesas with (c) sputter and (d) ALD deposited SiO_2. (e-f) Cross-sectional SEM image of mesa sidewalls coated with (e) sputtered SiO_2 with porosified n-GaN highlighted by a dotted blue outline, and (f) 25nm ALD SiO_2.

and bottom n-GaN regions, which both have an n-doping of approximately [Si] = 6×10^{18} cm^{-3}. By comparison, the ALD coated mesa, as shown in Figure 2.19 (f), has no visible pore penetration visible above the NP DBR. ALD coverage decreased visible pore penetration of mesas from ~85% down to ~10%, compared to sputter, ion beam deposition (IBD), and plasma-enhanced chemical vapor deposition (PECVD) SiO_2-coated samples. This is due to the ability of ALD to deposit uniformly along high aspect ratio structures, providing superior isolation to the mesa from the electrochemical etch[153].

In addition to modifying the isolation of active device layers, we also made improvements to the method by which the electrochemical etch proceeded. In our first nanoporous GaN efforts, we employed an etch setup that was similar to other groups pursuing III-nitride GaN[158,159]. Figure 2.20 (a) shows an overview of the method. In summary, the sample, which acts as the anode, is suspended over the electrolyte solution via a metal tweezer, and partially submerged. To ensure consistent electrical contact with the tweezer, indium metal is soldered to the back surface of the sample. The cathode, a Pt-wire, is submerged in the electrolyte

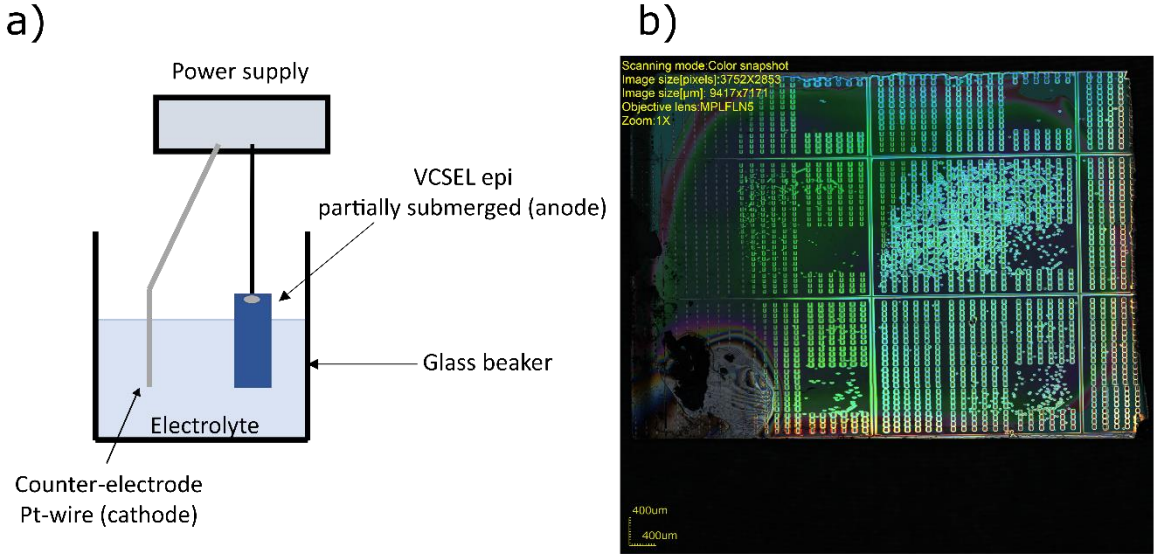

Figure 2.20. (a) Schematic of Tweezer etch setup. VCSEL is held by metal tweezer and partially submerged in electrolyte. (b) VCSEL sample etched using Tweezer method. Tweezer was attached to VCSEL on lower left side.

solution, and a bias is applied to facilitate the electrochemical etch. One disadvantage of this method is that the sample is only partially submerged into the electrolyte solution, since the electrical circuit will short and pores will not form if the tweezer makes contact with the solution. What this means in practice is that only a portion of the sample will receive the optimal EC etch, and yield is significantly reduced. Figure 2.20 (b) shows a VCSEL sample with a NP DBR etched using this method. On the left side, the NP etch did not proceed at all, due to the requirement that the tweezer, which was affixed to the left side, remain above the solution throughout the etch. Going to the right of the sample, it can be seen that both the porous etch rate and reflectivity of the etch NP DBR stopband shift across the wafer. Unfortunately, due to a processing issue in the center of the sample, the usable yield of devices after the NP etch was quite low.

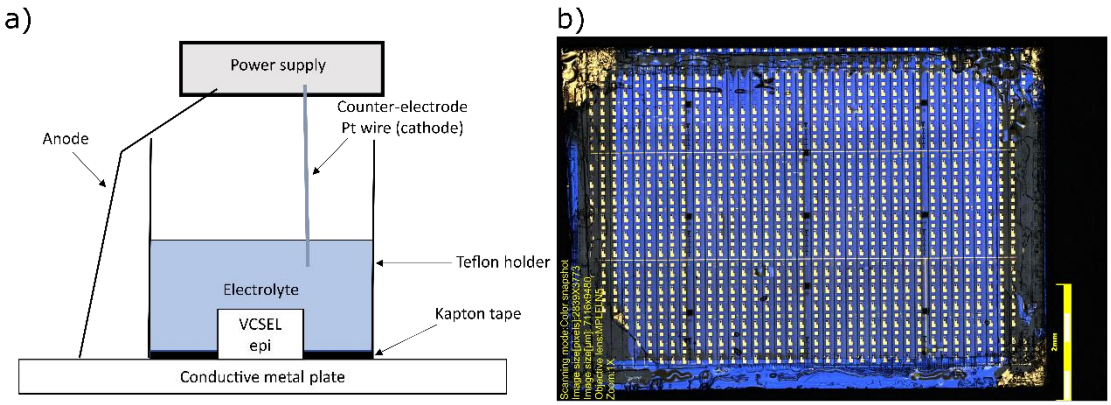

Figure 2.21. (a) Schematic of Metal Plate etch setup. VCSEL is attached to metal plate by Kapton tape, and conduction is facilitated through the substrate. Contact between substrate and plate is improved by Ti/Au backside metallization. (b) VCSEL sample etched using the Metal Plate method. Note that in this case, the etch is only limited by the tape covering the edges of the sample.

To address this consistency issue, we developed a new etch setup that is shown in Figure 2.21 (a). Now, instead of connecting the anode to the VCSEL via a metal tweezer and submerging, the anode is connected to the VCSEL through the bottomside of the substrate via a conductive steel plate. The main advantage of this method is that the bias is applied more

uniformly across the substrate, and is thus only limited by variations in the substrate resistivity caused by bowing, non-uniform dopings, etc. To minimize these variations, Ti/Au is deposited on the backside via electron beam evaporation. In order to prevent the electrolyte solution from shorting to the steel plate, Kapton tape is used to both physically secure the sample to the plate as well as electrically insulate the steel plate from the solution. Figure 2.21 (b) shows a VCSEL sample with a NP DBR etched using our new setup. Now, the porous etch proceeds very uniformly through all of the trenches, with only a minor deviation in the etch rate and reflectivity.

It is important to note that besides the variation in porosity, there are other reasons the reflectivity might drift such as non-uniformities in the MOCVD growth rate across the substrate. So, we prepared two sets of NP DBR samples using the tweezer etch method (now referred to as Tweezer) and using the steel plate etch method (now referred to as Metal Plate) to specifically study the variance in porous etch behavior. The epitaxial structure consisted of a 1 µm n-GaN template and 24-pairs of alternating unintentionally-doped (UID) GaN and n+-GaN ([Si] = 5×10^{19} cm^{-3}) to form a bottom-side NP DBR with a stopband centered at 405 nm, followed by a VCSEL epitaxial layer structure described in other sections. The full epitaxial stack was later processed into full VCSELs, but the present invention will only focus on the relevant fabrication steps to etch the NP DBR. After regrowth, trenches were dry etched using ICP to allow for electrochemical etching of the NP DBR. Atomic layer deposition (ALD) was used to deposit 25 nm SiO_2 across the entire sample to protect the devices from the electrolyte solution during the EC etch and provide electrical isolation and sidewall passivation.

the Figure 2.22 shows 3 sets of 2 representative cross-sectional SEM images taken at equally spaced and equivalent locations across both substrates, with Figure 2.22 (a-c) showing NP DBRs etched with the Tweezer, and Figure 2.22 (d-f) showing NP DBRs etched with the Metal Plate. In total, 9 FIB cuts were taken across the exposed surface of each sample, 3 across the left, right, and center, to study the uniformity of the porosity. The average porosity of each NP DBR was estimated by digitizing each SEM image and extracting the porosity through binarization and found that the NP DBR etched using the Tweezer was 25% ± 5.7% while it

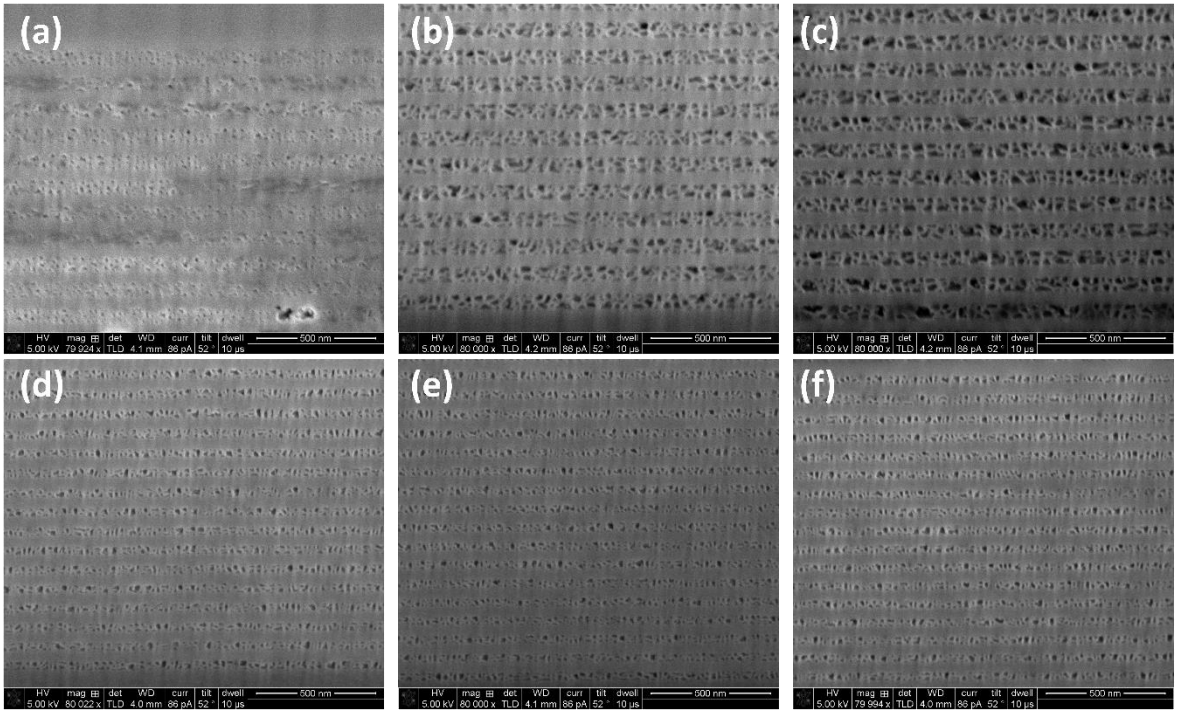

Figure 2.22. (a-c) are cross section SEM images that illustrate the porosity of NP DBRs etched using the Tweezer method. (d-f) are SEM images that illustrate the porosity of NP DBRs etched using the Metal Plate method.

was 22% ± 2% for Metal Plate. The plot of porosity versus the location on the substrate is plotted in Figure 2.23 (a), with the porosity normalized to the highest measured porosity for each sample plotted in Figure 2.23 (b). The Metal Plate improves the uniformity of the etch rate, and reduces the standard deviation of porosity across the sample by 2.5 compared to the Tweezer method. Additionally, the difference in the highest and lowest measured porosities

is significantly lower. For the Tweezer method, NP DBRs etched near the top of the electrolyte solution exhibited a minimum porosity of 16% and a lateral etch of only a couple of micron, whereas NP DBRs etched at the bottom of the electrolyte solution exhibited a higher porosity of 34% and lateral etch of approximately 50µm. By contrast, the highest and lowest porosities of NP DBRs etched using the Metal Plate were 25% and 19%, which is a difference of 6%. The lower variation in the porosity for the Metal Plate shows a high yield of devices, as the uniform porosity minimizes changes in the refractive index of the porous layer, which impacts peak reflectivity of the NP DBR, cavity resonance, and mirror loss for GaN VCSELs. Note that due to suspected growth rate and doping variations across the substrate, neither device was actually processed into full VCSELs, and their journey ended here.

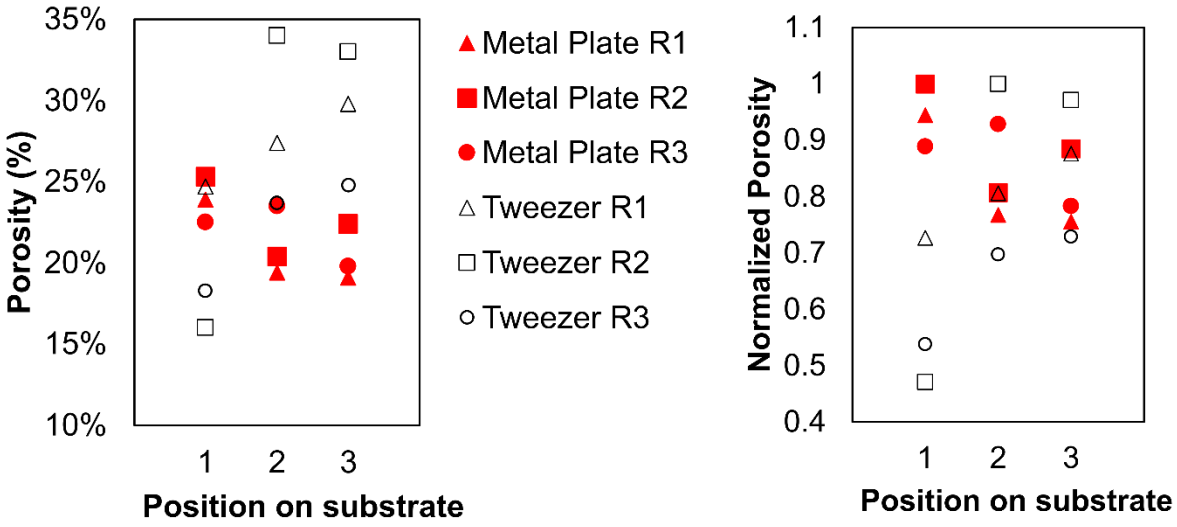

Figure 2.23. Porosity (%) vs. position on substrate for the two methods. (b) Normalized porosity vs. position on substrate for the two methods.

2.3 Optimizing the Topside Lens

A majority of reported GaN VCSEL designs have been planar short (L_{eff} <1λ) to medium (L_{eff} ~1-5λ) length cavities. They did this to ensure single longitudinal mode operation and

improve linewidth, and because that is the conventional approach to VCSEL design. However, GaN VCSELs struggle with self-heating due to higher input power requirements and high optical losses from p-GaN and current spreaders[8], as well as poor heatsinking due to the typically low thermal conductivities of the bottomside distributed Bragg reflectors (DBRs)[56]. These issues result in low thermal rollover and low device lifetimes and present significantly larger barriers to commercialization than in other material systems which have commercialized VCSEL products. Additionally, the longitudinal mode spacing for this cavity length regime is approximately 10-20nm[13], comparable to the typical width of the gain from the active layer. This means that precise growth control is critical for optimal performance. In other material systems such as AlInGaAs, lattice-matched, high index contrast epitaxial DBRs are readily available, leading to effective in-situ growth monitoring. While there has been recent progress on in-situ cavity length monitoring techniques for GaN VCSELs with epitaxial AlInN/GaN DBRs,[85] cavity length precision remains a pressing challenge for other GaN VCSEL architectures. Recently, long VCSEL cavities (L_{eff} >10μm) have shown significant promise towards addressing both the issue of thermal stability and cavity length control[9,72].

The main benefits of the long cavity are two-fold. First, a larger cavity volume enables generated heat to disperse throughout the structure rather than being concentrated near the active region[7,64]. This consideration is of particular importance for cavity structures that have thermally resistant DBR designs in the thermal path, such as flip-chip bonded dual-dielectric DBR VCSELs and nanoporous DBR (NP DBR) VCSELs[56,152]. The second benefit is that the longitudinal mode spacing is inversely proportional to cavity length, so increasing the cavity length will decrease mode spacing. For example, increasing the short to medium cavity length by a factor of 5 would decrease the mode spacing by an equivalent factor, to 2-4nm. In this

case, cavity control is less important, as the gain region will overlap several longitudinal modes regardless of how the growth rates shift.

For long planar cavities with fixed mirror diameters, diffraction loss increases quickly with cavity length[10]. This loss can be examined by analyzing the round trip loss of a beam within a planar cavity[13]. The beam is modeled as two Gaussian beams, $f(r)$ and $g(r)$, as follows,

$$f(r) = \frac{1}{\sqrt{2\pi a^2}} \exp\left(-\frac{r^2}{2a^2}\right) \tag{2.3}$$

$$g(r) = \frac{1}{\sqrt{2\pi b^2}} \exp\left(-\frac{r^2}{2b^2}\right) \tag{2.4}$$

where a and b are the standard deviation of each beam before and after one round trip. The coupling efficiency of the two beams is expressed as,

$$\frac{\int fg\, dS}{\int f^2\, dS} = \frac{\int_0^\infty fg\, 2\pi r\, dr}{\int_0^\infty f^2\, 2\pi r\, dr} = \frac{2ab}{a^2+b^2} \tag{2.5}$$

Assuming the beams undergo Fraunhofer diffraction, the ratio between a and b is,

$$\frac{a}{b} = \sqrt{1 + \frac{4\lambda^2 L^2}{\pi^2 \omega_o^4}} \tag{2.6}$$

where λ is the lasing wavelength, L is the cavity length, and ω_0 is the beam waist radius of the Gaussian beam. Substitution into the previous expression gives the full estimate of the coupling efficiency for one round trip. Assuming that the maximum coupling efficiency is 100%, the diffraction loss after one round trip can be expressed via the following,

$$1 - \frac{\sqrt{1+\frac{4\lambda^2 L^2}{\pi^2 \omega_o^4}}}{1+\frac{4\lambda^2 L^2}{\pi^2 \omega_o^4}} \tag{2.7}$$

From this equation, several intuitions arise. First, the diffraction loss will increase with increasing cavity length, and will also scale inversely with beam waist radius. These effects

can be seen in Figure 2.24 for variety of beam waists as a function of cavity lengths for a GaN cavity with planar mirrors at a wavelength of 405nm.

It can be seen that for a majority of beam waists diffraction loss quickly exceeds 1% as the cavity length. Since the typical gain of GaN QWs is approximately 1% per pass, minimizing this source of loss is critical for long cavity designs.

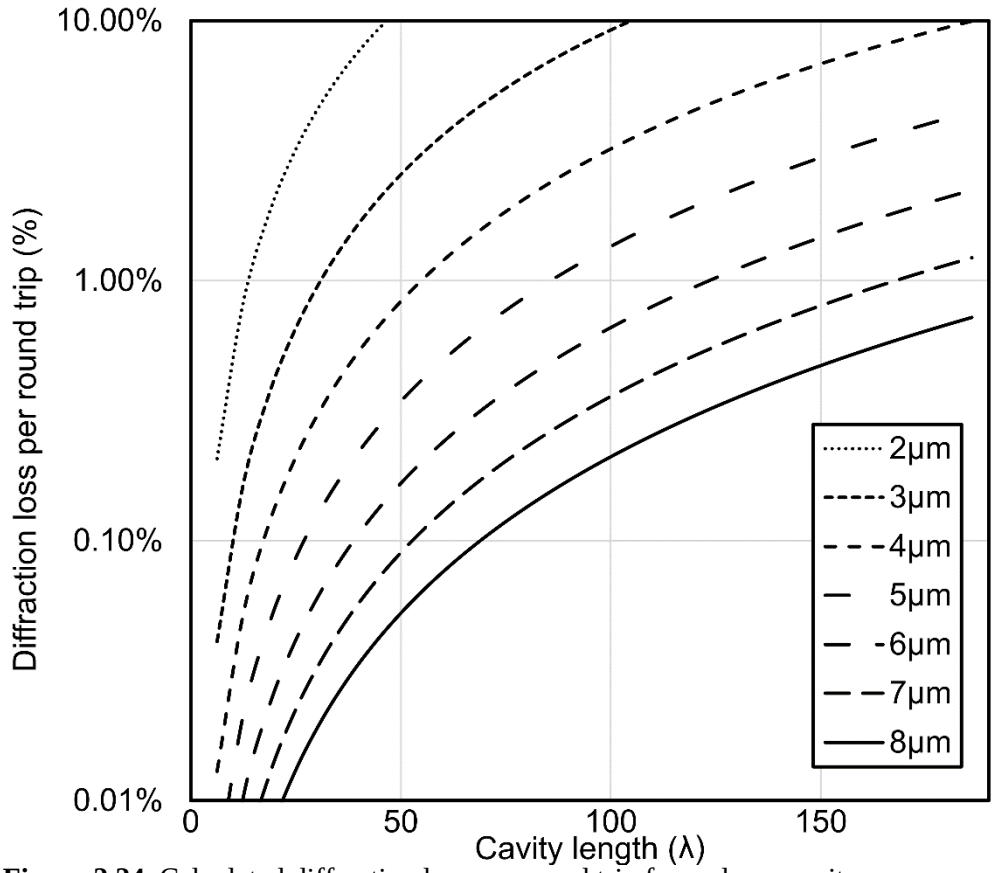

Figure 2.24. Calculated diffraction loss per round trip for a planar cavity.

For the recent designs, lateral mode confinement was achieved by introducing a curved concave mirror on one side[12]. Converting one of the planar DBRs into a curved DBR mirror is a recognized method for establishing a stable resonator configuration. This configuration results in the formation of a beam waist on the planar side, effectively reducing diffraction losses. This approach confines the lateral mode, and consequently, the dimensions of the beam waist and its propagation within the cavity are chiefly governed by two key parameters, the

cavity length (L) and the radius of curvature (ROC) of the mirror. Figure 2-X shows the dependence of the Gaussian beam waist diameter on the cavity length and ROC of the curved lens, and is adapted from ref[10]. Here, the beam waist diameter is defined as $2\omega_o$, and a full definition is expanded upon below. A given beam waist diameter can be recreated by a range of cavity lengths and ROCs, providing the laser design with two degrees of freedom by which the beam can be tuned.

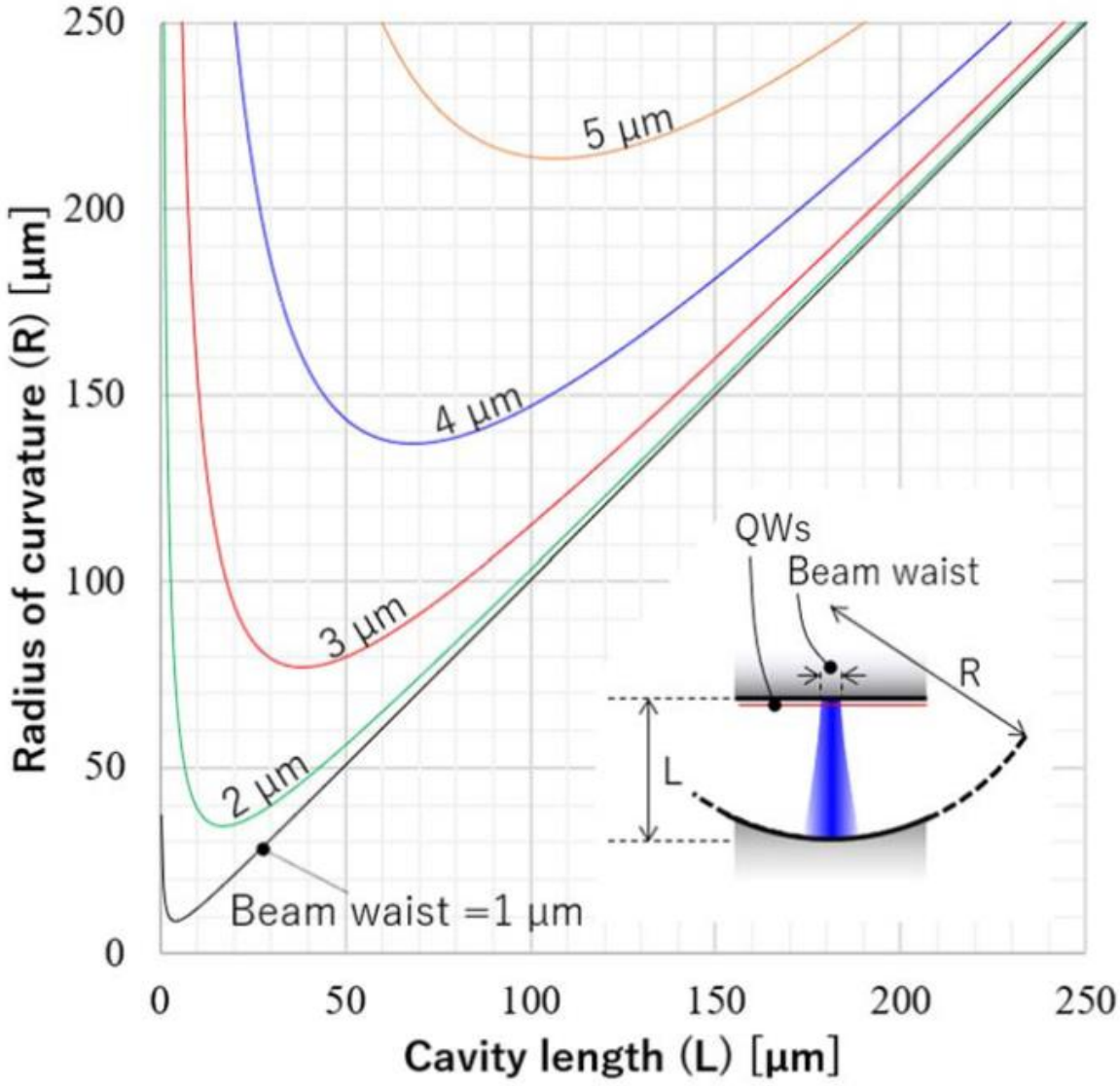

Figure 2.25. Dependence of beam waist diameter in GaN cavities with a planar and curved mirror on cavity length and ROC.

Assuming the beams are Gaussian, a resonator with a curved mirror and a planar mirror will create a beam waist (w_o) at the planar mirror that can primarily be described by the length of the cavity (L) and ROC (Equation 2.8). As the beam travels through the cavity, it expands, and the beam profile at an arbitrary value w(z) is determined by the initial beam waist as well as the position (z) in the cavity (Equation 2.9). Note that the additional prefactor of 2.9 out front of Equation 2.7 is added to include 99.7% of the light,

$$w_o = \sqrt{\frac{\lambda}{n\pi}\sqrt{L * ROC - L^2}} \tag{2.8}$$

$$w(z) = 2.9\sqrt{1 + (\frac{\lambda z}{\pi n w_o^2})^2} \tag{2.9}$$

Both of these terms describe a beam radius, so to compare with current apertures w(z) is multiplied by an additional factor of 2. Figure 2.26 shows the overlap between the beam and an active region placed 6.5μm away from the planar mirror within a 12.5μm thick cavity for

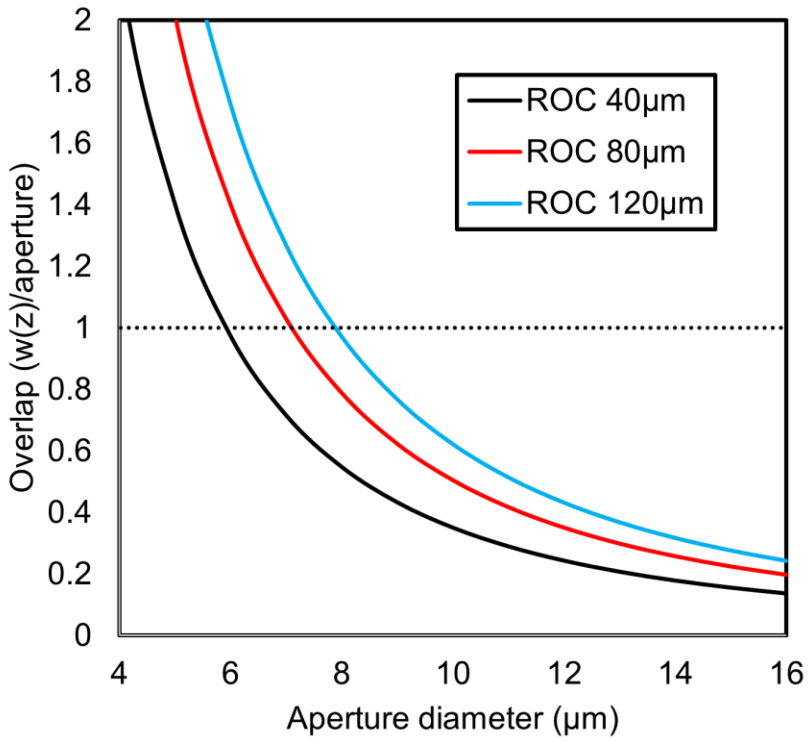

Figure 2.26. Influence of ROC on beam overlap with the current aperture. ROC and aperture values plotted are representative of values explored throughout this thesis.

different circular current aperture diameters. The plot is separated into two separate regimes, one where the beam overlap with the aperture is greater than 1, and the other where it is less than 1. In the overlap>1 case, the beam diameter is wider than the current aperture, and all of the excess light outside of the current aperture is considered scattering or diffraction loss. This isn't necessarily as bad as it sounds since a majority of the beam intensity is centered within the aperture for a majority of the current apertures explored. When designed carefully, this

effect has been used to suppress higher order transverse modes in other material systems, as higher order modes experience greater rates of diffraction loss due to their higher divergence angles[11]. However, the utility in this regime is limited by several factors, including the alignment tolerance of the microfabrication process and the internal absorption loss, both of which place constraints on how much loss is tolerable. By contrast, in the overlap<1 case, the beam diameter is narrower than the current aperture. In this regime, the current aperture couples to the mode, meaning no excess loss to diffraction. One might first assume that this is the preferable regime to be in, and for initial device prototyping, I would agree with that sentiment, as this regime is most tolerant to process fluctuations and uncertainties. However, there are significant tradeoffs with this regime. Assuming the entire current aperture is pumped uniformly, the portion of the aperture outside of the mode will produce useless spontaneous emission that doesn't contribute to lasing, essentially reducing the injection efficiency. Additionally, wider current apertures can suffer from current crowding around the edge of the aperture, meaning the distribution of current injection might directly oppose the mode profile. Even if we assume uniform injection efficiency, a low overlap with the fundamental Gaussian mode means that the current aperture will have an increased overlap with higher order transverse modes. Again, while this is not a concern when prototyping initial device structures, it becomes a concern when designing VCSELs for commercial use, as many applications require the fundamental mode. In practice, it is customary for commercial VCSEL cavities to have an overlap slightly greater than 1 to maximize the loss for higher order modes.

One characteristic of the planar-convex lens cavity is that the beam waist is confined at the planar mirror. In general, a laser beam's diameter is always the smallest at its waist. As

the beam leaves the laser cavity and travels away from the waist the beam diameter increases due to the effects of diffraction. The rate at which this occurs is defined as the beam's angular divergence, and it is approximately constant as a function of distance. The divergence half angle can be estimated using Equation 2.10 or Equation 2.11,

$$\theta_{FWHM} \sim \arctan\left(\frac{D_2 - D_1}{2\Delta z}\right) \tag{2.10}$$

$$\theta_{FWHM} \sim \sqrt{2ln(2)}\,\frac{\lambda}{\pi\omega_0} \tag{2.11}$$

where D_1 and D_2 are two measurements of the beam diameter separated by a distance Δz, λ is the lasing wavelength, and ω_0 is the beam waist. Equation 2.9 is most accurate when the beam diameter measurements are made far from the beam waist and outside of the Rayleigh Range[12], and both equations assume a Gaussian distribution of the beam.

2.3.1 Lens Fabrication Overview

Many suitable techniques for manufacturing microlens arrays have been developed[151]. Of these, the microfabrication of lenses via photolithography and resist reflow has shown promise in III-Nitride VCSEL development[10]. The main advantage of the reflow method is that it uses standard microfabrication processes and allows for the fabrication of high quality lenses for a variety of wavelengths. Figure 2.27 shows a basic process flow of the lens reflow process. First, photoresist is spin-coated onto the substrate, soft baked, and exposed as normal. After developing, an array of photoresist cylinders remains. The resist cylinders are then placed onto

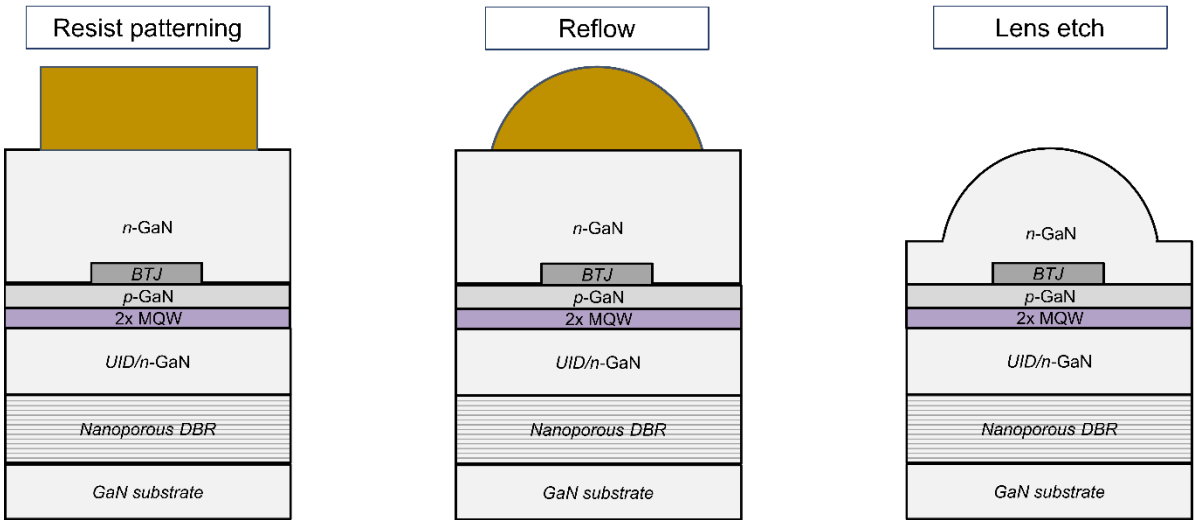

Figure 2.27. Schematic diagram of the fabrication process for topside GaN lens.

a hotplate that is set above its glass transition temperature, generally 120-200°C, causing the polymerous resist to abruptly transition from its amorphous rubbery state into a glass state system. The surface tension minimizes the surface area by rearranging the liquid masses inside of the cylinder/droplet complex. Ideally, the resist melts completely, with masses freely transported and the surface tension forming a spherical microlens. Any deviation from this reflow condition (either via temperature fluctuations, surface morphology, or time) can have an outsized impact on the final lens morphology[160], and optimizing the process condition is crucial. An example of how easily the process can deviate can be found in Section 4.1.2 when the design process for a topside GaN lens outlined in this section is applied to a dielectric lens structure. Theoretically, the volume of the lens is related to the initial cylinder parameters, but the final volume is generally lower due to outgassing and polymer crosslinking. Equation 2.12 relates the final volume of the lens (V_L) to the height of the lens at its vertex (h_L) and the radius of curvature (ROC). The height of the lens, in practice, is generally 1.3-1.7 times higher than the resist cylinder before melting, and that value can only be determined experimentally[151]. Equation 2.13 shows how the ROC is impacted by changes in the lens

height, where r describes the radius of the optical axis, and K is a value that is either 0 (spherical), -1 (parabolic), or more sophisticated.

$$V_L = \frac{1}{3}\pi h_L^2(3ROC - h_L) \tag{2.12}$$

$$ROC = (K+1)\frac{h_L}{2} + \frac{r^2}{2h_L} \tag{2.13}$$

For a spherical lens profile, the contact angle α is given by

$$\sin(\alpha) = \frac{h_L}{2r}\left[\left(\frac{h_L}{2r}\right)^2 + \frac{1}{4}\right]^{-1} \tag{2.14}$$

In addition to the resist volume and the diameter of the base of the PR cylinder at the reflow step, the contact angle is also affected by the surface energy of the sample. While developing the lens process for bulk single-crystalline GaN substrates, it was noted that the height of the resist cylinder changed across the surface of the samples. This was due to the small size of the *m*-plane GaN substrates available to us at the time, 10mm x 5mm. At this sample size, some amount of edge-beading and non-linearities of the resist across the surface were unavoidable. These non-linearities can reduce the quality of the resist cylinder, but most commonly introduce variance in the height of the resist lens after the reflow. These height changes change the resulting ROC of the etched lens, which can have impacts on device performance. To illustrate this, Figure 2.28 shows the variability in resist height and post-ICP etch GaN lens ROC for 3 lens diameters from 3 different samples processed within a similar time span. All data collected using a laser confocal microscope to image the 3D profile of the lens. It can be seen that the resist lens heights vary within 15% of each other across the three samples, and that the lens diameters are also within 10-15%. However, the ROC changes by a far larger amount, approximately 30-40% across the three lens diameters. There are several possible reasons for this outsized impact of resist height and lens diameter on ROC. First, ROC is proportional to the square of the lens diameter, so it is quite sensitive to deviations in diameter.

Second, it is known that RIE-ICP plasmas can locally heat the resist and sample surface, changing the properties of the resist across the duration of the etch[161]. One implication of this is that a shorter resist height will experience a shorter duration of state change before it is fully etched away, limiting this effect's impact on ROC relative to a taller lens[162]. Finally, if the etch ratio between the resist and the underlying material is lower than 1:1, then the difference in resist heights can become larger in the resulting etch. In practice, the etch for both the GaN lens and dielectric lens was designed for a slightly higher than 1:1 resist:surface etch ratio to minimize this effect.

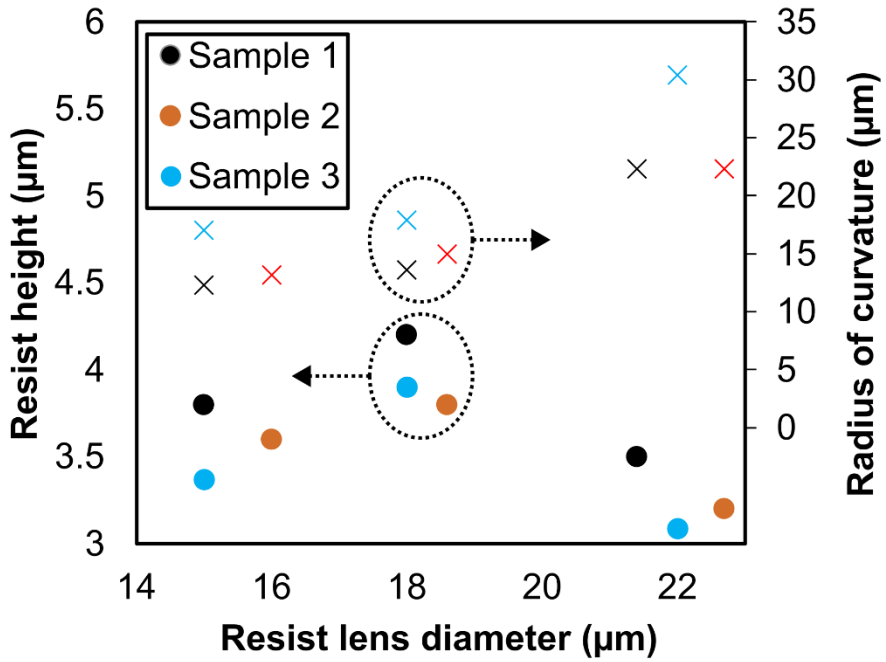

Figure 2.28. Variability of resist lens height and post-etch GaN lens ROC for 3 different lens diameters.

After optimizing the process for forming the lens PR, the next step is to transfer the resist pattern into the underlying material. Lenses fabricated this way for III-nitride devices have been demonstrated with single crystalline GaN[13] and sapphire[163]. During the transfer process, atoms from the resist surface and the material are removed simultaneously by energetic ions until the lens shape is completely etched into the substrate. The etch rate of the resist and

material are strongly dependent on the reactive-ion etching-inductively coupled plasma (ICP-RIE) etch conditions, and in practice, it is difficult to achieve and maintain a 1:1 etch ratio between the resist and material throughout the entire etch. Usually, especially when etching hard materials such as GaN and sapphire, the resist etches faster, giving a 1.5:1 or even greater than 2:1 resist:GaN/sapphire etch ratio. When this happens, the lens becomes flattened, with the lens height reduced and ROC increased proportional to the etch ratio. While this can cause the profile of the lens to deviate from the ideal spherical shape, it can enable the fabrication of lenses with significantly larger ROC values compared to what would otherwise be possible near a 1:1 PR:material etch ratio. Figure 2.29 shows the calculated ROC of 3μm photoresist lens with various radii (r=10, 20, 30 μm) that are etched into a material at varying etch ratios

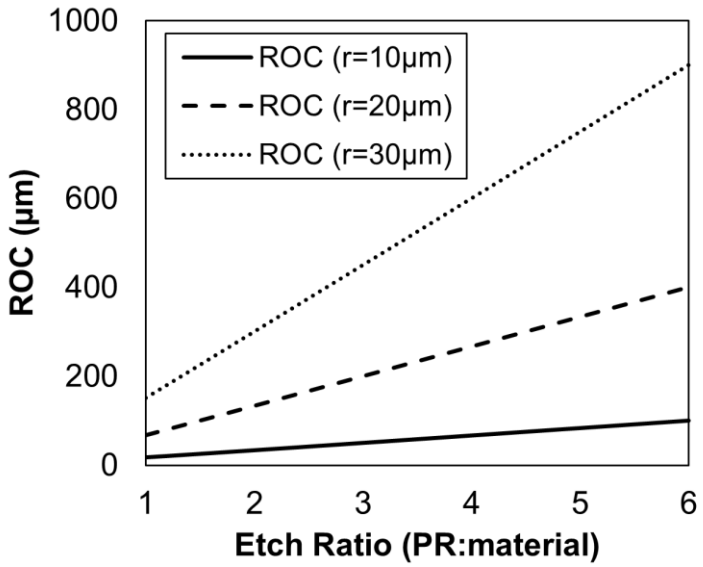

Figure 2.29. Dependence of ROC of a lens made of an arbitrary material on the dry etch ratio between the photoresist (PR) and material. Lens radii from 10μm to 30μm are explored.

from 1:1 to 6:1. For wider lenses, the effect of tuning the etch ratio has a greater effect on the resulting ROC due to the dependence of ROC on r, and ROC values on the mm-scale are readily obtainable. However, care should be taken when changing the etch ratio and etch rates significantly, as increasing the PR etch rate can lead to localized heat generation and affect

the photoresist shape and etch rate. Often, it might be beneficial to test out different photoresist lens heights, which can be achieved by using photoresists with different viscosities.

As mentioned previously, the profile of the microlens can deviate from the ideal spherical shape if the resist changes shape or composition due to local heating introduced by the etch condition. Usually, this manifests with the lens becoming steeper at the rim and flatter at the vertex. Aberrations in the lens shape will impact the beam formed within the VCSEL cavity and can cause scattering losses if not dealt with properly. One solution to this issue is to accommodate the expected change in etch rates by adopting a two-step etch flow, wherein the first part of the etch is etched more quickly at the beginning and more slowly at the end. This can be accomplished by adjusting the gas flow mixture to adjust the etch ratio between the resist and the surface, changing the overall flow of etch chemicals, changing the pressure within the reactor, or others. Another approach is to adjust the dimensions of the lens such that the lens region of interest, e.g. the portion of the lens that overlaps with the beam within the VCSEL cavity, is etched at the same rate. We took the second approach, as it simplified the lens process flow and had a higher tolerance to drift in the various photoresist, reflow, and etch conditions. Experimentally, high quality lenses have been demonstrated using many of the positive photoresists available in the UCSB nanofabrication facilities for GaN, sapphire, and dielectric lenses. Figure 2.30 shows AFM images comparing post-etch GaN surfaces compared with etched lenses with two ROCs, showing <1nm RMS for all etch conditions.

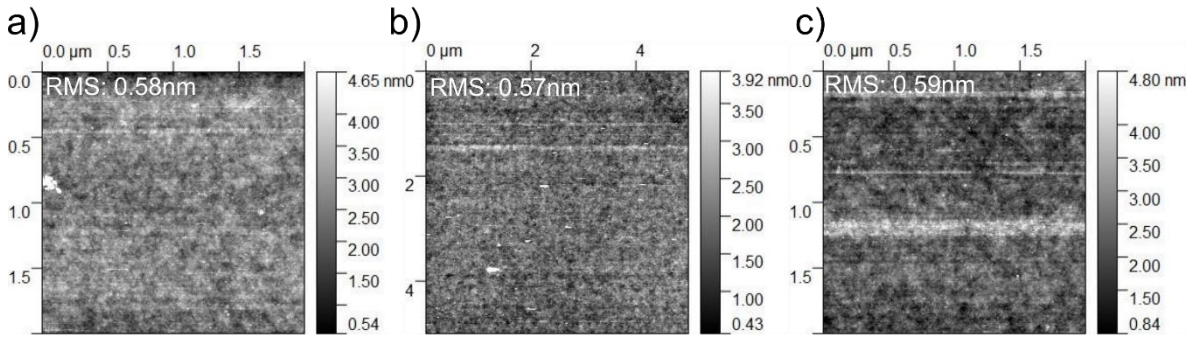

Figure 2.30. AFM scans of GaN lenses post RIE-ICP etch. (a) planar surface surrounding the lens area, (b) top of lens with ROC of 15μm, and (c) top of lens with ROC of 30μm.

2.3.2 Regrowth of Thick n-GaN

In order to form the topside GaN lens, a thick regrowth of n-GaN/unintentionally-doped (UID)-GaN was performed via MOCVD. The regrowth was designed such that the subsequent lens etch would terminate at least 100nm above the BTJ to allow for sufficient current spreading within the bottomside n-GaN layer. This meant that the regrowth had to be roughly 3,000nm in height to match with the photoresist reflow and ICP etch condition, and that the ICP etch rate had to be carefully calibrated to ensure the proper etch depth was not exceeded. The MOCVD regrowth had several practical challenges. First, the morphology of the regrown layer was highly sensitive to the growth rate, carrier gas mixture (N_2 vs. H_2). Additionally, the regrowth damaged the active region due to the thermal degradation and decomposition of InGaN at elevated temperatures[164]. Unfortunately, these two issues were made worse at higher and lower temperatures, respectively, so optimizing one came at the expense of the other.

Optimizing the morphology was the first priority due to its well-known effect on GaN VCSEL performance[104]. Due to the tendency for hillock formation on *m*-plane films grown in a H_2 environment, only 100% N_2 environments were considered[165]. It was found through experimentation that performing the regrowth using a two-step regrowth process, first with tri-ethyl-gallium (TEG) metallic precursor and then with tri-methyl-gallium (TMG) precursor

for a higher growth rate, in a 100% N_2 environment at 1000 °C added <0.3nm RMS roughness to the final epitaxial structure. However, early VCSEL devices processed from this regrowth condition appeared visually dim, and only showed some spontaneous emission clamping as a function of injection current. Due to this, attention was turned to the impact of the regrowth on the active region, which are essentially subjected to a thermal anneal for the duration of the regrowth. The total regrowth time was approximately 90min, and the growth temperature was 1000 ºC. It has been shown that *c*-plane $In_{0.08}Ga_{0.92}N$ layers are resistant to decomposition for annealing up to 15min at 1000 ºC, but experience a 50% decrease in photoluminescence (PL) intensity when annealed for 60min[166]. Figure 31 (a) shows the dependence of the PL intensity on anneal time for $In_{0.08}Ga_{0.92}N$, $In_{0.14}Ga_{0.86}N$, and $In_{0.18}Ga_{0.82}N$ layers annealed at 1000 ºC, 900 ºC, and 900 ºC, respectively. The case of the $In_{0.08}Ga_{0.92}N$ layer is likely most representative of our active region due to the similar In-composition. It can be seen that after annealing this layer for 30min at 1000 °C, the PL intensity stabilizes at approximately 50% compared to the pre-annealed condition, and doubling the anneal does not incur further damage. Figure 31 (b) shows the impact of a 15min anneal at a variety of temperatures for each InGaN condition. The $In_{0.08}Ga_{0.92}N$ layer exhibits a 30% reduction in PL intensity at 1000 °C, but only a 10% reduction at 800 °C. The mechanisms of thermal degradation of InGaN QWs discussed in the literature suggest that the decomposition of the QWs is initiated by the presence of small voids created by metallic vacancies, and decomposition within these voids is driven by In atoms that diffuse into the relaxed voids[164].

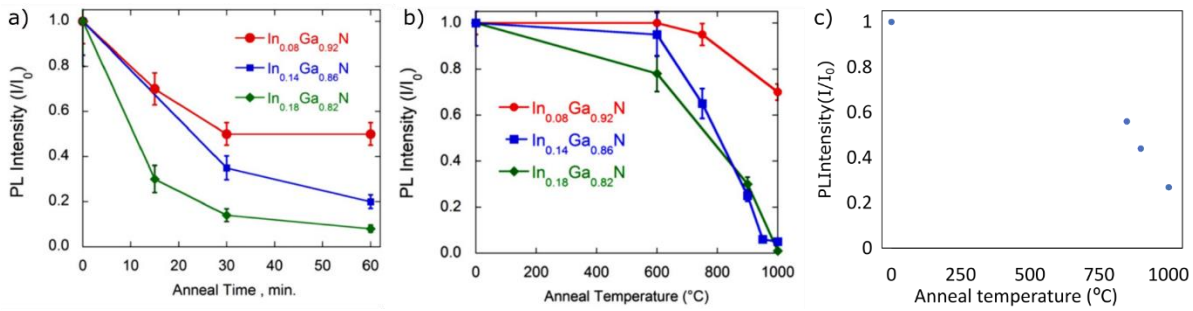

Figure 2.31. (a) Normalized *c*-plane InGaN PL peak intensities as a function of anneal time for a 1000 °C ($In_{0.08}Ga_{0.92}N$) or 900 °C ($In_{0.14}Ga_{0.86}N$, and $In_{0.18}Ga_{0.82}N$) anneal. (b) Normalized *c*-plane InGaN PL intensities as a function of anneal temperature for 15min total anneal time. (c) Normalized *m*-plane PL intensity as a function of anneal temperature for a 75min anneal time. (a-b) Copyright © 2010 Elsevier [G. T. Thaler et al, "Thermal stability of thin InGaN films on GaN," Journal of Crystal Growth **312**(11), 1817–1822 (2010).]

To analyze this effect on *m*-plane InGaN layers, a series of thermal anneals was performed. The structure was grown using atmospheric MOCVD on free-standing single-side polished (SSP) m-plane $(10\bar{1}0)$ substrates with an intentional 1° miscut in the $[000\bar{1}]$ direction. The epitaxial structure was similar to the VCSEL structure and consisted of a 2µm n-GaN buffer layer, 2 × 8nm InGaN quantum wells (MQWs) designed to emit at 410nm with 3nm GaN barriers, 5nm UID GaN, 10nm graded p-AlGaN electron blocking layer (EBL) graded along the growth direction from 30% to 0%, 80nm p-GaN, and 10.5nm p++-GaN. PL measurements were taken at several points on each sample using a 355nm laser before reloading into the reactor to perform the anneal. The anneal was performed in the MOCVD reactor for 75min at a variety of temperatures comparable to the thick GaN regrowth temperature. Each anneal was carried out in a low NH_3 environment with 5sccm TEG flow to prevent etching of the substrate. Afterwards, the PL intensity was re-measured in the same locations.

The result of three relevant temperatures is shown in Figure 31 (c). For a 75-min anneal at 1000 °C, the PL intensity of the MQWs is reduced by approximately 75%. This was taken to be the primary cause behind the failure of the early VCSEL round which exhibited the

clamping of spontaneous emission but no lasing. Decomposition of the QWs generates defects that act as non-radiative recombination centers, hurting laser performance[19].

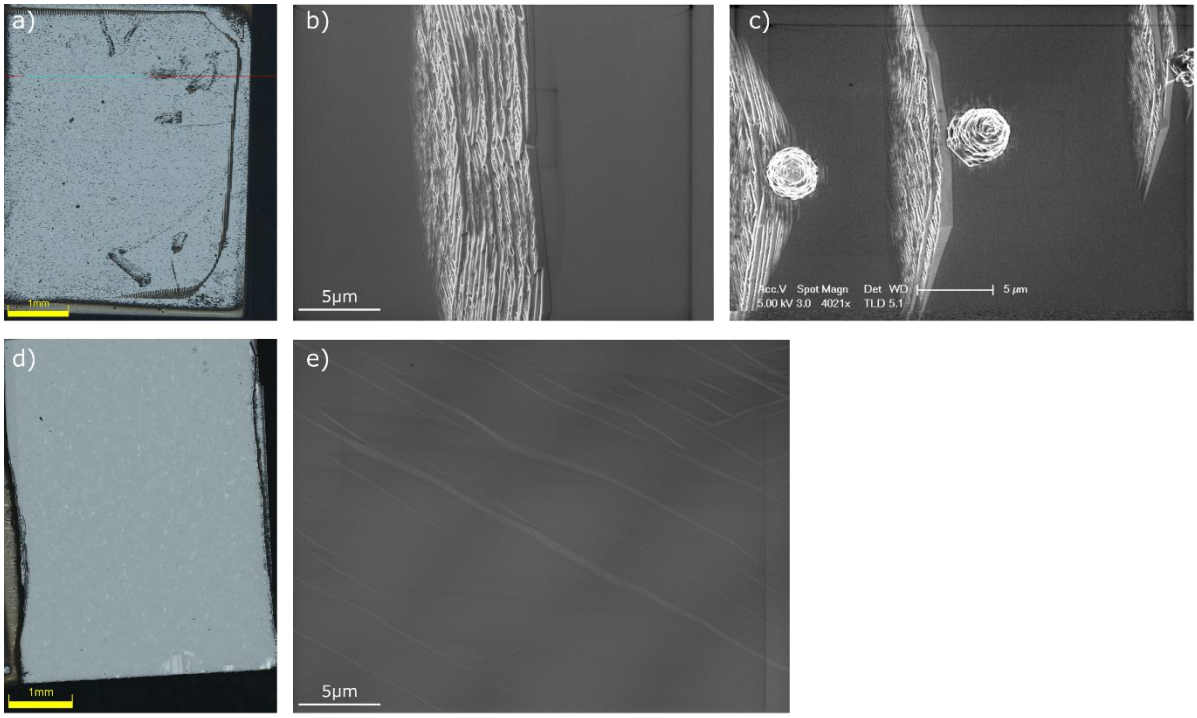

Figure 2.32. (a) Optical microscopy image of regrowth condition at 900 °C using 100% N_2. (b) SEM image of regrowth around BTJ, (c) SEM image of regrowth islands. (d) Optical microscopy image of regrowth condition at 900 °C using a 1:1 N_2:H_2 mixture. (e) representative SEM image near BTJ regrowth region.

We observed that for regrowth at 850 °C, the reduction in PL intensity was only 45%, and so next we decided to develop a regrowth condition that used a reduced regrowth temperature. Initially, we simply reduced the regrowth temperature of the previously stated 3,000nm regrowth condition from 1000 °C to 900 °C and performed the regrowth on top of etched BTJ apertures. However, as can be seen in the optical microscopy image in Figure 32 (a), this introduced significant morphology issues across the sample surface. Figure 32 (b) shows an SEM image of the regrowth region around a BTJ aperture, showing a highly scattering series of terminated growth fronts. It is unknown whether this is directly on top of or simply next to the BTJ aperture. However, the periodic nature of this regrowth suggested a relationship between the BTJ step and the formation of this regrowth. Figure 32 (c) shows another feature

that appeared across the substrate in the form of poly-GaN islands terminating a triangular facet with the long-face oriented roughly parallel to the c-direction. The origin and formation of the islands is unknown at this time. However, due to the 3-dimensional nature of these features, we suspected that we could remove them by introducing hydrogen, which acts as an etchant in MOCVD growth. Therefore, our next step was to perform the same regrowth on BTJ apertures but use a 1:1 N_2:H_2 mixture. The result can be seen in Figure 32 (d), with a representative SEM image shown in Figure 32 (e). As expected, the introduction of H_2 prevented the formation of the rough regrowth morphology, allowing for a low RMS roughness film to be deposited at a slightly less damaging regrowth temperature. However, this still led to an estimated reduction of >50% of the as-grown PL intensity, which is why in Chapter 4 we developed a dielectric lens that could be processed at room temperature.

3 Topside GaN Lens VCSEL

This chapter is adapted from Ref.[167] (copyright ©2023 by the Multidisciplinary Publishing Institute under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/)), and discusses the results from the initial topside lens VCSEL design utilizing a buried tunnel junction (BTJ) and nanoporous GaN DBR (NP DBR). While UCSB has demonstrated nonpolar III-N VCSELs with BTJs[63], this was UCSB's first demonstration of both a topside curved lens and utilizing a NP DBR, and there had not been a demonstration of a III-Nitride VCSEL with a topside curved lens. The goal of this design, shown in Figure 4-1, was to achieve continuous-wave (CW) operation by improving thermal dissipation of heat away from the active region. Additionally, with the

thick unintentionally-doped (UID) GaN cavity, the absorption loss would also be reduced, leading to a lower threshold current density relative to previous UCSB demonstrations.

The initial design demonstrated by Hamaguchi et al. prioritized low threshold conditions by placing the active region at the beam waist (100nm from the planar mirror) and minimizing aperture size[13]. To form their lens, they polished the substrate down to a thickness of approximately 28μm and formed lenses with ROC ranging from 37.7 μm to 56.6μm on the backside of the polished substrate using thermal reflow of photoresist cylinders[151]. The RMS roughness of the top of the lens was measured to be 0.2nm, similar to the roughness of a planar single-crystalline GaN substrate. Using this structure, they were able to demonstrate GaN VCSELs with record performances, all while achieving device yields greater than 90%. However, the polished substrate introduces processing complexity, requiring handling of a thin, fragile substrate, and requiring backside alignment of the mirror. This limits the scalability of this process past the 1cm^2 substrates that have comprised their reports. This captures the essence of the main advantage of the topside lens, which is to enable

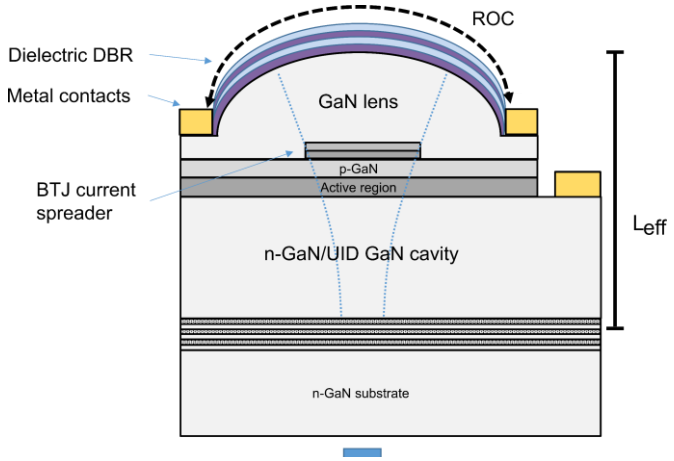

Figure 3.1. Schematic of the VCSEL structure with a topside curved GaN mirror.

microfabrication of microlens GaN VCSELs using simple processing techniques without

needing to lap or polish the substrate down to the desired cavity thickness. This also gives us the flexibility to explore cavity lengths shorter than 20μm (100λ+).

3.1 Cavity Design

The cavity was designed to have a length of approximately 60λ and emit at a wavelength of 405nm. The wavelength was chosen because it matched the wavelength of the highest powered quicktest samples grown during the recipe optimization process. The length of the cavity, as has been discussed previously, was chosen because of previous work showing the reduction in thermal resistance for thick GaN cavities[152]. Prior experimental *m*-plane VCSEL results from UCSB showed that the cavity length greatly improved the thermal properties, at the expense of increasing the total loss in the cavity due to diffraction and reducing the confinement factor[7]. The bottomside NP DBR was chosen because the thick UID-GaN growth required for the long cavity design led to complete decomposition of the sacrificial QWs that were necessary for the photoelectrochemical etch for the flip-chip dual dielectric DBR design[168]. Additionally, the long cavity design increased the tolerance of the resonant cavity to fluctuations within our MOCVD reactors, which were generally between 1-5% run to run. Figure 3.2 (a) shows the reflectance spectrum, calculated from 1D transmission matrix method simulations, of the mode spacing for a 7λ VCSEL cavity comparable to a recent publication from our group in 2019[6], and Figure 3.2 (b) shows the mode spacing for the following VCSEL design. Figure 3.2 (c) and Figure 3.2 (d) show the square of the electric field intensity of the mode at 436.4 and 411.1, respectively. For the 7λ cavity, the mode spacing was approximately 20nm, and a suboptimal growth condition required the use of Ta_2O_5 spacer layers to re-position the alignment of the standing mode to correct for the growth fluctuation. For the long 60λ cavity design, the mode spacing is approximately 2nm, and so regardless of growth

fluctuations the odds of a resonant mode aligning with the gain peak is significantly ensured given a 12nm full-width half-maximum (FWHM) of the gain.

The epitaxial device structure, shown in Figure 3.1 and summarized in Table 3.1, was grown using atmospheric metalorganic chemical-vapor deposition (MOCVD) on free-standing single-side polished (SSP) m-plane ($10\bar{1}0$) substrates with an intentional 1° miscut in the [$000\bar{1}$] direction. The epitaxial structure consisted of a 1µm n-GaN ([Si]~ $2x10^{18}cm^{-3}$) buffer layer grown at 1000 ℃ (18nm/min), 24-pairs of alternating unintentionally-doped (UID) GaN ([Si]~ $1x10^{16}cm^{-3}$) and n+-GaN ([Si]~$4x10^{19}cm^{-3}$) grown at 1180 ℃ (50nm/min) to form the bottomside DBR, 3,860nm of UID GaN grown at 1000 ℃ (45nm/min), 2,500nm

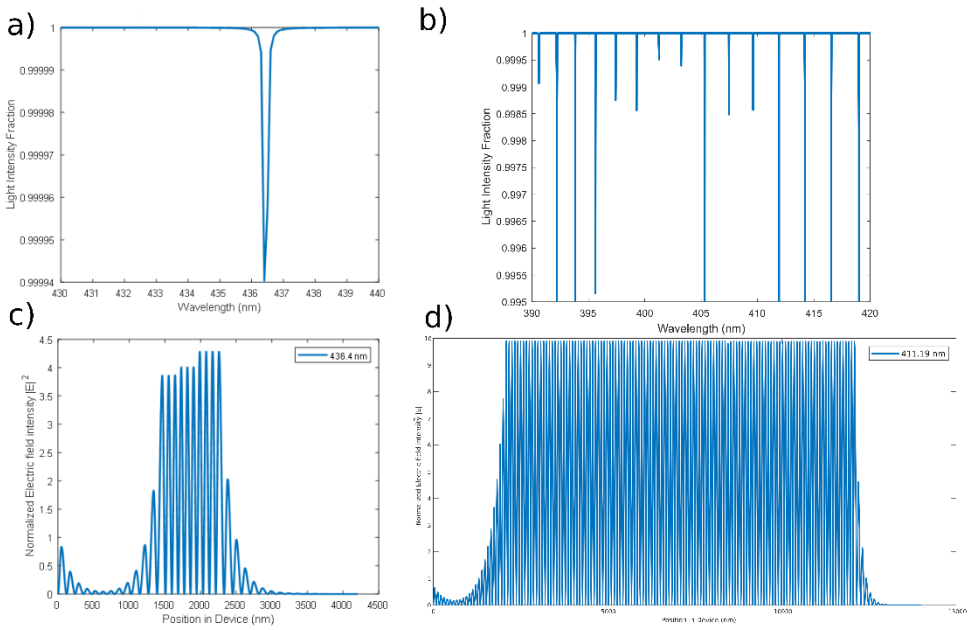

Figure 3.2. Close up of reflectance spectrums for a (a) 7λ and (b) 60λ VCSEL cavity. (c) and (d) show the electric field intensity, $|E|^2$, for a mode at 436.4nm and a mode at 411.1nm within the 7λ and 60λ cavity, respectfully.

of n-GaN([Si]~ $8x10^{18}cm^{-3}$ grown at 1000 ℃ (43nm/min), 2 × 8nm InGaN quantum wells (MQWs) designed to emit at 410nm with 3nm GaN barriers grown at 857 ℃ (6nm/min), 5nm UID GaN grown at 857 ℃ (6nm/min), 10nm graded p-AlGaN ([Mg]~ $1x10^{19}cm^{-3}$) electron

blocking layer (EBL) graded along the growth direction from 30% to 0% grown at 1000 ℃ (6nm/min), 80nm p-GaN ([Mg]~$1x10^{19}cm^{-3}$) grown at 1000 ℃ (8nm/min), and 10.5nm p++-GaN ([Mg]~$3x10^{20}cm^{-3}$) grown at 1000 ℃ (8nm/min). After the first growth, the samples were treated with concentrated HF and ozone before regrowing the 8nm n++-GaN ([Si]~ $1.5x10^{20}cm^{-3}$) TJ layer at 825 ℃ (2nm/min) by MOCVD[109]. Buried tunnel junction (BTJ) current apertures were defined by etching 30nm through the n++/p++-GaN layers using reactive ion etching (RIE). Then, all samples were annealed at 730℃ in a 4:1 N_2/O_2 environment for 30min to activate the p/p++-GaN[169]. Finally, 1810nm n-GaN ([Si]~ $4x10^{18}cm^{-3}$) and 1700nm UID GaN were grown at 900 ℃ (45nm/min) by MOCVD.

Table 3.1. Epitaxial structure, doping concentrations, and absorption coefficients[150].

Growth Step	Layer	Thickness (nm)	Doping Conc. (cm^{-3})	Abs. Coeff. (cm^{-1})
	SiO_2/Ta_2O_5 DBR (16x)	67.5/45.5	NA	**0**
	GaN	1700	UID	**2**
3rd	n-GaN	1810	$8x10^{18}$	**2**
2nd	n++-GaN	8	$1.5x10^{20}$	**235**
1st	p++-GaN	10.5	$2.5x10^{20}$	**180**
	p-GaN	80	$1x10^{19}$	**80**
	p-AlGaN EBL	10	$1x10^{19}$	**27**
	GaN barrier	5	UID	**2**
	GaN/InGaN QW (2x)	3/8	UID	**0**
	n-GaN	2500	$8x10^{18}$	**2**
	GaN	3860	UID	**2**
	n+-GaN/ GaN DBR (24x)	48.4/40.4	$5x10^{19}$/UID	**0/0**

Photoresist lenses were formed via photoresist reflow and then transferred into the upper UID/n-GaN layers by RIE[151]. The GaN lens had a diameter of 26μm and an ROC of 31μm. Next, SiO_2 was deposited on the curved GaN lenses using plasma-enhanced chemical vapor

deposition (PECVD) to act as a hard mask for subsequent processing steps. Following this, mesas were defined using RIE to allow for the p-GaN to be activated through the mesa sidewalls[107]. Next, 7µm deep, 15µm wide trenches were defined using RIE to etch the NP DBR. Then, all samples were annealed again at 730C in a N_2/O_2 environment for 30min to re-activate the BTJ through the mesa sidewall. Next, 25nm SiO_2 was deposited on both the top and sidewall surfaces of the mesa using atomic layer deposition (ALD) to protect devices from the NP DBR acid etch and provide electrical isolation[170] and sidewall passivation[171]. Next, the backside of the substrate was coated with 40nm/450nm Ti/Au using electron beam evaporation, and then the samples were taped to a conductive steel holder and submerged in 0.3M oxalic acid. A Pt wire was submerged alongside the substrate and a bias of 2.4V was applied for 30 hours to etch the NP DBRs. Under these conditions, the n+-GaN layers of the DBR chemically react with the oxalic acid and form a porous structure with pores ranging from 20-40nm in diameter[96]. After the etch was completed, the bottom metal was removed with adhesive tape and metal contacts comprised of Ti/Au (40nm/450nm) were deposited using electron beam evaporation on top of n-type GaN on the topside of the mesa and slightly overlapping the edge of the lens. Finally, a 16-period SiO_2/Ta_2O_5 dielectric DBR was deposited on the topside of the lenses using ion beam deposition (IBD).

A cross section of a completed device, taken using a focused ion beam (FIB) and imaged by scanning electron microscopy (SEM), is shown in Figure 3.3. Electrical characteristics were analyzed under pulsed operation with a 1000ns pulse width and a 1% duty cycle, and under continuous-wave (CW) operation, both at room temperature (20°C). Optical power measurements were taken by placing the sample directly on top of a Thorlabs bandpass filter centered at 410nm with a peak transmittance of 91% and placed onto a 3mm diameter silicon photodetector (model DET36A) reverse-biased at 10V for the pulsed measurements, and a wide-area 12mm diameter unbiased silicon photodetector (PD) for the CW measurements. The bandpass filter was employed because of excess spontaneous emission present in the unfiltered LIV measurement due to close proximity of the device to the PD that washed out the expected LI kink. Spectrum data was acquired with an Ocean Insight spectrometer with a spectral resolution of 2nm. Topside nearfield patterns (NFP) were taken using an optical

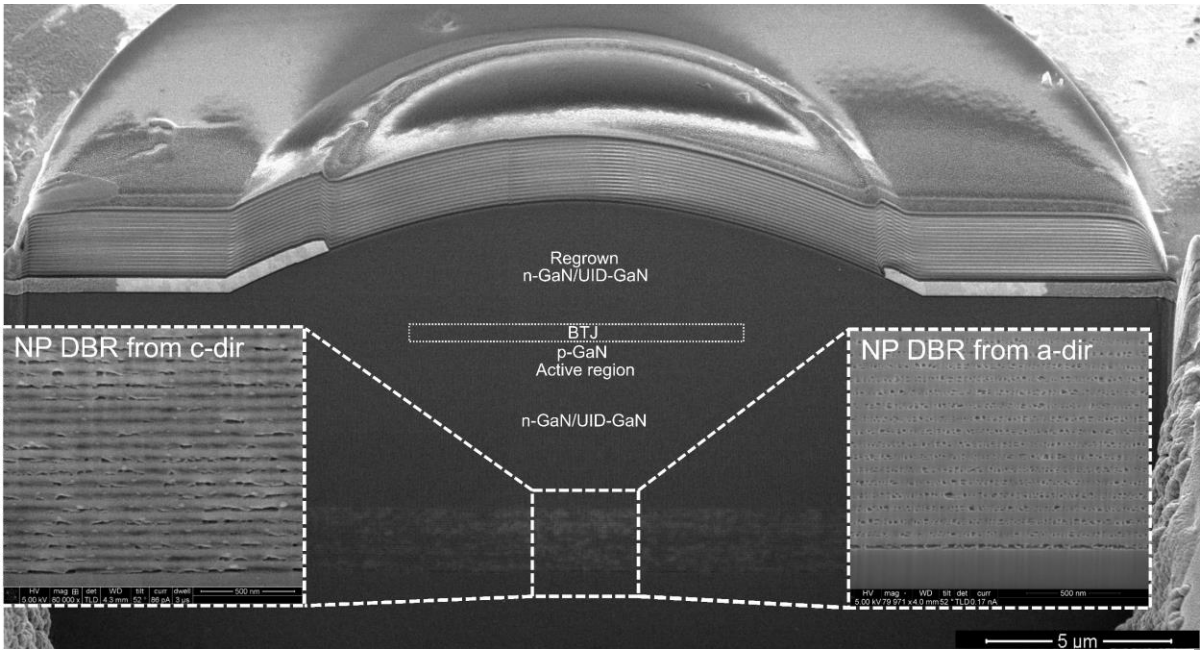

Figure 3.3. Cross sectional scanning electron microscope (SEM) image of fabricated device structure with inset cross sections of the NP DBR from the c- and a-direction.

microscope with a 20x objective lens, and the bottomside farfield pattern (FFP) was taken by placing a piece of fluorescent paper 16.5mm below the device, which was mounted to a

double-side polished (DSP) sapphire substrate. The 16.5mm thickness includes the thickness of the DSP sapphire. The resulting mode was imaged with a camera mounted at $\mathbf{35}^{\circ}$.

3.2 Device Results

The root-mean-square (RMS) roughness at the final regrowth surface was approximately 0.7nm, measured by atomic force microscopy (AFM). The fabricated devices had an effective cavity length of approximately 60.5λ (10.7μm) for a target emission wavelength of 410nm. Cross-sectional SEM images of the NP DBR are shown in the inset of Figure 5-3, with pictures taken of the pores in the c- and a-direction. The porosity of the NP DBR was extracted by binarizing the SEM image in the a-direction and calculating the porous fraction from the known thicknesses of the individual layers. Using this method, a porosity of 29% was calculated. From there, the index of refraction of the porous layer, n_{por}, can be described by the volume average theory (VAT):

$$n_{por} = [(1-\varphi)n_{GaN}^2 + \varphi n_{air}^2]^{1/2} \qquad (3.1)$$

where φ describes the porosity fraction[172]. At 410nm, n_{GaN}~2.5, leading to a calculated n_{por}~2.18, creating an index contrast of 0.32. Using 1D transmission matrix method (1D TMM) simulations, the peak reflectivity of the 24-period NP DBR is 99.617%. Additional 1D TMM simulations were carried out to calculate the internal loss <αi>, mirror loss α_m, confinement factor $\Gamma_{xy}\Gamma_z\Gamma_{enh}$, and dielectric DBR reflectivity, which were 2.52cm^{-1}, 1.8cm^{-1}, 0.00117, and 99.995%, respectively[66]. The absorption coefficients listed in Table 3.1 were rough estimates used to guide insights into the internal loss of the structure[150].

Figure 3.4 (a) shows the light-current-voltage (LIV) characteristics of a VCSEL with a 9µm current aperture analyzed under pulsed and CW operation. Under pulsed operation, the peak total output power was 260µW and the threshold current (J_{th}) and voltage (V_{th}) were 6.6kA/cm^2 and 8.9V, respectively, determined using the linear line fit method. Correcting for

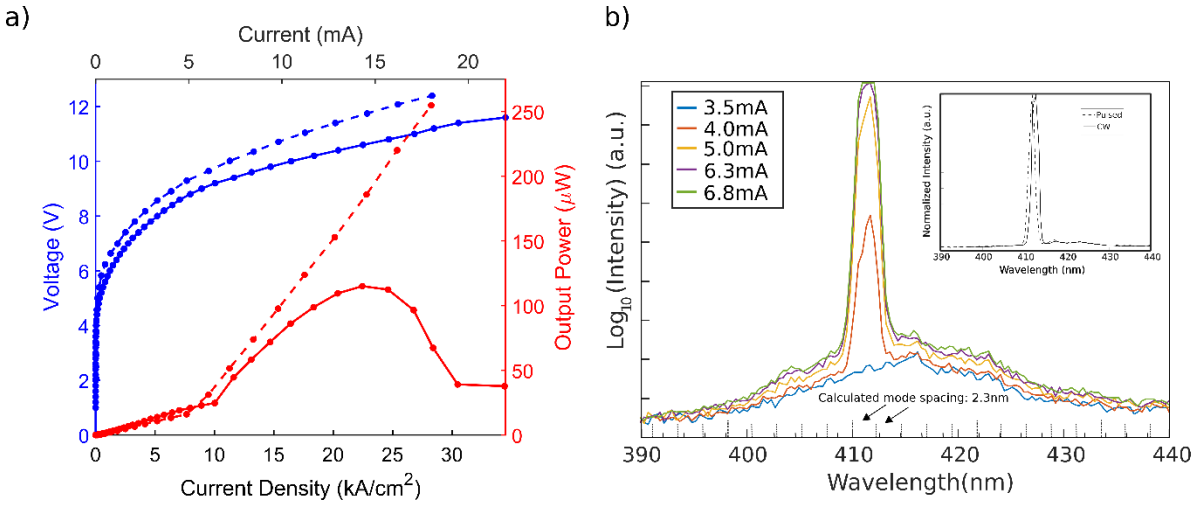

Figure 3.4. (a) LIV for pulsed (solid) and CW (dashed) operation of a VCSEL with a 9µm current aperture. Inset features LI for pulsed (solid) and CW (dashed) operation through a Thorlabs bandpass filter. (b) pulsed emission spectrum as a function of injected current. Inset shows comparison between pulsed and CW spectra taken at 8mA (12.5kA/cm^2). An arrow designates the adjacent longitudinal peak position.

the filter transmittance gives a peak output power of 290µW. The slope efficiency (SE) was 0.02W/A, leading to a differential efficiency (η_d) of 0.7%. Under CW operation, J_{th}, and V_{th} were 7.3kA/cm^2 and 8.8V, respectively, with rollover occurring at approximately 23kA/cm^2 at a peak total power of 120µW, 130µW with the filter correction. SE reduced to 0.013W/A, resulting in a reduced η_d of 0.4%.

The diameter of a Gaussian beam, 2ω(z), at the location of the active region can be expressed by the following equation[173]:

$$2\omega(z) = 2\omega_0\sqrt{1+(\frac{\lambda z}{n\pi\omega_0^2})^2} \qquad (3.2)$$

where λ is the lasing wavelength and n is the index refraction. ω_0 is the beam waist radius formed at the planar mirror:

$$\omega_0 = \sqrt{\frac{\lambda}{n\pi}\sqrt{L_{eff}R - L_{eff}^2}} \tag{3.3}$$

where L_{eff} is the effective cavity length and R is the ROC of the concave lens. At the active region, which is placed approximately 6.5μm from the planar mirror, 99.7% of the Gaussian profile is contained in a 5.8μm diameter. This was calculated by calculating the beam diameter using equations 3.2 and 3.3, and then multiplying the result by 2.9 to account for 99.7% of the light. This suggests that only 41% of the 9μm current aperture is coupled to the resonant mode, and the remaining light becomes excess spontaneous emission. However, while using the criterion $1/e^3$ is useful when calculating the internal diffraction loss, it might lead to over-estimation of the injection efficiency. It may be more appropriate to consider the $1/e^2$ intensity overlap, which for this cavity design is approximately 1μm. This leads to an estimated injection efficiency of 5%. Additionally, there was current crowding observed around the edge of the 9μm aperture. This non-uniformity in the current distribution could lead to increased recombination at the edge of the aperture and outside of the mode, which is approximately centered over the aperture. This low overlap is likely a significant factor behind the low differential efficiency. Figure 3.4 (b) shows the unfiltered spectra as a function of injected current under pulsed operation, showing the selection of a mode centered at 411nm that grows with injected current. The inset of Figure 3.4 (b) shows the lasing behavior at a bias of 8mA under pulsed and CW operation, showing minimal shift of the mode at the injected current. Note that the resolution of the spectrometer (2nm) is similar to the longitudinal mode spacing calculated using 1D TMM modelling (2.3nm). An arrow designates the adjacent longitudinal

peak position which is almost at the same position of the observed peak emission wavelength, so it is unknown whether the device was lasing in a single longitudinal mode or multiple.

Prior NP-DBR VCSEL demonstrations with cavity lengths of 8.9λ[102], 6λ[99], 6λ[100], and 1.5λ[52] exhibited threshold currents of 20kA/cm^2 (pulsed), 42kA/cm^2 (pulsed), 59kA/cm^2 (pulsed), and 0.7kA/cm^2 (CW), respectively. Previous curved mirror VCSEL demonstrations exhibited threshold current densities which ranged from 3.5 – 141kA/cm[210,13,73,74,174]. Our device performs favorably compared to prior NP-DBR VCSEL demonstrations, and in-line with prior curved mirror VCSEL demonstrations. Most importantly, the threshold current density was reduced by almost 5x compared to our group's previous CW *m*-plane VCSEL demonstration[7]. This is partly attributed to the curved lens, which minimized the loss that would otherwise have occurred due to diffraction of the beam outside of the optical aperture. However, we note that the threshold current density calculated from the threshold current divided by the current aperture area is not always an accurate metric, given that the injected current density is seldom uniform over the aperture and that the optical mode diameter is usually smaller than the current aperture diameter[175].

CW performance was limited by thermal rollover, which was caused by a higher than anticipated voltage. The high voltage is believed to be caused by incomplete activation of the TJ interface in the BTJ[67,176], a problem exacerbated by the thick n-GaN regrowth immediately following the BTJ etch. Additionally, the Mg-doping within the p++-GaN of the BTJ was approximately [Mg] = 3×10^{20} cm^{-3} as measured by secondary ion mass spectrometry (SIMS), potentially leading to passivating Mg-H complexes at or near the TJ interface[108].

Figures 3.5 (a) and (b) show topside NFP images taken of the device below and above J_{th}. Above threshold, a bright spot appears above the BTJ at the center of the lens that is

approximately 2μm wide. For this design, the beam waist diameter is calculated to be 2.15μm, in agreement with the observed experimental value.

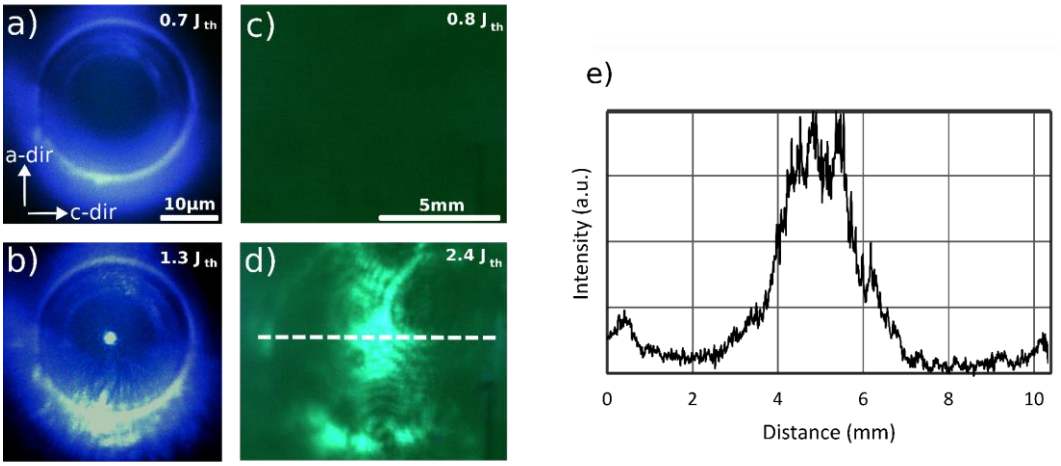

Figure 3.5. (a-b) Optical microscopy images of a 9μm-diameter-aperture VCSEL below and above J_{th} (pulsed), respectively. (c-d) Captured images of bottomside FFP of the same VCSEL below and above J_{th}, respectively. (e) Cross-sectional profile of bottomside FFP above J_{th} taken along the c-direction.

Figures 3.5 (c) and (d) show the fluorescent paper when illuminated through the bottomside of the VCSEL below J_{th} and above J_{th} at a bias of 10mA. The rough SSP GaN substrate contributes to significant scattering of the mode. However, a rough central lateral mode shape appears above threshold and grows with injected current. Figure 3.5 (e) shows a 2D line-scan of the mode, with a full-width half-max (FWHM) of approximately 2.9mm. The fluorescent paper was placed 16.5mm away from the bottom of the 250μm thick GaN substrate, leading to an extracted divergence half-angle, θ_{FWHM}, of 8.4°. This value is comparable to the theoretical $\theta_{FWHM} \approx 10°$, calculated using the following equation[173]:

$$\theta_{FWHM} = \sqrt{2ln2}\frac{\lambda}{\pi\omega_0} \tag{3.4}$$

Taking the radius of the spot observed in the topside NFP in Figure 3.5 (b) and applying to equation 3.4 gives an expected topside θ_{FWHM} of 8.8°, in reasonable agreement with the bottomside value. The experimental top and bottom θ_{FWHM} are in line with recent curved mirror cavity demonstrations, which reported divergence half angles of 8.5° and 3.9°[61,174], but higher than recent planar cavity demonstrations, which reported divergence half angles of 5.1° and 2.8°[79,91].

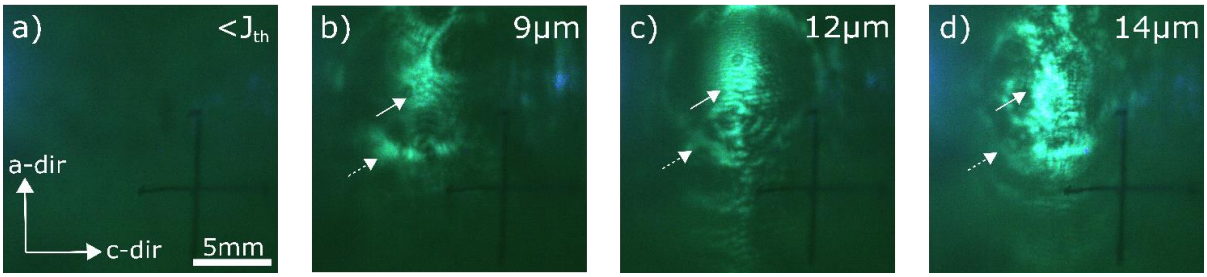

Figure 3.6. (a) Fluorescent paper illuminated by the 9μm VCSEL below J_{th}. (b) – (d) shows bottomside FFP images for a (b) 9μm, (c) 12μm, and (d) 14μm VCSEL operating above J_{th} under pulsed conditions. The devices were held at a bias of (b) 10mA, (c) 10mA, and (d) 18mA. The solid white arrow denotes the primary mode, the dashed arrow denotes the outer ring that appears at threshold.

Figure 3.6 (a) – (d) shows bottomside FFP images of the previously analyzed 9μm device next to neighboring 12μm and 14μm devices. The rough surface of the backside of the SSP GaN substrate contributes to significant scattering of the mode. However, a rough central lateral mode shape appears above threshold for each device that grows in intensity with injected current. The primary mode is indicated with a solid white arrow. The divergence half-angle for the 12μm and 14μm were 7.5° and 9°, respectively, measured along the c-direction. It is noted that the modal shape appears somewhat elliptical in behavior along the a-direction, more pronounced in the 12μm and 14μm devices. Additionally, an outer ring is visible in each FFP, highlighted by a dashed white arrow. The ring has a lower intensity than the central mode, but it appears at threshold and grows with the central mode. The ring diameter appears to be independent of aperture size, pointing to a structural issue common to all of the devices, possibly due to scattering at the edge of the GaN curved lens. To ascertain whether or not the

ring was part of the lasing mode, a linear polarizer was inserted into the pathway of the light and rotated from parallel to the a-direction to parallel to the c-direction, with the resulting FFP characteristic visible in Figure 3.7. It can be seen that as the polarizer is rotated away from the a-direction the central mode intensity drops, as is expected for *m*-plane laser emission[30]. However, the intensity of the outer ring remains relatively unchanged as a function of polarizer orientation, leading us to conclude that this ring is likely excess spontaneous emission that is scattered by some structural component within the VCSEL.

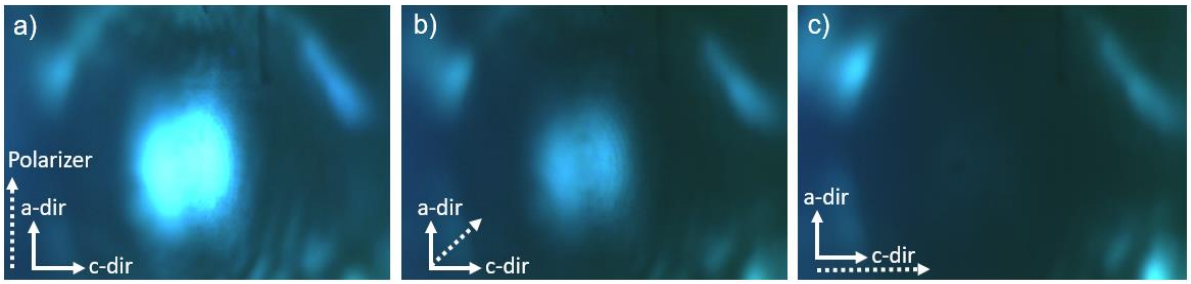

Figure 3.7. Fluorescent paper illuminated by a VCSEL above J_{th} with a linear polarizer aligned (a) parallel to the a-direction, (b) 45° from the a-direction, and (c) perpendicular to the a-direction.

In summary, 60.5λ-cavity GaN VCSELs utilizing a topside curved mirror, BTJ, and NP DBR were successfully fabricated. The peak output power for a 9μm aperture under pulsed operation was 290μW, with a J_{th} of 6.6kA/cm^2 and η_d of 0.7%. Under CW operation, J_{th} increased to 7.3kA/cm^2, η_d decreased to 0.4%, and the peak output power at rollover was 130μW. Bottomside FFP images show that the divergence half-angle was approximately 8.4°. The outer ring observed across multiple FFPs was determined to be scattered spontaneous emission from some internal rough interface.

4 Topside Dielectric Lens VCSEL

Portions of this chapter are adapted from Ref.[177] (copyright © 2023 from IOP Publishing). The chapter discusses the results from making *m*-plane VCSELs with a topside dielectric lens

as opposed to a GaN lens. While the VCSELs with a monolithic GaN lens successfully lased, the best CW threshold current density, 7.3 kA/cm^2, was significantly higher than previously reported VCSELs utilizing a curved mirror[72]. Additionally, the peak output power was significantly lower, both of which pointed to issues with the active region intensity. It was found that the regrowth condition required to fabricate the topside GaN lens reduced the photoluminescence (PL) intensity of *m*-plane QWs by 56% relative to the on-grown sample, as discussed in detail in Chapter 2.3.2. Decomposition of the QWs generates defects that act as non-radiative recombination centers, hurting laser performance[19]. It would be advantageous to replace the monolithic GaN mirror with a non-absorbing material that can be deposited and processed under standard temperatures. Based on this reasoning, we developed a SiO_2 concave mirror that can be processed near room temperature (RT) using standard microfabrication techniques. This chapter covers our initial VCSEL design which utilized an ion-implanted aperture (IIA) for current confinement, our second attempt which utilized a buried tunnel junction aperture, and then compares the performance of the two device sets.

4.1 SiO_2 lens VCSEL with Ion-Implanted Aperture

The epitaxial device structure, shown in Figure 4.1 (a), was grown and fabricated similarly to Ref[167], and will be briefly described below. The epitaxial layers were grown using atmospheric metalorganic chemical-vapor deposition (MOCVD) on free-standing double-side polished (DSP) *m*-plane $(10\bar{1}0)$ substrates with an intentional 1° miscut in the $[000\bar{1}]$ direction. The epitaxial structure consisted of a 21-period unintentionally-doped (UID) GaN and n+-GaN superlattice to form the bottomside NP DBR, UID GaN, n-GaN, 2 × InGaN quantum wells (MQWs), and a p-GaN layer. After the first growth, a Ti/Au hard mask was

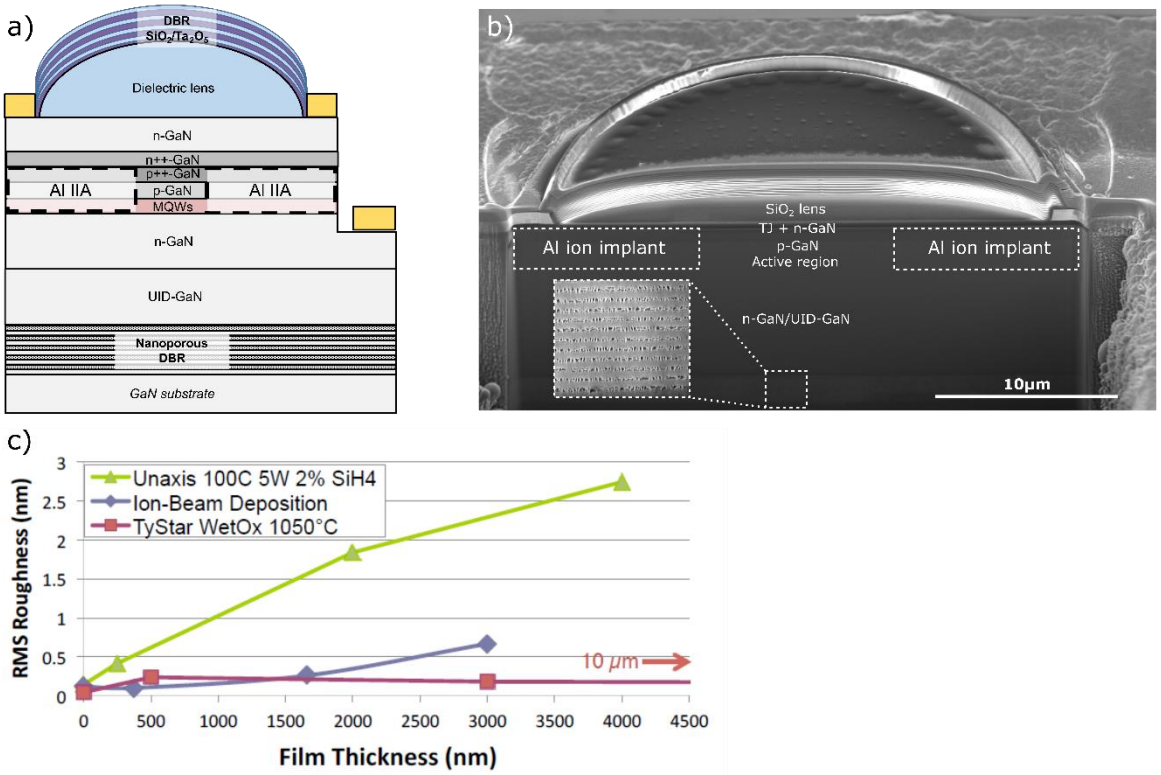

Figure 4.1. (a) schematic of VCSEL structure, (b) cross-sectional SEM image of fabricated device structure. (c) RMS roughness versus film thickness for SiO_2 deposited via IBD, ICP-PECVD, and wet thermal oxidation. Reproduced with permission.

deposited to define the aperture during ion implantation. Al ions were implanted with a dose of 10^{15} cm^{-2} and an acceleration voltage of 20kV. After removing the hard mask with heated aqua regia, the sample was cleaned with concentrated HF and ozone before regrowing the

8nm n++-GaN tunnel junction (TJ) layer and 150nm n-GaN current spreader by MOCVD[109]. Mesa structures and trenches were formed by reactive ion etching (RIE). Following this, 2,400nm SiO_2 was deposited via ion beam deposition (IBD). IBD deposition was chosen because it exhibited the optimal material properties that were desired, including a high density low-defect film, while also maintaining a low RMS roughness of deposited film. Figure 4.1 (c) shows the dependence of film RMS on the thickness of the deposited film[178]. PECVD deposited films increase in roughness rapidly due to the chemical deposition process, which nucleates islands of material that grow in roughness with increased deposition thickness. IBD deposited films, on the other hand, are deposited via ejection of an Si target by sputtering, greatly improving the surface quality. In principle, IBD and sputter-deposited films should be of comparable optical quality, but IBD was chosen due to the greater degree of control over the deposition rate. While wet thermal oxidation would yield a slight reduction to the overall roughness, the high temperature required (>1000 °C) were deemed too damaging to the active region. After depositing the SiO_2, photoresist lenses were formed via photoresist reflow and transferred into the SiO_2 by inductively coupled plasma etching (ICP) using a CF_4:O_2:CHF_3 gas mixture of 3:3:1[151]. After, the NP DBR was electrochemically etched, followed by deposition of metal contacts and a 16-period dielectric DBR. A cross section of a completed device, taken using focused ion beam (FIB) and imaged by SEM, is shown in Figure 4.1 (b). A close-up SEM image of the NP DBR is shown in the inset of Figure 4.1 (b). Electrical characteristics were analysed under pulsed operation with a 500ns pulse width and a 0.5% duty cycle at room temperature (20°C). Optical power measurements were taken by placing the sample 7mm above a calibrated 3mm diameter biased silicon photodetector (PD). Spectrum data was acquired with an Ocean Insight HR4Pro spectrometer with a spectral

resolution of 0.2nm. Topside nearfield patterns (NFP) were taken using an optical microscope with a 20x objective lens, and the bottomside farfield pattern (FFP) was taken using a Thorlabs goniometric stage with a 2.54cm point to rotation.

The root-mean-square (RMS) roughness at the final regrowth surface was approximately 0.8nm, measured by atomic force microscopy (AFM). After depositing the SiO_2 the RMS roughness remained near 0.8nm. The fabricated devices had an effective cavity length of approximately 65λ for a target emission wavelength of 405nm. A NP DBR porosity of 31% was determined from cross-sectional SEM images, leading to a calculated peak reflectance of 99.673%.

The light-current-voltage (LIV) characteristics of a 10 μm aperture VCSEL were analyzed under pulsed operation with a 500ns pulse width and a 0.5% duty cycle, shown in Figure 4.2 (a). The threshold current density was 14kA/cm^2, and the maximum output power was 370μW for a lasing mode at 404.5nm with a spectrometer resolution-limited linewidth of 0.22nm. The slope efficiency (SE) was 0.02W/A, leading to a differential efficiency (η_d) of 0.64%. As shown in Figure 4.2 (b), the device exhibited a side-mode suppression ratio (SMSR) of 30dB

down to the detection floor of the spectrometer, up to a current density of approximately 40kA/cm^2.

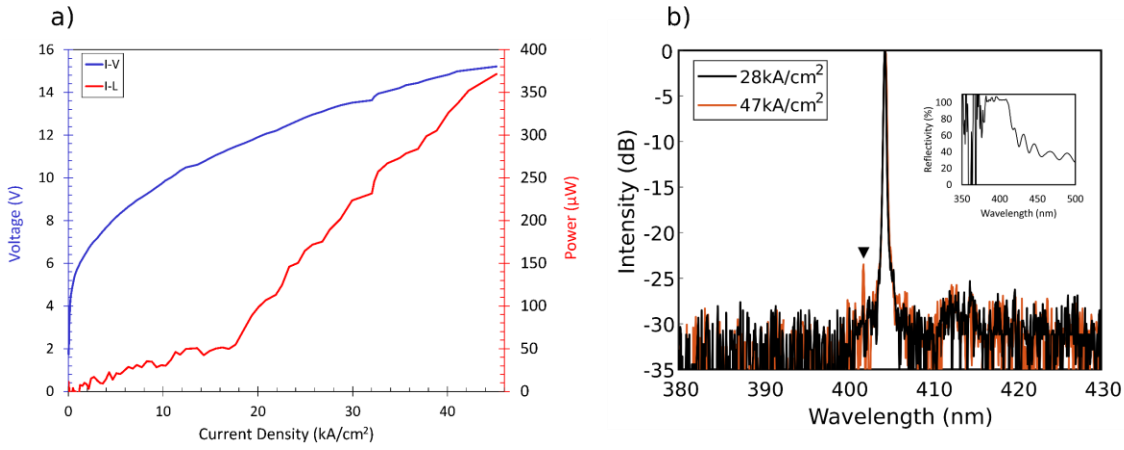

Figure 4.2. (a) LIV for pulsed operation of a 10μm VCSEL. (b) pulsed emission spectrum of the device above J_{th} showing SMSR of ~30dB (black) and the emergence of an additional mode at higher J (red). Mode denoted by black arrow. The inset shows the measured reflectivity of the bottomside NP DBR.

Above 40kA/cm^2, a second mode appears at 401.8nm, with a mode spacing of 2.7nm. The unexpected SMSR might be influenced by the narrow stopband of the NP DBR, which can be seen in the inset of Figure 4.2 (b). The calculated stopband width of 21nm, and fall-off at 410nm, prohibited half of the active region emission spectrum, which was centered at 405nm, from experiencing meaningful gain. It is suspected that high internal loss increased the threshold for adjacent modes, and similar single mode behavior was also observed by Ito et al. for a 3μm aperture VCSEL with a cavity length of 25μm and a lens with an ROC of 33 μm[179]. It has also been established that cavity control structures, such as filtering mirrors, can provide longitudinal mode control in long cavities[73].

Compared to previous work with a monolithic GaN lens, the SiO_2 lens creates an additional planar interface with the GaN epitaxial surface that affects the beam propagation through the cavity. For this initial demonstration, two simple models were constructed using matrix elements from Table 2-1 in Optical Electronics by Yariv[173], and a Gaussian beam was

propagated using ABCD matrix formalism. With this approach, the GaN/SiO_2 interface becomes an interface matrix element that introduces refraction. The beam waist equation, from equation 2.5-8 and 2.5-13, is:

$$\omega_0 = \sqrt{\frac{\lambda z_0}{n\pi}} \tag{4.1}$$

where z_0 is the confocal parameter. Propagating the beam modifies z_0, and the new expression for the beam waist becomes:

$$\omega_0 = \sqrt{\frac{\lambda\sqrt{-\frac{BD}{AC}}}{n\pi}} \tag{4.2}$$

where A, B, C, and D are matrix elements found by propagating the beam through the cavity structure. It is found with this method that, a cavity with a monolithic GaN lens has a beam waist of 1.33μm, while a cavity with an SiO_2 lens has a beam waist of 1.56μm, 17% wider than the GaN lens case. Using Equation 3.2 translates to a beam diameter at the active region of 7.88μm for the GaN lens, and 9.13μm for the SiO_2 lens, a 15.8% increase.

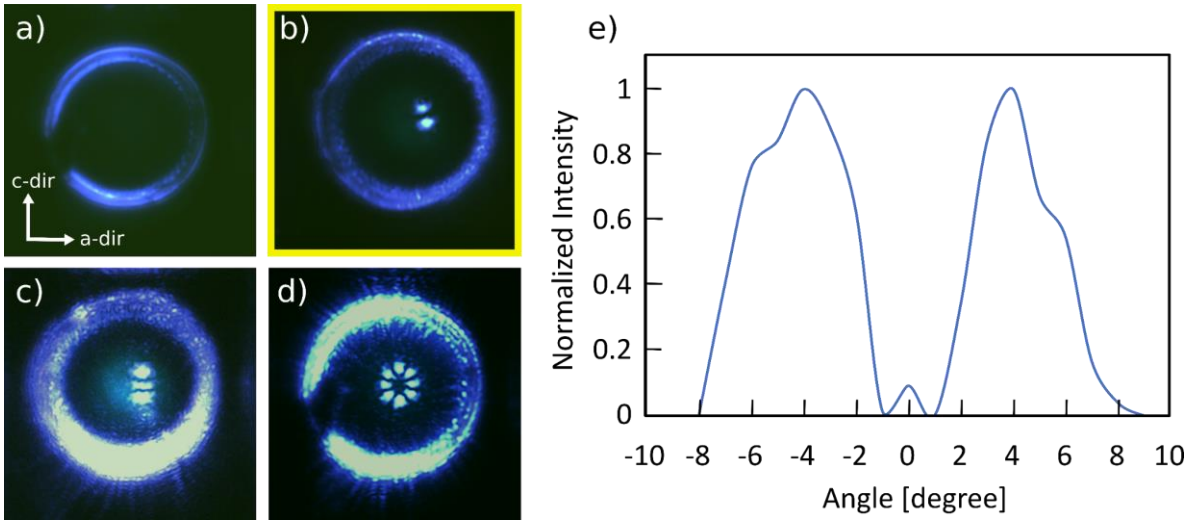

Figure 4.3. Optical microscopy images of representative 10μm VCSEL (a) below J_{th} (b-d) above J_{th}.. (e) Bottomside FFP of (b) measured at a current density of 27kA/cm^2. Measurement taken along the c-direction.

Assuming no other effects, this would improve the coupling efficiency of the 10μm current aperture into the mode from 62.4% to 83.3%. The coupling is also limited by the alignment between the current aperture and lens, which is approximately ±1μm.

Topside nearfield patterns (NFPs) for several 10μm VCSELs can be seen in Figure 4.3 (a) – (d). The modes are similar to higher order mode profiles that can be calculated using a Laguerre-Gaussian model[132], which is attributed to the circular symmetry of the lens. Figure 4.3 (e) shows the bottomside FFP for the device in Figure 4.3 (b). The higher order transverse mode behavior is in line with findings observed by Nakajima et al for a VCSEL with a similar lens ROC[9]. The similarity between the topside NFP and bottomside FFP is promising preliminary evidence that the large irregular voids in the bottomside NP DBR may not contribute to scattering of the farfield[156]. This is discussed in more detail in the following section.

4.1.1 Impact of Pitting on VCSEL performance

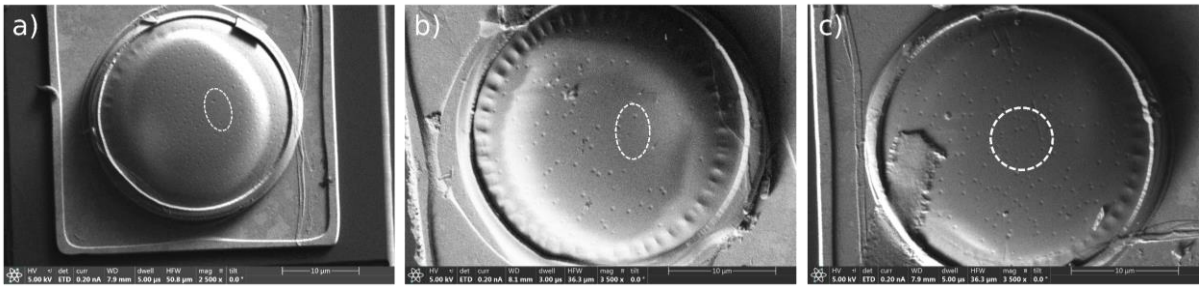

Figure 4.4. Topside SEM images of VCSELs from Figure 4.3 (b) – (d). Dashed white circles show the approximate location of the modes above J_{th}.

During testing, we observed that the modes in Figure 4.3 (b) and (c) were off-center from the peak of the lens. SEM imaging revealed the presence of pits across the surface of the lenses, shown in Figure 4.4 with a white dotted circle denoting the approximate position of each mode seen in the topside NFP.

Measurements on the pitted surface using atomic force microscopy (AFM) revealed that the pits were approximately 10-50nm deep, and 300nm wide. Dielectric lenses were fabricated on test samples following the same process used on the VCSELs to further study the pitting phenomena. An example AFM image can be seen in Figure 4.5 (a), with a line plot of a sample pit in Figure 4.5 (b).

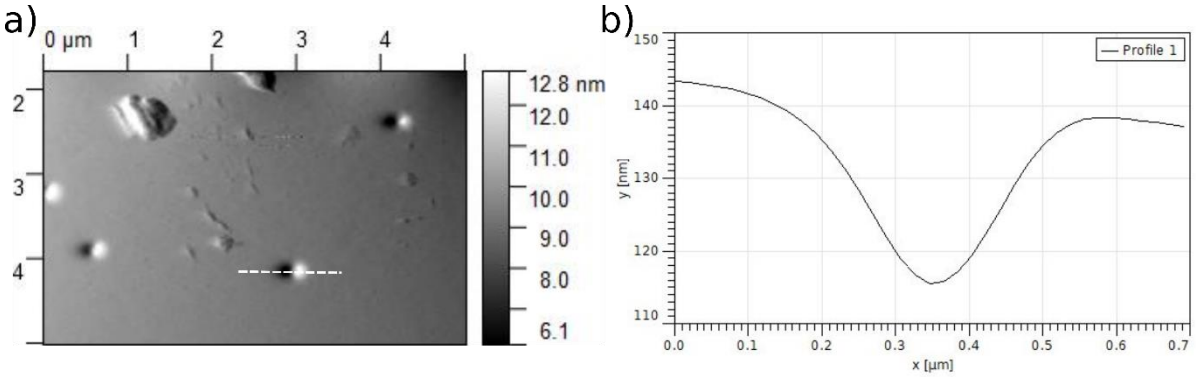

Figure 4.5. (a) AFM scan taken near center of dielectric lens. (b) line scan through pit denoted by white dashed arrow.

As deposited, the root-mean square (RMS) roughness was approximately 0.4nm. After etching, the RMS of regions without pits was comparable. However, across the lens surface, the RMS grew with the pit density, represented as a percentage coverage by area, as can be seen in Figure 4.6 (a). Note that the following analysis assumes a uniform distribution of pits 35nm deep, and 350nm wide, and that the pit roughness is averaged across the measured region. Using a modified version of the 1D TMM model developed by ref.[104], the RMS roughness was correlated to a reduction in the reflectivity of the topside curved DBR. First, the roughness introduced by the pits was integrated into the model by multiplying the complex amplitude reflection coefficient of light passing from layer 1 to layer 2, r_{12}, by a scattering factor, S_f:

$$r_{12} = \left(\frac{n_2 - n_1}{n_2 + n_1}\right) S_f \qquad 4.3$$

where n_1 and n_2 are the complex refractive indices for the corresponding layers. The scattering factor depends on the roughness profile of the interface, σ, and the correlation length, τ_c. The full form of the scattering factor can be approximated by assuming that either $\tau_c >> \lambda/n$ or $\tau_c << \lambda/n$, leading to two forms of the scattering factor:

$$S_f^{\tau \gg \lambda/n} = \exp\left[-\left(\frac{4\pi\sigma}{\lambda/n}\right)^2\right] \tag{4.4}$$

$$S_f^{\ll \lambda/n} = \exp\left[-\frac{64\pi^4\sigma^2\tau_c^2}{3(\lambda/n)^4}\right] \tag{4.5}$$

The physical significance of the scattering factor is to introduce a phase shift caused by the change in the surface from its ideal value. Both of these approximations assume $\sigma << \lambda/n$, and that the surface roughness is random[180]. While the first assumption fits well to this case, the second assumption limits the general applicability of this method, since the roughness around a pit is significantly higher than the mean value, and the roughness between two pits is significantly lower. However, the main consequence of this non-uniformity in roughness would be to affect individual spatial modes, and so the approximation is used for this analysis.

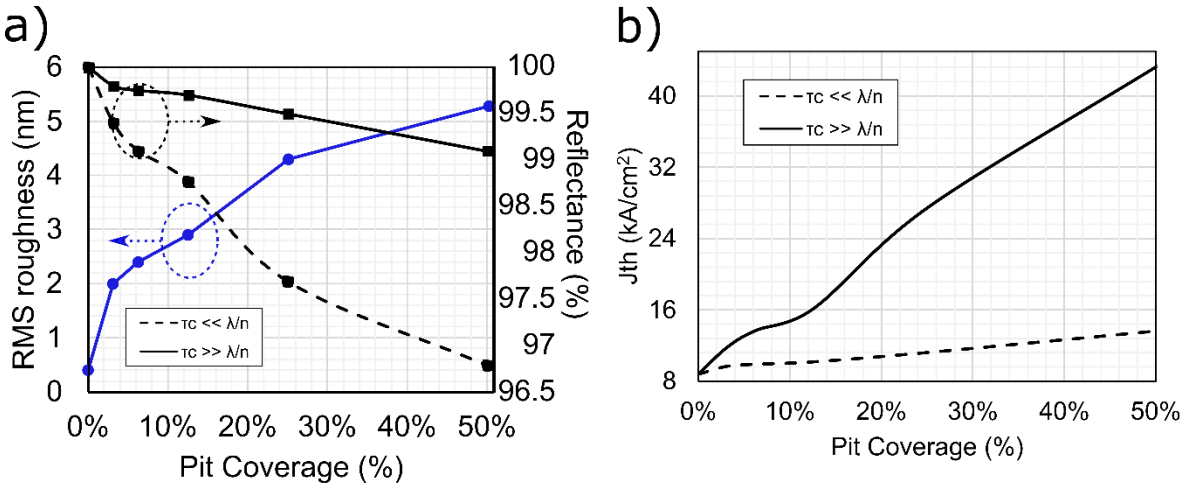

Figure 4.6. (a) Dependence of surface roughness on pit density, (b) calculated dependence of p-DBR peak reflectivity and threshold current density on pit density.

Implementing the modified complex reflection coefficient within the TMM model works as follows: the top layer is treated as the roughened layer, and then the top DBR layers are modified by the scattering factor. In practice, the scattering factor reduces the reflectivity of the p-DBR, increasing the mirror loss, α_m. The dependence of the peak mirror reflectivity is plotted as a function of observed RMS roughness in Figure 4.6 (a). It can be seen that while the mirror reflectance decreases with increasing RMS roughness, a correlation length $\tau_c >> \lambda/n$ severely impacts the mirror, while a correlation length $\tau_c << \lambda/n$ has a lower effect. Surfaces often have both long-range and short-wave correlation lengths[181], so the true p-DBR mirror reflectance is likely somewhere between these two cases. The reflectance values were then taken and plugged into the following equation to estimate J_{th} for a 10μm VCSEL:[182]

$$I_{thMQW} \approx \frac{qN_w V_1 B N_{tr}^2}{\eta_i} exp\left(\frac{2\left(<\alpha_i> + \alpha_m\right)}{N_w \Gamma_{xy} \Gamma_z \Gamma_{enh} g_{0N}}\right) \tag{4.6}$$

where N_w is the number of QWs, V_1 is the volume of a single QW, B is the radiative recombination coefficient, N_{tr} is the transparency carrier density, η_i is the injection efficiency, $<\alpha_i>$ and α_m are the internal and mirror loss, respectively, $\Gamma_{xy}\Gamma_z\Gamma_{enh}$ is the transverse, axial, and enhancement confinement factor of a single QW, and g_{0N} is an empirical gain coefficient. From 1D TMM simulations, the loss and confinement factor, $<\alpha_i>$, and $\Gamma_{xy}\Gamma_z\Gamma_{enh}$, were 2.83cm^{-1} and 0.00138, respectively[183]. The absorption coefficients used to calculate $<\alpha_i>$ were taken from Table 3.1. It was additionally assumed that the coupling efficiency to the 10μm current aperture was the more conservative 63%, and that this also impacted the xy-confinement factor Γxy by the same amount. Using parameters from nonpolar EELDs with similar active regions[184], specifically N_{tr} (8.6x10^{18}cm^{-3}), η_i (0.6), B (1x10^{-11}cm^{3}s^{-1}), and g_{oN} (5400cm^{-1}), the threshold current density of this design was calculated for each mirror

reflectance, plotted in Figure 4.6 (b). The J_{th} increases rapidly with pit density, increasing by over 5x for the $\tau_c >> \lambda/n$ case. The 10μm VCSEL had a J_{th} of 14kA/cm^2, and a pit density of approximately 8% around the location of the mode. The observed J_{th} is comparable to what was predicted by the model but lower, implying that the assumption of uniform RMS roughness was still underestimating the impact of the scattering loss.

The increased scattering loss caused by these pits provides one possible reason for the location of the lasing region on the VCSELs and for the higher order modes. The evidence for this is that the lasing spots generally occurred in areas with a lower pit density. However, it is possible that the higher order transverse modes were caused by non-uniform current injection into the active region due to non-uniform activation of the IIA TJ, an issue exacerbated by the wider 10μm current aperture[103,140].

In summary, we reported 65λ-cavity GaN VCSELs utilizing a topside dielectric curved mirror. For a device with a 10μm current aperture and a curved mirror with a 120μm ROC, single longitudinal-mode operation with a SMSR of 30dB up to 3x J_{th} was observed. Devices lased in a variety of higher order transverse modes, with mode behavior possibly influenced by pits introduced during the lens dry etch. The SiO_2 lens fabrication process offers advantages over prior long cavity curved mirror VCSEL demonstrations, as it can be fabricated using standard techniques and at room temperature. These results show promise for the expanded capabilities of GaN-based VCSELs.

4.1.2 Optimizing the Dielectric Lens

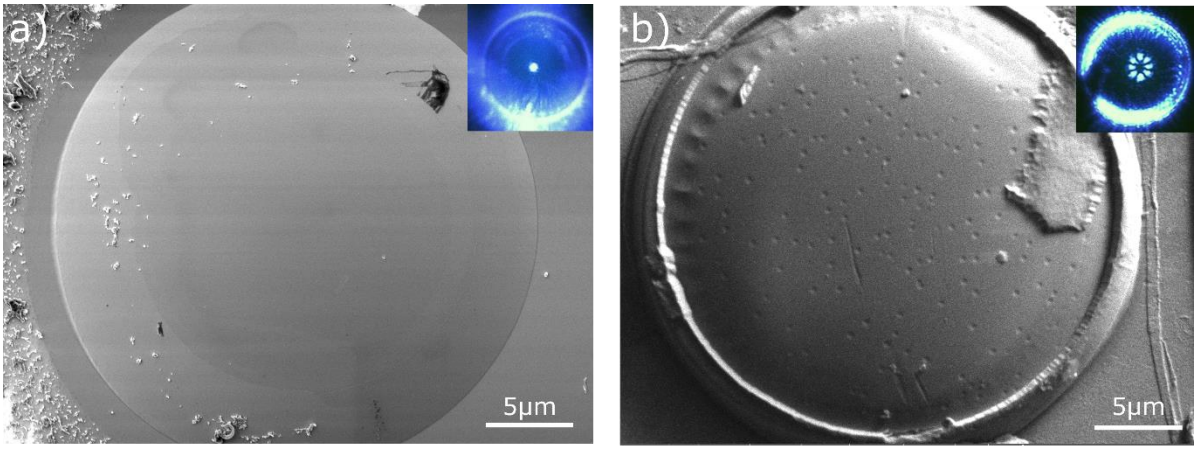

Figure 4.7. Comparison of VCSEL with (a) GaN lens and (b) SiO_2 lens. Inset images are topside NFP produced by the lens shown in the SEM in the main figure.

As noted in the previous section, the SiO_2 lens exhibited pitting across the surface, despite having the expected parabolic curvature. However, the same issue had not been observed with the GaN lens etch, which had smooth morphology across the surface. A comparison figure of the two can be seen in Figure 4.7, showing the VCSEL with a GaN lens from Chapter 3, and the VCSEL with a dielectric lens from the previous section. The inset NFPs were observed from the exact lenses shown in the SEM. The formation of pitting originated in either: the as-deposited dielectric, during the photoresist lens formation, or during the dry etch. To study this effect, 2,400nm SiO_2 was deposited via IBD on Si pieces to study the source of pitting. Note that the thermal conductivity of n-doped Si is comparable to bulk GaN (~150W/m-K vs. 130 W/m-K), and the cost of sample pieces is significantly lower. The as-deposited dielectric material did not show any pitting under AFM, SEM, or optical microscopy, and had an RMS roughness of 0.3nm, comparable to the roughness on a bare *m*-plane GaN substrate. Next, photoresist was spun onto the samples and lenses were formed via reflow. Thermal reflow was performed under the following two conditions: 150°C 90s, 135°C 120s without a

temperature ramp for either case. After reflowing the photoresist to form the lens, no pitting was observed. However, it is noted that there was a wrinkled shape around the edge of the lens reflowed at 150°C 90s, whereas the lens reflowed at 135°C had a much less pronounced disfiguration. The presence of this effect on both lenses points to an issue with the post-exposure or development steps, potentially due to a different effective concentration of solvents remaining post-development. However, we ignored this issue for our devices, as the expected beam diameter was significantly narrower than the diameter of the wrinkles. Figure 4.8 (a) shows a top-down SEM image of a photoresist lens with a reflow temperature of 150°C on top of SiO_2 before any dry etching has occurred. Next, a separate sample was loaded into the RIE-ICP reactor and briefly etched for 2min to study the etch in-progress. Figure 4.8 (b) shows a topdown SEM image of the partially etched lenses, with the main PR lens still mostly unetched. Several pits can be seen in the etch SiO_2 portion of the lens near the

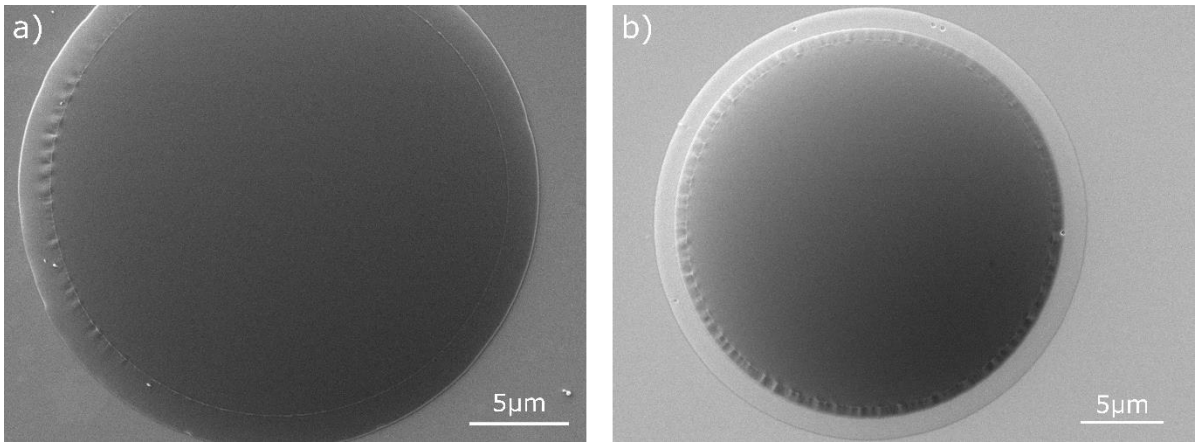

Figure 4.8. (a) SEM of photoresist lens formed via reflow at 150°C for 90s on top of planar SiO_2 film. (b) SEM of same system after 2min etching in RIE-ICP.

photoresist/dielectric interface, verifying that the dry etch nucleates pits and that pit nucleation occurs from the very beginning of the etch. The crinkled edge can still be observed at the edge of the etch interface. Going forward, the reflow temperature was maintained at 135°C to minimize the wrinkle effect.

Next, the samples were again separated into two groups: one was immediately dry etched following the reflow, and the other was allowed to sit at room temperature for 120mins. The aim of the rehydration is to allow any remaining solvents to equilibrate within the lens, and for water to diffuse back in from the ambient environment[185]. While the goal of the photoresist reflow is to force all solvents to diffuse out during the beading/lens transformation, inevitably some solvent can remain. Many resist solvents form azeotropes with water, and the boiling points of these azeotropes can be wildly different, e.g. 53°C lower in the case of PGMEA and its water azeotrope. The dry etch is performed in a He-cooled chamber at room temperature, but the surface of the sample can be significantly above room temperature due to collisions of particles with accelerated electrons and ion bombardment, in the high-density plasma reactors used in this study[161]. Normally, rehydration occurs between the exposure and develop, and is most effective for very thick photoresists, but it can also be critical for complex processes on thinner photoresists, such as this one which relies on total out-diffusion of the solvents. Figure 4.9 shows the comparison between the two lenses etched immediately and after a 120min rehydration period. Whereas the lens etched immediately after the reflow has a pitting profile which reflects the VCSEL lenses, the lens which had the rehydration period shows essentially no pitting. However, despite this, we later found that if the dielectric etch rate was increased past 200nm/min, pits began forming in the lens, albeit at lower densities. While the solution was to ensure the etch remained lower than 200nm/min, this told us that the process required further optimization to be fully rehydrated. The exact gas flows used in the high and low etch rates are unimportant, as each reaction chamber and ambient environment will elicit slightly different conditions. The overall ratio of gas flow for each etch rate was maintained at 3:1:1 CF_4:O_2:CHF_3. The optimal rehydration time is likely longer than 120min, or potentially an

additional rehydration period after the exposure or development may be necessary. However, reducing the etch rate allowed us to move forward without issue.

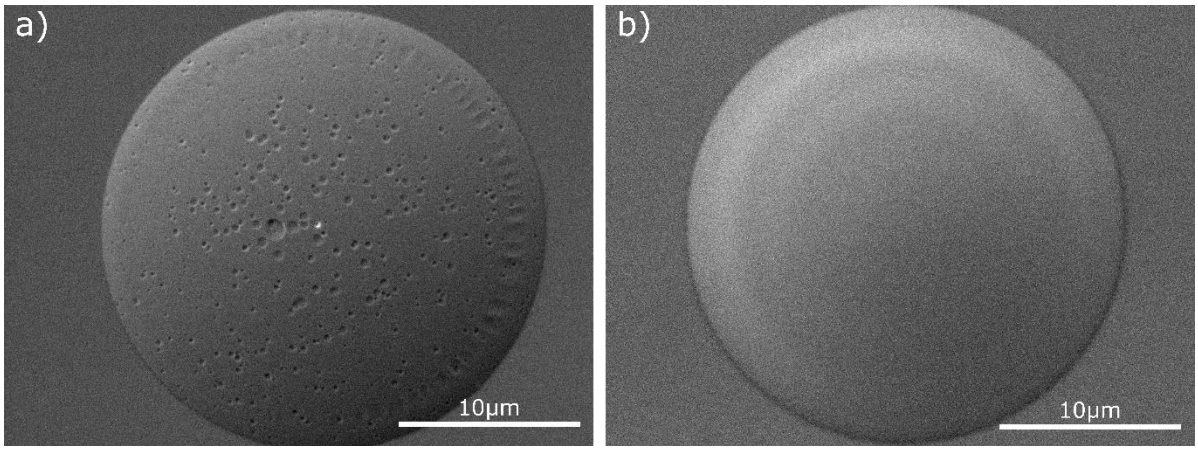

Figure 4.9. SiO_2 lens dry etched (a) immediately and (b) after 120min rehydration period.

In conclusion, the photoresist did not exhibit pitting before the dry etch. The processing of the photoresist, including exposure, develop, reflow, and rehydration time affected the density and depth of pit formation on the SiO_2 layer during the subsequent dry etch. First, reducing the photoresist reflow temperature from 150 °C to 135 °C reduced the prevalence of the outer ring and improved etch consistency. Second, it was important to allow the photoresist to sit at room temperature to re-hydrate and equilibrate solvents for 120min after the photoresist reflow lens formation. Finally, limiting the ICP etch rate below 200nm/min, in conjunction with the pre-etch processing steps discussed previously, fully prevented pit formation.

4.2 Dielectric lens VCSEL with BTJ

After optimizing the dielectric lens etch and removing pitting, another round of devices was fabricated. This time, a BTJ current aperture was chosen to more closely match the design of the GaN lens VCSEL. Devices were fabricated identically to the prior SiO_2 lens VCSEL, with the exception that instead of the formation of the ion implanted aperture, the aperture

was formed using the BTJ process outlined in Chapter 4 for the GaN lens VCSEL. The reasoning for this was that we were suspicious that the BTJ might be providing some additional waveguiding, similar to has been reported previously, and so we wanted to study this more closely[63,175]. A schematic of the device is shown below in Figure 4.10.

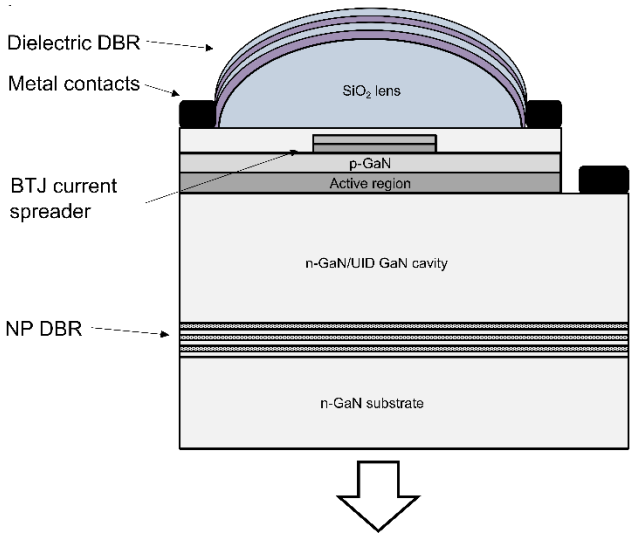

Figure 4.10. Schematic of SiO_2 lens VCSEL with BTJ.

4.2.1 Performance with Incomplete DBR Etch

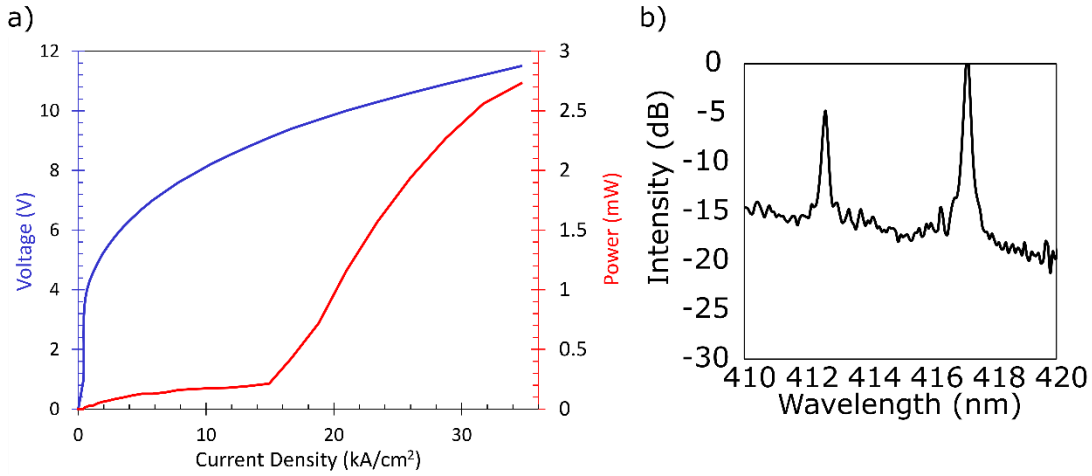

Figure 4.11. a) LIV characteristic of CW operation of a 10µm aperture VCSEL. b) Spectrum at a current density of 16kA/cm^2.

LIV performance of a VCSEL with a 10µm current aperture is shown in Fig 4.11 (a), depicting a threshold current density (J_{th}) of 14kA/cm^2 and a slope efficiency of 0.16 W/A.

Fig 4.11 (b) shows the spectra of the device above threshold at a current density of 16kA/cm^2. The device exhibited multiple longitudinal modes with primary mode at 417.17nm and a secondary mode at 412.59nm. The device exhibited thermal rollover at a current density of 34kA/cm^2 at a peak output power of 2.73mW. Measurements taken on an IR thermal camera showed that the device maintained an operating temperature of 36 °C at a current density of 26kA/cm^2. The differential efficiency was estimated to be 10.6% from the slope efficiency, a significant 10-fold improvement over our previous dielectric lens demonstration which had a differential efficiency below 1%. Additionally, the peak output power improved by over 700%, an increase that is partially attributed to the improved pit-free lens surface.

Topside NFP and bottomside FFP data for this device is shown in Fig. 4.12 (a), showing that the device with a current aperture diameter of 10μm is operating in a higher order transverse mode. This is a deviation from nearby VCSEL devices with a current aperture diameter of 7μm, 8μm and 11μm, respectively on the sample, shown in Fig. 4.12 (b) - (d), which all appear to show Gaussian-like modes under CW operation at threshold. The observed rings across the FFP are attributed to interference caused by the double side polished (DSP) substrate interface. The approximate overlap between the mode and the aperture of the 10μm VCSEL was extracted from the topside NFP by calculating the area of the NFP the corresponded to 1/e^2 intensity and was found to be ~90%. This is significantly higher than what would be expected from the fundamental mode, which would only have a 1/e^2 overlap of 6%. It was observed that VCSELs with current apertures as wide as 11μm consistently lased in the fundamental transverse mode at threshold, and the performance of these devices is discussed in detail in the next section. One possible reason why the above-mentioned device

with a current aperture diameter of 10μm of Fig. 4.12 (a) has a higher order transverse mode is discussed below.

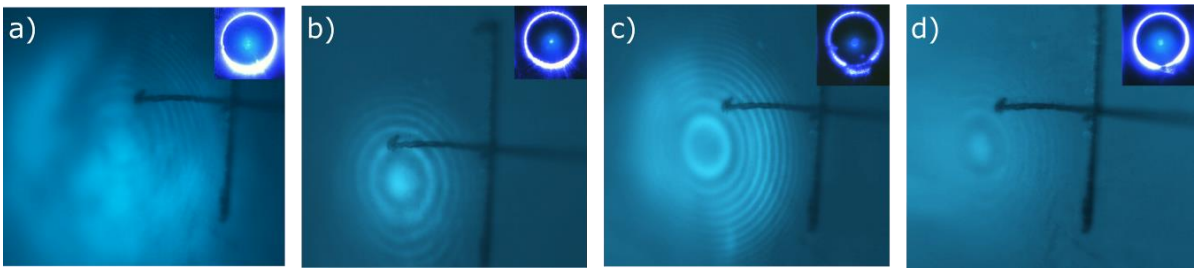

Figure 4.12. Bottomside FFP pattern of a) the tested 10μm VCSEL, and nearby b) 7μm, c) 8μm, and d) 11μm VCSELs. Black cross lines denote 10mm. The inset in each figure shows the corresponding topside NFP.

While testing, it was observed that the NP DBR etch front across the substrate was non-uniform, and the etch front underneath the multi-mode device stopped close to the edge of the current aperture. Notably, every single-mode device that lased was in a region where the etch front completely undercut the devices. It is suspected that this non-uniform etch behavior was caused by variations in the dry etch depth that exposed the sidewalls for the porous etch. An optical microscopy image of a VCSEL that lased single mode is shown in Fig. 4.13 (a), with a black circle denoting the approximate location of the BTJ current aperture. The blue-grey coloration beneath the lens is due to the NP DBR, and minimal discoloration is present, indicating a uniform porous etch characteristic. Fig. 4.13 (b) shows a cross-sectional SEM image of the NP DBR approximately underneath the aperture, taken along the a-direction and parallel to the porous etch direction. It can be seen that the full 22-period NP DBR is present across the device as expected. However, for the multi-mode device, which can be seen in Fig. 4.13 (c), the NP DBR etch front terminates roughly to the left side of the expected aperture location as denoted by black solid arrows. Additionally, a dark line is visible beneath the current aperture, indicating that the etch may have terminated non-uniformly. It was hypothesized that the NP DBR etch front could affect the performance of the VCSEL if it

overlapped with the beam location and could be one cause behind the higher order mode. Fig. 4.13 (d) shows the state of the NP DBR near the aperture. In general, each layer terminated at a different depth, and the upper 9 periods etched farther than the bottom 13 periods. It is suspected that the higher order mode is partially caused by the etch interface, which led to uneven reflectivity across the aperture and may have introduced scattering loss that suppressed the fundamental mode. This is partially supported by the FFP of this device shown in Figure 4.12 (a), which shows a higher emission intensity along the bottom half of the image, which corresponds to the alignment of the partial VCSEL during testing.

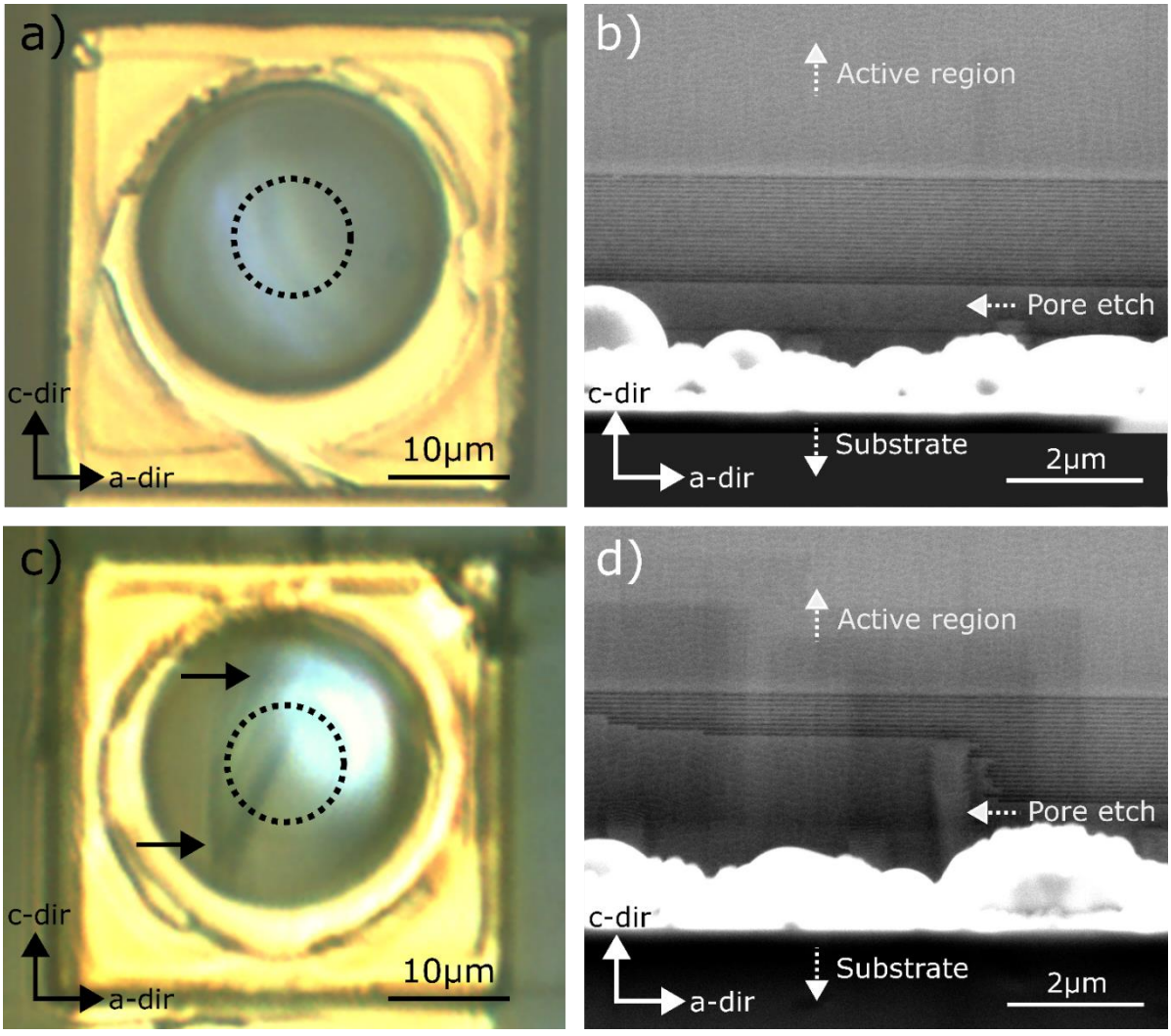

Figure 4.13. a) optical microscopy image of the 10μm VCSEL. The dotted black circle denotes the approximate location of the BTJ. b) cross-sectional SEM image taken along the a-direction.

Besides suppressing the fundamental transverse mode, the 9-period region could impact device performance, namely by increasing the effective mirror loss for the NP DBR side. As previously mentioned, the J_{th} for this device was 14kA/cm^2. A nearby 10μm VCSEL that lased single mode exhibited a J_{th} of 11.4kA/cm^2, implying that the NP DBR etch front increased the J_{th} by 22%. Ignoring other effects, the increased threshold could be due to increased mirror loss through the NP DBR. To analyze this, the expected threshold current density for various NP DBR reflectivites was calculated using Equation 4.6. From 1D TMM, $<\alpha_i>$, α_m, $\Gamma_{xy}\Gamma_z\Gamma_{enh}$, and dielectric DBR reflectivity were determined to be 2.29cm^{-1}, 0.53cm^{-1}, 0.00138, 99.87%, and 99.999%, respectively. Additionally, it was assumed that only 51% of the injected current contributed to stimulated emission due to poor coupling between the 10μm aperture and calculated 7.35μm beam diameter[186]. Considering everything, this VCSEL structure with a 22-period NP DBR that has a peak reflectivity of 99.89% should have a J_{th} of 9.98kA/cm^2. In comparison, a VCSEL with an 18-period NP DBR would have a lower peak reflectivity of 99.53% and a J_{th} of 12.18kA/cm^2, a 23% increase over the 22-period VCSEL. The magnitude of this difference is comparable to what was observed experimentally, leading us to believe that the effective mirror reflectivity of the NP DBR region beneath the multi-mode VCSEL is behaving similarly to an 18-period NP DBR. Future device improvements may decrease the number of NP DBR periods to further increase the output power at the expense of increased threshold current[187].

4.2.2 Single Transverse Mode Performance

Figure 4.14 shows a cross sectional SEM image of the NP DBR, showing a variety of nanoporous structures, including nanopores with diameters smaller than 20nm (white), nanoporous voids with diameters ranging from 50-100nm (yellow), and vertical nanoporous

rods aligned perpendicular to the DBR layer (blue). The porous structures were evenly distributed across the sample, and across the upper and lower DBR layers. Ever since we first

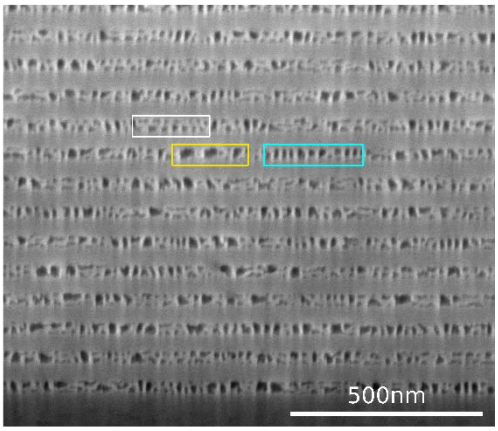

Figure 4.14. a) optical microscopy image of the 10μm VCSEL. The dotted black circle denotes the approximate location of the BTJ. b) cross-sectional SEM image taken along the a-direction.

demonstrated a VCSEL with a NP DBR, we consistently saw these structures. We had also observed that the other groups working on NP DBR VCSELs had not published any data on the farfield pattern of their devices, and so it was an open question whether or not the variance in the void size or porosity fluctuations might be influencing the spatial mode properties. Thus, while the output power and differential efficiencies of the VCSELs surrounding the high output power VCSEL were lower, they served as a useful template for studying the mode properties.

Light-current density-voltage (LJV) curve of a GaN VCSEL with an 8μm current aperture under continuous-wave (CW) operation can be seen in Fig 4.15. (a). The threshold current I_{th} was 4.5mA (J_{th} = 8.92kA/cm^2) and the threshold voltage V_{th} was 7.3V. The emission spectra, Fig. 4.15 (b), was taken at a current density of 30kA/cm^2, approximately 3.3x J_{th}. A primary peak at 406.5nm can be seen with a spectrometer-limited linewidth of 0.23nm, and a side-mode suppression ratio (SMSR) of 21dB to a secondary peak at 408.97. The mode spacing between the two peaks is 2.4nm, which is comparable to the mode spacing estimated using

1D TMM simulations. The slope efficiency is 0.012W/A, leading to a bottomside differential efficiency of 0.4%. The low output power and differential efficiency are partially attributed to the unexpectedly high porosity of the NP DBR, which was designed to have a lower porosity of 28% and subsequently lower reflectivity of 99.55% but exhibited a porosity of 35% and DBR reflectivity of 99.9%. This will be discussed more later.

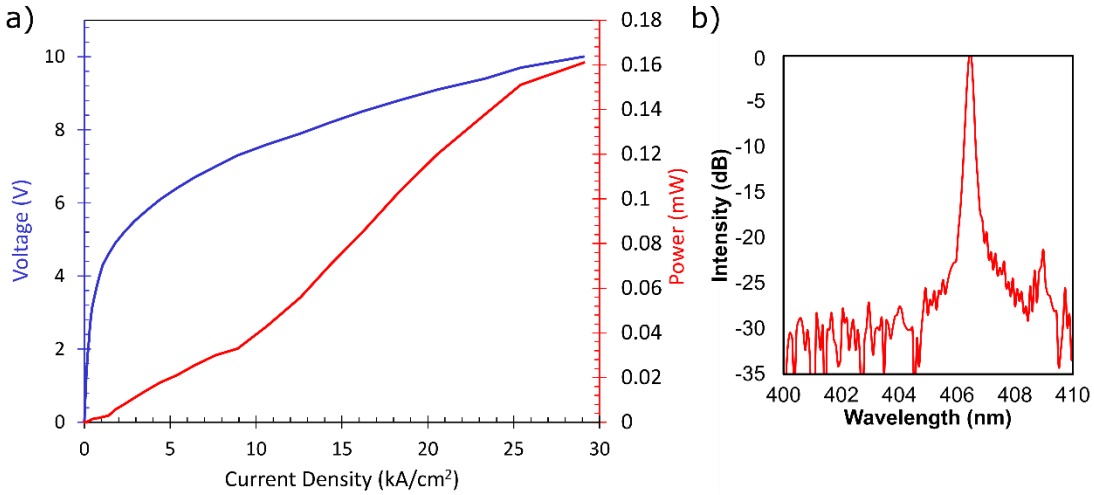

Figure 4.15. a) LIV characteristic of CW operation of an 8µm aperture VCSEL. b) Spectrum at a current density of 30kA/cm^2.

The thermal performance of the long-cavity structure was evaluated by assessing the thermal resistance (R_{th}) of the device, which is typically determined experimentally using the following relationship:

$$R_{th} = \frac{\Delta T}{\Delta P_{diss}} = \frac{\Delta\lambda/\Delta P_{in}}{\Delta\lambda/\Delta T} \tag{4.7}$$

following the measurement of variations in the peak emission wavelength with changes in the input power ($\Delta\lambda/\Delta P_{in}$) and with changes in the heat-sink temperature ($\Delta\lambda/\Delta T$)[131]. Using this method, we observed $\Delta\lambda/\Delta T$ of 0.015nm/K for the measured device with an 8µm current aperture, in line with reported $\Delta\lambda/\Delta T$ values for prior reports which range from 0.012 to 0.0185nm/K[54] and comparable to prior GaN VCSEL demonstrations with a NP DBR which reported 0.014nm/K[188]. The $\Delta\lambda/\Delta P_{in}$ was 9.1 nm/W, leading to a calculated R_{th} of 607 K/W.

This value is comparable with high power long cavity 10λ designs[54], and is in line with calculated values for VCSEL cavities with bottomside epitaxial DBRs[152]. Fig. 4.16 (a) shows

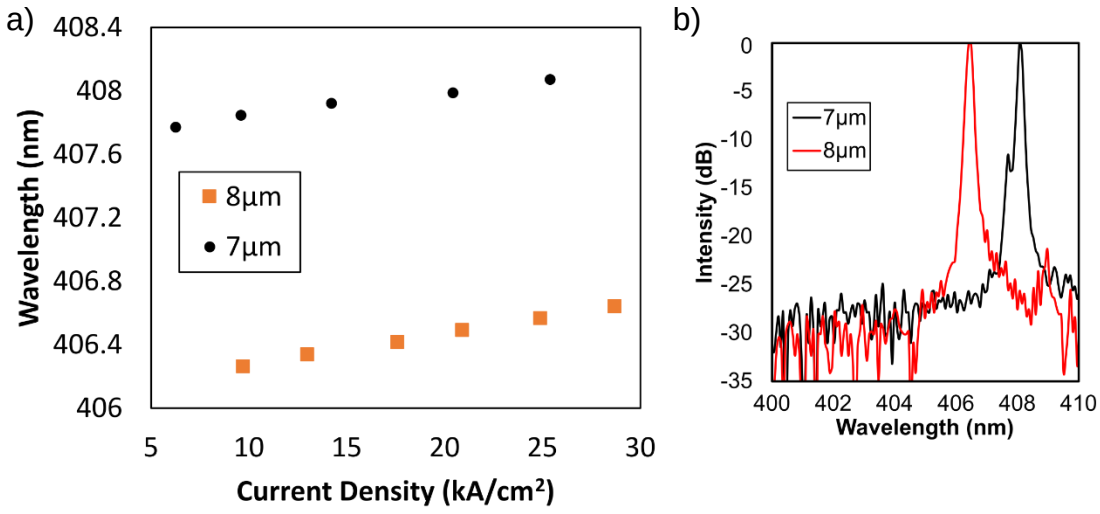

Figure 4.16. a) Dependence of dominant mode on injected current under CW operation for a 7µm and 8µm VCSEL. b) Spectrum for both at a current density of approximately 30kA/cm^2.

the wavelength shift within a 7µm and 8µm aperture device as a function of current density, with both devices exhibiting <0.5nm red-shift in the dominant mode up to a CW current density of 4.1x J_{th} and 3.2x J_{th}, respectively. The spectra at the maximum CW current density are shown in Figure 4.16 (b). This result shows that the long cavity design shows promise for GaN VCSELs utilizing NP DBRs as it minimizes the detrimental impact of the low thermal conductivity of the NP DBR.

Interestingly, it was noticed that some VCSELs, including the 7µm VCSEL seen in Figure 4.16 (b), lased with multiple longitudinal modes that had a spacing significantly lower than what was predicted by the 1D TMM model, 2.2nm. For the 7µm VCSEL, the spacing between the primary and secondary mode was approximately 0.37nm. As will be discussed in the next section, it is unlikely that this mode is related to a higher order spatial mode, as the calculated mode spacing between the fundamental mode LP00 and the next highest order mode LP01 is approximately 0.1nm based on the expected effective index contrast between

the fundamental and first higher order mode[189]. Instead, what we believe is happening is that the non-uniformity in the porous DBR porosity is leading to localized fluctuations in the cavity length, and therefore leading to a region of the device that is slightly blueshifted. This behavior was observed in optically pumped *m*-plane VCSELs utilizing a bottom NP DBR, in which multiple closely spaced longitudinal modes were observed in a cavity with an expected mode spacing of approximately 70nm[98]. Based on the non-uniform porous behavior of our NP DBRs, we believe similar behavior is occurring.

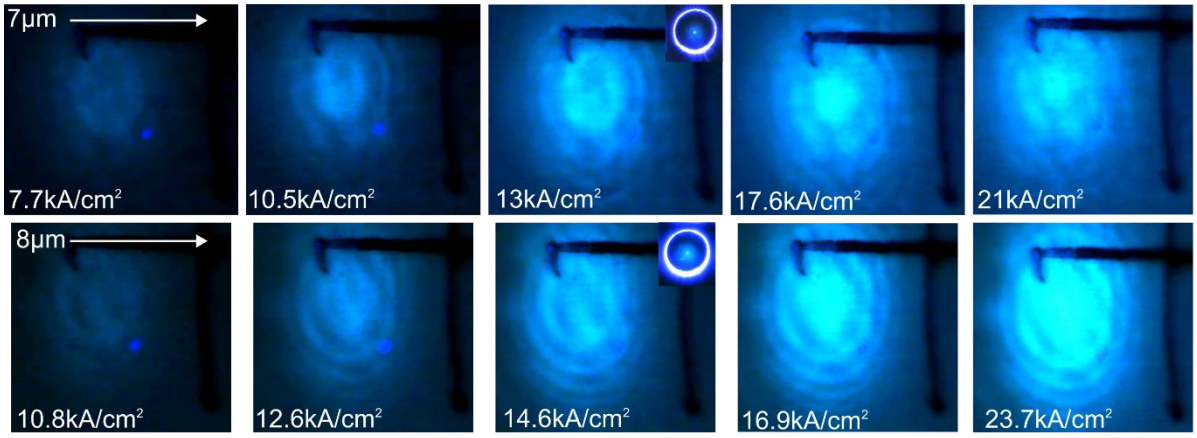

Figure 4.17. Bottomside FFPs as a function of CW current density for a (top) 7μm aperture VCSEL and (bottom) 8μm aperture VCSEL.

Figure. 4.17 shows bottomside FFPs from VCSELs with a 7μm and 8μm current aperture, as a function of current density. Insets of the topside NFPs at 1.9x J_{th} and 1.6x J_{th} are shown, respectively. It can be seen that each device lases in a characteristic similar to the fundamental transverse mode throughout the current injection. From the topside NFP, the beam waist, ω_0, is approximately 1.25μm, similar to the calculated beam waist radius of 1.21μm[177]. The divergence angle extracted from the FFP for the 7μm and 8μm device are 5.78° and 10.11°. These values are slightly lower and higher, respectively, than what is expected by theory[173], calculated using Equation 3.4, which estimates a divergence half-angle of 7.16°.

While measuring, both of the FFP images showed a series of rings with regular distance from the central optical axis. The observed phenomena are similar to an Airy pattern, which consists of a bright central region surrounded by a series of concentric rings. The first minimum corresponding to the first ring occurs at a radial distance r from the center of the pattern, determined by,

$$r = 1.22\frac{\lambda f}{d} \tag{4.8}$$

where *f* is the focal length and *d* is the diameter of the optical aperture. For the VCSEL, *d* is

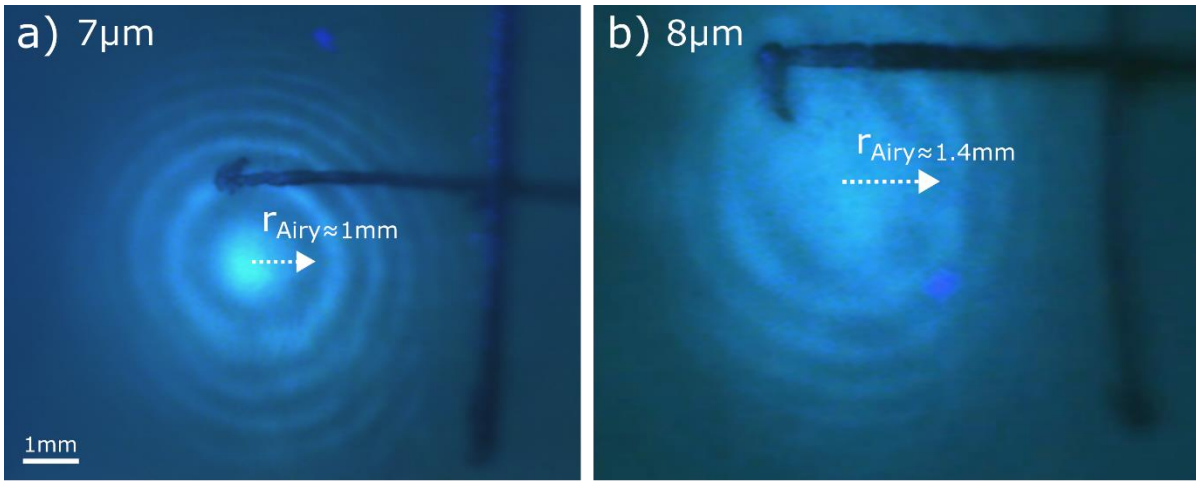

Figure 4.18. Schematic of FFP image showing radius of first minima for a) 7μm VCSEL and b) 8μm VCSEL.

assumed to be equal to the current aperture diameter, and for a screen distance L that is suitably larger than d, *f* can be assumed to equal L. Plugging the appropriate values into Equation 4.8 gives an approximate radius of 1.81mm for the 7μm VCSEL and 1.58mm for the 8μm VCSEL. These are both slightly larger than the experimental values of 1mm and 1.4mm extracted from the FFP, respectively. The accuracy of these measurements is limited by the FFP image measurement, but the values are of the same order of magnitude.

As mentioned previously, some VCSELs displayed higher order modes above J_{th}. Some example higher order modes can be seen in Figure 4.19 (a-c), with the corresponding LG mode shown in the inset.

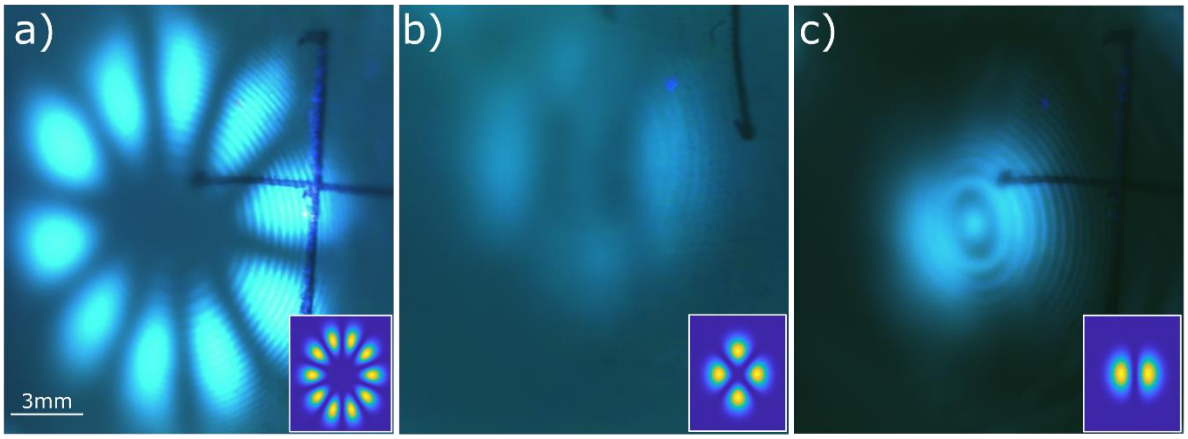

Figure 4.19. FFP for higher order modes observed, with inset showing corresponding Laguerre-Gaussian mode intensity profile. (a) LP_{50} (b) LP_{20} (c) LP_{10}.

The Gaussian beam diameter, $2\omega_z$, at the active region can be calculated using Equation 3.2. For this cavity design, 99.7% of the Gaussian profile is contained in a 7.35μm diameter, and 86.5% of the Gaussian profile is contained in a 2.53μm diameter. Compared to the multi-mode 10μm VCSEL, the differential efficiency of these devices was low, approximately 0.4%. The primary suspicion for this was the low injection efficiency, defined as the overlap with the modal intensity down to $1/e^2$, which was approximately 13% and 10% for the 7μm and 8μm VCSEL, respectively. Figure. 4.20 (a) shows the calculated $1/e^2$ and $1/e^3$ overlap of the fundamental mode for various current aperture diameters. An example of

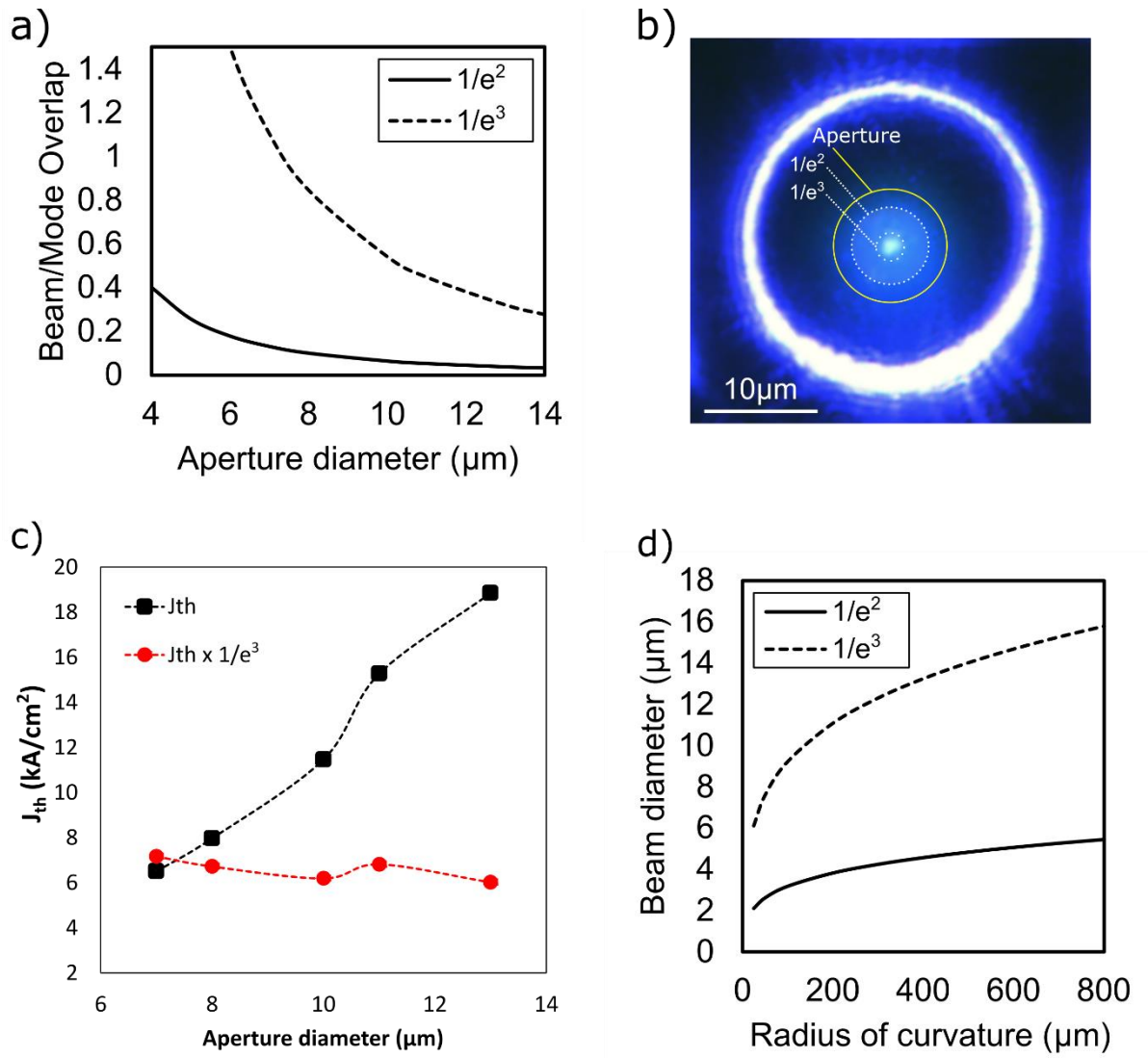

Figure 4.20. a) Dependence of dominant mode on injected current under CW operation for a 7μm and 8μm VCSEL. b) Spectrum at a current density of approximately 30kA/cm^2.

modal overlap with a 10μm aperture is shown in Figure 4.20 (b). Note that for apertures below 7μm the 1/e^3 overlap is higher than 1, meaning the diffraction loss outside of the aperture will be greater than zero. This provides one explanation for not seeing lasing for apertures below 7μm. Above 7μm, the 1/e^3 overlap decreases with increasing aperture size, as expected. In this regime, the emission outside of the mode does not contribute to meaningful gain. Note that the 1/e^2 overlap is quite low for all apertures considered. It was observed that the threshold current density (black) increased with the aperture diameter as shown in Figure. 4.20 (c), an

atypical result for planar GaN VCSELs with uniform current injection. Previous GaN VCSEL reports have observed that the J_{th} appeared to decrease with increasing aperture diameter[60]. This was attributed to non-uniform current injection, which made the assumption of uniform current injection produce the trend[60]. Imaging of the devices above threshold with an IR thermal camera showed a near uniform distribution of heat, indicating that current crowding effects are likely not a dominant contributing factor here. However, multiplying J_{th} by the $1/e^3$ mode overlap ratio yields a nearly uniform J_{th} which is shown in Figure. 4.20 (c) in red. This provides evidence that the $1/e^3$ modal overlap may provide more accurate insight into the behavior of our devices relative to the $1/e^2$ modal overlap. It also indicates that by increasing the diameter of the Gaussian profile, $2\omega_z$, larger overlaps could be achieved for wider current apertures. Assuming the effective index and lasing wavelength remain constant, then ω_z can be tuned by either placing the active region farther from the planar mirror, i.e. increasing z, or by increasing the beam waist ω_0. The active region is already placed near the top of the epitaxial layers, limiting the ability to increase z without increasing the overall cavity length. By contrast, ω_0 may be increased by increasing the ROC of the topside lens. Figure. 4.20 (d) shows the expected increase of the beam diameter as a function of ROC looking at both the $1/e^2$ and $1/e^3$ overlap condition. The optimal condition for a given current aperture diameter and ROC is likely somewhere within the bounds defined by the $1/e^2$ and $1/e^3$ overlap condition, which gives insight into the injection efficiency and internal loss, respectively. Hamaguchi et al recently explored this space and achieved the single transverse mode for a 8μm current aperture using lenses with ROC values greater than 170μm[61].

4.3 Conclusion

In summary, 65λ-cavity GaN VCSELs utilizing a topside curved dielectric mirror and NP DBR were successfully fabricated. Initial VCSEL structures with ion-implanted apertures did not lase CW and exhibited higher order spatial mode operation. The performance of these devices was inhibited by pitting across the lens surface. After optimizing the lens structure to remove pitting, a second round of VCSELs with a BTJ aperture lased CW in the single spatial mode. The BTJ provided a slight optical confinement, aiding in the generation of the single mode. Additionally, a device with an incomplete NP DBR etch exhibited a high output power above 2mW.

5 Conclusions and Future Work

In summary, we have demonstrated the first GaN VCSELs with a long cavity (L>60λ), a topside lens, and a NP DBR. The topside lens fabrication process was developed for both GaN and dielectric materials, demonstrating the flexibility of this process. For the NP DBR, an etch setup was designed specifically for etching fragile, conductive bulk GaN substrates. The long cavity design enabled several CW demonstrations up to higher current densities than what was previously demonstrated by other NP DBR GaN VCSELs, and a thermal impedance of 600 K/W was achieved. Notably, filamentary lasing was not observed across any of the demonstrations. Instead, only the fundamental mode or organized higher order modes were observed.

Table 5.1 provides a performance summary of the 4 devices analyzed throughout this thesis (note that only the 8μm single mode VCSEL is included). The mode diameter is the

estimated diameter of the fundamental mode using the $1/e^3$ condition. The differential efficiency was extracted from the slope efficiency.

Figure 5.1. Performance summary of GaN VCSELs discussed in Chapters 3 and 4.

Device	**ROC (μm)**	**Aperture (μm)**	**Mode Diameter (μm)**	**Mode/Aperture overlap ($1/e^2$ | $1/e^3$)**	**NP DBR R_{calc} (%)**	**Jth (kA/cm^2)**	**Vth (V)**	**η_d (%)**	**P_{max} (mW)**
GaN Lens w/BTJ	30	9	5.8	0.05 | 0.41	99.62	7.3	8.8	0.4%	0.13
SiO_2 Lens w/IIA	120	10	9.1	0.1 | 0.83	99.67	14	11.3	0.6%	0.37
SiO_2 Lens w/BTJ	45	8	7.35	0.1 | 0.54	99.89	8.92	7.3	0.4%	0.161
SiO_2 Lens w/BTJ	45	10	*	0.9 | 0.99	99.53	14	9.1	5.3%	2.73

Throughout the device process rounds, it was observed that apertures smaller than 8μm struggled to lase. The exact cause of this is still under investigation, but it is partly attributed to increased diffraction loss outside of the aperture and processing challenges. One consequence of this was that the $1/e^2$ injection efficiency for the 8 - 10μm current apertures was suboptimal, ranging from 0.05 – 0.1 for the single spatial mode VCSELs. One notable exception was the multi-mode 10μm VCSEL which had an estimated $1/e^2$ overlap of 0.9. This was caused by an incomplete NP DBR etch which led to a non-uniform bottom mirror reflectivity and contributed to both anomalously high output power and differential efficiency.

The lack of precise control over the NP DBR etch condition was a persistent issue throughout every device fabrication. For the GaN lens VCSEL, the NP DBR stopband was unexpectedly blueshifted due to MOCVD reactor drift, leading to low device yield. In the SiO_2 lens VCSEL with a BTJ aperture, the NP DBR etch led to a higher than expected porosity of 35%, possibly due to an unexpected increase in the n-doping, a reduction in the contact resistance through the substrate, or something else. The NP etch also proceeded non-

uniformly, leading to the aforementioned high power VCSEL. For the VCSELs with a fully etched NP DBR, the higher-than-expected porosity reduced mirror loss, leading to a lower differential efficiency.

Besides the processing issues with the NP DBR, the devices all exhibited a high threshold voltage, V_{th}. Across the 4 devices, the average threshold voltage was 9.1V. This is almost a 4V penalty from the field average of 5.3V, calculated from a selection of recent VCSEL demonstrations from outside UCSB[10,51,52,81,91,100,174]. The high voltage contributed to thermal rollover at lower current densities and limited the pumping range of all devices. The primary contributor to excess voltage was the TJ, as almost all TJ VCSEL demonstrations have shown a voltage penalty relative to ITO VCSELs. However, it is possible that unexpected dopant fluctuations in the top or bottom n-GaN current spreading layers contributed to increased series resistance.

The cavity structures performed quite well in several ways. First, the thermal impedance value of 600 K/W is a significant improvement over prior dual dielectric DBR designs, representing a 70% decrease compared with the last reported thermal impedance from UCSB[187]. Because of this, we were able to demonstrate CW lasing multiple times and characterize the FFP mode structure more rigorously. On the topic of mode control, another aspect of the performance worth highlighting is that we did not observe filamentary lasing for any of the devices. Often, higher order spatial modes were observed, but they were always organized higher order modes, as opposed to prior GaN VCSELs experiencing filamentary lasing of complex, disorganized higher order mode structures. This is primarily attributed to the curved lens, which provided optical confinement, and secondarily attributed to the BTJ current aperture, which helped promote the fundamental mode. Finally, one aspect worth

highlighting is the ease and flexibility of fabrication of the topside lens. Lenses with a variety of properties were explored across two different material systems. Fabricating the lens on the top of the device removed the requirement for substrate removal, greatly lowering the barrier for incorporating a lens into future GaN VCSEL processes. The current limitations of the bottomside lens include: requires CMP substrate removal, only possible on bulk GaN substrates, minimum cavity length ~20μm, only possible with a dual dielectric DBR scheme. For GaN VCSEL designs which may benefit from the optical confinement of a lens but require a deviation from these limits, the topside lens is a better fit.

There are multiple directions for this project. The first and most direct approach would be to focus on improving the device performance. As mentioned, the device performance was generally limited by the high threshold voltage and series resistance introduced by the TJ, and possible other sources. This would require some combination of improving the TJ activation parameters, as well as improving the TJ regrowth and optimizing the contact doping. This could be accomplished by adding an InGaN interlayer between the p+/n+ interface to increase the tunneling probability[190]. Additionally, the contact quality of the top and bottom n-GaN contacts was never fully characterized, and there may be performance gains to be had.

One option for "optimizing" the TJ would be to replace the TJ with ITO. While this would increase absorption loss from the ITO layer, this effect is less detrimental for long cavity designs with multiple available longitudinal modes. While this would introduce a planar aperture, convex optical guiding could be re-introduced by depositing a dielectric spacer, ex. Ta_2O_5, and then dry etching the spacer to achieve index contrast similar to the BTJ. This method could be combined with a topside lens to create some novel structures.

Besides improving the voltage, the NP DBR requires significant optimization efforts to achieve the desired yield and performance consistency benefits of a dielectric DBR. In fact, after this PhD experience, I am not convinced that the NP DBR provides enough benefits to outweigh its downsides, which include non-uniform porosity, high variance in the porosity due to fluctuations in the contact resistance, and mechanical stability of the porous structure post-etch. Since VCSEL performance is so highly sensitive to the state of both top and bottom DBR mirrors, I encourage further exploration of other alternative DBR options. From the literature review for this thesis, the AlInN/GaN DBR provides a promising path forward. It appears that major industry players, including Meijo University and Nichia Corp, are consolidating around this approach. The downside here is that the publication space for AlInN/GaN DBRs will become increasingly crowded. Alternatively, there may be value in re-visiting aspects of the ELO VCSEL design demonstrated by Hamaguchi in 2016[59]. While the thermal stress gradients in the dielectric DBR slab led to the authors abandoning the project, recent advancements in lift-off of ELO-grown GaN show promise for flip-chip VCSEL designs that circumvent the need for PEC or CMP[191]. If sticking with the NP DBR, transitioning from Si to Ge as the n-dopant for the n+-GaN layers would allow for an order of magnitude increase in the dopant concentrations, from ~$3x10^{19}cm^{-3}$ to $3x10^{20}cm^{-3}$ and beyond[192,193]. This would allow for much finer control of both the pore size as well as the pore uniformity, and this approach has already been adopted by the team at Yale University. This could potentially also be used to improve the TJ performance issue described above.

In addition to exploring alternative DBR options, the general philosophy of the emission side DBR should be re-examined. Throughout this project, the goal for each VCSEL round was simply to achieve lasing. This led to conservative emission DBR design to minimize the

expected mirror loss contribution and thus maximize the odds of reaching threshold. While this is a fine approach when exploring new device designs with significant unknowns, or with shorter cavities which have a higher chance of unexpected loss due to misalignment between the cavity and resonant mode, the approach was detrimental for the long cavity design. This is best exemplified by the accidental high power VCSEL which had an incomplete NP DBR with a lower effective mirror reflectivity. By reducing the number of mirror periods for the emission side DBR, the power can be greatly increased at the expense of also increasing the threshold current. However, since this does increase the risk of increasing the mirror loss too high, the recommendation here is to fabricate multiple VCSEL samples with different numbers of mirror periods that range from conservative (>99.9%) to risky (99 – 99.75%) reflectivities. This is, of course, easiest to implement with dielectric DBRs compared to epitaxial DBRs.

Another direction to explore would be to implement the topside lens on short cavity VCSELs. The lens provides optical confinement and appears to suppress filamentary lasing, so by combining the lens with a short cavity, single longitudinal lasing should be achieved. However, this removes the thermal advantage provided by long cavities, so this should only be explored for applications which have strict requirements for single mode operation.

On the topic of lens fabrication, there are many different aspects of the design space to explore. One option is to explore lenses with larger ROC to achieve single mode performance and improve overlap with wider current apertures. Another option is to develop an air-gap lens structure, which is the end-game structure for low-loss lens materials. An air-gap lens could also enable the fabrication of the lens on top of complex hole structures for further mode control, as discussed below.

A final direction to explore would be methods to achieve fundamental mode control for larger apertures. It was observed that BTJ current apertures larger than 8μm lased in the fundamental mode around J_{th}, but higher order modes quickly turned on with increasing current injection. This makes sense given the larger volume of higher order modes. However, there have been a variety of successful strategies implemented in VCSELs in other material systems. One particularly interesting strategy is the "holey" VCSEL, wherein shapes are etched in the path of the optical aperture to introduce scattering loss to particular modes[140]. The use of triangular shapes allows for the scattering loss to affect the higher order modes to a greater degree, enabling fundamental mode operation. This could be accomplished by etching into the topside dielectric lens, which would prevent the etch from introducing current leakage from the etched GaN sidewall. Alternatively, shapes could be etched into the GaN to provide both selective scattering loss as well as reduce the lateral pathway for hydrogen diffusion during the TJ activation.

Since 2008, there have been numerous advances from multiple research groups leading to large improvements in performance. Recently, the field has been seriously considering long cavity designs due to the improvements in thermal performance which have prevented GaN VCSEL commercialization to date. The GaN VCSEL design space is still largely unexplored, and there are numerous productive paths for future development. Good luck.

6 References

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