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Ultra-wide Band On-Chip Circulators with Sequentially-Switched Delay Lines (SSDL)



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# Ultra-wide Band On-Chip Circulators with Sequentially-Switched Delay Lines (SSDL)

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical and Computer Engineering

by

Mathew Michael Biedka

2019

ABSTRACT OF THE DISSERTATION

Ultra-wide Band On-Chip Circulators with
Sequentially-Switched Delay Lines (SSDL)

by

Mathew Michael Biedka
Doctor of Philosophy in
Electrical and Computer Engineering
University of California, Los Angeles, 2019
Professor Yuanxun Wang, Chair

As more and more people and devices become connected across the globe, the strain on the RF spectrum that they use to communicate increases. Current methods of communication typically separate transmit and receive information into frequency channels or time slots which leads to inefficiency due to the presence of guard bands or guard intervals. Wireless communication systems of the future will need to be able to transmit and receive electrical signals at the same time and over the same frequency. This is known as Full Duplex communication, which is achievable through the use of a circulator. Typical circulators are able to separate transmit and receive paths to achieve Full Duplex communication through the biasing of magnetic materials. They provide low loss from port to port as well as high power handling that is needed for the transmit path. These circulators are cavities that support non-reciprocal resonant modes which lack wideband performance. Also, their physical size is dependent upon the wavelength of operation, which makes them difficult to integrate with modern IC technology. As a solution to

these challenges, the Sequentially-Switched Delay Lines (SSDL) Circulator is proposed. The switches are turned on and off sequentially to distribute and route the propagating electromagnetic waves, allowing for simultaneous transmission and reception of signals through the device. There is no theoretical limit to the operating frequency range of the SSDL circulator, as the only requirement for operation is the synchronization of the switch timing and propagation delay. Experimental results for the original SSDL architecture composed of five RF switches and six transmission delay lines (six-line SSDL Circulator), along with a simplified design which preserves the nonreciprocal behavior (two-line SSDL Circulator) are reported. Preliminary results for the six-line SSDL Circulator using commercially available parts demonstrate isolation between the transmit and receive paths greater than 40dB from 200 KHz to 200 MHz. In addition, experimental results of both SSDL Circulator architectures on a GaN MMIC achieve full duplex behavior from DC up to 1 GHz.

The dissertation of Mathew Michael Biedka is approved.

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## PUBLICATIONS

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M. M. Biedka, R. Zhu, Q. M. Xu, and Y. E. Wang, "Ultra-wide band on-chip circulators for full-duplex communications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Philadelphia, PA, USA, Jun. 2018, pp. 987–990.

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M. Biedka, P. Rodgers, N. Gutierrez, T. LaRocca, and Y. E. Wang, "100MHz to 1GHz On-Chip Circulator with Integrated Driver Amplifiers," *IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, USA, June 2019, pp. 1-4.

# CHAPTER 1

# Introduction

## 1.1 Challenges faced in the RF spectrum

Wireless communication systems of the present have continually pushed the boundaries of operating bandwidth and physical size, and have lowered their production cost as integrated circuit (IC) technology has matured. However, as more and more users continue to move into an already crowded spectrum, novel techniques must be developed to ease the tension on the RF spectrum.

The Shannon Theorem [1] states that the upper bound of a data link, or the maximum data rate in a wireless channel, is a product of the available bandwidth and the logarithmic function of the signal-to-noise ratio. One of the ways in which this upper bound can be increased is by increasing the available bandwidth. But as was previously mentioned, the continual influx of spectrum users causes the available frequency resource to continually shrink. This means that new techniques must be developed to make the existing spectrum more efficient, as traditional means of communication are quickly being exhausted.

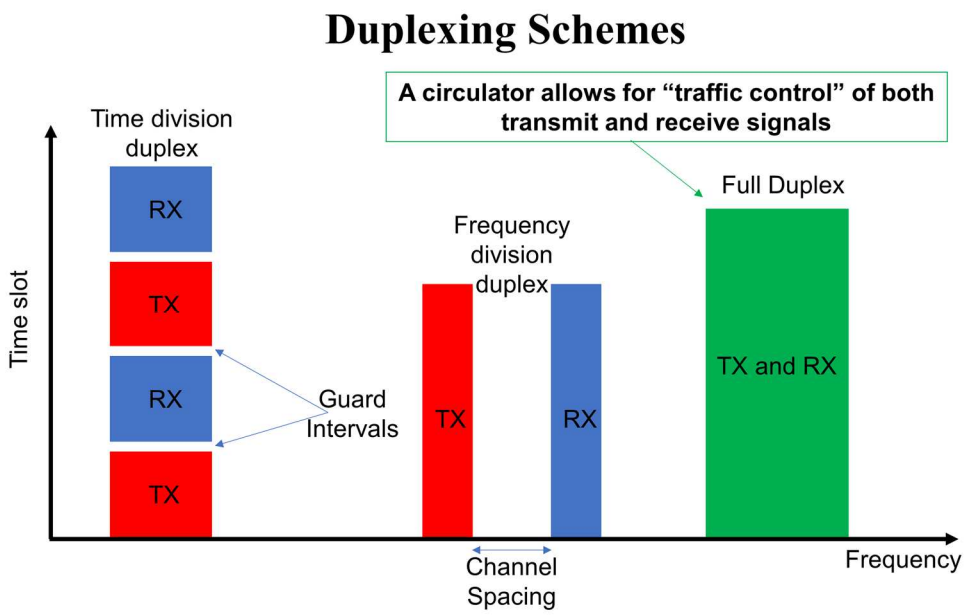



Figure 1.1: An illustration of time division duplex, frequency division duplex, and full duplex.

### 1.1.1 Duplexing Schemes

Communication systems that are currently in use contain terminals such as base stations and cellular phones that function as both transmitters and receivers. This is achieved through either time division duplex or frequency division duplex. Time division duplex (left of Figure 1.1) separates transmitted and received information into different time slots, while frequency division duplex (center of Figure 1.1) separates transmitted and received signals into different frequency channels. Both TDD and FDD are known as out-of-band full duplex due to the separation of the transmitted and received signals in time or frequency. The fixed bandwidth allocation of FDD and the guard intervals which separate the uplink and downlink in TDD have a negative impact on a spectrum which is becoming more and more scarce [2, 3]. There is a way to capitalize on the unused spectral resources of TDD and FDD, and this is known as full duplex.

As shown on the far right of Figure 1.1, full duplex communication [2], also known as in-band full duplex, is the ability to transmit and receive simultaneously over the same frequency band. This has the prospect of doubling the spectral efficiency, as both transmitted and received signals now share the same frequency channel. However, one of the main challenges when dealing with full duplex communication is the in-band self-interference caused by the transmitter which has a power much larger than the receiver, making in-band full duplex generally not possible [4]. This has led to recent works which have provided strategies for the suppression of this self-interference and have successfully demonstrated the advantages of in-band full duplex over out-of-band full duplex [5−9]. While cancellation techniques must occur in the analog and digital domains [9], the focus of the work here is on the circulator, which is the first line of defense in providing isolation between the transmit and receive signals.

### 1.1.2 Full Duplex Front-End Challenges

One approach to alleviate the self-interference between the transmit and receive paths is to separate the antennas used for transmitting and receiving [5−7]. Although this approach has been successful, separate antennas are not favorable for compact wireless systems. Also, the additional antennas used to separate transmit and receive signals could be utilized in a single package to form a MIMO antenna. For these reasons, monostatic (single antenna) in-band full duplex [8, 9] is highly desired, and the circulator presented here focuses on monostatic applications.

The majority of single antenna systems use a device called a duplexer that is responsible for routing the transmitted signal out through the antenna and routing the received signal from the antenna to the receiver. The duplexer also provides the initial amount of isolation between the transmitter and receiver ports. Figure 1.2 shows a simplified diagram of a duplexer which connects

a transmitter and receiver to a single antenna. In terms of out-of-band full duplex operation, this duplexer could be a switch for time division duplexing or a diplexer for frequency division duplexing. In the case of in-band full duplex, a circulator is used to connect the transmitter and receiver to the shared antenna, which is the subject of this work. The performance of the circulator used in a single antenna system will be elaborated on in the next section.

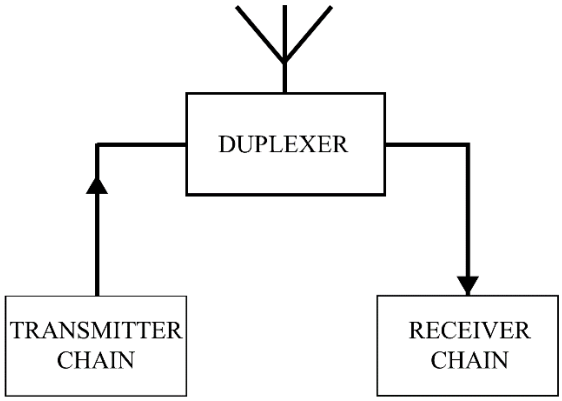



Figure 1.2: An illustration of a transceiver and the position of the duplexer nearest to the antenna.

## 1.2 Circulators for Single Antenna Full Duplex

A three-port network cannot be lossless, matched, and reciprocal at the same time. However, if one of these conditions is relaxed, a physically realizable device can be constructed [10]. A circulator is a nonreciprocal device, meaning that a signal is allowed to propagate in one direction and not backwards. This then allows the lossless and matched conditions of the three-port device to be enforced. This device operates in a way similar to that of a traffic roundabout. However, instead of vehicles being able to travel the entire distance around the structure, they must exit at the next available point. This rule applies to all vehicle traffic entering and exiting this modified roundabout. This means that traffic moving in different directions will stay separated

from each other, as shown below at the left of Figure 1.3. A circulator performs this same operation but for electrical signals, as demonstrated at the right of Figure 1.3. In the ideal case, a circulator is perfectly matched at all three ports, has zero insertion loss in the forward paths (port 1 to port 2, port 2 to port 3, and port 3 to port 1), and infinite isolation in the reverse paths (port 2 to port 1, port 3 to port 2, and port 1 to port 3). The circulator shown in Figure 1.3 provides circulation in the clockwise direction, but circulation in the counterclockwise direction is also possible. Also, circulators with more than three ports can be constructed.

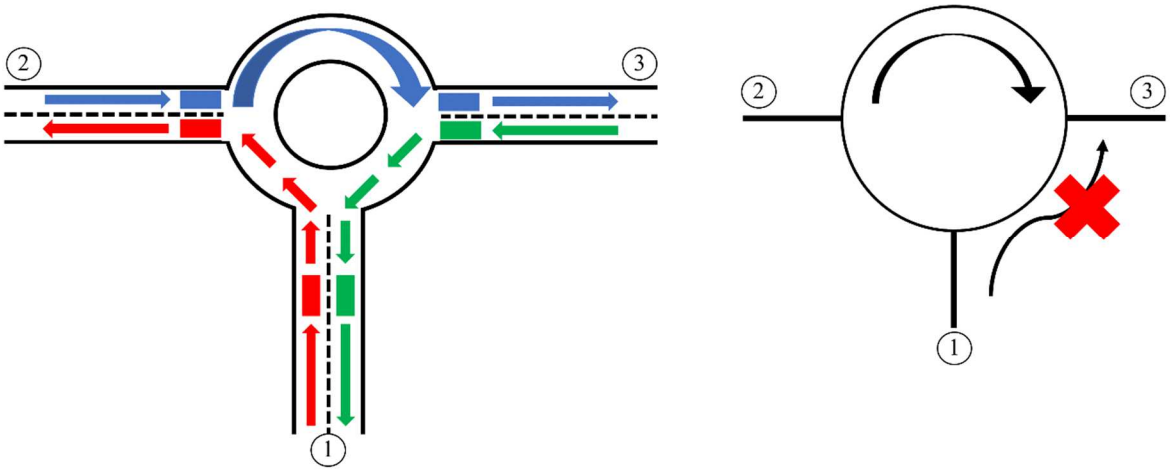



Figure 1.3: Illustration of the analogy between a traffic roundabout (left) and a radio frequency circulator (right).

When a circulator is used as the duplexer in Figure 1.2, there are many practical issues that must be addressed so that the transmitter and receiver can both operate effectively while in close proximity. When observing the right side of Figure 1.3, imagine that the transmitter (TX) chain is connected to port 1, the antenna (ANT) is connected to port 2, and the receiver (RX) chain is connected to port 3. A huge concern is the possibility of the TX signal leaking into the receiver path, which is represented by the arrow with the red "X" through it pointing from port 1 back to

port 3. This is a common problem due to the TX power being much greater than that of the RX power. The amount of leaked power into the RX path needs to be as small as possible, and the metric known as TX/RX isolation is the measurement of this leakage. The circulator also has to provide low loss from port to port to enable proper transmission and reception of electrical signals, while successfully handling the high TX power and required RX sensitivity. Other concerns are the physical size of the circulator as it pertains to integration with transceiver electronics, and the operating bandwidth of the circulator.

### 1.2.1 Ferrite Circulators

Traditional circulators are mainly composed of ferrite disks housed in a cylindrical cavity, and the circulation occurs when a magnetic field is applied to them through a biasing magnet [11−14]. Ferrite circulators which are commercially available can operate with port-to-port insertion loss of 1dB or less, with isolation greater than 20dB. These circulators are passive components, meaning that the noise figure is equivalent to the insertion loss. This is advantageous for the received signal, where additional noise must be minimized to avoid distorting the signal. Ferrite circulators are capable of handling TX power on the order of 10s of Watts. However, their physical size is dependent upon the wavelength of operation [15]. As the operating frequency decreases, the physical size of the ferrite circulator increases, meaning that an inherent tradeoff between operating frequency and size exists. This means that ferrite-based circulators are not easily combined with integrated circuit (IC) technology that currently exists. In addition, ferrite material is not compatible with IC processes, further increasing the difficulty of integration.

### 1.2.2 Active and Metamaterial Circulators

A considerable amount of work has been conducted to realize circulators by exploiting the nonreciprocal transfer function of transistors. Early work in this area using three transistors provided experimental evidence that an active circulator could be realized [16]. As the integration capabilities of transistor technology advanced, monolithic microwave integrated circuit (MMIC) implementations of active circulators were demonstrated [17−19]. However, the power handling capabilities of these circulator are limited, and contribute considerable noise figure to the system performance due to their active nature [20 − 22]. In [23− 25], a magnetless nonreciprocal metamaterial (MNM) is proposed as a circulator. It consists of traveling-wave resonant ring particles loaded by transistors, which exhibit some characteristics of ferrite-based devices without their physical size and cost drawbacks. Although the measured performance reported does not currently compare to that of state-of-the-art commercial ferrite circulators, this approach provides a proof-of-concept that MNM technology has the potential for use in MMICs with substantial benefits over ferrite and active-based circulators.

## 1.3 Nonreciprocity based on Photonics and Time-Modulation

There has been recent interest in the development of nonreciprocal devices based on time-modulation of transmission lines or of a material's properties [26-60]. The original ideas of achieving nonreciprocity were proposed in the field of photonics [26− 28], and the focus of discussions here are based on nonreciprocal devices developed for use in RF systems [29−60]. In [29−33], the concept of angular momentum biasing is introduced. The concept is based on the parametric modulation of three identical coupled resonators. Their resonant frequencies are modulated by external signals with the same amplitude and a relative phase difference of 120

degrees, imparting an effective electronic angular momentum to the system. [29−31] demonstrate the validity of the proposed concept. However, the insertion loss is large and the operating bandwidth is very narrow. In [32,33], major improvements to the concept are achieved. The measured insertion loss is approximately 2dB, with power handling greater than +28dBm over a 20dB TX/RX isolation bandwidth of 25MHz. In [34], nonreciprocal behavior is demonstrated through the commutation of MEMS resonators with a total power consumption of approximately 38uW. The introduction of time-varying components in a transmission line structure also lead to nonreciprocal behavior at RF. The directional dependency in the frequency mixing behavior of a time-varying transmission line (TVTL) can be used to separate signals overlapping in time, frequency, and space. In [35−39], implementations of TVTL on a printed circuit board (PCB) and a MMIC show nonreciprocal behavior over a 3:1 bandwidth, due to the non-resonant nature of the traveling wave structure.

Significant interest has been focused on creating nonreciprocal behavior through switching. A switching-based circulator was first demonstrated on a CMOS chip utilizing a nonreciprocal phase shifter, or gyrator, formed by a staggering commutating N-path filter [40−42]. The gyrator was later extended to a switched delay line configuration [43−50] in order to take advantage of the broad bandwidth offered by this approach. An Ultra-Wide Band circulator operating from DC to RF based on the concept of Sequentially-Switched Delay Lines (SSDL) was first proposed and demonstrated with off-the-shelf components in [51]. In addition to all of these demonstrations, several variations and realizations of a similar concept were reported in [52−55]. In particular, [54] presented a nonreciprocal network based on switched acoustic delay lines to create a significant delay time with compact physical size. This allows a reduction in the switching frequency which relaxes the performance requirement of the switch itself.

The SSDL concept is based on a series of sequential switching actions that are added to the electrical signal path in a speed synchronous to that of the signal propagating on the path. The SSDL circulator is a true time delay device. The only condition of operation is that the switching action is synchronized with the wave propagation in one direction, meaning that nonreciprocity can be achieved independent of frequency. However, this assumes that there is no frequency dispersion in the signal propagation path. Some preliminary experimental results over different generations of MMIC implementations have been briefly reported in [56−60]. The focus of this work is a comprehensive summary of the latest results which include design considerations and performance limits. In particular, when comparing with other circulator designs based on switched delay lines, this work chooses to switch at a frequency much higher than that of the RF signal frequency present in the circulator. As will be explained in more detail, this choice allows for the RF to be recovered at its output port without the presence of mixing tones if a lowpass filter is applied to the output port. This decision to switch at a very high frequency presents new design challenges which will be addressed in this work.

## 1.4 Dissertation Outline

This dissertation is organized in the following manner: Chapter 2 introduces the concept of Sequentially-Switched Delay Lines by providing signal propagation and timing diagram analyses. Chapter 3 demonstrates a SSDL proof-of-concept using parts that are commercially available. Following this is Chapter 4, which provides design considerations, detailed analyses of the circulator's performance limits, and spectrum appearing at the output ports. Chapter 5 provides simulated and experimental results over two phases of SSDL circulator development on a GaN MMIC platform, accompanied by explanations of the transistor switch model development.

Chapter 5 also discusses the types of gate matching that were explored for use over the two phases, and the advantages of each. Chapter 6 introduces an improved gate matching strategy that significantly increases the power compression point of the SSDL circulator with measured results. In addition, Chapter 6 develops the gate matching circuits that are used to further improve the measured power compression. Chapter 7 presents the noise floor and phase noise measurements of the SSDL circulator. A brief conclusion is given at the end of this dissertation.

# CHAPTER 2

## SSDL Operating Principles

### 2.1 The Concept of SSDL

The original SSDL circuit architecture presented in [51], as shown in Figure 2.1 is composed of a set of five single-pole double-throw (SPDT) switches and six transmission lines of equal length. There are three ports in the SSDL circulator, i.e. ports 1, 2, and 3 that are defined as the transmitting (TX), antenna (ANT), and receiving (RX) ports, respectively.

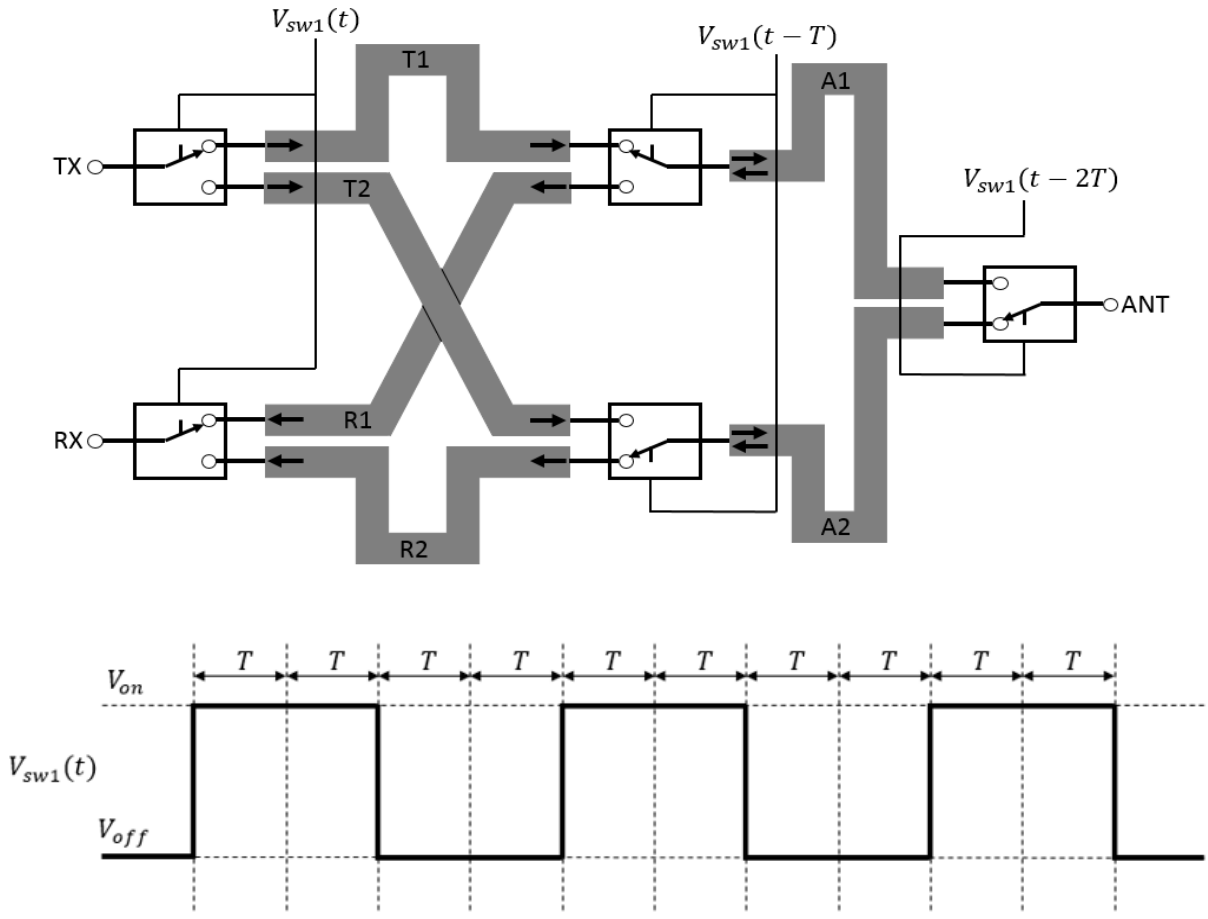



Figure 2.1: Original six-line architecture of the Sequentially-Switched Delay Line (SSDL) Circulator.

Note that these three ports are not symmetrical. However, the port denomination indicates the preferred way of utilizing this device to provide the desired transmitter to receiver isolation in a single antenna wireless system. It should be noted that the bottom of Figure 2.1 displays the voltage control signal applied to the switches. This switching signal has a 50% duty cycle and is the same signal applied to all of the SSDL designs reported in this work. The operating principle is described as follows: The transmitted wave is split into two pulses through the TX demultiplexing switch. Each pulse has a duration of 2*T*. They follow a path of either TX->T1->A1->ANT or TX->T2->A2->ANT. The switches are turned on sequentially right before the wave arrives and turned off right after the wave departs. Finally, the two pulses are combined at the ANT port through the ANT multiplexing switch. For the received wave, the ANT port now acts as a demultiplexing switch. It divides the received wave into two 2T pulses in a similar fashion but at a time delay of 2T compared to that of the TX device. The received wave follows a path of either ANT->A2->R2->RX or ANT->A1->R1->RX, where the sequential switching pattern described previously allows for the propagation of the received waves. The T/R switch or the R/T switch is always turned to the opposing path the moment the wave in the previous path departs, so there is neither reflection nor alteration to the waveform.

It is possible to simplify the structure in Figure 2.1 by reducing the length of transmission lines T1, T2, R1, and R2 to zero, and then merging the TX and RX switches with the two SPDT switches (shown in the middle of Figure 2.1) to form a double-pole, double-throw (DPDT) switch. The ANT port is left as the same SPDT switch to form the three ports of the circulator as shown in Figure 2.2.

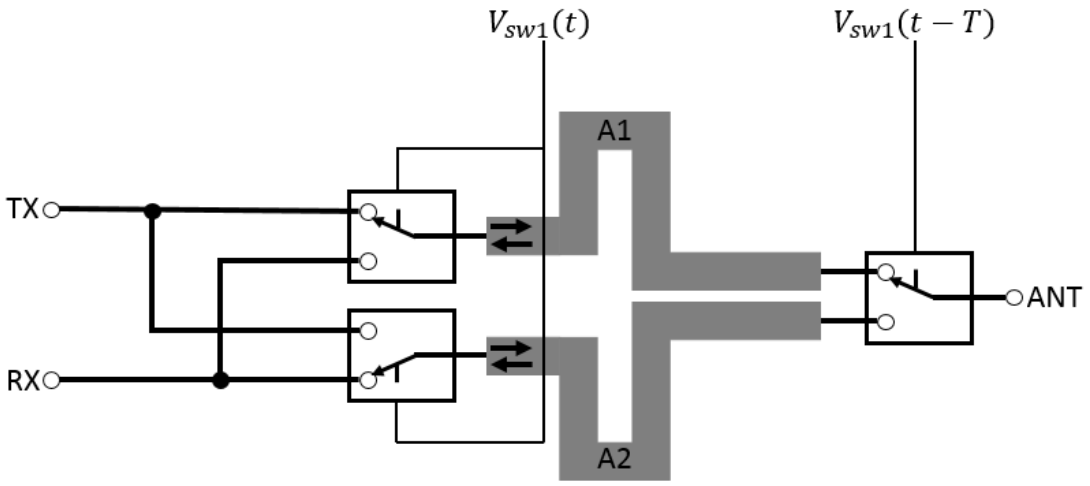



Figure 2.2: Simplified two-line architecture of the Sequentially-Switched Delay Line (SSDL) Circulator.

This simplification leads to a two-line SSDL circulator, which is the subject of many of the works cited in Chapter 1. It allows the exact same nonreciprocal behavior with lower insertion loss as well as a smaller surface area for on-chip integration. This design can be extended further by replacing the SPDT switch at the ANT port with a DPDT switch as shown in Figure 2.3, which forms a four-port circulator. Note that the delay is identical between the circulator's ports, due to the symmetry of the configuration.

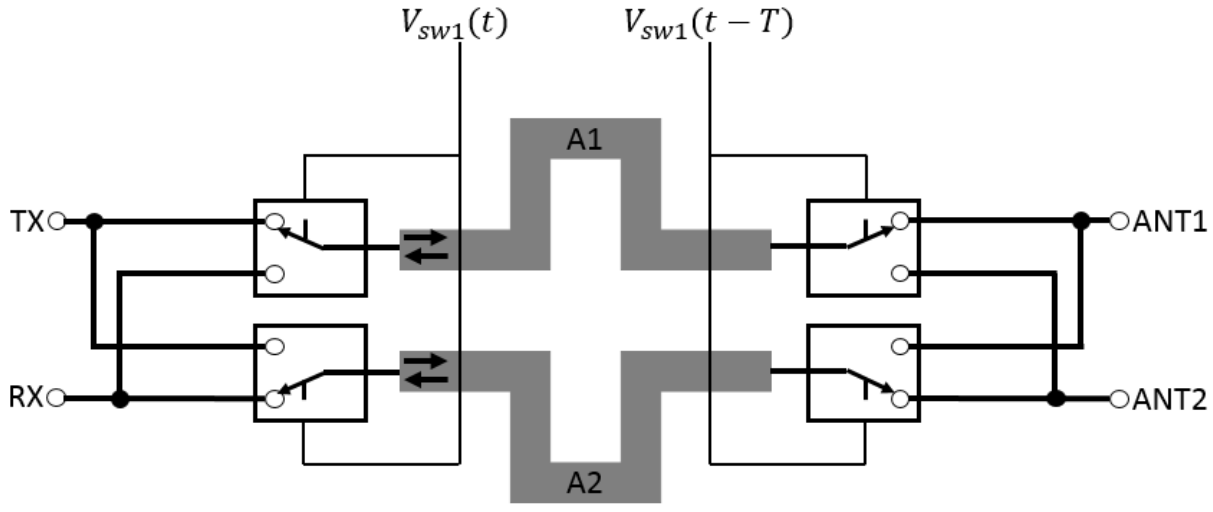


Figure 2.3: Simplified four-port two-line architecture of the Sequentially-Switched Delay Line (SSDL) Circulator.

### 2.1.1 Two-line circulator signal propagation analysis

To show the soundness of the SSDL circulator, the following mathematical derivations are performed: The analysis begins by looking at the transmitted signal leaving the TX port, as indicated in Figure 2.2. The original transmitted signal is denoted as $TX(t)$ and it is split into two pulses that travel respectively along an upper or a lower branch. The upper branch is denoted as "U", where the first TX pulse travels a transmission line sequence from A1 to ANT. The lower branch is denoted as "L" where the second TX pulse travels along the path from A2 to ANT. Both pulses finally arrive at the ANT port and combine to form the original transmitted signal. Assuming $V_{sw1}(t)$ is the normalized control voltage connected to the transmitter switch, e.g., the top left portion of the DPDT switch in Figure 2.2, the following summation represents its switching behavior:

$$V_{sw1}(t) = \sum_{n=-\infty}^{\infty} u(t - 2nT)(-1)^n \quad (1)$$

The ANT switch is controlled by the same sequence but at a delay of T compared to the DPDT switch, and has the following form:

$$V_{sw2}(t) = V_{sw1}(t - T) \quad (2)$$

One would then write the two split transmit pulses after the first DPDT switch as the product of the transmit signal and the normalized switch control voltage in the following form:

$$TX_1^{(U)}(t) = TX^+(t) \cdot V_{sw1}(t)$$

$$TX_1^{(L)}(t) = TX^+(t) \cdot \overline{V_{sw1}(t)} \quad (3)$$

Here, $\overline{V_{sw1}(t)} = 1 - V_{sw1}(t)$, while $TX_1^{(U)}(t)$ and $TX_1^{(L)}(t)$ represent the signals just to the right of the DPDT switch that populate transmission lines A1 and A2, respectively. Both signals are delayed by a time T before they arrive at the second switch, e.g. the ANT switch where the pulses are recombined. They now have the following form:

$$TX_2^{(U)}(t) = TX_1^{(U)}(t - T) \cdot V_{sw2}(t)$$

$$TX_2^{(L)}(t) = TX_1^{(L)}(t - T) \cdot \overline{V_{sw2}(t)} \quad (4)$$

This means that the two pulses are recombined at the ANT port with the following expression:

$$ANT^-(t) = TX_2^{(U)}(t) + TX_2^{(L)}(t)$$

$$ANT^-(t) = TX_1^{(U)}(t - T) \cdot V_{sw2}(t) + TX_1^{(L)}(t - T) \cdot \overline{V_{sw2}(t)}$$

$$ANT^-(t) = TX^+(t - T) \cdot V_{sw1}(t - T) \cdot V_{sw2}(t) + TX^+(t - T) \cdot \overline{V_{sw1}(t - T)} \cdot \overline{V_{sw2}(t)}$$

Note that using the simplification of (2) in the above expression leads to the following result:

$$ANT^-(t) = TX^+(t - T) \cdot V_{sw1}(t - T) + TX^+(t - T) \cdot \overline{V_{sw1}(t - T)}$$

$$ANT^-(t) = TX^+(t - T) \quad (5)$$

It is evident from (5) that the transmit signal will arrive at the antenna port with merely a delay of T. It is neither diverted nor altered. For receiving, the signal first arrives at the antenna port. The ANT port switch splits the received signal into two pulses that propagate on either the upper or lower branches, and follows a similar analysis to that presented for the transmit path.

When the waves are launched into the RX port, a simple mathematical derivation of the complete wave behavior is no longer possible, due to the existence of reflections as the wave encounters a switch connected to the opposing path. However, it is not difficult to derive the following relation with the help of some timing diagrams. Completing this study leads to the following time relationships between the SSDL circulator's three ports:

$$RX^{-}(t) = ANT^{+}(t - T) \quad (6)$$

$$TX^{-}(t) = RX^{+}(t - 2T) \quad (7).$$

The equations (5), (6) and (7) thus conclude that the operation of SSDL follows that of a three-port circulator except with an asymmetric delay response. For waves traveling from port 3 (RX) to port 1 (TX), a longer delay is expected, which implies a greater loss in practical scenarios. However, in most situations a symmetrical delay is most important for the transmit and receive paths, as these are the paths used in full duplex operations. The isolation between the transmit and receive ports is the other critical part of full duplex communications.

Carrying out a similar analysis for the two-line four port circulator shown in Figure 2.3 leads to the following transfer relationships among the circulator ports:

$$ANT1^{-}(t) = TX^{+}(t - T) \quad (8)$$

$$RX^{-}(t) = ANT1^{+}(t - T) \quad (9)$$

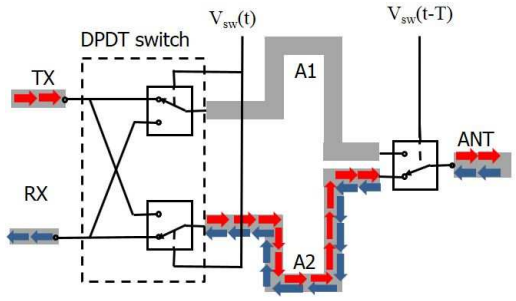
$$ANT2^{-}(t) = RX^{+}(t - T) \quad (10)$$

$$TX^{-}(t) = ANT2^{+}(t - T) \quad (11)$$

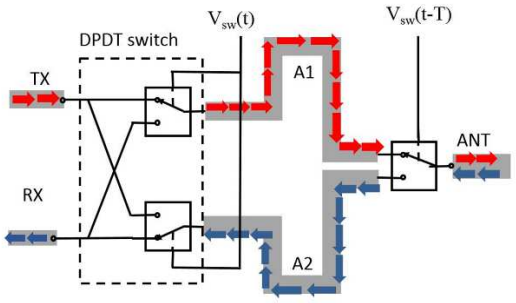
### 2.1.2 Timing diagram analysis of the two-line three port SSDL circulator

The switching operation of the two-port SSDL circulator will now be explained with the use of different snapshots in time. The timing diagram in Figure 2.4 illustrates the process of wave propagation at the four switching moments of each cycle. Note that the transmitted and received waves are represented respectively by the colors red and blue. The TX, ANT, and RX ports are connected to the correct transmission line for a time of 2T. Each timing instance will be explained with respect to the switching action of the double-pole double-throw (DPDT) switch. Figure 2.4a represents the locations of the transmitted and received waves at time 0+. The (+) sign indicates that the devices have just completed their switching action. The DPDT switch has just connected the TX and RX ports to transmission lines A1 and A2, respectively. The ANT port switch has been on for a time T+. This allows for the first received pulse to begin populating A2 simultaneously with the tail end of the second transmitted pulse, which arrives at the ANT port. The transmitted and received waves that occupy A2 at the same time do not interfere with each other because they travel toward different directions. Next, we progress in time to Figure 2.4b, which is a time snapshot at T+. In this case, the DPDT switch stays in its same position while the ANT port switch connects to A1. Here, the first transmitted pulse can be seen starting along A1 which will be sent out through the ANT switch. At the same time, the first received pulse is seen completing its journey to the RX port. It is important to note that right before the ANT port switch flipped, the tail end of the second transmitted pulse was captured at the ANT port. As time moves forward to Figure 2.4c, the switch positions are now seen at time 2T+. The DPDT switch has flipped its orientation after being in its previous state for a time 2T. Now, the TX and RX ports are respectively connected to transmission lines A2 and A1. The first transmitted pulse now completes its journey along A1 and out through the ANT port. Also, the second received pulse begins to traverse A1. As

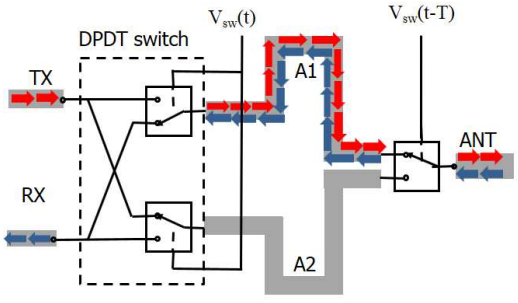
time advances further, the positions of the transmitted and received waves in the circulator are seen at time 3T+ in Figure 2.4d. Here, the ANT port switch connects to transmission line A2 after being in its previous state for a time of 2T. Here, the second transmitted pulse starts to propagate along A2 while the second received pulse completes its journey along transmission line A1. As time is progressed further, the switches and positions of the TX and RX signal pulses match those of Figure 2.4a.



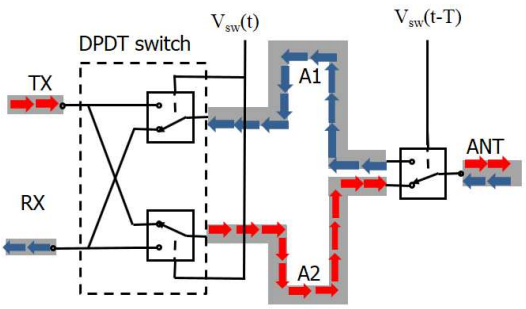

(a)




(b)




(c)

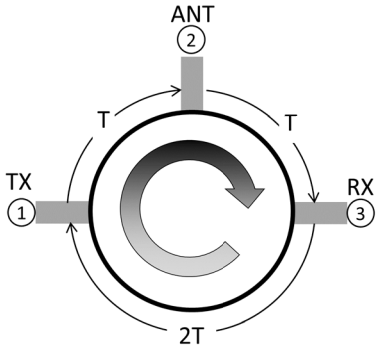



(d)

Figure 2.4: Positions of the switches along with the transmitted and received waveforms (a) at time 0+ (b) at time T+ (c) at time 2T+ (d) at time 3T+.

### 2.1.3 Circulator equivalence for the two-line SSDL circulators

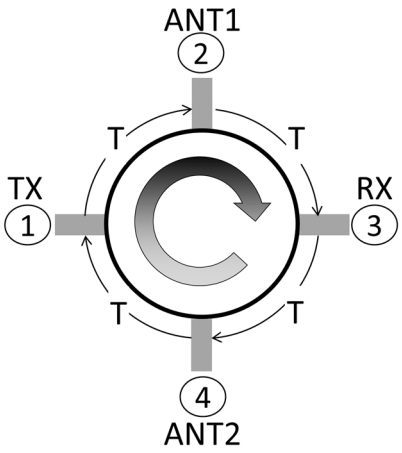
It was concluded in section 2.1.1 that the two-line three port circulator behaves as a circulator with an asymmetric time delay response. This is summarized below using the circulator equivalency symbol and associated S-parameter matrix.




$$\begin{bmatrix} 0 & 0 & S_{13}e^{-j\omega 2T} \\ S_{21}e^{-j\omega T} & 0 & 0 \\ 0 & S_{32}e^{-j\omega T} & 0 \end{bmatrix}$$

Figure 2.5: Circulator equivalence symbol (left) and associated S-parameter matrix (right) for the two-line three port SSDL circulator.

It was also demonstrated that the two-line four port circulator forms symmetrical delay among the circulator's ports. Signals enter the circulator and travel through the circulator in a clockwise fashion, as shown by the symbol in Figure 2.6, with a time delay which corresponds to the delay of a single transmission line. Also shown with the circulator equivalence symbol is the associated four port scattering matrix.




$$\begin{bmatrix} 0 & 0 & 0 & S_{14}e^{-j\omega T} \\ S_{21}e^{-j\omega T} & 0 & 0 & 0 \\ 0 & S_{32}e^{-j\omega T} & 0 & 0 \\ 0 & 0 & S_{43}e^{-j\omega T} & 0 \end{bmatrix}$$

Figure 2.6: Circulator equivalence symbol (left) and associated S-parameter matrix (right) for the two-line four port SSDL circulator.

There are a few things to note about the four port circulator scattering matrix. First, that terminating port 4 with an open circuit load will reduce the four port matrix to the scattering parameters of an ideal 3-port circulator. In practice, one can simply terminate port 4 with a matched load for full-duplex operation, as will be explained in later chapters.

# CHAPTER 3

# SSDL Demonstration

## 3.1 SSDL Circulator COTS Demo

As a proof of concept for the theory described above, parts that are commercially available were purchased and used to demonstrate the feasibility of the six-line SSDL circulator approach.

### 3.1.1 Experimental Methods

An experimental setup with coaxial cables and Commercially Off the Shelf (COTS) switches is used to test the operation of the SSDL device as shown in Figure 2.7. The setup consists of six coaxial cables of equal length with a time delay of T of 43 ns. Each individual cable is 30 feet long. The delay time T was measured for each of the six transmission lines using a vector network analyzer. The switching action should thus happen at a rate of approximately 24 Msps with each switch turned on or off at the rate of 12 Msps to synchronize with the delay of the cable. Figure 2.7 also shows five single-pole double-throw (SPDT) switches that are imperative to the simultaneous transmit and receive operation of the device. These switches are available from Mini-circuits (part number ZFSW-2-46). A 10% to 90% transition time of approximately 3 ns and an insertion loss of 1 dB are claimed by the manufacturer. The switches are connected in the SSDL test bed as shown in Figure 2.7 among the three radio frequency (RF) ports. The control signals are a series of square waves at 6 MHz with programmed delays, which are generated by the digital outputs of a Sony Tektronix Arbitrary Waveform Generator (part number AWG520).

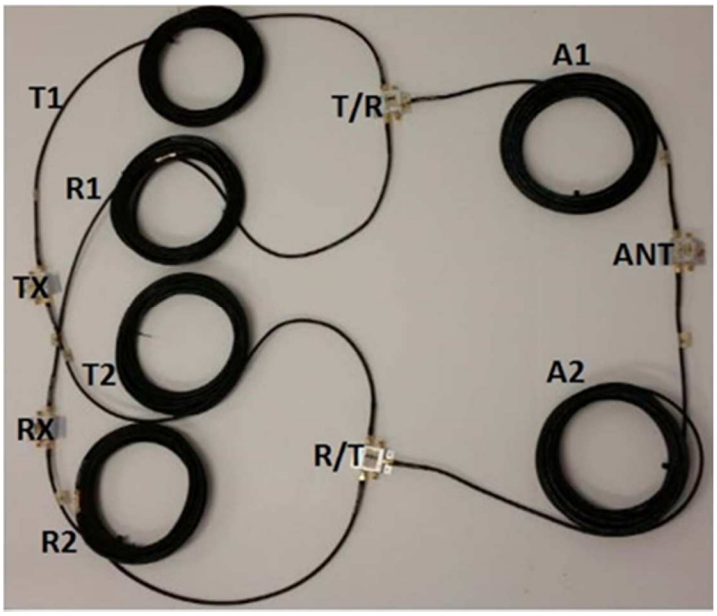


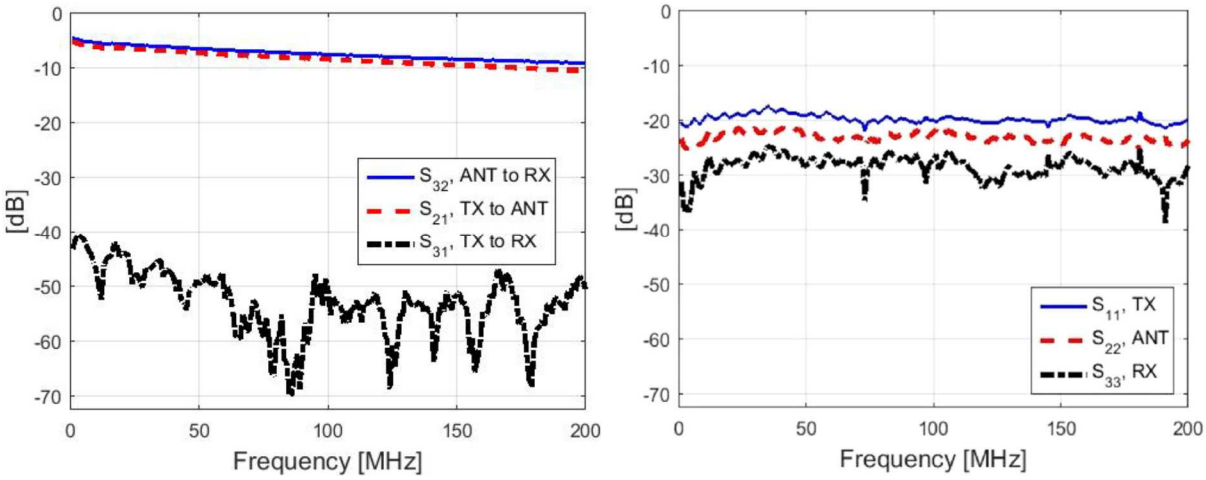

Figure 3.1: SSDL circulator setup showing the cables and COTS switches.

### 3.1.2 Experimental Results

S-parameter results are collected from this circulator. The insertion losses, isolation, and port matching parameters were measured using a network analyzer. With the TX, ANT, and RX ports defined as ports 1, 2, and 3, respectively, Figure 2.8 represents the S-parameter results captured. In this case, the start and stop frequencies of the vector network analyzer are set to 200 KHz and 200 MHz, respectively. Figure 2.8a represents the insertion losses and isolation measured for the circulator. The insertion loss is measured in two ways, e.g. one with S21 being measured from the TX port to the ANT port and the RX port matched with 50 Ohm load, and the second with S32 being measured from the ANT port to the RX port with the TX port matched with 50 Ohm. In both scenarios, the insertion losses range from 5 dB to 10 dB from 200 KHz to 200 MHz, respectively. It should be noted that the insertion loss of each switch in its stationary mode is approximately 1 dB. At 200 MHz, the loss of each assembled RF cable is approximately 1.5 dB. As the signal propagates from the ANT to RX or TX to ANT path, it passes through two cables

and 3 switches. Therefore, up to 6 dB insertion loss can then be attributed to the stationary loss of the setup and the rest of the insertion loss can be considered as the dynamic switching loss. It should also be noted that the control voltage outputs from the AWG were below the voltage required that fully turns the switches on and off. The dynamic switching loss can be attributed to this factor as well as the finite transition time of the switches.

To measure the isolation, the forward and reverse ports of the vector network analyzer are attached to the TX and RX ports, respectively. The ANT port is terminated with a matched 50 ohm load, and the isolation loss is measured as S31. The isolation measured between the TX and RX ports is exceptional with approximately 40 dB at the worst case, which occurs around at the frequency of 200 KHz. Figure 2.8b relates the port matching for all three circulator ports. The measured data shows that all three ports are well matched to the system characteristic impedance of 50 ohms. These results validate that the SSDL circulator demonstrates non-reciprocal behavior from 200 KHz to 200 MHz. In fact, similar non-reciprocal behavior is also observed at 20 KHz, which is the lowest frequency of the vector network analyzer. This shows that indeed there is no lower frequency limit of the circulator's operation.




(a) (b)

Figure 3.2: Measured insertion loss and isolation (a) and return loss (b) for the SSDL circulator using COTS components.

# CHAPTER 4

## Performance Limits and Design Considerations

### 4.1 Switching Noise Performance of SSDL

The SSDL device operates by splitting the signal waveform in time into two sets of pulses at the input, which are combined later at the output to form the original signal. The process is distortion free if ideal switches with zero transition time are used. In practice, the finite transition time of the switches may cause gaps or spurs in the wave- form when the signal energy is lost or discharged during the transition time. The switching noise often behaves as frequency spikes contaminating the signal spectrum. It is thus important to understand the characteristics of such noise. A simplified model of the switching noise is shown in Figure 2.7, where periodic gaps are introduced into the signal waveform during the switching actions.

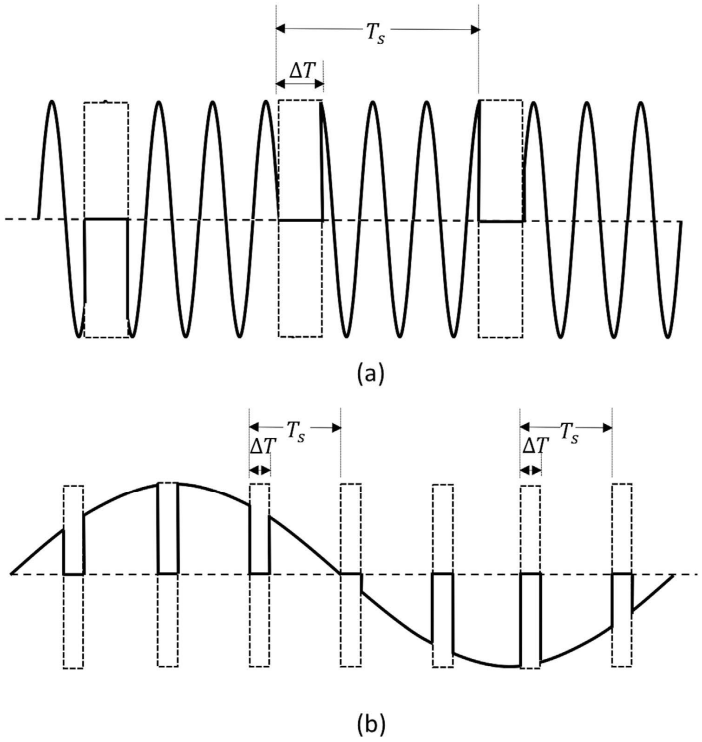



Figure 4.1: Switching noise represented by periodic rectangular gaps in the signal waveform.

The noise is represented by the rectangular gaps appearing at every period of $T_s$, with $T_s = 2T$ and the width of the gaps is assumed to be $\Delta T$. Figure 2.7a shows a case when the angular switching rate $\omega_s = 2\pi/T_s$ is much lower than the signal angular frequency $\omega_0$ while Figure 2.7b displays a case when the switching rate is much greater than the signal frequency. In either case, the switching noise, which is the removed portion in Figure 2.7, is expressed by:

$$f_N(t) = f(t) \cdot \sum_{n=-\infty}^{\infty} rect\left(\frac{t - nT_S}{\Delta T}\right) \quad (12)$$

where $f(t)$ is the original signal. The spectrum of the switching noise is thus obtained as:

$$F_N(\omega) = F(\omega) \otimes \frac{\Delta T}{T_S} sinc\left(\frac{\omega \Delta T}{2}\right) \sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_S) \quad (13)$$

which behaves as the repetition of the original signal spectrum in a period of $\omega_s$, following a pattern of SINC function. Assuming a single-tone signal at the angular frequency of $\omega_0$ with a unit amplitude, the spectrum becomes:

$$F_N(\omega) = \frac{\Delta T}{T_S} sinc\left(\frac{(\omega - \omega_0)\Delta T}{2}\right) \sum_{n=-\infty}^{\infty} \delta(\omega - \omega_0 - n\omega_S) \quad (14)$$

which is represented by the multiple spectral lines plotted in Figure 2.8. In general, the noise spectrum scales down in magnitude when the fraction of the transition time versus the switch period reduces. It is observed that the strongest spectral line at $\omega_0$ that has a magnitude of $\left({}^{\Delta T}/_{T_s}\right)$ is the lost portion of the original signal that should be counted as the insertion loss rather than noise. Therefore, the strongest noise components are indicated by the two spectral lines at $\omega_0 - \omega_s$ and $\omega_0 + \omega_s$, which has a magnitude of:

$$F_N(\omega_0 \pm \omega_S) = \frac{\Delta T}{T_S} sinc\left(\pi \frac{\Delta T}{T_S}\right) \quad (15).$$

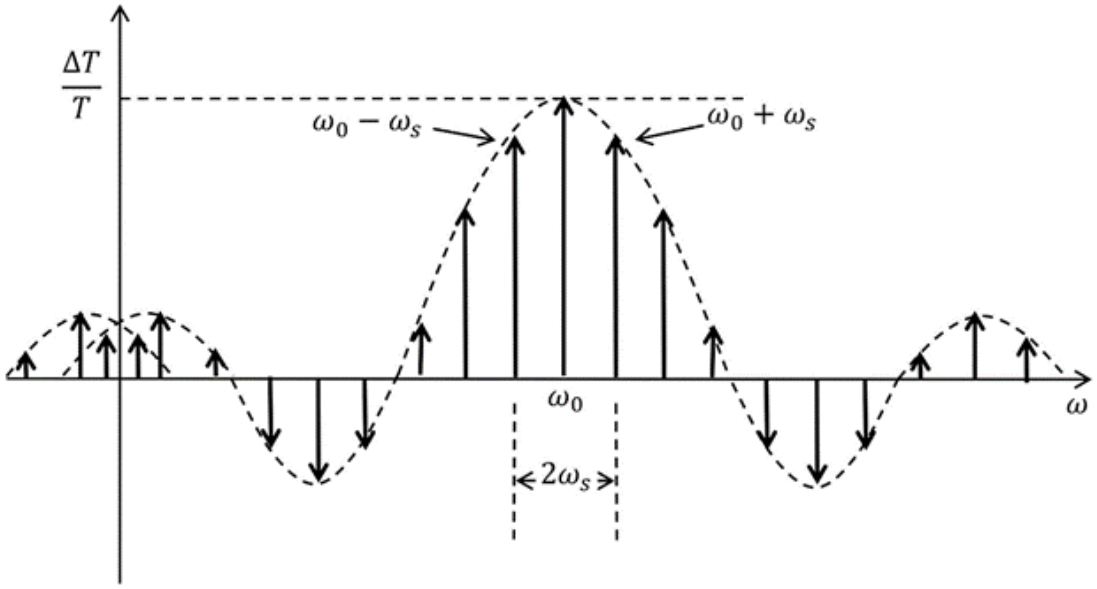



Figure 4.2: Spectrum of the switching noise when the input is a single-tone sinusoid at $\omega_0$.

The further noise components in general decay following a SINC function or other spread functions for non-rectangular gap representation of switching noise. In the case $\omega_s \ll \omega_0$, the noise spreading from the negative side of the spectrum may be ignored. It is evident from Figure 2.8 that the region between these two spectral lines, i.e. $[\omega_0 - \omega_s, \omega_0 + \omega_s]$ defines an operating bandwidth (without switch mixing products) of $2\omega_s$. A bandpass filter with a passband centered at $\omega_0$ may then be utilized to suppress the switching noise at the price of reduced bandwidth of circulator operation. On the other hand, if $\omega_s \gg \omega_0$ one can easily prove that all the noise spectral lines, including those spreading from the negative side, will appear at angular frequencies higher than $\omega_0$. This corresponds to the standard case of sampling above the Nyquist rate, in which case a low pass filter can help to remove all the switching products.

## 4.2 SSDL MMIC design considerations

The SSDL circulator MMIC designs presented in this paper are carried out on the 0.2um GaN HEMT process from Northrop Grumman Aerospace Systems (NGAS). They are based on switching frequencies of 1.25GHz and 2.5GHz. The time delay match between the signal

propagation and switch timing is what allows for the theoretically infinite bandwidth operation of the SSDL circulator. For this condition to be satisfied, each transmission line must have a delay time equivalent to T, which is an electrical length of 90 degrees at the switching frequency. Using the LineCalc program in Agilent ADS, the required straight-line microstrip lengths for switching frequencies of 1.25GHz and 2.5GHz are 23.8mm and 11.9mm, respectively. For a compact on-chip implementation, one must meander the microstrip lines to reduce the overall chip dimensions.

An RF switch is characterized by its on-resistance and off-capacitance which set the time constant of the switch itself. Since the SSDL circulator is designed to switch at high frequencies, the time constant must be low to avoid significant losses during circulator operation. Figure 2.9a and Figure 2.9b show the schematics of two topologies used to construct the RF single-pole double-throw (SPDT) switch. In the first topology shown in Figure 2.9a, the switch is symmetrical about the RFOUT port, with each throw arm consisting of two series transistors and one shunt transistor. The series transistor devices have seven gate fingers with a total periphery of 805um. The shunt transistor device has 3 gate fingers with a total periphery of 120um. The control signals are such that $\overline{V_{sw}(t)}$ is the differential signal of $V_{sw}(t)$, which respectively control the connection of RF2 and RF1 with RFOUT. Two of these SPDT RF switches are combined in parallel with each other to form a double-pole double-throw (DPDT) RF switch. This configuration has the following features. The first is that the shunt device grounds any leakage current through the RF path when it is in the OFF state. The second is the protection against a short circuit condition for the RF signal when the opposing path is in the OFF state.

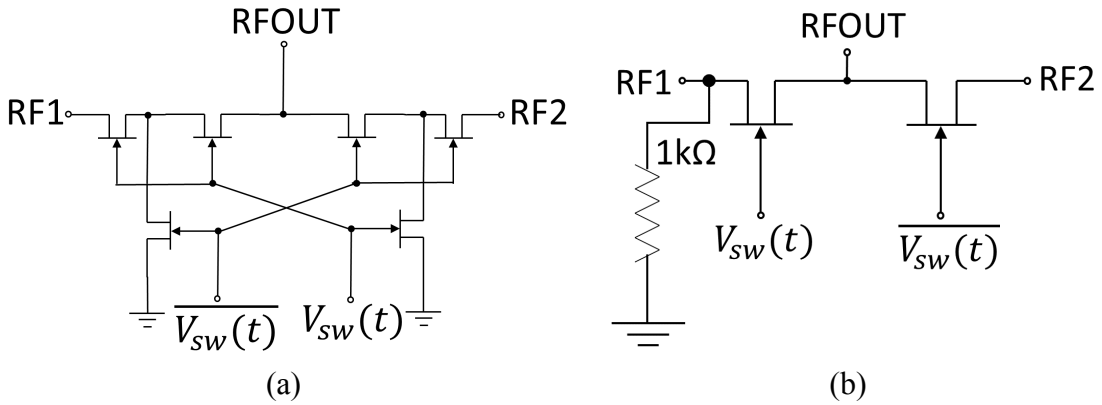



Figure 4.3: RF SPDT switch used in the two-line SSDL Circulator (a) topology one with a series-shunt-series configuration (b) topology two with a single series configuration.

Without the additional series transistor device at the terminal of each throw arm, the SPDT switch would have the shunt device as its first element observed when looking from the output of the switch arm. If this was the case, the combination forming the DPDT switch would present a short circuit to ground for the RF signal in the parallel path. The advantage of this topology is the high isolation of the switch brought forth by the series and shunt combination, but this is at the price of complexity and higher insertion loss as the signal power through the drains and sources may leak to the gate control paths through multiple gate connections.

In an effort to reduce the complexity of the switch design, the second SPDT switch topology is shown in Figure 2.9b. The simplified switch design accomplishes the same goals as the switch shown in Figure 2.9a with only one series transistor in each throw arm, which reduces the total on-resistance and thus the insertion loss of the switch. Each series transistor has seven gate fingers with a total periphery of 805um. Again, two of the SPDT switches of Figure 2.9b are placed in parallel to form the DPDT switch for use in the SSDL circulator. Figure 2.10 shows the schematic of the full two-line SSDL circulator. Each rectangle represents a SPDT switch displayed in Figure 2.9a or 2.9b, with two connected in parallel to form the DPDT switch for the TX and RX

ports (left of Figure 2.10) and the ANT port (right of Figure 2.10). The port shown at the bottom right of Figure 2.10 is terminated into a matched load so that a three-port SSDL circulator is formed. When two of the SPDT switches of Figure 2.9b are connected in parallel as shown in Figure 2.10, notice that the 1kohm resistor provides a reference path to ground for both the RF1 and RF2 ports of the upper and lower SPDT switches, respectively.

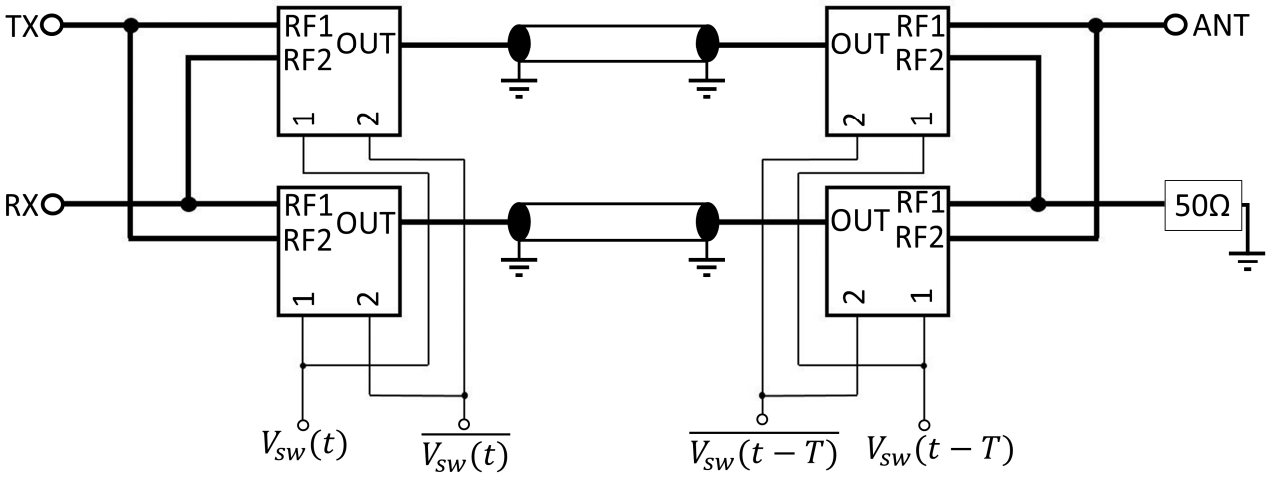



Figure 4.4: General block diagram of the two-line SSDL Circulator.

## 4.3 Insertion Loss Performance of SSDL

Comparing to RF circulators made of magnetic materials, the insertion loss of current non-magnetic circulators is generally higher. Therefore, it is important to understand the theoretical limit of SSDL circulator insertion loss for a given technology. The analysis carried out here is assuming no leakage of the signal to the control path and the insertion loss is only contributed by the on-resistance and the off-capacitance of the switch. The transistor that is used to construct a switch has a technology dependent figure of merit defined as,

$$f_{FOM} = \frac{1}{2\pi R_{on} C_{off}} \qquad (16)$$

where $R_{on}$ is the on-resistance and the off-capacitance $C_{off}$ of the transistor. The input power into the SSDL circulator can be written as,

$$P_{input} = \frac{1}{2} I^2 Z_0 \qquad (17)$$

where $I$ is the current flowing on the transmission line and $Z_0$ is the characteristic impedance of the transmission line. For the single series switch topology shown in Figure 2.9b, every time when the switch is turned on from off, the energy stored in the off-capacitance of the transistor is lost. During one switching cycle of 4T, the transitions from off to on states in each DPDT switch happens once for all four transistors, which leads the capacitive power loss given by:

$$P_{loss}^{C} = \frac{1}{2} f_s C_{off} V^2 \cdot 4 = \frac{1}{2} I^2 \cdot 4 f_s C_{off} Z_0^2 \qquad (18)$$

where $f_s$ is the switching frequency and the Ohmic loss at the switch is yielded as:

$$P_{loss}^{R} = \frac{1}{2} I^2 R_{on} \qquad (19)$$

This is because the wave encounters the on-resistance of one transistor at any given time. The power lost in each DPDT switch is thus given by summing the capacitive power loss in (18) with the Ohmic power loss in (19), yielding:

$$P_{loss} = \frac{1}{2} I^2 \left(4 f_s C_{off} Z_0^2 + R_{on}\right) \qquad (20)$$

The fractional power loss is then derived as:

$$\frac{P_{loss}}{P_{input}} = 4f_s C_{off} Z_0 + \frac{R_{on}}{Z_0} \qquad (21)$$

It is noted that the two loss terms in (21) have a fixed product, therefore the minimum insertion loss is achieved when these two terms are equal to each other, which requires:

$$\left(\frac{R_{on}}{Z_0}\right)^2 = 4f_s C_{off} R_{on} = \frac{2f_s}{\pi f_{FOM}} \qquad (22)$$

Therefore, the optimum condition for switch design is to choose the periphery of the transistor so that the following condition holds true:

$$R_{on} = Z_0 \sqrt{\frac{2f_s}{\pi f_{FOM}}} \qquad (23)$$

With this optimum matching condition and taking account of the fact two DPDT switches are needed in the SSDL, the fundamental limit of SSDL circulator insertion loss is defined as:

$$IL = 1 - 2\frac{P_{loss}}{P_{input}} = 1 - 4\frac{R_{on}}{Z_0} = 1 - 4\sqrt{\frac{2f_s}{\pi f_{FOM}}} \qquad (24)$$

For example, in the current NGAS 0.2um GaN MMIC process, a typical transistor has an on-resistance of 4 Ohms and an off-capacitance of 0.31pF, which gives a switch figure of merit of 128GHz. At the switching frequency of 1.25GHz and a 50Ohm reference impedance system, the optimum on-resistance of the switch should be the following:

$$R_{on} = Z_0 \sqrt{\frac{2f_s}{\pi f_{FOM}}} = 4\ Ohm \qquad (25)$$

Under this optimum match, the insertion loss given by (24) is 1.65dB. This loss is in addition to the loss of the meandered microstrip line which is approximately 0.3 to 0.5dB. It is also evident

from (25) that the insertion loss can be further reduced when technology with a higher switch figure of merit is used. However, in practice, the leakage of the RF signal to the gate control path may be the primary reason that prevents the theoretical limit shown in (24) from being reached. Techniques to isolate the gate signal from the RF signal flowing across the drain and source terminals will be discussed in later sections.

# CHAPTER 5

# Practical SSDL Designs

## 5.1 Experimental Methods for SSDL MMICs

The beauty of this concept is that it can be adapted to any process or material where switches and transmission delay lines exist. To show the potential for the SSDL concept to provide broadband full duplex operation, two generations of GaN MMICs that have been developed will be summarized. All of the presented designs are fabricated on the NGAS 0.2um GaN HEMT process, and are designed based on the over-multiplexing scheme explained in chapter 4.

### 5.1.1 First generation SSDL MMIC

The first generation SSDL MMIC design is shown below in Figure 5.1. The switch design follows that in Figure 2.9a, and is designed for a switching frequency of 1.25GHz.

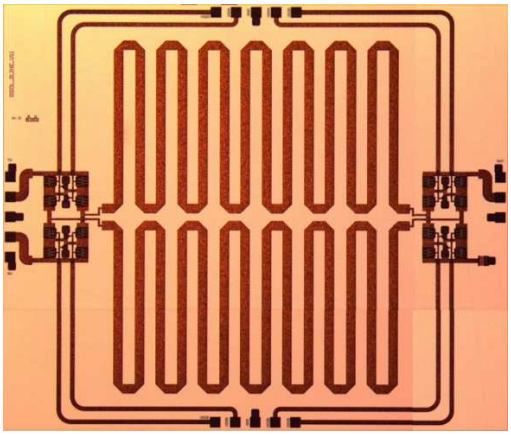


Figure 5.1: SSDL MMIC circulator switching at 1.25GHz with series-shunt-series switch topology.

This MMIC chip has probing pads which are either ground (represented by G) or signal (represented by S) ports. The transmitter (TX) and receiver (RX) ports are at the left edge of the chip and are connected to a double-pole double-throw (DPDT) RF switch through a G-S-G-S-G probe pad. The antenna (ANT) port is located at the right side of the chip and is connected to a

DPDT RF switch through a G-S-G probe pad. The probes corresponding to these pad layouts are manufactured by Cascade Microtech. RF signals are applied through these probes from a network analyzer. The microstrip lines associated with each transistor gate have an impedance of 70 ohms, which corresponds to a process line width of 41um. The second switch pole at the right side of the chip is connected to ground through a 50ohm resistor. In theory, the ANT port is connected to a single-pole double-throw (SPDT) RF switch. In this design, a DPDT RF switch at the ANT port identical to the TX/RX side is used and the other switch pole is terminated in a 50ohm matched load for simplicity. The two DPDT switches are connected by two meandered microstrip lines which have a 50ohm line width of 90um. The chip has dimensions of 5.1mm by 4.3mm. The electrical length of each delay line was originally designed to be 90 degrees at 1.25GHz to match the condition specified by the switching actions. Since the DPDT switches contribute additional passive delay, the delay lines were shortened to 90 degrees at 1.44GHz to resynchronize the switching action with the propagation delay. The adjustment was made based on the simulation with a preliminary transistor model.

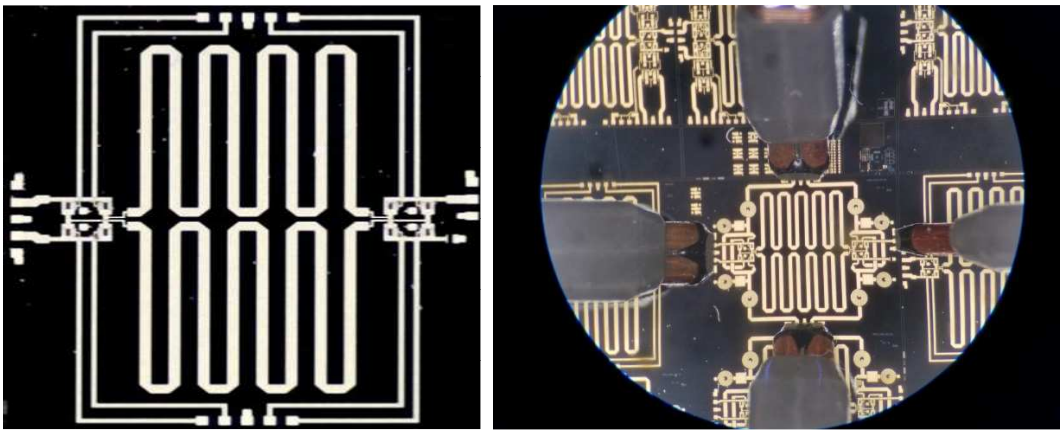
The top and bottom of this chip has S-S-G-S-S RF pads from left to right through which the switching signals are applied to the device gates. These probes are also manufactured by Cascade Microtech. There are eight drive signals that provide the correct on and off sequencing for full-duplex operation. These signals are 1.25GHz CW tones which are generated by a power amplifier and split using a hybrid coupler network. These sinusoidal signals at the coupler outputs are used to turn the switches on and off at 1.25GHz. The GaN devices are typically in the ON state when a potential of 0V is applied to the gate, and are OFF with a minimum potential of -3V. The proper DC offset is applied to each individual drive signal through a bias tee so that the full voltage swing of the gate control signal is presented to the gate of each switch.

The equipment setup used to test this chip is shown below in Figure 5.2, composed of a network analyzer and probe station for on-wafer testing.

Figure 5.2: Four port network analyzer, probe station with microscope, broadband bias tees, and hybrid coupler network used to test the SSDL circulator.

### 5.1.2 Second generation SSDL MMICs

The second generation SSDL MMIC designs are shown below in Figure 5.3. The switch designs for both circulators follow that in Figure 2.9b, and are designed for a switching frequency of 1.25GHz.



(a) (b)

Figure 5.3: SSDL MMIC circulators switching at 1.25GHz with single series switch topology and no gate matching circuitry (a) and gate matching circuitry (b).

Figure 5.3a is without any matching circuitry at the gate. This chip has dimensions of 4.2mm by 4.9mm. Its design is very similar to that of the first generation MMIC. The other adjustment made in addition to the simpler switch topology is the reduction of the delay line length. Each delay line has an electrical length of 90 degrees at 2GHz to account for the increased delay due to the transistor capacitance. The adjustment was greater based on a refined capacitance model of the transistor. It was found that the preliminary transistor model underestimated the gate-drain and gate-source capacitance of the switch, so values for these capacitors were derived from comparing modeled and measured results.

Figure 5.3b includes identical matching circuits placed at each of the four corners of the SSDL MMIC chip. It has dimensions of 5mm by 4mm. The impedance seen looking into the switch gate must also be considered in the design of the SSDL circulator. In order to improve the performance of the circulator, an L-section matching circuit consisting of two inductors is used to transform the capacitive switch gate into a 50ohm impedance. The “7F805” label associated with each transistor device means that each has 7 fingers with a total periphery of 805um. L1 has a value of 13.4nH at 1.25GHz and L2 has a value of 11.1nH at 1.25GHz. There is a DC voltage that is applied to the switch gates so that the switching signal properly turns each switch path on and off. The capacitor in series with the shunt inductance keeps the DC gate bias from being pulled directly to ground, which has a value of 27pF. The schematic associated with this design is shown below in Figure 5.4. Here, the L-match circuit is split so that one resonant circuit output feeds two switch gates. The impedance of the resonant circuit lines is 50ohm.

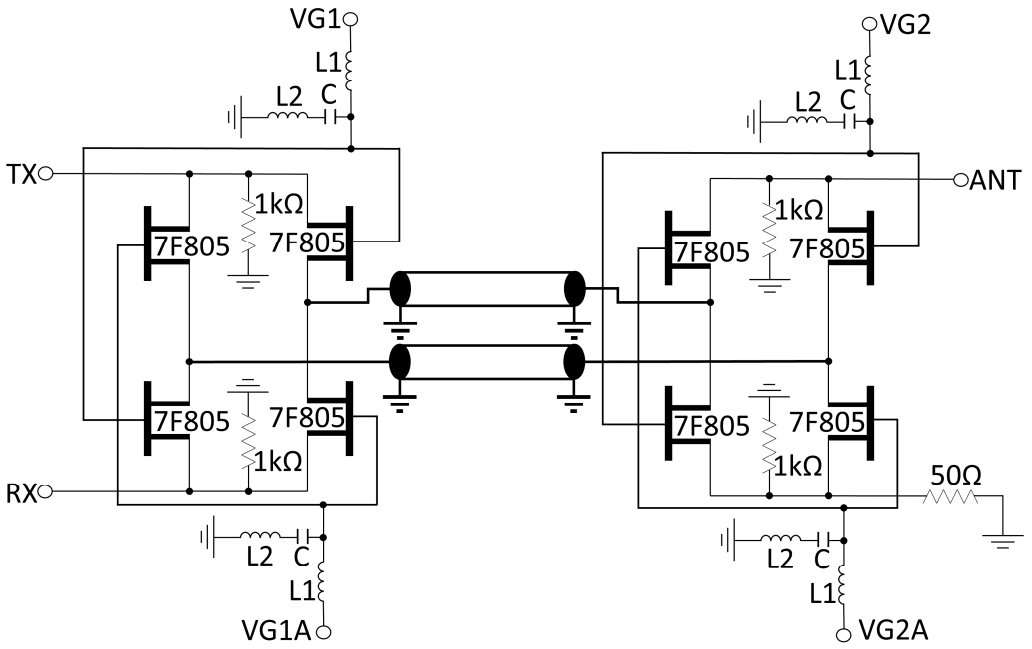


Figure 5.4: Circuit schematic overview of the second generation SSDL circulator with gate matching designed to switch at 1.25GHz.

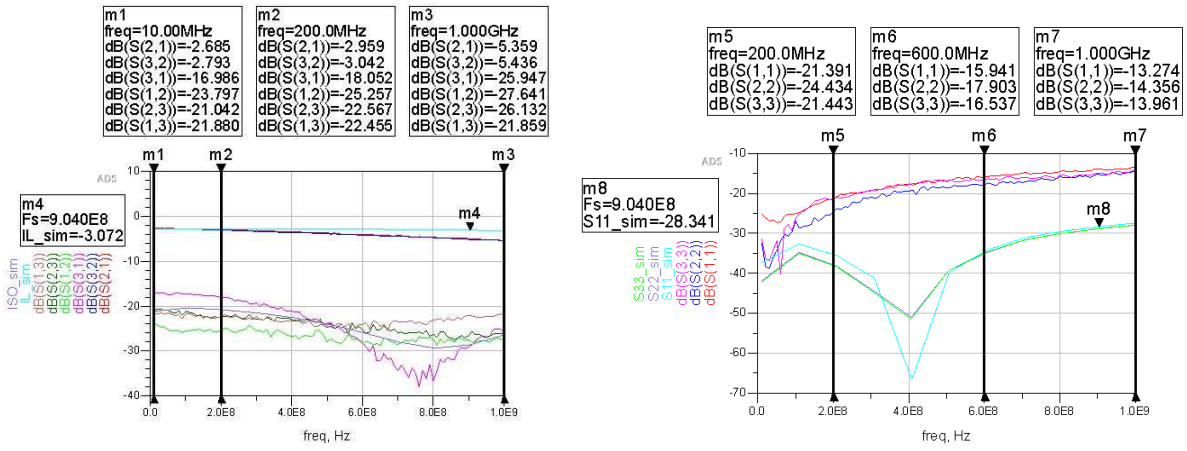
The equipment setup for the second generation MMICs is also on-wafer and very similar to the testing environment for the first generation SSDL MMICs.

## 5.2 Experimental Results for SSDL MMICs

### 5.2.1 First generation SSDL MMIC

A four-port PNA-X was used to characterize the performance of the First generation GaN SSDL circulator, which is shown below in Figure 5.5. The insertion loss from TX to ANT (S(2,1)) and ANT to RX (S(3,2)) measures from 2.7dB at 10MHz to 5.4dB at 1GHz. The isolation between TX and RX (S(3,1)) measures 17dB to 38dB over the same frequency range. It is also observed that the reverse path isolation from ANT to TX (S(1,2)) and RX to ANT (S(2,3)) is greater than 20dB over the entire measured frequency range, indicating that signal propagation is only in one direction as intended. The insertion loss from RX to TX (S(1,3)) measures approximately 22dB from 10MHz to 1GHz, which at first glance does not agree with the predicted theory for the two-

line circulator. However, the loss is high because the ANT port is the same DPDT switch used for the TX and RX ports. Due to this symmetrical design, the signals leaving the RX port end up in the 50ohm matched load of the ANT port switch. This follows the theory predicted for the four-port SSDL circulator. The simulation results using the preliminary transistor switch model are also plotted against these measured results. The switching actions during the circulator's operation dictate two modes of operation. The over-multiplexing mode (10MHz to 625MHz) is where the TX and RX signals can be recovered at their respective ports without the presence of mixing tones produced by the sequential switching actions. In this case, a lowpass filter can be used at the output ports to recover the RF signals. For most of this frequency range (10MHz to 500MHz), we can see that there is good agreement between the simulated and measured results.




(a) (b)

Figure 5.5: Simulated and experimental results for the first generation SSDL MMIC: insertion loss, isolation, and reverse path isolation (a), and return loss (b).

The remainder of the circulator's measured performance range (625MHz to 1GHz) falls into the under-multiplexing operation mode. As shown in Section 4.1, the mixing products created by the switching actions start to appear within the vicinity of the RF signal. In this case, a bandpass filter would need to be used to recover the RF signal at the output port. However, beyond 500MHz the

agreement between simulated and measured results degrades. It is observed that the preliminary transistor model predicts a flat 3dB insertion loss over the entire measured frequency range. The measured results do not follow this prediction, with an insertion loss delta of 2.2dB between the simulated and experimental results at 1GHz. A similar discrepancy can be observed when comparing the simulated and measured return loss. The return loss is degraded from the simulated performance by more than 10dB over the frequency range of interest. This is due to the preliminary model's underestimation of the gate-drain and gate-source capacitances ($C_{gd}$ and $C_{gs}$ respectively). As will be explained in the next section, adding in the appropriate terms for these capacitances gives a better agreement with the second generation MMIC performance.

### 5.2.2 Second generation SSDL MMICs

The same four-port PNA-X was used to measured the performance of both second generation SSDL GaN MMIC circulators. After comparing the modeled switch with first generation measurements, it was discovered that the preliminary switch transistor required an additional 2.5 times additional gate-drain and gate-source capacitance. These capacitances were added in parallel to the gate-drain and gate-source terminals of each device model in simulation as an improvement to the preliminary model. Figure 5.6 shows the measured insertion loss and isolation of the second generation SSDL circulator without the presence of gate matching circuitry. All of the results presented in this section are with the single series DPDT switch configuration (topology two of Figure 2.9). This circulator has a measured insertion loss from 3.7dB to 4.3dB from 10MHz to 1GHz, respectively. The isolation between TX and RX is greater than 20dB over the entire measured frequency range, which shows good isolation between the transmit and receive ports. The reduction of the delay line length in this configuration in conjunction with the use of

switch topology two helps to reduce the insertion loss at 1GHz by 1.1dB when compared to the first generation MMIC utilizing switch topology one.

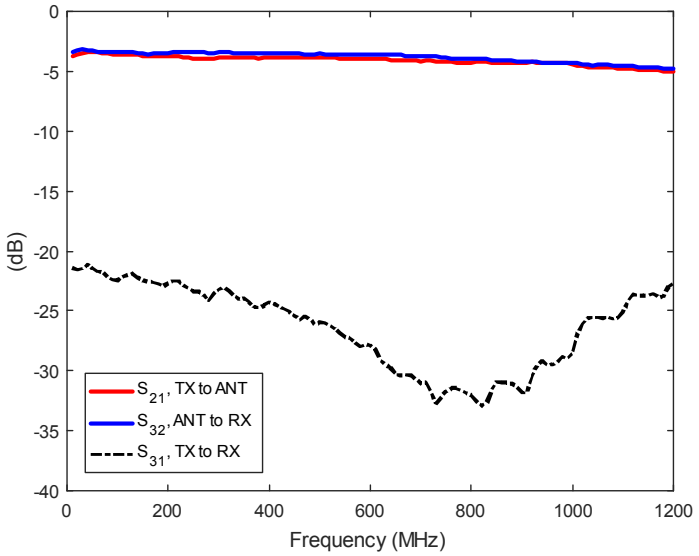



Figure 5.6: Experimental results for the second generation SSDL MMIC without gate matching: insertion loss and isolation.

Even though the improvements to the switch model and delay length have improved the insertion loss at 1GHz when compared to the previous generation, the insertion loss at 10MHz is degraded by about 1dB. This may be attributed to the dispersion of the transmission line loaded with the transistor capacitance. The line appears shorter for lower signal frequencies, and becomes misaligned in delay with the switching signal. The other possibility is that a portion of the RF signal flows into the gate path instead of across the drain-source terminals. This creates two issues: the first is that the insertion loss will be higher than expected at the output, and the second is that the RF signal will modulate the gate signal and misalign the timing sequence, directly affecting power compression performance. This issue of gate-drain isolation is shown below in Figure 5.7. When a RF probe is used to touch down and provide the gate drive signals on-wafer, the probe's parasitic inductance resonates with the gate-drain capacitance, creating additional insertion loss.

Transforming the capacitive switch gate into a 50ohm impedance at the gate input using an L-match circuit greatly improves the observed insertion loss.

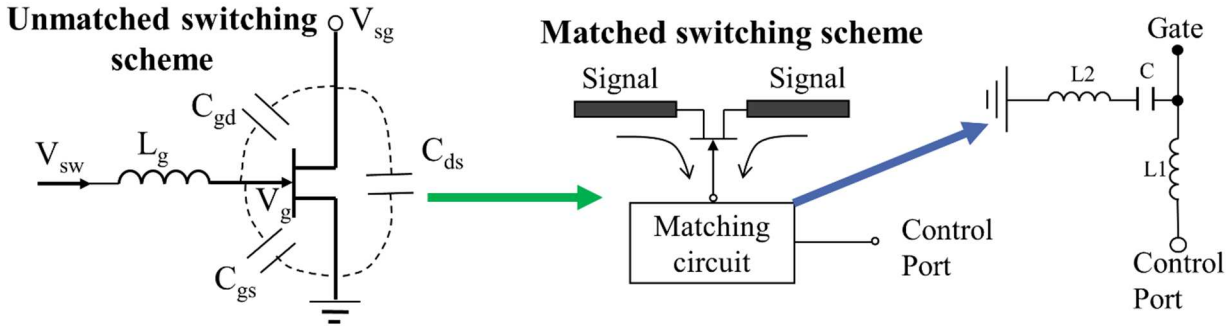



Figure 5.7: Unmatched switch gate showing the unwanted resonance, and the improved gate showing the L-match circuit.

Figure 5.8 shows the simulated and experimental results for the second generation SSDL MMIC circulator with gate matching. The insertion loss measures 2.5dB to 3.1 dB from 10MHz to 1GHz for this chip which is designed for a switching frequency of 1.25GHz. The matching circuit placed at the switch gates helps to improve the measured loss to a sub-3dB curve throughout the over-multiplexing operating range from 10MHz to 625MHz, as dictated by the Nyquist rate. The isolation is greater than 15dB over the measured frequency range between the TX and RX ports.

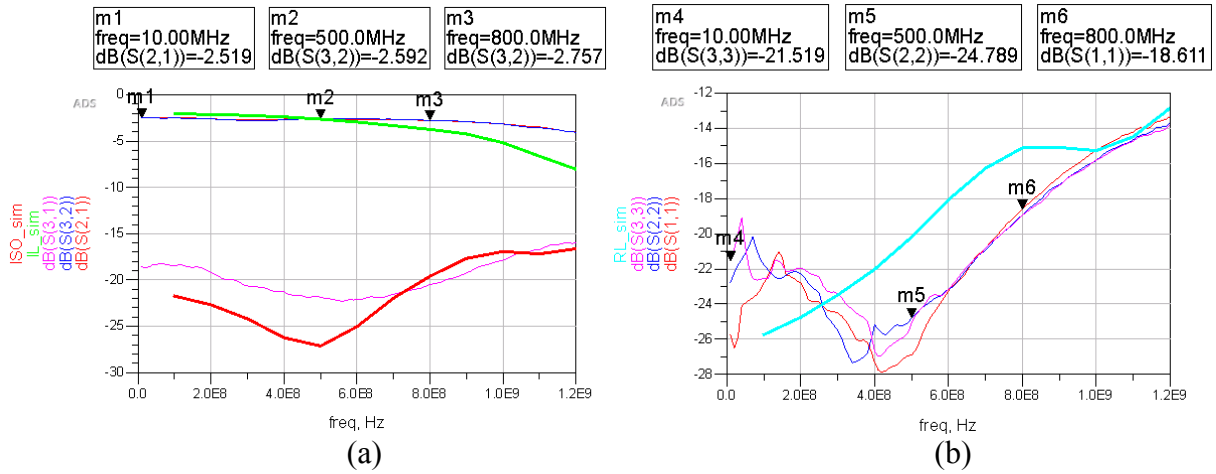



Figure 5.8: Simulated and experimental results for the second generation SSDL MMIC with gate matching: insertion loss and isolation (a), and return loss (b).

The measured return loss is mostly better than 20dB for the over-multiplexing operation mode. The simulated results, namely the insertion loss, shows degraded performance beyond 600MHz. This comparison shows that the additional capacitance terms added to the preliminary model were slightly overestimated. This overestimation also appears in the simulated return loss, which is worse than that of the measurement. Still, there is good agreement between the simulated and measured results over the over-multiplexing mode operation range, which is the focus of these designs. It is noted that the overall insertion loss has been greatly improved from the gate unmatched cases. This is because the addition of the matching circuit at the gate prevents the leakage of the RF signal to the control path. In addition to this, the over-estimated cap values could explain the higher IL at 10MHz for the unmatched second-generation chip (Figure 5.6). This difference would add to the dispersion of the transmission line and lead to timing misalignment for the lower portion of the frequency range. The disagreement between simulated and measured cases could also be the result of further refinements that are needed for the gate matching strategy. This is the subject of the next chapter.

### 5.2.3 Power Compression for Second generation SSDL MMICs

Power compression is also an important metric for circulator operation. OP1dB testing (1dB compression point referenced to the output) is performed at 500MHz for the second-generation GaN MMIC circulators. The OP1dB for the circulator without gate matching is approximately 10dBm with a total power consumption of 320mW, as shown by the blue trace in Figure 5.9. This power consumption counts the inputs to all of the switch transistor gates. The OP1dB for the circulator with gate matching is approximately 11dBm with a total power consumption of 50mW, as shown by the red trace in Figure 5.9.

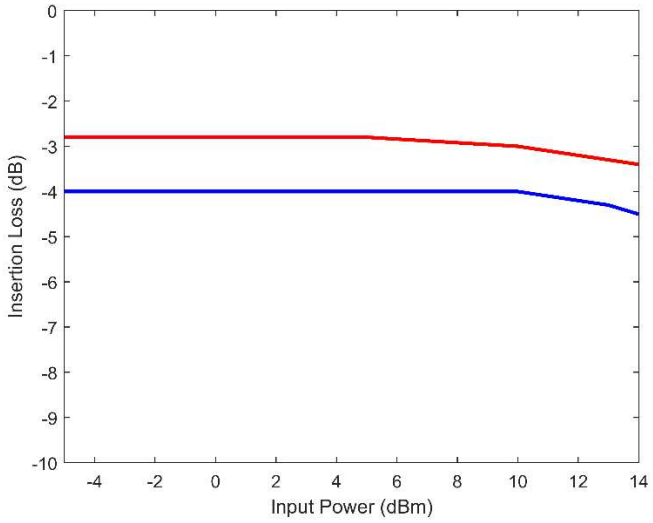



Figure 5.9: Measured P1dB results for the unmatched gate SSDL (blue trace) with a total power consumption of 320mW and the matched SSDL (red trace) with a total power consumption of 50mW.

As expected, the power consumption at the gates are greatly reduced due to the presence of the matching circuit. But it is evident from Figure 5.9 that the slight increase of OP1dB with the gate matching circuit is due to the reduced insertion loss observed in the SSDL circulator. Other methods to improve the observed OP1dB while maintaining the low insertion loss are investigated in the following chapter.

# CHAPTER 6

## Gate Matching Strategies for Power Compression Improvement

### 6.1 Gate matching considerations for high speed switching

As was verified in the previous chapter, the presence of gate matching circuitry helps to improve the observed insertion loss. However, the power compression point is not nearly high enough to be considered useful for future communication systems. As was discussed previously, the P1dB can also be affected by the signal leakage to the gate, as the large RF signal will turn the switch ON or OFF at improper times. This chapter will serve as a solution to the problem of power compression, while maintaining a low insertion loss.

#### 6.1.1 Bootstrapping circuits for switching-based circulators

Bootstrapping is a technique used frequently to increase the P1dB in RF switches by adding a high-value resistor at the gate. This ensures that the gate voltage follows that of the drain and source for RF and avoids unwanted turning ON and OFF scenarios. This traditional architecture utilizing the gate resistor is shown below in Figure 6.1.

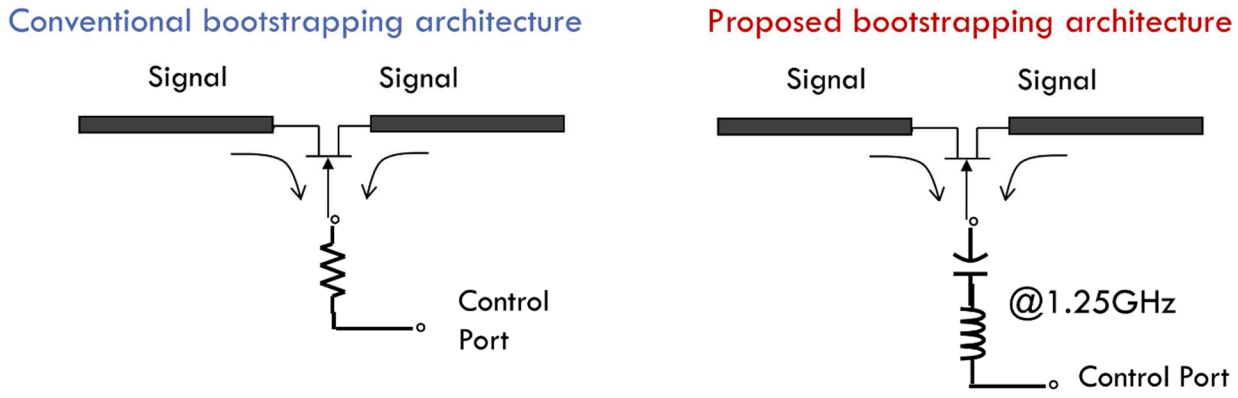



Figure 6.1: Conventional bootstrapping architecture (left) versus the proposed bootstrapping architecture (right) for SSDL.

However, the conventional architecture works only for a slower switching rate. It does not work for SSDL as the switching rate is faster than the signal frequency. If a resistor was placed in series with the switch transistor, the time constant created by the large resistance and series device capacitance would severely degrade the performance. A high-Q series LC resonator, resonating at the switching frequency, can be used instead for bootstrapping in the SSDL circulator. The impedance response versus frequency for a series LC resonator creates a low impedance at resonance, and a high impedance out of band. This means that the switching signal can be passed to the gate, and the RF signal will see a high impedance looking into the gate and continue across the drain-source as intended. An implementation of this strategy is presented in the next section.

## 6.2 Bootstrapping for the second generation unmatched SSDL MMIC

### 6.2.1 Experimental Methods

A picture of the printed circuit board used to test the high-speed bootstrapping strategy is shown below in Figure 6.2. The PCB material is Rogers 4003C with a substrate thickness of 32mil. It was fabricated using a laser milling machine manufactured by LPKF. The SSDL MMIC is the unmatched gate circulator from the second generation of designs (single series switch topology). The GaN chip sits on a layer of copper in the center of the PCB. There are ground vias made by the laser, which are later connected to the backside ground plane using conductive epoxy. The MMIC is then placed on top of the epoxy and is baked in an oven to create a reliable ground connection. There are also the COTS chip inductor and capacitor used to create the series LC resonator at 1.25GHz. Each part (size 0402) was placed onto the PCB after conductive epoxy was placed in the appropriate spots. Great care was taken to ensure that short circuit conditions were not created if the epoxy accidentally touched two transmission lines of the PCB.

These parts were secured to the board in a second baking cycle after mounting the MMIC chip. In addition to this, it is crucial to provide the proper DC bias to the switch gates to swing between the ON and OFF states at the correct time instances. For this PCB, two 500ohm resistors (size 0402) were placed in series on the PCB just after the capacitor in each series resonator. This allows a DC bias to be applied to the switch gates. The red wires are connected to each high resistance bias path and run to an external DC power supply.

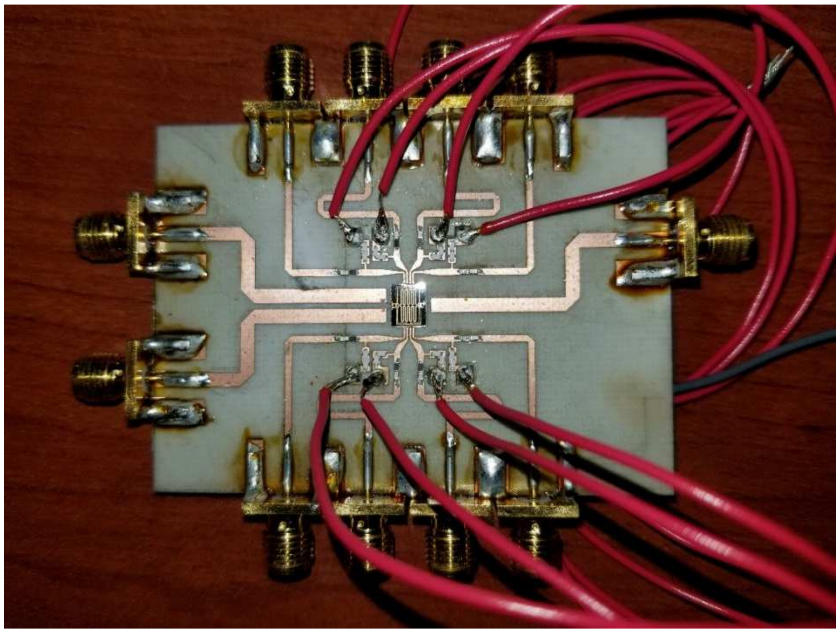


Figure 6.2: PCB assembled with the GaN MMIC circulator and COTS parts to realize the off-chip bootstrapping circuit.

The top and bottom of the PCB each have 4 SMA connectors. One SMA connector feeds a series LC resonator with a resistive DC bias to realize the off-chip bootstrapping circuit. Also, the impedance of these lines are closer to 70ohm on the 4003C PCB material to help alleviate the parasitics observed in simulation while using the COTS parts models. The TX and RX ports are on the left side of the PCB, and the ANT port is on the right. Each is fed by an SMA connector with 50ohm lines on the 4003C substrate. All of the signal paths (both RF and gate drive) are connected to the SSDL circulator using wire bonds. Three wire bonds are placed in parallel for

each connection from PCB to MMIC in an effort to reduce the inductance associated with the wire bonds. The drive network that supplies the gate drive signals is the same one used to test the previously demonstrated versions (hybrid couplers used to split a signal from a power amplifier). The results from this test setup are presented in the next section.

### 6.2.2 Experimental Results

Figure 6.3 shows the simulated and experimental results for the SSDL MMIC circulator with the off-chip bootstrapping circuit. The insertion loss measures 2.5dB to 3.3 dB from 10MHz to 1GHz for this chip which is designed for a switching frequency of 1.25GHz. The matching circuit placed at the switch gates again helps to improve the measured loss to a sub-3dB curve throughout the over-multiplexing operating range from 10MHz to 625MHz, as dictated by the Nyquist rate. The isolation is at worst 20dB over the over-multiplexing operating range between the TX and RX ports.

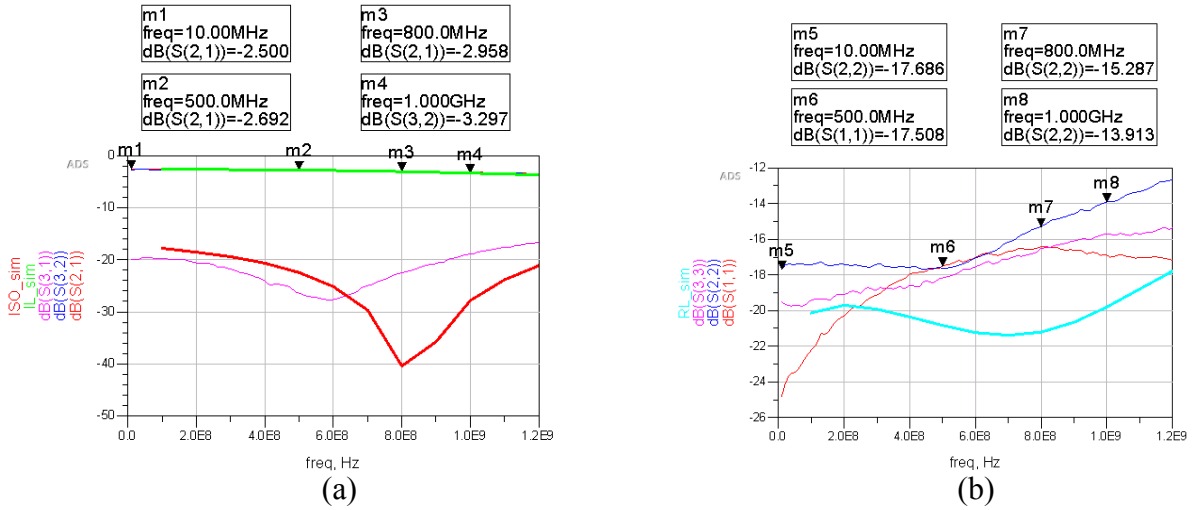



Figure 6.3: Simulated and experimental results for the SSDL MMIC with off-chip bootstrapping: insertion loss and isolation (a), and return loss (b).

There is excellent agreement between the simulated and measured insertion loss. This is due to the isolation created between the gate and drain by the series LC resonators. The RF signal should

only flow across the drain and source of the switch devices, and this appears as the insertion loss which is in addition to the loss incurred by the delay lines. The simulated and measured isolation are in relatively good agreement for the over-multiplexing mode frequency range, and the return loss is slightly worse than predicted by the model.

Most importantly, it must be validated that the power compression point increases using this bootstrapping gate method. The measured power compression results at 500MHz are shown below in Figure 6.4.

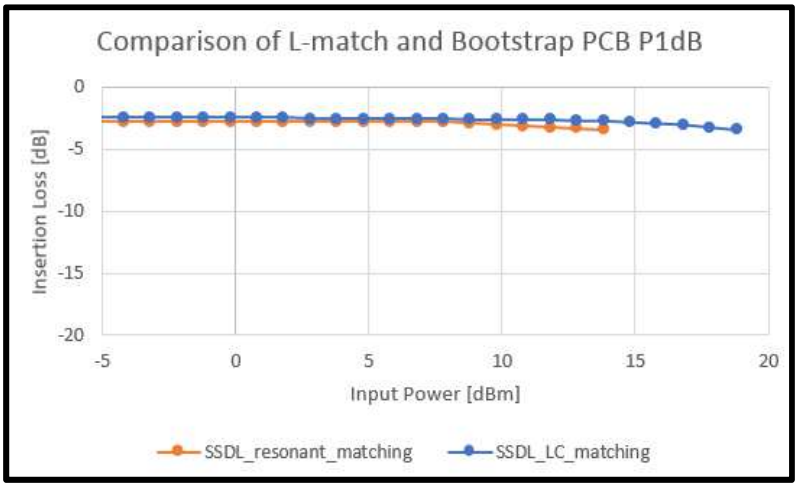



Figure 6.4: Experimental results for power compression of the bootstrapped gate PCB (blue trace) and the L-match on-wafer SSDL (orange trace).

The power compression is now 16dBm when referenced to the output. This is a 5dB improvement over the performance reported in the previous chapter. The bootstrapping technique must be move on-chip in order to improve the performance. In the next section, a technique similar to this is reported to further increase the SSDL GaN circulator power compression performance.

## 6.3 Development of harmonic matching circuit for P1dB improvement

Passive Bootstrapping with a series LC gate matching helps to improve P1dB by avoiding self-turning off (when transistors are supposed to be on) and positive biasing of the gate diode. In the ideal case, a square wave is applied to each switch gate and provides a 50% duty cycle of ON

and OFF times. However, this is very difficult to achieve practically, especially when using a series LC resonator which has a narrowband frequency response. The square wave helps to avoid self-turning on (when transistors are supposed to be off) by biasing the gate more negatively, as both of the self-turning off and self-turning on situations have to be considered in the design process. The development of a harmonic matching circuit is explained in this section which allows the fundamental and third harmonic signals to reach the switch gate and create a rectangular waveform.

### 6.3.1 Theoretical developments for SSDL harmonic gate matching

The harmonic matching circuit placed at the switch gate is shown below in Figure 6.5. It consists of a parallel LC tank placed in series with a series LC resonator. We want to create a series resonance for this circuit at both the fundamental and third harmonic frequencies. The resonant conditions created at each frequency can be related to each other to arrive at circuit values. This analysis is shown below.

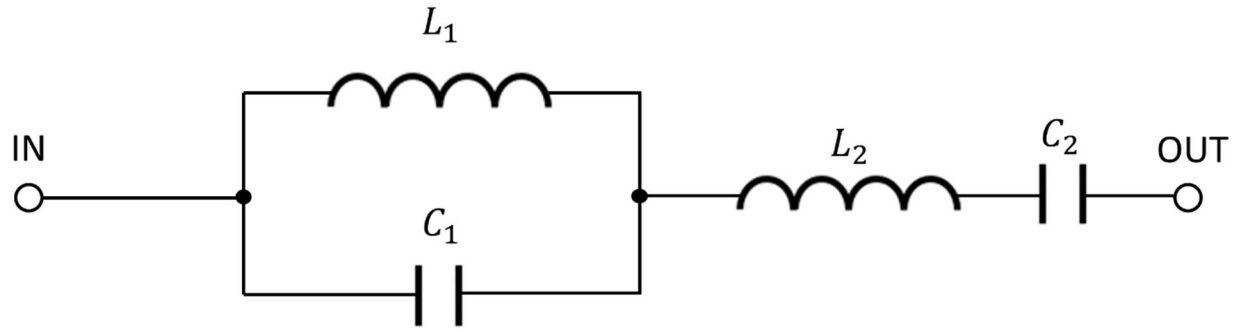



Figure 6.5: Schematic of harmonic matching circuit used to improve power compression performance of SSDL circulators.

The first step is to obtain the equivalent impedance response versus frequency for this circuit, as Equation 26 below shows:

$$Z(j\omega) = (Z_{L1} \,//\, Z_{C1}) + Z_{L2} + Z_{C2}$$

$$Z(j\omega) = \frac{j\omega L_1}{1 - \omega^2 L_1 C_1} + j\omega L_2 - \frac{j}{\omega C_2} \quad (26)$$

At resonance, the reactance terms are equal, meaning that:

$$\frac{\omega L_1}{1 - \omega^2 L_1 C_1} + \omega L_2 = \frac{1}{\omega C_2} \quad (27)$$

From here, the next step is to get Equation 27 in terms of $(a_1 x^2 + b_1 x + c_1 = 0)$, which leads to the following:

$$\omega^4 (L_1 C_1 L_2 C_2) - \omega^2 (L_2 C_2 + L_1 C_1 + L_1 C_2) + 1 = 0 \quad (28)$$

Note that $x = \omega^2$ so that $x^2 = \omega^4$. In addition, the following conditions are set:

$$Let\ a_1 = L_1 C_1 L_2 C_2\ ,\ b_1 = -(L_2 C_2 + L_1 C_1 + L_1 C_2),\ and\ c_1 = 1.$$

Series resonance at $3\omega$ is also required. Following similar steps as above, and setting $Z(3\omega) = 0$ leads to the equation shown below:

$$\frac{3\omega L_1}{1 - 9\omega^2 L_1 C_1} + 3\omega L_2 = \frac{1}{3\omega C_2} \quad (29)$$

The next step is to get Equation 29 in terms of $(a_2 x^2 + b_2 x + c_2 = 0)$, which leads to the following:

$$\omega^4 (81 L_1 C_1 L_2 C_2) - \omega^2 (9 L_2 C_2 + 9 L_1 C_1 + 9 L_1 C_2) + 1 = 0 \quad (30)$$

Again, $x = \omega^2$ so that $x^2 = \omega^4$. In addition, the following conditions are set:

$$Let\ a_2 = 81 L_1 C_1 L_2 C_2 = 81 a_1\ ,\ b_2 = -9(L_2 C_2 + L_1 C_1 + L_1 C_2) = 9 b_1,\ and\ c_2 = 1 = c_1.$$

Now, two equations exist from the information in Equations (28) and (30), each in terms of the quadratic formula:

$$a_1 x^2 + b_1 x + c_1 = 0 \text{ and } 81 a_1 x^2 + 9 b_1 x + c_1 = 0.$$

Setting these two equations equal gives the following:

$$80 a_1 x^2 + 8 b_1 x = 0 \quad (31)$$

Solving Equation 31 using the quadratic formula gives the following expression:

$$x = \omega^2 = \frac{1}{10}\left[\frac{1}{L_1C_1} + \frac{1}{L_2C_2} + \frac{1}{L_2C_1}\right]$$

Now, the expression for $\omega$ can be obtained as:

$$\omega = \sqrt{\frac{1}{10}\left[\frac{1}{L_1C_1} + \frac{1}{L_2C_2} + \frac{1}{L_2C_1}\right]} \quad (32)$$

Equation (32) describes the resonant frequency response of the harmonic matching circuit. The next step is to solve Equation (31) for the ratio of $b_1$to $a_1$:

$$x = \frac{-b_1}{10a_1} \quad (33)$$

Next, Equation (33) is substituted back into $(a_1x^2 + b_1x + c_1 = 0)$ to get:

$$b_1{}^2 = \frac{100a_1}{9},\ or\ b_1 = \pm\frac{10}{3}\sqrt{a_1}.$$

The solution $b_1 = -\frac{10}{3}\sqrt{a_1}$ is chosen with $b_1 = -(L_2C_2 + L_1C_1 + L_1C_2)$ and $a_1 = L_1C_1L_2C_2$ to get the following expression:

$$L_2C_2 + L_1C_1 + L_1C_2 = \frac{10}{3}\sqrt{L_1C_1L_2C_2} \quad (34)$$

If we set $L_1 = L_2$ in Equation (34), it simplifies to:

$$2C_2 + C_1 = \frac{10}{3}\sqrt{C_1C_2} \quad (35)$$

Squaring both sides of Equation (35) and rearranging terms gives the following expression:

$$4C_2{}^2 - \frac{64}{9}C_1C_2 + C_1{}^2 = 0 \quad (36)$$

Dividing the above expression by $C_1{}^2$ leads to a quadratic equation with the following parameters:

$$x = \frac{C_2}{C_1},\ a = 4,\ b = -\frac{64}{9},\ and\ c = 1.$$

Now, the quadratic formula is used to solve for x. The solution that is used here is:

$$C_2 = 1.624C_1 \; with \; L_1 = L_2$$

Finally, we plug in the above conditions to Equation (32) to get everything in terms of $L_1 \; and \; C_1$:

$$\omega = \sqrt{\frac{1}{10}\left[\frac{1}{L_1C_1} + \frac{1}{L_2C_2} + \frac{1}{L_2C_1}\right]} = \sqrt{\frac{1}{10}\left[\frac{1}{L_1C_1} + \left(\frac{1}{1.624}\right)\frac{1}{L_1C_1} + \frac{1}{L_1C_1}\right]} \quad (37)$$

Rearranging Equation (37) for $L_1$ leads to the following expression:

$$L_1 = \frac{2.616}{10\omega^2 C_1} \quad (38)$$

Setting $C_1 = 0.3\text{pF}$ in Equation (38) gives example values for the harmonic matching circuit:

$$L_1 = \; L_2 = 14.1nH. \; C_2 = 1.624C_1 = 0.5pF.$$

### 6.3.2 SSDL simulation results using harmonic gate matching

A layout picture of the harmonic matching circuit designed on-chip with the SSDL circulator is shown below in Figure 6.6.

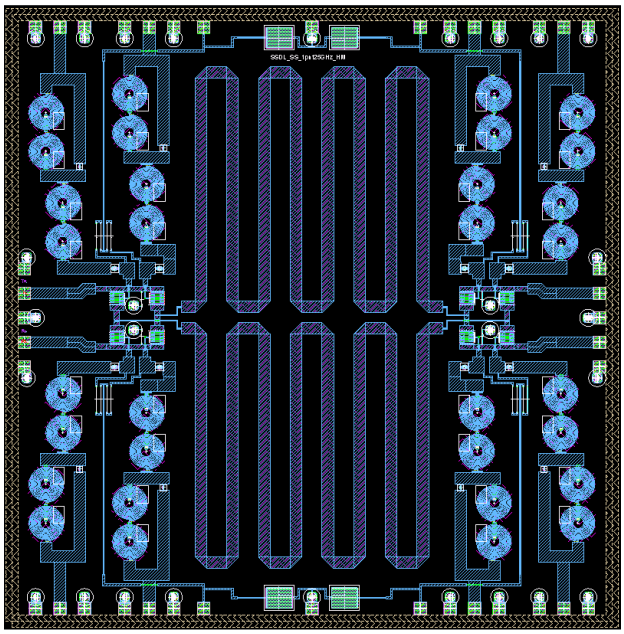


Figure 6.6: Layout of harmonic matching circuit used to improve power compression performance of SSDL circulators.

This chip is configured to measure the four-port circulator performance as described in Chapter 2, with dimensions of 5mm by 5mm. The DPDT switches are composed of the single-series topology. The TX and RX pads are at the left edge of the chip, and the ANT1 and ANT2 are at the right edge of the chip. There are a total of eight identical harmonic matching circuits, each of which drives a transistor of each DPDT switch. The inductors are sized to give the maximum possible Q, and thus the highest quality factor for series resonance at 1.25GHz. $C_1$ has a value of 50.7fF and $C_2$ has a value of 187.5fF. It turns out that the value of $C_2$ has to be optimized when placed in series with the capacitive gate of the transistor in order to maintain the proper frequency response. Input gate signals are fed to the harmonic matching circuits through GSG RF pads. Also, the resistive DC bias is added on-chip in this version. There are four identical DC voltage paths each with 10pF RF bypass caps to ground. Two 2.5kohm resistors are placed in series to give the total bias path resistance of 5kohm. The simulated results for power compression performance at 530MHz are the only results available at this time, and are shown below in Figure 6.7.

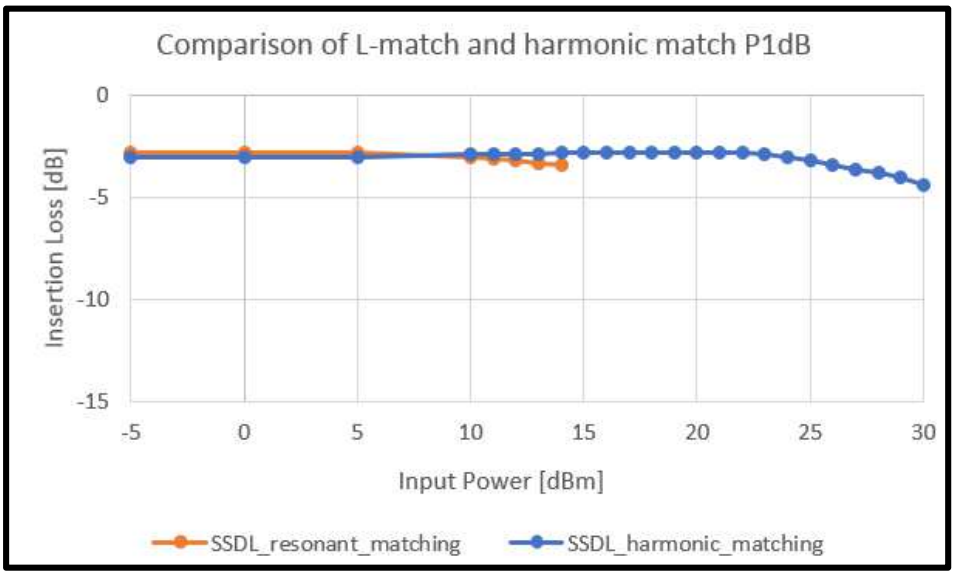



Figure 6.7: Power compression results for the SSDL with harmonic matching (blue trace) versus the second-generation SSDL with L-section matching (orange trace).

It is evident that the harmonic matching at the switch gates leads to significantly higher power compression (>25dBm OP1dB). This is a >10dB improvement in power compression performance when compared to the previously measured results. This circulator MMIC will be taped out with experimental results to be reported as part of the future work. In simulation, the power consumption is ~700mW, which is much higher than that of the gate matching circuit with an L-section match. This is because the harmonic matching design for this tape out was solely focused on achieving the highest possible P1dB. An ideal harmonic matching design would need additional matching circuitry to boost the voltage that appears at the gate through the Q-factor, as is the case for the L-section match SSDL circulator. The focus of this latest tape out is to verify the power compression performance of the harmonic matching circuit, and then move on to more efficient designs.

# CHAPTER 7

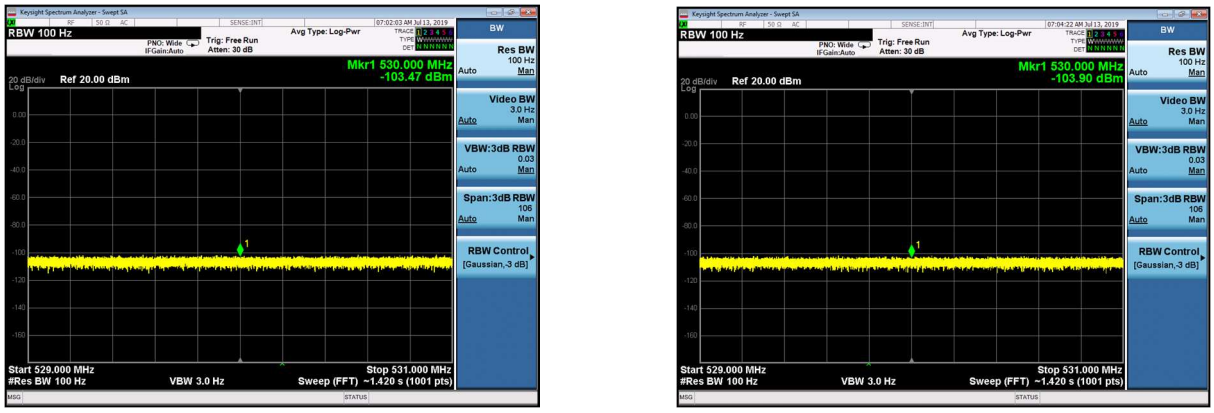
# Noise Floor Performance for the SSDL Circulator

## 7.1 Noise floor characterization

When dealing with any switch-based circuit, it is important to characterize any degradation to the noise floor of the test environment. If the switching mechanisms are working properly, there should be no degradation to the system noise floor, as the switches are passive elements. The tests conducted here are on the SSDL GaN MMIC with external boot-strapping circuits on PCB (Section 6.2).

### 7.1.1 Noise floor with and without switching signal

The SSDL circulator works by introducing sequential switching operations to a waveform, that divides it into equal pieces in time. The switching (clock) signal should not interfere with the noise floor of the circulator. Figure 7.1 below proves that this is indeed the case.




(a) (b)

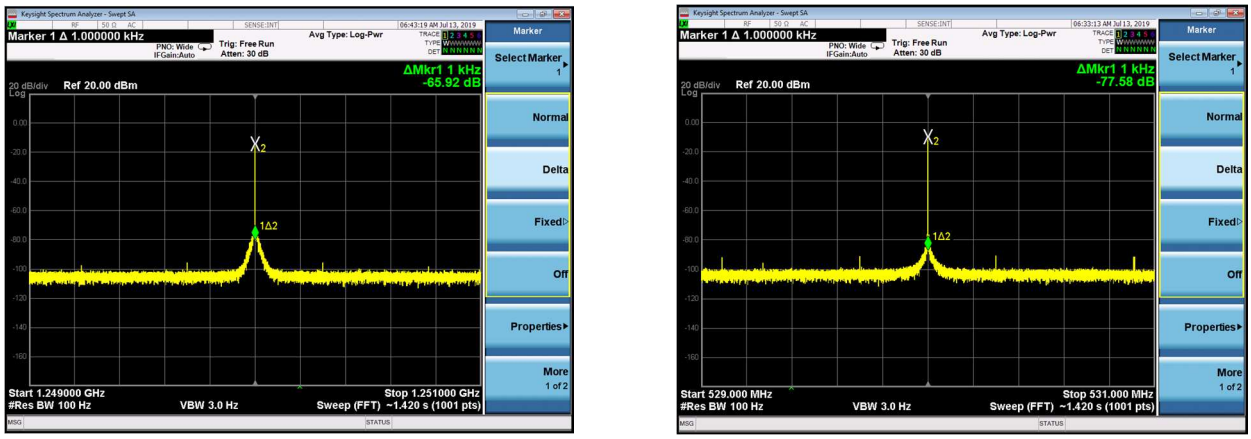
Figure 7.1: Noise floor of SSDL ANT port without switching (a) and with switching (b).

Noise floor tests are conducted by terminating the TX and RX ports in matched loads while monitoring the ANT port on the spectrum analyzer. The clock signals are applied at 1.25GHz to show that there is no degradation to the noise floor whether the clock signal is applied or not. The

Resolution Bandwidth (RBW) and Video Bandwidth (VBW) are respectively set to 100Hz and 3Hz. This allows for a very fine spectral resolution and a low noise floor to start. These settings are the same for all of the test results in this chapter.

### 7.1.2 Phase Noise of the Clock and RF input

It is just as important to understand the signal quality of both the RF input signal and the clock signal before applying them to the SSDL for spectral measurements. Figure 7.2 shows the spectrums of both the clock and RF input signals that are coming from signal generators.



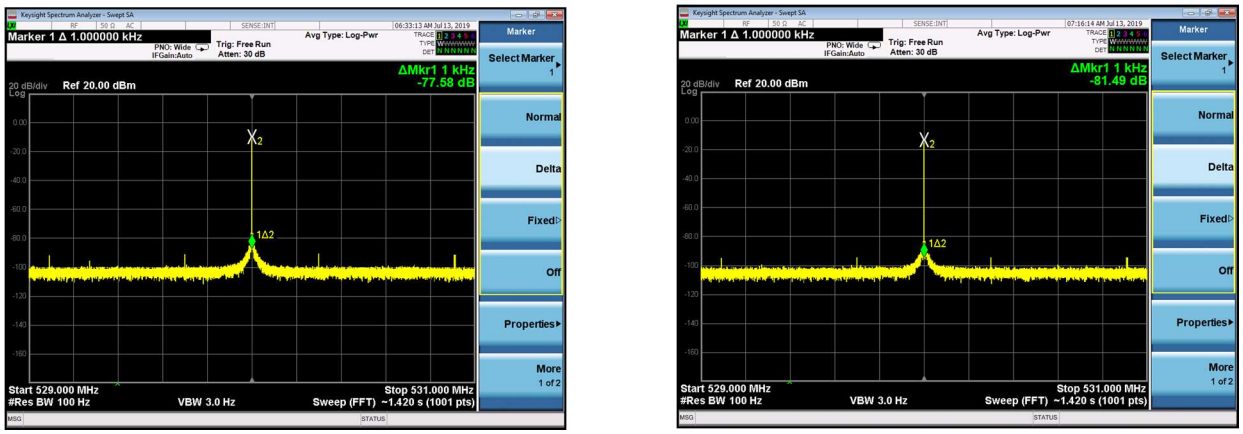

(a) (b)

Figure 7.2: Phase noise of the clock at 1.25GHz (a) and the RF input signal at 530MHz (b).

The clock and RF signals each have a marker used to detect their peak. A 1kHz offset (delta) marker is applied to this peak measurement to obtain the initial phase noise of the two signal generators. Even though the same signal generator model is used for the tests, it was discovered that one generator had a phase noise approximately 12dB better than the other. It was decided that the signal generator with the better phase noise was to be used for the TX signal, as demonstrated in Figure 7.2b.

### 7.1.3 Phase noise performance versus RF input power

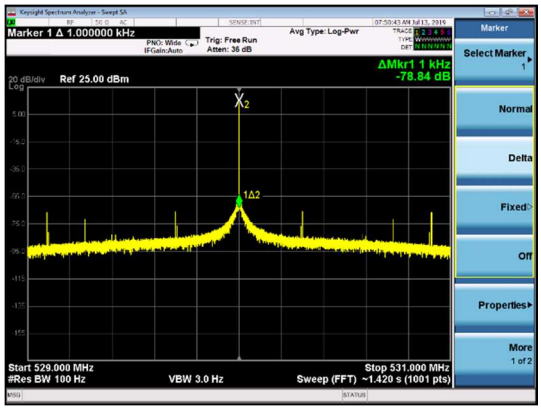
Now that the noise floor and phase noise performance of the clock and RF inputs have been characterized, the next step is to measure the phase noise performance of the SSDL circulator with the clock signal and RF signal present. The first test is with an RF input power of -10dBm at 530MHz. Figure 7.3 shows the before (TX) and after (ANT) spectral performance of SSDL.



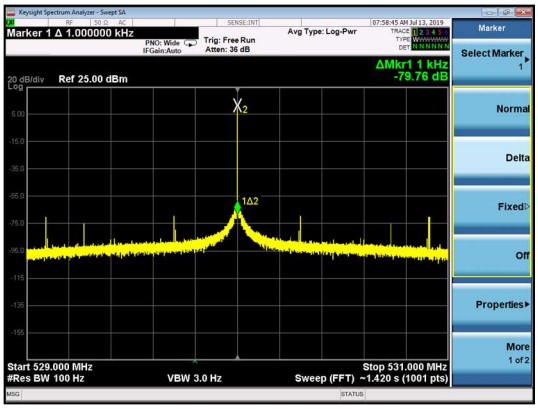

(a) (b)

Figure 7.3: Phase noise of the -10dBm RF signal entering the TX port (a) and after the SSDL circulator at the ANT port output (b).

There is no observed degradation to the phase noise of the TX signal as shown by Figure 7.3. At this small TX input power of -10dBm, this is the expected behavior. However, as the circulator starts to compress (where the insertion loss starts to increase) the phase noise will start to degrade. Figure 7.4 shows the results for the same test setup as Figure 7.3, but with a TX input power of +15dBm. The SSDL circulator with off-chip bootstrapping on PCB has an OP1dB of +16dBm, so this TX input power level should create some phase noise degradation.




(a)



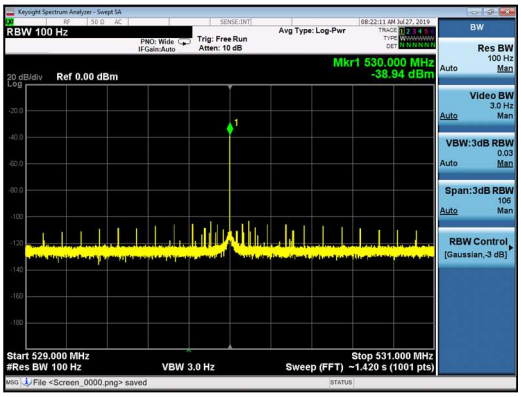

(b)

Figure 7.4: Phase noise of the +15dBm RF signal entering the TX port (a) and after the SSDL circulator at the ANT port output (b).

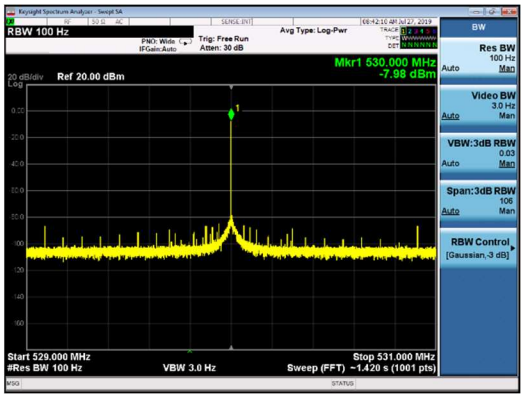
No degradation to the noise floor is observed in this case either. This may be to the limited capability of the signal generator used to create the TX input signals at 530MHz. A possibility of future work could be a more in-depth study of the phase noise of SSDL circulators. With that said, the SSDL circulator behaves as intended with no noise floor penalty due to switching.

### 7.1.4 RX spectrum under phase noise measurements

It is also important to measure the isolation at the RX port when the RF signal is active at the TX port and the clock signal is present. Figure 7.5 below shows that the isolation is maintained between the TX and RX ports for TX input power levels of -10dBm and +15dBm.




(a)




(b)

Figure 7.5: Signal level observed at the RX port during TX input powers of -10dBm (a) and +15dBm (b).

The TX to RX isolation is approximately 26dB for the -10dBm TX input and approximately 23dB for the +15dBm TX input. The -10dBm input case agrees well with the reported small signal measurements for this same design. These tests demonstrate that the SSDL with bootstrapping maintains good isolation between the TX and RX ports during operation. These gate matching techniques will need to be moved on-chip in order to improve the overall performance, as was previously discussed.

# CHAPTER 8

## Conclusion and Future Work

The Sequentially-Switched Delay Line (SSDL) circulator has the potential to provide full duplex communication over a broad bandwidth in a package size which is more suitable for integration with various integrated circuits. The theory of SSDL operation was introduced, followed by a COTS demo and various performance analyses. Practical SSDL designs were introduced over two generations of SSDL GaN MMIC circulators, followed by two separate improvements to the power compression point through switch gate matching. The last chapter introduced the validation of noise floor and phase noise performance of SSDL.

Future work will complete measurements of the on-chip harmonic matching gate circuits used with SSDL. These measurements will be compared against the simulated results shown in this dissertation. Beyond this, more in-depth characterizations of the phase noise performance of SSDL and further P1dB improvements will be made.

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