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NEM Relay Scaling for Ultra-low Power Digital Logic

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NEM Relay Scaling for Ultra-low Power Digital Logic

by

Jack Yaung

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Committee in charge:

Professor Tsu-Jae King Liu, Chair
Professor Elad Alon
Professor Junqiao Wu

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Abstract

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CMOS has been the building block for modern digital logic for decades and the performance and energy efficiency of CMOS continues to improve as technology develops, mainly through scaling. However due to the 60 mV/dec limit on MOS transistors, continue to reduce the power supply voltage would result in an increase in off-stage leakage current that would eventually dominate and increase the energy per operation of a transistor. In order to overcome this barrier, mechanical switches are proposed. Mechanical relays has the benefit of no leakage current through the air gap in the off state, which potentially enables further scaling of power supply voltage that can surpass MOS transistors. Several groups have been able to demonstrate mechanical switches with no leakage and abrupt on-off switching characteristics, however both the sizes of switches (~10^4 μm^2) and the operation voltages (> 10 V) are huge, causing the switching energy to be significantly larger than MOS transistors. Scaling efforts are needed to minimize the switching energy of a mechanical switch.

In this thesis, prototype relay devices demonstrated by previous studies are discussed and the key factors that need to be addressed in order to minimize the switching energy are pointed out. The minimum switching energy is found to be limited by the contact adhesive force between contacts; studies on prototype devices with different contact areas shows that van der Waals force between contacts are the main source of adhesion in the prototype mechanical relays. Experiments show that by adding surface coating materials with low Hamaker constant can lower the contact adhesive force. In order to lower the structural stiffness, process development of poly-SiGe is optimized through multiple post-deposition processing techniques for reduced stress gradient of 100 nm thin films, a 10X reduction from the prototype devices. The combined learning from adhesive force work and thin film processing leads to the experiments of fabricating scaled devices of 500X smaller footprint. The results show that scaled relays can potentially operate at low voltages (~2V), but more process optimization needs to be done to demonstrate a fully operational device.

To my family

Table of Contents:

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Chapter 1

Introduction

1.1 The CMOS Power Crisis

The evolution of technology not only depends on great minds, but also the capability to store and compute large amounts of information. As technology advances the amount of information processed is reaching incredible levels and yet more computational capacity is needed than ever. Complementary Metal-Oxide-Semiconductor (CMOS) transistors are the building blocks used predominantly in very large scale integrated circuits (“chips”) since the 1980s. The number of transistors on a chip has roughly doubled every two years with each new generation of CMOS technology, so that the transistor count in the most advanced microprocessors grew from 42 million to 3 billion over the past decade [1]. Along the way, the performance and energy efficiency of CMOS transistors has improved, mainly due to miniaturization. By scaling down the device dimensions, capacitance and resistance are reduced, resulting in improved switching speed and decreased switching energy.

A fundamental challenge for continued CMOS technology scaling is that the chip operating voltage (V_{DD}) cannot be reduced without degrading the transistor on/off current ratio. For this reason the leakage power density has been allowed to increase in recent CMOS technology nodes, so that it is now comparable to active power density [2] as shown in Fig. 1.1, in order to ensure sufficient circuit operating speed. Due to exponentially increasing off-state leakage current with threshold voltage (V_{TH}) reduction, however, V_{TH} and V_{DD} scaling has slowed since the 90 nm technology node [3] as shown in Fig. 1.2.

If V_{DD} is not reduced proportionately with transistor dimensions, then the active (switching) power density of a chip increases. For this reason parallelism (i.e. multi-core processors) was adopted beginning in 2005 to achieve improvements in system-level performance while averting a chip power density crisis (Fig. 1.3) [4].

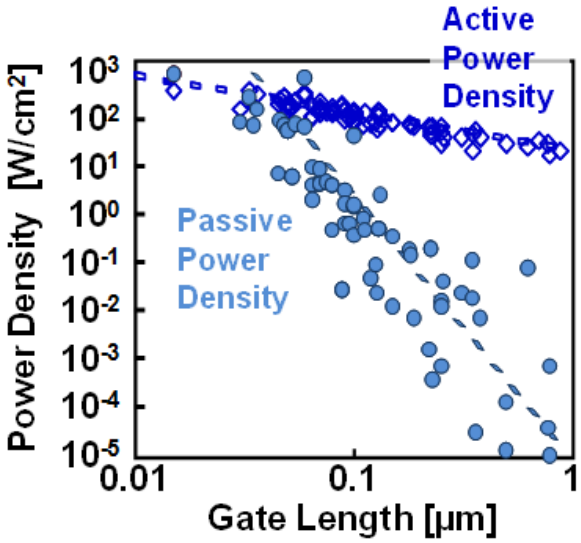


Fig. 1.1 Chip power density vs. MOSFET gate length. Passive power density has been allowed to increase to become comparable to active power density (adapted from [2]), with CMOS scaling.

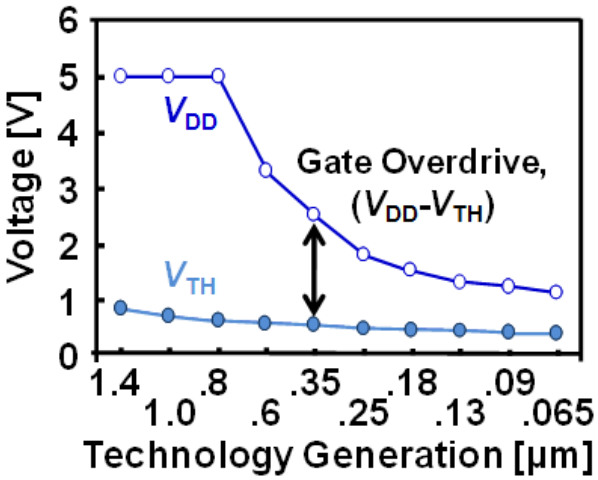


Fig. 1.2 Historical supply voltage and MOSFET threshold voltage scaling (adapted from [3]).

1.2 The Subthreshold Swing Limitation of CMOS

The reason for the CMOS power crisis is the nonscalability of V_{TH}. Fig. 1.4 illustrates the transfer characteristics of a CMOS transistor. In the sub-threshold region of operation, the output (drain) current increases exponentially as the input (gate) voltage increases. The steepness of this switching behavior is the Subthreshold Swing (SS), which is defined as the voltage swing required to effect a change in current by one order of magnitude (*i.e.* the inverse slope of the transfer characteristic in the sub-threshold region). A low value of SS is desirable, since it would mean that a smaller voltage swing is needed to switch the transistor on/off (*i.e.* V_{DD} can be reduced). SS for a conventional planar bulk silicon MOS transistor is given by the following equation [5]:

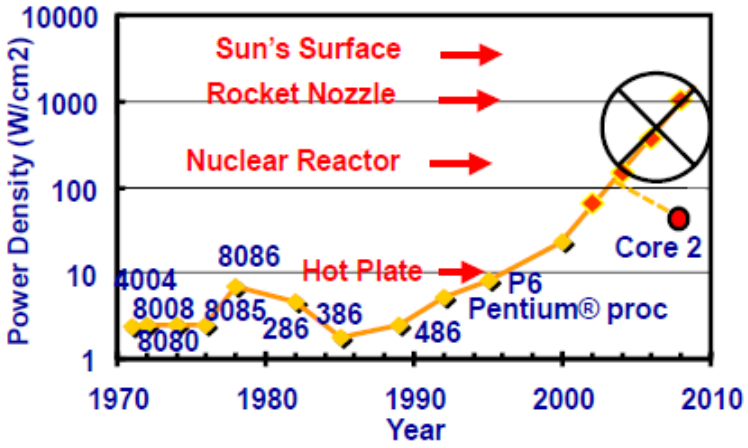


Fig. 1.3 Power density of commercial microprocessors. In recent years the power density of a microprocessor operates around the power density of a nuclear reactor, e.g. 65 W and 130W for Intel® CoreTM2 Duo E6320 (die size of 143 mm^2) and Intel® CoreTM i7-990X (die size of 239 mm^2), respectively [4].

$$SS = \left(1 + \frac{C_{DEP}}{C_{OX}}\right)\left(\frac{kT}{q}\ln 10\right) \tag{1.1}$$

where C_{OX} is the gate capacitance, C_{DEP} is the depletion capacitance, k is the Boltzmann constant, T is the absolute temperature and q is the electronic charge. The first factor on the right-hand side accounts for the capacitive voltage divider effect, and represents the ability of the gate voltage to control the semiconductor surface potential; it is always larger than 1. The second term relates to the thermal distribution of mobile charge carriers. Since kT/q = 25.6 mV, SS cannot be smaller than 60 mV/dec at room temperature.

For a given (maximum) off-state leakage current specification (I_{OFF}), SS sets the minimum value of V_{TH}. Lower I_{OFF} dictates a higher V_{TH} and hence lower on-state drive current (I_{ON}) for a fixed value of V_{DD} [6]. This trade-off between I_{OFF} and I_{ON} is illustrated in Fig. 1.5.

An electronic switch that has SS lower than 60 mV/dec would allow for lower operating voltage with the same off-state leakage, making the device more energy efficient. The lower the SS, the more energy efficient a device can be.

1.3 MEM Relays for Energy-Efficient Computing

Current flow in a mechanical switch (relay) – which functions by making and breaking physical contact between conductive electrodes – transitions abruptly between off and on states, so that SS is nearly zero. Also, a mechanical switch has zero I_{OFF}, since an air-gap exists between the conductive electrodes in the off state, so that it can in principle provide for zero static power dissipation as well as very low active power dissipation. A simple three-terminal micro-electro-mechanical (MEM) relay structure comprising a cantilever beam is illustrated in Fig. 1.6. In the

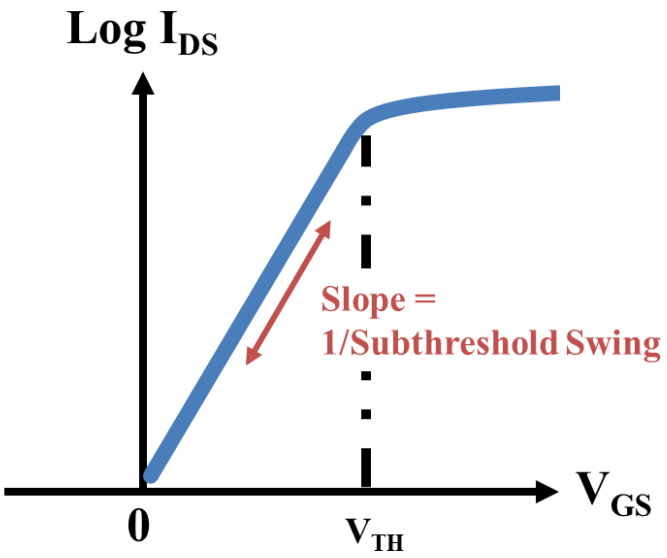


Fig. 1.4 Transfer characteristic of an n-channel MOSFET (semi-log plot). Current increases exponentially with gate voltage (V_{GS}) in the subthreshold region, then linearly for $V_{GS} > V_{TH}$. The subthreshold swing (SS) is defined as the inverse of the subthreshold slope. Note that there is non-zero current in the off state ($V_{GS} = 0$ V), which results in static power dissipation.

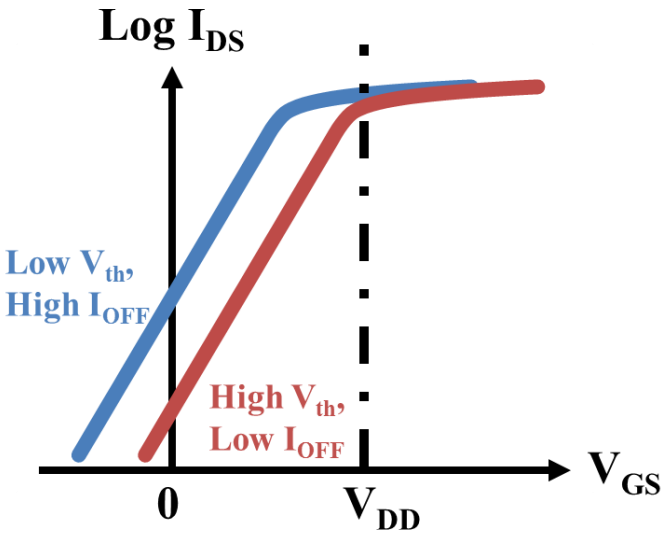
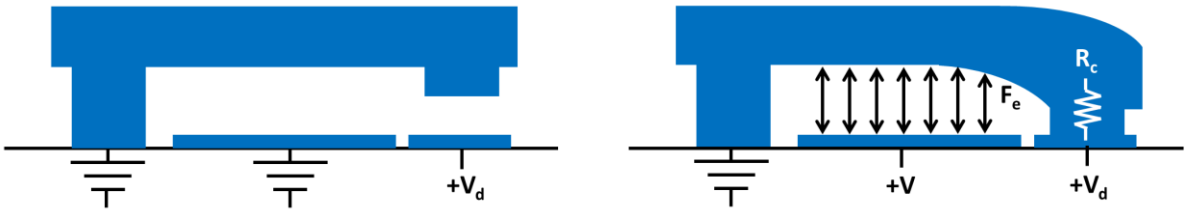


Fig. 1.5 Transfer characteristics for MOSFETs with different values of V_{TH}. Low V_{TH} provides not only for higher drive current (at $V_{GS} = V_{DD}$) and hence faster circuit operation, but also much higher off-state leakage current (I_{OFF}) and hence greater static power dissipation.

off state, an air gap exists between the cantilever tip and the underlying drain electrode so that no current can flow. If the voltage applied between the gate electrode and the cantilever beam exceeds a certain threshold, the electrostatic attractive force is sufficient to pull the tip of the cantilever beam into contact with the drain electrode so that current can flow. A conceptual current-*vs*.-voltage (I-V) characteristic is plotted in Fig. 1.7.



a) b)

Fig. 1.6 Schematic cross-sectional illustration of a MEM relay. a) In the off state, there is zero leakage current since an air gap prevents current flow between the cantilever beam tip and underlying drain electrode. b) In the on state, electrostatic force between the gate electrode and the beam brings the tip into contact with the drain electrode. The on-state resistance is dominated by the contact resistance (R_C).

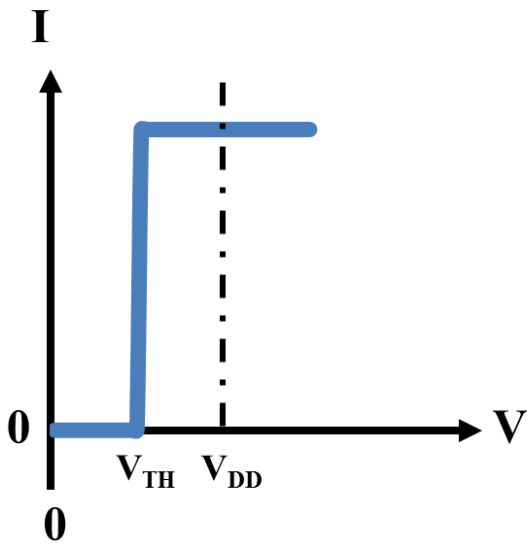


Fig. 1.7 Conceptual transfer characteristics of a MEM relay. There is no leakage in the off state and the transition between off- and on-states is abrupt. V_{TH} can be reduced without any leakage power penalty.

Since they are generally larger and slower than transistors, MEM relays have been considered for applications such as RF switching or CMOS power gating [7][8]. In recent years, interest in scaled relay technology for digital computing has grown due to the CMOS power crisis. This is because a scaled, low-voltage relay technology potentially can provide for improved energy efficiency beyond the limits of CMOS technology. Much progress has been made in recent years to realize MEM switches with operating voltage approaching 1 V with high manufacturing yield and to demonstrate relay-based integrated circuits. Recently reported MEM switches are still behind state-of-the-art CMOS devices, as can be seen in Fig. 1.8 [10-18]. Relays must be scaled to nanoscale dimensions in order to be competitive [9].

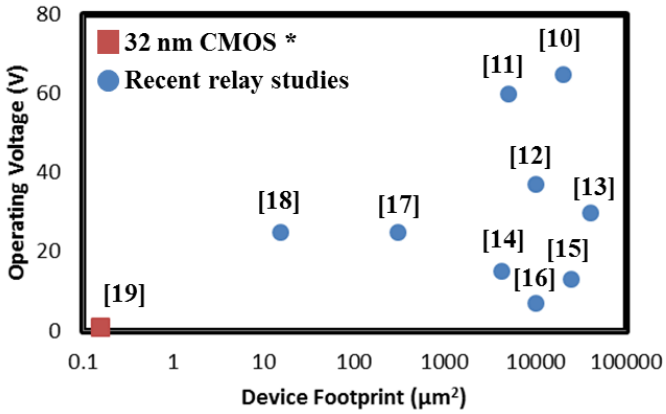


Fig. 1.8 Benchmarking of device footprint and operating voltage of recently reported mechanical switches for digital logic. It is desired to have low operating voltage with small device footprint. There is generally a tradeoff between device footprint and operating voltage. *Shown for reference is the footprint of a 6-transistor SRAM cell (0.157 μm^2) operated with V_{DD} = 1 V [19].

1.4 Thesis Overview

This thesis investigates NEM relays as potentially more energy-efficient alternatives to CMOS transistors for digital computation. Fundamental limitations for relay technology are identified, since off-state leakage and SS are not the limiters. Process technology challenges for NEM relay fabrication are also addressed.

Chapter 2 presents a MEM relay design that achieves zero off-state leakage and abrupt switching characteristics, and identifies the key issues that must be addressed in order to realize an energy efficient NEM relay. Performance characteristics of ultimately scaled NEM relays are projected.

Chapter 3 investigates contact adhesion, which can limit the energy efficiency of a mechanical switch. Adhesive force is extracted from electrical measurements and careful characterization of relay dimensions and contact topography. The cause of adhesion is identified by comparing experimental results with theoretical modeling. Surface coating is demonstrated to mitigate contact adhesion.

Chapter 4 investigates approaches to reduce the stress gradient within a thin polycrystalline $Si_{1-x}Ge_x$ (poly-SiGe) structural film, which is used for nanoscale relay fabrication.

Chapter 5 describes the fabrication of scaled relays using e-beam lithography and optimized thin poly-SiGe films, which have 500× smaller footprint as compared to the prototype devices in Chapter 2. Remaining challenges for realizing a fully functional scaled NEM relay are discussed.

Chapter 6 summarizes the key results and contributions of this work, and offers suggestions for future research directions.

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Chapter 2

MEM Relay Theory and Operation

2.1 Introduction

A scaled relay is a promising candidate to replace the transistor for ultra-low-power digital computing applications, because it offers the ideal characteristics of zero off-state leakage and abrupt switching behavior so that it in principle can provide for zero standby power and overcome fundamental V_{DD} scaling limitations for CMOS technology [1].

In this chapter, a prototype micro-electro-mechanical (MEM) relay design for digital logic applications is presented. In Section 2.2, the structure and operation of the 6-terminal relay are described. With the aid of the relay switching energy expression developed in Section 2.3, Section 2.4 identifies contact adhesion reduction and spring constant scaling by thinning the structural film as the key challenges to improve relay energy efficiency. In Section 2.5, switching energy projections of nanometer-scale (NEM) relays are made using Finite Element Method (FEM) simulations. Finally, Section 2.6 discusses some of the common concerns for NEM relays.

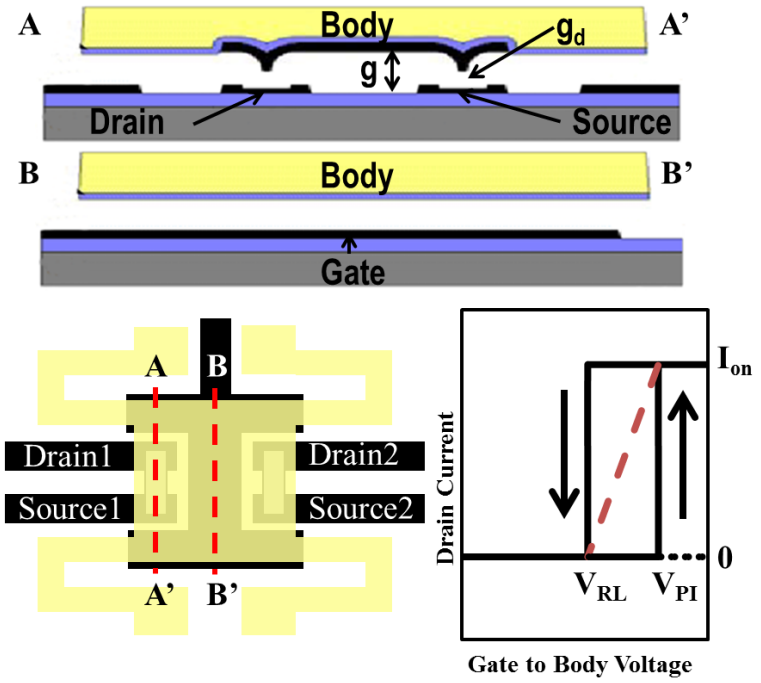

Fig. 2.1 Top: Schematic cross sections through the channel (A-A') and center (B-B') of a MEM logic relay. Bottom left: Plan-view illustration of the MEM logic relay. Bottom right: conceptual I_{DS}-V_{GB} characteristic of a MEM logic relay. The dashed line indicates an effective sub-threshold slope due to the difference between the turn-on voltage (V_{PI}) and turn-off voltage (V_{RL}).

2.2 Prototype MEM Relay

2.2.1 Device Structure and Operation

Fig. 2.1 illustrates the structure of an electrostatically actuated relay designed for digital logic applications [2]. The movable body electrode is suspended by folded-flexure beams above the source, drain and gate electrodes. No current flows in the off state because the channels (conductive strips attached underneath the body via an intermediary dielectric layer of Al_2O_3) are separated from the source/drain electrodes by the contact dimple gap. If a voltage is applied between the gate and body electrodes, the resultant electrostatic attractive force (F_e) will actuate the body downward. When the applied gate-to-body voltage (V_{GB}) is greater than or equal to the pull-in voltage (V_{PI}), the channels will come into contact with the underlying source/drain electrodes, so that current can flow and hence the device is in the on state. Note that the current increases abruptly as V_{GB} is increased above V_{PI} to turn on the device. To turn off the device, V_{GB} must be reduced below the release voltage (V_{RL}) such that the spring restoring force (F_k) is larger than the contact adhesive force (F_A) plus the electrostatic force (F_e) and the channels will come out of contact with the source/drain electrodes. Note that the current decreases abruptly as V_{GB} is decreased below V_{RL} and that $V_{RL} < V_{PI}$.

2.2.2 Fabrication Process

Prototype 6-terminal MEM logic relays were fabricated as follows. First, 100 nm Al_2O_3 was deposited via Atomic Layer Deposition (ALD) to insulate the surface of the Si wafer substrate. Then, 50 nm Tungsten (W) was deposited by sputtering and patterned to form the source, drain and gate electrodes. Next, 100 nm SiO_2 (low temperature oxide, or LTO) was deposited via Low-Pressure Chemical Vapor Deposition (LPCVD) to form the first sacrificial layer, and patterned to define the contact dimple regions. Afterwards, a second layer of sacrificial LTO was deposited to provide for the contact dimple gap. Then, 50 nm W was sputtered and patterned to form the channels, and 50 nm Al_2O_3 was deposited by ALD to insulate the channels from the body. Prior to deposition of 1 μm p-type polycrystalline-$Si_{0.4}Ge_{0.6}$ structural/body material by LPCVD, via holes were etched through the sacrificial layers to form anchor and interconnect regions. Lastly the structures were released by selectively removing the sacrificial LTO layers in HF vapor. Lithography is done using an ASML300 stepper with minimum feature size of 250 nm. ALD Al_2O_3 is chosen as the insulating material due to its high resistance to HF vapor etching [3] [4]. An illustration of the process flow is shown in Fig. 2.2. Fig. 2.3 shows plan-view and cross-sectional scanning electron microscopy (SEM) images of a fabricated relay.

2.2.3 Measured Device Characteristics

Measured I_{DS}-V_{GB} characteristics are shown in Fig. 2.4. In the off state, the relay shows immeasurably low leakage current (<1 pA) [5]. The relay turns on abruptly when V_{GB} increases above 10 V, transitioning from the OFF state to the ON state within a 1 mV step, as shown in Fig. 2.5. (1 mV is the minimum step size of the semiconductor parameter analyzer, so the actual subthreshold slope can be even steeper.) A 6-terminal relay has two sets of source/drain electrodes, *i.e.* it comprises two electrical switches. Since the structure is symmetrical, the two switches exhibit the same on-state current and switching voltages.

The switching gate voltages can be adjusted by applying a non-zero bias to the body electrode ($V_B \neq 0$) [6], since the electrostatic actuation force depends on V_{GB}. A negative body voltage ($V_B < 0$) can lower the gate voltage needed to turn the device on, as shown in Fig. 2.6.

The relay can be operated similarly as an n-channel (NMOS) transistor, to serve as a "pull-down" device, by applying zero or negative body bias ($V_B \leq 0$). Since electrostatic force is ambipolar, the relay also can be turned on by applying $V_{GB} < -10$ V (*e.g.* by setting $V_G = 0$ V and applying $V_B > 10$ V). Thus, a relay can be operated similarly as a p-channel (PMOS) transistor, to serve as a "pull-up" device, by applying a positive body bias ($V_B \geq 0$). This enables complementary logic circuits to be implemented without any extra process steps [7] [8].

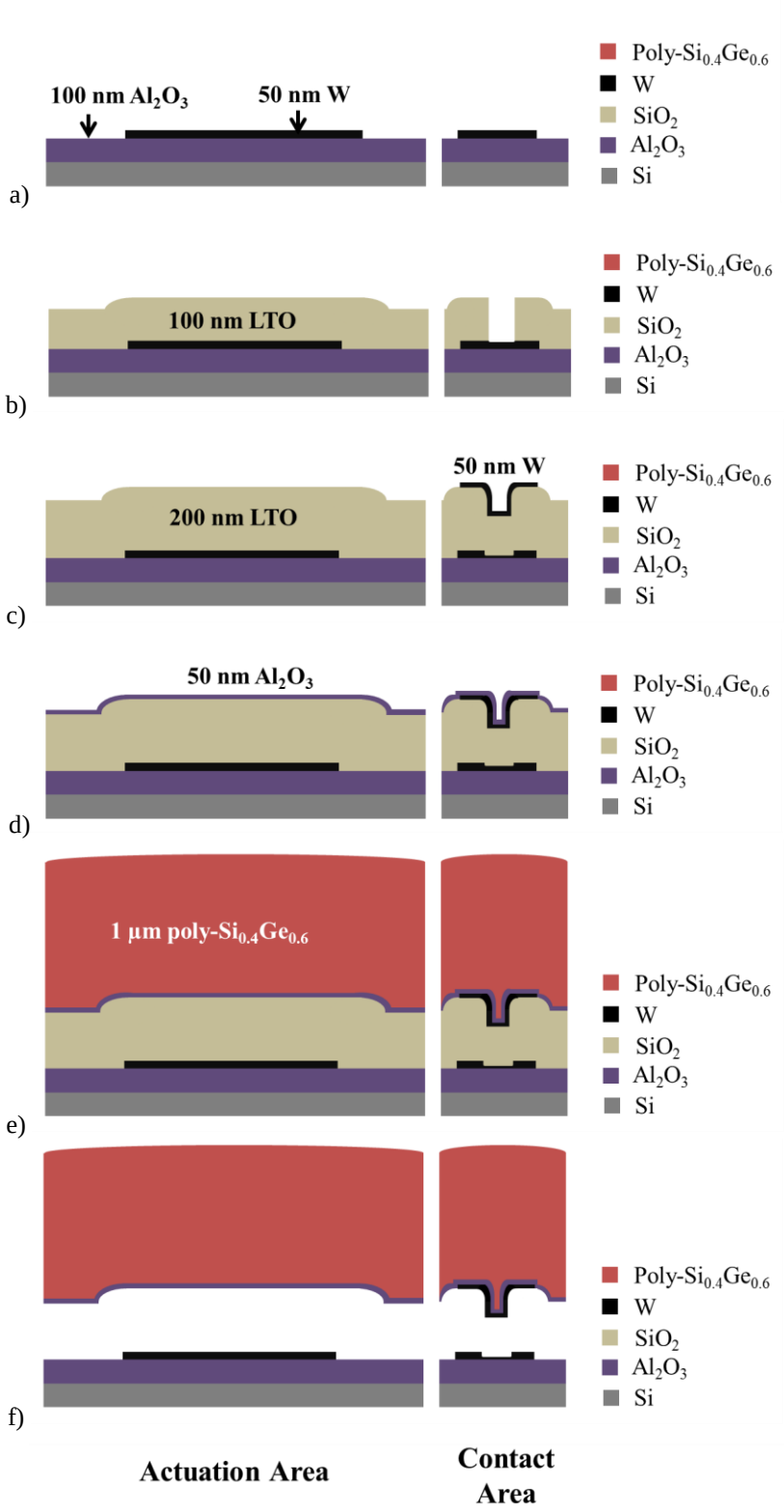

Fig. 2.2 Schematic cross-sections illustrating the relay fabrication process. ((a) Bottom electrodes are formed on Al_2O_3-coated substrate. (b) 1st sacrificial layer deposition and contact definition. (c) 2nd sacrificial layer deposition followed by metal channel deposition and patterning. (d) Al_2O_3 gate oxide deposition. (e) Via patterning (not shown) and poly-$Si_{0.4}Ge_{0.6}$ structure formation. (f) vapor-HF release etch.

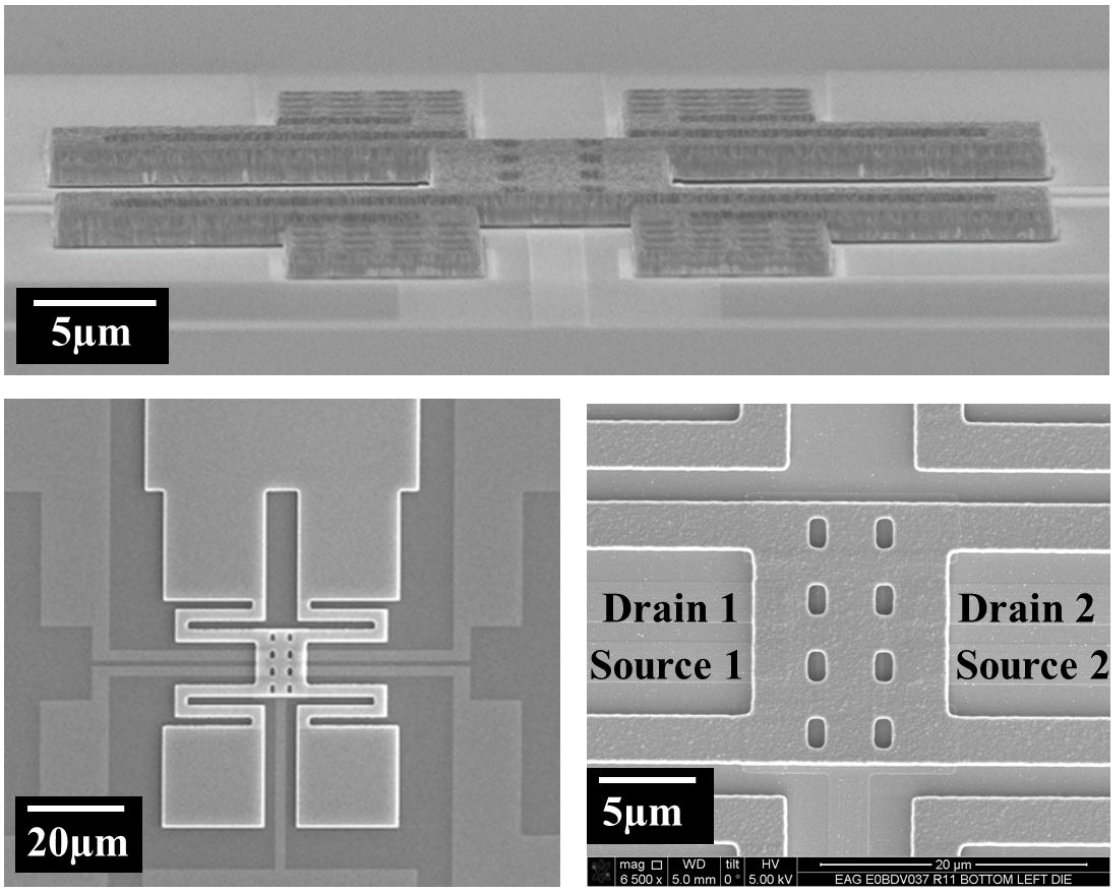

Fig. 2.3 Scanning electron micrographs of a MEM logic relay. Top: Side view. Bottom left: plan view. Bottom right: Zoomed-in plan view with two sets of source/drain electrodes labelled.

As shown in Fig. 2.4, the voltage at which a relay turns off (V_{RL}) is smaller than the voltage at which the relay turns on (V_{PI}), *i.e.* there is hysteresis in the switching characteristic. The hysteresis voltage ($|V_{PI} - V_{RL}|$) sets the lower limit for the relay operating voltage, since the gate voltage swing must be sufficiently large to switch the relay between OFF and ON states. (A body bias voltage can be applied to reduce the gate switching voltages, but the turn-off voltage must be greater than or equal to zero in order for the relay to be OFF at 0 V.)

This prototype device demonstrates that a MEM relay can achieve zero standby power and has abrupt switching behavior so that it can potentially operate with very low voltage. Further work is needed, however, to demonstrate that a relay can be further miniaturized (to have comparable minimum dimension as a transistor) with a hysteresis voltage that is much lower than 1 V (corresponding to V_{DD} for modern CMOS technology). This is necessary in order to achieve superior energy efficiency [9].

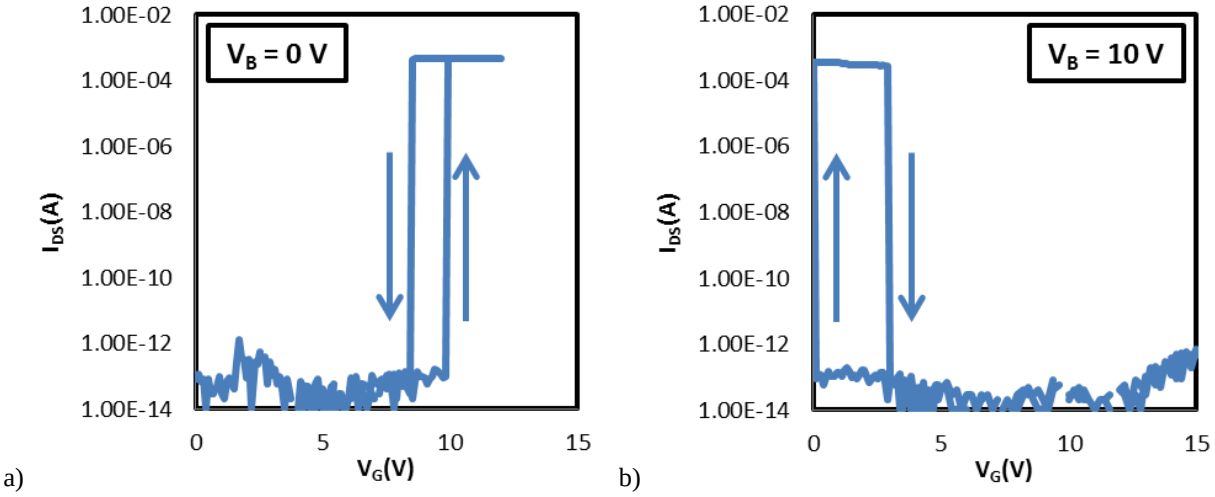

Fig. 2.4 Measured I_{DS}-V_G characteristics of a 6-terminal relay. The off-state current is measured to average around 100 fA, which is limited by the semiconductor parameter analyzer noise level. Relay turn-on and turn-off is observed to be extremely abrupt. (a) MEM relay with V_B = 0 V exhibits "NMOS like" characteristics. (b) MEM relay with V_B = 10 V shows "PMOS like" characteristics (*i.e.* turning on with decreasing V_G and turning off with increasing V_G).

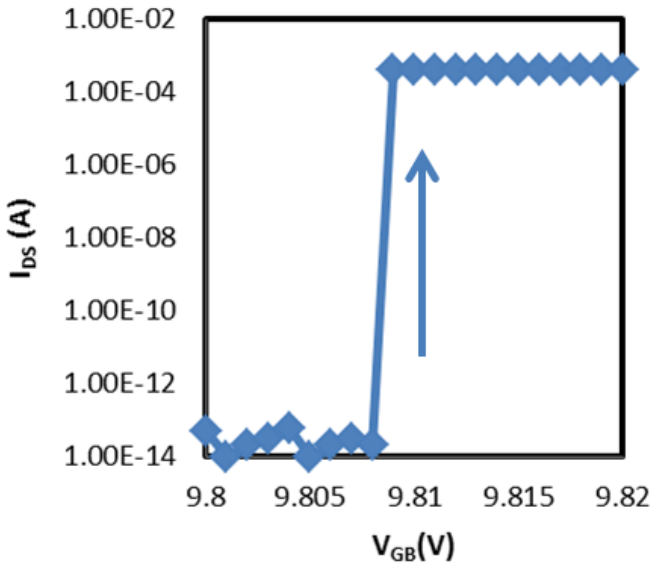

Fig. 2.5 Measured I_{DS}-V_{GB} (for the same device as in Fig. 2.4) showing turn-on abruptness. The relay turns on between 9.808V and 9.809V with 10 orders of magnitude on/off ratio. SS is extracted to be less than 0.1 mV/dec.

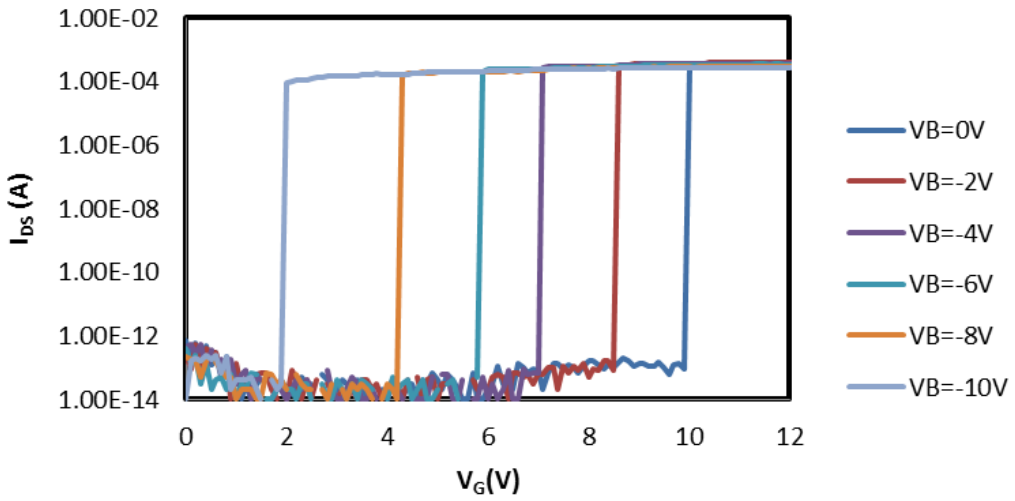

Fig. 2.6 Measured I_{DS}-V_G curves for different body biases. $|V_{GB}|$ at pull-in slightly increases as V_B becomes more negative, most likely due to parasitic capacitance between the gate and the source/drain electrodes.

2.3 MEM Relay Switching Energy

Modeling the switching energy of a relay requires the knowledge of all forces acting on the relay; mainly F_e and F_k. Fortunately, with the folded flexure structure design, the modeling can be relatively simple. A number of assumptions are made in order to simplify the model:

1) The moveable plate is rigid, so the stiffness of the relay only depends on the stiffness of the flexures.

2) F_e only exists between gate and body electrodes, since the gate/body area is significantly larger than the drain/source area.

Under these assumptions, the relay structure can be modelled as a spring attached to a parallel plate shown in Fig. 2.7. The vertical positions are labeled on the right. Without any voltage applied, the moveable plate is suspended by the flexures and would be at z = g. When the relay is pulled down, the dimples will make contact with the bottom electrode and the moveable plate will be at position $z = g - g_d$.

Based on assumptions 1) and 2), F_e of the relay can be modeled as the electrostatic force between conductive parallel plates, which is given by the following equation [10]:

$$F_e = \frac{\varepsilon_o A_{OV} V^2}{2z^2} \tag{2.1}$$

where z is the distance between the parallel plates, ε_o is the permittivity of air, A_{OV} is the parallel plate area and V is the voltage between the plates. F_k can be modeled by Hooke's Law:

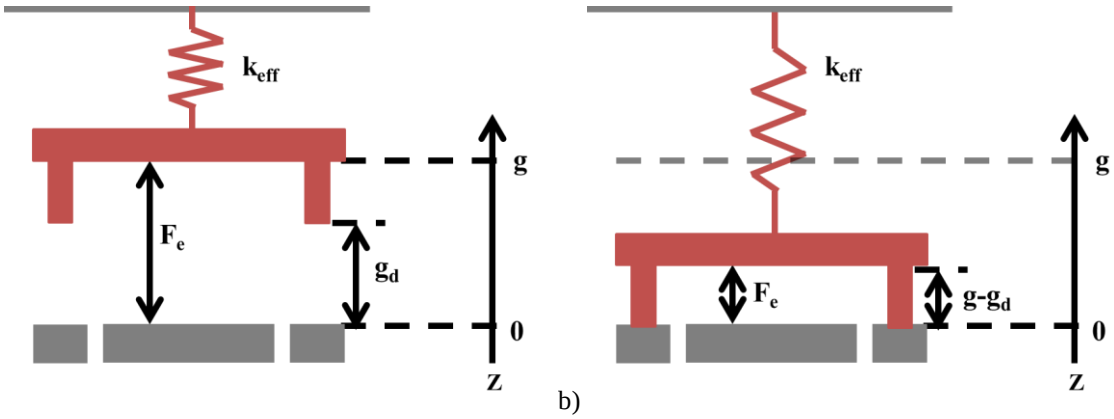

Fig. 2.7 Simplified model of a relay structure. (a) In the off state, the vertical position is at z = g. (b) In the on state, the structure travels a distance of g_d and stops when the dimples make contact; the vertical position of the structure is $z = g - g_d$.

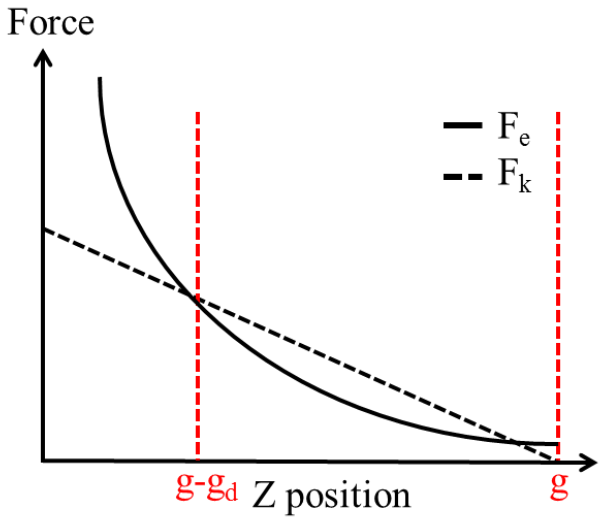

Fig. 2.8 Forces vs. vertical position of a relay in the off state. With $V < V_{PI}$, F_k is always larger than F_e so the air gap cannot be closed.

$$F_k = k_{eff}(g - z) \tag{2.2}$$

where k_{eff} is effective spring constant, dominated by the folded flexures, g - z is the deflection of the springs. To switch the relay from off to on, the electrostatic force needs to be larger than the spring restoring force. Fig. 2.8 shows the forces *vs.* vertical position of a relay. According to the force equations above, F_e has a superlinear relationship (z^{-2}) to distance and F_k has a linear relationship to deflection. If F_e is larger than F_k at a given position, there is a net pull-down force on the relay. However if F_k is larger than F_e, then the relay will experience a net pull-up force.

With $V < V_{PI}$ (Fig. 2.8), the electrostatic force is only sufficient to pull the structure part-way down. But with $V = V_{PI}$ (Fig. 2.9), F_e will be larger than F_k at any given position, so the relay

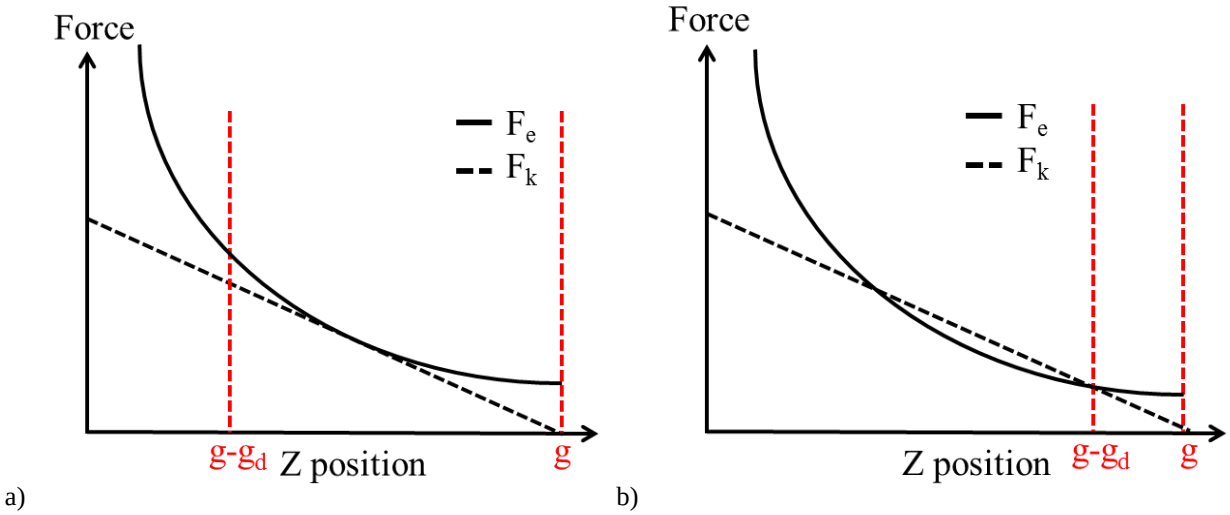

Fig. 2.9 Electrostatic force at V = V_{PI} vs. vertical position in the on state of (a) a relay designed for pull-in-mode operation, *i.e.* large g_d/g ratio, and (b) a relay designed for non-pull-in mode operation, *i.e.* small g_d/g ratio.

will experience a net pull-down force until the dimples come into contact with the source/drain electrodes to turn on the device.

According to Fig. 2.9a, the pull-in voltage is the voltage for which F_e will always be larger than F_k. In this situation, the F_e curve has only one point of intersection with the F_k curve, at z = 1/3 g. The above condition results in the following expression [11]:

$$\frac{\varepsilon_o A_{OV} {V_{PI}}^2}{2(g-z)^2} > k_{eff} z \tag{2.3}$$

$$\frac{\varepsilon_o A_{OV} {V_{PI}}^2}{2k_{eff} g^3} = \frac{z}{g}\left(1-\frac{z}{g}\right)^2 > \frac{4}{27} \tag{2.4}$$

At V = V_{PI}, the left hand side of Equation 2.3 is larger than the right hand side regardless of z. Since the right hand size has a maximum when z = (1/3)g, the pull-in voltage can be solved as:

$$V_{PI} = \sqrt{\frac{8k_{eff} g^3}{27\varepsilon_o A_{OV}}} \tag{2.5}$$

The device turns off once F_k is sufficient to pull the structure away from the bottom electrodes; this condition gives the release voltage as shown below:

$$k_{eff} g_d > \frac{\varepsilon_o A_{OV} {V_{RL}}^2}{2(g-g_d)^2} + F_A \tag{2.6}$$

$$V_{RL} = \sqrt{\frac{2(k_{eff} g_d - F_A)(g-g_d)^2}{\varepsilon_o A_{OV}}} \tag{2.7}$$

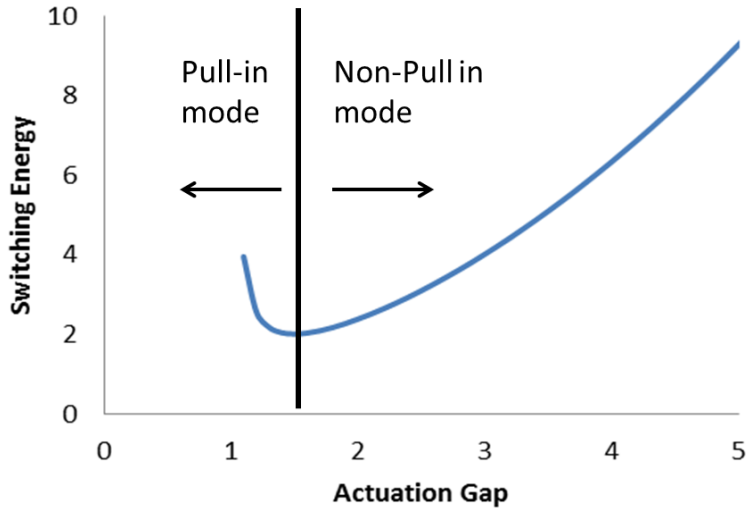

Fig. 2.10 Normalized switching energy vs. normalized (to g_d) actuation gap, assuming a fixed minimum dimple gap limited by the process technology. g_d, A_{OV}, k_{eff} each are set to 1. A minimum at $g/g_d = 3/2$ is observed.

where F_A is the contact adhesive force. It is obvious that the pull-in and release voltages are not the same, resulting in hysteresis. From Equations 2.6 and 2.7, there are two main causes of hysteresis; one is the contact adhesive force, which works against F_k. The other can be seen from Fig. 2.9a: for this relay design, F_e exceeds F_k when the device is on, so the voltage must be lowered further (even without F_A) in order to turn off the device. The hysteresis voltage is a fraction of V_{PI} and can be minimized by reducing g_d to be no greater than g/3. Fig. 2.9b shows the force curve for such a relay design: in the on state, F_e will be equal to F_k, and without F_A this device will have no hysteresis. A relay corresponding to Fig. 2.9a is of the "pull-in mode" design, whereas a relay corresponding to Fig. 2.9b is of the "non-pull-in-mode" design. The voltage at which a non-pull in mode relay turns on is

$$V_{NPI} = \sqrt{\frac{2k_{eff}g_d(g-g_d)^2}{\varepsilon_o A_{OV}}} \tag{2.8}$$

Regardless of the operating mode, the switching energy of a relay based on the earlier assumptions presented is the energy required to charge the structure-to-bottom-electrode parallel plate capacitor, which is the on-state capacitance times the operating voltage squared:

$$E_{PI} = C_{ON}{V_{PI}}^2 = \frac{\varepsilon_o A_{OV}}{(g-g_d)}\left(\sqrt{\frac{8k_{eff}g^3}{27\varepsilon_o A_{OV}}}\right)^2 = \frac{8k_{eff}g^3}{27(g-g_d)} \tag{2.9}$$

$$E_{NPI} = C_{ON}{V_{NPI}}^2 = \frac{\varepsilon_o A_{OV}}{(g-g_d)}\left(\sqrt{\frac{2k_{eff}g_d(g-g_d)^2}{\varepsilon_o A_{OV}}}\right)^2 = 2k_{eff}g_d(g-g_d) \tag{2.10}$$

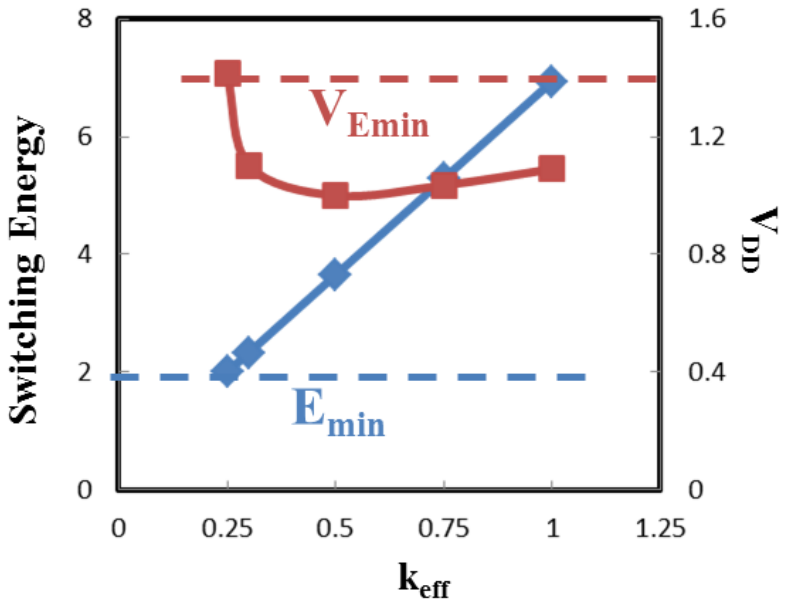

Fig. 2.11 Switching energy (blue diamonds) and minimum operating voltage (red squares) *vs.* k_{eff} for an applied body bias of $-V_{RL}$. E_{min} is the minimum switching energy allowed by F_A. V_{Emin} is defined to be V_{DD} for $E = E_{min}$.

From the equation above it can be seen that in order to minimize the switching energy, one should lower the spring constant and minimize the actuation gap: lowering the spring constant would decrease F_e needed to turn the device on; reducing the actuation gap would decrease the voltage needed to create the same F_e. Relay switching energy scaling is ultimately limited by the contact adhesive force which sets the minimum F_k required to turn the device off, which in turn sets the minimum F_e needed to turn the device on. Given this F_A constraint, the minimum switching energy is derived below [12]:

$$k_{eff} g_d > F_A \tag{2.11}$$

$$E_{PI,MIN} = \frac{8k_{eff}g^3}{27(g-g_d)} = \frac{8F_A g^3}{27 g_d (g-g_d)} \tag{2.12}$$

$$E_{NPI,MIN} = 2F_A(g - g_d) \tag{2.13}$$

The optimal operation mode for a relay can be identified from Fig. 2.10; F_A and g_d values are assumed to be limited by the process technology and physics. The curve shows that there is a minimum energy for a relay operating in the pull-in mode at $g_d = (2/3)g$, which corresponds to pull-in-mode operation. This is mainly because there is a trade-off between on-state capacitance and voltage: as the actuation gap increases the on-state capacitance decreases but the actuation voltage increases, and *vice versa* [13].

It was mentioned above that a body bias voltage can be used to adjust the gate switching voltages, which can also reduce V_{DD} for a MEM relay. With body bias applied, V_{DD} can be reduced to the hysteresis voltage of the relay. The switching energy can be calculated by

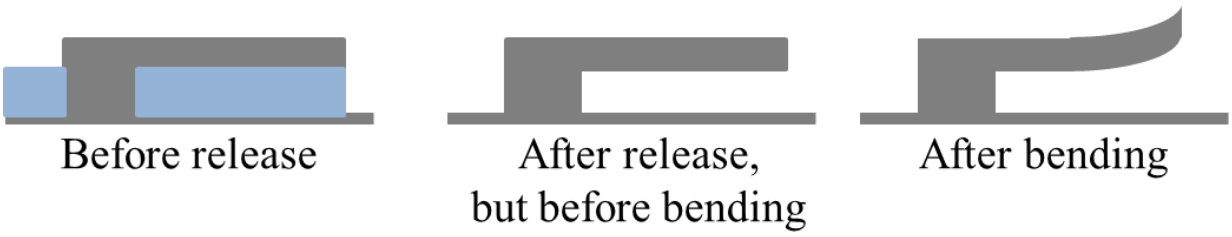

Fig. 2.12 Cantilever with a stress gradient before and after release. After release but before bending is a hypothetical intermediate state to illustrate how residual stress is released to cause out-of-plane deflection. (Adapted from [10]).

subtracting the energy stored in the capacitor in the OFF state from the energy stored in the ON state, assuming $V_B = -V_{RL}$:

$$C_{ON}{V_{PI}}^2 - C_{OFF}{V_{RL}}^2 = \frac{8k_{eff}g^3}{27(g-g_d)} - \frac{\varepsilon_o A_{OV}}{(g-g_{off})}{V_{RL}}^2 \tag{2.14}$$

Note that

$$\frac{\varepsilon_o A_{OV}{V_{RL}}^2}{2(g-g_{off})^2} = k_{eff}g_{off} \tag{2.15}$$

where g_{off} is the amount of deflection in the off state. The switching energy and minimum operating voltage $V_{DD} = V_{PI} - V_{RL}$ for a pull-in-mode relay with an applied body bias $V_B = -V_{RL}$ are plotted as a function of k_{eff} in Fig. 2.11. Although V_{DD} is not minimized at minimum k_{eff}, the switching energy is still minimized at minimum k_{eff}. This indicates that, although body biasing can provide for lower V_{DD}, it is more important to lower k_{eff}, *i.e.* make the relay structure as compliant as allowed by F_A, to achieve the minimum switching energy.

2.4 Key Challenges for Reducing Relay Switching Energy

From the switching energy expression derived in the previous section, a number of technological challenges can be identified:

1) F_A scaling: In order for the relay to turn off, F_k must be larger than F_A. For the device to turn on F_k has to be overcome by F_e, which determines V_{PI} and switching energy. As a result, the minimum switching energy of a normally-off relay ultimately is limited by F_A. To study the origin and scalability of F_A is extremely important.

2) It is desirable to create relays with low structural stiffness (k_{eff}), to lower the energy needed to turn the device on. For example the main reason the prototype relay has high operating voltage (ref. Fig. 2.4) is because the structure is too stiff. One can easily make a relay softer by making the suspension beams longer, but this increases the device footprint which is not desirable from a chip cost standpoint. It is preferable to scale down the structural layer thickness. Out-of-plane bending due to non-zero stress gradient (Fig.

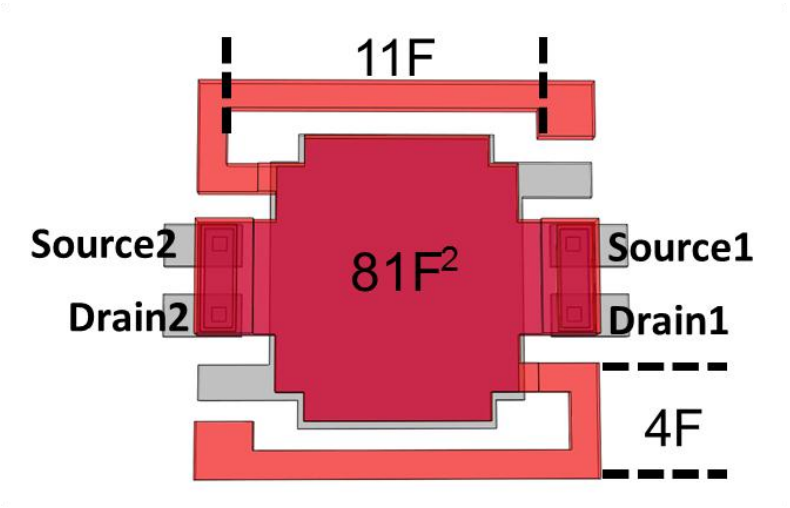

Fig. 2.13 Plan-view schematic of a 6-terminal relay design comprising two folded suspension beams. F is the minimum feature size, which is also the contact dimple width.

	NEM Relay			CMOS
Technology Node (nm)	**15**	**11**	**8**	**8.4**
Actuation Gap (nm)	**5.5**	**4**	**3**	**N/A**
Pull-in Voltage (mV)	**113**	**100**	**86**	**610**
Switching Energy (aJ)	**1.1**	**0.6**	**0.3**	**1.28**

Table 2.1 Relay technology scaling projections compared against 8 nm CMOS technology [18].

2.12) in polycrystalline films worsens with decreasing thickness, however. Thin-film process refinements are needed to mitigate this issue.

3) The actuation and contact dimple gaps should be as small as possible, and generally are limited by the sacrificial material deposition and selective etch (for structural release) process capabilities. It is desirable to have a conformal deposition process that can uniformly deposit films of thickness below 5 nm, and a release process than can have etchants undercut the structure and create nanometer-scale air gaps. Previous work on nanogap formation shows that, a gap of 3 nm can be successfully released using vapor-HF; however, a deposition process more uniform than LPCVD SiO_2 is desired.

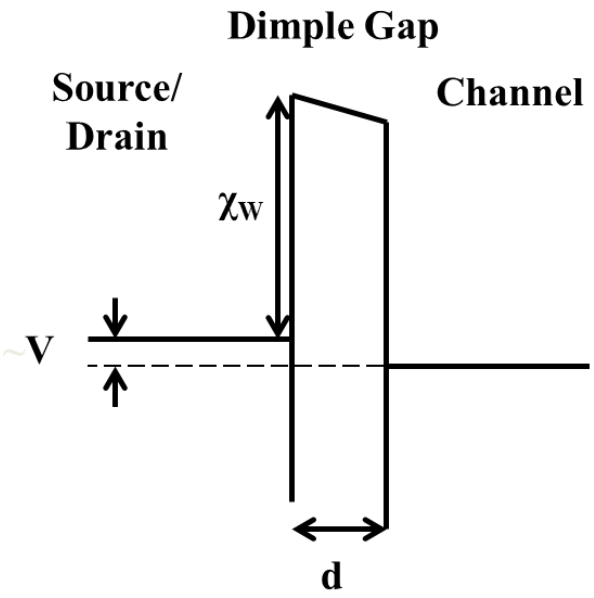

Fig. 2.14 Energy band diagram of a metal-insulator-metal tunnelling junction with an applied bias of V. The insulator is an air gap and the barrier height is the work function (χ_W) of the contact metal.

2.5 Switching Energy Projection of Ultimately Scaled Relays

Using the model developed in Section 2.3, projections of switching energy can be made for ultimately scaled relay technology for comparison against CMOS technology. Fig. 2.13 shows the layout of the NEM relay structure studied herein, which comprises two folded-flexure suspension beams to reduce the spring stiffness. The technology node is defined by the smallest lithographically defined dimension, *i.e.* the dimple contact width. The switching energy is estimated by using FEM simulation tool Coventorware™ [14] to determine V_{PI} and to calculate the on-state capacitance.

Table 2.1 shows the projection for ultimately scaled relays at various technology nodes, compared with the switching energy of a comparably scaled CMOS technology according to the latest ITRS predictions [15]. It shows that the active switching energy of a relay can be competitive, if the contact adhesive force is negligible. In order to discover the energy efficiency limit of an ultimately scaled NEM relay, surface adhesion in nano-scale contacts must be investigated.

2.6 Noise Considerations for Ultimately Scaled NEM Relays

Due to the nature of mechanical devices having air gaps and moving structures, there are concerns that a relay would be affected by noise, either due to tunneling current, gravitational force or thermal vibration, especially for relays with nanometer-scale gaps. These concerns are addressed in this section.

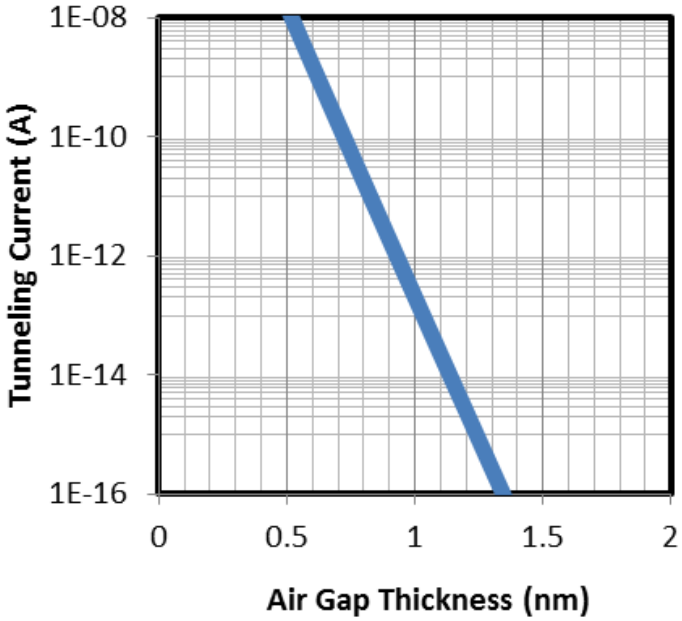

Fig. 2.15 Direct tunnelling current vs. air gap thickness for an 8nm x 8nm contact dimple with a contact voltage of 100 mV. For off-state leakage current to be less than 10 fA, g_d should be larger than 1.1 nm.

2.6.1 Direct Tunneling Through the Contact Gap

The greatest advantage of a MEM relay is that there is negligible current flow through the air gap in the OFF state. However this may no longer be true for extremely scaled relays, since significant direct tunneling can occur across a nanometer-scale gap with sufficient applied voltage across the gap.

Tunneling current of a metal-insulator-metal junction is well studied and estimated based on the model illustrated in Fig. 2.14. The two flat contact metal surfaces are separated by air, mimicking a mechanical contact. The direct tunneling current density is given by [16] [17]:

$$J = J_o\{\varphi \exp\left(-A\varphi^{\frac{1}{2}}\right) - (\varphi + eV)\exp(-A(\varphi + eV)^{\frac{1}{2}} \tag{2.16}$$

$$J_o = \frac{e}{2\pi h(\beta d)^2} \tag{2.17}$$

$$A = \frac{4\pi\beta d}{h(2m)^{\frac{1}{2}}} \tag{2.18}$$

where m is the electron mass, h is the Plank's constant, φ is the mean barrier height, V is the voltage applied and β is a correction factor (~1). The calculated direct tunneling current is

shown in Fig. 2.15 for an 8 nm wide contact, assuming 100 mV is applied across the tunnel junction according to the ultimately scaled relay predictions (V_{PI} = 86 mV) and barrier height according to the Tungsten work function [18]. It can be seen that, to limit the off-state leakage below 10 fA for an ultimately scaled NEM relay, the contact gap has to be larger than 1.1 nm.

2.6.2 Gravitational and Acceleration Forces

It is a common concern that a NEM relay would accidentally turn on if the device is dropped to the ground or it is experiencing acceleration. However due to the extremely low structural mass, the amount of deflection caused by gravitational force is extremely small. The calculated result of an ultimately scaled 8 nm relay is shown below [19]:

$$z_{gravity} = \frac{mg}{k_{eff}} = \frac{1.03\times10^{-18}N}{0.0435\frac{N}{m}} \approx 23 \times 10^{-18}m \tag{2.19}$$

Using a similar calculation, it can be shown that the acceleration required to turn the relay on is extremely large:

$$a = \frac{k_{eff}g_d}{m_{eff}} = \frac{8.7\times10^{-11}N}{10^{-19}kg} = 8.7 \times 10^{8}\,\frac{m}{s^2} \approx 8.8 \times 10^{7}G \tag{2.20}$$

As a result, NEM relays should not be effected by gravitational and acceleration forces.

2.6.3 Thermal Vibrations

Even at room temperature, there is concern that there can be enough thermal energy to create thermal vibrations and would turn a scaled relay on, especially with an ultimately scaled contact gap. Assuming a scaled 8nm NEM relay at room temperature, the amount of deflection can be approximated as the following calculation:

$$z_{thermal} = \sqrt{\frac{kT}{k_{eff}}} \approx 3.4 \times 10^{-10}m \tag{2.21}$$

which is much smaller than the minimum contact gap. Therefore, thermal vibrations should not be an issue in the operating temperature range of interest.

2.7 Summary

A scaled relay technology shows promise for ultra-low power digital logic applications. Proof-of-concept prototype devices exhibit ideal switching properties such as zero off-state leakage current and nearly infinite local subthreshold slope, which potentially can provide for extremely low operating voltage. However, due to a relatively large device footprint and pull-in voltage (V_{PI}), the active switching energy is significantly larger than for a CMOS transistor. Moreover, hysteresis is observed due to contact adhesive force (F_A), resulting in finite effective subthreshold slope and limiting the minimum operating voltage. Scaling is needed to minimize the switching energy as well as the operating voltage.

The switching energy of a relay is dominated by the energy required to charge and discharge the parallel plate (or gate to body) capacitor. The simple model derived herein shows that the key to minimizing the switching energy is to reduce g and k_{eff}, where the minimum g possible is limited by fabrication process capabilities and the minimum k_{eff} possible is limited by F_A. It is shown by FEM simulations that ultimately scaled NEM relays potentially can have switching energy less than 1 aJ, assuming that F_A is negligible. The following chapters will focus on understanding the source of F_A, and process technology development to enable k_{eff} reductions, in order to realize the sub-aJ switching energy projected by FEM simulations.

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Chapter 3

Study of Contact Adhesive Force

3.1 Introduction

The adhesive force between contacting surfaces in the on state determines the minimum spring restoring force required for the relay to turn off in the absence of an applied electrostatic force. In turn, the spring restoring force determines the minimum electrostatic force and hence the minimum applied voltage required to turn on the relay. As a result, the minimum energy required to operate a relay is set by the contact adhesive force, which can depend on various factors such as the contact material, area and surface properties (which can depend on the device operating conditions) [1].

In this chapter, contact adhesive force in prototype MEM relays is investigated. Firstly, common causes of adhesion are discussed in Section 3.2. Then, experimental results for prototype relays with different contact dimple areas are presented in Section 3.3. Theoretical predictions of contact adhesive force are presented in Section 3.4, followed by projections of relay switching energy accounting for contact adhesive force in Section 3.5. Experimental investigations of surface coatings to mitigate adhesion are presented in Section 3.6.

3.2 Common Sources of Adhesion

It is important to identify the primary source(s) of contact adhesion so that appropriate measures can be taken to mitigate it. The most common sources of adhesion in micro-electro-mechanical devices include capillary force, van der Waals force, and bonding [2]. The mechanism which is dominant will depend on the contacting surface properties and device operating conditions.

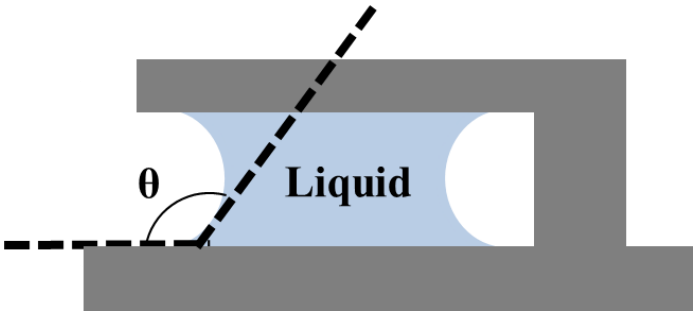


Fig. 3.1 Schematic illustration of capillary force due to liquid condensation during a wet release process. The contact angle between the liquid and the contact surface is θ, and the surface is assumed to be hydrophilic in this diagram.

3.2.1 Capillary Force

To form the actuation and contact air gaps in a relay, a sacrificial material such as SiO_2 is selectively removed from the regions between the actuation electrode and the structure, and between the contacting electrodes [3]. SiO_2 is commonly removed using a liquid hydrofluoric acid (HF) etchant. The exposed surfaces can be hydrophilic, such that a strong capillary force develops when the structure is pulled out from the liquid (either the etchant or a subsequent water rinse bath). The capillary pressure between surfaces created in this situation is given by the following equation [4] [5]:

$$P_L = \frac{2\gamma_l cos\theta}{d} \tag{3.1}$$

where γ_l is the surface tension, d is the separation between two surfaces and θ is the contact angle between the liquid and the solid surface. If the surface is hydrophilic, *i.e.* $\theta < 90^o$, there will be a strong attractive capillary force between the two surfaces. An illustration is shown in Fig. 3.1.

There are alternative techniques to release micro-mechanical structures without using a wet HF etch. For example, vapor-phase HF can be used. Although it has a slower etch rate, it allows devices to be released without immersion in liquid, to mitigate stiction.

Even with a dry release etch process there can still be capillary forces, *e.g.* during device operation. Water vapor can condense into small cracks and pores creating capillary force, a phenomenon called capillary condensation. The capillary condensation force is given by the following equation [1]:

$$F = \frac{2\gamma_l d_0 cos\theta}{d^2} \tag{3.2}$$

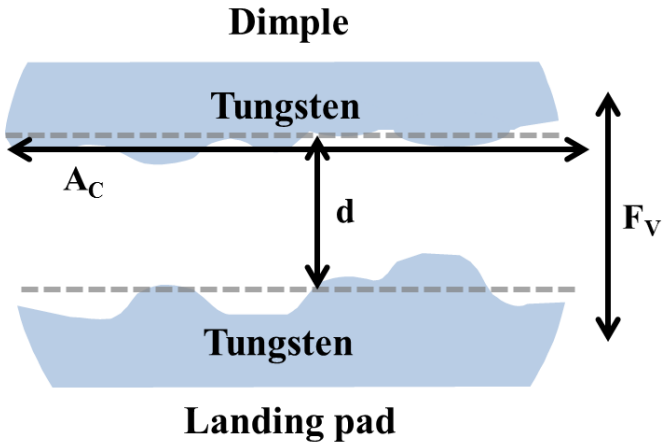


Fig. 3.2 Illustration of van der Waals force between surfaces.

$$d_0 = \frac{2\gamma_l v cos\theta}{RT \log(\frac{P}{Psat})} \tag{3.3}$$

where R is the Bozeman constant, T is absolute temperature; P/P^{sat} is the relative humidity. Capillary condensation can be minimized or eliminated by hermetically sealed packaging.

3.2.2 van der Waals Force

Van der Waals force is an attractive force originating from interactions between instantaneous dipole moments of atoms. Assuming two parallel flat surfaces, the van der Waals force can be modeled by the following equation [5]:

$$F_V = \frac{HA_c}{6\pi d^3} \tag{3.4}$$

where H is the Hamaker constant, d is the distance between the two surfaces and A_C is the contact area. d cannot be infinitesimally small, due to repulsion between surfaces in extremely close contact; the minimal distance is typically in the range from 0.2 nm to 0.7 nm [6]. An illustration of van der Waals force between surfaces is shown in Fig. 3.2.

Equation 3.4 assumes that the separation between surfaces is smaller than the characteristic length (z_0) of approximately 20 nm. If the separation is larger than this, the van der Waals force is retarded and can be more accurately modeled by the following equation [7]:

$$F_V = \frac{HA_c}{6\pi d^3} \frac{z_0}{(d+z_0)} \tag{3.5}$$

Ideally the contact gap of a micro/nanometer-scale relay should be less than 20 nm; hence Equation 3.4 is relevant. If the van der Waals force dominates the force of adhesion (F_A), then it should scale down with the contact area.

3.2.3 Hydrogen Bonding

Surface hydroxyl groups can form strong hydrogen bonds when the separation between surfaces is very small [8], *i.e.* when the surfaces are in contact. The strength of the hydrogen bond is between 10 and 40 mJ/mol.

Due to surface roughness, the actual area of physical contact can be significantly smaller than the area of the dimpled contact region. If the contact dimple area is much larger than an asperity, then physical contact is made only at a few asperities and F_A should be relatively independent of the dimple area. If the dimple area is smaller than an asperity, then F_A should scale with the dimple area.

3.3 Characterization of Relay Contact Adhesion

Contact area and surface properties are major factors for adhesive force [9]; relays with contact dimple width ranging from 100 nm to 1.3 μm are characterized herein to investigate the dependence of F_A on dimple area, to identify the primary source of adhesion and to allow for more accurate prediction of scaled relay switching energy accounting for contact adhesion.

3.3.1 Experiment

Relays of various contact sizes were fabricated to investigate contact adhesive force, using the same process flow as described in Section 2.2.2, but with drawn contact dimple width in the range from 100 nm to 1 μm. During the contact dimple lithography process, larger features were overexposed in order to ensure that the minimum-sized feature sizes were printed. As a result, the fabricated devices have contact dimple widths in the range from 100 nm to 1.3 μm, as measured by atomic force microscopy (AFM). Scanning electron microscopy (SEM) images of a fabricated relay with 100 nm contact dimple width, in plan view and in cross section, are shown in Fig. 3.3.

3.3.2 Adhesive Force Extraction from Electrical Measurements

The pull-in voltage (V_{PI}) is the voltage at which the electrostatic force overcomes the spring restoring force, so the spring restoring force can be determined from the measured value of V_{PI}. The release voltage (V_{RL}) is the voltage at which the electrostatic force is equal to the spring restoring force minus the contact adhesive force (F_A). Therefore, F_A can be derived from the values of V_{PI} and V_{RL} as follows [10]:

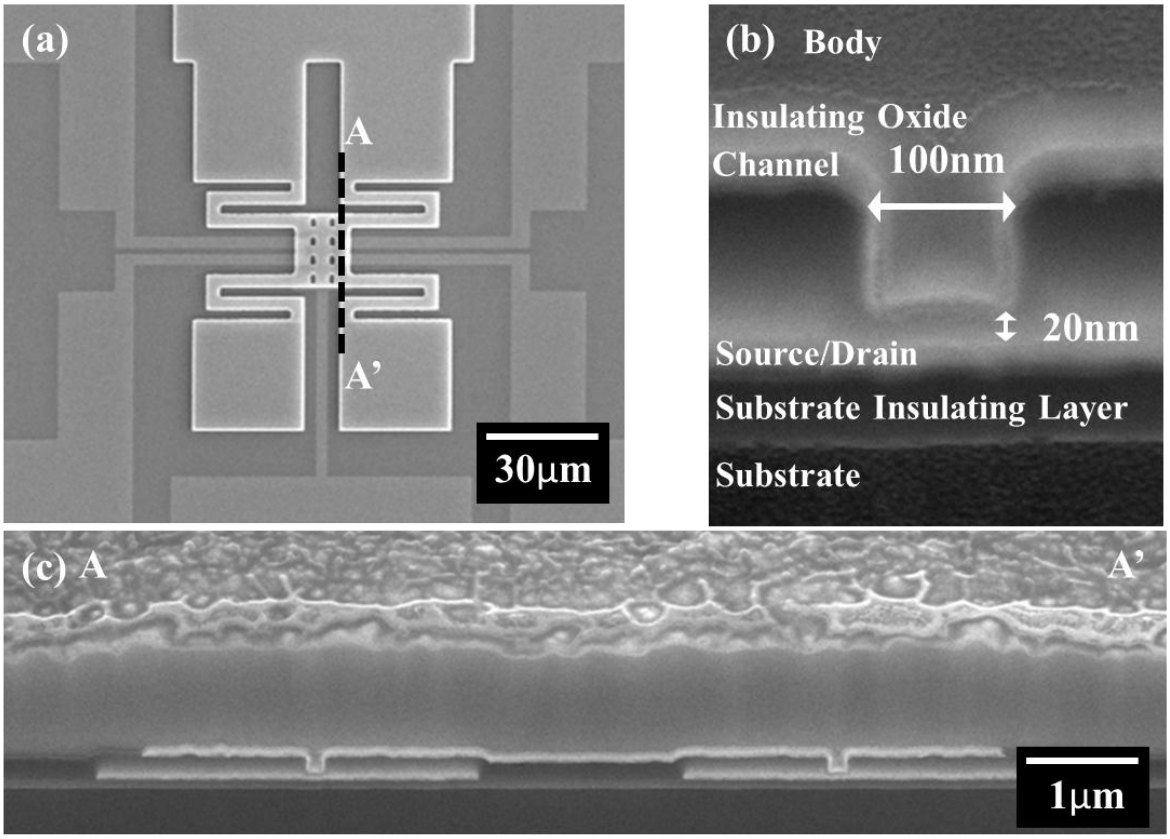


Fig. 3.3 SEM images of a MEM logic relay with ultra-small contact dimples: (a) plan view, (b) cross-sectional view of contact dimple region, (c) cross sectional view through the channel region.

$$V_{PI} = \sqrt{\frac{8k_{eff}g^3}{27\varepsilon_0 A_{OV}}} \tag{3.6}$$

$$V_{RL} = \sqrt{\frac{2(k_{eff}g_d - F_A)(g-g_d)^2}{\varepsilon_0 A_{OV}}} \tag{3.7}$$

$$F_A = \frac{27\varepsilon_o A_{OV} g_d}{8g^3} {V_{PI}}^2 - \frac{\varepsilon_o A_{OV}}{2(g-g_d)^2} {V_{RL}}^2 \tag{3.8}$$

3.3.3 Observations of Fabricated Relays

From Equation 3.8 it can be seen that in order to determine F_A, the values of the as-fabricated actuation gap (g), contact gap (g_d) and actuation area (A_{OV}) are needed. A_{OV} is found to be approximately the same as designed. Ideally, g_d and g should be determined by the thicknesses of the sacrificial layers formed during the device fabrication process. However, this is not the case due to the effects of 1) non-conformal thin-film deposition within the contact dimple region, causing g_d to be smaller than designed; and 2) non-zero strain gradient within the structural

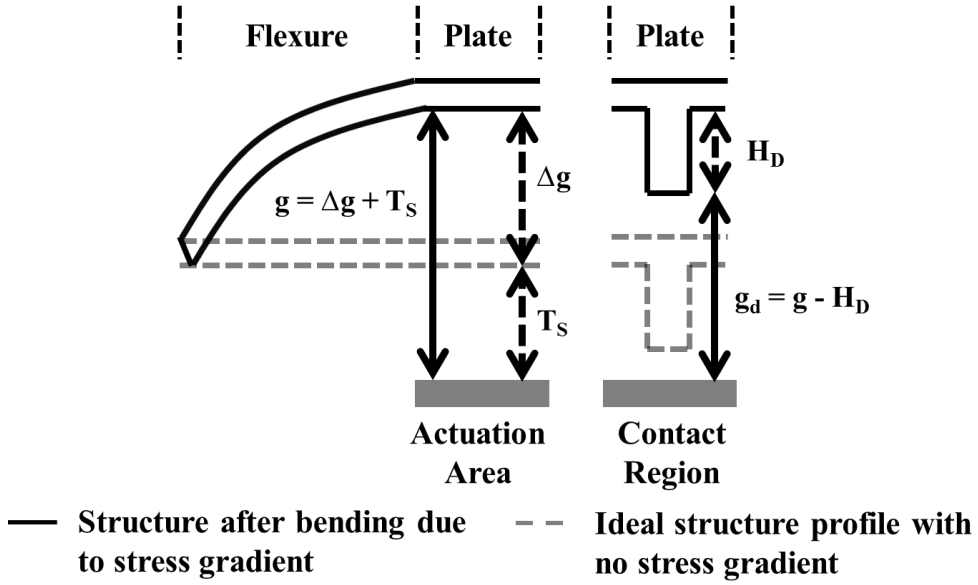


Fig. 3.4 Schematic cross-sections showing how g and g_d change due to a negative strain gradient within the structural layer causing the released structure to bend out of plane (primarily in the more compliant folded-flexure suspension beam regions) and increase g and g_d by the amount Δg.

material that results in out-of-plane deflection which increases both g and g_d [11] as illustrated in Fig. 3.4.

In order to accurately determine the values of g and g_d, the relay structures were carefully lifted off the substrate using conductive carbon tape, and an AFM was used to measure the actual dimple height (H_D), which is the difference between g and g_d. Fig. 3.5 shows the AFM scan of a 1 μm-wide dimple and a 100 nm-wide dimple, where the dimple height is measured. It can been seen from these measurements that the dimple height increases as the dimple width decreases, due to poor conformality of the LPCVD process used to deposit the sacrificial SiO_2 layers.

The amount of out-of-plane deflection (Δg) of the relay structure can be determined from a surface map taken using an optical interferometry tool. An example is shown in Fig. 3.6. It is observed that the structure has a concave downward shape due to a negative strain gradient, with most of the out-of-plane deflection occurring along the folded-flexure suspension beams. The vertical deflection increases both g and g_d, and is measured by comparing the vertical positions at the two ends of a folded-flexure beam. It is found that the deflection ranges from 100 nm to 200 nm, depending on the flexure beam length. Given these extracted values, the actual g and g_d can be estimated as follows:

$$g = T_S + \Delta g \tag{3.9}$$

$$g_d = g - H_D = T_S + \Delta g - H_D \tag{3.10}$$

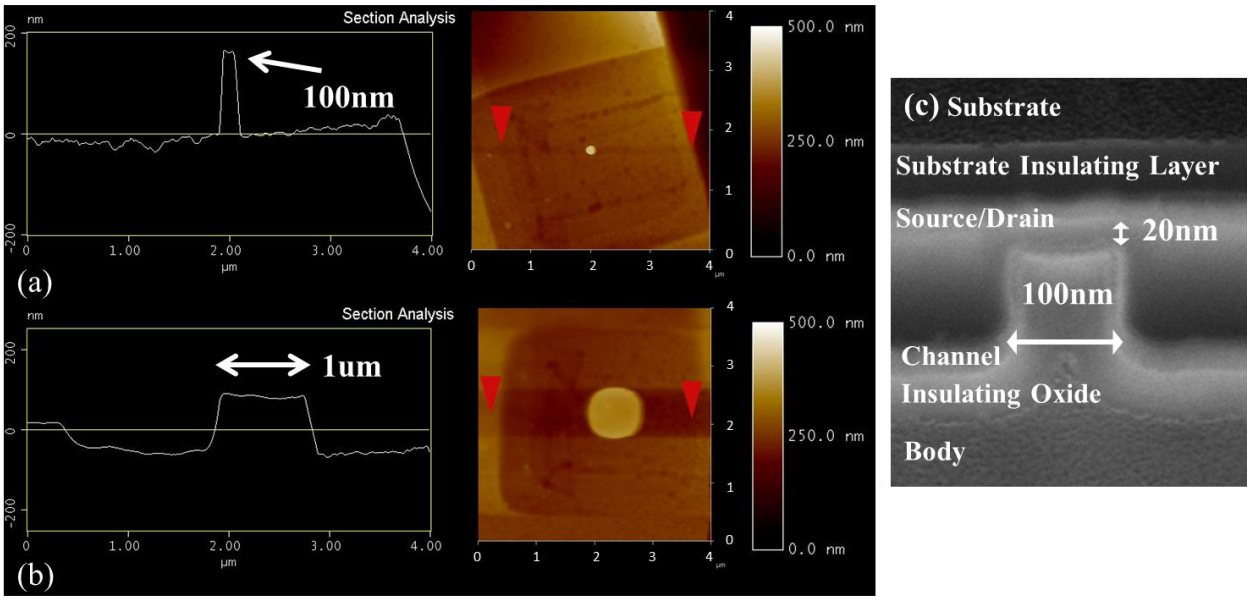


Fig. 3.5 (a) AFM scan of a 100 nm-wide contact dimple (upside down). (b) AFM scan of a 1 μm-wide dimple (upside down). (c) SEM cross section of a contact dimple for reference (shown upside-down as compared to Fig. 3.3b). Due to poor conformality of the LPCVD process, the 2nd sacrificial LTO layer is thinner in the contact region, so that the as-fabricated dimple gap (g_d) is smaller.

where T_s is the total thickness of the sacrificial SiO_2 layers. Since the actual values of g and g_d depend on the lengths of the folded flexures and the contact dimples, g and g_d was measured for each relay design.

3.3.4 Electrical Measurement Results

Fig 3.7 shows measured values of V_{PI} and V_{RL} for relays of various contact dimple areas [12]. The data shown is for a set of relay devices that have the same structure and gap dimensions with contact dimple width as the only design variation. V_{PI} is approximately the same for all of the devices, confirming that they have the same structure.

The difference between V_{PI} and V_{RL} is the hysteresis voltage. It is observed that the hysteresis is roughly the same for relays with large contact dimples, and that the hysteresis is dramatically lower for the relays with the smallest contact dimples suggesting a significant reduction in F_A.

The adhesive force extracted using the method described in Section 3.3.3 is shown in Fig. 3.8. For each value of contact dimple area, roughly 15 devices were measured. The larger contact dimples have contact adhesive force of roughly 4 μN, almost independent of dimple size. The smallest contact dimple has significantly lower contact adhesive force, ~ 0.7 μN. To explain these experiment results, theoretical modeling is necessary.

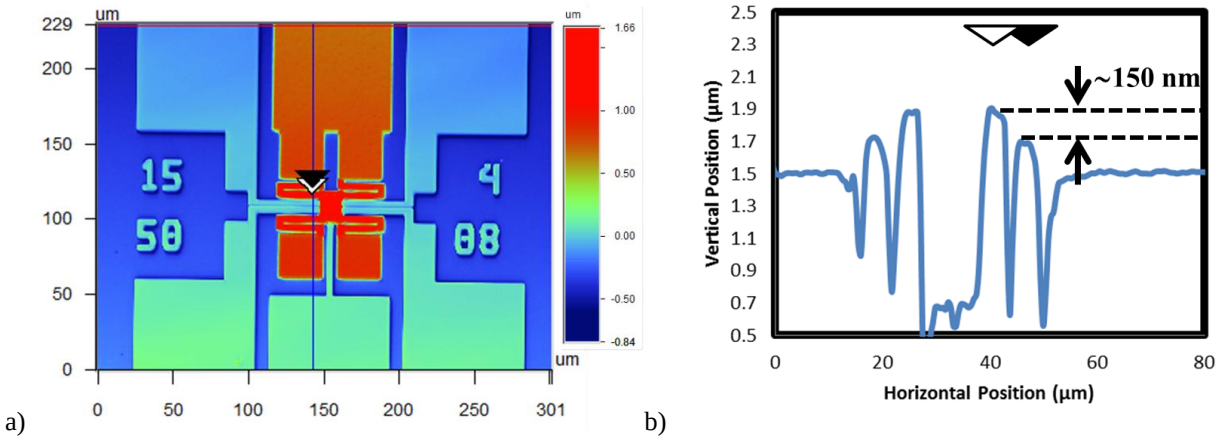


Fig. 3.6 a) Surface topology of a MEM relay, obtained by optical interferometry. The out-of-plane deflection is extracted from the height difference between the flexure ends near the anchor and near the center plate. b) 1-D cutline profile showing an extracted out-of-plane deflection of 150 nm.

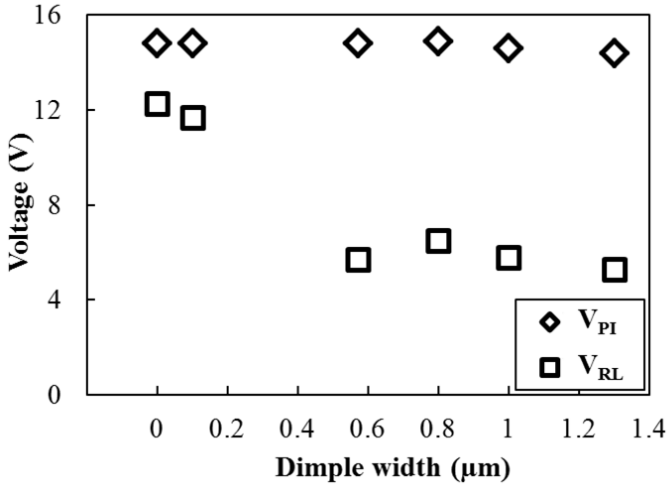


Fig. 3.7 Measured pull-in and release voltages of MEM logic relays of various contact dimple sizes. Theoretical values for the case of zero adhesive force are shown for "0" dimple width, for reference. (Note that the hysteresis voltage in this case is due purely to pull-in mode operation.)

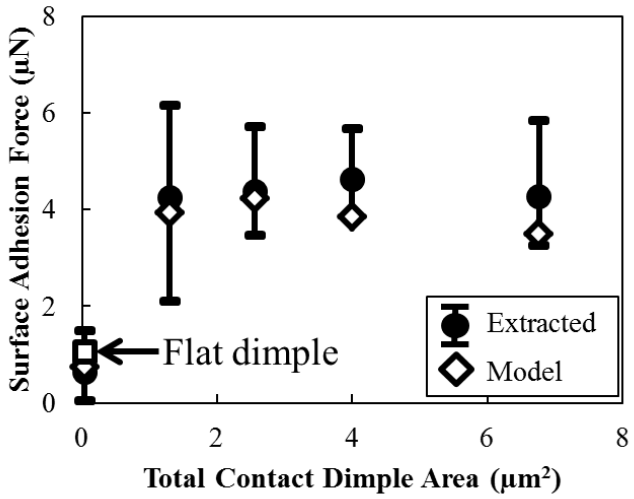


Fig. 3.8 Extracted F_A vs. total contact dimple area. Modeling results assuming 1.5 nm dimple surface roughness are indicated with diamond symbols. Also shown is the modeling result for the case of a flat (non-curved) contact dimple surface.

3.4 Modeling of Relay Contact Adhesion

As mentioned in Section 3.2, the three most commonly observed sources of adhesion are capillary force, van der Waals force, and bonding. For a rough surface, contact is only made at a few asperities; the number of asperities that are in contact should be almost independent of the contact dimple area [13]. Given that bonds can only be made at the contacting asperities, F_A should be the same for all contact sizes if bonding were the dominant source of adhesion. Also, the relays in this work are operated in a nitrogen-purged environment, and hence should not suffer from stiction [14].

To estimate F_A due to capillary condensation, the surface profile must be investigated. From Fig. 3.5 it is observed that the contact dimple surface is curved instead of flat, due to non-conformality of the LPCVD SiO_2 process, illustrated in Fig. 3.9. Hence, only the perimeter of the dimple is in contact with the bottom electrode. From Equations 3.2 and 3.3, it can be estimated that capillary condensation is only significant when the distance between surfaces is less than 2 nm. Moreover, if capillary condensation were the dominant source of adhesion, F_A should be proportional to the contact dimple perimeter length, and hence show a linear dependence on contact dimple size, which is not seen in Fig. 3.8. The calculated value of capillary condensation force is not significant (< 0.1 μN) compared to the observed F_A. With neither bonding nor capillary force likely to be dominant, van der Waals force is the most likely dominant source of adhesion.

Equation 3.4 can be used to estimate the adhesive force between tungsten surfaces. However, one must be careful to consider the non-planar topography and roughness of the contact dimple surface.

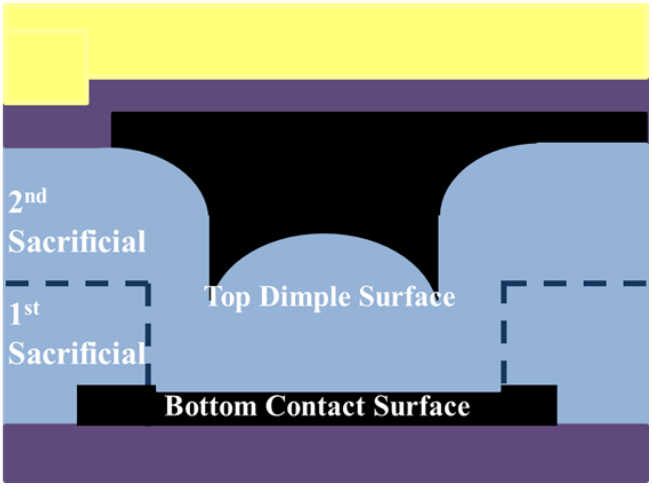


Fig. 3.9 Schematic cross section of a contact dimple. Due to poor conformality of deposition, the 2nd sacrificial LTO results in a curved dimple surface.

As shown in Fig. 3.9, the dimple surface is concave due to a non-conformal sacrificial-LTO deposition process. In contrast, the surface of the bottom electrode (which is contacted by the dimple when the relay is in the on state) is roughly planar. The van der Waals force at any location along the contact dimple surface is dependent on its separation from the bottom electrode surface, which depends on the curvature of the contact dimple surface as well as the surface roughness:

$$F_V = \int_{A_C} \frac{HdA}{6\pi(d_{loc}(x,y)+d_{rms})^3} \tag{3.11}$$

where d_{rms} is an equivalent root mean square (rms) roughness of the two contacting surfaces [15] and d_{loc} is the local distance between the two contacting surfaces due to the curved shape. The Hamaker constant used for tungsten is 40×10^{-20} J [16]. The roughness of the bottom electrode is measured by AFM. Since it is very difficult to measure the roughness of the contact dimple, estimations are made based on typical measured rms surface roughness of the 2nd sacrificial layer (SiO_2). The modeled contact geometry is shown in Fig. 3.10.

The modeled van der Waals force is shown in Fig. 3.11 [17], for various values of rms surface roughness. It can be seen to be roughly independent of contact dimple size for total contact dimple areas larger than 1 μm^2, and to decrease significantly for the smallest total contact area (0.04 μm^2). This behavior can be explained qualitatively by the fact that, while the perimeter of the contact dimple decreases the average separation between contacting surfaces also decreases with decreasing contact size. However, for very small contact sizes the effect of the surface curvature becomes negligible, so that F_A scales with contact size. The effect of decreasing average separation is more pronounced for lower surface roughness.

The modeled van der Waals force for 1.5 nm rms surface roughness well explains the experimental findings, as shown in Fig. 3.8. The large variation in F_A observed for the larger

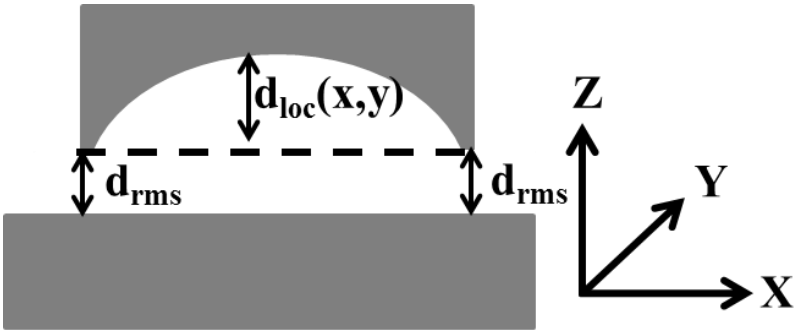


Fig. 3.10 Illustration of the modeled contact geometry. Surface roughness results in an average separation distance d_{rms}. The local separation distance between contacts is $d_{total} = d_{rms} + d_{loc}$. The radius of curvature for the top surface is 10.5μm, based on AFM measurements.

contacts is most likely due to variations in contact dimple surface curvature, which is confirmed by AFM measurements of several contact dimples. For reference, the van der Waals force assuming flat contacting surfaces is also shown in Fig. 3.8 for the smallest contact dimple area. Since the effect of surface curvature on F_A is relatively minor at that point, it can be used to estimate the van der Waals force per unit area: 0.02 nN/nm^2.

3.5 Relay Switching Energy Projections Accounting for Contact Adhesion

Table 3.1 shows the minimum switching energy values for a 100 nm (minimum feature size) relay and an 8 nm relay calculated using Equation 2.12, assuming a contact adhesive force of 0.02 nN/nm^2. The minimum switching energy of an 8 nm relay is 18 aJ instead of 0.3 aJ as projected in Chapter 2. Clearly, methods for reducing the contact adhesive force are desirable to reduce the switching energy of ultimately scaled relays to sub-aJ levels.

3.6 Impact of Ultra-thin Surface Coating

In order to reduce the van der Waals force between contacts, one can increase the average distance between surfaces in the on state, or use contact materials with a lower Hamaker constant.
For a large contact dimple, the average contact distance can be increased by increasing the surface roughness [9]. However, this approach will not be effective for an ultimately scaled relay, since the contact dimple will comprise only one asperity.

Table 3.2 compares the Hamaker constants for different materials [16] [18] [19]. It can be seen that oxides generally have much lower Hamaker constants than metals. However, oxides are poorer electrical conductors. Hence the use of an ultra-thin oxide coating is a more practical approach. To demonstrate this, relays were fabricated and electrically characterized before

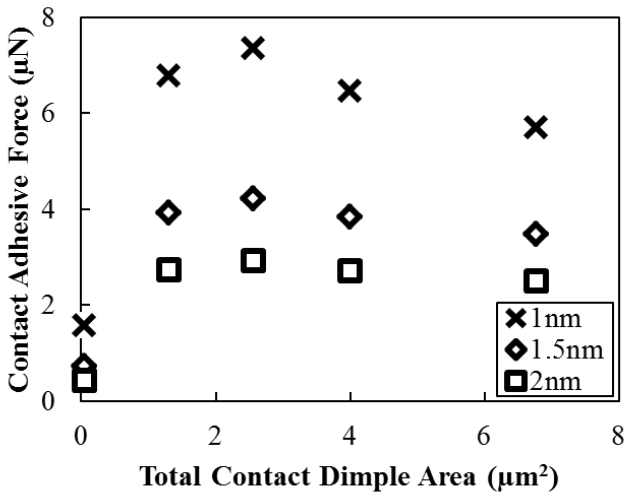


Fig. 3.11 Modeled van der Waals force vs. total contact dimple area, for various values of rms roughness of the contact dimple surface. As surface roughness decreases, the average separation distance decreases and F_A increases.

	NEM Relay			CMOS
Technology Node (nm)	**100**	**8**	**8 (+TiO_2)**	**8.4**
F_a (nN)	**700**	**4.5**	**1.7**	**N/A**
Actuation Gap (nm)	**30**	**3**	**3**	**N/A**
k_{eff} (N/m)	**35**	**2.25**	**0.85**	**N/A**
Pull-in Voltage (mV)	**310**	**100**	**61**	**610**
Switching Energy (aJ)	**$2.8x10^4$**	**18**	**6.8**	**1.28**

Table 3.1 Scaled relay switching energy compared to 8 nm CMOS transistors [18].

further processing to apply an ultra-thin TiO_2 coating (~0.5 nm) by atomic layer deposition [20]. The F_A measurement results are shown in Fig. 3.12. It can be seen that the TiO_2 coating provided for a significant reduction in F_A.

Organic coating materials also have been considered for MEM devices, since they tend to be hydrophobic and hence can reduce capillary force even in non-dry conditions [21] [22]. Some also have very low Hamaker constants. Self-assembled-monolayer (SAM) coating methods have been used to coat surfaces with organic films as thin as 1 nm depending on the size of the molecules [23]. In this work, Perfluorodecyltrichlorosilane (or FDTS) molecules were self-assembled onto relays after structural release. Some common molecules used for SAM coatings

Material	Hamaker Constant (10^{-20}J)
Al_2O_3	15.2
TiO_2	15.3
SiO_2	6.5
Al	33
Au	48
Ni	32
W	40
FDTS	5

Table 3.2 Hamaker constant of common contact or coating materials [16] [18] [19].

are illustrated in Fig. 3.13. A simple illustration of the SAM coating process is shown in Fig. 3.14.

Due to SAM coating process limitations, FDTS cannot be directly coated onto tungsten. ALD TiO_2 was used as an adhesion layer between the SAM coating and tungsten electrodes. (3 cycles were used to ensure sufficient surface coverage.) Thin films of FDTS were coated onto a flat sample along with a relay, and contact angle measurements were made on the flat sample before and after FDTS coating to monitor the surface properties. Fig. 3.15 shows that the sample before FDTS coating (after ultra-thin TiO_2 coating) is hydrophilic, while it is very hydrophobic (with a contact angle greater than 100^o) after FDTS coating.

The measured I_{DS}-V_{GB} characteristics in Fig. 3.16 show that the relay coated with FDTS turns on around 15 V, similarly as before coating. However V_{RL} appears to be larger than V_{PI} (~18 V), which suggests that V_{PI} actually increased during the measurement, likely due to surface charging in the actuation area. (The TiO_2 and FDTS layers coat all of the surfaces of the relay.)

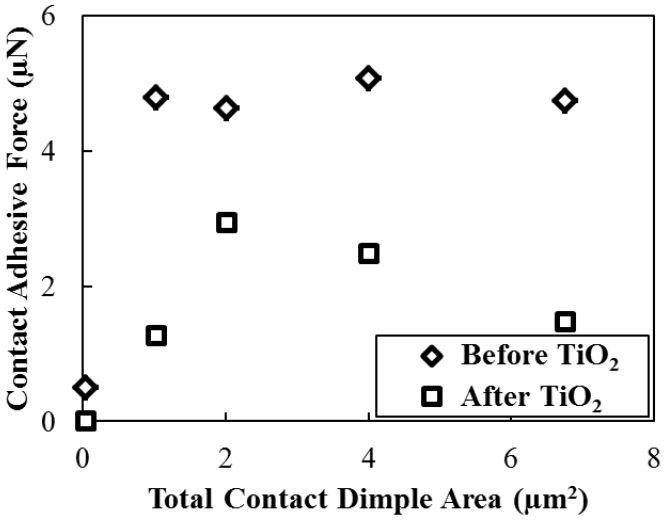


Fig 3.12 F_A (extracted from V_{PI} aind V_{RL} measurements) *vs*. total contact dimple area before and after ALD TiO_2 coating. F_A as reduced significantly after coating, since TiO_2 has a lower Hamaker constant than W.

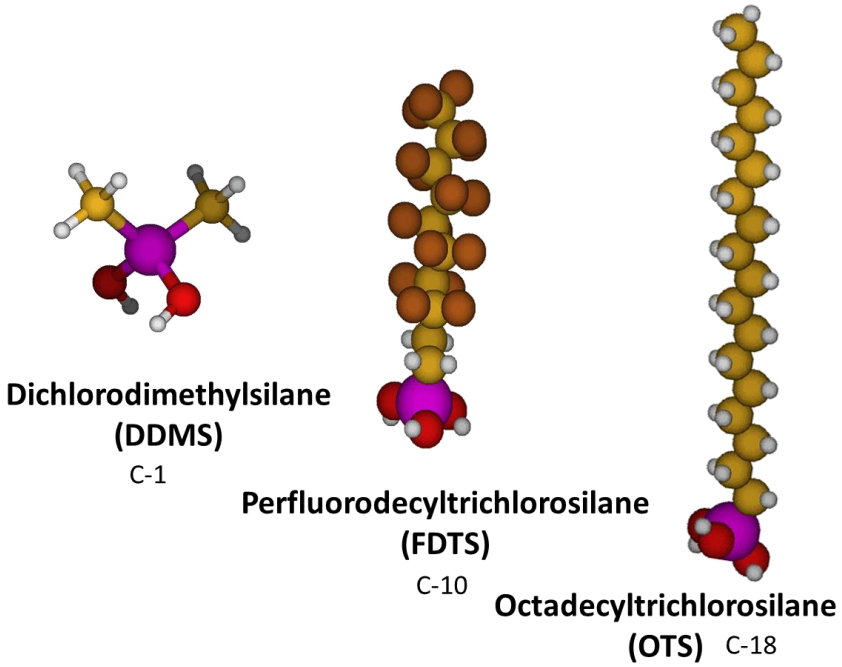


Fig 3.13 Schematic of commonly used self-assembling organic molecules DDMS, FDTS and OTS.

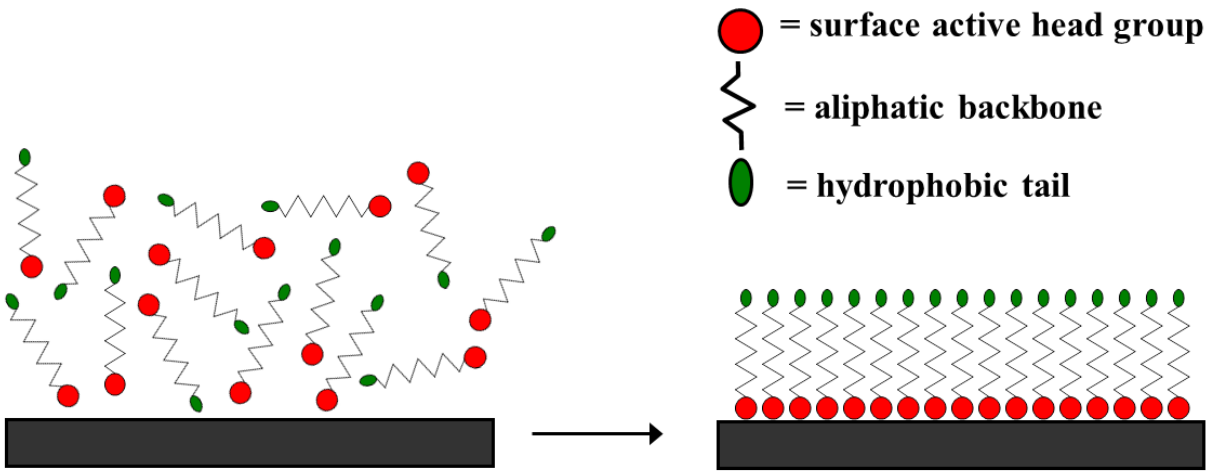
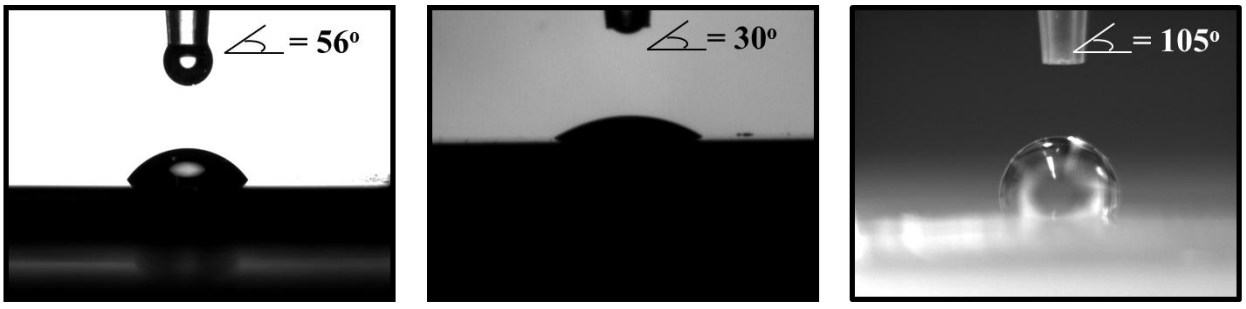


Fig 3.14 Schematic illustration of the Self-Assembled Monolayer formation process. The process starts with the hydrolysis of the polar head groups, that converts Si-Cl to Si-OH groups. Then the hydrophilic Si-OH groups which are strongly attracted to the oxidized substrate react and form covalent bonds.



12 cycles TiO_2sample **3 cycles TiO_2 sample** **FDTS SAM + 3 cycles TiO_2**

Fig 3.15 Contact angle measurements for different surface coatings. Left: Results for 12 cycles of ALD TiO_2. Middle: Results for 3 cycles of ALD TiO_2, which is the reference surface before FDTS coating. Right: SAM-coated FDTS on top of ALD TiO_2. All coatings were deposited on a sputtered tungsten sample.

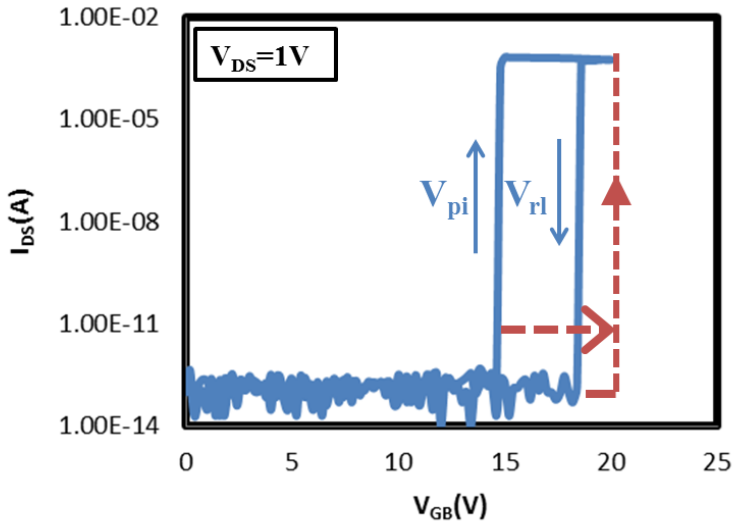


Fig 3.16 Measured I_{DS}-V_{GB} characteristics for FDTS coated MEM relay. The red dashed line shows how the turn-on characteristic of the relay likely shifted due to surface charging during the measurement.

3.7 Summary

6-terminal MEM relays with various contact dimple sizes were fabricated to experimentally extract F_A and its dependence on contact dimple size, to investigate the source of adhesion and its scalability. It is found that van der Waals force is the predominant source of adhesion. For tungsten contacting surfaces, F_A is 0.02 nN/nm^2. To lower F_A, surface coating with a material that has lower Hamaker constant is effective. Ultra-thin TiO_2 was coated by ALD onto relays after the standard release process and electrical characterization, and was observed to reduce F_A for at least 2× on all contact dimple sizes.

3.8 References

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Chapter 4

Thin Film Process Development for NEM Relay Structure

4.1 Introduction

As discussed in Chapter 2, it is desirable to have a softer structure to minimize the energy required to turn on a relay (so long as the surface adhesive force is even smaller). As the length of a suspension beam is scaled down to reduce the device footprint, the stiffness of the beam increases unless its thickness is reduced proportionately, as can be seen from the equation for the effective spring constant of a folded-flexure beam:

$$k_{eff} = \frac{EWH^3}{2L^3} \tag{4.1}$$

where E is the Young's Modulus, W is the flexure width, L is the flexure length and H is the structural layer thickness.

This chapter discusses optimization of the structural layer formation process to minimize the out-of-plane deflection of very thin beams. Section 4.2 reviews the relationship between out-of-plane deflection and the stress gradient of a thin structure. Section 4.3 discusses prior work [1] on process optimization to minimize the stress gradient in thick (1 μm) polycrystalline $Si_{0.4}Ge_{0.6}$ films, noting the challenges of using the same deposition process for thin films, and then investigates approaches to reduce out-of-plane deflection of thin (100 nm) poly-$Si_{0.4}Ge_{0.6}$ structures. Experimentally observed thin-relay failure modes are explained by out-of-plane deflection induced by the residual stress gradient.

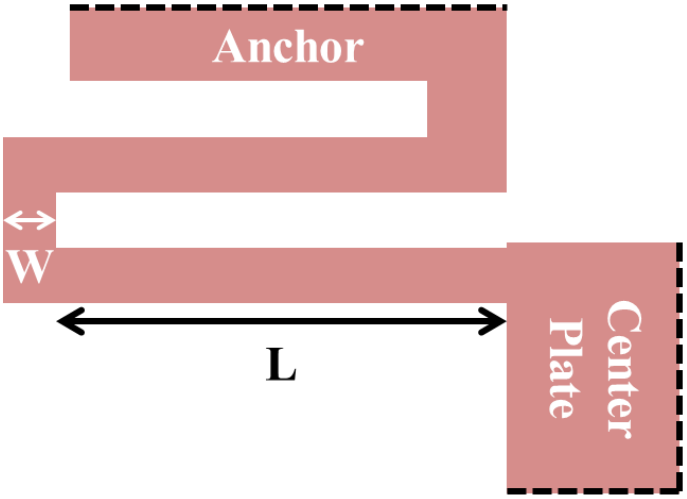


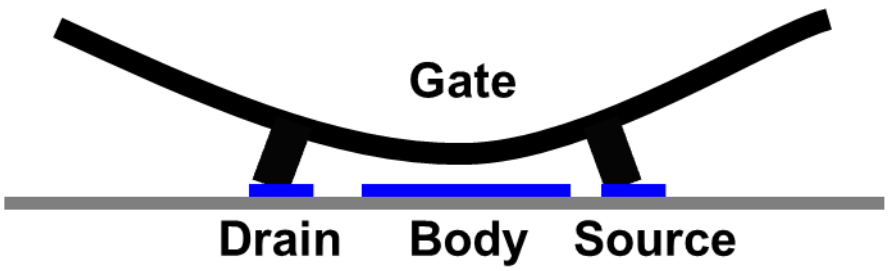
Fig. 4.1 Plan view schematic of the folded-flexure suspension beam design used in the prototype MEM relays in this work.

4.2 Stress Gradient Induced Out-of-Plane Deflection

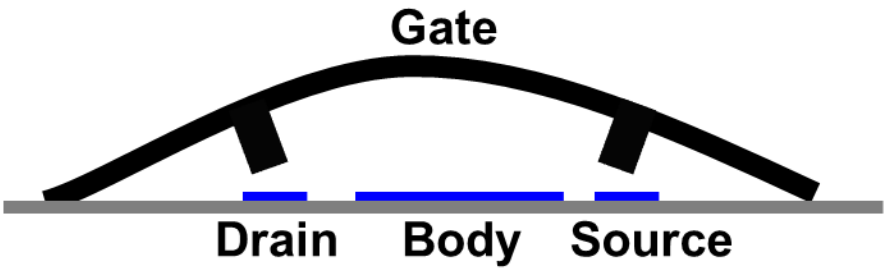
It is generally desirable to minimize out-of-plane deflection upon release of a MEM structure [2] [3]. The problems with excessive out-of-plane deflection for the prototype relay structures in this work are illustrated in Fig. 4.2. If the structural film has a positive stress gradient (*i.e.* the bottom portion of the film is more compressive than the top portion), the bottom portion of the film expands more than the top portion upon release, so that the structure has a concave upward shape; this decreases the actuation gap and the contact gaps, and in a severe case can cause the relay to be stuck on. If the structural film has a negative stress gradient, the released structure has a concave downward shape; this increases the actuation gap and the contact gaps, and in a severe case can cause the device to be stuck off. Clearly, the actuation and contact gap sizes are directly affected by out-of-plane deflection due to a non-zero stress gradient, which should be minimized to allow for the reliable formation of ultra-small gaps.

Out-of-plane deflection is gauged by the radius of curvature of the structural film. For the cantilever beam shown in Fig. 4.3, the radius of curvature (ρ) is related to the out-of-plane deflection of the beam tip (Δz) and the length of the beam (L) [4]:

$$\frac{1}{\rho} = \frac{2\Delta z}{L^2} \tag{4.2}$$



a)



b)

Fig. 4.2 Simplified cross-section schematics of MEM relays with non-zero stress gradient. a) Positive stress gradient results in a concave upward structure, and in a severe case can cause the device to be stuck on. b) Negative stress gradient cause a concave downward shape, and in a severe case can prevent the device from turning on.

The relationship between the radius of curvature and the stress gradient is given by the following equation [4]:

$$\frac{1}{\rho} = \frac{12}{EH^3}\int_{-n}^{H-n} \sigma(z) z dz \tag{4.3}$$

where E is the Young's modulus, H is the thickness of the film, σ(z) is the residual stress at depth z, and n is the position of the neutral axis. Assuming a film with constant positive stress gradient throughout the film, with a neutral axis at the middle of the film, Equation 4.3 can be rewritten as

$$\frac{1}{\rho} = \frac{2\sigma_o}{EH} \tag{4.4}$$

where $2\sigma_o/H$ is the stress gradient of the film. $1/\rho$ is known as the strain gradient of the film and is proportional to the stress gradient by a factor of E. In order to increase the radius of curvature (which will result in less out-of-plane deflection), the average stress gradient must be reduced.

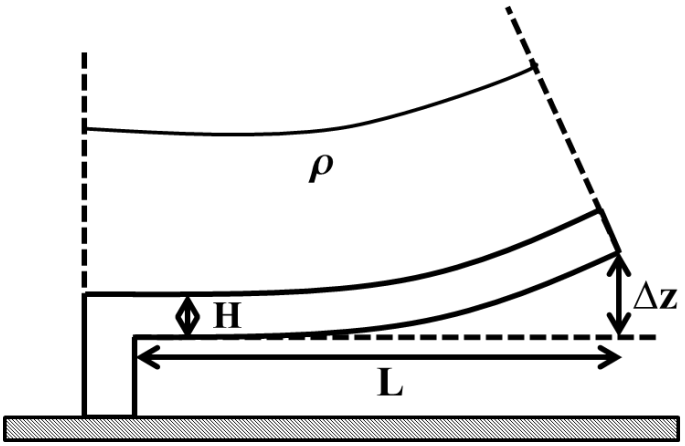


Fig. 4.3 Schematic cross-sectional illustration of a cantilever beam with out-of-plane deflection.

4.3 Reduction of Stress Gradient in LPCVD Poly-$Si_{0.6}Ge_{0.4}$ Films

4.3.1 Structural Properties of Poly-$Si_{0.6}Ge_{0.4}$

The factors which can affect the stress gradient within a polycrystalline film include dopant concentration, deposition temperature and deposition pressure [5] [6]. Optimization of the deposition process to reduce the stress gradient of a poly-SiGe film is described in [7] and [8]. The poly-$Si_{0.4}Ge_{0.6}$ LPCVD process initially used for the prototype relays in this work was optimized in prior work to achieve 1 µm-thick films with minimal out-of-plane deflection. The corresponding stress profile is shown in Fig. 4.4a, with the deposition conditions indicated in the top left corner of the figure [7]. The average residual stress in the film is compressive, and the strain gradient is 8×10^{-5} μm^{-1} (*i.e.* ρ = 12500 µm), which would result in 9 nm deflection for the prototype relay of Fig. 3.3. A high-resolution cross-section transmission electron micrograph of the film is shown in Fig. 4.4b.

The deposition recipe starts with an amorphous Si seed layer, ~1 nm thick, followed by SiGe deposition with *in-situ* Boron doping. Initially the SiGe is actually amorphous; as the deposition proceeds, it eventually becomes polycrystalline. From Fig. 4.4b it can be seen that the thickness of the amorphous region (comprising the amorphous Si seed layer and a portion of the SiGe layer) ranges from tens of nanometers to ~500 nm. If a 100 nm-thick film is deposited using the same recipe, it would be mostly amorphous with local crystalline regions as shown in Fig. 4.5 resulting in highly variable stress gradient across the wafer substrate.

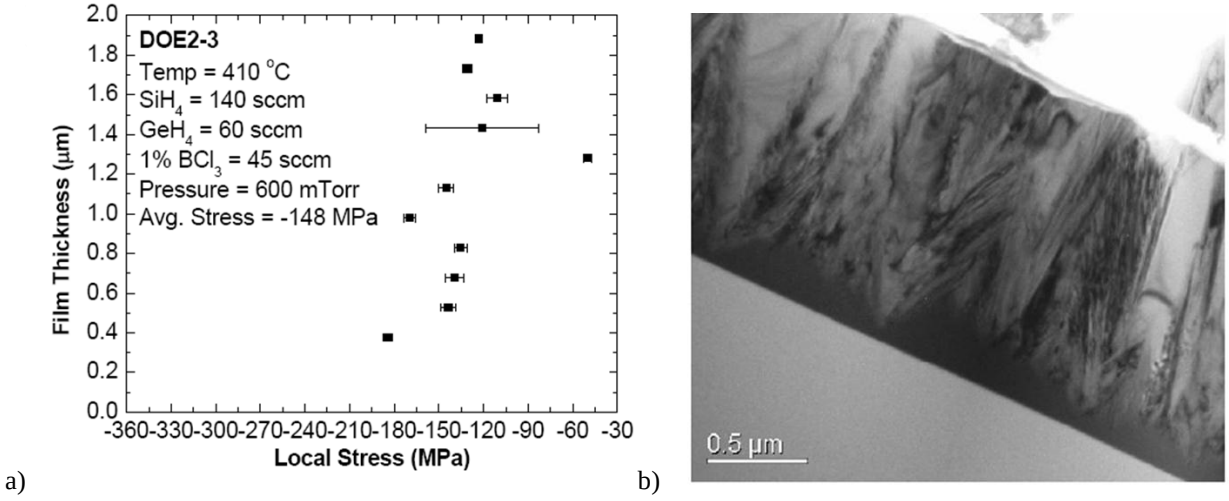


Fig. 4.4 Stress gradient optimized poly-$Si_{0.4}Ge_{0.6}$ film. a) Stress profile. b) High-resolution cross sectional TEM (HR-TEM) image (adapted from [7]).

Fig. 4.5 HR-XTEM of a ~500 nm-thick poly-$Si_{0.4}Ge_{0.6}$ deposited using the stress gradient optimized deposition recipe. Note that the film is only partially polycrystalline with significant thickness variation (adapted from [7]).

In order to achieve low stress gradient within a thin poly-$Si_{0.4}Ge_{0.6}$ film, the crystalline structure must be made to be more uniform throughout its depth.

4.3.2 Minimization of Amorphous Region Thickness

The key to mitigate variations due to polycrystalline grain non-uniformities (cf. Fig. 4.5) is to minimize the amorphous region thickness. Generally, reducing the deposition rate can enhance the chance to form crystal seeds and hence reduce the amorphous region thickness. Lowering the deposition rate by lowering the process pressure is known to reduce the amorphous region thickness, as shown in Fig. 4.6.

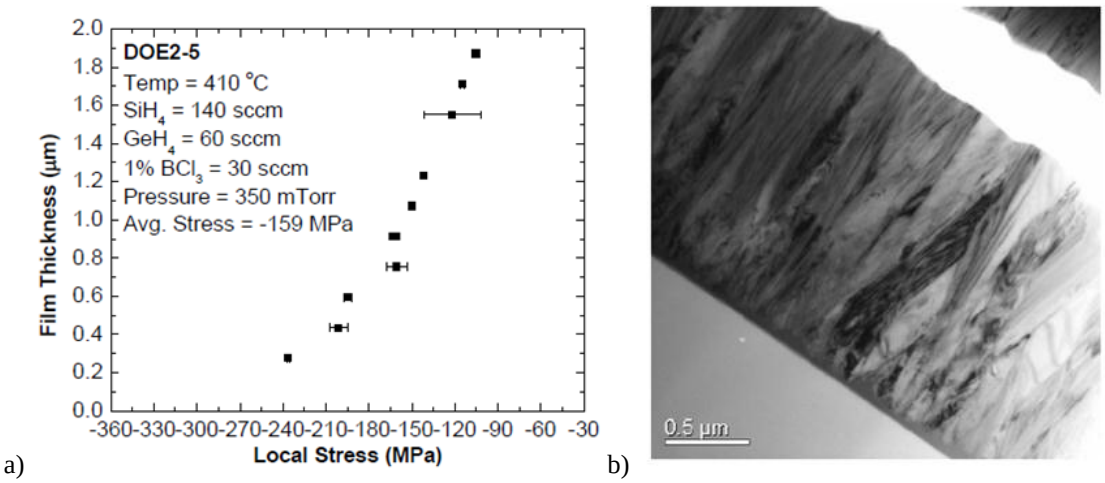


Fig. 4.6 Poly-SiGe film deposited with lower process pressure (350 mtorr vs. 600 mtorr). a) Stress profile. b) HR-XTEM image (adapted from [7]).

Since an amorphous film is known to be more compressive, a film comprised of a polycrystalline layer on top of an amorphous layer would result in a positive stress gradient. This is observed in the measured stress profile in Fig. 4.6.

It should be noted that one of the requirements for thin film processing is to limit the deposition time to reduce cost, hence putting a practical limit on deposition time *i.e.* a minimum deposition rate for a given thickness. If the target film thickness is much thinner (10×), then a much lower deposition rate can be acceptable.

4.3.3 Post Deposition Processing to Reduce Stress Gradient

The stress gradient within a film can be altered post-deposition. One technique that can be used is thermal annealing, which is known to reduce the resistivity, stress gradient and improve the quality factor of poly-SiGe or poly-Si films [9-10]. For example, annealing in a low-pressure N_2 environment can result in secondary grain growth, which would transform the bottom portion of the film into polycrystalline material. However, since the amorphous portion of the film is less dense to begin with, this crystallization would result in tensile stress. If the bottom portion of the film turns from compressive to tensile, the stress gradient becomes less positive. Table 4.1 shows that as the thermal budget increases, the stress gradient turns from positive to negative. If the as-deposited film has a positive stress gradient, then, post-deposition thermal annealing can be effective for reducing the stress gradient.

To study the effect of post-deposition annealing conditions, relays were fabricated with a structural film thickness of 100 nm. The footprint of the relays is the same as that of the devices discussed in Chapter 3, shown in Fig. 4.7. The device dimensions are shown in Table 4.2.

Temperature (°C)	Time (min.)	Resistivity (mΩ-cm)	Stress (MPa)	Strain Gradient ($\times 10^{-5}$ μm^{-1})
As-deposited	N/A	0.6	-150	4.7
430	30	0.6	-147	2.7
430	180	0.6	-144	-15.2
600	30	0.6	-115	-44

Table 4.1 Impact of thermal annealing on residual stress and strain gradient. As the thermal budget increases, strain gradient turns from positive to negative (adapted from [7]).

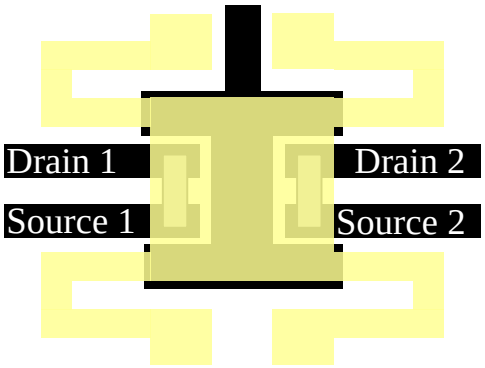
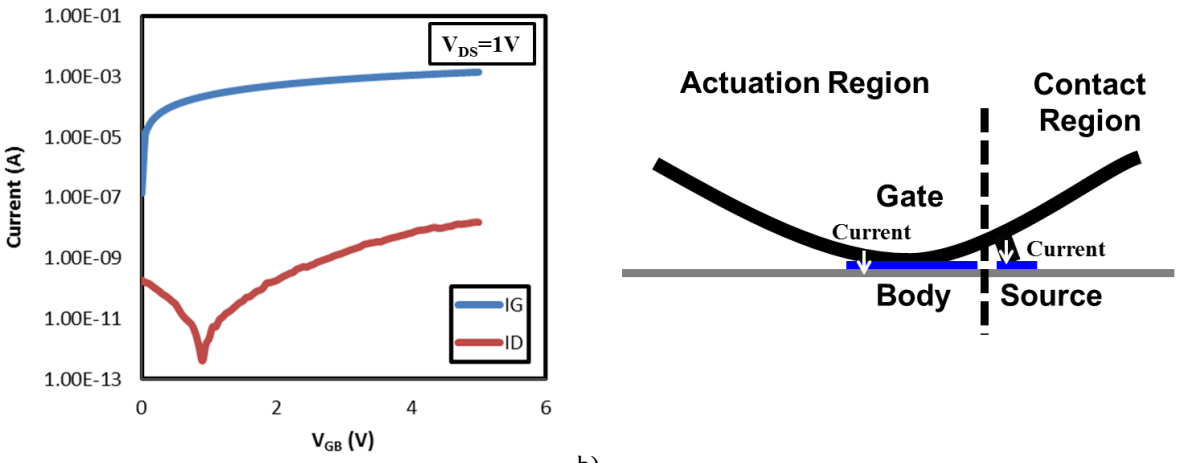


Fig. 4.7 Plan view schematic of the MEM relay design used for thin-film stress gradient study.

Flexure Length (L)	15 μm
Flexure Width (W)	4 μm
Actuation Area (A_{OV})	200 μm^2
Actuation Gap (g)	180 nm
Dimple Gap (g_d)	40 nm
Structure Thickness (H)	1 μm
Dimple Width	0.8 μm

Table 4.2 MEM relay design parameter values used for thin-film stress gradient study (adapted from [3]).



a) b)

Fig. 4.8 Results for a thin MEM relay which went through a 2-hr anneal at 450°C in N_2. a) Measured I-V_{GB} characteristics. Gate to body current and drain to source current is observed suggesting a conduction path caused by contact between the structure and underlying body electrode. b) Cross-sectional schematic showing out-of-plane deflection suggested by the electrical measurement results.

The structural film of the relays was deposited at 300 mtorr, reduced from 600 mtorr of the original recipe. The devices were annealed in N_2 at 450°C before structural release and electrical measurement. The thickness of the Al_2O_3 gate oxide deposited via ALD was 5 nm, scaled down proportionately with the structural layer thickness reduction (from 50 nm). Unfortunately this thin gate oxide was found to be damaged by the release etch process, so that gate current can flow if the structure is in contact with the drain, source or body electrodes.

Fig. 4.8a shows the measured I-V_{GB} curves for a device that was annealed for 2 hours in N_2 at 450°C. Gate-to-body current as well as drain-to-source current is seen. It was found that the center plate is in contact with the bottom electrode, causing the gate-to-body short. The contact dimples are also in contact with the source/drain electrodes, causing the drain-to-source short. These results suggest that the structural plate has a concave upward shape, *i.e.* it has positive stress gradient as illustrated in Fig. 4.8b. Fig. 4.9a shows the measured I-V_{GB} plot of a device annealed for 3 hours in N_2 at 450°C. The electrical results still show a gate-to-body short, but with a much smaller amount of current. No drain current is observed. These results suggest that the structural plate has a concave downward shape, *i.e.* it has negative stress gradient causing the edge of the center plate to contact the body interconnect lines (which run between the body electrode and the probe pad), as shown in Fig. 4.9b. This curvature also prevents the contact dimples from making contact with the source/drain electrodes.

These annealing experiments show that stress gradient can be altered from positive to negative. However, developing an effective annealing process may be difficult if the duration of the (furnace) anneal must be precisely controlled. A post-deposition treatment with more precise control is needed to fine-tune the stress gradient of the structural film.

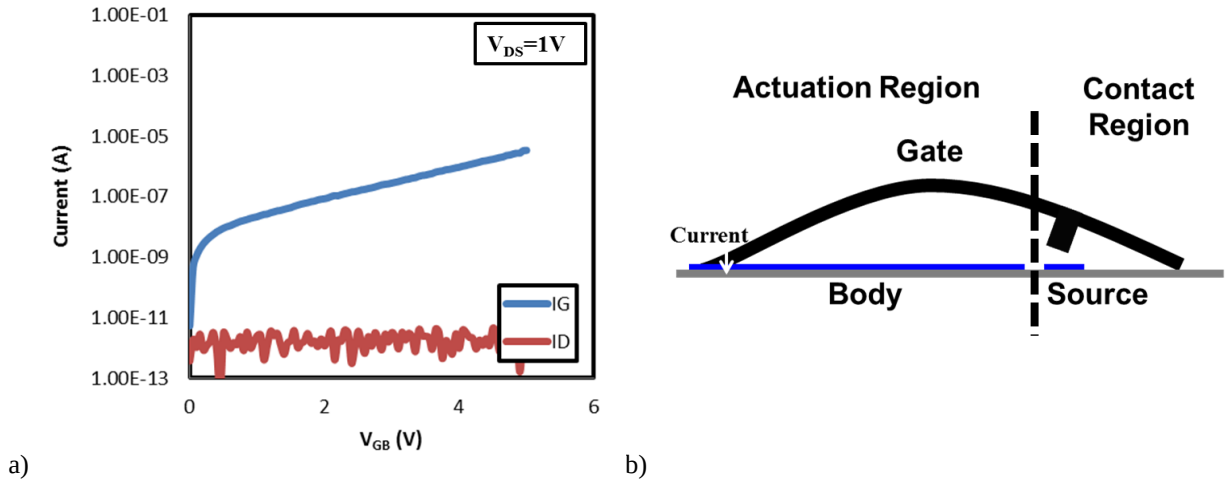


Fig. 4.9 Results for a thin MEM relay which went through a 3-hr anneal at 450°C in N_2. a) Measured I-V_{GB} characteristics. b) Cross-sectional schematic showing out-of-plane deflection suggested by the electrical measurement results.

One of the most precise process techniques available is ion implantation, which can also be used to alter thin film stress. Ion implantation damages the crystalline structure and relieves the residual stress throughout the thickness of implantation projection depth [11] [12]. Since the stress of poly-SiGe is generally compressive, reducing compressive stress within the top portion of the film would make it have less negative stress gradient.

The effect of ion implantation will depend on the implant energy and dose, as shown in Fig. 4.10. The implant energy determines the projected range, which affects the depth to which the stress is relieved. The implant dose affects the amount of damage to the film; from previous experiments it was found that the dose only needs to be large enough to generate sufficient crystal damage, *i.e.* a dosage beyond this level does not further affect the stress gradient of the film. As shown in Fig. 4.10, there is a linear relationship between the implant energy and strain gradient, for an Argon ion dose of 10^{14}/cm^2; lower doses show little to no effect, whereas higher doses show the same trend line as for a dose of 10^{14}/cm^2. Thus 10^{14} ions/cm^2 is a sufficient dose for stress relaxation purposes. Ar was chosen as the implant species in this work because it provides for a relatively low-cost and high-throughput process.

Relays were fabricated using a poly-$Si_{0.4}Ge_{0.6}$ structural film of 100nm deposited using a low process pressure and then annealed in N_2 furnace at 500°C for 10 minutes to ensure a negative stress gradient. The structural film was subsequently implanted with 10^{14} Ar^+/cm^2 at an implant energy of 20 keV, 30 keV or 40 keV, which should amorphize 33%, 50%, 67% of the structure film accordingly [7].

It is worth noting that ion implantation not only changes the stress gradient of the film, but also affects other properties such as surface roughness and resistivity. As the implant energy increases, the thickness of the top amorphous region increases, hence the resistivity of the film

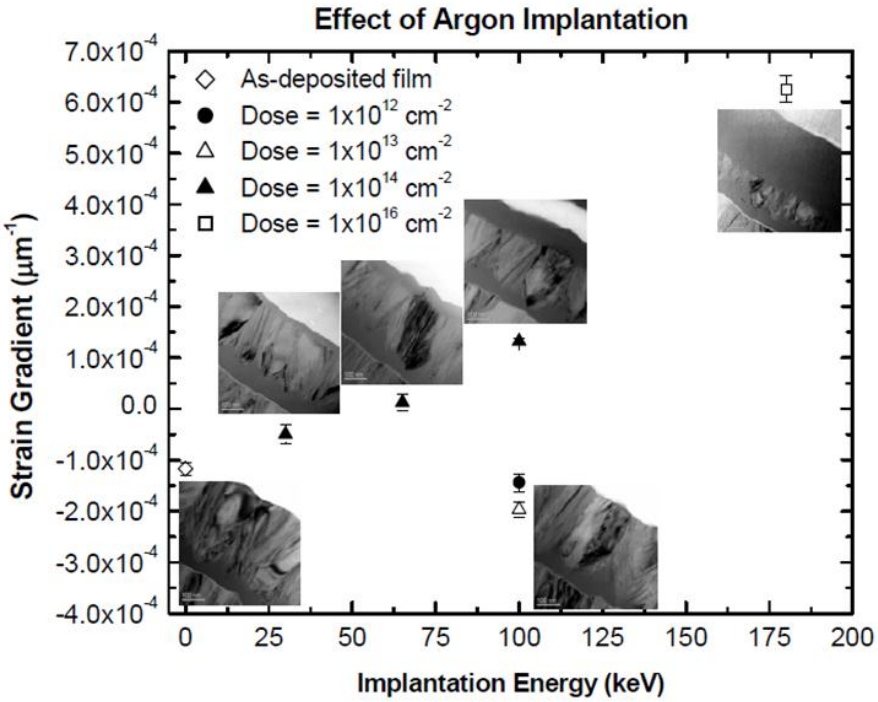


Fig. 4.10 Strain gradient *vs.* Ar ion implantation energy, for various implant doses. It is found that strain gradient turns positive as the implant (damage) depth increases. The effect of dose when larger than 10^{14} ions/cm^{-2} on strain gradient is negligible (adapted from [7]).

increases. Measured surface roughness and sheet resistivity values are tabulated in Tables 4.3 and 4.4, respectively.

For a 20 keV implant, the relay exhibits small gate-to-body current with no drain current (*i.e.* similar to the characteristics shown in Fig. 4.9), indicative of a negative stress gradient. Fig. 4.11 shows measured electrical characteristics of relays fabricated with structural films implanted with Argon ions at 30 keV or 40 keV. The 30 keV implanted device has a low V_{PI} value of 0.3 V; however, both drain-to-source current and gate-to-body current are seen when the device is turned on, which suggests that the vertical positions of the bottom of the contact dimple and the bottom of the gate are roughly the same due to the stress gradient, to cause the gate and dimples to contact the co-planar actuation and source/drain electrodes at the same time, *i.e.* the structure has a slightly positive stress gradient. The 40 keV implanted device exhibits gate-to-body current which turns on/off at lower voltage than the drain-to-source current, which suggests that the vertical position of the bottom of the gate is lower than the bottom of the dimples, *i.e.* the structure has a positive stress gradient. These results confirm that the stress gradient can be tuned by adjusting the implant energy.

With out-of-plane deflection mitigated, a thin poly-$Si_{0.4}Ge_{0.6}$ structural film provides for lower pull-in voltage (~4 V *vs*. 15 V). A combination of post-deposition treatments including thermal annealing and ion implantation can reduce the strain gradient to be less than 4×10^{-4} μm^{-1}. In this case, the out-of-plane deflection should be less than 0.1 nm for the ultimately scaled relay design shown in Fig. 2.12.

Experimental Split	Surface Roughness (nm)
As deposited	2.9
500°C 2hr N_2 anneal	2.7
Implanted run	6.2

Table 4.3 Measured surface roughness of a poly-$Si_{0.4}Ge_{0.6}$ film at various steps. The roughness increases significantly after ion implantation.

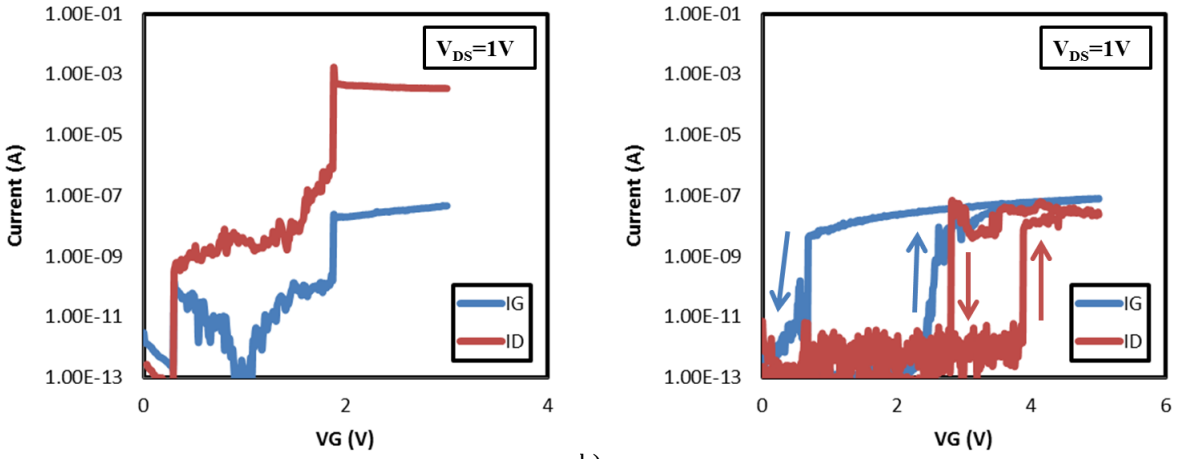


Fig. 4.11 Measured I-V_{GB} characteristics of relays with implanted structural films: a) 30 keV implant energy (V_{PI} = 0.3 V but both gate and drain current are observed); b) 40 keV implant energy (V_{PI} = 4 V but gate-to-body contact is also observed at V_{GB} ~ 2 V).

Implant Energy	Before Implant (Ω/sq)	After Implant (Ω/sq)
20 keV	180.32	483.1
30 keV	174.7	1013.6
40 keV	169.94	2932.4

Table 4.4 Comparison of poly-$Si_{0.4}Ge_{0.6}$ film sheet resistivity before and after Ar ion implantation, for different implant energies. As the depth of the amorphized region increases, sheet resistance increases.

4.3.4 Additional Scaling Challenges

Although post-deposition treatments can serve to shift the stress gradient, they are not effective for reducing variability in stress gradient. The scatter plot in Fig. 4.12 shows the extent of variation in poly-$Si_{0.4}Ge_{0.6}$ strain gradient and resistivity for three different LPCVD recipes; each recipe yields films with strain gradient values ranging from negative to positive, due to local variations in temperature and gas flow hence grain nucleation and growth [13] [14]. Post-deposition processing can reduce the overall device yield, since the stress gradient will worsen in some devices while it gets better in other devices. Tighter control of stress gradient is needed as the film thickness is scaled down.

Some post-deposition processing techniques can be impractical to implement for very thin structural films. For example, as the film thickness is scaled below 50 nm, the poly-$Si_{0.4}Ge_{0.6}$ sheet resistance increases to ~1000 Ω/sq; in this case, it may not be acceptable to tune the stress gradient via ion implantation because it further increases the sheet resistance.

Other than better process control, moving away from a polycrystalline structural film can be another option for the ultimately scaled relay. For example, as more advanced deposition technology such as metal atomic layer deposition emerges, it may become practical to use a uniformly thin and amorphous metal as a structural film. Metals are generally very conductive and have relatively low Young's modulus and hence can be attractive for an ultimately scaled NEM relay [15-17].

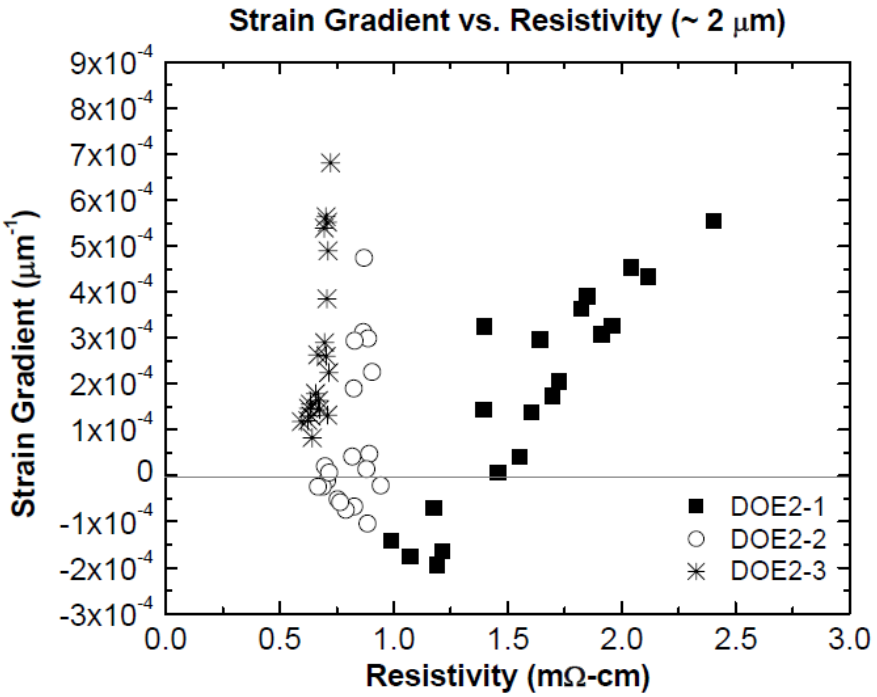


Fig. 4.12 Poly-$Si_{0.4}Ge_{0.6}$ strain gradient *vs.* film resistivity for 3 different LPCVD recipes. For each recipe, large variations in strain gradient are observed (adapted from [7]).

4.4 Summary

As the lateral dimensions of a relay structure are scaled down, the thickness of the structure also must be scaled down to ensure low stiffness (required for low voltage operation). The thin-film deposition and post-deposition processes must be optimized to minimize stress gradient in order to minimize out-of-plane deflection which can result in yield issues.

In this chapter, stress gradient optimization methods are investigated to facilitate a reduction in poly-$Si_{0.4}Ge_{0.6}$ structural layer thickness, from 1 µm to 100 nm. It is found that the deposition conditions need to be re-optimized to limit the extent of (and variation in) the initial amorphous layer. Stress gradient can be adjusted by post-deposition thermal annealing and ion implantation. MEM relays fabricated with 100 nm-thick poly-$Si_{0.4}Ge_{0.6}$ films exhibit relatively low pull-in voltage, below 5 V.

Further scaling of the poly-$Si_{0.4}Ge_{0.6}$ structural layer thickness below 50 nm will be extremely difficult due to process variations. Also, post-deposition processing techniques such as ion implantation can be ineffective below 50 nm, since it is not desired to have a significant portion of the film amorphous, as this would make the film highly resistive. An alternative is to use an amorphous metal structural film, as metals are generally softer and more conductive compared to poly- $Si_{0.4}Ge_{0.6}$.

4.5 References

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Chapter 5

NEM Relay Fabrication using Electron-Beam Lithography

5.1 Introduction

Previous studies showed that relays have the ideal switching properties of zero off-state leakage and abrupt on/off transition. The demonstrated prototype devices have relatively slow switching speed and high operating voltage relative to transistors, however. These issues can be mitigated by scaling down the device dimensions [1]. Recently, micro-mechanical switches have been demonstrated with operating voltage below 1 V; however, these devices either still have relatively large footprint (~900 μm^2) [2] or are simple two-terminal devices which are not suitable for digital logic applications [3]. A factor of 10^6 reduction in layout area is needed to achieve a device footprint that is comparable with that of modern CMOS transistors [2].

This chapter describes the fabrication of aggressively scaled relays employing the folded-flexure ("crab-leg") suspension beam design and thin poly-$Si_{0.4}Ge_{0.6}$ structural film described in earlier chapters, achieving minimum feature size below 100 nm by using electron-beam lithography. Section 5.2 describes the 3-terminal relay design, along with the fabrication process flow. Finite element method simulations are used to estimate the operating voltage of relays with aggressively scaled dimensions. Section 5.3 shows measured characteristics of the fabricated relays, and notes remaining challenges.

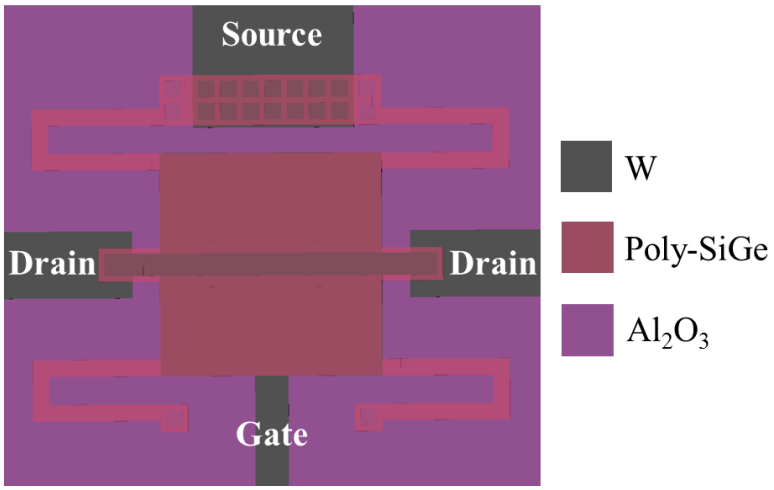


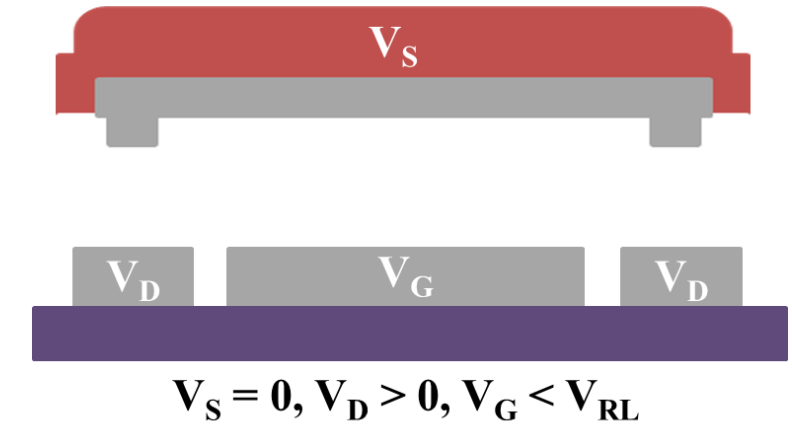
Fig. 5.1 Layout of the 3-terminal relay design showing the patterns of the tungsten (W) electrode layer, the insulating oxide (Al_2O_3) layer, and the poly-$Si_{0.4}Ge_{0.6}$ structural layer. The structure serves as the source electrode; the two electrodes on either side of (and coplanar with) the underlying gate electrode serve as the drain electrode.

5.2 Relay Design and Fabrication Process

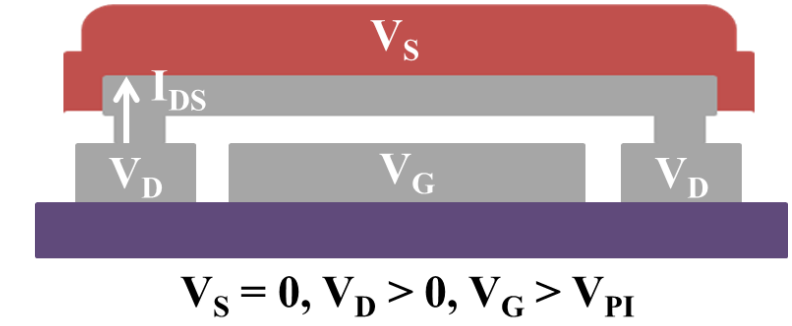
A 3-terminal switch design [5] is adopted in this work, eliminating the Al_2O_3 gate oxide layer from the fabrication process so that the movable structure comprises a thin poly-$Si_{0.4}Ge_{0.6}$ film (discussed in Chapter 4) rather than a poly-$Si_{0.4}Ge_{0.6}$/Al_2O_3 multi-layer film. The pull-in voltage (V_{PI}) should be similar to that for the 6-terminal relay design (discussed in Chapter 2) if the gate-oxide layer is significantly thinner (by more than 10×) than the structural layer and has similar residual stress and Young's modulus [6] [7]. Although 3-terminal relays can be used to implement complementary logic circuits, isolation between the input signal path and output current path is desirable, so that relays with a gate oxide (*i.e.* having 4 or more terminals) are preferred for implementation of complex digital logic circuits [8].

Fig. 5.1 shows the layout of the 3-terminal relay, and Fig. 5.2 illustrates its operation. The movable structure serves as the source electrode, the underlying fixed metal electrode serves as the gate electrode, and the fixed metal electrodes on both sides of (and coplanar with) the gate electrode serve as the drain electrodes. Voltage is applied between the gate and source to actuate the structure downward and bring the metallic channel strip (attached underneath the movable poly-$Si_{0.4}Ge_{0.6}$ plate) into contact with the drain electrodes, allowing current to flow between the source and drain.

Fig. 5.3 shows a scaled relay design with dimensions as listed in Table 5.1. It has a minimum feature size of 50 nm, and footprint of 12 μm^2. From finite element method (FEM) simulations, the expected switching voltage is ~3.5 V assuming no stress gradient in the structural film. Comparison against experimental measurements should reveal the effects of residual stress and stress gradient on relay performance.



a)



b)

Fig. 5.2 Schematic cross-sections illustrating the operation of the3-terminal relay. a) Off state ($V_{GS} < V_{RL}$), b) On state ($V_{GS} > V_{PI}$) – contact dimples and bottom electrodes are in contact so that current can flow between the source and drain.

Nano-electro-mechanical (NEM) relays were fabricated using electron-beam (e-beam) lithography as follows: 50 nm of Al_2O_3 was deposited via Atomic Layer Deposition (ALD) to insulate the surface of the Si wafer substrate. Then, 30 nm of tungsten (W) was deposited by sputtering and patterned to form the drain and gate electrodes. Next, 35 nm of SiO_2 (low temperature oxide, LTO) was deposited via LPCVD to form the first sacrificial layer, in which 100 nm-wide contact dimple regions were defined. Afterwards, a second layer of 35 nm sacrificial LTO was deposited to (eventually) form the contact dimple gap. Then, 30 nm of W was sputtered and patterned to form the metallic channel strip. Prior to deposition of the 100 nm p-type poly-$Si_{0.4}Ge_{0.6}$ structural film by LPCVD, via holes were etched through the sacrificial layers to form anchor and interconnect regions. Due to the limited field size of e-beam lithography, deep-UV lithography was used to complete the patterning of the structural layer. After poly-$Si_{0.4}Ge_{0.6}$ patterning, the structures were released by selectively removing the sacrificial LTO layers in HF vapor. Key steps in the process flow are illustrated in Fig. 5.4.

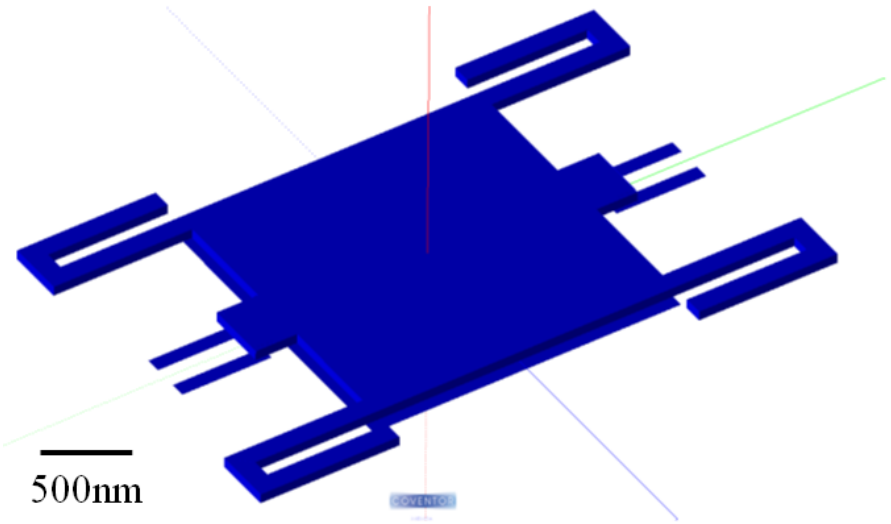


Fig. 5.3 Simulated NEM relay structure. The ends of the folded-flexure suspension beams are fixed (serving as anchors) in the simulation.

Flexure Length (L)	1 μm
Flexure Width (W)	150 nm
Actuation Area (A_{OV})	4 μm^2
Actuation Gap (g)	60 nm
Dimple Gap (g_d)	30 nm
Structure Thickness (H)	0.1 μm
Dimple Width	50 nm
V_{PI}/V_{RL}	3.5V/0.4V

Table 5.1 Dimensions of the simulated NEM relay structure.

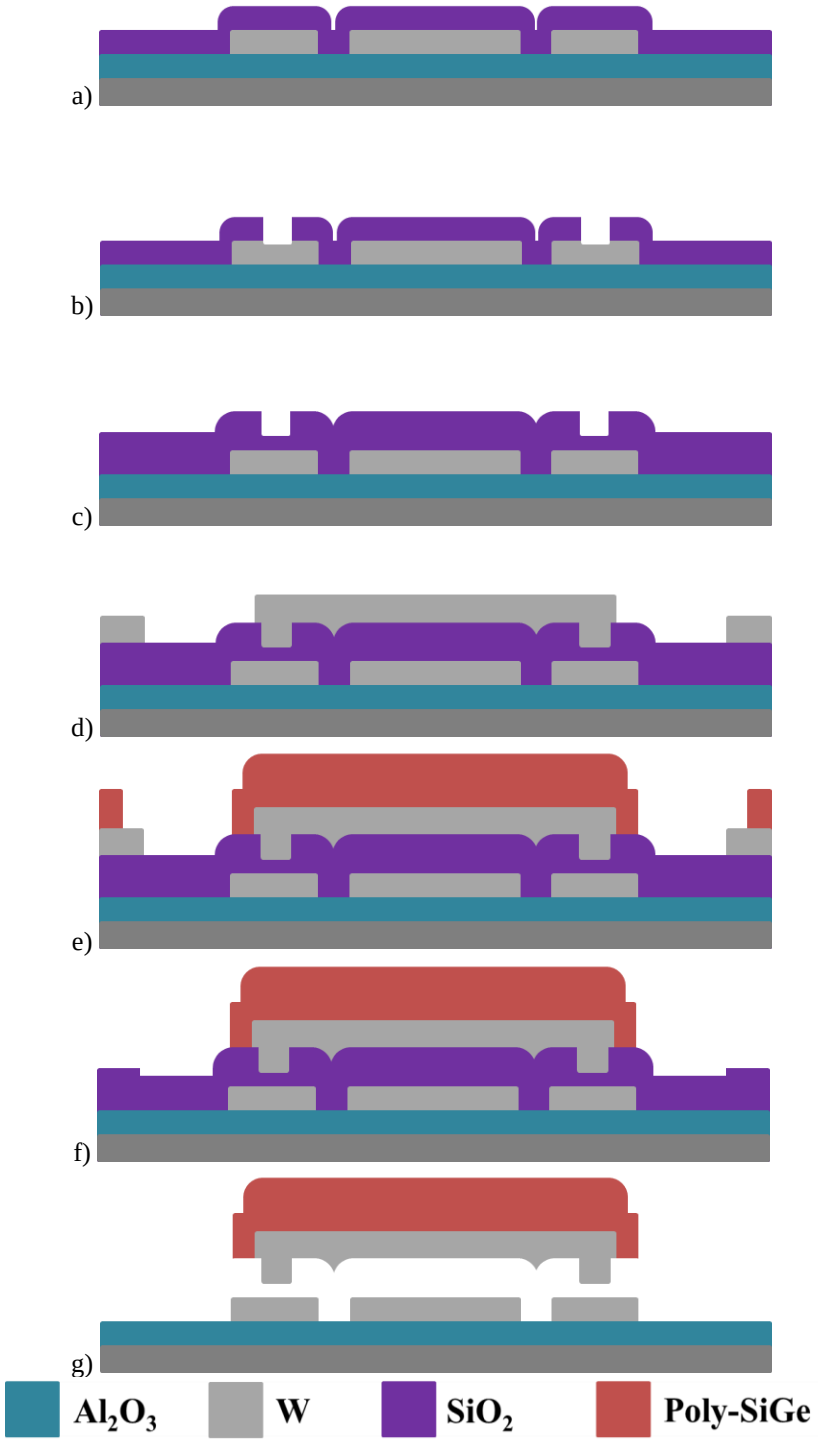


Fig 5.4 Schematic cross-sections illustrating key steps in the relay fabrication process. a) W electrode layer is sputtered and patterned, followed by deposition of the 1st LTO sacrificial layer. b) Contact dimples are defined. c) 2nd sacrificial LTO layer is deposited. d) W channel layer is sputtered and patterned. e) poly-$Si_{0.4}Ge_{0.6}$ structural layer is deposited and patterned. f) Complete patterning of poly-$Si_{0.4}Ge_{0.6}$ and W (out of e-beam lithography field). g) Release the structure using vapor-HF to selectively remove the LTO.

5.3 NEM Relay Experimental Results

Fig. 5.5 shows a tilted-view scanning electron micrograph (SEM) of a fabricated device with dimensions as listed in Table 5.2. It can be seen that the structures is released successfully. A comparison of the air gap thicknesses underneath the folded-flexure beams and underneath the center plate suggests minimal out-of-plane deflection. Measured electrical characteristics are shown in Fig. 5.6. V_{PI} of 9 V is measured, but the relay does not turn off properly.

Based on the adhesive force study in Chapter 3, it is estimated that the device (with a contact dimple width of 50 nm) should turn off at 1.6 V; but this was not experimentally observed. Upon close examination, it was found that the contact gap is much thinner than expected, resulting in low spring restoring force as well as non-pull-in mode operation. FEM simulations were performed to confirm this: as shown in Fig. 5.7, the relay should pull in at 10 V as designed (with a 35 nm contact dimple gap as fabricated); the lower pull-in voltage of 8.8 V suggests that the contact dimple gap is actually closer to 10 nm. The spring restoring force in the on state is therefore only one-third of that designed, causing the relay to be stuck down once it is turned on.

These results indicate that the contact dimple formation process should be refined to either increase the spring restoring force or reduce the contact adhesive force, to achieve a properly functioning relay. Fig. 5.8 illustrates two approaches. First, by depositing a thicker 2^{nd} sacrificial LTO layer, the contact dimple can be overfilled to result in a peaked contact surface; this would result in lower contact area and hence lower adhesive force. It should be noted that the electrical resistance of an atomic contact (single metallic bond) is approximately 10 kΩ [10], which is acceptable for digital logic applications since circuit operating speed is limited primarily by mechanical delay rather than electrical "RC" delay; experimental extraction of the adhesive force in this case would allow the switching energy of an ultimately scaled relay to be accurately projected. Second, by using a thinner 1^{st} sacrificial LTO layer together with a thicker 2^{nd} sacrificial LTO layer (and perhaps slightly larger contact dimple area) the as-fabricated contact gap can be made larger to increase the spring restoring force in the on state.

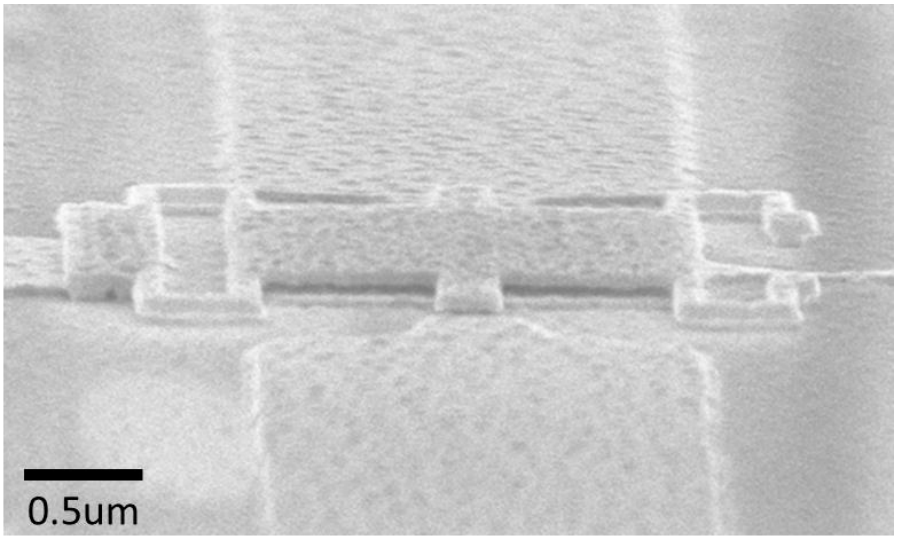


Fig 5.5 Tilted-view SEM of a fabricated NEM relay. It can be seen that the structure is successfully released with little out-of-plane deflection.

Flexure Length (L)	0.5 μm
Flexure Width (W)	150 nm
Actuation Area (A_{OV})	1 μm^2
Actuation Gap (g)	70 nm
Dimple Gap (g_d)	35 nm
Structure Thickness (H)	0.1 μm
Dimple Width	50 nm

Table 5.2 Dimensions of the fabricated device shown in Fig. 5.5.

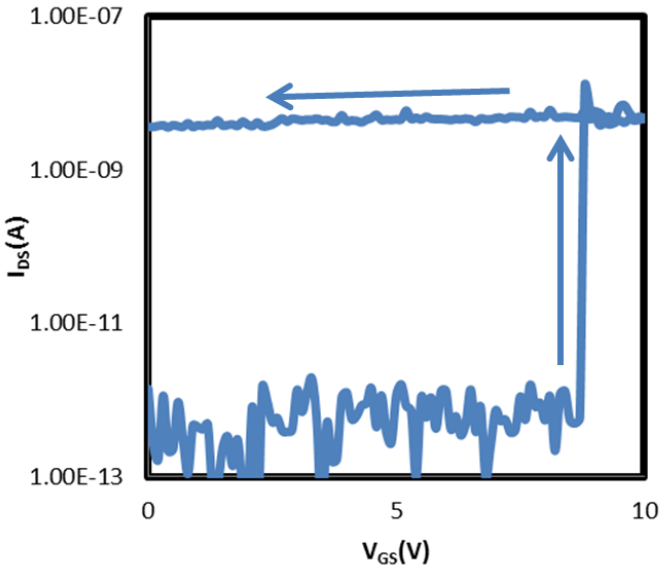


Fig 5.6 Measured I_{DS}-V_{GB} characteristics of the scaled NEM relay shown in Fig. 5.5. V_{PI} is 8.8 V, but the relay remains on when the applied voltage is reduced back down to 0 V. V_D = 5 mV.

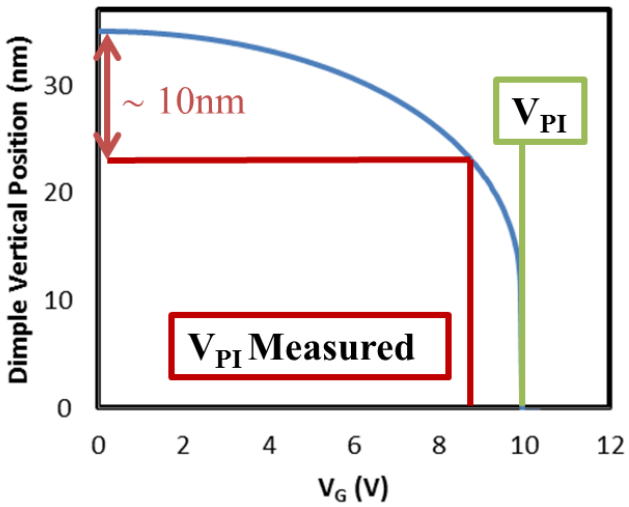


Fig 5.7 Simulated deflection vs. V_G of a scaled relay. Assuming that the contact dimple gap (g_d) is 35 nm as fabriated, the relay should turn on at 10 V. The measured value of 8.8 V (cf. Fig. 5.6) suggests that only ~10 nm of deflection occurred, *i.e.* the actual g_d is approximately 10 nm.

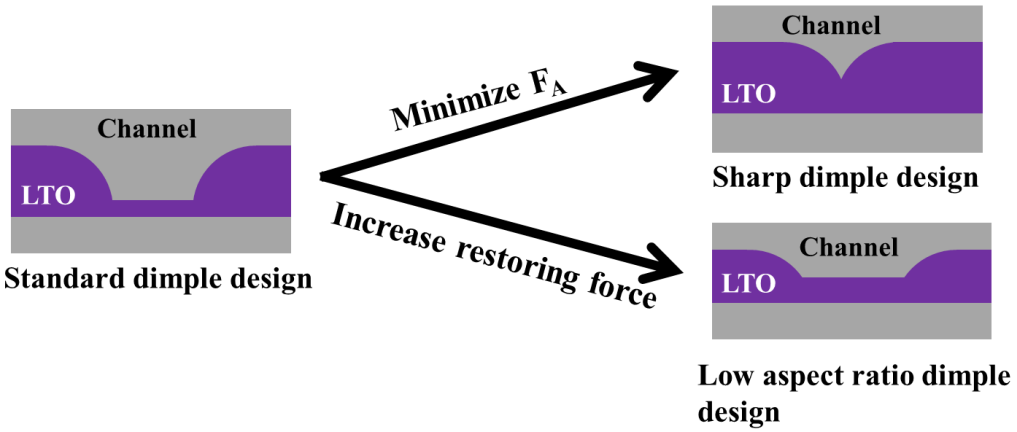


Fig 5.8 Proposed approaches to improve the contact dimple formation process

A second experiment was performed to fabricate relays with sharp contact dimples. Fig. 5.9 shows an SEM image of a fabricated device, which has minimal out-of-plane deflection as for the devices from the first experiment. Unfortunately no dimple structures are seen, which indicates that the thickness of the 2nd LTO layer was too thick, resulting in a planarized (non-dimpled) surface. Measured electrical characteristics are shown in Fig 5.10. A V_{PI} of 2 V is seen. Without contact dimples to serve as a stopper, the entire structure comes into contact with the bottom actuation electrode, resulting in a gate to source short instead of drain to source current. Since the contact area in this case is the entire actuation area, there is excessive adhesive force (800× larger than for two 50 nm-wide contact dimples) causing the relay to be stuck down.

The result of these NEM relay fabrication experiments indicate that the stress gradient of the thinner structural film can be sufficiently suppressed to achieve functional structures with 500× smaller footprint than the original prototype relays, and that the adhesive force of 50 nm-wide contact dimples should allow NEM relays to operate at voltages below 2 V.

Flexure Length (L)	2 μm
Flexure Width (W)	150 nm
Actuation Area (A_{OV})	4 μm^2
Actuation Gap (g)	70 nm
Dimple Gap (g_d)	NA
Structure Thickness (H)	0.1 μm
Dimple Width	NA

Table 5.3 Dimensions of the fabricated "sharp dimple" relay.

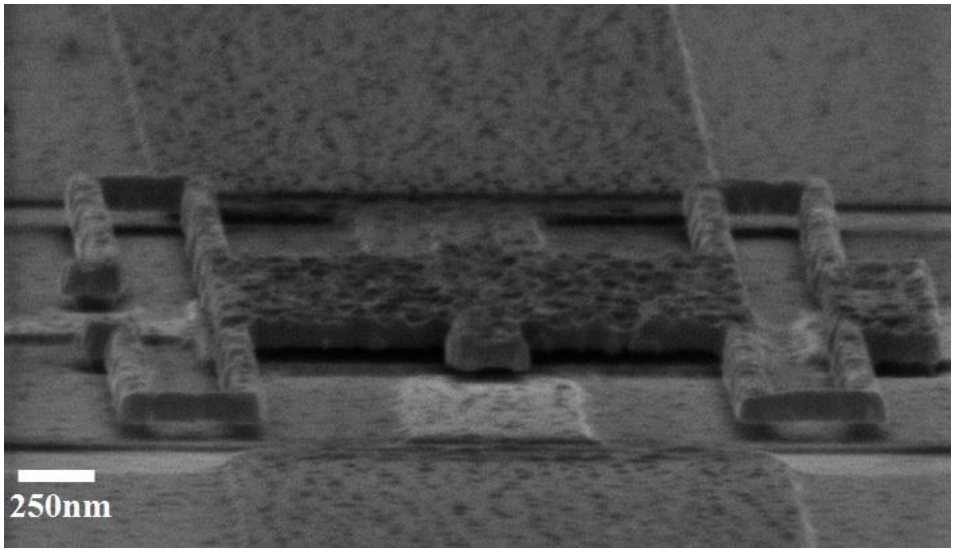


Fig 5.9 Tilted-view SEM of a fabricated "sharp dimple" NEM relay. There is little out-of-plane deflection, but no contact dimples are observed.

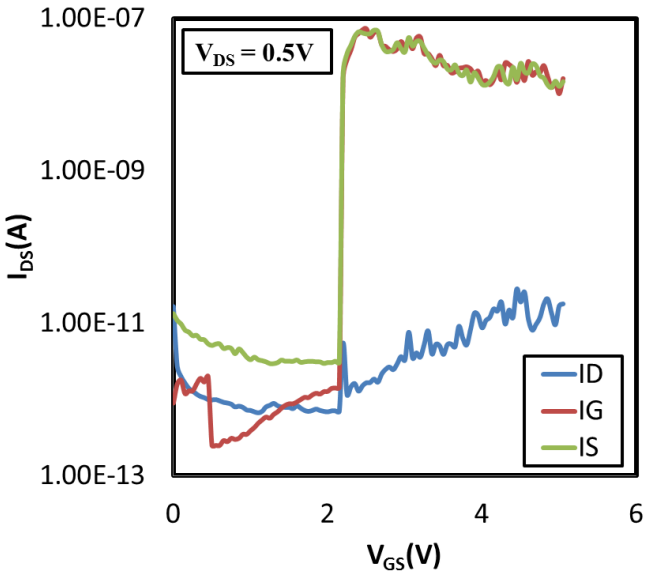


Fig 5.10 Measured I_{DS}-V_{GB} of a "sharp dimple" NEM relay. Gate to source current is observed with a V_{PI} of 2 V. No significant drain current is observed. V_D = 0.5 V.

5.4 Summary

Miniaturization is necessary to aggressively reduce the operating voltage and hence the switching energy of a relay. FEM simulations suggest that the vertically actuated planar relay design can be scaled to a footprint of ~10 μm^2 with an operating voltage of a few Volts. Building upon the work presented in previous chapters, scaled relays with 50 nm feature size and 100 nm-thick structural films were fabricated with 500× smaller footprint than the prototype relays shown in Chapter 2. The experimental results show that minimal out-of-plane deflection can be achieved reproducibly with thin structural films, providing for low operating voltage (< 2 V) even with a relatively small footprint (~ 25 μm^2). Further process refinement is needed to optimize the contact dimple formation steps in order to achieve properly functioning NEM relays.

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Chapter 6

Summary

Integrated circuit performance today is limited by chip power density constraints, so that improvements in energy efficiency are needed not only to achieve ever higher levels of functionality on a chip but also to reduce the power consumption of electronic devices in the age of mobile computing. To overcome the fundamental energy efficiency limit of CMOS transistors, researchers have proposed a variety of new switching devices [1] [2] [3]. One of the most promising candidates is a scaled mechanical relay, because of its ideal switching characteristics of abrupt on-off transition and zero off-state leakage current. A challenge for realizing the promise of mechanical computing is miniaturization. Most demonstrated relays to date have relatively large footprint ($10^6\times$ larger than a transistor) and high operating voltage (>10 V) [4]. Therefore, scaling is necessary to reduce the switching energy.

This thesis aims to elucidate challenges for NEM relay technology scaling. The next section summarizes the contributions of this work.

6.1 Contributions of This Work

In Chapter 2, the working principle of a vertically actuated MEM logic relay is reviewed with details of the pull-in voltage (V_{PI}), release voltage and switching energy. The fabrication process and measured electrical characteristics of prototype relays are presented. It is explained that contact adhesion caused hysteretic switching behavior ultimately sets the minimum switching energy of a relay. In the absence of contact adhesion, an ultimately scaled relay is projected to operate with less than 1 aJ of energy.

In Chapter 3, contact adhesion in the prototype MEM relays is investigated. It is found that van der Waals force is the main source of adhesion. The measured force per unit of apparent contact area is 0.02 nN/nm^2 for tungsten-tungsten contacts, which would dictate a minimum switching

energy greater than 10 aJ in an ultimately scaled relay. An ultra-thin oxide coating of TiO_2 deposited by atomic layer deposition is shown to be effective for reducing contact adhesion.

In Chapter 4, stress gradient optimization for thin poly-$Si_{0.4}Ge_{0.6}$ structural films is investigated. Post-deposition processing techniques such as thermal annealing and ion implantation are applied to reduce the strain gradient in a 100 nm-thick poly-$Si_{0.4}Ge_{0.6}$ film to less than 4×10^{-4} μm^{-1}. This film was used to realize a functional relay with lower V_{PI}. Variability is identified as a challenge for high-yield fabrication of scaled devices, which potentially could be reduced by employing an amorphous film as the structural material.

In Chapter 5, the fabrication of relays with 500× smaller footprint (50 nm minimum dimension) using electron-beam lithography is investigated. The 100 nm-thick poly-$Si_{0.4}Ge_{0.6}$ structural film developed in Chapter 4 is applied, and found to provide for relatively low pull-in voltage, ~2 V. Due to issues with the contact dimple formation steps, the devices were stuck down after turn on. Nevertheless, these experimental results suggest that a properly scaled NEM relay will be able to operate at voltage levels comparable to those for state-of-the-art CMOS transistors.

6.2 Suggestions for Future Work

6.2.1 Processes and Materials for NEM Relays

Chapter 3 concluded that contact adhesive force needs to be significantly reduced in order to achieve sub-aJ switching energy at scaled dimensions, which is not possible with Tungsten contacts or any other common metals. It was found that an ultra-thin oxide coating can be applied to reduce the adhesive force. Further studies should be conducted to identify the best surface coating material to mitigate adhesive force without significantly limiting current conduction, that can withstand 10^{15} cycles of operation [5]. The capability to deposit this material in monolayers and with perfect coverage is required. Although there have been many studies on ultra-thin surface coating for MEMS lubrication applications [6] [7] [8], none of these applications require current flow through the coatings, hence information on current conduction capabilities is lacking.

It was suggested at the end of Chapter 4 that amorphous metal is a promising candidate for the structural material. An atomic layer metal deposition process is necessary to achieve uniformly thin metal films with minimal stress gradient, scalable to thicknesses below 50 nm. An understanding of how material properties change with scaling is also important, as thin film properties can differ substantially from bulk material properties either due to thickness scaling or process condition change [9] [10]. Finally, the experimental results in Chapter 5 indicate that further process development is required to improve the manufacturing yield of NEM relays.

6.2.2 Reliability of Scaled NEM Relays

CMOS is the predominant technology for very large scale integrated circuits (ICs) not only because of it offers excellent device performance but also because it has high manufacturing yield and device reliability. State-of-the-art CMOS device lifetime can be 10 years, with failure

modes and accelerated testing methods well understood [11]. From a product perspective, any new semiconductor devices also need to have these other properties to be practical for IC applications.

Tungsten oxidation resulting in increased contact resistance can limit the practical operating lifetime of a relay [12], to ~10^9 cycles. Although the mechanism is known, it is unclear how it changes as device contact size aggressively scales, or when ultra-thin coating is applied for mitigating adhesive force. If oxidation can be reduced with hermetic packaging [13], the lifetime limiting mechanism may change [14]. The failure modes of NEM relays require further study, and accelerated lifetime testing methods need to be established.

6.2.3 Improved Relay Layouts

In order to achieve low operating voltage, the actuation area cannot be too small. As a result, the footprint of a relay is larger than that of a CMOS transistor at the same technology node ($144F^2$ to ~$30F^2$). This issue can be mitigated by 1) adding in extra source, drain or gate contacts [15] [16] (which adds < 10% to the footprint but adds significant functionality to the device), or 2) optimizing the circuit topology to reduce the number of switching devices needed to implement a function [17].

The "crab" relay design comprising a plate suspended by folded-flexure beams was adopted due to its robustness against the effects of residual stress. It also has the benefit of distinct actuation and spring portions of the structure, which makes it very easy to analyze (as it can be modeled as a spring connected to a parallel plate capacitor). To minimize the relay footprint, cantilever beam structures [18] [19] (which combine the actuation plate and spring) could be considered. An example of such a structure is shown in Fig. 6.1 and Fig. 6.2. It mainly comprises a cantilever beam anchored at one end, with the gate oxide and metal channels formed along the sidewalls of the beam using spacer technology, a double-patterning technique used in CMOS processes [20] to achieve feature sizes smaller than the lithographic resolution limit. The footprint of this relay can be as small as $20F^2$ (where F is the minimum feature size that can be printed using lithography), comparable to a CMOS transistor. A possible fabrication process flow is illustrated in Fig. 6.3.

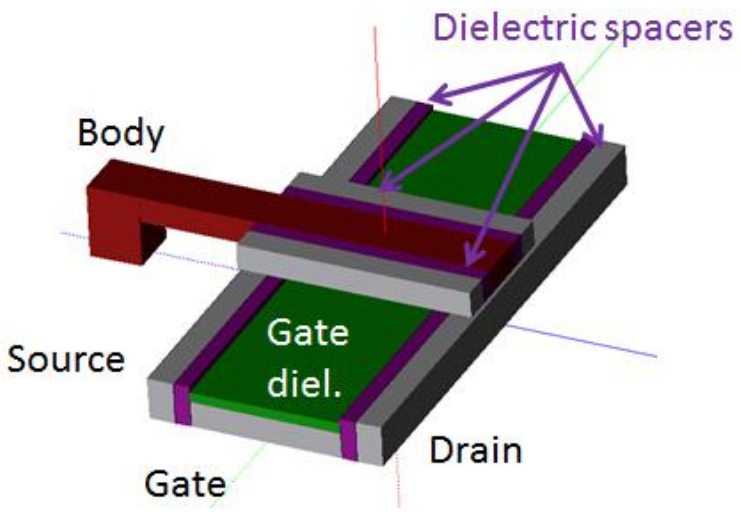

Fig 6.1 Schematic of a cantilever beam NEM relay device.

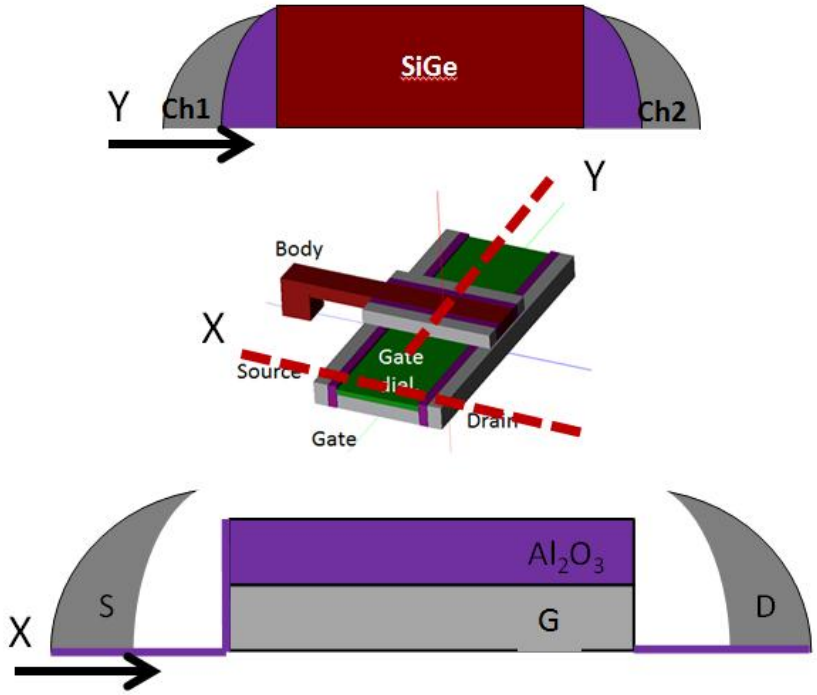

Fig 6.2 Cross-section of the proposed cantilever beam relay. Top: Cross-section of the cantilever beam, Bottom: cross-section of the bottom gate stack and source/drain electrodes. The metal channels and source/drain electrodes are fabricated using spacer processing.

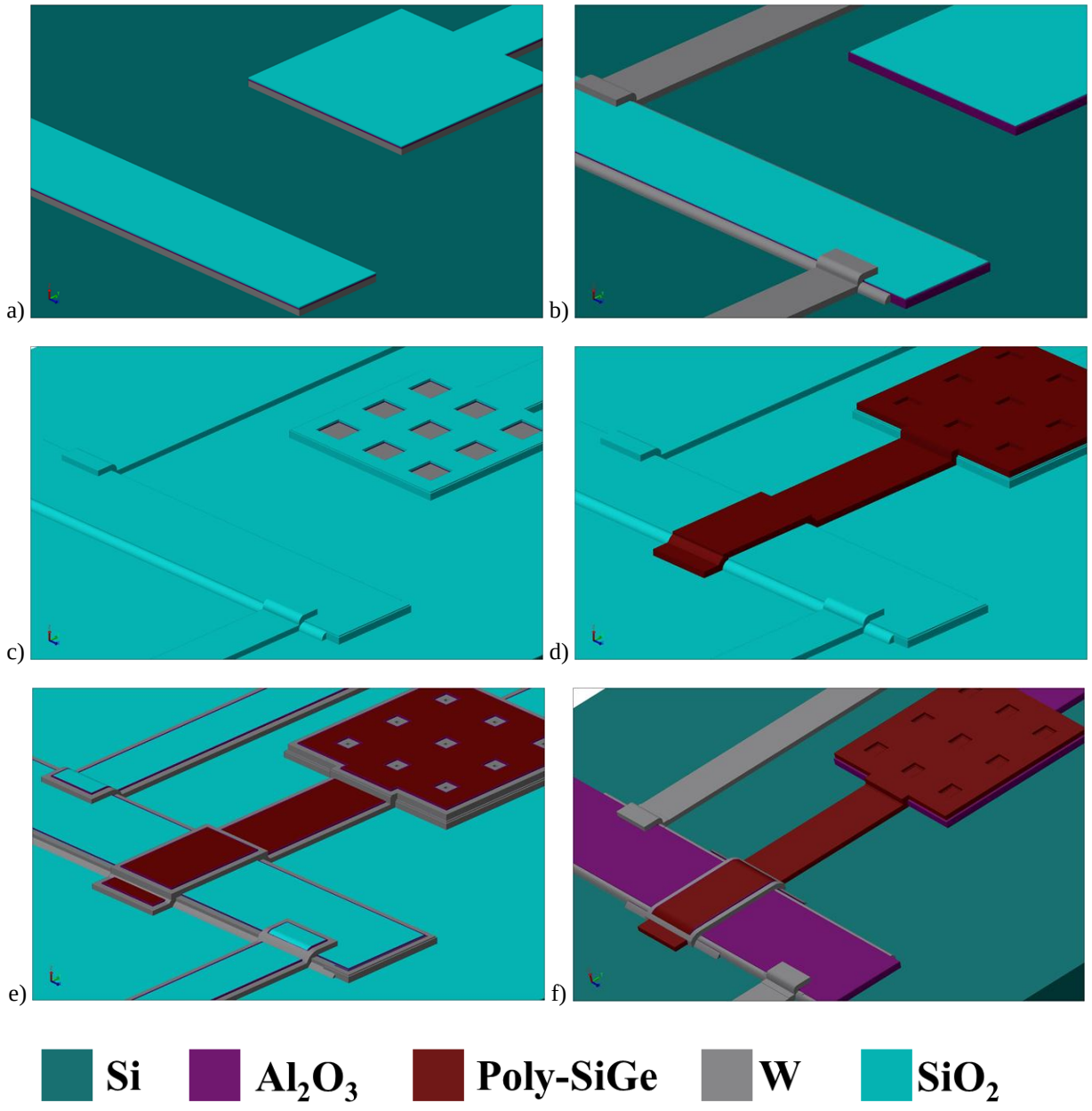

Fig 6.3 Proposed fabrication process of the NEM cantilever relay. a) Deposition and patterning of gate stack. b) Deposition and patterning of insulating oxide and source drain spacers, while patterning metal interconnects. c) Sacrificial layer deposition and via etch. d) Structure deposition and patterning. e) Insulating oxide and metal channel spacer deposition and patterning. f) Release etch.

6.3 References

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