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Printed Organic Circuits for Reading Ferroelectric Rewritable Memory Capacitors

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(Invited Paper)

***Abstract*— We demonstrate an inkjet-printed organic thin-film transistor (OTFT) circuit for reading ferroelectric (FE) nonvolatile rewritable memories. With the large difference in polarization charge between FE memory states, we implement a single-OTFT gain stage with latch and show that a gain of −2.8 is sufficient to distinguish memory states. This paper evaluates the effect of device variations on the yield of this readout circuit.**

***Index Terms*— Ferroelectric (FE) memory, inkjet printing, organic thin-film transistor (OTFT).**

I. Introduction

MEMORY is an essential component in many electronic systems [1]–[3], but most implementations of organic thin-film transistor (OTFT) circuits for memory data retrieval have been limited to nonrewritable resistive memories [1] or volatile SRAM [4]. Because of the challenges in implementing precise, high-gain circuits in OTFT technologies, conventional silicon electronics have been used to read rewritable nonvolatile organic memory arrays [5]–[8], losing the cost and form-factor advantages conferred by organic circuits. Common silicon memory readout circuits, such as an op-amp charge amplifier or a Sawyer-Tower comparator, are challenging to realize in OTFT technologies because of low mobility, device mismatch, and bias stress. Leveraging a design approach based on the consideration of the specific characteristics of OTFT processes, we demonstrate an inkjet-printed OTFT circuit for reading ferroelectric (FE) nonvolatile rewritable memories. Noting that high gain is not required for the readout circuit, due to the large difference in polarization charge between FE memory states, we implement a readout circuit based on a single-OTFT gain stage. The circuit uses a few OTFTs, which leads to higher yield, and does not require matching.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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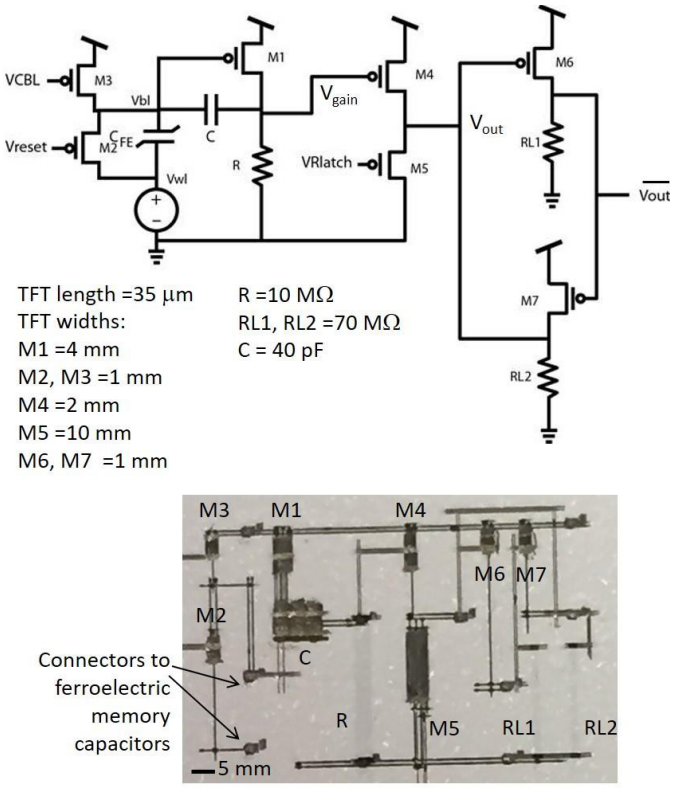
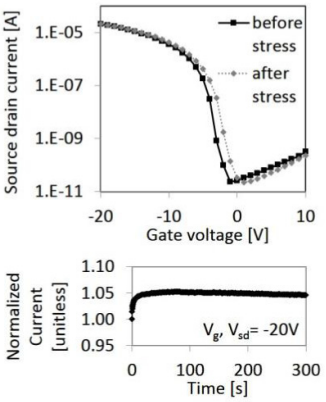


Fig. 1. Circuit schematic and photograph of the FE memory readout circuit on plastic foil.

II. Experimental Methods

A. Circuit Design

The readout circuit in Fig. 1 is designed for discriminating between memory states of an organic FE capacitor C_{FE} using the switching voltage of 20 V. The memory bitline V_{bl} is connected to the gate of a common-source gain stage, comprising OTFT *M1* and resistor *R*. *M2* is for zeroing the read circuit and *M3* allows for writing the memory cell [9] and is switched OFF in the readout process. V_{CBL} is gate voltage to *M3* to control the memory bitline voltage. V_{CBL} is normally high and is set to low during memory writes. The readout circuit is operated through the application of a positive voltage pulse on the memory wordline V_{wl}. This pulse discharges the memory cell with a memory-state-dependent charge, which is integrated on feedback capacitor *C* of the gain stage. The gain stage output V_{gain} is sent to a latch comprising OTFTs *M6* and *M7* and resistors *RL1* and *RL2*. Devices in the latch and gain stage are sized, such that the latch threshold is midlevel between



V_T [V]	Before bias stress	After bias stress
mean	-1.59	-0.75
max	0.33	0.80
min	-2.26	-1.58
Std dev	0.76	0.77

Mobility [cm²/Vs]	Before bias stress	After bias stress
mean	0.61	0.60
max	0.70	0.66
min	0.52	0.45
Std dev	0.05	0.05

Fig. 2. Top-left: transfer characteristics of a typical OTFT using p-type semiconductor, before and after 5-min bias stress at gate voltage $V_{gs} = -20$ V and source–drain voltage $V_{sd} = -20$ V. The channel width is 500 μm. Bottom-left: current change over time during bias stress. Right: extracted parameters of 15 OTFT samples before and after bias stress.

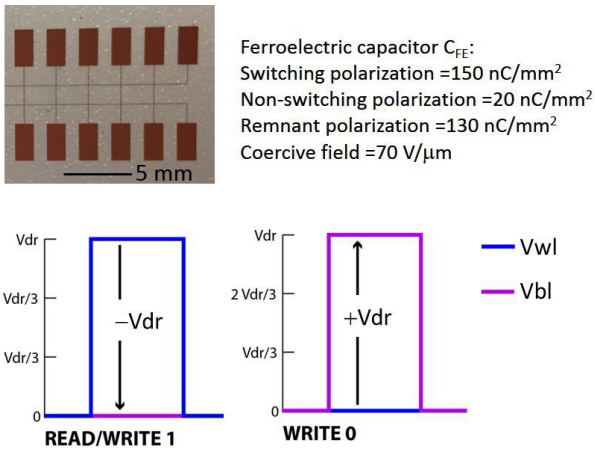


Fig. 3. Top: photograph and characteristics of the FE memory capacitors on plastic foil. Bottom: voltage input to memory wordline and bitline during the write 1/read/reset or the write 0 process.

the voltage on V_{gain} resulting from a 0 or a 1 memory state. Depending on the state of the memory, the V_{gain} signal either does or does not fall below the latch threshold. In this way, the latch discriminates between the memory states and provides a stable digital output V_{out}. Before each read event, the circuit is reset through *M5* with a low signal on V_{Rlatch}, which is held high in operation.

As in conventional electronics, SPICE simulations provide understanding of the impacts of sizing in OTFTs, resistors, and capacitors on the circuit performance, and help determine tolerance to device variation, which is significant in printed circuits. Here, we used Tanner T-Spice (Mentor Graphics). In this design, divergence from the nominal design by a factor of 2 in resistance and gate width in individual resistors and OTFTs, respectively, does not compromise circuit functionality. Varying the feedback capacitor C in the gain stage requires a tradeoff. Larger C reduces the bitline voltage V_{bl} during readout, more fully discharging the FE memory. However, it leads to lower gain and reduced discrimination at V_{gain}. To maximize the ability to read the memory, it is preferable to use a smaller capacitor. This means that the memory may be only partially erased after reading, and a separate rewrite operation to reset the FE memory to either state. The circuit

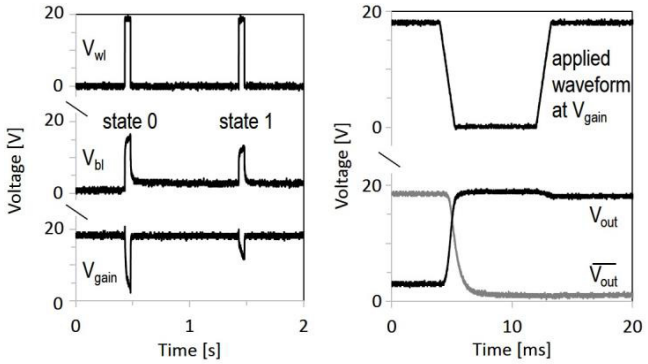


Fig. 4. Left: signals measured at the gain stage during the read process. Right: measured response of the latch to a negative pulse on V_{gain}. The latch trigger threshold is 7 V.

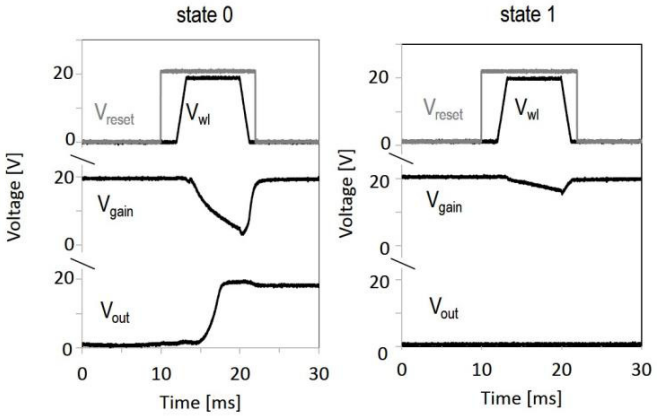


Fig. 5. Signals measured at nodes V_{gain} and V_{out} during reading of the 0 or 1 memory state.

operates correctly if the latch OTFTs *M4* and *M6* deviate from nominal value by a factor of 0.5–2. The greatest sensitivity is to the resistor values in the latch, requiring matching to within ± 10 MΩ or $\pm 14\%$ of the nominal value of *RL1* and *RL2* = 70 MΩ.

B. Fabrication

We print the readout circuit monolithically using inkjet on plastic polyethylene naphthalate substrates. This circuit uses a single OTFT polarity, which reduces the number of fabrication steps compared with complementary designs. The p-channel OTFTs are chosen as they generally have higher mobilities and are more stable than n-channel OTFTs [10]. The semiconducting polymer [11] is purchased from Flexink and patterned by inkjet. The transistor electrodes are inkjet-printed [12]–[14] from silver nanoparticle dispersion (colloidal ink). The gate dielectric is a bilayer with a Teflon layer next to the semiconducting layer and a high-k PVDF-TrFE-CTFE polymer (Piezotech). Fig. 2 shows the transfer characteristics of a typical OTFT before and after bias stress. For a supply voltage of 20 V, the threshold voltage (V_T) shifts <1 V for 5 min of continuous bias stress. The rise in current during the first 30 s of operation is caused by slow polarization of the PVDF terpolymer high-k relaxor dielectric; thereafter,

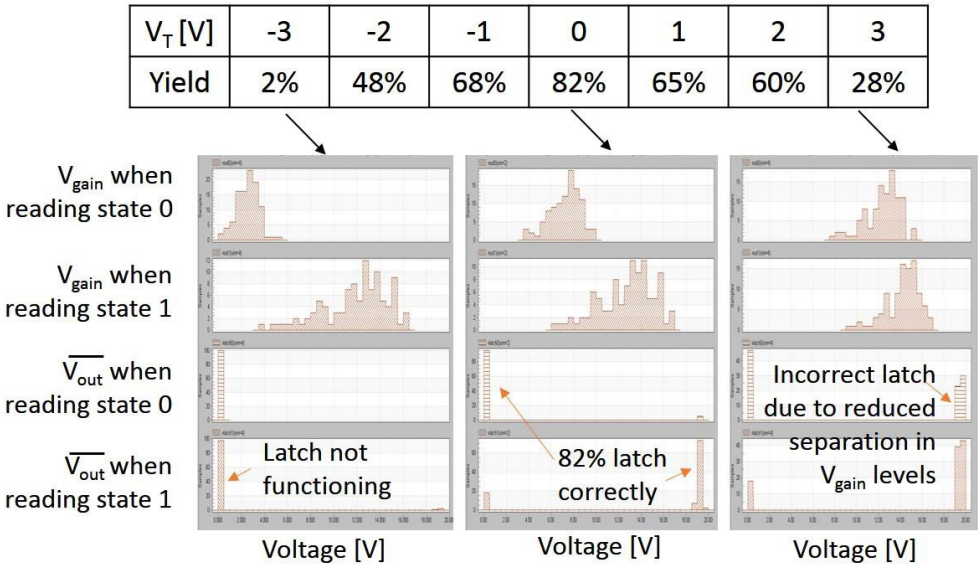


Fig. 6. Monte Carlo analysis histograms of 100 samples, where the OTFT width is varied with 25% standard deviation and a constant V_T is applied to all OTFTs.

the current decreases with a stretched-exponential characteristic. The change in current due to bias stress is small relative to variation among devices, for which the maximum/mininum values for parameters, such as mobility and V_T, can be 0.67–1.5 times of the mean value.

The memory capacitors in Fig. 3 are cross-bar structures with area of (100 μm)^2 and a PVDF-TrFE copolymer as the FE dielectric. The memories are patterned by gravure printing or photolithographic process [9]. If the FE capacitor size is reduced, the gain stage components are resized accordingly. The FE memories are externally connected to the readout circuit via silver paste interconnects. A memory cell is written to the 0 or 1 state, respectively, by the application of a positive or negative potential across the capacitor; by convention, the potential polarity is relative to the wordline electrode. In the read process, the memory state is discerned by measuring the quantity of charge released during the application of a negative potential $-V_{\rm dr}$ (positive pulse on $V_{\rm wl}$), with more charge released for a 0 state than for a 1 state. Since the potential applied during read would also set the cell to the 1 state, this is a destructive read process. Here, the readout process is demonstrated with a single FE element, but the same procedure also works on passive matrix arrays [9].

III. Results and Discussion

Fig. 4 shows the measured results for the gain stage and the latch stage. At the gain stage, a clear difference between the $V_{\rm gain}$ values is seen for opposite polarization states. Reading the 0 state results in 15 V on $V_{\rm bl}$ which leads to 2.5 V on $V_{\rm gain}$. Reading the 1 state results in 12 V on $V_{\rm bl}$ and 11 V on $V_{\rm gain}$. The ratio $\Delta V_{\rm gain}/\Delta V_{\rm bl}$ gives an effective gain of -2.8. Following the gain stage, the latch is designed to set $V_{\rm out}$ in a low state when reading a 1 and a high state when reading a 0. In Fig. 4, the trip point for resetting the latch is 2.5 V at $V_{\rm reset}$, and the trigger threshold voltage to switch the latch is 7 V at $V_{\rm gain}$. These values can be modified by varying the relative sizes of the latch TFTs *M4* and *M5*. Due to device variations, trigger voltages for this readout circuits may range between 7 and 9 V. Fig. 5 shows the comparison of the signals at nodes $V_{\rm gain}$ and $V_{\rm out}$ during reading of the 0 or 1 memory state. The latch output switches upon reading a memory cell with state 0, whereas the output remains at the low value when the memory state is 1. Thus, the single-OTFT gain stage with latch circuit is demonstrated to properly distinguish between the memory states. One characteristic of this circuit is that it does not require high gain. A gain of -2 is sufficient to distinguish memory states. Higher gain circuits, however, would be more robust to variations in the $V_{\rm gain}$ levels and in the latch trigger threshold. This implementation uses 35-μm channel length, but smaller features in the future will improve speed.

Monte Carlo analysis is carried out to evaluate the effect of device variations and threshold-voltage (V_T) shift on yield. Each Monte Carlo simulation includes 100 circuit runs, with independent variation of either the channel width or the effective threshold voltage, simulated as a voltage source in series with the OTFT gate. Variations are defined by normal distributions with equal standard deviations (σ) normalized to the nominal designed parameter value. Fig. 6 shows the analysis histograms, where the OTFT width is varied with $\sigma = 25\%$. A constant V_T is assumed for all OTFTs, as V_T tends to vary batch-to-batch, and not device to device. The V_T shift results in mismatch between the latch trigger threshold and the gain-stage output. In particular, batch-to-batch shifts over a 5 V range can lead to circuit yields ranging from 28% to 82% on individual batches. With positive V_T shift, the two $V_{\rm gain}$ distributions have very little separation. With negative V_T shift, the distributions of $V_{\rm gain}$ are fairly broad, and the latch does not function properly. For a boundary

condition of V_T shifted to -2 V, we run the above analysis with $\sigma = 10\%$ or 5% of nominal values. In these cases, the distribution of V_{gain} voltages is tighter and the yield reaches 80% and 98%, respectively, in the $\sigma = 10\%$ or 5% case. These statistics provide the boundary target for future device development.

IV. Conclusion

In summary, the polarization states of FE memory cells are distinguished with a printed readout circuit consisted of a single-OTFT gain stage and a latch stage. The circuit uses minimum number of OTFTs and tolerates variations up to 1.5 times of the nominal value in transistor transconductance.

References

[1] K. Myny *et al.*, "8b thin-film microprocessor using a hybrid oxide-organic complementary technology with inkjet-printed P^2ROM memory," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 486–487.

[2] V. Fiore *et al.*, "A 13.56MHz RFID tag with active envelope detection in an organic complementary TFT technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, vol. 57. Feb. 2014, pp. 492–493.

[3] P. Heremans, G. H. Gelinck, R. Müller, K.-J. Baeg, D.-Y. Kim, and Y.-Y. Noh, "Polymer and organic nonvolatile memory devices," *Chem. Mater.*, vol. 23, no. 3, pp. 341–358, 2010, doi: 10.1021/cm102006v.

[4] K. Fukuda *et al.*, "A 4 V operation, flexible braille display using organic transistors, carbon nanotube actuators, and organic static random-access memory," *Adv. Funct. Mater.*, vol. 21, no. 21, pp. 4019–4027, Nov. 2011.

[5] T. Sekitani *et al.*, "Organic nonvolatile memory transistors for flexible sensor arrays," *Science*, vol. 326, no. 5959, pp. 1516–1519, 2009.

[6] R. C. G. Naber, K. Asadi, P. W. M. Blom, D. M. De Leeuw, and B. De Boer, "Organic nonvolatile memory devices based on ferroelectricity," *Adv. Mater.*, vol. 22, no. 9, pp. 933–945, Mar. 2010.

[7] S. Nau, C. Wolf, S. Sax, and E. J. W. List-Kratochvil, "Organic nonvolatile resistive photo-switches for flexible image detector arrays," *Adv. Mater.*, vol. 27, no. 6, pp. 1048–1052, 2015.

[8] T. Lee and Y. Chen, "Organic resistive nonvolatile memory materials," *Mater. Res. Soc. Bull.*, vol. 37, no. 2, pp. 144–149, 2012.

[9] T. N. Ng *et al.*, "Scalable printed electronics: An organic decoder addressing ferroelectric non-volatile memory," *Sci. Rep.*, vol. 2, p. 585, Aug. 2012.

[10] J. E. Anthony, A. Facchetti, M. Heeney, S. R. Marder, and X. Zhan, "n-type organic semiconductors in organic electronics," *Adv. Mater.*, vol. 22, no. 34, pp. 3876–3892, Sep. 2010.

[11] D. Venkateshvaran *et al.*, "Approaching disorder-free transport in high-mobility conjugated polymers," *Nature*, vol. 515, no. 7527, pp. 384–388, 2014.

[12] T. N. Ng *et al.*, "Pulsed voltage multiplier based on printed organic devices," *Flexible Printed Electron.*, vol. 1, no. 1, p. 15002, 2016.

[13] T. N. Ng *et al.*, "Printed dose-recording tag based on organic complementary circuits and ferroelectric nonvolatile memories," *Sci. Rep.*, vol. 5, p. 13457, Aug. 2015.

[14] R. A. Street *et al.*, "From printed transistors to printed smart systems," *Proc. IEEE*, vol. 103, no. 4, pp. 607–616, Apr. 2015.

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Christer Karlsson, photograph and biography not available at the time of publication.