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INTEGRATED CIRCUIT READOUT FOR CLOSELY SPACED WIRE ARRAYS

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ABSTRACT

We review some of the recent advances in solid-state circuitry which permit the readout of large arrays of closely spaced wires. We present a scheme that allows charges as small as 10^{-13} coulomb to be read from lines spaced 63 microns apart. Projected chip cost is 30 cents/line.

1. INTRODUCTION

For many applications of multiwire particle detectors, it is sufficient to periodically scan the wires and reduce the readout to a single data line. Recent advances in the large-scale integration of solid-state circuits make possible the automatic scanning of large arrays of closely spaced wires.

By "scanning" a multiwave particle detector, we mean that the charged lines are interrogated sequentially, to determine whether they have gained any charge since the last time they were scanned. This is different from the faster but more expensive scheme of having only the charged lines transfer their charge information and location.

In this paper we describe a large-scale integration switching device currently used in conjunction with a photodiode array. A rather small modification of the production mask would enable it to be used as a self-scanned array to switch 128 wires spaced on 0.005-in. centers, at a frequency of 1 to 10 MHz. The device uses FET gates and has a switching noise below 10^{-13} coulomb, making it suitable for reading out multiwave detectors in which a noble liquid is used. It may also be useful for other detectors in which the charge developed is above 1 picocoulomb. The projected cost if the chips are purchased in quantities is 30 cents/line.

For the purpose of proportional mode readout, we also describe a different scheme using what is called a "bucket-brigade

storage device." This circuit provides a temporary storage of the analog charge from each wire, and obviates the need for a fast and expensive analog-to-digital converter.

When better time resolution is required, an additional scheme can be used incorporating fast switches, storage capacitors, and a scanned readout. The time resolution could be made less than 100 nsec.

2. READOUT BY SCANNING

Readout by scanning requires a relatively simple electronic gating system which can be integrated on a single chip with small spacing between adjacent gates. The anode wires are scanned after the passage of a nuclear particle, and the serial information of charge location (and magnitude) appears on a single output line. In order to process the high rate of information at say, 1 to 10 MHz, a buffer storage register can be used until the computer is ready to read the data into its memory. This allows us to "freeze" the track information after isolating it from the chamber wires.

Unless an additional gating is provided (see Section 4), the time resolution involved is the time required to go through one scan cycle. Our design is based on the requirements of the proposed noble liquid detector[1,2] in which the distance between adjacent conductors is on the order of a few thousandths of an inch.

A useful electronic rotary switch would be a monolithic device in which the spacing between the bonding pads (input con-

nections) is close to typical spacing between the detector wires. The design should also allows several chips to be connected in series so that they can act as a single larger chip, scanning thousands of wires. The single chip described accommodates only 128 wires or less. The switching characteristics should produce a minimum of noise at the single output connection.

3. UTILIZATION OF A SELF-SCAN ARRAY

An "electronic rotary switch" can be easily constructed with any of the 8- or 16-channel multiplex switches shown in Table I. Such switches can be constructed to service many wires, as shown in Fig. 1. The number of lines that can be serviced per scaler (up-counter) is determined by the size of the scaler. Due to high cost per line and packaging difficulties, this system would be suitable only for a small number of lines (say, several hundred) and spacing not smaller than 1 mm. A charge level of 1 to 100 picocoulomb, such as in the noble liquid detector, will provide a signal well above the switching noise seen at the common amplifier.

By utilizing the large-scale integrated (LSI) circuit technology, it is possible to produce a monolithic device that would employ the principle shown in Fig. 2. In this device the driving circuit and the switching gates are all integrated on one chip, and the detector wires are bonded to the bonding pads on the chips.

A self-scanned array such as that shown in Fig. 2 can be produced by many manufacturers of integrated circuits. Since the

application is intended for many thousands of wires, we have the incentive to reduce the cost per line as low as possible. At the same time we require a large array and small spacing between wires. A practical limit for the size of the chip considering the state of art is about 0.5 in. The spacing between wires is limited by the convenient size of the bonding pads and by the "ON" resistance, which must be low for quick drain of the charge the wire. A reasonable spacing range would be 0.004 – 0.007 in.

Mr. Don Peters of Siliconix[7] indicated that his company has the capability and the interest in manufacturing such a self-scanned array on short notice. For a production run of 5000 to 10 000 chips in the first year, the cost is expected to be on the order of 20 to 30 cents per line in an array of 128 lines.

Recently, a promising device became available from Fairchild Semiconductors.[3] The Fairchild FPA600, is a linear array of 48 photodiodes on 0.005-in. centers. Each photodiode has associated with it a silicon field-effect transistor. Integrated into the same silicon chip is a two-phase dynamic shift register used to sequentially read out the photodiodes at 1 MHz. This device could satisfy many of our needs provided a metallic bonding pad could be made in place of the photodiodes. From the discussion with the designer of the device, Mr. Gene Weckler of Fairchild, it appears that a rather minimal alteration of the production mask would provide these bonding pads. A modified FPA600 is shown in Fig. 2.

4. HIGH TIME-RESOLUTION SCHEME

When a narrow time-window readout is required,[8] the self-scanned array can be used in conjunction with a window-generating array (see Fig. 3). A bleeding resistor combined with the chamber wire capacitance provides a memory long enough for a subsequent evaluation of the event, (say 100–500 nsec). When an event of interest is detected, A is turned ON. In this condition, the charge received by the wire is shared with the storage capacitor. After ~100 nanoseconds, A is turned OFF and the charge can be read by the self-scanned array.

The time resolution possible with a P-channel enhancement mode MOS FET transistor is less than 100 nsec. By assuming a 0.1-pA leakage current in the OFF position and a 10 pC charge on the storage capacitor in the window-generating array module, one would expect a charge leakage time constant of 100 sec, much longer than any storage time needed in practice.

In Fig. 5, the window-generating array is shown as a monolithic device separated from the self-scanned array. This separation is done with the consideration that a self-scanned array is a general device and its development cost can be distributed over many applications.

5. PROPORTIONAL COUNTER READOUT

When operating in a proportional counting mode, in which the charge level on the wire is proportional to the energy loss of the incoming particle, we would like to store the analog charge level. When a scanned readout is used, the data comes out serially at a rate of say 1 MHz.

Two ways of storing the analog data are considered here:

1) Direct storage of the charge data on a wide band instrumentation taperecorder preserves both timing and pulse-height information. This is done by synchronous operation of the tape and the driving frequency. The driving frequency must be lower than the frequency response of the taperecorder used. Taperecorders of 2-MHz response are readily available.

In an application where the detector is scanned at large intervals (on the order of seconds or more) and the stopping and starting of the taperecorder is not practical, an analog disc recorder can be used (Ampex[9] corporation produces up to 12-MHz disc recorders). Here the data generated during each scan cycle is dumped on a single track which can store a string of data 16-msec. long; then the recording head moves to the next track, ready to accept another string of data. 900 tracks per disc are available.

2) The data is processed by analog-to-digital conversion and the binary information is transferred to memory. However, an

A/D converter operating at 1 MHz is rather expensive and requires complicated fast control logic. We can avoid this difficulty by utilizing a newly developed analog shift register made by Philips,[5] known as a Bucket-Brigade circuit (see Fig. 4).

The wires are scanned at 1 MHz and the charge is shifted into the Bucket-Brigade circuit for temporary storage. Now there is sufficient time to interrogate each analog register, using a slow less-expensive analog-to-digital converter. An A/D converter operating at 10 kHz may cost an order of magnitude less than one running at 1 MHz. Or, a fast A/D converter can now be time-shared by many self-scanned arrays.

F. J. Sangster of the Philips Corporation[4] reports storage of 1 second on a 72-stage register without appreciable loss of charge. The charge is stored in an array of capacitors not directly as a charge level but rather as a charge deficit. The capacitor is an enlarged parasitic Miller capacitance of the series-connected transistors. This scheme provides very little degradation of the original charge level on each capacitor. (See Ref. 4 for complete explanation).

6. ORGANIZATION OF COMPUTER INTERFACE

One possible organization of a complete readout scheme for self-scanned array is shown in Fig. 5. Here we want to know only what line was struck and not the amount of charge deposited. For

the purpose of demonstration we use the Fairchild FPA600, although any of the other devices shown on Table I could be employed.

Let us assume we have a detector made of 4608 wires, using 96 modified FPA600 devices or 48 serial pairs. A start signal from the computer (or external source) starts driving the series-connected arrays at 1 MHz. This causes an integrated 96-bit register (such as the Plessey MP 225B, Ref. 6) to be loaded with bits corresponding to the state of charge of the wires. At the end of the 96-microsecond cycle this information is waiting to be serially read into the computer.

A typical cycle time of a small computer is between 0.8 and 1.5 μsec. Assuming a 1-MHz computer with 16 data lines, it will take 288 μsec to put all the data into memory. Maximum size of the data block is based on one bit per wire, or 4608 bits. This means that only 1/15 of the memory of a 4-K 16-bit computer is utilized for data storage.

The logic design would be extremely simple in an experiment where the count rate is low, such as a cosmic ray experiment. Because of the low count rate, time permits all the detector wires to be read sequentially, and sent directly to the computer. This means that all the self-scan devices (such as the FPA 600) can be connected serially and a continuous string of data can be sent directly into memory.

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3. Fairchild Microwave and Photoelectronics, 2513 Charleston Road, Mountain View, California.
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5. Philips Corporation, represented in the U. S. By Amperex.
6. Plessey Co., LTD., Microelectronics Div., London, England.
7. Siliconics, 2201 Laurelwood Road, Santa Clara, California.
8. Richard A. Muller, Stephen E. Derenzo, Robert G. Smits, Haim Zaklad, and Luis W. Alvarez, Lawrence Radiation Laboratory Report UCRL-20135, 1970; published in Proceedings of the International Conference on Instrumentation for High Energy Physics, Dubna, 1970.
9. Ampex Corporation, Redwood City, California.

Table I. Comparison of some multiplex switches.

	Number of channels	Switching time (μsec)	Off resistance (G Ω)	Data input leakage current (nA)	Data input capacitance (pF)	Minimum detectable signal (pC)	Package size	Price per chip (in quantity)
Fairchild 3705	8	1	1.5	3 (at 15 V)	7.5		16 lead dual in line	$20
Motorola MC 1150L	8	2	1	15 (at 10 V)	3		16 lead dual in line	$20
National Semiconductor MM-4503 (preliminary)	8	1	100	0.025 (at 10 V)	10		16 lead dual in line	$25
Radiation Inc. RS-1000	16	1	0.5	0.03	4.0		28 lead	$80
Fairchild FPA 600, modified	48 (128-?)	1		0.0001		0.02	special	$100[a] (estimated projection)

[a] Siliconix cost projection for a similar chip is about $30 for 128 lines.

FIGURE LEGENDS

Fig. 1. Series connection of 2-multiplex switches.

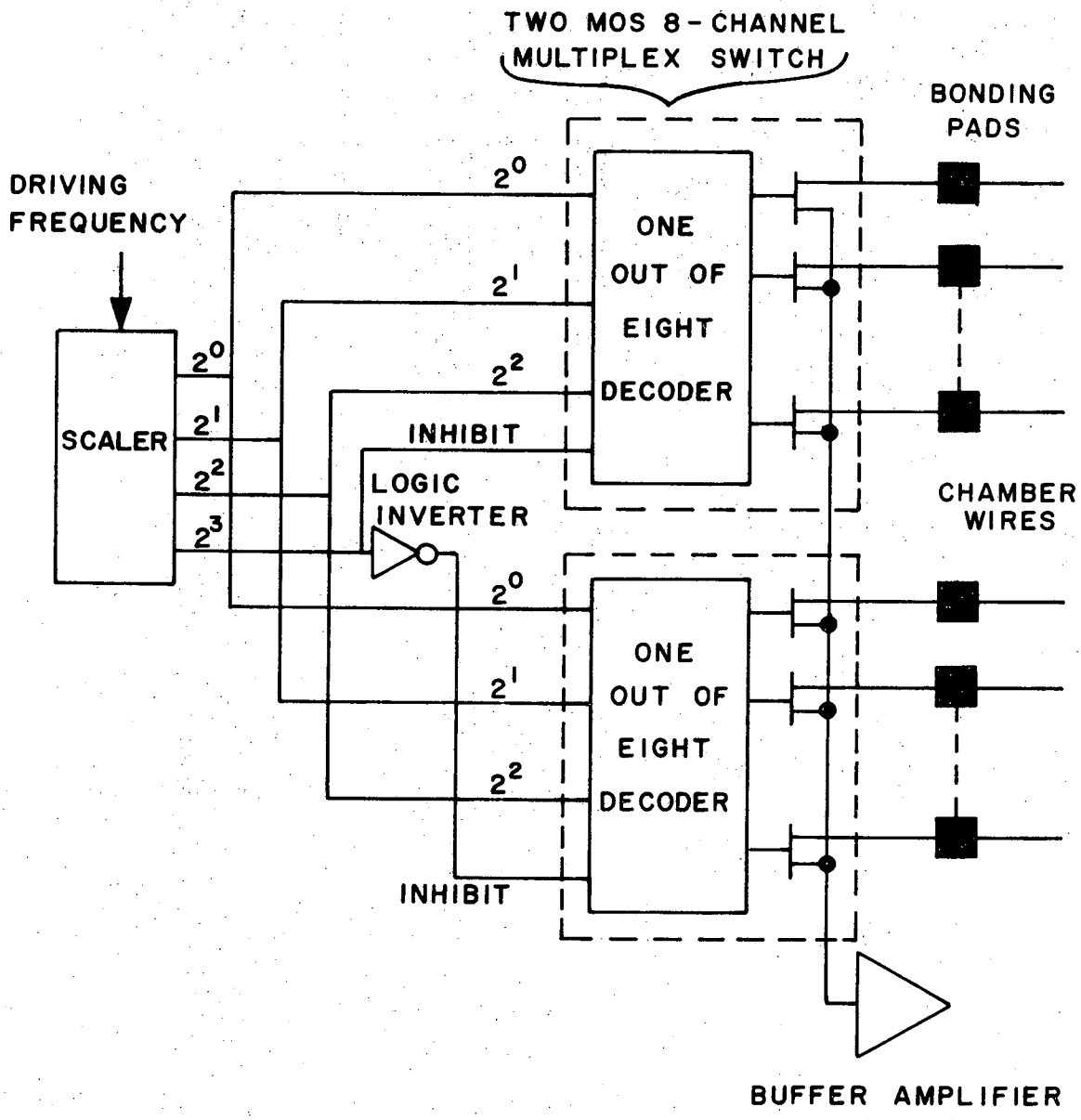
Fig. 2. Self-scanned switching array circuit diagram.

Fig. 3. Narrow time-window scheme.

Fig. 4. Analog information readout.

Fig. 5. An example of computer interface organization.

SERIES CONNECTION OF TWO MULTIPLEX SWITCHES



XBL 708-1958

Fig. 1

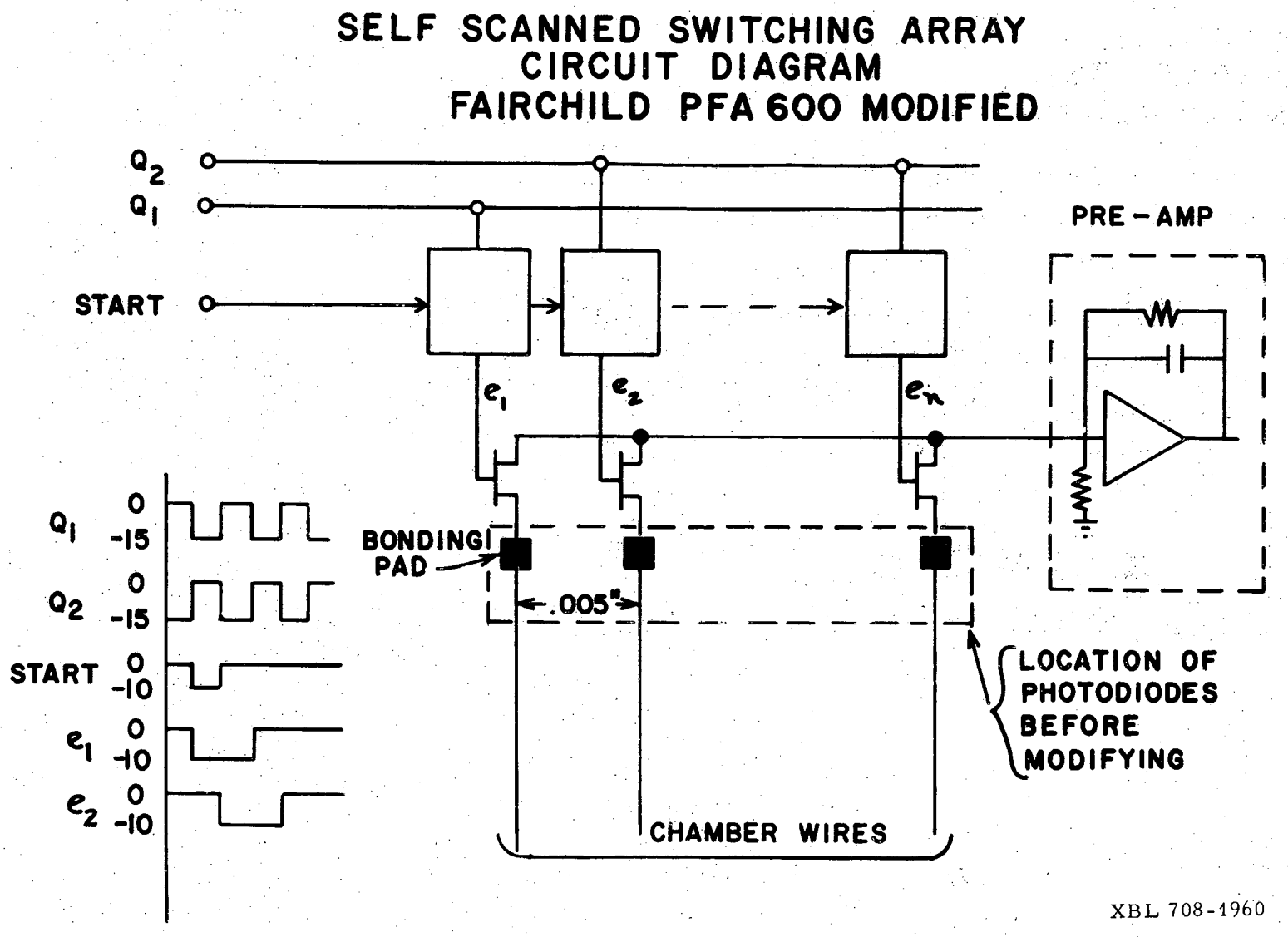

SELF SCANNED SWITCHING ARRAY
CIRCUIT DIAGRAM
FAIRCHILD PFA 600 MODIFIED
Q2
Q1
START
PRE-AMP
e1
e2
en
Q1 0 -15
Q2 0 -15
START 0 -10
e1 0 -10
e2 0 -10
BONDING PAD
.005"
LOCATION OF PHOTODIODES BEFORE MODIFYING
CHAMBER WIRES
XBL 708-1960

Fig. 2

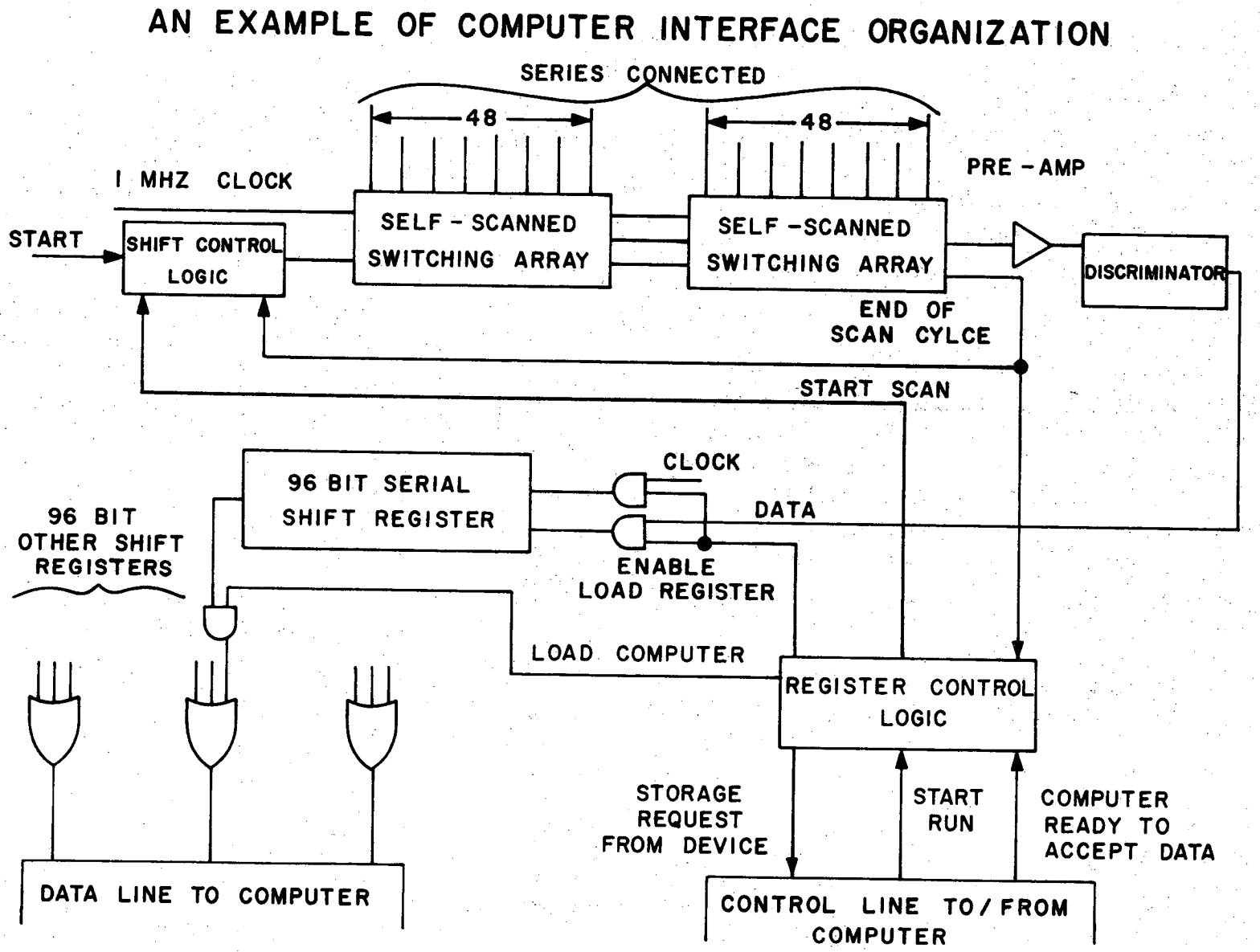
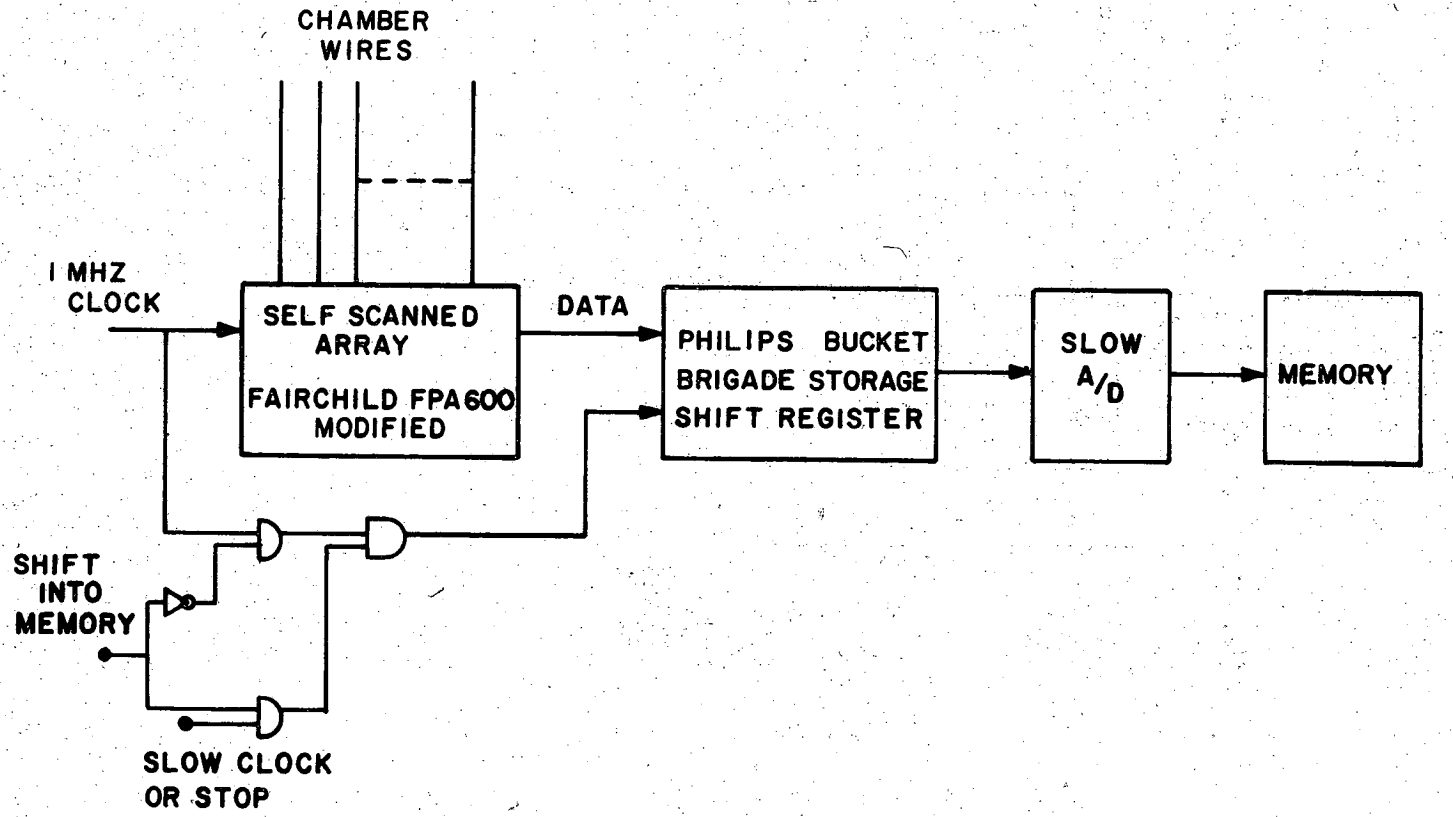

AN EXAMPLE OF COMPUTER INTERFACE ORGANIZATION
SERIES CONNECTED
48
48
1 MHZ CLOCK
PRE - AMP
START
SHIFT CONTROL LOGIC
SELF - SCANNED SWITCHING ARRAY
SELF - SCANNED SWITCHING ARRAY
DISCRIMINATOR
END OF SCAN CYLCE
START SCAN
96 BIT SERIAL SHIFT REGISTER
CLOCK
DATA
96 BIT OTHER SHIFT REGISTERS
ENABLE LOAD REGISTER
LOAD COMPUTER
REGISTER CONTROL LOGIC
STORAGE REQUEST FROM DEVICE
START RUN
COMPUTER READY TO ACCEPT DATA
DATA LINE TO COMPUTER
CONTROL LINE TO / FROM COMPUTER
XBL 708-1956

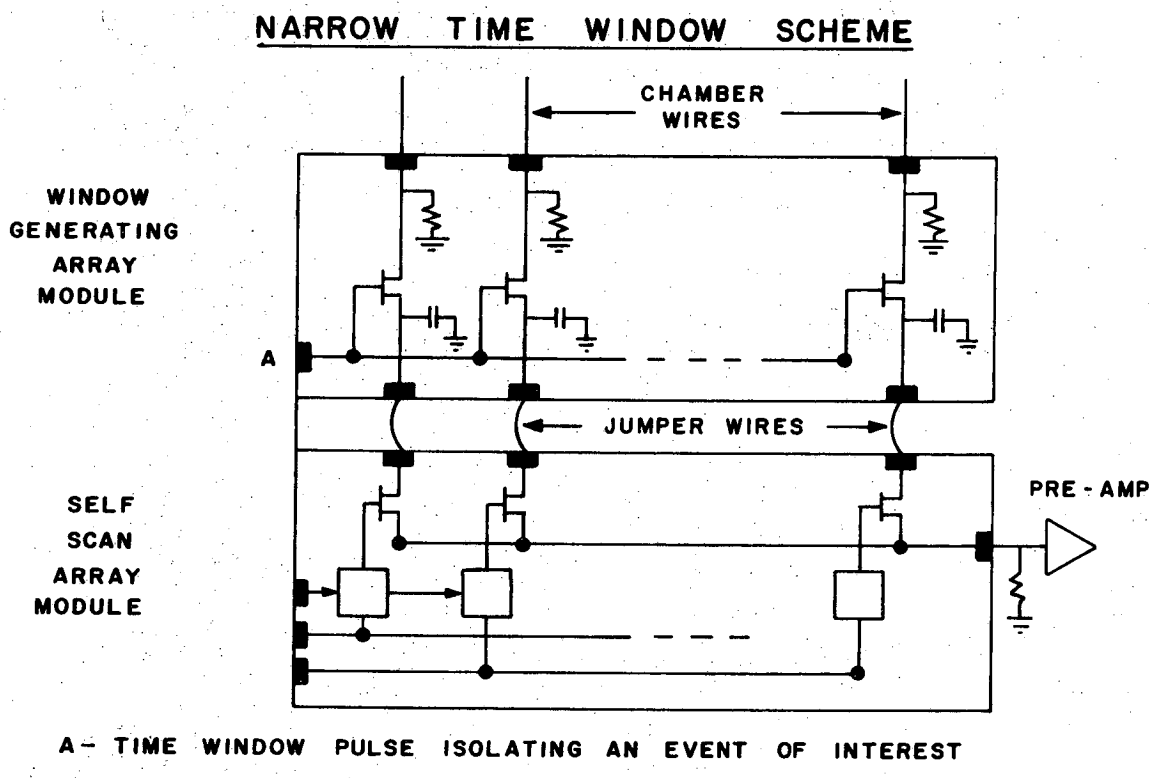
Fig. 3

ANALOG INFORMATION READOUT



XBL 708-1959

Fig. 4



XBL 708-1957

Fig. 5

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