Enhanced Interfacial Stability of Si Anodes for Li-ion Batteries via Surface SiO_2 Coating

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Abstract

Silicon is a promising alloying anode for lithium-ion batteries owing to its high capacity and low cost. However, its use has been hampered by mechanical failure arising from the large volume change upon cycling and by an insufficiently stable solid-electrolyte interphase (SEI). SEI formation depends on the Si surface, which is often an oxide (SiO_x). In this study we compare three different Si surfaces using Si wafers: 1.3 nm native SiO_x, 1.4 nm thermally grown SiO_2, and a SiO_x-free surface. The oxide-free surface showed the worst electrochemical performance, never exceeding 94% Coulombic efficiency (CE). It also exhibited the thickest SEI and the highest overpotential for lithiation, which correlated with uninhibited electrolyte reduction and the incorporation of P-F species into the SEI. The oxide-coated surfaces performed significantly better, demonstrating a CE above 99% beyond the second cycle, low overpotential for lithiation, and a thinner and more stable SEI. The oxides lower the onset potential for electrolyte reduction, and yield an SEI with fewer P-F species. However, it was found that the CE with the native oxide surface decays from the fifth cycle onwards and correlates with a resurgence of electrolyte reduction. A 1-2 nm thermal SiO_2 coating is optimum for achieving a stable SEI that minimizes side reactions and sustains efficient cycling.

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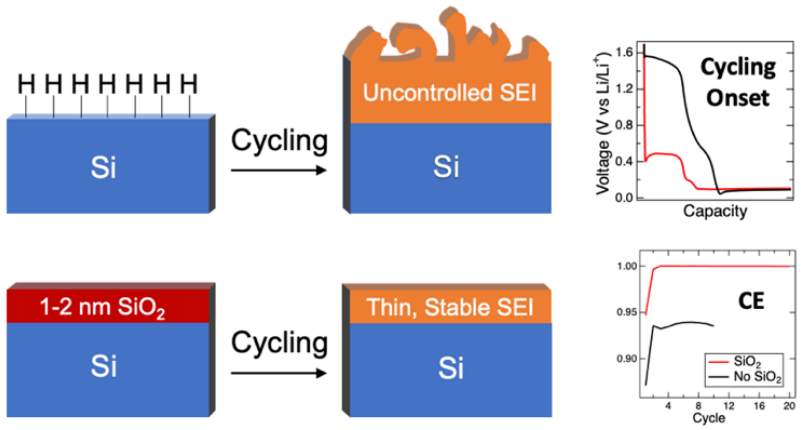

Keywords

Silicon anode, silicon oxide, lithiation, lithium ion battery, solid electrolyte interphase, carbonate electrolyte, interface, electrolyte reduction

Introduction

Silicon is of great interest as an anode material in advanced lithium-ion batteries (LIBs) as it is abundant, inexpensive, non-toxic, and has a roughly ten times greater theoretical capacity than graphite, the industry-standard anode[1-3]. Unfortunately, it tends to suffer from poor cycle life, which is typically attributed to two factors: mechanical failure[1, 4], and the lack of a stable surface layer[5] - a solid-electrolyte interphase (SEI) - as exists on graphite[6, 7]. The former exacerbates the latter because mechanical cracking reveals fresh surfaces that can form more SEI, consuming Li inventory. It is, therefore, critical to understand how the Si surface affects SEI chemistry and formation in order to form a stable SEI.

Si oxidizes readily in air, even at room temperature, so Si surfaces are often SiO_x and depend on the preparation method. However, this effect is rarely controlled when Si materials for LIBs are prepared. Where it was controlled, an SiO_x coating has been found beneficial[8-13], detrimental[14-17], or either depending on thickness[18, 19]. In this study, we examine how the electrochemical performance of Si anodes depends on the Si surface. Polished Si wafers are used as a model system with high purity and well-defined active area, and a native oxide surface is compared to an HF-etched oxide-free surface and a thermally oxidized surface. While native oxide surfaces have been studied using model systems[9, 20], we report the first comparison to (1) a thermal oxide coating that is equally thick, and (2) to a completely SiO_x-free surface. The former is important because we recently showed a strong effect of SiO_2 coating thickness on lithiation[21], and the latter ensures that our comparison is indeed to oxide-free Si.

The results obtained herein on Si wafers are expected to be applicable to Si nanomaterials for LIBs, which are typically <150 nm to avoid cracking[22], for a number of reasons: native oxide formation[18], oxide removal via HF[16] and thermal oxidation[10] have all been reported on different Si nanostructures; oxidation of Si yields an amorphous SiO_x[23] whose growth rate and properties depend only weakly on Si crystal orientation[24]; and our cycling procedure is designed to cycle only the top ~50 nm of the Si wafer[2, 8, 25, 26] at ~C/2 (~1700 mA/g). The main difference is that Si wafers are rigid and much thicker than the cycled depth, which means capacity losses due to dead Si are not detected (there is always more Si), and in-plane strains in the SiO_x coating and/or SEI are minimized. This allows us to characterize the electrochemistry of Si while minimizing the impact of other electrode components (binder, conductive additive), dead Si, and strain. We demonstrate that a thin thermal oxide delays the onset of electrolyte reduction, results in a thinner SEI, suppresses parasitic reactions, and enables cycling at lower overpotential and with high Coulombic efficiency (CE). We conclude by determining general criteria for a beneficial SiO_x coating.

Experimental Methods

The methods used for this study largely follow Ref. 21. Briefly, the three surfaces were prepared on highly-doped Czochralski-grown monocrystalline (100) Si wafers (0.002 Ωcm, boron-doped, 675 μm thick, single-side polished) purchased from Addison Engineering. SiO_x-free Si was obtained by etching in dilute HF followed by immediate transfer to an Ar-filled glovebox. Native SiO_x (1.3 nm) was present on as-received wafers and received an RCA clean[27] without HF steps. Thermal SiO_2 (1.4 nm) was grown in a tube furnace at 850°C within a cleanroom on RCA-cleaned wafers; an HF etch was performed immediately before growth. Oxide thicknesses were determined by spectral ellipsometry[21]. It is expected that the low surface roughness of the single-side polished Si wafer surfaces is maintained after HF etching since HF is very selective for SiO_2 over Si[28]. To

verify this, atomic force microscopy was performed on native oxide and thermal oxide samples before and after removing the oxide with dilute HF (Fig. S1). The root-mean-square surface roughness was below 0.25 nm for both samples before and after etching. This indicates that a flat surface is maintained for all samples which enables a comparison of surface chemistry independent of surface morphology.

Samples were assembled into custom three-electrode half-cells with Li foil counter and reference electrodes in an Ar-filled glovebox (<0.6 ppm H_2O, <0.3ppm O_2)[21]. Half-cells with Li foil have unlimited Li inventory and can therefore exhibit higher CE than full cells. The electrolyte was 1.2 ml of 1.2 M $LiPF_6$ in ethylene carbonate:ethyl methyl carbonate (EC:EMC, 3:7 w/w, <10 ppm H_2O, Tomiyama Pure Chemical Industries, Ltd.). Electrodes were held in place mechanically and no separators were used. Galvanostatic cycling was performed at 20μA/cm^2 between 0.01 and 1.5 V (*vs*. Li/Li$^+$, hereafter, Fig. 1). Lithiation and delithiation half-cycles were limited to 2 h, such that the maximum cycled capacity was 40 μAh/cm^2. Assuming all this charge went into converting crystalline Si into amorphous $Li_{3.5}Si$[2, 8, 25, 26], the top ~50 nm of the Si wafer would be lithiated. Electrochemical experiments were performed 2-3× at 20 μA/cm^2, and once at 30 μA/cm^2, always yielding the same trends.

Samples for XPS were prepared electrochemically at 20 μA/cm^2 as described above, removed from their custom cell inside an Ar-filled glovebox within 1 h of the end of electrochemistry, soaked in 1 ml dimethyl carbonate (DMC) for 1-2 min to remove electrolyte residue, and then dried in a glovebox antechamber for at least 1 h. An effort was made not to agitate the DMC to prevent removal of organic SEI components, but such an effect cannot be ruled out[29, 30]. Samples were then immediately transferred to the XPS chamber without exposure to air. XPS was measured using a Kratos Axis Nova instrument with an Al Kα source under an exit angle of 45°. Data analysis was performed using a custom program adapted from Schmid et al.

Results and Discussion

Electrochemistry

Cycling results for Si wafers with the three different surfaces are presented in Fig. 1. Panels (a), (b), and (c) show the 1st, 2nd, and 10th cycle, respectively; the CE is shown in (d). The beginning of the first cathodic half-cycle is enlarged in Fig. 1(a)inset and its differential capacity plot (dQ/dV) given in Fig. 1(e). The full cycling and dQ/dV dataset is provided in Fig. S2. During this first cathodic half-cycle all samples consume 1.1-1.5 μAh/cm^2 for electrolyte reduction and SEI formation before reaching the lithiation plateau of monocrystalline silicon at 0.1 V. This plateau is flat because lithiation of monocrystalline Si is an interface-limited process where Si is converted to amorphous Li_xSi at constant x[2, 8, 25, 26]. Upon delithiation and subsequent cycling, the Si never recrystallizes, so all subsequent cycles lithiate and delithiate amorphous Si[2, 25], which occurs at higher voltage (0.4-0.1 V) and with a finite voltage slope[25].

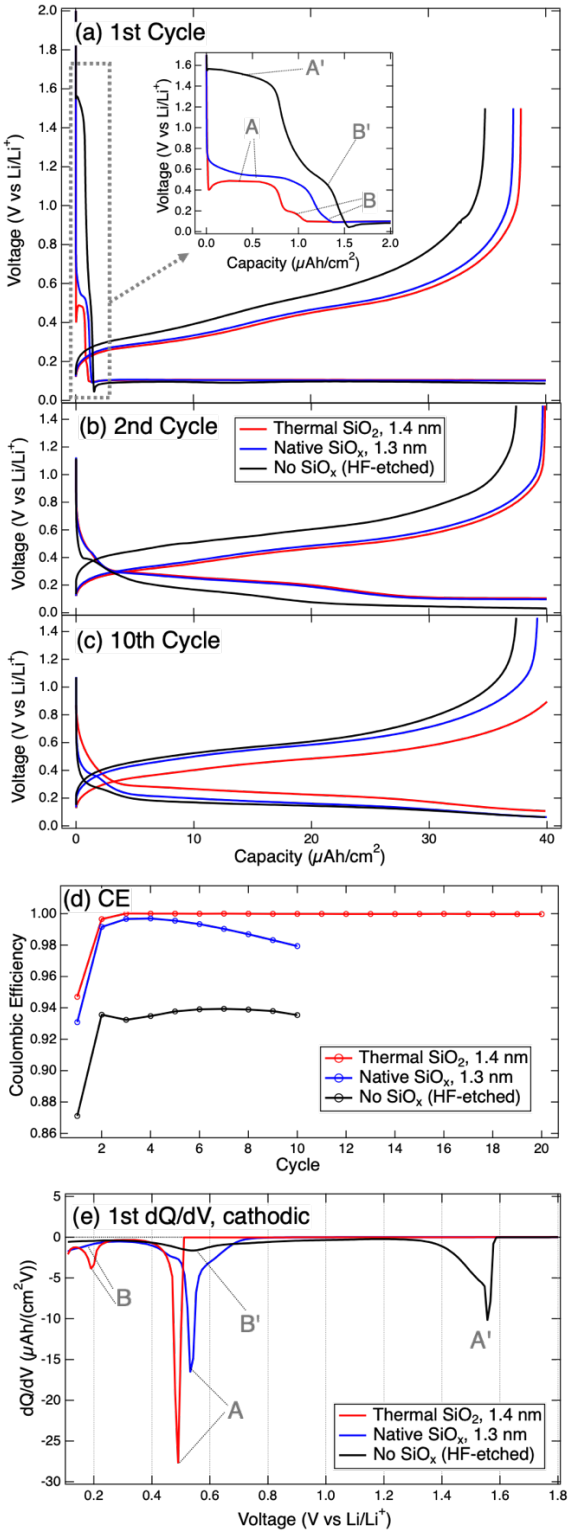

Figure 1. Galvanostatic cycling of Si wafers with three different surfaces. (a) 1st cycle (start of 1st cathodic half-cycle is enlarged in inset and differential capacity dQ/dV is shown in (e)), (b) 2nd cycle, (c) 10th cycle, (d) Coulombic efficiency. Panels (a)-(c) share a common horizontal axis and legend. Data points at local minima in (a), e.g. at ~0.4 V for thermal SiO_2, were removed before differentiation to eliminate discontinuities in dQ/dV (e). In (a) and (e) reduction processes prior to lithiation are labelled, these are discussed in the text.

The impact of the Si surface is visible from the very onset of cycling. An SiO_x-free, HF-etched surface enables electrolyte reduction starting at a reduction onset potential (ROP) of 1.55 V (Fig. 1 (a),(e)). The oxide-covered samples exhibit much lower ROP; 0.7 V for native oxide and 0.5 V for thermal oxide. We find that lower ROP correlates with less charge consumption prior to lithiation. Two reduction processes labelled A and B are identified which will be discussed later (A', B' for SiO_x-free Si). The SiO_x-free surface exhibits poorer CE and higher overpotential for lithiation and delithiation than surfaces with an oxide in all cycles (Fig. 1(a)-(c)). The oxidized surfaces perform much better, with similar electrochemical performance in the initial cycles observed for both oxides. However, after the 4th cycle the CE for the native SiO_x drops noticeably, and by the 10th cycle the sample exhibits similar overpotentials to the HF-etched sample (Fig. 1(c)). The cycling stability of these Si surfaces is thus ranked as follows: thermal SiO_2 > native SiO_x >> no SiO_x, showing that a thin thermal SiO_2 surface effectively mitigates parasitic reactions during cycling.

XPS

The Si 2p core level data for pristine samples is shown in the top row of Fig. 2. The thermal oxide has a slightly larger SiO_2 peak and smaller Si peak than the native oxide, indicating it is slightly thicker or denser. The Si-O signals are well fitted with a single component, indicating that both are mostly SiO_2. The SiO_2 peak is absent for the oxide-free sample, confirming that it did not reoxidize during sample transfer. After an HF etch, Si surfaces are terminated with Si-H bonds[31], which possess some stability against oxidation in air[31]. However, Si-H bonds have been reported to react chemically with the electrolyte used here, resulting in the partial substitution of surface hydrogen by ester and carbonyl groups[32].

To understand how an oxide coating affects SEI formation, XPS spectra were acquired at three electrochemical sample conditions: 0.115 V (early-stage SEI or es-SEI, just before lithiation begins)[33, 34], after the lithiation half-cycle, and after one full cycle. The fitted Si 2p, F 1s, and P 2p core levels are shown in Figures 2 and 3. The full dataset (C 1s, O 1s, Li 1s core levels) and quantitative fitting results are given in the Supporting Information. Spectra are not corrected for charging because different phases exhibit different degrees of charging-related peak shift[35], and phases are identified based on binding energy differences rather than absolute binding energies[35]. For example, the SiO_2 peak in Fig. 2 experiences a shift towards higher binding energies upon SEI formation, which could be due incommensurate charging[35], or formation of a space charge region at the electrode/SEI interface[36], yet it can be identified because the corresponding peak in the O 1s core level (Fig. S4) shifts as well.

As seen in Fig. 2, some Si or Li_xSi signal is visible for all samples, indicating that the Si is probed, that the entire SEI is probed, and that the SEI is less than 6 nm thick. All detectable elemental Si is unlithiated at 0.115 V, lithiates after half a cycle, and delithiates after a full cycle. Si lithiation appears fully reversible in all samples. The native oxide has partially lithiated at 0.115 V, whereas the thermal oxide has not. Over the course of the first cycle, both oxides partially lithiate in a largely irreversible manner. The thermal and native oxide samples both exhibit a strongly decreased overall Si 2p signal at 0.115 V, which decreases a little more upon lithiation and recovers on delithiation. This is consistent with the formation of a fairly stable SEI at 0.115 V that exhibits a mild "breathing" effect[29, 37], thinning during delithiation and thickening during lithiation. Conversely, the SiO_x-free sample actually has quite a strong Si 2p signal at 0.115 V, suggesting a thin SEI at 0.115 V. However, the Si 2p signal then decreases on lithiation, and even more so on

delithiation, indicating that the early-stage SEI was unstable and continued to thicken. After a full cycle, the low overall Si 2p signal suggests that the SiO_x-free surface has the thickest SEI.

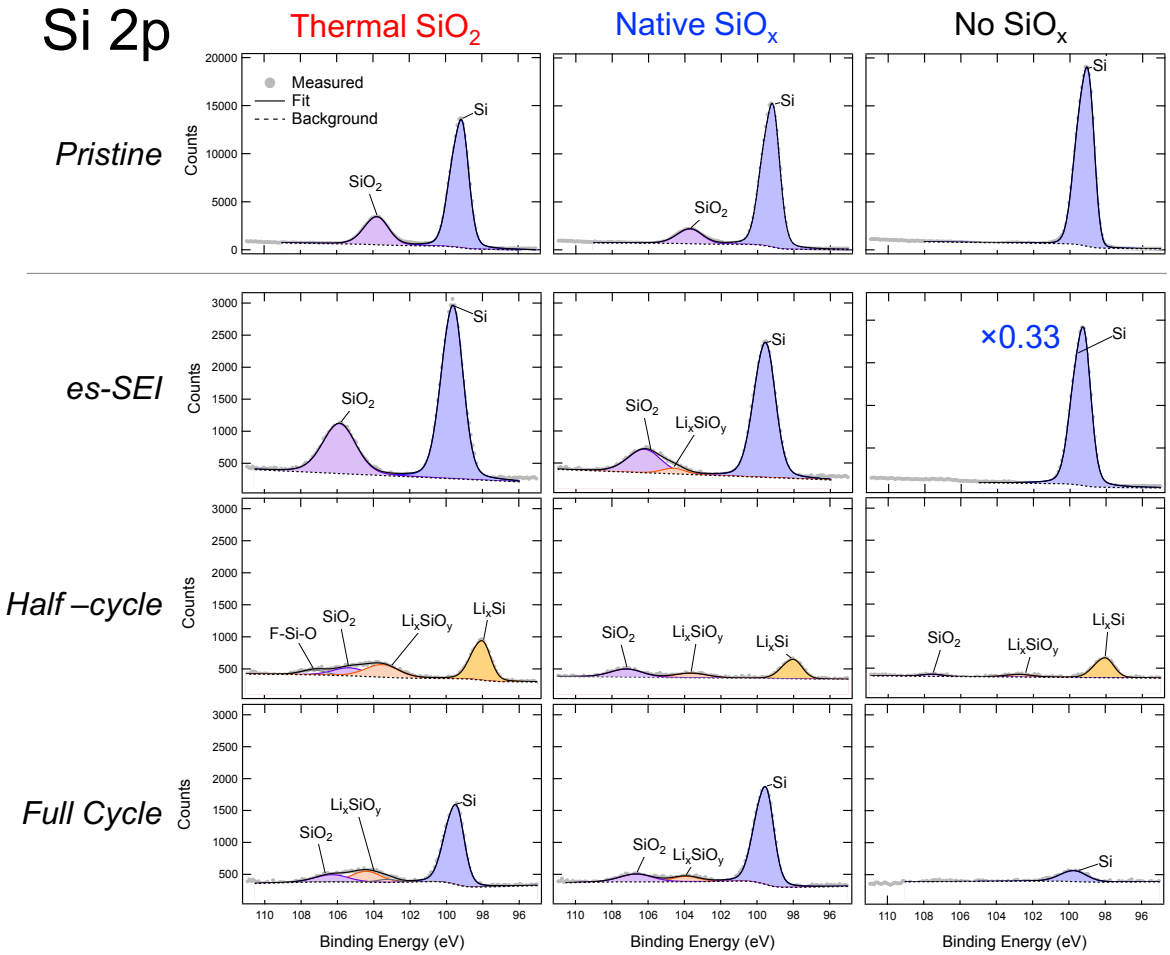

Figure 2. Fitted Si 2p core level XPS data for the three Si surfaces investigated. For each surface, spectra acquired on pristine samples, at 115 mV (early stage SEI, es-SEI), after half a cycle (lithiated) and after a full cycle (delithiated) are shown from top to bottom. All panels share the legend of the top-left panel and use the same binding energy scale, but note that the pristine spectra utilize a different vertical scale, and one panel was rescaled as noted in the panel. The following phases are shaded: Si (blue), SiO_2 (purple), Li_xSi (yellow), Li_xSiO_y (orange). Each peak fit to Si 2p levels actually consists of two peaks of fixed intensity ratio and binding energy separation to account for spin-orbit splitting.

SEIs on all surfaces exhibit a strong LiF signal and a weaker P-F signal assigned to $LiPF_6$ decomposition products (Fig. 3). Native and thermal oxides exhibit similar F 1s and P 2p spectra at 0.115 V which evolve very little upon lithiation and delithiation. The SiO_x-free sample exhibits less LiF but a lot more P-F groups than the oxide-coated samples at 0.115 V, and both signals grow throughout the first cycle. C 1s levels (Fig. S3) show the formation of carbonates and ester/carboxyl groups; however, the total carbon signal is not substantially larger than the adventitious carbon signal on pristine samples, suggesting that little organic SEI formed. Overall, XPS demonstrates that oxide-coated Si forms a relatively stable SEI at 0.115 V, whereas the SEI on an SiO_x-free surface continues to thicken and evolve throughout the first cycle.

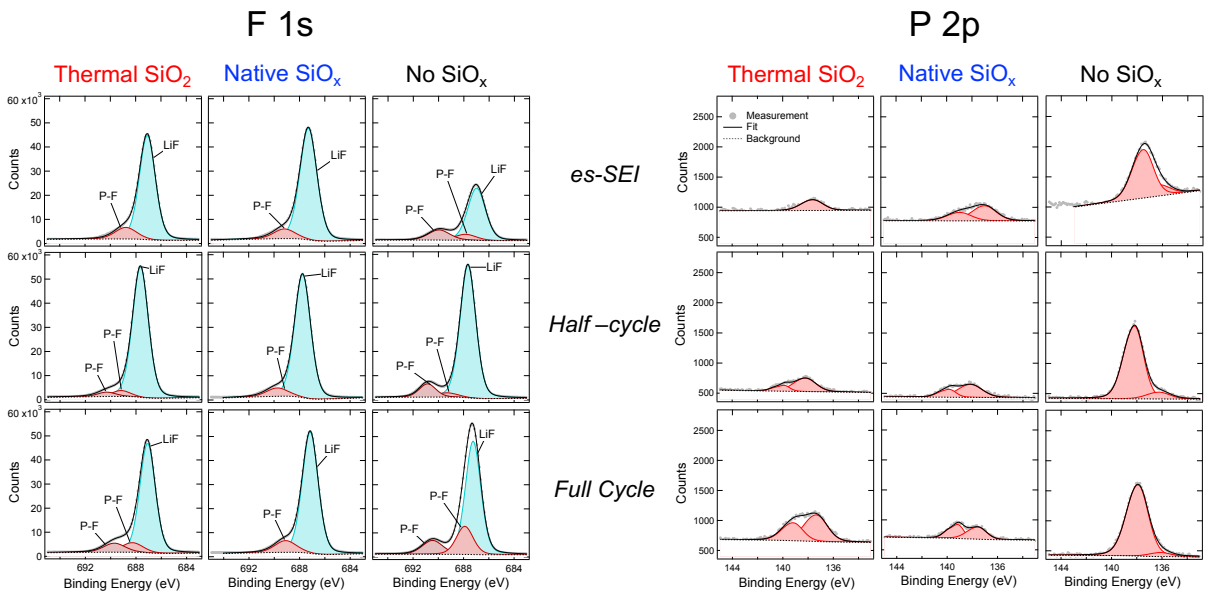

Figure 3: Fitted F 1s and P 2p core level XPS data for the three Si surfaces investigated. For each surface, spectra acquired at 115 mV (early stage SEI, es-SEI), after half a cycle (lithiated) and after a full cycle (delithiated) are shown from top to bottom. Only trace quantities of F and P were present on pristine samples. All panels share the legend of the top-left P 2p panel. All F 1s panels use the same axes. The following phases are shaded for F 1s: LiF (turquoise) and $LiPF_6$ decomposition products (P-F, red). All P 2p panels use the same axes, and all shaded peaks are attributed to $LiPF_6$ decomposition products, i.e. P-F bonds. Multiple peaks indicate multiple such species. Each peak shown for P 2p levels actually consists of two peaks of fixed 1:2 area ratio and 0.84 eV binding energy separation to account for spin-orbit splitting of the P 2p level.

Discussion

Generally, stable lithiation and delithiation of an anode at which electrolyte reduction is thermodynamically favorable requires a stable SEI[38] which kinetically inhibits electrolyte reduction by being impermeable to electrons, while remaining permeable to Li^+. SiO_x, and the lithium silicates (Li_xSiO_y) to which they might be converted during lithiation[1, 39-41], are very electronically resistive (>10^9 Ωcm[23, 42]), suggesting that they could form an artificial SEI. However, our prior work showed that >3 nm thermal SiO_2 is also a barrier to Li^+[21]. The optimum balance appears to be a 1-2 nm thick SiO_x coating, which still allows some electron transport via tunneling[23, 43], and thus exhibits some electrochemical SEI formation. Nevertheless, the ~1.4 nm thick oxides depress the ROP from 1.55 V to ≤ 0.7 V.

A recent study proposed that SiO_x coatings lower the ROP because they must be converted to Li_xSiO_y at ~0.7 V before $LiPF_6$ reduction can occur on them[9, 25], while another study showed LiF formation prior to SiO_x lithiation[44]. Our data illustrates both cases: the native oxide exhibits a Li_xSiO_y signal in its es-SEI Si 2p level (Fig. 2), and its process A exhibits a high-voltage shoulder in dQ/dV (Fig. 1(e)) matching the corresponding Li_xSiO_y peak in Ref. 9. Thermal SiO_2 does not exhibit this shoulder, or a Li_xSiO_y signal in its es-SEI Si 2p level. Li_xSiO_y formation occurs prior to Si lithiation for native oxide but not for thermal oxide, indicating that the thermal oxide is more stable and that Li_xSiO_y formation need not be a prerequisite for Li transport through SiO_2. However, it appears that Li transport through SiO_2 does eventually lead to Li_xSiO_y, which is observed in all samples after half a cycle (Fig. 2).

To facilitate analysis of electrolyte reduction reactions during the first cycle, ROP and several charge losses Q during the first cycle are tabulated in Table 1. The charge consumed before the lithiation plateau is denoted $Q_{>0.1V}$, which is further separated into Q_A and Q_B attributable to processes A and B, respectively (see Fig. 1(a),(e)). Q_{total}=40 μAh/cm^2×(1-CE) denotes the total first cycle loss, and Q_{total}-$Q_{>0.1V}$ is the charge loss *after* lithiation begins, under the assumption that $Q_{>0.1V}$ is fully irreversible.

Table 1. First cycle reduction onset potentials (ROP) and charge losses Q, as defined in the text. The errors in Q are estimated as ±0.1 μAh/cm^2.

	ROP (V)	Q_{total} (μAh/cm^2)	$Q_{>0.1V}$ (μAh/cm^2)	Q_{total}-$Q_{>0.1V}$ (μAh/cm^2)	Q_A (μAh/cm^2)	Q_B (μAh/cm^2)
No SiO_x	1.55	5.2	1.5	3.7	0.8 (A')	0.7 (B')
Native SiO_x	0.7	2.8	1.4	1.4	1.2	0.2
Thermal SiO_2	0.5	2.1	1.1	1.0	0.8	0.3

Two recent studies have examined SEI formation on Si wafers with native oxide, and both observed processes A and B[9, 34]. Cao *et al*. attributed A to $LiPF_6$ reduction yielding LiF, and B to Li_2O formation[9]. Yin *et al*. showed that LiF is present in similar quantities after A and after B, while the quantity of C-O, O-C=O, and CO_3 groups increased via process B specifically[34]. We find that for native and thermal oxide surfaces, Q_A>>Q_B, and XPS yields 65-75% LiF in their es-SEI (Fig. 3, Tables S1-S2). We therefore assign process A to $LiPF_6$ reduction. For the native oxide, only the main dQ/dV peak of process A at 0.53 V (Fig. 1(e)) is attributed to $LiPF_6$ reduction; the shoulder at 0.6-0.7 V is tentatively attributed to Li_xSiO_y formation as described earlier. Turning to process B, if it were Li_2O formation, we could estimate the thickness of Li_2O corresponding to Q_B, assuming one electron per Li atom incorporated and literature values for the molar mass and mass density of Li_2O[45]. This yields 0.4-0.9 nm Li_2O, which would be discernible by XPS. We do not observe Li_2O in the es-SEI of oxide-coated samples (Fig. S5), but we do observe an increase in carbon-oxygen bonds (Fig. S3), so we tentatively attribute B to solvent reduction, in agreement with Ref. 34. Since the more polar solvent that solvates Li^+ is typically reduced, we attribute B to EC reduction.

As the es-SEI of SiO_x-free Si shows >60% LiF and $LiPF_6$ decomposition products, either A' or B' should correspond to $LiPF_6$ reduction. Two possible explanations are that B' is $LiPF_6$ reduction and A' is a process unique to the SiO_x-free surface, or processes A' and B' correspond to A and B, respectively, but are shifted to higher voltage. While our data does not conclusively prove either explanation, much evidence supports the latter (i.e. A'=A, B'=B). First, the reduction potentials for $LiPF_6$ and Li^+-solvating EC have been calculated as 1.46-1.61 V[46, 47] and 0.45-0.6 V[47], respectively, corresponding to A' and B', and it is plausible that both would occur with little overpotential in the absence of a SiO_x barrier. Experimental evidence for reduction of $LiPF_6$ at ~1.6 V has been reported on silicon carbide[9] and glassy carbon[47]. Second, we showed previously that the ROP is lowered further by thicker thermal SiO_2, to 0.15 V for 2.1 nm and to -0.4 V for 2.6 nm[21]. Linear extrapolation to 0 nm SiO_2 yields ~1.6 V. Third, the sharp dQ/dV peaks of A in Fig 1(e) are more similar to A' than to B', suggesting a similar mechanism. It appears that an oxide-free surface allows electrolyte reduction to proceed near predicted potentials, whereas ~1.4 nm SiO_x lowers the potentials significantly, by up to 1.0 V for process A.

While the electrolyte reduction reactions appear to be similar, the consequences are dramatically different for the different surfaces. Oxide-coated surfaces slightly lower $Q_{>0.1V}$, but they lower Q_{total} much more, leading to ~3× lower Q_{total}-$Q_{>0.1V}$. SiO_x kinetically inhibits electrolyte reduction *before* lithiation, but the reduction that does occur yields a more stable SEI at 0.115 V that strongly reduces charge loss *during* lithiation/delithiation. This is in agreement with XPS data which evidenced stable SEI on oxide-coated Si, and continued growth of SEI (with a particularly high concentration of P-F groups) on SiO_x-free Si. The discrepancy between the high $Q_{>0.1V}$ and strong Si 2p signal of es-SEI on SiO_x-free Si suggests that reduction reactions on SiO_x-free Si yield products that are less amenable to dense SEI formation, resulting in either a patchy SEI or a larger proportion of soluble reduction products. The picture that emerges is that electrolyte reduction on SiO_x-free Si is less controlled, occurring at higher voltages and leading to an unstable and possibly porous SEI that limits CE to <94% for ten cycles. With a thin SiO_x, reduction occurs in a more controlled manner, leading to a thinner, more stable SEI and higher CE. Interestingly, with SiO_x a *greater* overpotential for electrolyte reduction yields an SEI that *lowers* the overpotential for lithiation and delithiation (Fig. 1).

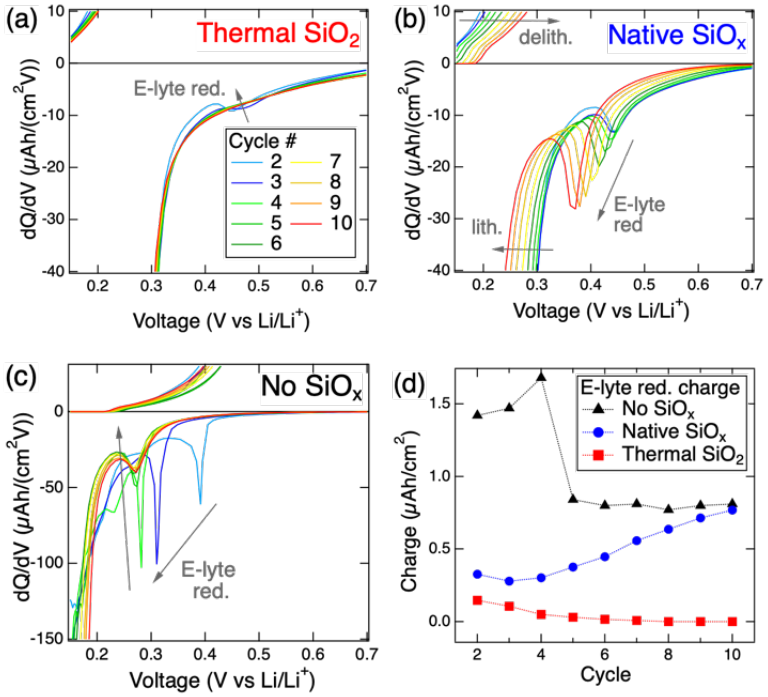

Figure 4. Differential capacity plots (dQ/dV) for cycles 2-10 on (a) thermal SiO_2, (b) native SiO_x, (c) no SiO_x. The legend of (a) applies to (a)-(c). All show an electrolyte reduction peak labelled "E-lyte red." prior to lithiation for at least some cycles. The charge consumed by this process was determined by peak integration and is shown in (d).

Oxide-coated Si surfaces yield CE >99% after 3-4 cycles, but thermal oxide maintains high CE whereas the CE with native oxide decays, and its overpotential for lithiation increases (Fig. 1). Examination of dQ/dV plots for cycles 2-10 (Fig. 4) reveals that electrolyte reduction persists past the first cycle for all surfaces, decaying for thermal oxide but growing for native oxide. SiO_x-free Si initially exhibits two peaks (Fig. 4(c)), but one of them disappears after four cycles and the associated charge consumption drops (Fig. 4(d)), but stays high. Given the very similar SEIs formed on the two oxide-coated surfaces after one full cycle, we propose that the native SiO_x might

be mechanically weaker and fracture sooner on cycling, exposing more fresh Si to electrolyte in each cycle which then reduces it, consuming charge. Electrolyte reduction on fresh Si is proposed to be akin to that on SiO_x-free Si, yielding successively lower CE (Fig. 1(d)) and higher overpotential (Fig. 4(b)). A greater mechanical resilience of thermal SiO_2 could arise from its elevated growth temperature, allowing the formation of more stable bonds, or its slightly higher density or thickness (Fig. 2, "pristine"), also providing an explanation for why it did not lithiate at 0.115 V. Furthermore, thermal SiO_2 has built-in compressive stress[48], so it is only under tension in later stages of lithiation.

Comparison to the literature yields a more holistic understanding of SiO_x coatings. Three studies suggested an improvement with native SiO_x over nominally SiO_x-free Si[8, 11, 25]. A study that varied SiO_x from 0-15 nm found that 2 nm native SiO_x were better than a nominally SiO_x-free surface, while 7 nm thermal SiO_2 yielded optimum CE[18]. Another study showed that 2-5 nm thermal SiO_2 improved capacity retention in nanoporous silicon[13]. Of the studies that reported a detrimental effect of SiO_x, one compared 6 nm SiO_x to an "oxide-free" surface with 1.3-2.7 nm SiO_x[16], and another compared fairly thick 7.4 nm and 3.4 nm SiO_x to a SiO_x-free surface[17]. Another studied Li_xSiO_y coatings[14], finding a detrimental impact on cycling, and concluded that since SiO_x lithiates, it is a detrimental coating. However, applying Li_xSiO_y differs from lithiating SiO_x during SEI formation since Li_xSiO_y forms some SEI on contact with electrolyte whereas SiO_x does not[49]; the stable SEI formation on SiO_x is related to delayed electrolyte reduction. We found that electrochemical SiO_x lithiation occurs with, or after, formation of the SEI.

Thin SiO_x coatings formed by surface oxidation of the Si generally improve Si anode performance provided they are no more than 5±2 nm thick and unlithiated before cell assembly[11, 13-19, 21, 32]. They lower the reactivity of the surface to prevent SEI formation on contact with electrolyte, and enable the controlled electrochemical formation of a thin, dense SEI. The low thickness allows for charge transport and minimizes the irreversible charge consumption associated with SiO_x lithiation. It should be noted that this conclusion refers to oxides grown into Si via oxidation. Our preliminary findings show that additive SiO_x layers produced via sputtering or evaporation are more permeable to Li transport than thermal SiO_2 for a given thickness, suggesting they may not achieve the same level of passivation. However, sputtering and evaporation are directional and therefore of less relevance for the conformal coating of Si nanomaterials for LIBs.

Conclusions

The cycling performance and SEI formation was compared across three different Si surfaces on model Si samples: HF-etched (no SiO_x), native SiO_x, and thermal SiO_2. The oxide-free surface performed the worst (CE <94%), whereas both oxide-coated surfaces reached >99% after a few cycles. This was attributed to uninhibited electrolyte reduction on the oxide-free Si, yielding a high concentration of P-F species, soluble reduction products and/or inhomogeneous SEI, an unstable SEI, and increased overpotential for lithiation. The oxide coatings lower the electrolyte reduction onset potential, yield a stable SEI, and decrease first cycle losses. The CE decay of the native SiO_x surface after the fifth cycle correlates with a resurgence of electrolyte reduction and is tentatively attributed to the exposure of fresh Si upon cycling. A 1-2 nm thermal SiO_2 coating is found to be optimum for achieving a stable SEI.

Associated Content

File "Schnabel_SiOxlith_SI_8.pdf" contains: Atomic Force Microscopy of pristine oxidized and etched surfaces, Full galvanostatic cycling results for all samples, Full XPS dataset and fitting results for all samples.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Funding Sources

Funding was provided by the U.S. Department of Energy's Vehicle Technologies Office under the Silicon Electrolyte Interface Stabilization (SEISta) Consortium directed by Brian Cunningham and managed by Anthony Burrell.

Acknowledgements

The authors thank Matthew Page and Ryan Pekarek for enabling Si wafer processing and for fruitful discussions. This work was authored by the National Renewable Energy Laboratory, operated by the Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding was provided by the U.S. Department of Energy's Vehicle Technologies Office under the Silicon Electrolyte Interface Stabilization (SEISta) Consortium directed by Brian Cunningham and managed by Anthony Burrell. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government.

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