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A Ku-Band Inductive Neutralized NPN–PNP LNA in 130-nm SiGe BiCMOS

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A Ku-Band Inductive Neutralized NPN–PNP LNA in 130-nm
SiGe BiCMOS

A Thesis submitted in partial satisfaction
of the requirements for the degree

Master of Science
in
Electrical and Computer Engineering

by

Lian Liu

Committee in charge:

Professor James Buckwalter, Chair
Professor Clint Schow
Professor Mark Rodwell

June 2026

The thesis of Lian Liu is approved.

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June 2026

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by

Lian Liu

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Abstract

A Ku-Band Inductive Neutralized NPN–PNP LNA in 130-nm SiGe BiCMOS

by

Lian Liu

The demand for high-performance amplifiers in wireless communication systems continues to grow as radio-frequency front ends require improved sensitivity, gain, and noise performance. Low-noise amplifiers (LNAs) with high gain and low noise figure are therefore critical for enhancing overall receiver performance. To improve gain at the target operating frequency, an inductive-neutralization technique can be employed to mitigate the effect of parasitic feedback capacitance.

This thesis presents the design and characterization of an inductively neutralized low-noise amplifier implemented in a 130 nm complementary NPN–PNP SiGe BiCMOS process. The proposed architecture uses a complementary NPN–PNP amplifier with inductive neutralization to investigate the cancellation of the base–collector overlap capacitance, C_{bc} .

The fabricated amplifier achieves an average measured small-signal gain of approximately 9 dB at 15.5 GHz while dissipating 9.12 mW of DC power. A minimum noise figure of 4.92 dB is obtained at 12 GHz. The total chip area, including pads, is 0.57 mm².

The use of inductive feedback improves reverse isolation, S_{12} , at the operating frequency, indicating effective cancellation of the base–collector overlap capacitance. This

characteristic is beneficial for suppressing local-oscillator leakage in RF front-end applications.

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Chapter 1

Introduction

1.1 Motivation

The performance of a wireless communication system is strongly influenced by the performance of its receiver. In modern receiver architectures, including both homodyne and heterodyne receivers, front-end amplifiers, as shown in Fig. 1.1, play a critical role in determining overall system sensitivity and signal quality. To reliably detect weak incoming signals, these amplifiers must provide sufficient gain while introducing minimal additional noise [1].

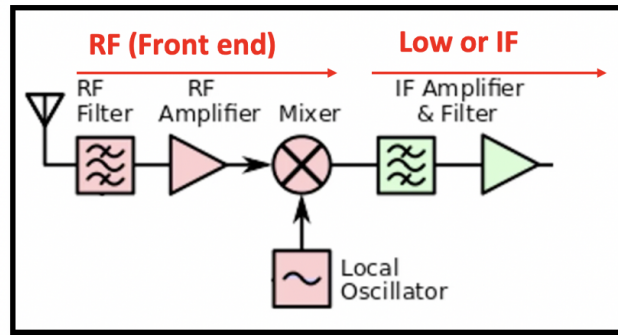


Figure 1.1: Block diagram of a typical heterodyne receiver (adapted from [2]).

The performance of a receiver is fundamentally governed by the relationships among gain, noise figure, signal-to-noise ratio (SNR), and minimum detectable signal

(MDS). The minimum detectable signal can be expressed as [3]

$$\text{MDS} = -174 + 10 \log_{10}(B) + NF + \text{SNR}_{\min}$$

where B is the receiver bandwidth in hertz, NF is the receiver noise figure in decibels, and $\text{SNR}_{\min}$ is the minimum signal-to-noise ratio required for detection.

As a result, improvements in amplifier gain and noise figure directly enhance receiver sensitivity by reducing the minimum detectable signal. This enables the reception of weaker signals, leading to extended communication range and improved overall system performance.

1.2 Limitations of Existing Approaches

The overlap capacitance of transistors can introduce significant performance limitations in high-frequency circuits, including local-oscillator (LO) leakage in receiver front ends. In particular, the base-collector (or gate-drain) overlap capacitance provides a direct feedthrough path that allows the LO signal to couple back to the input, thereby degrading reverse isolation. In communication systems with closely spaced frequency channels, the leaked LO signal may act as an unwanted interferer, potentially degrading the performance of neighboring channels [4].

To address this problem, several amplifier topologies have been proposed. One widely adopted approach is the use of emitter (or source) degeneration inductors to improve input matching, stability, and noise performance. However, degeneration introduces local negative feedback, which reduces the effective transconductance and consequently lowers the amplifier gain.[5] As a result, amplifier designers must carefully optimize the degeneration inductance to balance gain, noise figure, input matching, and

stability requirements. Furthermore, excessive degeneration can introduce additional poles that degrade the high-frequency gain response, requiring further compensation techniques.[6]

1.3 Outline

This thesis focuses on the design, simulation, fabrication, and measurement of an inductively neutralized amplifier. It is organized as follows. Chapter 2 presents the circuit analysis, simulation results, comparison between theoretical predictions and simulations, and measurement results of the fabricated amplifier. Chapter 3 summarizes the main contributions of this work and discusses future research directions, including the development of multi-stage amplifier architectures incorporating inductive-neutralization techniques.

Chapter 2

Circuit Analysis, Design, and Measurements

2.1 Circuit Analysis

To investigate the effect of overlap-capacitance cancellation on amplifier performance, a complementary NPN–PNP amplifier with inductive feedback is proposed. At the resonance frequency of the LC network formed by the overlap capacitance and the feedback inductor, the reactive components effectively cancel each other, thereby minimizing the feedback path. As a result, the influence of overlap capacitance is significantly reduced within a narrow frequency band, leading to improved gain and reverse isolation near the operating frequency.

The amplifier was implemented in the GlobalFoundries 130CBIC high-performance complementary SiGe BiCMOS process. The technology provides high-performance NPN and PNP bipolar transistors with reported f_T/f_{max} values of approximately 350 GHz/450 GHz and 200 GHz/250 GHz, respectively.[7] Since the target operating frequency of 15.5 GHz is significantly lower than the maximum oscillation frequencies of both devices, the transistors are capable of providing substantial power gain at the operating frequency. This large margin between the operating frequency and f_{max} allows the amplifier performance to be primarily limited by circuit topology, passive component losses, and parasitic effects rather than the intrinsic speed limitations of the transistors.

2.1.1 Gain Analysis

A circuit, shown in Fig. 2.1, was designed to verify the proposed topology. The corresponding small-signal model is presented in Fig. 2.2. To simplify the analysis, the base-emitter capacitances C_{be} are neglected, and equal base currents are assumed for the NPN and PNP transistors. Under these assumptions, a closed-form expression for the short-circuit current gain H_{21} can be derived.

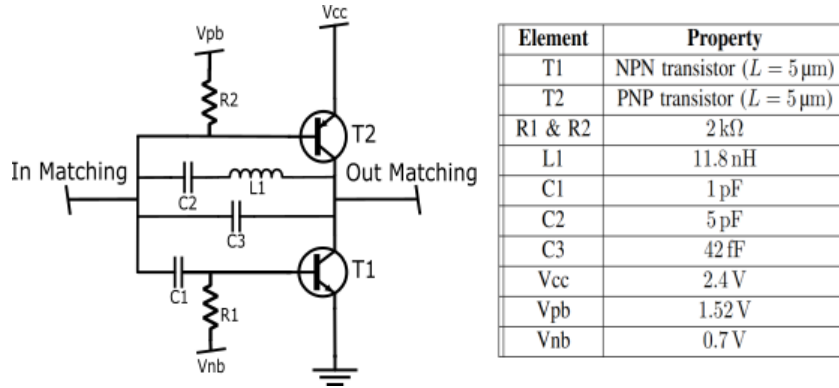


Figure 2.1: Schematics of the designed amplifier.

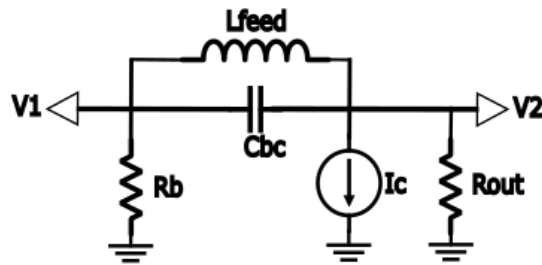


Figure 2.2: Simplified small signal model of the designed amplifier.

The feedback network formed by L_{feed} and C_{bc} is modeled as a parallel LC resonator with finite quality factor Q , having an equivalent impedance Z_{LC} . The total collector current is given by

$$I_c = (\beta_n + \beta_p)I_b,$$

where β_n and β_p are the current gains of the NPN and PNP devices, respectively.

From the input network,

$$V_1 = I_1 \left(\frac{Z_{LC} R_b}{Z_{LC} + R_b} \right),$$

and therefore

$$I_b = \frac{V_1}{R_b} = I_1 \frac{Z_{LC}}{Z_{LC} + R_b}.$$

The output current can be expressed as

$$I_2 = I_c - \frac{V_1}{Z_{LC}}.$$

Substituting the expressions for I_c and V_1 yields

$$I_2 = I_1 \left[(\beta_n + \beta_p) \frac{Z_{LC}}{Z_{LC} + R_b} - \frac{R_b}{Z_{LC} + R_b} \right].$$

Hence, the short-circuit current gain is

$$H_{21} = \frac{I_2}{I_1} = \frac{(\beta_n + \beta_p)Z_{LC} - R_b}{Z_{LC} + R_b}.$$

For the practical case where

$$(\beta_n + \beta_p)Z_{LC} \gg R_b,$$

the current gain may be approximated as

$$H_{21} \approx (\beta_n + \beta_p) \frac{Z_{LC}}{Z_{LC} + R_b}.$$

Near the resonance frequency of the LC tank, Z_{LC} becomes very large, resulting in

$$H_{21} \approx \beta_n + \beta_p,$$

demonstrating that the complementary NPN–PNP topology effectively combines the current gain of both transistors while minimizing the loading effect of the overlap capacitance.

This trend is further confirmed by circuit simulations of the topology shown in Fig. 2.1. The simulated results, presented in Fig. 2.3, indicate that the maximum stable gain (MSG) at the operating frequency is approximately 11 dB higher than that of the circuit without the feedback inductor. This improvement is attributed to the resonance between the feedback inductor and the overlap capacitance, which effectively neutralizes the capacitive feedback path and enhances the current gain of the amplifier.

In contrast, the degradation in noise performance due to the thermal noise associated with the finite series resistance of the feedback inductor is minimal. As a result, the inductive neutralization technique provides a significant gain enhancement while introducing only a negligible increase in the overall noise figure.

2.1.2 Noise Analysis

The minimum noise figure achievable by transistors in the 130CBIC process is approximately 0.45 dB, based on simulations performed on the transistor devices alone. The minimum noise factor of a bipolar transistor can be approximated by [8]

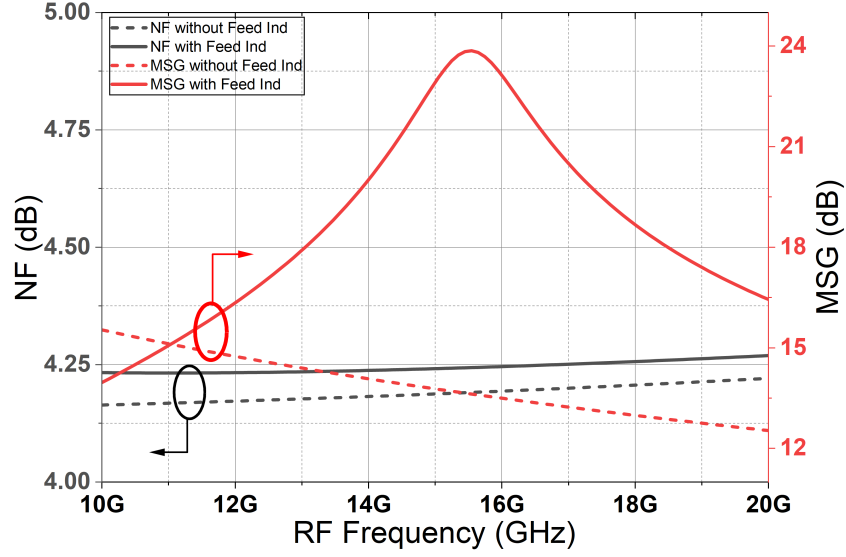


Figure 2.3: Simulation of the core part of the designed amplifier.

$$F_{\min} \approx 1 + h \left(1 + \sqrt{1 + \frac{2}{h}} \right),$$

where

$$h \approx 0.04 I_{Cr_b} \left(\frac{f}{f_t} \right)^2.$$

Under the operating conditions used in this work, the parameter (h) is calculated to be approximately 0.0116, yielding

$$F_{\min} \approx 1.164,$$

which corresponds to a minimum noise figure of approximately 0.66 dB. This analytical result is in reasonable agreement with the simulated minimum noise figure of 0.45 dB obtained using an ideal biasing network.

It should be noted that the amplifier was primarily optimized for gain rather than

noise performance. Consequently, the input and output matching networks were designed for gain matching instead of noise matching. As a result, the measured circuit exhibits a noise figure of approximately 4.25 dB, which is significantly higher than the intrinsic minimum noise figure of the transistor.

In addition to the mismatch between the optimum gain and noise matching conditions, several other mechanisms contribute to the overall noise figure. Thermal noise generated by the biasing resistors, finite losses in the matching network, and resistive losses in the on-chip interconnects and inductors all introduce additional noise that degrades the amplifier performance.

An alternative approach to improving the overall receiver noise performance is to precede the amplifier with a low-noise gain stage. According to Friis' noise formula, [9]

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots$$

the noise contribution of subsequent stages is suppressed by the gain of the preceding stages. Since the amplifier presented in this work was specifically optimized for high gain, it is well-suited for use as a second-stage amplifier, where its noise figure contribution is effectively reduced by the gain of the first stage. In such a cascaded architecture, the high gain achieved by the proposed amplifier can be exploited while minimizing its impact on the overall receiver noise figure.

2.1.3 Comparison of similar work

2.2 Measurement of the Fabricated Circuit

Following fabrication in the GlobalFoundries 130-nm SiGe BiCMOS process as the amplifier chip showing in Fig 2.4, the LNA was characterized through on-wafer S-parameter

Table 2.1: Performance Comparison with Inductive-Neutralized Amplifiers

Parameter	Kim 2022 (1st Stage)[12]	This Work (Proposed)	Unit
Technology	65-nm CMOS	130-nm SiGe BiCMOS	–
Topology	CS + Neutralization	NPN–PNP + Neutralization	–
Operating Freq.	42	15.5	GHz
Peak Gain	8	15	dB
3-dB Bandwidth	4	2	GHz
Noise Figure	—	3.5	dB
P_{DC}	—	9.12	mW
Chip Area	0.37	0.57	mm ²
MSG	15.1	17	dB

measurements using a Keysight N5247A PNA-X Microwave Network Analyzer. The amplifier performance was evaluated over the frequency range surrounding the target operating frequency of 15 GHz. Calibration was performed using on-wafer multilayer through-reflect-line (TRL) standards with RF probe pads matching those of the fabricated amplifier, thereby moving the reference planes to the device under test and minimizing measurement errors associated with the probe interface.

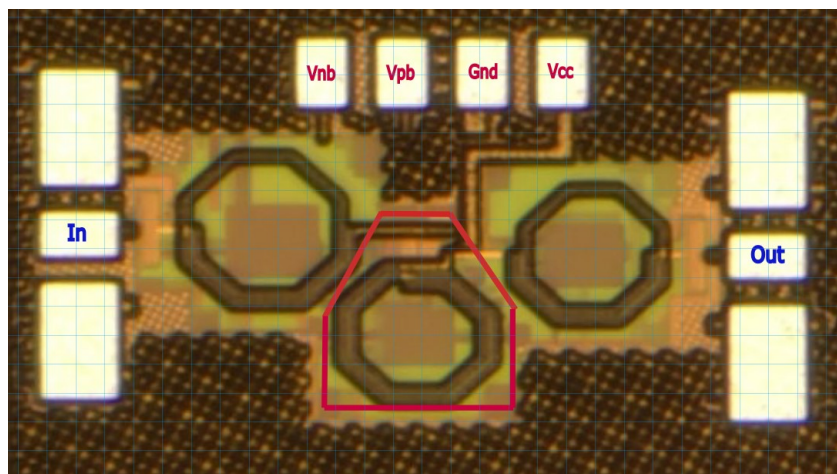


Figure 2.4: Chip microscopic photo with circled part showing the circuit in Fig 2.1

2.2.1 Input and Output S-parameters

The measured and simulated S-parameters are compared in Fig. 2.5.

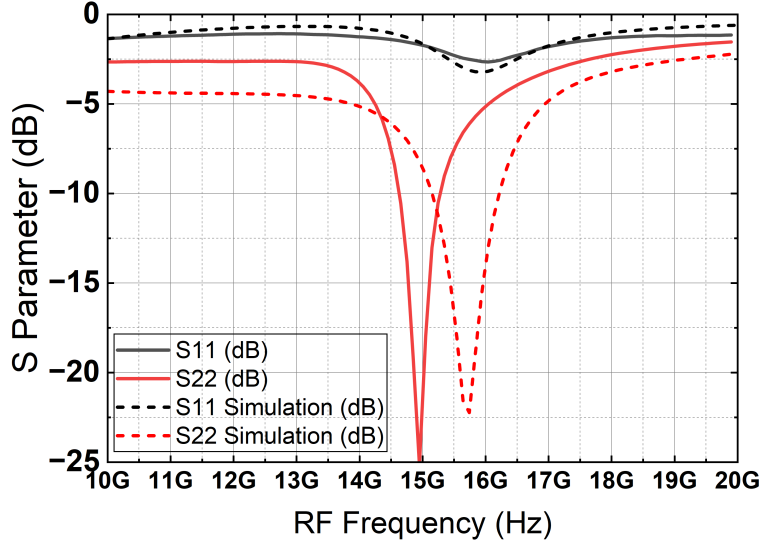


Figure 2.5: Comparison of simulated and measured S-parameters.

As shown in Fig. 2.5, the measured and simulated responses exhibit good overall agreement, validating both the proposed circuit topology and the electromagnetic modeling methodology. The simulation results were obtained from a full-layout EMX electromagnetic simulation, which captures the majority of the parasitic effects associated with the fabricated layout.

However, the resonance frequencies corresponding to the minima of S_{22} in the simulation and measurement differ by approximately 0.6 GHz, indicating a modest discrepancy between the predicted and measured output matching characteristics. One possible explanation is the sensitivity of the transistor output impedance to the biasing condition. Since S_{22} is strongly influenced by the transistor's small-signal parameters,[10] variations in the fabricated bias network can alter the output impedance and shift the matching frequency. In particular, process-induced variations in the DC biasing resistors

may lead to deviations in the collector current from its nominal design value, resulting in changes to the transistor capacitance and transconductance. These effects can subsequently modify the output matching condition and account for the observed shift in the S_{22} resonance frequency.

Another noticeable discrepancy is observed in the input reflection coefficient S_{11} . This mismatch is believed to arise from coupling effects between the input matching inductor L_{input} and the feedback inductor L_1 that were not fully captured during the partial electromagnetic extraction process.[11] Mutual inductive coupling between closely spaced on-chip inductors can significantly modify the effective inductance and input impedance of the network, resulting in shifts in the matching condition. Despite this discrepancy, the measured gain and overall frequency response remain in reasonable agreement with the simulated results, indicating that the full-layout EM simulation accurately predicts the principal amplifier behavior.

2.2.2 Noise Figure and Gain

The matrix amplifier noise figure was measured using the hot/cold Y-factor method up to 18 GHz with a noise source having a nominal excess noise ratio (ENR) of 15.2 dB. A Keysight N4001A noise source was connected directly to the RF probe through a coaxial cable. The insertion loss of the cable was de-embedded from the measured noise figure using manufacturer-provided loss data. In addition, the probe loss was characterized through a back-to-back measurement using a pair of RF probes connected by an on-chip thru structure, and the measured loss was incorporated into the de-embedding procedure.

As shown in Fig. 2.6, the simulated noise figure ranges from approximately 5 dB to 10 dB over the frequency range up to 18 GHz. The elevated noise figure at certain frequencies may be associated with potential instability in the amplifier. At the target

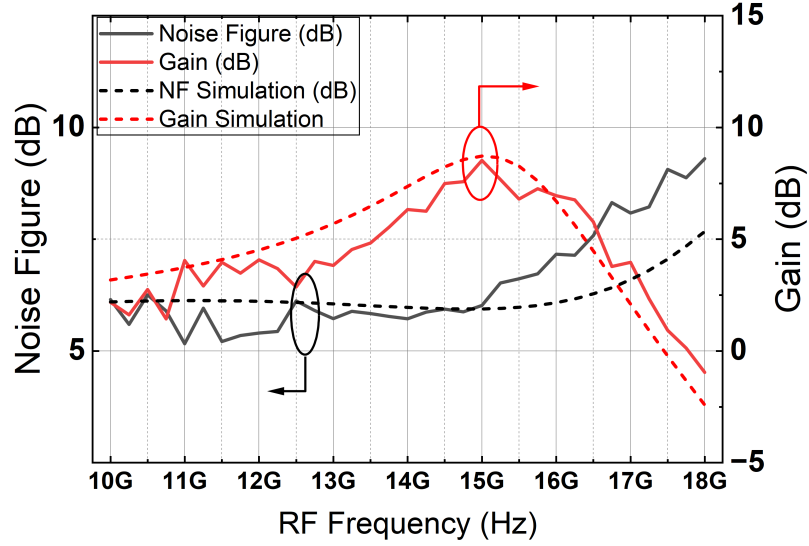


Figure 2.6: Comparison of simulated and measured noise figure and gain.

operating frequency of 15 GHz, the measured noise figure is 5.7 dB, which is in close agreement with the simulated result.

2.2.3 Discussion of Stability

Stability remains a significant challenge in the neutralized circuit topology. Fig. 2.7 presents the simulated and measured μ -factor of the amplifier, where the measured values were extracted from the measured S-parameters. Both simulation and measurement indicate potentially unstable operation below approximately 15.4 GHz, corresponding to a μ -factor less than unity.

The reduced stability is primarily attributed to the inductive neutralization network, which introduces additional feedback between the input and output nodes.[12] Furthermore, electromagnetic coupling between the feedback inductor and the input matching inductor can create unintended feedback paths, further degrading stability. The observed discrepancy between the simulated and measured μ -factor peaks is believed to

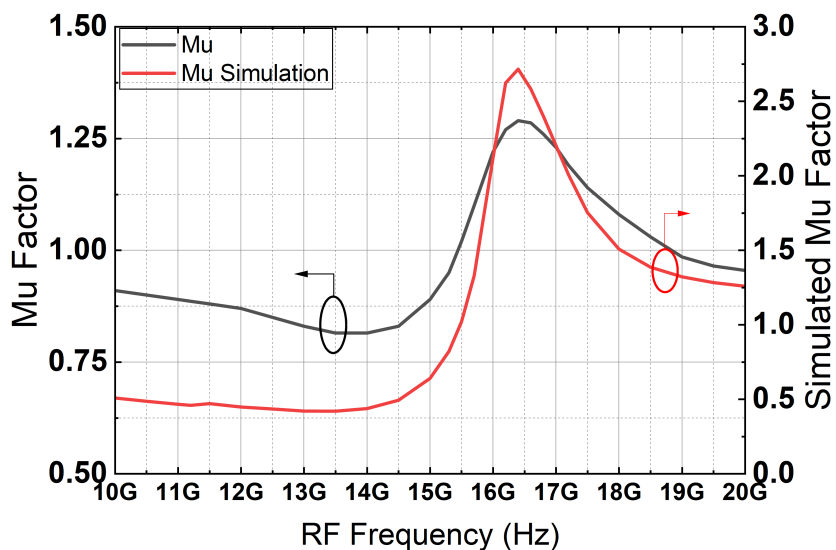


Figure 2.7: Comparison of simulated and measured Mu factor.

result from layout parasitics and mutual inductive coupling effects that were not fully captured by the electromagnetic simulation, highlighting the sensitivity of neutralized amplifier topologies to layout-dependent parasitic effects.

A post-measurement simulation with measured S-parameters is conducted. The stability is improved as the input of the transistor is matched, suggesting reflections are a factor affecting the stability of the circuit.

2.2.4 Smith chart results

As shown in Fig 2.5, the circuit's input is not matched. This flaw is not captured in the partial EMX simulation before chip fabrication due to time constraints. The partial EMX simulation is conducted with only desecrated matching networks and components simulated, which did not capture the coupling between the input matching inductor and the feedback inductor. The full layout EMX simulation is conducted after chip fabrication, and the result is close to the measurement.

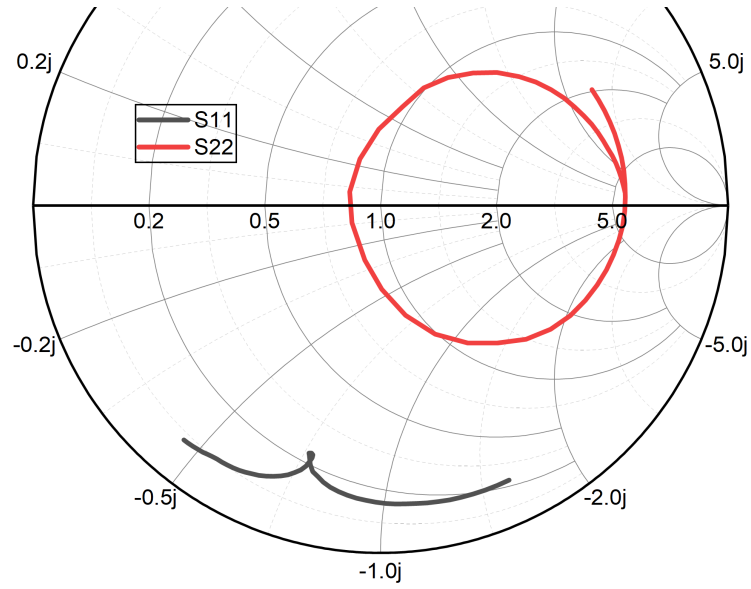


Figure 2.8: Measured Smith Chart results.

Fig 2.8 shows the Smith chart of input and output S-parameters, illustrating how the output matching network successfully matches the circuit, while an additional series inductor and shunt capacitor are needed for the input matching.

Chapter 3

Conclusion and Future Work

3.1 Conclusion

This thesis has demonstrated a Ku-band complementary BJT amplifier employing an inductive neutralization technique. The primary contribution of this work is the application of inductive neutralization to a complementary NPN–PNP amplifier topology, enabling the simultaneous exploitation of the gain enhancement provided by both the complementary transistor pair and the feedback inductor. Analytical and simulation results show that the neutralization network effectively reduces the impact of the transistor overlap capacitance, resulting in improved current gain and reduced reverse signal coupling.

Circuit simulations based on a partially EMX-extracted layout predicted a peak gain of approximately 17 dB. Although the full-layout EMX simulations and measured results exhibited lower gain than initially expected, the overall trends remained consistent with the partial EMX simulations. The measured amplifier achieved an average gain of approximately 9 dB near 15.5 GHz while maintaining a measured noise figure of approximately 4.9 dB. These results validate the effectiveness of inductive neutralization in complementary amplifier architectures and demonstrate the feasibility of using this technique to mitigate overlap-capacitance-related limitations in RF amplifier design.

The measured results also revealed challenges associated with layout-dependent parasitic effects and stability. Electromagnetic coupling between the feedback induc-

tor and the input matching network introduced discrepancies between simulation and measurement and contributed to reduced stability at lower frequencies.

3.2 Future Work

As shown in both Fig. 2.5 and Fig. 2.3, the proposed amplifier exhibits its optimum performance over a relatively narrow bandwidth. One possible approach to extending the bandwidth is to cascade multiple amplifier stages, each optimized for a different but adjacent frequency band. By appropriately staggering the peak-gain frequencies of the individual stages, a broader overall frequency response can be achieved while maintaining adequate gain across the desired operating range. [13] [12]

In addition, the bandwidth of the inductive neutralization network can be adjusted by introducing a series resistor in the feedback path. The added resistance reduces the quality factor (Q) of the resonant network, thereby broadening the frequency response and improving stability. However, this approach introduces several tradeoffs. The resistor generates additional thermal noise, which degrades the overall noise figure, and reduces the peak gain by lowering the effective impedance of the resonant feedback network. Consequently, careful optimization of the feedback resistance is required to achieve an appropriate balance among gain, bandwidth, stability, and noise performance.

Another important area for future work is the improvement of electromagnetic modeling and layout optimization. The measured results indicate that parasitic coupling between the feedback inductor and the input matching network significantly affects both stability and impedance matching. More comprehensive full-wave electromagnetic simulations, combined with optimized inductor placement and shielding techniques, may reduce these parasitic effects and improve agreement between simulation and measurement. Such improvements could enable the amplifier to achieve performance closer to

that predicted by the idealized circuit simulations.

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