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***Abstract*—Single-phase grid-connected converters typically require reactive buffering on the dc bus to maintain a constant dc power in the presence of ac-side twice-line-frequency power pulsation. Compared to bulky passive capacitors, active buffers can process higher amounts of power with reduced capacitance requirements. This paper investigates a method for energy storage reduction in the capacitors of the series-stacked buffer (SSB) utilizing deliberate ac-side current harmonic injections within IEC61000-3-2 regulatory limits. This work outlines the theory behind harmonic injection in the active buffer, demonstrates a digital control implementation, and provides hardware verification showing that appropriately injected harmonics can be used to reduce the energy stored and thus the capacitance required in each SSB capacitor.**

***Index Terms*—power pulsation buffering, grid-tied converter, harmonic injection, active buffer**

I. Introduction

Twice-line-frequency power pulsation buffers decouple the dc and ac buses in single-phase systems, which is critical in grid-interfacing applications where a constant dc-side power is required [1]–[5]. Traditionally, large electrolytic capacitors that store energy during each twice-line cycle are used for the buffer stage [6]. The energy storage requirements in a passive buffer capacitor can be further reduced by allowing higher-order odd current harmonics, which still meet IEC61000-3-2 current emissions standards, into the ac side of the converter [7], [8]. Figure 1 demonstrates that with an added third harmonic, the net energy flowing into and out of a buffering capacitor, found by integrating the power over a half twice-line period T_{2l}, can be reduced in comparison to the case with no added higher order harmonics.

The usable energy stored in (or released from) the buffer per twice-line cycle is described by the integral of instantaneous power below (or above) its dc offset, shown in (1).

$$W_{store} = \int_0^{\frac{T_{2l}}{2}} P_{buff}(t)\,\mathrm{d}t \tag{1}$$

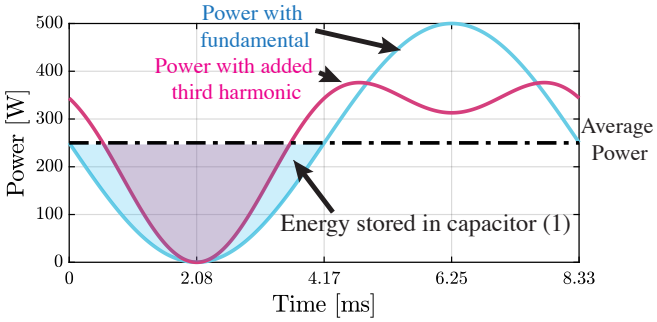

Fig. 1. Instantaneous power processed by the twice-line-frequency power pulsation buffer with and without an added third harmonic.

For the case with just the fundamental harmonic, this integral is evaluated as

$$W_{store_{fund.}} = \frac{P_{in}}{\omega}. \tag{2}$$

As odd harmonics are added, the required energy storage is reduced as the limits of integration are narrowed. Similarly, the peak-to-peak voltage ripple on a buffer capacitor is reduced by the harmonic content in the voltage waveform, minimizing (3), the equation for energy buffered in a capacitor per twice-line cycle.

$$W_{store} = \frac{1}{2}CV_{max}^2 - \frac{1}{2}CV_{min}^2 \tag{3}$$

The limits posed by IEC61000-3-2 are shown in Table I. Class D refers to the allowable limits for devices operating at $75 - 600$ W, while Class A applies to some devices above 600W. An example ac-side current i_{ac} with the maximum allowable third and fifth harmonics for IEC61000-3-2 Class D is shown in Fig. 2. The current drawn on the dc side of the dc-ac device is also distorted by these harmonics, and is represented by $i_{pulsate}$.

For the passive buffer solution using the IEC61000-3-2 Class D emissions standards as limits for harmonic injection, there is a possible energy storage reduction of 44% for the full third harmonic, 55% for the full third and fifth harmonics,

TABLE I
IEC61000-3-2 CLASS D & CLASS A HARMONIC LIMITS

n^{th} Harmonic	Class D Limit (mA/W)	Class A Absolute Limit (A)
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13	$3.85/n$	0.21
$15 \leq n \leq 39$	$3.85/n$	$0.15 \cdot 15/n$

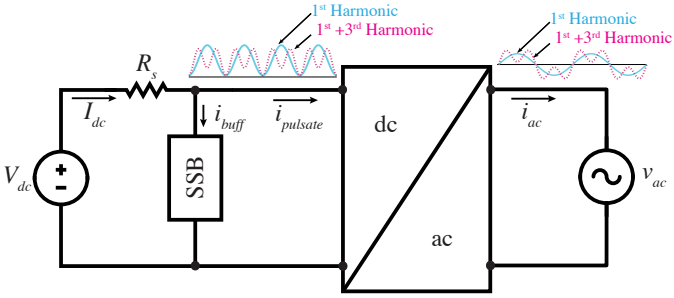

Fig. 2. System-level schematic showing the third harmonic injection in the current of a dc-ac device.

and 61.5% if all allowable harmonics are used [8]. For the purposes of this paper, only the third and fifth harmonics are considered, as it is impractical to inject all harmonics, particularly as the required filtering used in the control scheme would become increasingly complex and have poor transient response. While passive buffers are easily implemented, they are much larger in volume and weight in comparison to advanced active twice-line frequency buffer topologies such as the series-stacked buffer (SSB), which may be preferred in weight and volume-restricted applications [2]. The SSB combines a primary energy buffer capacitor C_1 that is in series with an H-bridge auxillary converter, as shown in Fig. 3. With the appropriate control, this allows for a larger voltage ripple across C_1 and thus allows C_1 to achieve a greater energy utilization ratio [9]. Much of the large capacitance required for the passive solution is essentially replaced by an active switching and control scheme.

This paper explores the use of odd harmonics in the ac-side current to significantly reduce the energy storage requirements of the capacitive components in the SSB and further improve overall power density. The remainder of this paper is organized as follows: Section II explores the theory behind deliberate harmonic injection into the SSB, and Section III presents the control scheme. Lastly, Section IV describes the experimental validation of the proposed concept for both Class D and Class A harmonics.

II. DERIVATIONS FOR HARMONIC INJECTION IN THE SERIES STACKED BUFFER

Consider the single-phase inverter modeled with dc input voltage V_{dc} and ac load current $i_{pulsate} = \frac{v_{ac}(t)\ i_{ac}(t)}{v_{bus}}$ as shown in Fig. 3. Note that although a dc-ac system is considered in this case, the analysis applies equally well for an ac-dc case. The SSB is tied to the dc bus to provide twice-line frequency power pulsation to keep the voltage on the dc bus constant. The main energy storage capacitor C_1 is in series with an H-bridge auxiliary converter, which together behave as a low impedance branch to shunt the ac twice-line frequency current [10]. Capacitor C_2 acts as an approximate dc voltage source for the H-bridge converter.

A. SSB Theory of Operation

In order to characterize the voltages across each SSB capacitor, the power through the buffer can be used to relate the currents through each capacitor. In a system with no harmonic content, the instantaneous dc input and ac output power respectively are

$$P_{dc} = I_{dc}\, V_{dc} \tag{4}$$

and

$$\begin{aligned} P_{ac}(t) &= v_{ac}(t)\, i_{ac}(t) \\ &= V_1 \sin(\omega t) \cdot I_1 \sin(\omega t) = V_1 I_1 \frac{1-\cos(2\omega t)}{2}. \end{aligned} \tag{5}$$

Ideally, the inverter-side current is defined as

$$i_{pulsate} = \frac{P_{ac}}{v_{bus}}, \tag{6}$$

where v_{bus} is the dc voltage at the node where the buffer is connected.

The power processed by the buffer, P_{buff}, is the difference between the input and output power. We use this to derive an expression for the current through the buffer. Within the SSB, (7) and (8) relate the buffer current to the current through C_1, and can be used to solve for $v_{C_1}(t)$.

$$i_{buff}(t) = \frac{P_{dc}(t) - P_{ac}(t)}{v_{bus}} \tag{7}$$

We also know that the buffer current is the same as the current through C_1:

$$i_{buff}(t) = i_{C_1}(t) = C_1 \frac{dv_{C1}}{dt}. \tag{8}$$

This makes it possible to solve for $v_{C1}(t)$ as

$$v_{C_1}(t) = \frac{1}{C_1} \int_0^t i_{buff}(t)\, \mathrm{d}t. \tag{9}$$

Additionally, the power through the ab terminals and the power flowing through C_2 are equivalent, making it possible to solve for $v_{C_2}(t)$ using (10) since $v_{ab} = v_{bus} - v_{C_1}$ [9].

$$v_{ab}(t) \cdot i_{buff}(t) = v_{C_2}(t) \cdot C_2 \frac{dv_{C_2}(t)}{dt}. \tag{10}$$

This results in an equation that can be evaluated via integration and separation of variables, shown in (11).

$$\int v_{C_2}(t) \frac{dv_{C_2}(t)}{dt}\, \mathrm{d}t = \frac{1}{C_2} \int v_{ab}(t) \cdot i_{buff}(t)\, \mathrm{d}t. \tag{11}$$

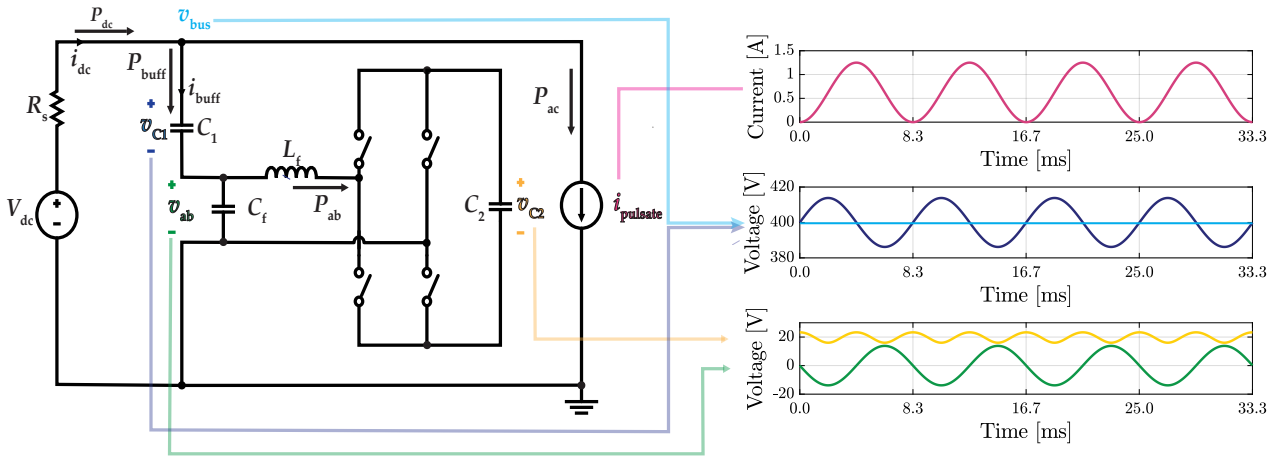

Fig. 3. Series-stacked buffer schematic with corresponding waveforms for the voltages and current $i_{pulsate}$ shown. Note that $i_{pulsate}$ is at the twice-line frequency, as are the buffer voltage waveforms.

Thus, a solution for $v_{C_2}(t)$ is found. The same method of solving for the capacitor voltages can be used for the addition of higher order harmonics. This does result in more complexity, and values are not easily found by hand.

B. Adding the Third Harmonic

If harmonics are added, i_{ac} takes the form $i_{ac}(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t)$. Allowing just the third harmonic changes the ac-side power to

$$P_{ac}(t) = V_1 \sin(\omega t)\cdot\big(I_1 \sin(\omega t) + I_3 \sin(3\omega t)\big). \quad (12)$$

The dc power remains $P_{dc} = \frac{V_1 I_1}{2}$ where V_1 and I_1 are the peak ac voltage and current respectively, and the buffer power is thus

$$P_{buff}(t) = \frac{V_1 I_1}{2} - V_1 \sin(\omega t)\cdot\big(I_1 \sin(\omega t) + I_3 \sin(3\omega t)\big). \quad (13)$$

With the harmonically injected buffer current from $P_{buff}(t)$, the voltage/current relationship of C_1 in (8) can be used to solve for $v_{C_1}(t)$ as

$$v_{C_1}(t) = v_{bus} + \frac{I_1 V_1 \sin(2\omega t)}{4 C_1 v_{bus} \omega} - \frac{I_3 V_1 \sin(2\omega t)}{4 C_1 v_{bus} \omega} + \frac{I_3 V_1 \sin(4\omega t)}{8 C_1 v_{bus} \omega}. \quad (14)$$

Substituting the expressions for $i_{buff}(t)$ and $v_{C_1}(t)$ into (10), the following is derived for $v_{C_2}(t)$:

$$v_{C_2}(t) = \Bigg[v_{C_2}^2(0) + \frac{V_1^2}{128 C_1 C_2 \omega^2 v_{bus}^2} \cdot \Big(-4(I_1 - I_3) I_3 \cos(2\omega t) + 4(I_1 - I_3)^2 \cos(4\omega t) + 4 I_3 (I_1 - I_3) \cos(6\omega t) + I_3 \cos(8\omega t)\Big)\Bigg]^{1/2}, \quad (15)$$

where $v_{C_2}(0)$ is the desired initial voltage and dc voltage offset of C_2.

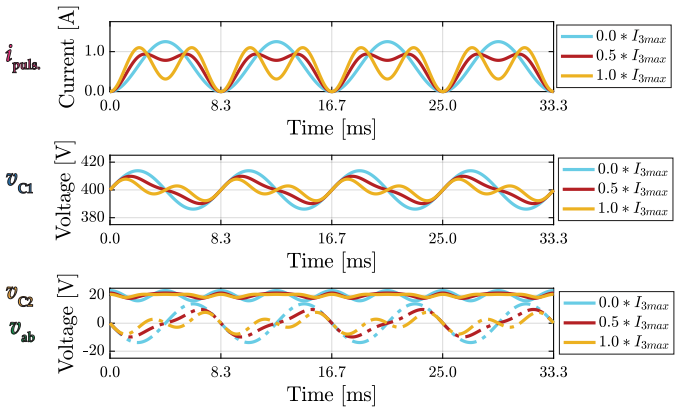

Fig. 4. $i_{puls.}(t)$, $v_{C_1}(t)$, $v_{C_2}(t)$, $v_{ab}(t)$ for 0%, 50% and 100% of the allowable third harmonic.

The characteristic equations in (14) and (15) enable the determination of possible energy storage reductions in each capacitor using (3). Figure 4 shows the waveforms for various levels of third harmonic content for a 250 W system with $V_1 = 220\sqrt{2}$ V, $V_{dc} = 400$ V, $C_1 = 60$ μF, and $C_2 = 40$ μF. The maximum amount $I_{3,max}$ is set by the IEC61000-3-2 Class D limits, and scales with power level. Note that the ac-side current is defined as $i_{puls.} = \frac{v_{ac}(t) i_{ac}(t)}{v_{bus}}$, hence the twice-line frequency and the trough at fixed points in time in Fig. 4. The required capacitance can be reduced with the proposed technique. The peak of $v_{C_1}(t)$ must be less than the trough of $v_{C_2}(t)$, which can be described by the inequality $|\frac{v_{ab}(t)}{v_{C_2}(t)}| \leq 1$ [9]. It is then possible to solve for values of C_1 and C_2 which satisfy the inequality, and the minimum C_1 and C_2 required to ensure operation for third harmonic injection is shown in Fig. 5. Note that $v_{C_2}(t)$ is a function of $v_{C_2}(0)$, which is fixed as $v_{C_2}(0) = 20$V for hardware testing. Several operating points are shown that enable capacitance reductions with harmonic injection.

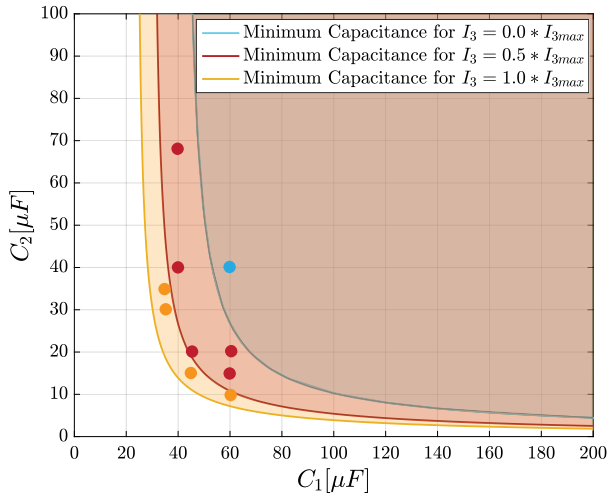

Fig. 5. Plot of C_2 versus C_1 showing the minimum required capacitance for operation, and points for combinations used in hardware.

III. Control

One of the primary challenges associated with injecting harmonics into the SSB is the isolation of the desired harmonics such that a reference control voltage for v_{ab} may be constructed. Figure 6 illustrates the control schematic developed in this work to address this challenge. The controller implementation consists of two parts: a reference voltage for v_{ab} and loss compensation.

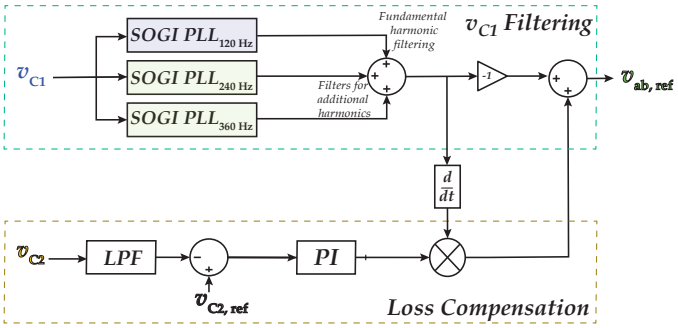

Fig. 6. Control scheme showing the use of PLL filters to create a reference voltage for v_{ab} and enable the loss compensation for C_2.

A. Reference Voltage for v_{ab}

The first segment of the controller involves second order generalized integrator (SOGI) phase-locked loop (PLL) filters, which are used to isolate the harmonics present in v_{C_1} [11]. The filtered waveforms are added to form an ideal reference voltage for v_{C_1}, which is used to create the antiphase waveform v_{ab}. The advantages of using SOGI PLL filters as an alternative to bandpass filters are discussed in [12]. In the hardware and the in simulation of this work, SOGI PLL filters have been shown to be more stable and less susceptible to noise than the bandpass filters used in [10].

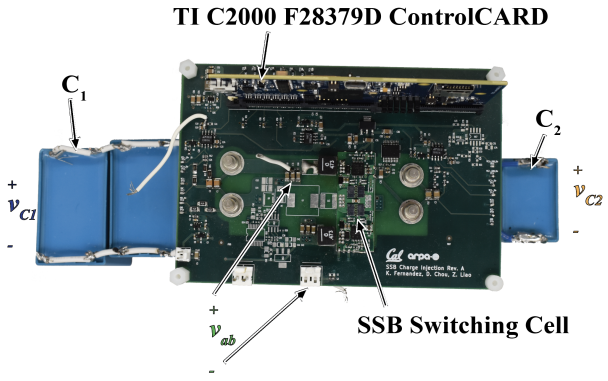

Fig. 7. Labeled hardware showing reference probe points for the voltages of interest. Note that the film capacitors were easily switched out via banana plugs.

B. Loss Compensation

The second portion of the controller is the loss compensation control which injects charge into C_2 to keep its dc voltage constant. Without the loss compensation, the voltage across C_2 decays as the capacitor loses charge due to power conversion losses, causing v_{C_2} and thus v_{ab} to saturate. For this portion of the control, a lowpass filter is used to isolate the dc voltage of v_{C_2}. While multiple filters were used to isolate the harmonics present in v_{C_1}, only a 120 Hz filter is needed for this portion of the control loop. To prevent the saturation of v_{C_2} and v_{ab}, we want to prevent the voltage peaks of v_{ab} from "touching" the troughs of v_{C_2} (i.e., $v_{C_2} > v_{ab}$). When no harmonics are injected and only the 120 Hz frequency is present, the voltage ripple is maximized and thus the worst case is represented. Considering this case alone in control ensures that for a given $v_{C_2,ref}$, saturation will not occur regardless of higher order harmonics being present.

IV. Hardware Validation

For the system previously described, hardware validation is provided for both Class D and Class A harmonic injection, ranging from 250 W to 1 kW. This hardware validation also shows the reduction in capacitance illustrated in Fig. 5.

A. Hardware Validation for Class D Harmonics

Figure 7 shows the full prototype including the TI C2000 F28379D ControlCARD. Capacitors C_1 and C_2 are large Polyethylene Terephthalate (PET) film capacitors, and are initially set to 60 μF and 40 μF respectively. The SSB is implemented in hardware for the 250 W system. The hardware prototype produces the waveforms shown in Fig. 8 and Fig. 9 for the first and third harmonics respectively. The voltage ripple decreases as harmonics are added such that the energy stored in the capacitor is reduced. The injection of the allowable fifth harmonic in addition to the third is shown in Fig. 10, where the hardware results are compared to the theoretical values. Strong agreement between simulation and experiment is observed.

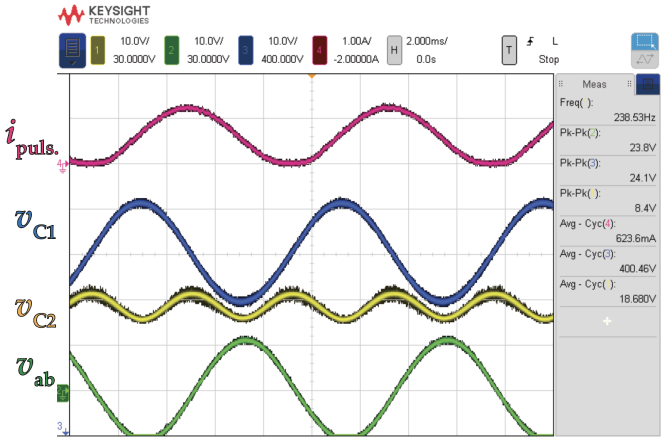

Fig. 8. Oscilloscope waveforms for 250W with no harmonic injection.

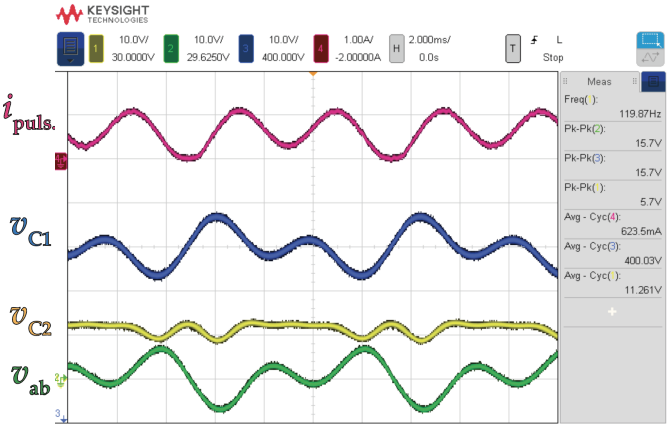

Fig. 9. Oscilloscope waveforms for 250W with 100% of the third harmonic injected.

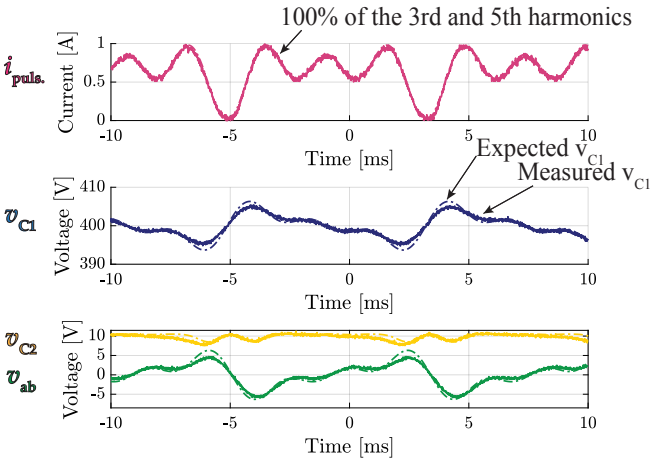

Fig. 10. Expected theoretical values and hardware results for 100% injection of both the third and fifth harmonics.

To better compare the energy density of the the SSB, the required dc-link equivalent capacitance for a passive solution

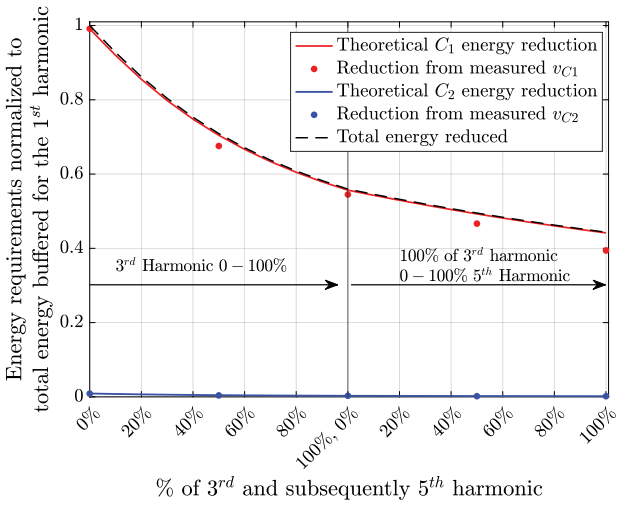

Fig. 11. Plot showing the normalized reduction in buffered energy for $C_1 = 60\mu$F and $C_2 = 40\mu$F.

TABLE II
PEAK ENERGY STORED IN THE SSB CAPACITORS COMPARED TO AN EQUIVALENT PASSIVE SOLUTION.

Capacitor	**1st Harmonic**		**1st + 3rd Harmonic**	
	C	$\frac{1}{2}C\,V^2_{\max}$	C_{eq}	$\frac{1}{2}C_{eq}\,V^2_{\max}$
Passive Buffer	753 μF	60.6 J	422 μF	33.9 J
SSB C_1	60 μF	5.14 J	34 μF	2.90 J
SSB C_2	40 μF ($> 27\mu$F)	0.011 J	20 μF	0.005J

is calculated using an estimated bus voltage ripple of 2.2 V. To achieve this ripple, a capacitance of 753 μF is required, found using (3). The peak energy stored in the passive solution is estimated using $\frac{1}{2}CV^2_{max}$. The injection of the third harmonic makes it possible to reduce the capacitance while holding the peak-to-peak voltage ripple fixed. The comparison of this energy storage to that of the SSB capacitors is shown in Table II. The SSB not only uses smaller capacitors than an equivalent dc-link passive solution, but requires a smaller amount of peak energy. In the case for the SSB, the peak-to-peak voltage ripple across C_1 is held constant for different levels of harmonic injection, as C_1 accounts for the nearly all of the stored energy in the SSB. It is then possible to solve for an equivalent required capacitance for C_1 when harmonics are injected. Then, using the curve of C_2 as a function of C_1 in Fig. 5, C_2 is found for the new potential value for C_1, and the peak energy stored may be computed. Note that for no added harmonic, Fig. 5 dictates that for $C_1 = 60\mu$F, $C_2 = 27\mu$F is required. With the third harmonic this is reduced to 20μF for the new required C_1. Increasing the dc-offset of the voltage across capacitor C_2 would enable the use of a smaller capacitance, but it would need to be rated for higher voltage.

The normalized reduction in energy buffered introduced

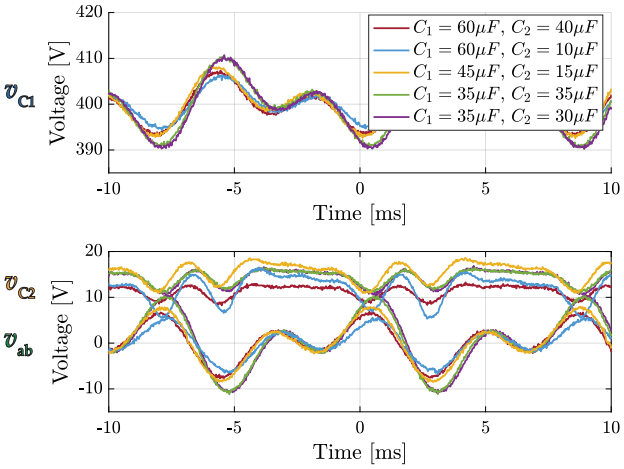

Fig. 12. Plot showing scope data for varying levels of capacitance for 100% of the third harmonic added.

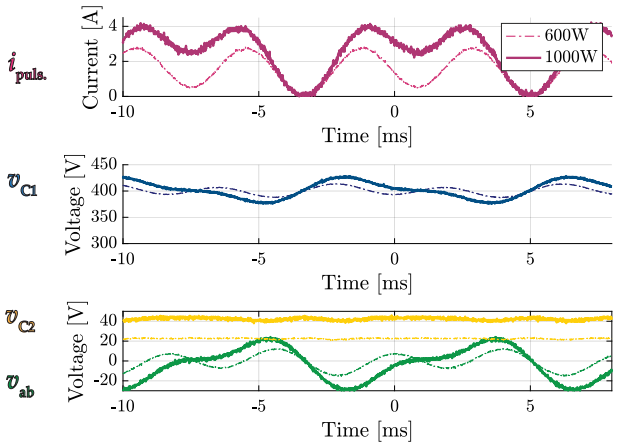

Fig. 13. Plot showing oscilloscope data for $C_1 = 60$ μF and $C_2 = 40$ μF, 100% of the third harmonic added for both 600 W and 1 kW.

by the addition of harmonic content is shown in Fig. 11. The dotted line shows the full buffered energy reduction for the active buffer and overlaps significantly with the energy reduction of C_1, the main energy storage capacitor. The energy buffered by C_2 accounts for a negligible amount of energy buffered by the entire system. The addition of the third and fifth harmonic results in a buffered energy reduction of 55% which is the same as the passive solution [8]. This is consistent with what is expected—the buffered energy storage calculated using (3) is not changed or increased for the active buffer, but is split between two smaller capacitors.

The reduction in required energy storage also enables the reduction in required capacitance. The active buffer hardware prototype was evaluated with a range of different capacitor combinations, shown visually in Fig. 5. As capacitance is reduced, the maximum voltage ripple increases such that v_{ab} and v_{C_2} nearly touch. The elimination of injected harmonics would cause v_{ab} and v_{C_2} to saturate and the buffer to not work.

B. Hardware Validation for Class A Harmonics

Hardware results are obtained for Class A Harmonics. For the addition of each harmonic, absolute harmonic limits are set, allowing for the addition of 2.30 A and 1.14 A average amplitudes for the third and fifth harmonics respectively. The hardware was tested for 600 W and 1 kW, and results are shown in Fig. 13 for both power levels at 100% of the full third harmonic injected. Note that as the power level is increased, as Class A permits an absolute limit, the voltage ripple is less drastically reduced, and subsequently the required energy storage is not reduced as much from the no harmonic case. This suggests the technique of injecting harmonics is comparably more useful at lower power levels for buffering.

V. Conclusion

This paper has illustrated how injecting harmonics on the ac side of a single-phase converter with a series-stacked active buffer can reduce the overall capacitance requirement by reducing the required energy stored. Moreover, a theoretical derivation of the control parameters, a digital control algorithm and implementation, and hardware validation has been presented. The proposed harmonic injection for the SSB affords energy reductions in both C_1 and C_2 such that we can drastically reduce the required capacitances. Hardware results are provided for several capacitance levels for Class D harmonic injection, some of which are only possible with added harmonic content. Lastly, hardware results for IEC61000-3-2 Class A standards at 600 W and 1 kW are provided, and show that as power levels increase the benefits of harmonic injection are diminished.

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