UNIVERSITY OF CALIFORNIA, SAN DIEGO

Enabling Millimeter-wave Circuit Techniques for High Data Rate Communication

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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2017

The dissertation of Najme Ebrahimiseraji is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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DEDICATION

To my family

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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Chapter 3 is mostly a reprint of the material as it appears in N. Ebrahimi, P. Wu, m. Bagheri and J. F. Buckwalter, "A 71-86 GHz Bidirectional Phased-Array Transceiver using Wide-bandwidth Injection-locked Oscillator Phase shifter", IEEE Transactions on Microwave Theory and Techniques, 2017. The dissertation author was the primary investigator and author of this paper and materials.

Chapter 4 is mostly a reprint of the material as it will be appeared in N. Ebrahimi and J. F. Buckwalter, "A 71-86 GHz Bidirectional Image Selection Transceiver Architecture", IEEE RFIC Conference, 2017 and will be submitted to N. Ebrahimi and J. F. Buckwalter, "A 12 Gb/s 71-86 GHz Bidirectional Front-end with Novel Image-selection Weaver Mixer for high data rate communications", IEEE Journal of Solid-State Circuits, 2017. The dissertation author was the primary investigator and author of these papers and materials.

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N. Ebrahimi and J. F. Buckwalter, "A 71-86 GHz Bidirectional Image Selection Transceiver Architecture", *IEEE RFIC Conference, 2017*, accepted.

N. Ebrahimi, P. Wu, m. Bagheri and J. F. Buckwalter, "A 71-86 GHz Bidirectional Phased-Array Transceiver using Wide-bandwidth Injection-locked Oscillator Phase shifter", *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 346-361, February 2017.

N. Ebrahimi and J. F. Buckwalter, "Robustness of Injection-locked Oscillators to CMOS Process Tolerance", *International Conference in Theory and Application in Nonlinear Dynamics (ICAND), Springer, Publication, 2016.*

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ABSTRACT OF THE DISSERTATION

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Najme Ebrahimiseraji

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This dissertation has been mainly focused on reconfigurable mm-wave integrated circuits for next generation wireless communication systems (namely, 5G). One of the major approaches to making 5G a reality is the use of high-frequency signals in the millimeter-wave (mm-wave) frequency band to facilitate access to more bandwidth. This can deliver faster and more reliable data to more users. This dissertation contributes to making wideband, bidirectional, and scalable RFICs for high data rate point-to-point communications over large distances in mm-wave bands, particularly the E-band (71-76 GHz, 81-86 GHz). The E-band is a licensed band in the US, with 10 GHz of bandwidth allocated to low-cost, high-capacity,

and point-to-point communication. For backhaul base-stations or air-to-ground communication, a scalable and large-element phased array is desired to acquire the appropriate isotropic radiated power and signal to noise ratio. Additionally, bidirectional operation supporting transmit (TX) and receive (RX) in a single aperture is desirable to minimize the area and save power. This dissertation has focused on new architectures for scalable, bidirectional, and wideband phased arrays using IBM's fastest SiGe technology, 90 nm.

In this dissertation, the first E-band scalable phased-array transceiver is proposed based on coupled oscillator architecture. Coupled oscillator phased arrays have the advantage of low power and low complexity, resulting in an architecture that easily scales to the number of elements as multiple die can be aggregated to form a larger array through local oscillator (LO) power distribution and intermediate frequency (IF) power combining. However, silicon processes introduce undesirable parasitics and manufacturing tolerances to the transistor and passive devices. When multiple oscillators are present in a single die, the oscillators couple through the substrate. The substrate coupling introduces additional parasitic coupling paths between oscillators; this causes pulling and, consequently, amplitude and phase variation between the oscillators. In addition, the parasitics from the injection node to the substrate deviate the ILO performance from its ideal behavior. Conventional analysis of the amplitude and phase noise typically ignores the effect of the silicon substrate parasitic effects.

This dissertation investigated the nonlinear dynamics of an injection-locked oscillator (ILO), where the effective circuit parameters of ILO performance were observed. More specifically, new amplitude and phase equations are derived that took into account the transistor's device parasitics and silicon substrate's parasitic coupling effects, including the transistor injection node parasitic capacitance (C_P), substrate parasitic conductive (R_{sub}) and dielectric (C_j) features. The derived models are compared with both the simulation and measurement results.

The proposed 2x2 transceiver phased array block diagram described in this dissertation employs 4 injection-locked oscillators (ILOs) operating at a lower frequency range (in this case, 1/4 of the desired LO frequency), followed by a fre-

quency quadrupler, to form a beam in transmit and receive modes. The bidirectional front-end is designed to operate at E-band within 3-dB bandwidth. Since the ILO-based phase shifting is technically challenging at millimeter-wave bands due to the parasitics of the injection circuitry and the oscillator phase noise trade-offs, the high-frequency limitations of the ILO phase shifter is considered and wide locking range and a less parasitic sensitive solution for current injection using folded-cascode architecture is proposed. The proposed ILO-based phase array architecture result in low phase noise and low channel to channel isolation supporting 6 Gb/s data rate at 256 QAM modulation.

The conventional architectures of the E-band transceiver require a wide tuning range, around 10 GHz, for the LO signal and wide-bandwidth IF blocks. The wide-bandwidth requirement of LO and IF frequency for mm-waves increases the power consumption and complexity of the system. This dissertation proposes a novel architecture, named the "Image-selection" E-band phased array. This new architecture makes the upper-band (81-86 GHz) and the lower-band (71-76 GHz) of the E-band spectrum images of each other in comparison to the LO signal, which is located at the center frequency (78.5 GHz). Therefore, an image rejection architecture is desired to select the wanted band while rejecting the other. The significant advantage of this architecture is that it only requires an LO with the quadrature phases within a tuning range lower than 1 GHz . This will relax the system design trade-offs to the circuit impairments. For bidirectional operation purpose and preventing use of quadrature generation circuitry at direct intermediate frequency (IF) or radio frequency (RF) signal paths, sliding-IF weaver architecture mixers are employed with the phase inverter in the divider path to select the upper or lower band. This architecture leads in to a flat conversion gain over the bandwidth and low amplitude and phase imbalance. The achieved QAM modulation data rate from this technique is the state of art,najmebiMon May 29 19:43:48 2017 9Gb/s (64 QAM) with less than 5% EVM and 12 Gb/s (16 QAM) with less than 10% EVM.

Chapter 1

High data-rate High-speed Wireless Communications

Two major trends have emerged in wireless technology, these being ultra-high-data-rate mobile communications and the massive connectivity of machines through network protocols, called the Internet of Things (IoT), both of which necessitate a new wireless access technology, namely 5G [1, 2]. The applications of 5G and IOT include smart cities, home automation, vehicle connectivity, cloud computing services, e-health, and many more. Development of these new technologies require a significant flexibility in reliability, bandwidth, the maintenance of ultra-low-latency connections and power efficiency. To meet these requirements, academia and industry have made efforts to develop new system interfaces and technologies such as massive multiple-input multiple-output (MIMO) antennas, beamforming, operations at mm-wave frequencies, and scalable large-element radio architectures, Fig. 1.1. Millimeter-wave phased arrays have been demonstrated for both 60-GHz short-range communications ([3] to [12]) and point-to-point communication at E band (71-76 & 81-86 GHz) and W band (75-110 GHz), ([13] to [18]). Among the different mm-wave frequency and spectrum allocations, E-band from 71-76 GHz and 81-86 GHz [19–22], provides the widest spectrum by far having 5 GHz bandwidth per band, which makes it an excellent candidate for multigigabit data rate over long distance, e.g 1 km, communications. The other advantages of this frequency range, 71-86 GHz, is the low atmospheric loss com-

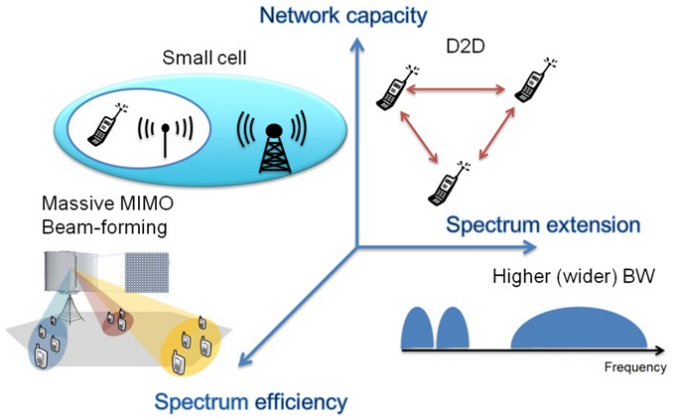


Figure 1.1: Road to 5G.

pared to other mm-wave or microwave bands such as 60 GHz. Due to the short wavelength, the antenna gain is high at this frequency band providing high directivity and high efficient beam-former. Recently, E band has been proposed for ground-to-air backhaul links to provide internet access to under-served areas where infrastructure might be economically unfeasible [23]. In addition to these features, the compatibility of E band with other RF and millimeter-wave bands for access networks make it a strong candidate for future 5G networks, Fig. 1.2. A scalable phased-array is desired for backhaul base-stations communications to obtain the desired signal-to-noise ratio (SNR) and effective isotropic radiated power (EIRP) through spatial power combining and interference mitigation. Additionally, bidirectional operation supporting transmit (TX) and receive (RX) in a single aperture is desirable to save area and power while supporting multiple-input/multi-output (MIMO) mesh networks [8, 24]. Scaled CMOS and BiCMOS technologies allow low-cost phased array integration. Specifically, SiGe BiCMOS has made significant technology advancements to provide f_T/f_{max} as high as 300 GHz/350 GHz in the 90-nm node [25, 26]. Achieving high data rate communications for 5 G and IoT applications requires developing new architecture and circuit techniques to provide low complex and low power system to mitigate the nonideal impairments of wide bandwidth circuits. The CMOS circuit is also prone to device mismatches and other fabrication non-idealities requiring complex calibration blocks in a high data

rate quadrature amplitude modulation (QAM) systems.

Figure 1.2: mm-wave E-band applications.

1.1 Injection-Locked Oscillator Phase Shifter, High-frequency Design and Trade-offs

Synchronized and coupled oscillators have received attentions for different applications. Nonlinear dynamics of oscillators have a great potential to realize signal modulation and demodulation with low power. For example, for secure communication, the inherent noise of coupled oscillators is added to the transmitted signal and subtracted with a synchronized oscillator in the receiver side [27, 28]. Coupled lasers have also rates due to fast dynamics [29–31]. For electronic systems, phased array and grid amplifiers are two areas that could benefit from synchronized nonlinear oscillators. Phased arrays increase the effective isotropic radiated power, EIRP, and signal to noise ratio, SNR, of a communication link. Coupled oscillator phased arrays have the advantage of low-power and low-complexity, providing a phased-array architecture that easily scales the number of elements. However, the size of the array decreases and the power required to lock the array increases with larger variation between oscillator elements [32,33]. Silicon and Silicon-Germanium BiCMOS integrated circuits are the important technologies for the implementation of phased array systems in microwave and millimeter-wave regimes, primarily because of the low-cost of silicon processing and the yield of the processes. However, silicon processes also introduce undesirable parasitics and manufacturing toler-

ances on the transistor and passive devices. As silicon processes scale, these parasitic effects are a greater percentage of the device parameters and these tolerances strongly impact the nonlinear dynamics from a CMOS-based injection-locked oscillator (ILO). For instance, recent technology nodes, such as 90-nm SiGe offer high f_T/f_{max} (300 GHz/350 GHz), however, these parameters vary as much as +/-20%. Tuning range, phase noise, locking range, phase shifting range and power consumption are common trade-offs for high-frequency, wideband oscillators and ILOs. It is well-known that parasitics of MOSFETs and bipolar junction transistors (BJTs) impact the tuning range and phase noise of the oscillator and locking range and phase shift range of ILO. Therefore, the ILO-based phase shifting is technically challenging at millimeter-wave bands due to the parasitic capacitance of the injection circuitry, which limit the ILO phase shifter performance for high-frequency and wideband applications. In addition, when multiple oscillators are present in a single die, the oscillators couple through the substrate. The substrate coupling introduces additional parasitic coupling paths between oscillators, which causes pulling and, consequently, amplitude and phase variation between the oscillators. The substrate coupling effectively reduces isolation between each oscillator.

1.2 Scalable High Data-rate Phased Array using Wideband Injection-locked Oscillator Phase Shifter

Scalable phased arrays have been proposed in three different architectures: digital/IF beamforming [34,35], RF phase shifting ([6]to [12]) , ([15]to [18]) and LO phase shifting ([3]to [5]), [13,14], [36,37], Fig. 1.3. Digital beamformers support phase-shifting in the digital domain and readily scale to multiple elements. However, each signal path requires high linearity since the spatial filtering occurs in the digital signal processing (DSP) unit and, therefore, requires high analog-to-digital converter (ADC) resolution and dynamic range and typically incurs high power consumption. Radio frequency (RF) phase shifting forms the beam before

the down-conversion mixer, relaxing the linearity requirement. However, RF phase shifting introduces loss and mismatch to the RF signal. Therefore, calibration circuits are needed to compensate the loss [38]. Local oscillator (LO) path phase shifting avoids loss and noise in the RF signal path and is well-suited for bidirectional operation. By incorporating low-frequency LO and intermediate frequency (IF) signals, an array chip can be scaled to multiple elements through combining and splitting the IF and LO signals.

LO phase shifting was proposed with a central multi-phase voltage-controlled

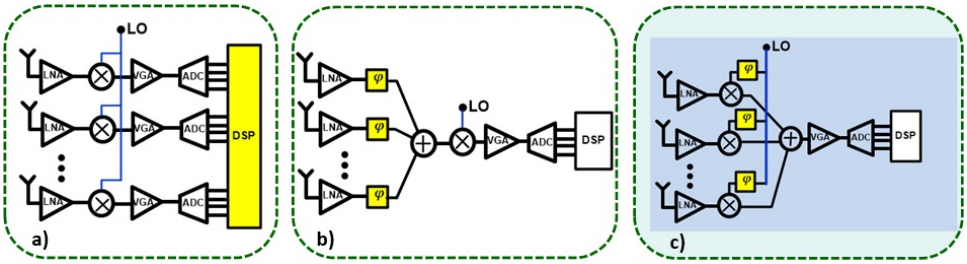


Figure 1.3: Scalable phased-array architectures, a) digital Beam-former), b) RF phase-shifting , c) LO phase-shifting.

oscillator (VCO) that generates discrete phase states distributed to each array element at the expense of significant area and power consumption [37]. Additionally, the phase resolution is limited to the number of distributed phases. An I/Q phase interpolator was proposed at each mixer to compensate for phase skew, incurring additional power penalties [13]. Injection-locked oscillators (ILOs) were originally proposed for microwave phased arrays implemented with discrete devices [39, 40] and were proposed for CMOS integration as a low-power alternative to LO phase shifting [41–43]. In this scheme, the phase shift is introduced through injection locking in oscillators [44]. However, the challenges and the trade-offs that ILO-based phase shifter encounters at the high-frequency regime such as the phase noise, injection circuit parasitics and substrare parasitice limits the ILO phase shifter performance and the number of elements in the each of the scalable array chip. Distribution of a millimeter-wave reference signal across the chip is also lossy and reduces the locking range and increases the required power to lock the array of phase shifters as described in chapter 1.1.

In this chapter, a fully-integrated 2 x 2 transmit and receive (transceiver) phased array is presented for the first time that uses wideband (62-72 GHz) ILO array for phase shifting. Each array element front-end implements a wideband bidirectional transceiver path that covers E band. Considering the high-frequency limitations of the ILO phase shifter, a wide locking range and less parasitic sensitive phase shifter using a folded-cascode injection architecture is designed. A wideband frequency multiplier designed that covers a 10-GHz tuning range with 23-dB power gain. Several advantages are shown for the ILO-based phase shifter including low amplitude variation across the phase range, low channel-to-channel isolation, and small amplitude errors which are verified experimentally. In addition, the improved phase noise of the injection locked system and low phase noise variation across the phase shifting range result in a 256-QAM modulation over a 750-MHz bandwidth for a data rate of 6 Gb/s.

1.3 A Novel Image Selection Bidirectional Architecture

To achieve a high data rate communication system high output power in transmit mode and wide-band operation circuit blocks are required. These factors will affect the error vector magnitude (EVM) of the communication system. Recent work on E-band and W-band show enough amount of output power on the power amplifier to transmit the required power calculated from the link budget, e.g 20 dBm. In addition, PA operation at back-off will insert the PA in the linear region and hence, the AM-AM and AM-PM issues of the PA on the E-band and W-band system can be neglected. Therefore, the wideband operation bandwidth of the down-conversion or up-conversion mixers can be considered as the main challenges. For example, the system presented in the past publications, [17,45–48], requires more than 15 GHz LO tuning range for the RF up/down conversion blocks. Furthermore, generating the quadrature signals within the wide bandwidth LO tuning range is challenging at mm-wave regime as it produces phase and amplitude mismatch within the operation bandwidth. Different schemes have been used to

produce quadrature signals at mm-wave, such as quadrature VCO (QVCO) [49], multi-stage polyphase filter (PPF) [50–52] or coupled line coupler [53]. The QVCO I/Q generation scheme requires wide-band locking range over the wide LO tuning range. Achieving wideband locking range from the oscillators over the mm-wave range is very challenging and will lead to a power hungry system. Furthermore, using a wideband multi-stage PPF as explained in [46,48] is also very lossy over the E-band and produce large I/Q imbalances. In addition, this scheme will be more sensitive to the layout of the resistance and capacitance as the number of stages increased. A compact layout for the 2-stage PPF is proposed in [48] to reduce the mismatch originated from the device sizing and mm-wave interconnects. However, it employs calibration circuit composed of switchable varactor and inductors with switchable lines. This switchable inductor and varactor needs to be wideband and are going to be lossy, which makes multi-stage PPF another power hungry option. In addition, [47] proposes a load-intensive approach with a broadband oscillator employing 45 degree power splitter in the quadrature generation path to achieve lower amplitude and phase imbalance. However, they approach has the limited bandwidth and they could only go up to 0.04 Gb/s data rate for the QAM modulation. Another quadrature generation technique is the wideband hybrid coupler. This technique produces lower loss and I/Q imbalance. However, it has a very bad isolation between the ports (13 dBc), which makes it unfavorable candidate for I/Q generation.

Consequently, the wide LO tuning range is very challenging at the mm-wave regime due to the lossy passive and parasitic elements. This results in conversion gain variation over the required wide bandwidth operation, often more 10-dB conversion gain variation across E-band. In addition, it deteriorates the phase noise of LO, and most importantly the I/Q phase and amplitude balances. Therefore, a complex and power hungry calibration circuits are required for compensation. To relax the LO tuning range, this chapter proposes the image-selection planning for the E-band transceiver. In this scheme, the LO tuning should be placed in between the 71-76 GHz band (LSB) and 81-86 GHz band (USB). The resulting 3 GHz IF band is centered at 5 GHz. Consequently, this approach requires the LO to

tune across only 3 GHz tuning range with quadrature phases and phase inverting option to select either the upper or lower image sides of LO with a 3 GHz IF bandwidth. This chapter is demonstrates that this frequency plan reduces the tuning range and results in more uniform circuit performance in terms of conversion gain and IRR. The IRR is also subject to a smaller tuning range and therefore is not prone to bandwidth induced amplitude and phase mismatch, which relaxes the PPF requirements.

1.4 Dissertation Organization

Background material, previous work and the proposed and novel contributions have been mentioned in Chapter 1. The challenges of mm-wave high data rate system and phased array has been outlined.

Chapter 2 presents the analysis of the ILO as phase-shifter. The non-linear dynamics of an LC injection-locked oscillator are derived in the presence of non-ideal effects originated from the integration of the oscillator on a silicon substrate; i.e the injection circuit parasitics and the substrate parasitics. In other words, the effects of substrate parasitics, $R_{sub,}C_{sub,}$ and injection transistor's parasitic capacitor, C_p, on amplitude and phase error of each ILO or two neighboring ILOs are discussed. The locking parameters, injected current, quality factor, and frequency detuning are discussed given the derived dynamics. The linear region performance of the high-frequency ILO phase shifter is investigated and a novel injection circuitry for the wideband high frequency ILO is proposed. The silicon substrate parasitic coupling effect on the array of ILO phase shifter is considered and the two new amplitude and phase equations were derived and compared with both the simulation and the measurements results.

Chapter 3 presents an LO-phase shifting approach based on injection-locked oscillators for operation over 71-86 GHz. The implemented four oscillator array operates at 1/4th of required LO tuning range and provides a power-efficient solution for scalable mm-wave phased array. A frequency multiplier increases the tuning range and provides 23-dB power gain to drive the bidirectional down/up

conversion mixers. The high-frequency limitations of LO-phase shifting based on injection locking are mitigated by using folded cascode injection mechanism. This technique improves the locking bandwidth of the array of ILO phase shifter. The folded-cascode scheme compensates the effect of parasitic capacitance at the injection node and improve the locking range. A minimum 3-dBm injection power is demonstrated to lock the 4 ILOs with 250-MHz locking bandwidth, $\pm 300^\circ$ phase shift range, and less than 1-dB amplitude mismatch. The cascode provides high isolation between each phase shifter element to improve the channel-to-channel coupling to under 0.5 dB. A 2x2 array is implemented with a bidirectional front-end to support transmit and receive operations through a common aperture in 90-nm SiGe BiCMOS. The low amplitude and phase noise variation supports 6-Gb/s, 256-QAM modulation for the implemented ILO system.

Chapter 4 presents a wideband, millimeter-wave image-selection architecture based on a Weaver architecture at E-band. The principle operation of the proposed architecture and its benefit on the QAM modulation signals are described analytically. The architecture can be applied to multiple input/output (MIMO) and phased-array systems. The circuit implementation of the two channel system is presented in this chapter with the detailed description of the bidirectional circuit blocks. The bidirectional TX and RX measurement performed and showed uniform performance over the two USB and LSB bands. Finally, it demonstrates QAM modulation for transmitter with low EVM ($< 5\%$) through a reduced 3 GHz LO-tuning range that mitigates gain variation and amplitude/phase imbalance.

Chapter 2

Injection-Locked Oscillator Phase Shifter, High-frequency Design and Trade-offs

2.1 Non-linear Dynamics of LC Injection-locked Oscillator (ILO)

An electronic LC oscillator is shown in Fig. 2.1 and consists of a resonant tank circuit consisting of a parallel inductor, L, and a capacitor, C that stores electrical energy. However, a portion of the energy is lost in the real resistance of the capacitor and the inductor dampening the oscillation. This resistance illustrated as R_P in Fig. 2.1 relates to the quality factor, Q, of the tank, which is defined by the ratio of oscillation frequency to bandwidth. The Q can also be defined as the ratio of the stored energy in the tank to the total energy loss per cycle [54]:

$$Q = 2\pi \times \frac{Energy\,stored}{Energy\,dissipated\,per\,cycle} \tag{2.1}$$

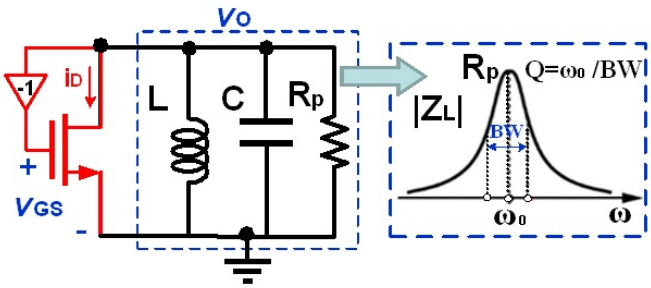


Figure 2.1: Single-ended model of LC oscillator schematic.

The parallel resistance, R_p, of an LC tank is related to Q as follows:

$$R_p = \frac{Q}{\omega_0 C} = \frac{\omega_0 L}{Q} \tag{2.2}$$

This loss must be compensated to sustain the oscillation. An active negative conductance g_m is introduced with a FET or bipolar transistor as shown in Fig. 2.1. The equivalent admittance of the LC oscillator shown in Fig. 2.1 can be written as

$$Y_L = (\frac{1}{j\omega_0 L} - j\omega_0 C) + \frac{1}{R_p} - g_M. \tag{2.3}$$

where Y_L is the equivalent output admittance of the feedback transistor. The oscillation occurs at f_0 when the imaginary part of Y_L is zero, i.e. the admittance of the capacitor and inductor cancel. Therefore, the oscillation frequency is equal to:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{2.4}$$

To start the oscillation, the negative conductance should be greater than $1/R_p$. The conductance of a FET transistor amplifier depends on its biasing condition, I_D, and V_{GS} as $g_m = 2I_D/(V_{GS} - V_{th})$. The FET transistor starts working in the linear small signal mode. In steady state, the transistor conducts current over a short period of time and has a square-wave shape. The LC tank filters out harmonics as found in the Fourier-series expansion:

$$i_{D-switching}(t) = \frac{4}{\pi}\sum_{k=1}^{\infty}\frac{sin\,(2\pi(2k-1)f_0)}{2k-1} = \frac{4}{\pi}\left[sin\,(2\pi f_0) + \frac{1}{3}sin\,(6\pi f_0)\right] \tag{2.5}$$

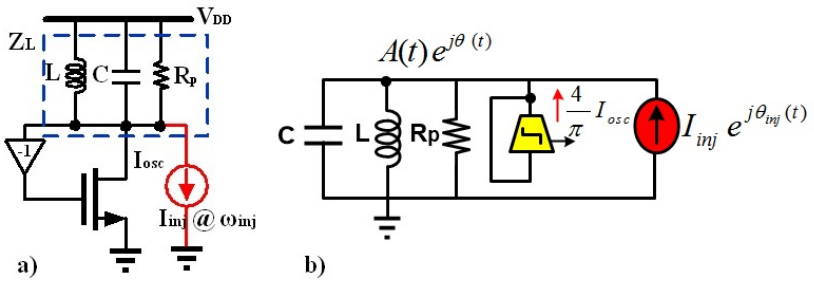


Figure 2.2: LC injection-locked oscillator: a) LC oscillator under unilateral injection, b) single-ended half-circuit equivalent model [55, 56].

The schematic of an LC oscillator under injection is shown in Fig. 2.2. The half-circuit equivalent model is illustrated in Fig. 2.2 b) including the lossy LC tank, the amplitude of the switching transistor output current, $4/\pi I_{osc}$, the amplitude I_{inj}, and phase θ_{inj} of the injection transistor. To solve the nonlinear dynamics of an LC ILO, Kirchoff's Current Law (KCL) is applied at the output voltage with a time-varying amplitude A(t), and phase of $\theta(t)$ as suggested in [55]:

$$\frac{1}{R_p} A\, e^{j\theta} + C\frac{d}{dt}\left(Ae^{j\theta}\right) + \frac{1}{L}\int^{t} Ae^{j\theta} d\tau = \frac{4\, I_{osc}}{\pi} e^{j\theta} + \frac{4\, I_{inj}}{\pi} e^{j\theta_{inj}} \tag{2.6}$$

Where $\theta_{inj} = \omega_{inj} t + \psi$. By multiplying both sides of (6) by exp(-jθ) we have

$$\frac{1}{R_p} A + C\,\frac{dA}{dt} + j\,C\,A\,\frac{d\theta}{dt} + \frac{1}{L}\, e^{-j\theta} \int^{t} A\, e^{j\theta} d\tau = \frac{4 I_{osc}}{\pi} + \frac{4 I_{inj}}{\pi} e^{j(\theta_{inj}-\theta)} \tag{2.7}$$

To solve this equation, we define two functions F_1 and F_2 as the real and imaginary parts of the integral.

$$\int^{t} A\, e^{j\theta} d\tau = F_1 + jF_2 \Rightarrow F_1 = \int^{t} A\, sin\theta,\; F_2 = \int^{t} A\, cos\theta \tag{2.8}$$

By replacing (2.8) in (2.7) to separate the real and imaginary part, the amplitude and phase dynamics are derived as (2.9) and (2.10) respectively.

$$\frac{1}{R_p} A + C\,\frac{dA}{dt} + \frac{1}{L}\, F_1\, cos\theta + \frac{1}{L}\, F_2\, sin\theta = \frac{4}{\pi} I_{osc} + \frac{4}{\pi} I_{inj} cos\left(\theta_{inj} - \theta\right) \tag{2.9}$$

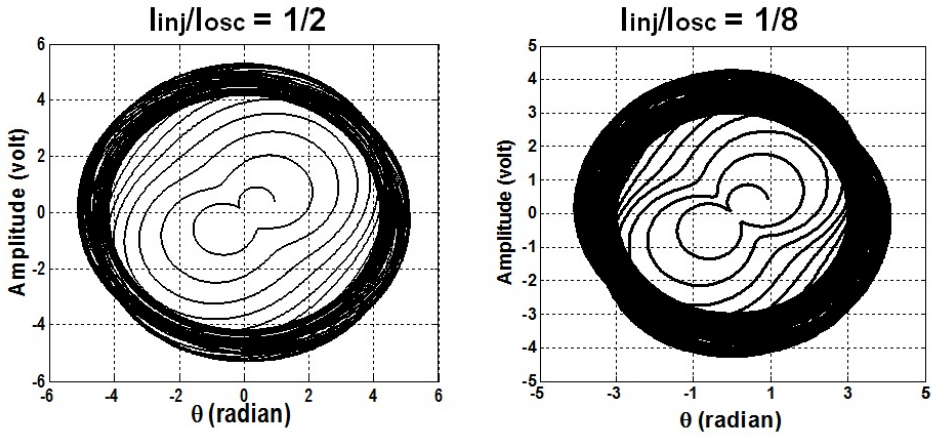


Figure 2.3: Injection-locked oscillator, ILO, amplitude/phase bifurcation diagram for two different I_{inj}/I_{osc} ratio 1/2 and 1/8.

$$C\,A\,\frac{d\theta}{dt} - \frac{1}{L}\,F_1\,sin\theta + \frac{1}{L}\,F_2\,cos\theta = \frac{4}{\pi} I_{inj} cos\,(\theta_{inj} - \theta) \tag{2.10}$$

Equations (2.8), (2.9) and (2.10) are solved in MATLAB using function of "ode15s" which is used to solve first-order derivative equations in the forms of $dy/dt = f(t, y)$. To find out the relation of amplitude, A, and phase, θ with the ILO parameters, the polar bifurcation diagram of A and θ based on the equations of (2.9) and (2.10) are plotted by changing various parameters.

2.1.1 Injection Current Ratio and Locking Range

One of the effective factors in ILO performance is the unilateral coupling ratio, I_{inj}/I_{osc}, which is the ratio of injection current to oscillation current. The A-θ polar bifurcation diagram for two values of 1/2 and 1/8 are illustrated in Fig. 2.3.

As the phase increases periodically over time, the amplitude converges to constant value if the ILO reaches a steady-state condition. Converging to steady-state point needs certain coupling ratio, for the injection ratio of 1/8 the amplitude cannot settle to a constant value in the A-θ bifurcation, however, increasing the ratio to 1/2 helps the system to converge to a constant amplitude as shown in Fig. 2.3. The time-responses of amplitude for various ratios of I_{inj}/I_{osc} are demonstrated in Fig. 2.4. For small coupling ratio, the ILO is not able to converge

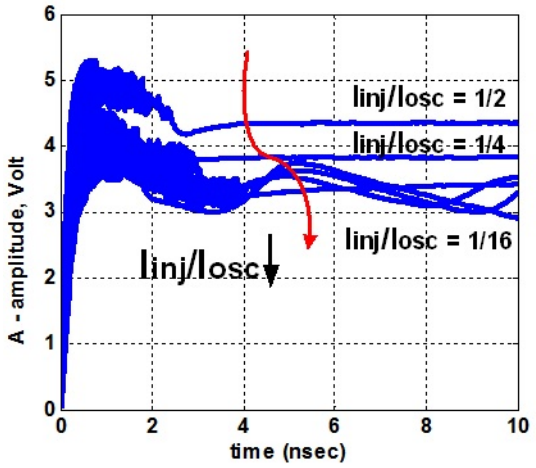


Figure 2.4: Time response of amplitude, A, for various unilateral coupling ratio,I_{inj}/I_{osc}, for $f_{inj} - f_0$=100 MHz and Q=5.

to constant amplitude and it exhibits amplitude fluctuation due to beat frequencies. In other words, for smaller I_{inj}/I_{osc}, the stability time-constant increases in addition to smaller amplitude voltage magnitude.

2.1.2 Quality Factor and locking range

The quality factor, Q, is another important parameter in characterizing ILO behavior. The A-θ polar bifurcation diagram for two values of Q (5 and 20), and for I_{inj}/I_{osc}=1/2 are shown in Fig. 2.5. A large value of Q prevents the ILO from locking and it does not converge to the steady-state constant amplitude. Larger Q implies small locking bandwidth, as shown in Fig.2.1. In other words, smaller Q is required to have larger locking range at the expense of phase noise degradation. The amplitude time response for different amounts of Q are plotted in Fig. 2.6, which shows smaller Q reaches steady state over shorter period.

2.1.3 Frequency Detuning and Phase shifting

When there is no injected current, $I_{inj} = 0$, the natural oscillation frequency is $\omega_0 = 1/\sqrt{LC}$. The oscillator's natural frequency can be varied across a tuning

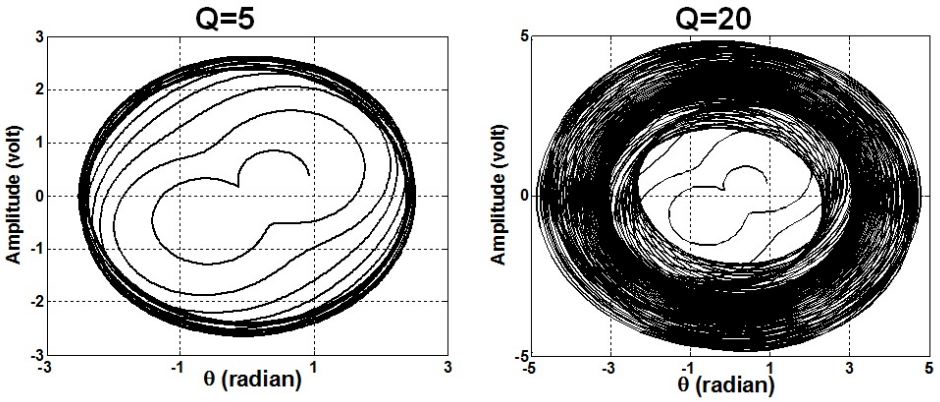


Figure 2.5: The amplitude/phase bifurcation diagram for two different Q of 5 and 20, $I_{inj}/I_{osc} = 1/2$, and $f_{inj} - f_0$=100 MHz.

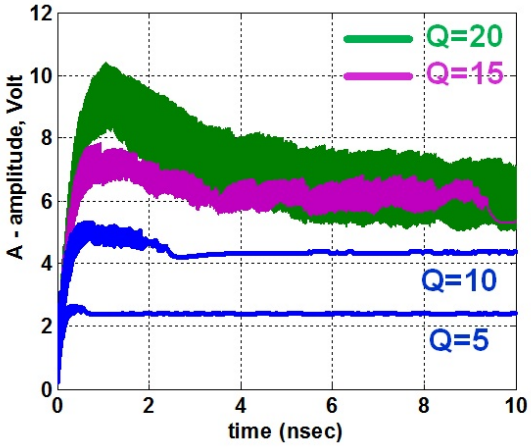


Figure 2.6: Time response of amplitude, A, for different values of quality factor, Q for $I_{inj}/I_{osc} = 1/2$ and $f_{inj} - f_0$=100 MHz.

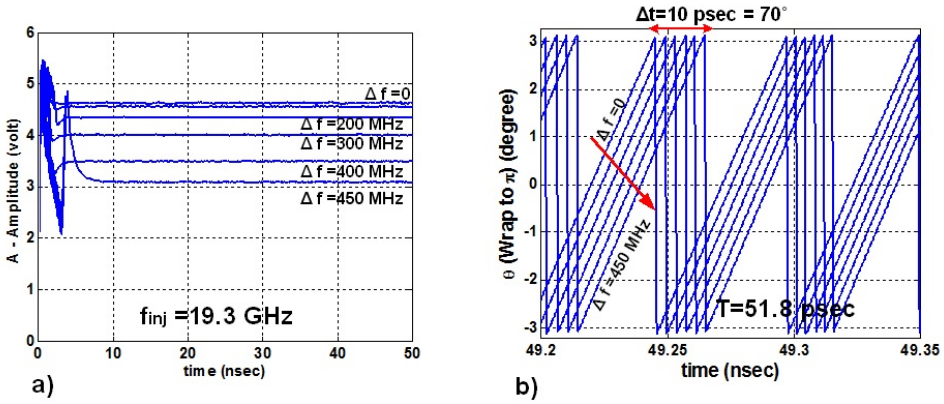


Figure 2.7: Time response of amplitude and phase of ILO under different frequency detuning, $f_{inj} - f_0$. (a) amplitude, A, (b) phase response warped to π.

range while free-running. When a current is injected into the tank of the LC oscillator at frequency, ω_{inj}, the LC oscillator frequency can be pulled to the same frequency as ω_{inj} even as the injected frequency differs from the natural frequency. The frequency detuning, $\Delta\omega$, is defined as the difference between the natural frequency and the injected frequency, $\omega_0 - \omega_{inj}$, and results in a phase shift of $\Delta\phi$ under locked conditions as illustrated in Fig. 2.7. Fig. 2.7 demonstrates the ILO amplitude and phase behavior under different injection signal frequencies and consequently frequency detuning, $f_{inj} - f_0$. As the injection signal frequency, f_{inj}, increases to the maximum locking bandwidth, ω_L, the stability time constant increases while the amplitude magnitude decreases. Therefore, detuning the locked oscillator introduces amplitude variation in the ILO output. A feature of the phase shifting produced by frequency detuning provides to the ILO output as shown in Fig.2.7 b).

For example, under an injection signal at 19.3 GHz (T= 51.8 psec), 450 MHz detuning frequency introduce 10 psec time delay which is equivalent to 70 degree phase shifting of the ILO output. For injection frequencies outside the locking bandwidth of ILO, the oscillator will remain unlocked. The A-θ polar bifurcation diagrams for two detuning frequencies are shown in Fig. 2.8 and show convergence to steady state does not happen when the frequency detuning exceeds the locking bandwidth.

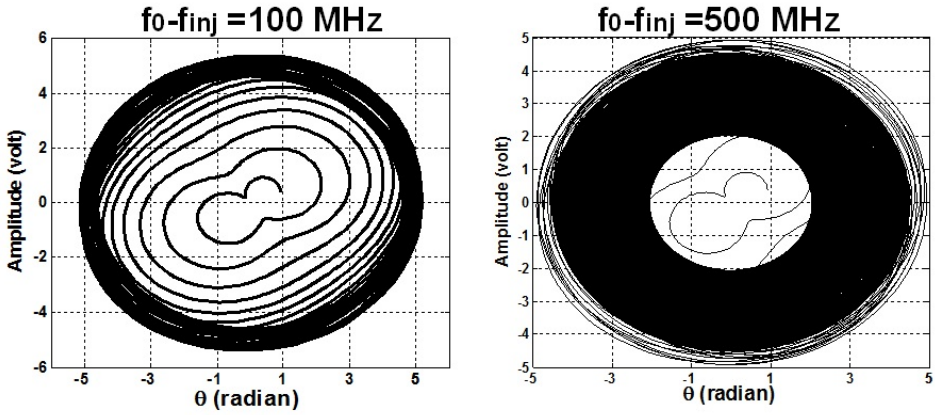


Figure 2.8: The amplitude/phase bifurcation diagram for two different $f_{inj} - f_0$, 100 MHz and 500 MHz (smaller and larger than locking bandwidth, (ω_L).

2.2 ILO phase shifter in Linear and Weak Injection Regime

2.2.1 Simplified Dynamic Model of ILO

To understand the ILO phase shifter performance, a simple model is desired to approximate the effects of circuit parameters based on equation 2.7. Reference [55] solves 2.7 by using an auxiliary function $F(t)$:

$$F(t) = e^{-j\theta} \int^{t} A\, e^{j\theta} d\tau \tag{2.11}$$

Differentiating both sides of (11) implies that:

$$\frac{dF}{dt} + j\frac{d\theta}{dt} = A(t) \tag{2.12}$$

Equation (2.12) is a first-order differential equation with a time-varying input amplifier $A(t)$, and output $F(t)$. The cut-off frequency of filter is a complex variable as $jd\theta/dt$. Under steady state, $A(t)$ is constant and $F(t)$ can be written as follows for small detuning frequency value [55]:

$$F \simeq \frac{A(t)}{j\frac{d\theta}{dt}} = \frac{A(t)}{j\left(\omega_0 + \left(\frac{d\theta}{dt} - \omega_0\right)\right)} \simeq -j\frac{A(t)}{\omega_0^2}\left(2\omega_0 - \frac{d\theta}{dt}\right) \tag{2.13}$$

Substituting (2.13) in (2.7) and separating real and imaginary parts, the simplified model for amplitude and phase are derived:

$$RC\,\frac{dA}{dt} + A = R(\frac{4}{\pi}I + I_{inj}cos\,(\theta_{inj} - \theta)) \tag{2.14}$$

$$\frac{d\theta}{dt} = \omega_0 + \frac{\omega_0}{2\,Q}\frac{I_{inj}\,sin\,(\theta_{inj} - \theta)}{\frac{4}{\pi}I + I_{inj}\,cos\,(\theta_{inj} - \theta)} \tag{2.15}$$

At the steady-state condition, $d\theta/dt = \omega_{inj}$ and $dA/dt = 0$, the relation between phase shift and frequency detuning, $\omega_{inj} - \omega_0$, and also the maximum locking bandwidth, ω_L, are derived.

$$\Delta\phi = sin^{-1}\left(\frac{2Q}{\omega_0}\,\frac{I_{osc}}{I_{inj}}\,(\omega_{inj} - \omega_0)\right) \tag{2.16}$$

$$\omega_L = \omega_{inj} - \omega_0 = \frac{\omega_0}{2\,Q}\,\frac{I_{inj}}{I_{osc}} \tag{2.17}$$

The phase shift range, $\Delta\phi$, the locking range, ω_L, are the important parameters defining the ILO phased shifter performance. As the simplified model presented in (2.14) - (2.17) equate, the phase shift depends on three parameters: the average quality factor of resonance tank, Q, the frequency detuning, $f_{inj} - f_0$, and the ratio of the injected current to the oscillator current, I_{inj}/I_{osc}. The simplified single-sideband locking bandwidth, ω_L, is related to the oscillator's parameters as stated in (2.17). The oscillator will lock to the injected frequency when the frequency detuning falls within the locking range, ω_L. Therefore, the tuning range for natural frequency of the oscillator should exceed the sum of desired RF band and the locking range. To increase the locking range, either the ratio I_{inj}/I_{osc} should increase or the Q of the tank should decrease based on (2.17). Decreasing the Q degrades the phase noise of the ILO.

Given these equations the amplitude, A, and phase shift, $\Delta\phi$, versus $\omega_{inj} - \omega_0$ are plotted in Fig. 2.9 a) and b) for different I_{inj}/I_{osc} ratios. As it was also predicted in Section 2.1, increasing I_{inj}/I_{osc} ratio increases the locking range bandwidth with smaller phase shift slope implying smaller phase dynamic range, as shown in Fig. 2.9 a). In addition, the amplitude variation for different I_{inj}/I_{osc},

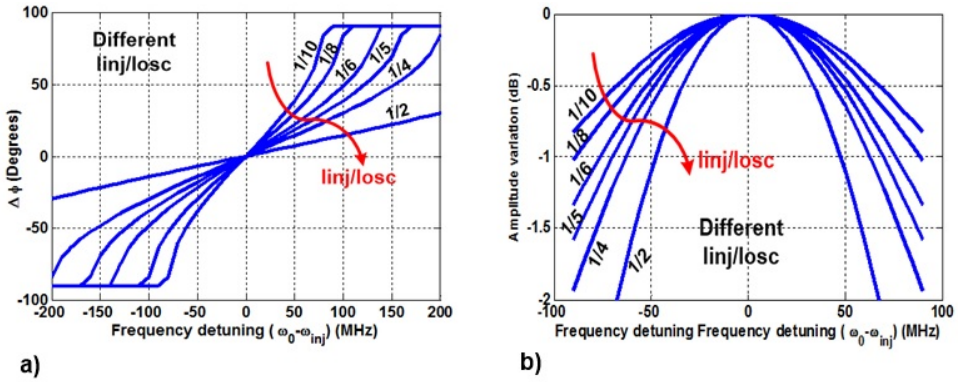


Figure 2.9: Simplified model of phase shift and amplitude variation of ILO versus of frequency detuning, $\omega_0 - \omega_{inj}$ for different I_{inj}/I_{osc} ratios.

shown in Fig. 2.9 b), demonstrates that smaller injection current results in smaller amplitude variation.

2.2.2 Definition for Linear Phase Shift

Ideally, the phase shift that results from the ILO phase shifter is linear with the frequency detuning. As shown in Fig. 2.9 a), the plot of $\Delta\phi$ versus $\Delta\omega$ is an arcsine function and saturates as the phase approaches $\pm 90°$. In these regimes, the frequency detuning does not change linearly as $\Delta\omega$ changes. This is undesirable from the standpoint of a phase shifter. A linear range of operation is found from expanding (2.16), through a Taylor series. Using (2.17), the phase shift is expressed as

$$\Delta\phi = \frac{\Delta\omega}{\omega_L} + \frac{1}{6}\left(\frac{\Delta\omega}{\omega_L}\right)^3 + ... \tag{2.18}$$

The linear region is defined as the phase variation as a function of $\Delta\omega$ with a constant slope of $1/\omega_L$. The linear phase shift range is found by bounding the third order term to a maximum deviation θ (in degrees) for the phase. Substituting this bound into (2.18), the linear range of frequency detuning is related to the locking range.

$$\Delta\omega \leq 0.5\,\omega_L \times \sqrt[3]{\theta} \tag{2.19}$$

In other words, a phase deviation of 1 degree results bounds the desired frequency

Table 2.1: Linear range performance of an ILO phase shifter and resulting phase shift range

Phase Deviation,θ (degree)	Normalized Frequency Detuning $\Delta\omega/\omega_L$	Linear Phase Shift Range $\Delta\phi$ (degree)
0.5°	40%	± 24°
1°	50%	± 30°
2.5°	67.8%	± 42.7°
5°	73%	± 46.9°

detuning to 50% of the locking range. Substituting this limit into the phase shift from (2.16), the maximum phase shift is ±30 degrees. Table 2.1 summarizes the trade-off between linear locking range and phase shift range for the ILO phase shifter. Note that the phase deviation of 5° must be calculated with higher order terms. Table 2.1 also suggests the linear locking range required to achieve the desired phase deviation. Typically, the locking range is around 10% of the nominal oscillator frequency for a tank with Q of 10 and I_{inj}/I_{osc} equal to 0.5. Therefore, the linear frequency detuning to generate a 30° phase shift may be only around 5% of the oscillation frequency. To increase the linear phase shift range, a frequency multiplier is required. For example, multiplying the frequency by 4 increases the linear phase shift of ±46.9° to more than ± 180° if a phase deviation of 5° is tolerated. If a smaller phase deviation is required, more frequency multiplication must be introduced.

The desired ILO phase shifter performance in a phased array should provide a phase shift range that covers 360° (+/-180°). In addition to linear phase shift, minimum amplitude variation is desirable across the frequency detuning since amplitude mismatch and variations affect the conversion gain and degrade the peak-to-null ratio of array pattern. Additionally, the ILO should offer phase and amplitude independence between each phase shifter. Phase and amplitude independence between phase shifters of each element is also desired to have more isolation between them and minimize phase and amplitude errors.

2.3 Device Parasitic Effecs on ILO

Achieving the ILO locking range and tuning range at microwave and millimeter-wave bands is challenging due to resistive and capacitive parasitic impedance at the injection node. As (2.16) and (2.17) predicts, increasing I_{inj}/I_{osc} increases the locking range and provides finer phase resolution with larger amplitude variation. However, the increased injection current also suggests the need for larger transistors to provide this current, adding more parasitic capacitance to the oscillator tank, and therefore, reducing the effective locking range by absorbing fraction of injection current and tuning range of natural frequencies. Therefore, I_{inj}/I_{osc} needs to increase to have finer phase resolution resulting in wider injection transistors W_{inj} and adding more parasitics. This suggests the need to carefully balance the desired tuning range and locking range of the injection-locked oscillator phase shifter.

A differential LC oscillator is designed and simulated in Cadence, and the simulation results are compared with amplitude and phase equations of (2.14) and (2.15). Fig. 2.10 illustrates mismatch exists between the simulations and the simplified model. The mismatch occurs from neglecting parasitic capacitance and inductance in the dynamic models. These parasitics have significant effects at high-frequency applications, when the parasitic capacitance of devices to the substrate creates an additional coupling path between the oscillator output and the injection port but also between neighboring oscillators.

These parasitics to the substrate arise from the ILO injection circuit and contribute three parasitic components: C_p, C_{gd} and r_o as depicted in Fig. 2.11. The gate-to-drain capacitance, C_{gd}, creates a path between input and output of each ILO that reduces the isolation between each ILO phase shifter and is a source of LO pulling. Furthermore, the output parasitic capacitance, C_p, which captures the injection transistors C_{db} and C_{ds} reduces the oscillation natural frequency, ω_0, as

$$\frac{df}{f_0} = \frac{-1}{2}\frac{dC}{C_0} = \frac{-1}{2}\frac{C_p}{C_0}. \tag{2.20}$$

In addition, C_p in parallel with output resistance r_o absorbs some fraction of the

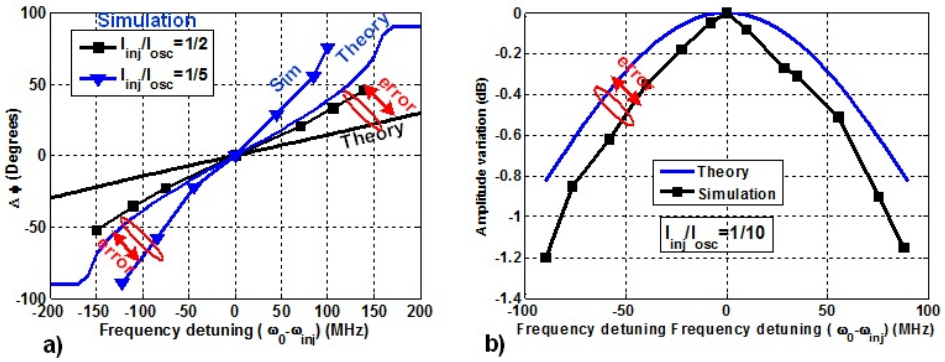


Figure 2.10: Circuit simulation and simplified model comparison, a) phase shift, b) amplitude variation versus frequency detuning.

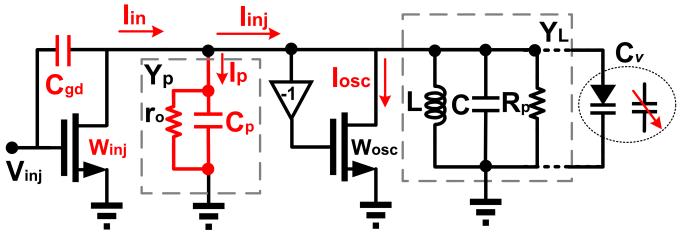


Figure 2.11: ILO injection circuit including parasitics.

desired injection signal, reducing the locking bandwidth of the ILO as predicted by 2.17.

To calculate the effect of the parasitics on the locking range, the parasitic current needs to be calculated and added to (2.17). Equation (2.17) is a simplified response of the first-order differential equation under weak injection condition and presented in [55] but does not consider the high-frequency parasitic device model. To modify the equation, , the ac current can be approximated as $\frac{4}{\pi} I_{DC} sin(\omega_{inj} t)$ for a linear ILO under weak injection. Therefore, the injected current, I_{inj} and dissipated current, I_p, are related to the parasitic and tank admittance.

$$\frac{I_p}{I_{inj}} = \frac{Y_p}{Y_L} = \frac{sC_p + \frac{1}{r_o}}{sC + \frac{1}{SL} + \frac{1}{R_p}} \tag{2.21}$$

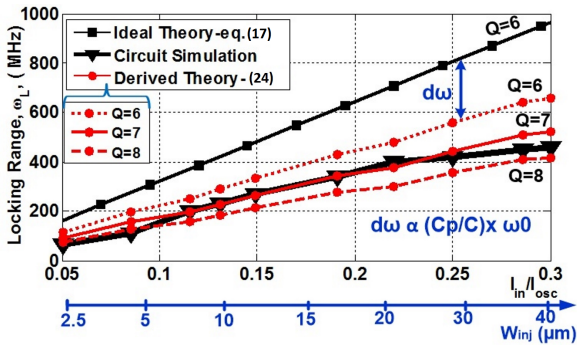


Figure 2.12: Comparison between the theoretical expressions and circuit simulation results (schematic-view) of locking-range, ω_L, as injection transistor width, W_{inj}, C_p/C and I_{inj}/I_{osc} increase at 19.3 GHz with $W_{osc} = 100\,\mu m$.

By replacing $s = j\omega_{inj}$, where $\omega_{inj} = \omega_0 + \Delta\omega$ and substituting this into (2.21), the expression can be simplified to

$$\left|\frac{I_p}{I_{inj}}\right| = \left|\frac{j(\omega_0+\Delta\omega)C_p + \frac{1}{r_o}}{-j\frac{2\,\Delta\omega}{L\,\omega_0^2} + \frac{1}{R_p}}\right|. \tag{2.22}$$

When $\Delta\omega >> 0$ and R_p and r_o are large and their contributions to (2.22) are negligible near the edge of the locking range, the equation simplifies to

$$\left|\frac{I_p}{I_{inj}}\right| = \alpha = \frac{1}{2}\frac{C_p}{C}\left(1+\frac{\omega_0}{\Delta\omega}\right) \simeq \frac{1}{2}\frac{C_p}{C}\frac{\omega_0}{\Delta\omega}. \tag{2.23}$$

This equation predicts that the effect of C_p/C ratio is related to $\omega_0/\Delta\omega$. If $I_{inj} = \frac{1}{1+\alpha}I_{in}$ where α is found from (2.23), the ω_L relation to C_p is

$$\omega_L = \frac{\omega_0}{2Q}\frac{I_{in}}{I_{osc}} - \frac{1}{2}\frac{C_p}{C}\omega_0. \tag{2.24}$$

Equation (2.24) shows the relation between the C_p/C and I_{in}/I_{osc} to ω_L. As the width of the injection transistor W_{inj} increases, g_m, the I_{inj}/I_{osc} ratio, and C_p/C will increase. When W_{inj} is small, I_{inj}/I_{osc} dominates and (2.24) reduces to the ideal expression in (2.17). When W_{inj} is large, C_p/C becomes significant and deviation is predicted compared to (2.17). An n-MOS oscillator with a common-source injection transistor and n-MOS varactor for frequency tuning, shown in Fig. 2.11, is simulated and compared with (2.24) and (2.17). The results are plotted in

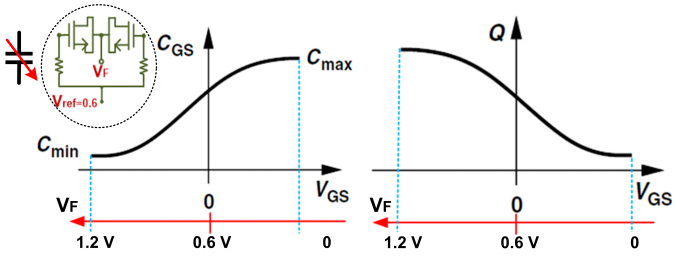


Figure 2.13: Nonlinear variation of the quality factor, Q, of the frequency detuning component, n_MOS varactor, as analog voltage and correspondent capacitance vary [57].

Fig. 2.12. In the simulation, the dc ratio of injection current, I_{inj}/I_{osc}, is constant and set to 0.1 for the weak injection assumption. As W_{inj} increases from $2.5\mu m$ to $40\mu m$, I_{inj}/I_{osc} increases. The C_p/C and I_{inj}/I_{osc} are captured separately and inserted into (2.24). The free-running frequency changes as W_{inj} varies and C_p/C was re-calculated using (2.20). The Q of the simulated ILO tank is dominated by the varactor Q, which is around 6. However, the varactor Q varies with the control voltage and, therefore, the capacitance varies as illustrated in Fig. 2.13.

The results plotted in Fig. 2.12 for three different Q values which demonstrate good agreement between the locking range from (2.24) and circuit level simulations that capture C_p/C effects and also predict the equivalent Q of ILO to fit the simulation ($Q = 7$). Moreover, the difference between the derived theory, (2.24), and original expression in (2.17) for the same value of Q is equivalent to $0.5(C_p/C) \times \omega_0$, illustrating that the locking range of ILO is bounded by the parasitic capacitance and will saturate as C_p/C becomes large.

2.4 Substrate Parasitic Coupling Effect on Array of ILOs

Implementing an array of ILOs on a silicon substrate create an unwanted coupling path between them due to the high-frequency conductivity and dielectricity characteristic of Si-substrate. To revise the ILO amplitude-phase $(A - \theta)$

model to include substrate parasitic coupling from intrinsic transistor to substrate and between adjacent transistors, the parasitic coupling path needs to be modeled. Advanced CMOS and SiGe technology shrinks the device transistor implementing on a Si substrate, which increases the device parasitic effects to the substrate. Therefore, modeling substrate coupling to account for conductive and dielectric material is important. Prior work [58, 59] discusses a substrate coupling model as a geometry scalable network of circuit elements. For instance, Fig. 2.14 shows an equivalent circuit model presented in [59]. Each device has a junction capacitance to the substrate,C_j, depending on the device size and geometry. The resistive coupling part of the substrate modeled by R_{sub} represents its conductivity and it depends on the doping level of the substrate. A high resistivity substrate is commonly used for high-frequency applications; therefore, the dielectric behavior of the substrate with its associated material cut-off frequency, C_{sub}, must be considered. The substrate resistance is modeled as distributed resistors depending on the different geometry distance path between each device, for instance, the resistance from the device active region to its isolation box and the resistance between device 1 isolation box to device 2 isolation box in Fig. 2.14. For distant devices, the latter part has a more significant effect which can be approximated as

$$R_{sub} = \rho_{sub}\frac{D_i}{W_B L_B} \tag{2.25}$$

where ρ_{sub} is the substrate resistivity, D_i is the distance between each device, and L_B and W_B are the length and the width of the isolation box surrounding each device. The associated capacitance of the bulk substrate, C_{sub}, which is shunted to the substrate resistance, is approximated as

$$C_{sub} = \frac{\rho_{sub}\varepsilon_{si}}{R_{sub}} \tag{2.26}$$

where ε_{si} is the Si-substrate permittivity. Equations 2.25 and 2.26 show that the substrate has a time constant associated with $R_{sub}C_{sub}$ equivalent to the substrate bulk material properties, $\rho_{sub}\varepsilon_{si}$, and corresponding to the cut-off

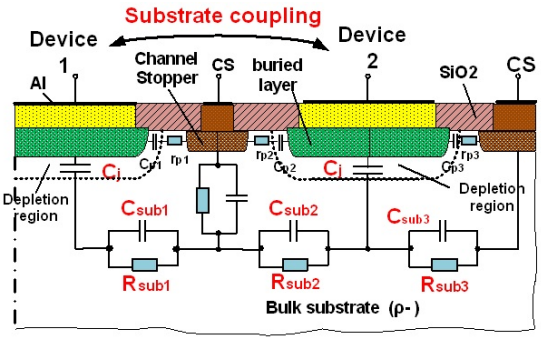


Figure 2.14: An equivalent circuit for modeling substrate coupling proposed in [59].

frequency.

$$f_{sub} = \frac{1}{2\pi R_{sub} C_{sub}} = \frac{1}{2\pi \rho_{sub} \varepsilon_{si}} \simeq 10\,GHz \tag{2.27}$$

Eq. (2.27) explains that for frequencies around 10 GHz and higher than that the substrate can not be accurately modeled only by its conductivity feature, therefore, the dielectric capacitance must be considered. To take into account the parasitic coupling effect in the ILO phase shifter performance, the parasitic coupling current needs to be characterized. Fig. 2.15 illustrates the equivalent model for parasitic coupling path between two neighboring oscillators. The unilateral injection current, I_{inj}, is the desired coupling current that characterizes the ILO behavior as described in sections (2.1) and (2.2). However, the bi-directional parasitic current, I_p, is an undesired coupling path that leads to deviation of the ILO performance from its ideal behavior, thereby introducing phase and amplitude errors to the output.

To calculate these amplitude and phase errors, the amount of parasitic injection current, I_p, needs to be evaluated first. As shown in Fig. 2.15 b), I_p is equal to the current passing through C_j as

$$i_p = C_j \frac{d\,(V_x - V_1)}{dt} = -C_j \frac{d\,(V_y - V_2)}{dt} \tag{2.28}$$

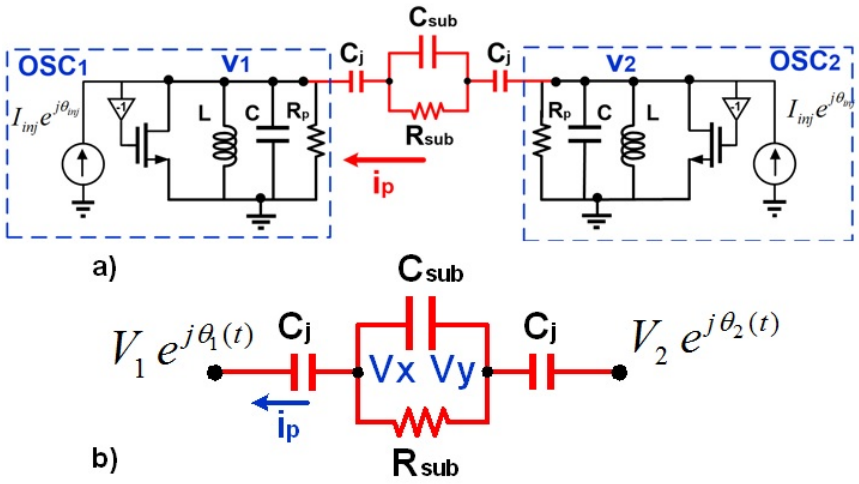


Figure 2.15: An equivalent circuit diagram for substrate parasitic coupling between two neighboring ILOs.

where two ILOs are represented by their associated amplitude, V_i, and phase, θ_i as $V_1 = |V_1|exp(j\theta_1)$ and $V_2 = |V_2|exp(j\theta_2)$. V_x and V_y are calculated by writing KCL at the two interface nodes as:

$$C_j \frac{d\,(V_x - V_1)}{dt} + C_{sub} \frac{d\,(V_x - V_y)}{dt} + \frac{V_x - V_y}{R_{sub}} = 0 \tag{2.29}$$

$$C_j \frac{d\,(V_y - V_2)}{dt} + C_{sub} \frac{d\,(V_y - V_x)}{dt} + \frac{V_y - V_x}{R_{sub}} = 0 \tag{2.30}$$

Adding (2.29) and (2.30), and subtracting (2.30) from (2.29) result in:

$$V_x + V_y = V_1 + V_2 = const. \tag{2.31}$$

$$\frac{d\,(V_x - V_y)}{dt} + \frac{2}{R_{sub}(C_j + 2C_{sub})}(V_x - V_y) = \frac{C_j}{C_j + 2C_{sub}} \frac{d\,(V_1 - V_2)}{dt} \tag{2.32}$$

Equation (2.32) shows that the phase difference, $\theta_1 - \theta_2$, between two ILOs is an important parameter. If $\theta_1 - \theta_2$ is equal to zero, the circuit model shown in Fig. 2.15 b) can be modeled as an even-mode equivalent circuit, meaning that $I_p = 0$. On the other hand, for $\theta_1 - \theta_2$ equal to 180°, the circuit can be modeled as an odd-mode equivalent half circuit loaded by parasitic C_j, $2C_{sub}$ and $R_{sub}/2$ in each side. This odd mode can be another representative model of the single transistor

parasitic coupling path to the substrate, where the C_p from Fig. 2.11 can be approximated as $(C_j||2C_{sub})$. Equation (2.32) is a first-order differential equation with coefficients of ρ_1 and ρ_2:

$$\frac{d\,(V_x - V_y)}{dt} + \rho_1\,(V_x - V_y) = \rho_2 \frac{d\,(V_1 - V_2)}{dt} \tag{2.33}$$

where $\rho_1 = 2/R_{sub}(C_j + 2C_{sub})$ and $\rho_2 = C_j/(C_j + 2C_{sub})$. Equation 2.33 can be solved using the following well-known solution for the first order differential equation:

$$\frac{d\,y}{dt} + p(t)\,y = q(t) \xrightarrow{sln} y(t) = \frac{1}{u(t)} \left(\int u(t)\,q(t) + c \right), \; where\, u(t) = e^{\int p(t)\,dt} \tag{2.34}$$

Using (2.34) to solve (2.33) and consequently (2.32) b), we can represent V_x and V_y in terms of V_1 and V_2 as follows:

$$V_x = \frac{1}{2}\left(1 + \rho_2 \frac{j\omega_{inj}}{j\omega_{inj} + \rho_1}\right) V_1 + \frac{1}{2}\left(1 - \rho_2 \frac{j\omega_{inj}}{j\omega_{inj} + \rho_1}\right) V_2 \tag{2.35}$$

$$V_y = \frac{1}{2}\left(1 - \rho_2 \frac{j\omega_{inj}}{j\omega_{inj} + \rho_2}\right) V_1 + \frac{1}{2}\left(1 + \rho_2 \frac{j\omega_{inj}}{j\omega_{inj} + \rho_1}\right) V_2 \tag{2.36}$$

Therefore, i_p is derived as

$$i_p = C_j \frac{d\,(V_x - V_1)}{dt} = \frac{1}{2} C_j \left(1 - \rho_2 \frac{j\omega_{inj}}{j\omega_{inj} + \rho_1}\right) \frac{d\,(V_1 - V_2)}{dt} \tag{2.37}$$

in terms of the difference between V_1 and V_2 and has the coefficient $0.5C_j\,(1 - \rho_2(j\omega_{inj}/j\omega_{inj} + \rho_1))$ which contains all the required parameters for modeling the substrate parasitic, C_j, ρ_1, and ρ_2 and also the frequency dependence, ω_{inj}. This coefficient can be also separated into the real and imaginary parts as $\rho_3 - j\rho_4$ where ρ_3 and ρ_4 are given as

$$\rho_4 = \frac{C_j^2}{4C_{sub}} \frac{\omega_{sub}\omega_{inj}}{\omega_{inj}^2 + \omega_{sub}^2} \tag{2.38}$$

$$\rho_3 = \frac{1}{2}C_j - \frac{C_j^2}{4C_{sub}} \frac{\omega_{inj}^2}{\omega_{inj}^2 + \omega_{sub}^2} = \frac{1}{2}C_j - \rho_4 \frac{\omega_{inj}}{\omega_{sub}} \tag{2.39}$$

where ρ_1 and ρ_2 are as follows:

$$\rho_1 = \frac{2}{R_{sub}\left(C_j + 2C_{sub}\right)} \simeq \frac{1}{R_{sub}C_{sub}} = \omega_{sub} \tag{2.40}$$

$$\rho_2 = \frac{C_j}{C_j + 2C_{sub}} \simeq \frac{C_j}{2C_{sub}},\ (C_j \ll C_{sub}) \tag{2.41}$$

Now, the derived parasitic current, i_p, needs to be added to the KCL written at the output of ILO in (2.7). By rearranging the revised KCL and using the techniques explained in Section 2.2 that derived equations (2.11)-(2.13), the revised KCL is as follows:

$$\begin{aligned} &A + R_pC\,\frac{dA}{dt} + j\,R_pC\,A\,\frac{d\theta}{dt} - 2jQ \times A + j\,\frac{Q\,A}{\omega_0}\frac{d\theta}{dt} \\ &= R_p\frac{4I}{\pi} + R_p\frac{4I_{inj}}{\pi}e^{j(\theta_{inj}-\theta)} - (\rho_3 - j\rho_4)\frac{d}{dt}\left(A_1e^{j\theta_1} - A_2e^{j\theta_2}\right) \end{aligned} \tag{2.42}$$

By separating the real and imaginary parts of (2.42) and setting the steady-state condition, $d\theta/dt = \omega_{inj}$ and $dA/dt = 0$, the amplitude and phase dynamics are derived as follows:

$$\begin{aligned} A\ &= \frac{R_p}{1 + R_p\rho_4\omega_{inj}}\left(4/\pi\left(I_{osc-1} + I_{inj-1}\,cos(\theta_{inj} - \theta)\right)\right. \\ &\left. + A_2\omega_{inj}\left(\rho_4\,cos(\theta_2 - \theta_1) - \rho_3\,sin(\theta_2 - \theta_1)\right)\right. \end{aligned} \tag{2.43}$$

$$\begin{aligned} &\Delta\phi = (\theta_{inj} - \theta) \\ &= sin^{-1}\left(\frac{1}{R_p\,I_{inj1}}\left(\left(\left(\left(1 + \frac{\rho_3}{2C}\right)\omega_{inj} - \omega_0\right)\frac{2Q\,A_1}{\omega_0}\right)\right.\right. \\ &\left.\left. - \left(\left(\rho_3\,cos(\theta_2 - \theta_1) - \rho_4\,sin(\theta_2 - \theta_1)\right) \times A_2R_p\,\omega_{inj}\right)\right. \end{aligned} \tag{2.44}$$

The revised amplitude dynamic(2.43) contains a decaying term $(R_p/(1 + R_p\rho_4\omega_{inj}))$ which causes amplitude degradation, and an error term caused by adjacent ILO amplitude and phase changes, θ_2, A_2. The amplitude error is plotted in Fig. 2.16 for different C_j/C_{sub} ratios versus relative phase of the two adjacent ILOs. The unilateral injection of ILO_1, I_{inj1}, is set to zero in order to only capture the in-

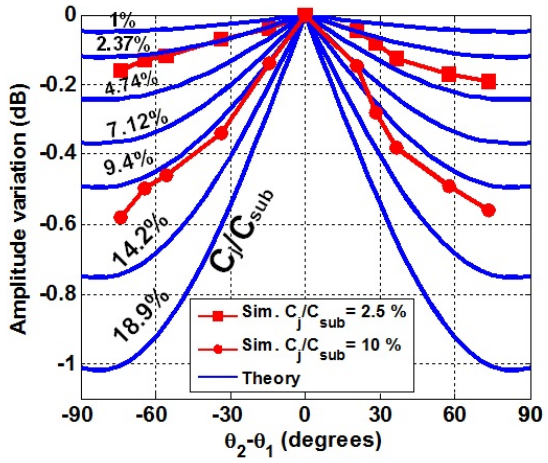


Figure 2.16: Amplitude variation of ILO number 1 for various C_j/C_{sub} ratios as the relative phase of two neighboring ILOs varies.

jection parasitic current effects and its corresponding amplitude error. The C_j is the junction parasitic capacitor that depends on the size of the transistors. In Fig. 2.16, it is varied from *1 fF* to *20 fF* with assuming $R_{sub} = 1\,k\Omega$ and Q of 5. To verify (2.43) and (2.44) with simulation, the two differential ILOs were simulated in Cadence while their parasitic coupling path is modeled as shown in Fig. 2.15 b), with series C_j, and shunt R_{sub}, C_{sub}. The circuit simulation results for two values 2.5% and 10% for C_j/C_{sub} are also plotted in Fig. 2.16, which almost matches the derived dynamic and parasitic coupling model and the circuit simulations. Another observation is that the larger transistor has more parasitic to substrate coupling and therefore, larger C_j/C_{sub} ratio, causing larger amplitude error in the ILO output.

Fig. 2.17 shows the amplitude error caused by different substrate resistivity as a function of phase changes for adjacent ILOs under the assumption that $C_j = 20\,fF$. As observed in Fig. 2.17, higher resistivity substrate or further distance between two neighboring ILOs is desired in order to have smaller amplitude deviation. The revised phase dynamics are expressed in (2.44) has the frequency bandwidth decaying term proportional to $1/R_pI_{inj1}(1 + \rho_3/2C)$. Also, the phase error term depends on the second ILO amplitude and their relative phase, $\theta_1 - \theta_2$. As it is illustrated in Fig. 2.18 a), smaller ratios of C_j/C_{sub} and higher resistiv-

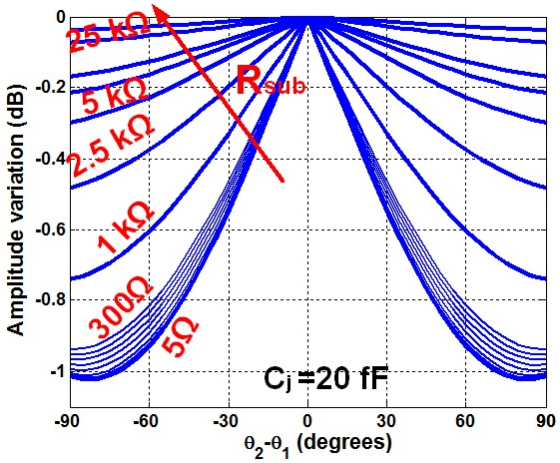


Figure 2.17: Amplitude variation of ILO number 1 for various R_{sub}values as the relative phase of two neighboring ILOs varies.

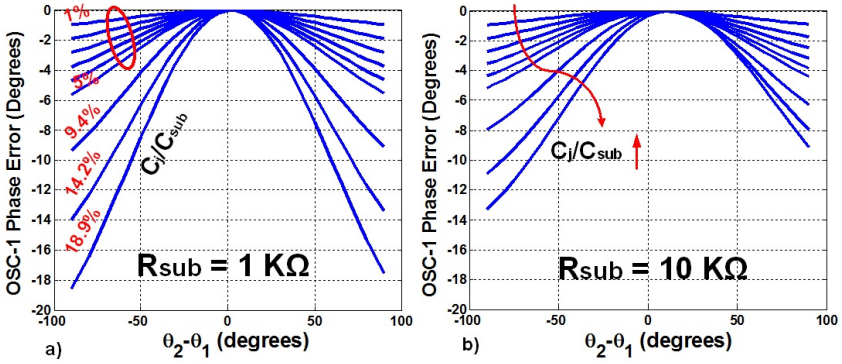


Figure 2.18: Phase error of ILO number 1 for various C_j/C_{sub} ratios as the relative phase of two neighboring ILOs varies: a) $R_{sub} = 1\,k\Omega$, b) $R_{sub} = 10\,k\Omega$.

ity substrates result in smaller phase error due to the substrate parasitic coupling path.

To characterize the parasitic effect on the ILO with respect to device geometry, one may assume the two ILOs are relatively far from each other. In other words, the amplitude of the second ILO, A_2 is zero. Therefore, the phase shift of ILO due to the device parasitic is

$$\Delta\phi = sin^{-1}\left(\frac{\left(\left(1+\frac{\rho_3}{2C}\right)\omega_{inj}-\omega_0\right)\frac{2Q\,A_1}{\omega_0}}{R_p\,I_{inj1}}\right) \tag{2.45}$$

where $A_1 = R_p I_{osc}$. This equation is a revision of equation (2.16) to include the capacitance parasitic of the original ILO, with a term proportional to $(1+(\rho_3/2C))$ that impacts the locking bandwidth. Note that under ideal assumption where the parasitic capacitance path is neglected, replacing $\rho_3 = 0$ as $C_j = 0$ in (2.45) will result in (2.16) where any parasitic effects ignored.

The circuit simulation result of the phase shift versus frequency detuning relation, $(\Delta\varphi vs(\omega_{inj}-\omega_0))$, for a single ILO with $I_{inj}/I_{osc} = 1/5$ is plotted in Fig. 2.19. The modified phase shift equation for single ILO, 2.45, is also plotted in Fig. 2.19 while the ratio of the parasitic capacitance, C_j, to the tank capacitance, C, is changed until it fits the circuit simulation results. The revised model in (2.45) can be used to estimate the parasitic capacitance of the implemented ILO by finding out for what value of C_j/C_{sub} , the derived equation and circuit simulation results match.

2.5 Proposed Folded-Cascode ILO

As it was explained in the previous sections, the ILO phase shifter is influenced by the circuit parasitics and introduces phase error, amplitude error, and lower locking bandwidth. Therefore, lower parasitic sensitive circuit and technique are required for implementing ILO on silicon technology. To inject current into the tank of the oscillator, common source or cascode amplifiers are commonly used.

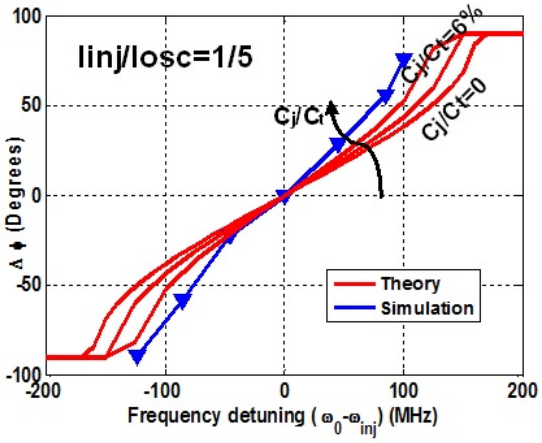


Figure 2.19: Phase shift versus frequency detuning of single ILO, both circuit simulation results and modified dynamic equation, (2.45) comparison.

common-source transistor, Fig. 2.20(a), converts the gate voltage into drain current, which can be coupled into the oscillator tank. A cascode amplifier, shown in Fig. 2.20(b), improves upon the common-source transistor to reduce the C_{gd} parasitic capacitance dependence by adding a common-gate transistor to provide better isolation. Additionally, it offers higher output resistance, $g_m r_o^2$, to the injection node. However, the size, i.e. width, of common-source and common-gate transistors are not independent parameters since both transistors are typically n-MOS or p-MOS devices that are biased with the same dc current. Increasing the common-gate transistor width adds more capacitance C_p to the ILO output and the trades-off of C_p/C and g_m remains. The size of the common-gate transistor also impacts the headroom of the common-source transistor. In steady state, large swing across the oscillator tank and injection transistors forces the transistors into triode mode. Larger common-gate transistors limit the common source transistor swing headroom and, therefore, reduce its injection transconductance, g_m.

A folded cascode solution is proposed here to overcome the headroom and isolation challenges. In the folded cascode structure, the n-MOS common-source transistor produces a dc and ac current. While the dc current is supplied by bias transistors, the ac current flows into a p-MOS common-gate transistor as shown

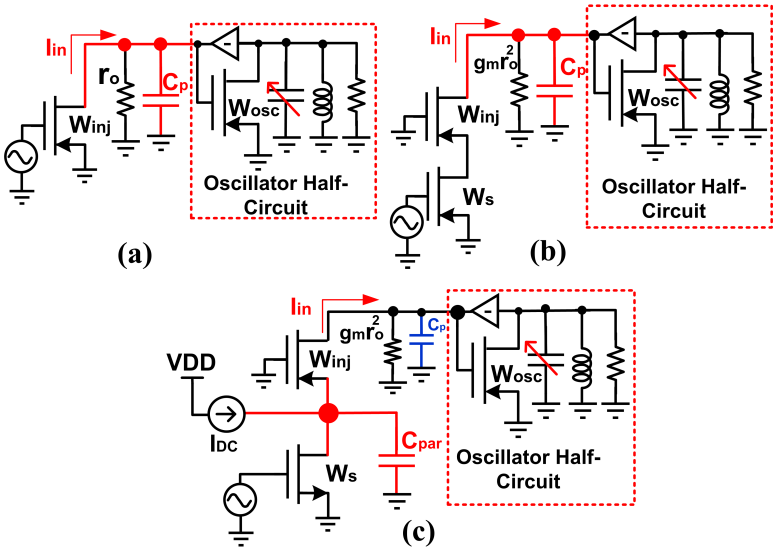


Figure 2.20: Different possible injection circuit schemes: a) common source, b) cascode, and c) folded-cascode.

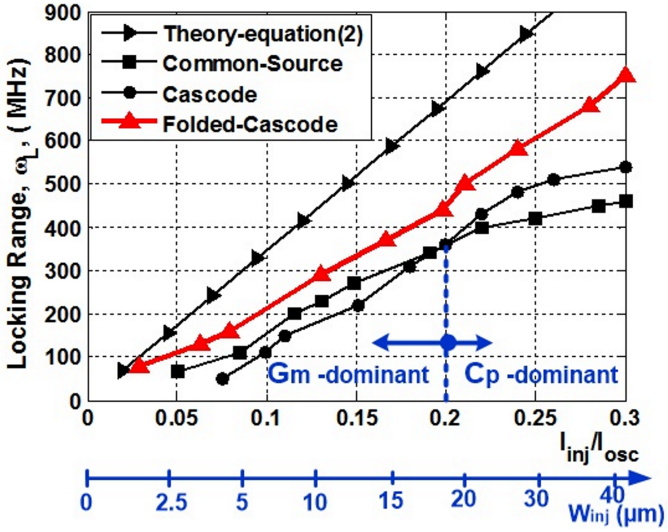


Figure 2.21: Simulation and comparison results for ILO with different injection scheme for various W_{inj}, and I_{inj}/I_{osc} with $W_{osc} = 100\ \mu m$ at 19.3 GHz.

in Fig. 2.20(c) assuming the ILO tank as an equivalent load of a typical amplifier. This modification shifts the parasitic capacitance from the injection node to the folded node and relaxes the swing headroom issues as a separate dc current source is used to bias the common-gate transistor. The folded cascode allows separate dc biasing of common-gate and common-source transistors, giving the circuit design more latitude to choose the cascode transistor width. The width of the common-gate transistor, W_{inj}, is reduced to lower the C_p/C ratio while the width of the common-source transistor, W_s, is independently chosen to increase the g_m and I_{inj}/I_{osc}. In other words, the folded cascode has the advantage of larger output impedance, $g_m r_o^2$, and better isolation, but also relaxes the g_m- C_p/C trade-offs described in the previous section.

Transistor-level simulations of three different circuit schemes are plotted in Fig. 2.21 for different W_{inj} and, therefore, I_{inj}/I_{osc}. The current ratio I_{inj}/I_{osc} is set as small as 0.1, and only W_{inj} changes to verify the effect on g_m- C_p/C trade-offs. The results in Fig. (2.21) indicate that the common-source and cascode schemes saturate as W_{inj} increases due to the C_p reduction, while the folded cascode reduces the C_p/C by controlling the folded transistor size, W_s, and provides extra g_m as the folded transistor size is 2 to 4 times larger than W_{inj}. The circuit simulations verify that the folded-cascode, injection-locking circuit more closely follows ideal theory with an improved locking range given a dc current.

Acknowledgment

This chapter is mostly a reprint of the material as it appears in [60, 62], N. Ebrahimi and J. F. Buckwalter, "Robustness of Injection-locked Oscillators to CMOS Process Tolerance " International Conference in Theory and Application in Nonlinear Dynamics (ICAND), Springer, Publication, 2016 and N. Ebrahimi, P. Wu, m. Bagheri and J. F. Buckwalter, "An E-band, Scalable 2x2 Phased-Array Transceiver Using High Isolation Injection Locked Oscillators in 90nm SiGe BiCMOS", IEEE RFIC Conference, 2016. The dissertation author was the primary investigator and author of these papers.

Chapter 3

Scalable High Data-rate Phased Array using Wideband Injection-locked Oscillator Phase Shifter

3.1 Scalable LO-shifting Transceiver Array Architecture

The conceptual block diagram of the scalable LO phase-shifting array is shown in Fig. 3.1(a) where multiple die are aggregated through LO distribution and IF combining or splitting. One significant advantage of LO phase shifting is that the phase shift can be implemented at low-frequency and distributed across the chip and then multiplied at each transceiver element. The advantages of low-frequency LO distribution are that, first, the LO tuning range is also multiplied and provides coverage over a wideband (but not larger from the standpoint of a fractional bandwidth) and, second, a low-frequency LO signal avoids pulling from the PA since the LO frequency well-separated from the RF band.

The proposed 4-element bidirectional phased array block diagram is illustrated in Fig. 3.1(b). The transceiver architecture implements a heterodyne fre-

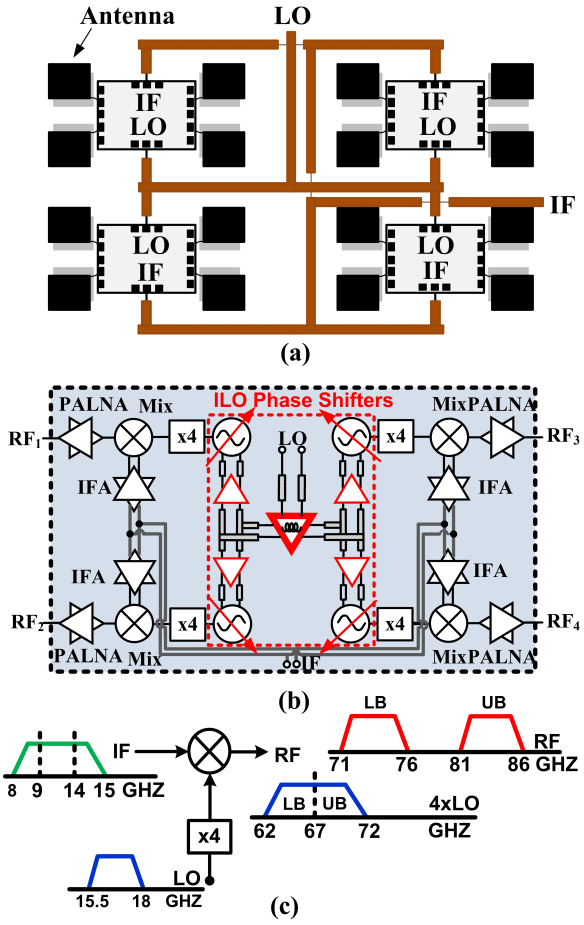


Figure 3.1: (a) Conceptual block diagram of scalable LO-path phased array. (b) Proposed 2x2 bidirectional LO-path phased array block diagram. (c) Frequency planning of *E*-band system.

quency plan shown in Fig. 3.1(c) to eliminate the problems of direct-conversion architectures, such as dc offsets, flicker noise, and IP2. Four VCOs are locked to an external reference to provide channel selection and tune the frequency across the band. In addition, each VCO provides phase shifting through injection locking. The frequency of operation of each VCO is 15.5-18.2 GHz and is multiplied by four (x4) to provide broader frequency range, 62-72.8 GHz, and also widen the phase shifting range. Each of these four LOs drives a bidirectional up/down conversion mixer in each single element of the phased array. The mixer's RF and IF amplifiers are also designed to be wideband, 71-86 GHz and 2-18 GHz, respectively, and combined in the output and input for bidirectional operation. The combiner is designed to provide enough isolation between each RX and TX amplifier (Sec. 3.2.3). The IF ports of each element are also combined on-chip and further amplified by additional bidirectional IF amplifiers while routing through the chip to the IF port.

With a 10-GHz LO tuning range (62-72.8 GHz) and wideband IF amplifiers, the frequency plan uses the upper sideband of the mixing products and requires filtering of the lower sideband products as shown in Fig. 3.1(c). To move the sideband or image signals out of the band of interest, the lower LO signal band, 62-67 GHz, and upper band LO signals, 67-72 GHz, select the lower (71-76 GHz), and upper (81-86 GHz) bands of E band, respectively. If the IF signals are centered at 9 and 14 GHz for lower and upper band, respectively, the image and sidebands will move to the 53-58 GHz band, which are easily attenuated by RF filters and antenna bandwidth limitations.

3.2 Wideband Bidirectional Circuit Implementation

3.2.1 ILO Phase Shifter

Folded cascode architecture is the optimum scheme for current injection in high frequency regime, which is verified in chapter analytically. The proposed

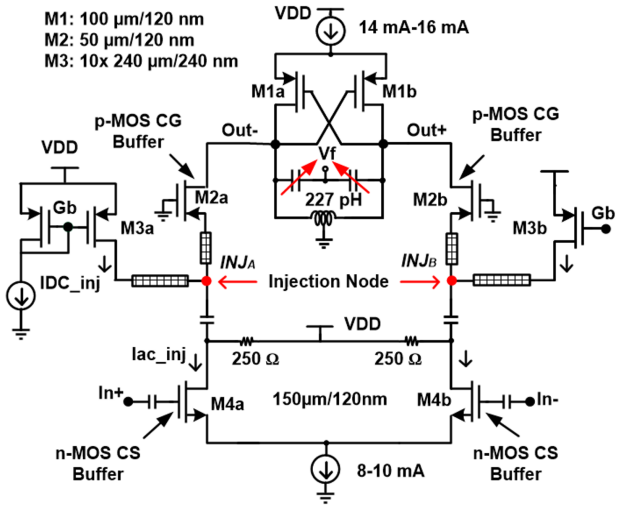


Figure 3.2: Proposed folded-cascode ILO phase shifter.

folded-cascode ILO phase shifter is shown in Fig. 3.2. Cross-coupled p-MOS transistors, M_{1a-1b}, offer lower flicker noise contribution compared to n-MOS transistors when biased at similar dc current. M_{2a-2b} are the common-gate p-MOS transistors with half of the size of M_{1a-1b} with 120-nm length. Common gate injection transistors are biased with M_{3a-3b} current sources. The size of M_3 controls the admittance of the current source, which adds to the parasitic capacitance of the folded node, INJ_A and INJ_B, detailed in the analysis of the locking bandwidth from chapter 2. Moving the parasitic-sensitive node to the source of the injection transistors, INJ_A and INJ_B, rather than the ILO output in the common-source and cascode transistors is a significant advantage. M_3 is sized to create larger impedance than the $1/g_{m2}$ at the interface node, $(\frac{1}{sC_{M3}} \parallel r_o) \geq \frac{10}{g_{m2}}$, by adding smaller capacitance, C_{M3}, to the folded node. The common-source transistor provides injection current and ac coupling from the common-gate transistor and its output impedance also creates a large impedance compared to $1/g_{m2}$. Separate biasing of the injection transistors relaxes the size constraints and provides two degree of freedom for controlling the dc and ac injection current to the ILO.

The oscillator core schematic is illustrated in Fig. 3.3. As described in Sec. 3.1, the LO tuning range covers 62-72 GHz. Since frequency multiplication is employed, the required tuning range of oscillator, $f_{LO}/4$, is 15.5-18.2 GHz corresponding to 16% tuning range. The oscillator design is sensitive to the Q of

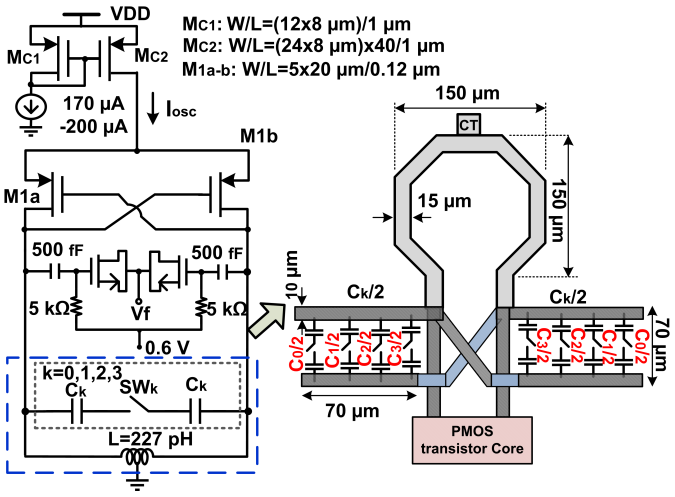


Figure 3.3: Oscillator core schematic with inductor and 4-bit switched capacitors layout illustration.

capacitors and inductors as well as the parasitics associated with routing. While the interconnect inductance between the capacitors and the inductor could be absorbed as a total tank inductance, the routing introduces mismatches as each capacitor in the capacitor bank will not see the same inductance. For this reason, this design sought to minimize the parasitic routing. Given the assumption that 100 μm metal routing provides approximately 70 pH parasitic inductance, the minimum tank inductor value is defined to be at least 3 times bigger than the parasitic inductance, therefore, the inductor value was chosen to be 270 pH. The inductor metal uses top metal layer of the technology with 15 μm width and 150 μm outside diameter. Metal-Insulator-Metal (MIM) capacitors offer smaller footprint with 2.87 $fF/\mu m^2$ density with Q of 20-30. Therefore, 4 bits of MIM capacitors with C_{max}/C_{min} of 3 are used for coarse tuning. However, the capacitors are arranged symmetrically between the differential lines. Two symmetric positive and negative metal lines branch out perpendicularly from each side of inductor and the required capacitance bank is divided by half and distributed to right and left sides as shown in Fig. 3.3. The biggest capacitance value is located closer to the core as it contains the maximum energy transfer to the inductor. With this layout, as each capacitor in capacitance bank turned on, both positive and negative lines see the same amount of capacitance. For fine tuning, n-MOS varactors are used that

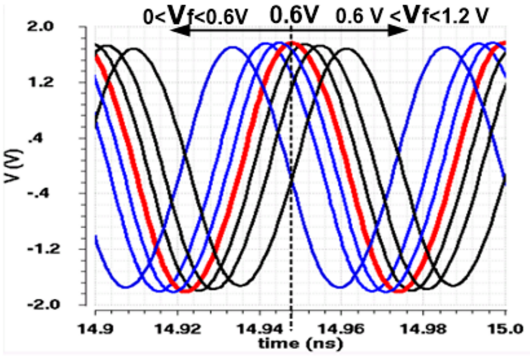


Figure 3.4: Proposed ILO phase shifter simulation results in Cadence using parasitic extraction and EM simulator.

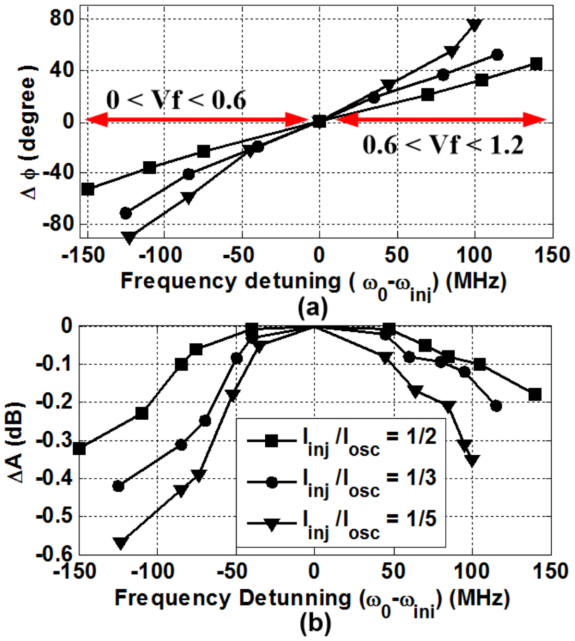


Figure 3.5: Proposed ILO phase shifter simulation at 19.3 GHz using parasitic extraction and EM simulator, a) phase shift VS $\Delta\omega$ for different I_{inj}/I_{osc}. b) amplitude variation for different I_{inj}/I_{osc}.

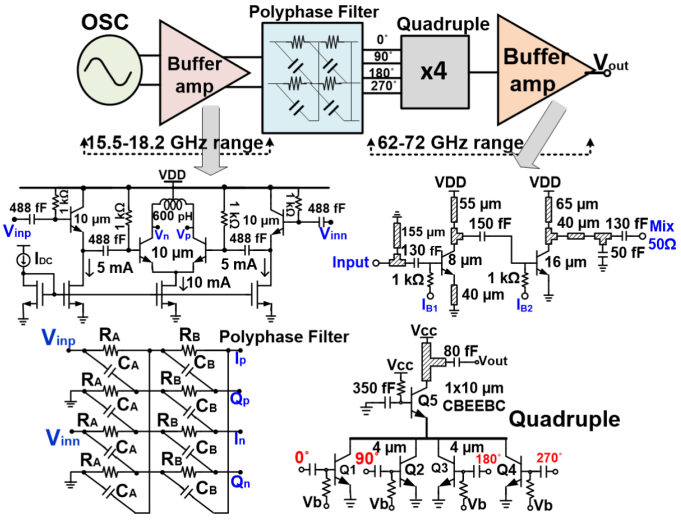


Figure 3.6: Multiplier by ×4 frequency generation path.

limit the quality factor of resonance tank to 7. The varactors are controlled by an analog voltage from 0 to 1.2 V to provide phase shifting along with frequency tuning. The LO simulated tuning range is 21% (16.5-19.8 GHz) and the least significant bit (LSB) of fine tuning of 300~350 MHz which is around two times of the simulated LSB of coarse tuning (120-180 MHz). The simulated transient response of the proposed folded cascode ILO phase shifter for different varactor voltages is shown in Fig. 3.4. In this simulation, the LO is locked to the injected signal with -10 dBm input power at 19.3 GHz frequency, and the LO coarse bits are set to 0000 to oscillate near 19.3 GHz. Tuning the varactor provides frequency detuning and, therefore, a maximum $\Delta\phi$ of 50 degrees is predicted with less than 10% amplitude mismatch, $\Delta A/A$.

In addition, the proposed ILO performance in terms of phase shifting and amplitude variation as detuning the ILO is plotted in Fig. 3.5 (a) and (b) respectively for different ratio of I_{inj}/I_{osc}. For I_{inj}/I_{osc} of 1/2, the simulation results predict a 300-MHz locking bandwidth with $\pm$ 50 $^\circ$ phase shift and under 0.5 dB amplitude variation. While this injection current is larger than satisfied by the weak injection assumptions, the underlying theory is still reasonably correct. Most importantly, it is evident that another benefit of the reduced frequency detuning requirement is the lower amplitude variation to achieve a given phase shift. The

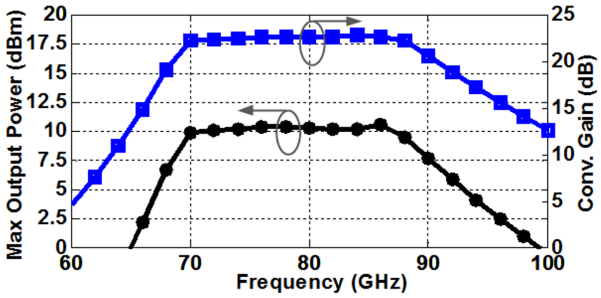


Figure 3.7: LO-path simulated conversion gain and maximum output power versus frequency.

amplitude variation as shown in Fig. 3.5 is explained by the variation of the varactor Q as explained in chapter 2. As the varactor voltage changes, the varactor capacitance varies nonlinearly, [57]. Additionally, the varactor Q changes as the series resistance of the channel varies. For example, the capacitance values are changing with smaller slope for $\omega_{inj} - \omega_0 > 0$ where $0.6 < V_f < 1.2$, and the Q is larger. Therefore, the corresponding amplitude variation is smaller for $\omega_{inj} - \omega_0 > 0$ while for $\omega_{inj} - \omega_0 < 0$ where $0 < V_f < 0.6$ the amplitude variation is larger as the Q is smaller.

3.2.2 Frequency Multiplier

To tune the phase of the oscillator linearly across the 71-86 GHz band, the frequency multiplier and buffers are shown in Fig. 3.6. Firstly, the output voltage of oscillator is buffered with two amplifier stages followed by two polyphase filter (PFF) stages with $f_1 = 1/R_1C_1$ and $f_2 = 1/R_2C_2$. The simulated PFF has 2° degree phase imbalance and less than 1-dB quadrature mismatch within the ILO tuning range (16.5 – 19.8 GHz) and 9-dB loss. The input buffer stages compensate the PFF loss by providing 19-dB voltage gain. Circuit simulations for R-C mismatch predicts less than $\pm 1^\circ$ quadrature phase mismatch and 1-dB amplitude mismatch, resulting in under 0.5-dB power variation at the multiplier output. In addition, the input buffer stage is a variable gain amplifier to calibrate any uncertain and unpredictable mismatches raised from different conditions of process, voltage, and temperature (PVT) variation. The quadrature signals drive

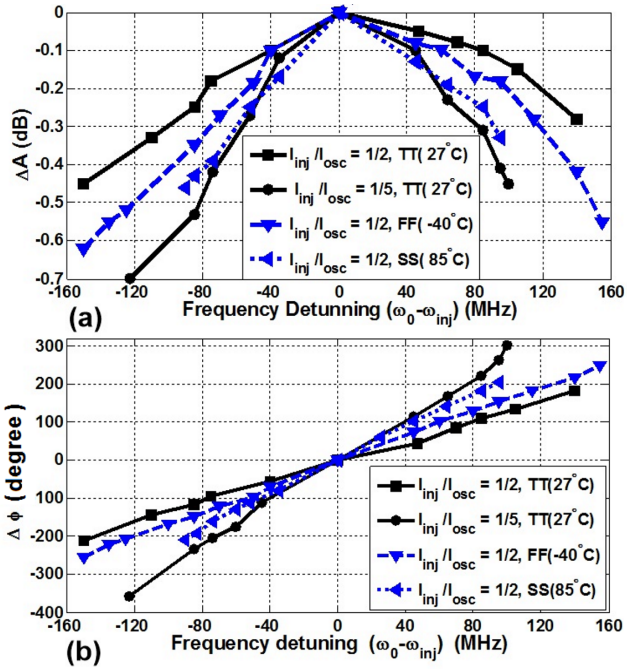


Figure 3.8: Simulation results for 4xILO under 19.3 GHz injection frequency for $I_{inj}/I_{osc} = 1/5$, $1/2$ and two worst-case process conditions, a) amplitude variation versus frequency detuning, $\Delta\omega$, b) phase variation versus frequency detuning, $\Delta\omega$.

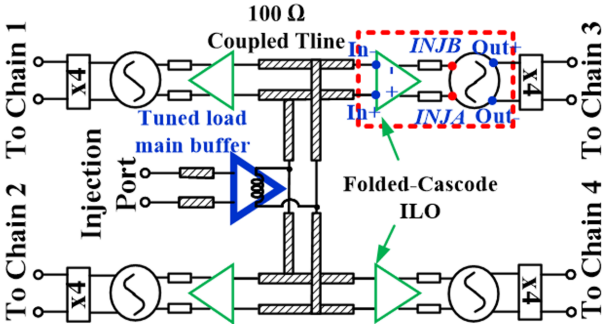


Figure 3.9: Distribution of LO injection reference between each channel's phase shifter.

the transconductance, Q_{1-4}, of the quadrupler circuit, which are combined in the output and connected to CG, Q_5, buffer. The quadrupler consumes 4 mA dc current from 2.5-V supply voltage and provides 1-dB gain.

To increase the power delivered to up/down conversion mixer for higher conversion gain, two wideband amplifier stages are used. This amplifier follows the quadrupler operates from 62-72 GHz is depicted in Fig. 3.6. The first and second stage HBT transistors are biased with 12 mA and 24 mA current, respectively, from a 1.8-V supply. These amplifiers provide an average 15-dB voltage gain within the bandwidth. Fig. 3.7 illustrates the P_{sat} and conversion gain of LO chain over the frequency range which shows 10.2-dBm output power delivered to mixer with 23-dB power gain.

The simulated amplitude and phase shift range of the LO-chain under -10 dBm input injection power at 19.3 GHz is illustrated in Fig. 3.8 a) and b). The output phase shift versus $\Delta\omega$ for two I_{inj}/I_{osc} ratio of 1/2 and 1/5 shows $\pm 300^{\circ}$ phase shift with less than 0.8-dB amplitude variation. The simulation results for slowest and fastest corner cases, SS $85^{\circ}C$ and FF $-40^{\circ}C$, are also plotted. Simulations for different PVT conditions, result in an average 100 MHz variation in the free-running oscillation frequency. Using 4-bit digital coarse tuning with LSB of 120-180 MHz and an analog-voltage controlled varactor with 300-350 MHz LSB can re-tune the free-running oscillation frequency. The phase shifting performance of ILO for these two corner cases from Fig. 3.8 a) and b) illustrates that for slowest condition, SS $85^{\circ}C$, the locking range is reduced by at most 50% and the phase shift range by 10%. The performance under the slow corner (SS $85^{\circ}C$) condition is similar to the typical condition (TT $27^{\circ}C$) performance with smaller injection ratio, I_{inj}/I_{osc} of 1/5. Consequently, the injection current ratio, I_{inj}/I_{osc} , can compensate the locking range or phase shift range under different PVT conditions.

To distribute the LO injection power to the common source amplifiers of each ILO phase shifter of each channel, a tuned load amplifier centered at 18 GHz resonates out the routing parasitic capacitance as shown in Fig. 3.9. The maximum power transfer to each ILO minimizes the input sensitivity. The distribution of injection signal and ILO tanks are located at the same frequency which is another

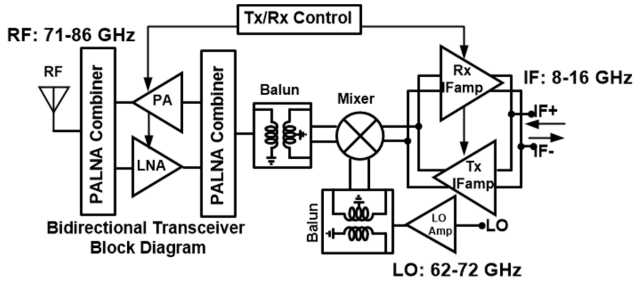


Figure 3.10: Bidirectional front-end block diagram of each channel

feature of the proposed phase shifting approach. The disadvantage of sub-harmonic injection which was used previously [5,42,43] is that a higher-Q tank must filter out the desired harmonic of injection signal which limits the locking range as described in chapter 2.

3.2.3 Bidirectional Front End

The block diagram of the bidirectional front-end for each channel of phased array is shown in Fig. 3.10. The mm-wave bidirectional front-end has been previously reported in [24] at 45 GHz and recently the wideband version at E-band was proposed in [63]. The proposed wideband 62-72 GHz LO-path phase shifter in this work is inherently bidirectional and produces a phase shift for both RX and TX modes. Therefore, the RF and IF amplifiers are designed to be bidirectional and wideband. At this frequency range, 71-86 GHz, the insertion loss of switches as duplexer is very high; so this work uses a transmission-line network that combines PA output and LNA input at the antenna and LNA output and PA input at the mixer [24, 63]. The TX/RX IF amplifiers operate from 2-18 GHz and are connected at the input and output. Since the IF frequency is low, combiners are not needed for IF amplifiers. Switching off the circuit biasing of the complementary amplifier in half duplex operation provides enough isolation and high impedance at the interface node. For the up/down conversion, the mixer is used as MOSFET switches, which are inherently bidirectional due to the source and drain symmetry. The mixer and IF amplifiers are differential while RF and LO amplifier blocks are single ended. Therefore, two wideband baluns are implemented at both RF and

LO ports of mixer.

PALNA The PA/LNA (PALNA) amplifier is shown in Fig. 3.11 and has three amplifier stages controlled with base biasing circuits to enable operation. The first transistor is optimized for low noise-figure and has a $10\,\mu m$ emitter length biased at 15-mA dc current bias and degenerated with a $40\,\mu m$ transmission line (T-line). The T-line is a grounded coplanar waveguide (G-CPW) as shown in Fig. 3.11 and uses one layer below top layer with $7\,\mu m$ width and $8\,\mu m$ distance to ground to provide $50\,\Omega$ impedance. The other two output stages are designed for high-gain and are biased with $4\,\mu m$ emitter length. The input and output matching network of the LNA create $50\,\Omega$ impedance at antenna and mixer port while the interstage are matched for complex conjugate values. The PA contains 4 stages; the final stage is a simple common-emitter structure with $40\,\mu m$ emitter length biased with 55 mA dc-current in class- A configuration. This provides 15 ohm PA loadline impedance, which is transformed to $50\,\Omega$ at the output matching network. The PALNA input/output matching is not affected by combiner transmission line length. However, the combiner transforms the disabled amplifier stages input or output impedance to a large impedance at the combined port. In TX mode, the PA bias is enabled and LNA is disabled. Thus, the PA output is $50\,\Omega$ while the LNA creates a low impedance; therefore, a proper transmission line length at the input of LNA moves the low impedance of LNA input to high impedance at the interface node [63]. This scenario is also applied for the RX mode where the PA is disabled and LNA is enabled. The combiner transmission line length provides impedance transformation and isolation are also shown in Fig. 3.11. The transmission line combiner adds around 1-dB insertion loss to the PA/LNA simulated performance, which is favorable when compared to the insertion loss of a CMOS switch at this band, 2-3 dB. Simulated results of the combined PALNA are shown in Fig. 3.12 and indicate 24-dB gain and 6.6-dB NF at 78 GHz in RX mode. For TX mode, the gain reaches 32 dB, 14.5-dBm saturated output power, and 12% PAE at 78 GHz.

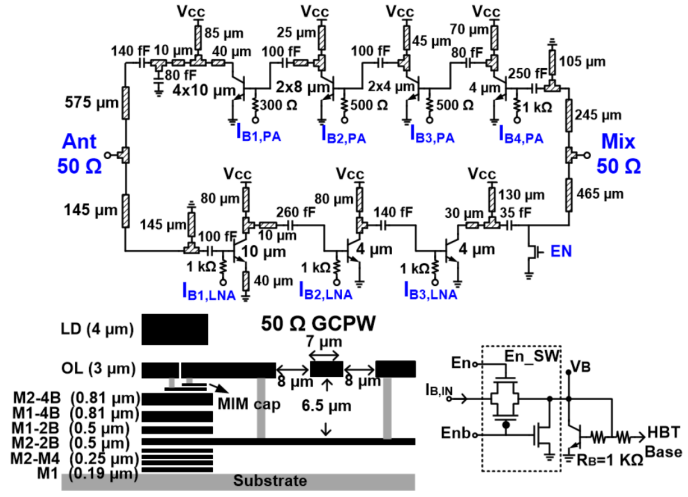


Figure 3.11: Bidirectional wideband PA/LNA amplifier.

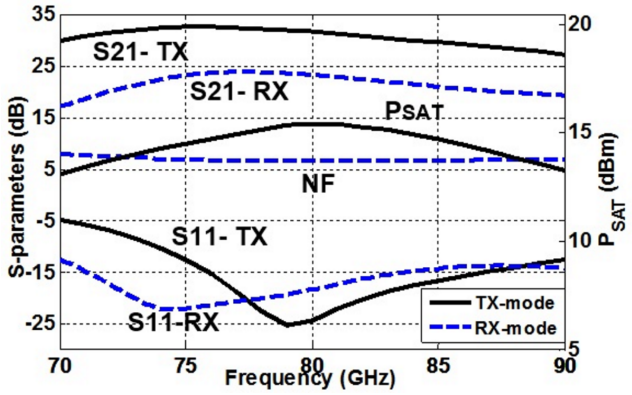


Figure 3.12: PA/LNA Simulation results; S-parameters and P_{SAT} for the PA, S-parameters and NF for the LNA.

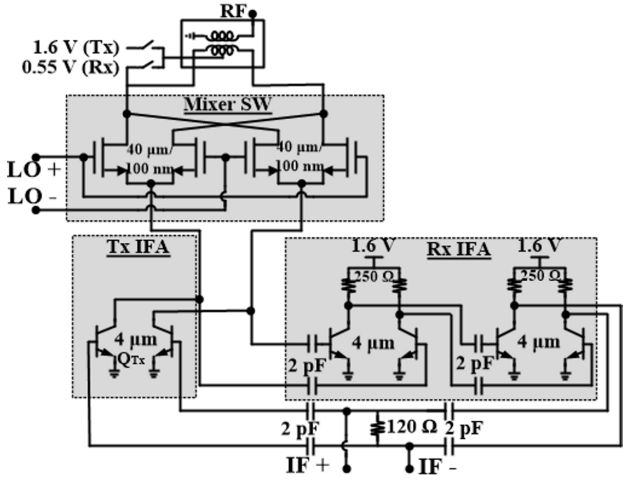


Figure 3.13: Schematic circuit of bidirectional Mixer and IFA.

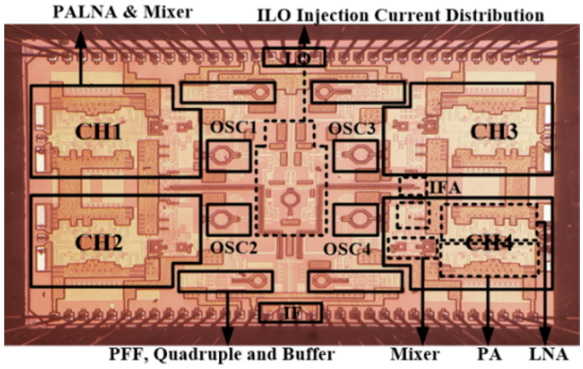


Figure 3.14: A 2x2 phased-array transceiver micrograph.

Bidirectional Mixer and IFA The bidirectional up/down converter is shown in Fig. 3.13. The mixer is composed of four n-MOS transistors in a ring configuration. In RX mode, higher linearity is desired while in TX mode higher delivered power to PA and conversion gain is desired [63]. Therefore, in RX mode, the four n-MOS transistors of mixers are biased with a 0.55-V supply voltage with zero dc-current to create passive mixer for better linearity. Two stages common-emitter HBT amplifier follows the mixer to compensate the loss. In this mode, the connected IF amplifier of TX is disabled by turning off its biasing while in TX mode, the IF amplifier of RX is disabled. This creates big impedance at the interface node of complementary circuit. In TX mode, in order to achieve higher conversion gain, the four mixer transistors draw DC-current through the common-emitter HBT IF amplifier, Q_{Tx}, which creates Gilbert-like active mixer. The output balun also provides output matching for Gilbert mixer. In TX mode, Gilbert mixer provides around 5.5-dB conversion gain and 3.5-dBm output power. In RX mode, the conversion gain is 10.3 dB with -16.2 dBm input P_{1-dB}.

3.3 Phased array Measurement results

The micrograph of 2 x 2 phased array transceiver is shown in Fig. 3.14. The circuit was implemented in 90-nm SiGe BiCMOS process with 10 metal layers interconnection, 9 copper metal and one aluminum top layer and measures 3.4 $\times$ 2.1 mm^2 including pads and ESD. The technology offers HBT transistor with 300

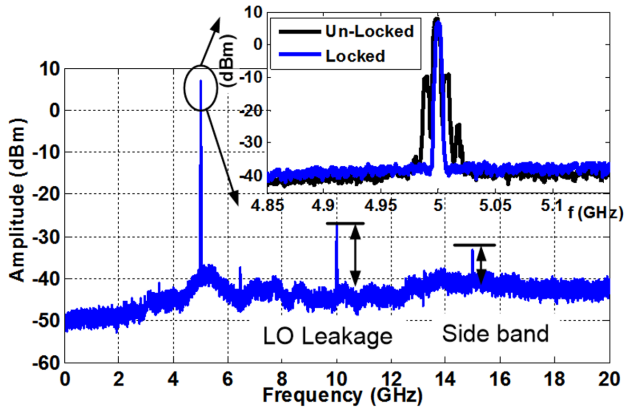


Figure 3.15: De-embedded output power spectrum @ f_{RF} = 71GHz for one channel with f_{IF} = 5GHz, f_{LO} = 16.5 GHz and 76 GHz down-converted LO for discrete mixer in measurement setup.

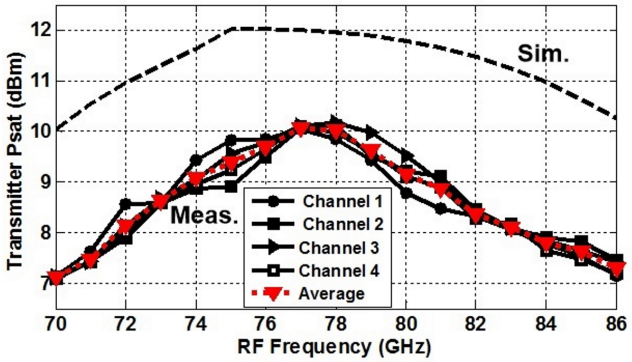


Figure 3.16: Measured transmitter saturated output power for four elements and simulated result.

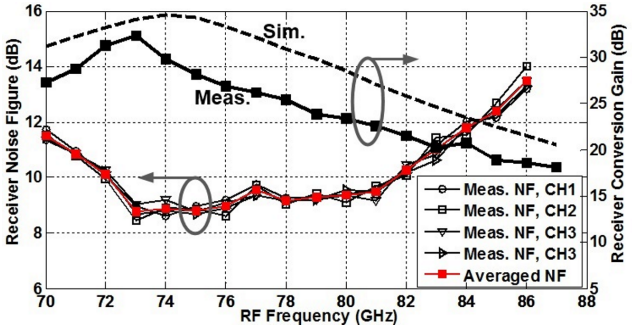


Figure 3.17: Measured and simulated receiver conversion gain and measured NF per channel.

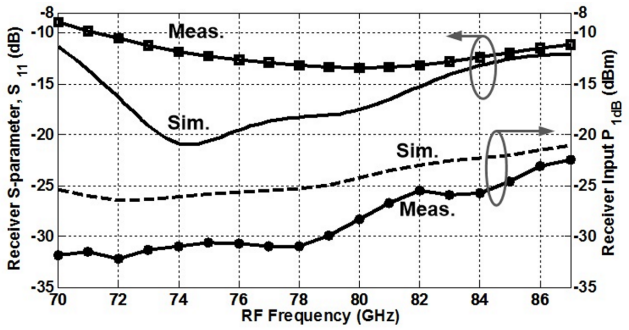


Figure 3.18: Measured and simulated receiver input P1-dB and S11.

GHz/350 GHz f_T/f_{max}, metal-insulator-metal (MIM) capacitors, vertical-natural (VN) capacitors and resistors. The chip is mounted on a Rogers 5880 printed circuit board (PCB) with 10-mil thickness. Multiple dc pads were considered in the chip in order to be able to better characterize single chain performance, and all these dc, LO and IF pads were wire-bonded to the PCB traces. All the RF pads of every element were probed with 1-mm coaxial (GSG) probes. The power consumption of each block is as follows: 17 mW per VCO, 32 mW each quadrupler and its buffers, and 40 mW injection current network (4 local buffers and tuned load amplifier). Every bidirectional front-end also consumes 330 mW and 230 mW in TX and RX mode, respectively.

3.3.1 Transmitter/Receiver Measurement

Fig. 3.15 shows the down-converted output spectrum of one channel using a 5-GHz IF frequency and 16.5-GHz LO, (66 GHz for 4×ILO) to select the 71-GHz channel. An off-chip, 76-GHz LO signal down-converts the signal to sidebands at 5 GHz and 15 GHz, respectively. The LO leakage and sideband rejection are higher than 40 dB. The saturated output power, P_{SAT}, for the four channels and the average results over 71-86 GHz bandwidth are shown in Fig. 3.16 and also compared with average simulation results. The average P_{SAT} reaches maximum value of 10 dBm and remains higher than 7.2 dBm over the 3-dB bandwidth. The power measurement is performed by using W8486A for power sensing and Agilent E4419B power meter for power reading. The average conversion gain of

each channel is 24.5 dB in TX mode and the input return loss is better than 10 dB over the 71-86 GHz band.

The receiver NF of every array element is measured using the gain method [57] and shown in Fig. 3.17. The average NF_{min} is 9.5 dB and remains below 14 dB within 70-86 GHz. The average conversion gain of single element is around 26.2 dB which is considered in NF measurement and also shown in Fig. 3.17 and compared with circuit simulation results. In addition, the measured receiver RF port input return loss is below 10 dB and the input compression port is better than -30.6 dBm over the bandwidth as shown in Fig. 3.18 with the simulation results. The difference between simulation and measurement results, 2 dB of P_{SAT} and 5 dB of conversion gain arise from underestimated loss in the interconnects and passive elements. For example, the Q of capacitors simulated with a 2.5D electromagnetic simulation (EMX) differs by a factor of 5 when compared to simulations based on process design kit (PDK). An average 2 dB lower measured maximum available gain for transistors and 1 dB/mm more loss for transmission line was found in test cells, resulting in shifted measured gain and frequency response compared to PDK-based simulations.

3.3.2 ILO Phase Shifter

The RF port of each element is probed to characterize the performance under free-running and locked conditions. The measured VCOs have a tuning range from 15.5 to 18.2 GHz as shown in Fig. 3.19(a), using the 4-bit digital control word for coarse tuning and analog voltage, V_f. The least significant bit (LSB) of the coarse tuning is equal to 140 MHz for low-frequency band (LB), *i.e.* 15.5 GHz, and 170 MHz for high-frequency band (HB), *i.e.* 18.2 GHz. The analog fine tuning is 280 and 350 MHz for the LB and HB, respectively. The measured locking range is also illustrated in Fig. 3.19(b) versus detuning frequency and compared with simulation result. The LO injected power is 3 dBm and the average ILO locking range is approximately 220 MHz, close to the predicted 300 MHz by simulations. The transient response of the locked transmitter is shown in Fig. 3.20 a) for 78°, 190°, and 290° phase shifts with analog fine tuning voltage, V_f. The channels are

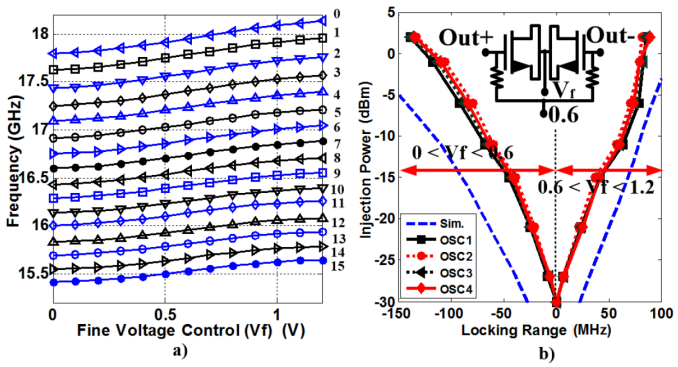


Figure 3.19: ILO average measurement for a) free-runing TR, b) locking range when four phase shifters locked and simulation result.

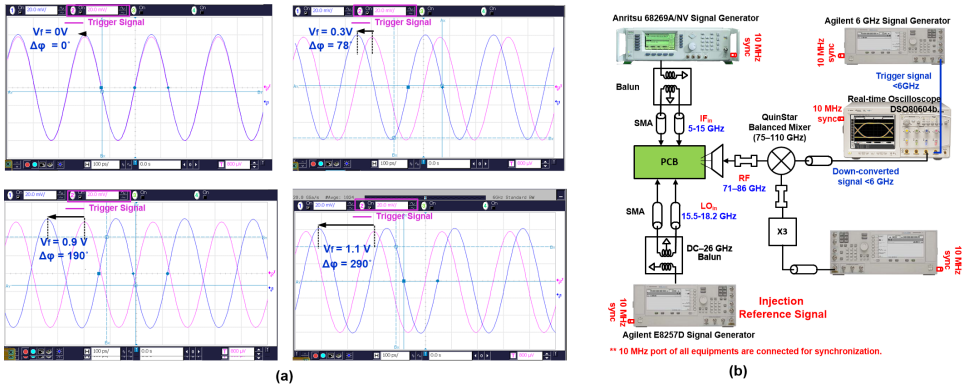


Figure 3.20: ILO phase shifter measured transient response (*.csv data) from oscilloscope for single element locked at $f_{inj} = 16.5GHz$ under different phase shift, a) 78° , 190° and 290°b) measurement set-up.

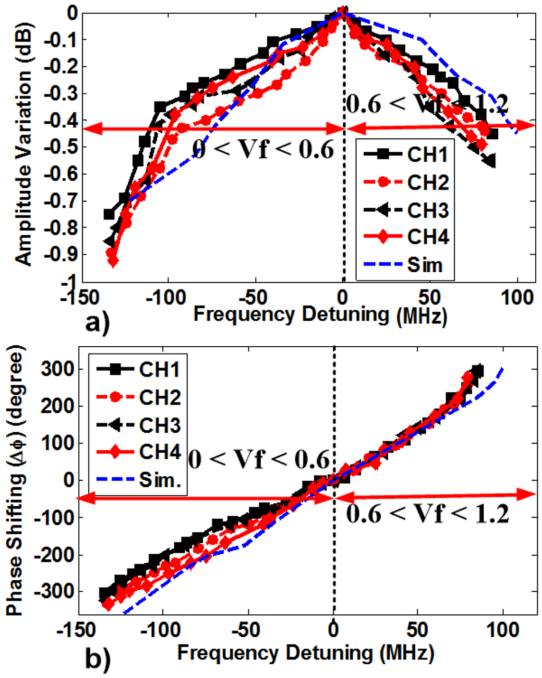


Figure 3.21: ILO phase shifter averaged measured and simulated results a) amplitude variation versus $\Delta\omega$, and b) phase shifting versus $\Delta\omega$.

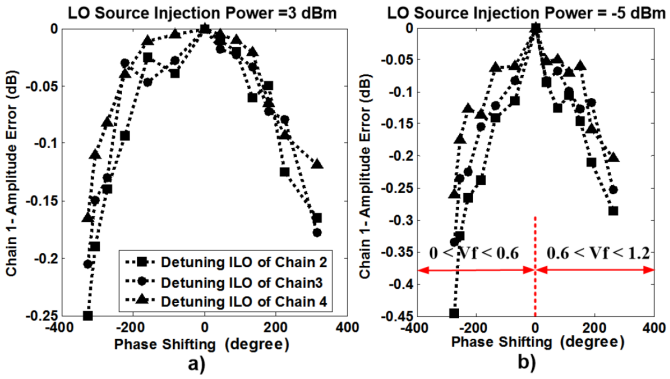


Figure 3.22: Measured channel to channel isolation for injection power a) 3 dBm and b) -5 dBm.

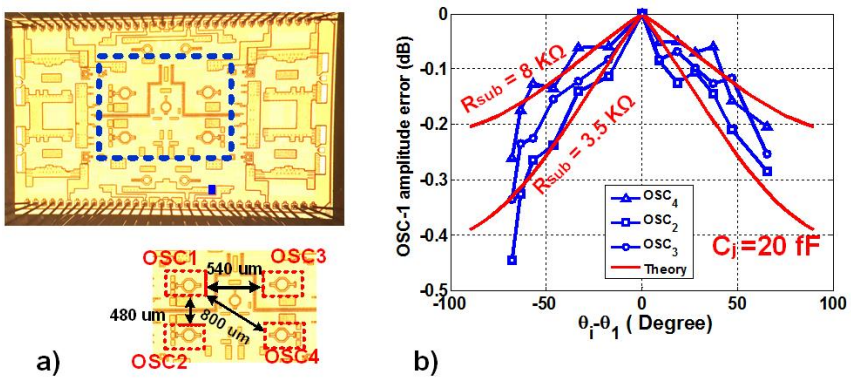


Figure 3.23: 2x2 ILO phase shifter placement and distance to each other, b) amplitude error of OSC1 due to relative phase changes to other OSC and the comparison with revised amplitude dynamic, (43).

locked through an Agilent source signal at LO port and the RF port is probed and down-converted to lower frequency with a W-band mixer. The down-converted signal is captured with real-time oscilloscope (DSO80604b) and compared with a reference signal as a trigger, Fig.3.20 b) shows this. The measured phase shift and amplitude variation for the four channels under 3-dBm injection power are shown in Fig. 3.21 a) and b), respectively. The amplitude variation is under 1 dB and the phase shift range is $\pm 300°$ as the ILO is detuned over the locking range. High-frequency coupling causes amplitude variation and errors between channels. Fig. 3.22 shows the amplitude variation of channel 1 when the ILO of other channels varies. When the injected power is -5 dBm, the amplitude error is around -0.5 dB. When the injected power is 3 dBm, the amplitude error is under -0.25 dB.

To verify the matching of the amplitude and phase dynamics that derived in chapter 2.4 and expressed in equations (43) and (44) with the measurement results, the ILO number 1 was probed while the other ILO2-4 were de-tuned separately over their locking range. The unilateral injection current of ILO1 did not capture the effect of parasitic coupling path. The measurement results shown in Fig. 3.23 b) demonstrate that ILO4 has the lowest amplitude error compared to other ILOs as it has the largest distance to ILO1. To approximate the substrate parasitic coupling values, Cj, C_{sub}, and R_{sub}, used in (43) and (44), these parameters were swept separately to fit to the plots. For example, by assuming C_j equals

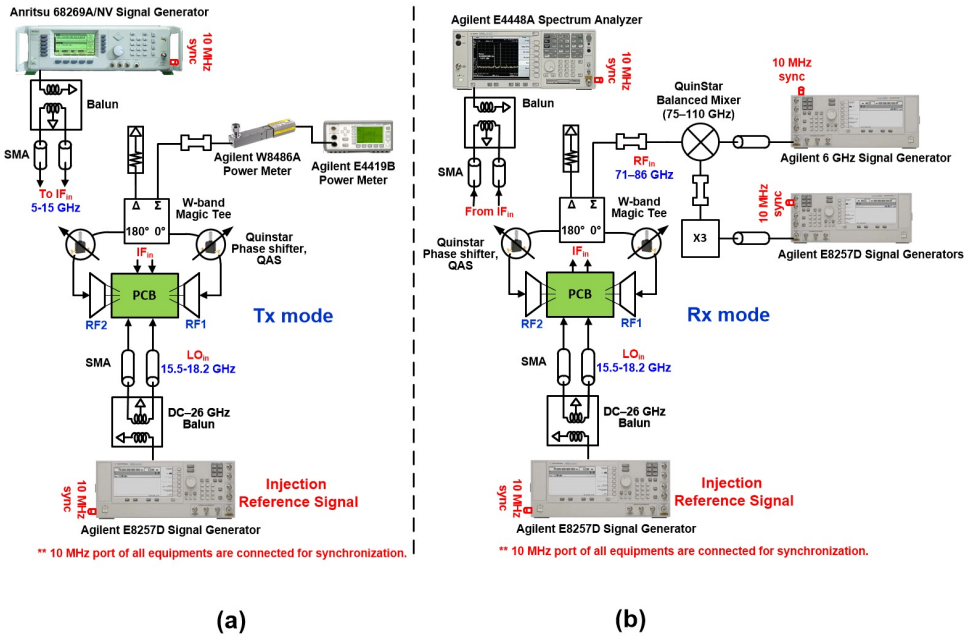


Figure 3.24: Measurement set-up for array pattern measurement for phased array using ILO phase shifter a) for Tx mode, b) for Rx mode.

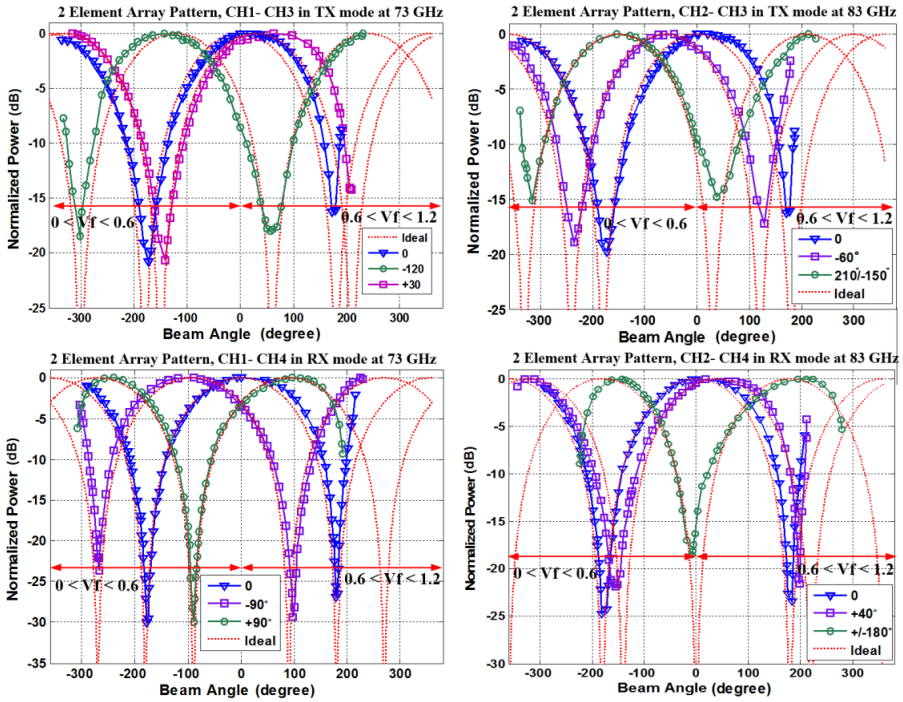


Figure 3.25: Measured 2-element array pattern for: a) CH1-CH3 in TX mode at 73 GHz, b) CH2-CH3 in TX mode at 83 GHz, c) CH1-CH4 in RX mode at 73 GHz, and d) CH2-CH4 in RX mode at 83 GHz.

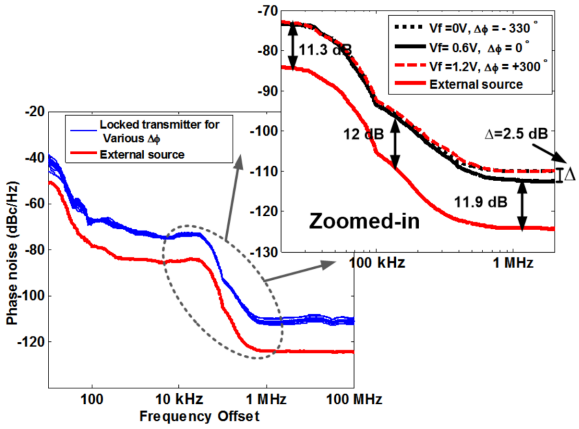


Figure 3.26: Measured locked transmitter phase noise for different phase setting and frequency detuning at 73 GHz compared to the LO external injection source.

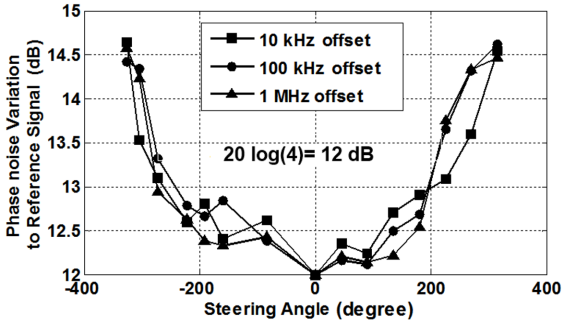


Figure 3.27: Phase noise variation to 12 dB theoretical value compared to LO source versus scanning angle (phase shift) at different offset frequencies.

to 20 fF, the amplitude equation (43) will fit the ILO4 amplitude error curve at R_{sub} equal to 8 kΩ, while it fits the ILO2 amp-error curve at 3.5 kΩ. The distance between ILO1-ILO4 is twice the distance be-tween ILO1-ILO2, which predicts the parasitic R_{sub} must be twice in the former. This shows an acceptable agreement of the derived amplitude and phase relations, (43) and (44), to be used for consider-ing unpredicted parasitic coupling path in the design of injection-locked oscillator circuit.

The TX and RX array patterns measurement setup is shown in Fig. 3.24. The measured results are shown in Fig. 3.25 at 73 GHz and 83 GHz in both TX and RX modes. Discrete phase shifters are inserted in RF path to emulate the propagation delays of the antenna array. For the TX mode, two channels were

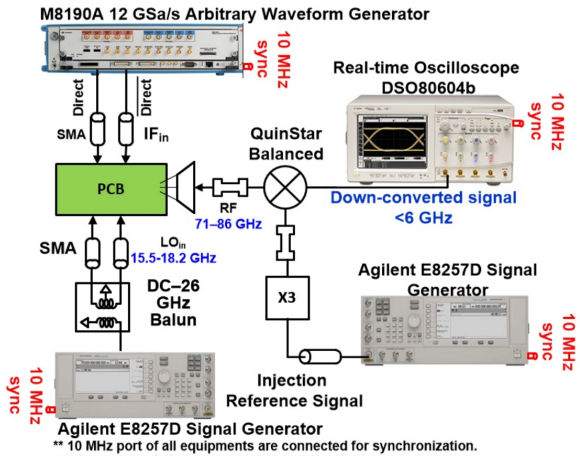


Figure 3.28: Transmitter modulation setup.

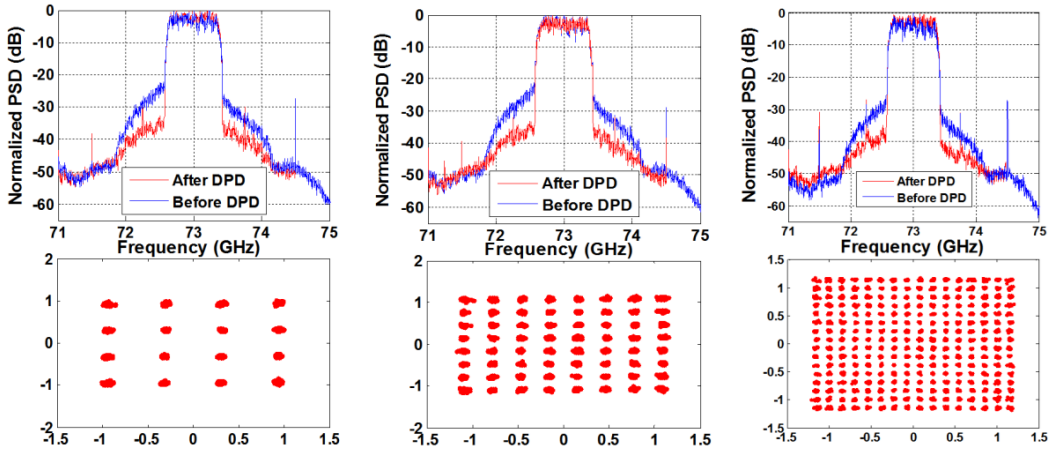


Figure 3.29: Modulation measurements results for 16 QAM (3Gb/s), 64 QAM (4.5 Gb/s), and 256 QAM (6 Gb/s).

probed while the discrete phase shifter set to a certain value. The ILO phase shifter reproduces the pattern over the ±300° phase shift range with continuous phase resolution. The *E*-band front-end produces below 20-dB peak to null ratio which reduces to 15 dB for the bigger beam steering angles as the phase shifter enters to near the locking edge in these states. Operating near the locking edge increases the amplitude mismatch and errors as illustrated in Fig. 3.21, which consequently decreases the peak-to-null ratio in the overall array factor performance.

For ILO phase shifter, the phase noise contributes to the integrated phase jitter. ILO phase noise follows the reference sources noise and jitter, therefore,

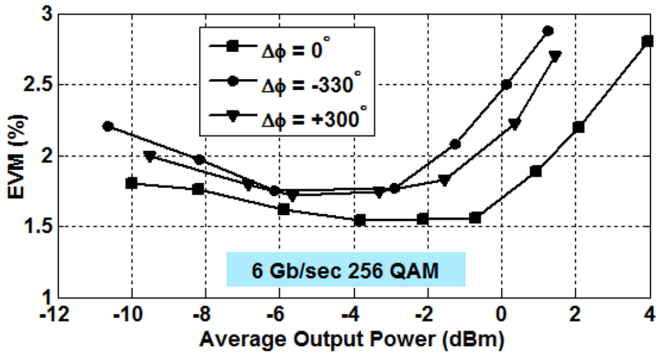


Figure 3.30: Measured EVM of transmitter for three phase state, 0° ,+300°and −330° versus averaged P_{out} for 256 QAM.

another limitation of phase resolution is the injection reference phase jitter. The root-mean-square phase error can be estimated from the phase noise according to

$$\phi_{RMS,source} = \sqrt{2 \times 10^{\int_{f_{min}}^{\infty} L(f)\, df/10}}, \tag{3.1}$$

However, multiplication by four will increase the error of ILO output by four as:

$$\frac{\phi_{RMS,ILO_{out}}}{\phi_{RMS,source}} = \sqrt{10^{(\Delta A/10)}} = 3.98, \tag{3.2}$$

In other words, multiplication by four will add $20\log_{10} 4 = 12$ dB to the phase jitter of the signal source and the rms phase jitter is increased by a factor of 4. However, the phase resolution variation as the phase shifter changes to different state is also important which defines the phase error within scanning angle. The phase noise of the RF output at 73 GHz is plotted in Fig. 3.26 for different phase shifter states with a reference at 16.5 GHz. The locked transmitter has -72.9 dBc/Hz at 10 kHz, -93.2 dBc/Hz at 100 kHz, and -112 dBc/Hz at 1 MHz. Integrating the jitter over a 100-MHz bandwidth and using (3.1) and (3.2) results in roughly 2° rms phase uncertainty to the transceiver output. However, the phase resolution is limited by the discrete phase shifter used in the measurement setup. The theoretical difference between the RF output and injection source are equal to frequency multiplication factor. To discriminate the transmitter phase

noise from the down-converter phase noise, the phase noise of the LO provided to the measurement discrete down-converter must be better than the injection LO source, which has a noise floor of -124 dBc/Hz at 1-MHz offset and is 12 dB lower than the RF output phase noise. The phase noise of the transmitter under different steering angles and detuning frequency range is also shown in Fig. 3.27 for different offset frequencies. Multiplication by 4 degrades the phase noise by 12 dB but an additional 2.5 dB penalty is observed over the steering angles that cover +/-180 degrees. This 2.5-dB phase noise variation across the scanning angle range results maximum $\sqrt{10^{(0.25)}} = 1.33^{\circ}$ phase uncertainty to the transceiver output.

3.3.3 QAM Modulation

Complex modulation such as QAM modulation demonstrates multi-gigabit-per-second data rates. At high frequency, PA non-linearity, LO leakage and phase noise are the main constraints for QAM modulation. Injection locking improves the transmitter phase noise as the locked oscillators track the reference phase noise within the locking bandwidth as explained in Sec.3.3.2.

PA non-linearity distorts the transmitter output signal and poses a more significant SNR degradation at peak power than the LO phase noise. Digital pre-distortion (DPD) can be implemented to compensate the compression of the PA [64,65]. The memory polynomial model (MPM) was used to model the LO-leakage, I/Q imbalance impairment, amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) compression of the PA as

$$y(n) = \sum_{m=0}^{M} \sum_{k=0}^{K} c_{m.k}\, x(n-m)\, |x(n-m)|^{k-1} + c_i, \tag{3.3}$$

where K is the non-linearity order and M is the memory depth which were set to 5 in our measurement setup. The dc offset, c_i, is applied to the model to compensate the LO leakage. The DPD modulation setup is also shown in Fig. 3.28. Firstly, arbitrary digital I/Q data is generated using a 12 GS/s generator and applied to the IF port of phased array and monitored on a single channel. The down-converted output is captured by 6 GS/s real-time oscilloscope and pre-

Table 3.1: Mm-wave Phased Array Comparison, W-band and E-band

	[16]	[17]	[18]	[5]	[10]	**This Work**
Frequency (GHz)	76-82	70-100	76-84	60	77	**70-86**
Function	TX/RX	TX/RX	RX	TX	TX	**TX/RX**
3-dB Bandwidth (GHz)	6	20	8	5	2.5	**16**
# of Elements	8 RX, 8 TX	4	16	4	4	**4**
Phase Shifting	Active RF	Active RF	Active RF	LO Phase shifter	LO- I/Q [1]PI	**[2]ILO**
TX Gain / element (dB)	>10	N/A	-	20	40.6	**>20**
TX P_{sat}/ element (dBm)	2-4	>6	-	11	12.5	**7.2-10**
TX output P_{1-dB} (dBm)	N/A	N/A	-	N/A	+10.2	**+7.5**
RX Gain / element (dB)	>5	>25	11-16	-	-	**>20**
RX input P_{1-dB} (dBm)	-10	-35	-26	-	-	**-30.6**
RX NF / element (dB)	17	<7	11.4-13	-	-	**9-14**
Constellation	N/A	16 QAM-32 QAM	N/A	N/A	N/A	**256 QAM**
Data Rate (Gb/s)	N/A	10	N/A	N/A	N/A	**6**
DC Power	RX: 1.6 W TX: 0.94 W /Total	TX/RX: 0.5 W /element	RX: 1.2 W /Total	147.5 mW/element	460 mW/ element	**RX: 286 mW, TX: 386 mA /element**
Area (mm^2)	26.1	3.4	31.9	4.06	25.84	**7.1**
Technology	BiCMOS $0.12\mu m$	BiCMOS $0.18\mu m$	BiCMOS $0.12\mu m$	65 nm CMOS	BiCMOS $0.12\mu m$	**BiCMOS $90nm$**

1 PI=Phase Interpolator.2 ILO= Injection-Locked Oscillator.

Table 3.2: Mm-wave LO-path phase shifter comparison

	[10]	[4]	[42]	[43]	**This Work**
LO-path Frequency (GHz)	50.3-55.5	43.7-52	24	42.75-49.5	**62-72.8**
Phase Shifting Technique	I/Q- PI	I/Q- PI	ILO	ILO	**ILO**
Phase Shift Range (degree)	N/A	45°, 90°, 180°	±180°	±90°	**±300°**
Phase Resolution (degree)	N/A	45° Discrete	4°	22.5°	**2°~5°**
Amplitude Mismatch (dB)	1.5	~4-1.6	1.5	±0.4	**0.4-0.9**
# of Path	4	2	2	4	**4**
Power/total (mW)	362.7	51.5	24	85	***236**
Technology	BiCMOS $0.12\mu m$	CMOS 90 nm	SiGe $0.13\mu m$	CMOS $65nm$	**BiCMOS $90nm$**

* Limited to 5°by measurement equipment and 2°is from phase jitter. ** 4 VCO, 4 injection buffers + 4 quadrupler and buffers.

distorted using MATLAB based on eq. (3.3). The new predistorted signal is resent to the transmitter to linearize the PA. The input signal has 750 MHz bandwidth and is located at a 4.5 GHz IF frequency. The input modulated signal bandwidth and center frequency are chosen based on the 6 GS/s oscilloscope sampling rate. Fig. 3.29 represents the results for 16 QAM (3Gb/s), 64 QAM (4.5 Gb/s), and 256 QAM (6 Gb/s) at a 7-dB average output back-off power before and after DPD. DPD is shown to improve the ACPR of the output spectrum as it calibrates the AM-AM and AM-PM PA non-linearity while the in-band improvement indicates below 3% transmit EVM. The spurs were present both before and after DPD and exist because of the out-of-band spurs that are present in the DAC. To observe the effect of amplitude and phase noise variation on the ILO phase shifter near the edge of the locking range, QAM modulation is applied on the locked transmitter under three ILO phase state 0° ,+300°and −330° shown in Fig. 3.30. To compare them at the same output power within the 750 MHz bandwidth, the amount of LO injection power for 0° state was around -13 dBm and for ±300° state was around -10 dBm. As the ILO approaches the edge of the locking range, the phase noise degrades by 2.5 dB and amplitude is reduced by 1 dB, resulting in under a 1% EVM variation in the transmitter modulation signal which proves another significant feature of ILO based phased array. The comparison of this work with other E- and W-band phased array are shown in Table. 3.1. As it can be seen, it is the first phased array above 70 GHz using ILO phase shifter which also provides operation over a 16-GHz band. Table 3.2 also compares the proposed folded-cascode ILO phase shifter with other state-of-the-art LO-path phase shifters. This work is the first ILO phase shifter above 60 GHz is wideband and consumes only 60 mW per channel. It can cover $\pm 300^\circ$ phase shift range with low amplitude and phase error.

Acknowledgment

We are grateful for support from Nokia for this research and, in particular, Mr. Tom Kovarik. This chapter is mostly a reprint of the material as it appears in [61], N. Ebrahimi, P. Wu, m. Bagheri and J. F. Buckwalter, "A 71-86 GHz Bidi-

rectional Phased-Array Transceiver using Wide-bandwidth Injection-locked Oscillator Phase shifter", IEEE Transactions on Microwave Theory and Techniques, 2017. The dissertation author was the primary investigator and author of this paper and materials.

Chapter 4

A Novel Image Selection Bidirectional Architecture

4.1 EVM Degradation in Wideband Transceivers

For M-QAM communication systems, the signal to noise ratio (SNR) and error vector magnitude (EVM) are related. On the other hand, SNR, bit-error rate (BER) and signal-error rate (SER) are related to each other. Therefore, EVM is also related to BER/SER as [66]:

$$P_{e,s} = 4 \times Q(\sqrt{\frac{3}{(M-1)\,EVM^2}}). \tag{4.1}$$

$$P_{e,b} = 1 - (1 - P_{e,s})^2. \tag{4.2}$$

Fig. 4.1(a) illustrates the BER for 16 and 64 QAM. At a BER of 10^{-5}, the EVM should be below 5% and 10% for 64- and 16-QAM, respectively. Lower EVM is needed for higher order QAM that provides the benefit of more spectral efficiency. However, the EVM is degraded by circuit nonidealities including local oscillator (LO) leakage, LO phase noise, DC offset, conversion gain flatness, I/Q mismatch and non-linearity. The LO leakage and DC offsets are the common issues with homodyne-based architecture and heterodyne schemes trade LO leakage for image

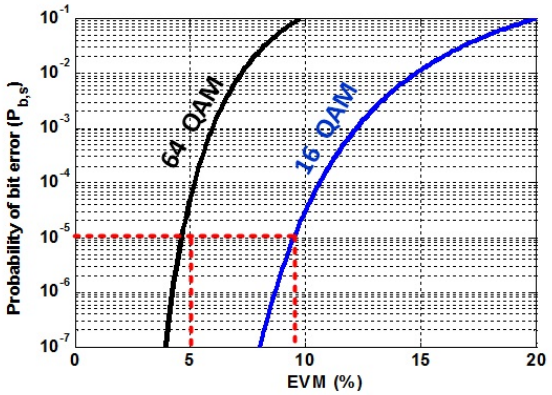


Figure 4.1: Probability of bit error rate versus EVM.

rejection. Using a double-balanced mixer will also improve the LO to RF isolation to suppress LO leakage. The nonlinearity of the PA is mitigated under back-off at the cost of efficiency. The LO generation frequency path driving the quadrature mixer causes sever issues for modulation constellation. Besides the LO phase noise which rotates the constellation, the amplitude and phase mismatch of the quadrature LO paths will degrade the EVM as not providing desired attenuation of unwanted image band and flat conversion gain of mixer within the operation bandwidth. In other words, the amplitude and phase mismatch both degrade the IRR and cause unequal conversion gain within the modulated signal bandwidth. For wideband mm-wave communication systems, I/Q mismatch and LO phase noise are the significant limitations to realize high-order QAM [48]. Assuming each impairment is independent, the EVM of the affected of these impairments in a heterodyne system is

$$EVM \approx \sqrt{EVM_{IRR}^2 + EVM_{LO-PN}^2} \tag{4.3}$$

Where the EVM_{IRR} and EVM_{LO-PN} are the EVM contribution of image rejection ratio (IRR) and rms phase error of LO phase noise, respectively. Equation (4.3) can be approximated considering the EVM of IRR and LO phase noise as follows:

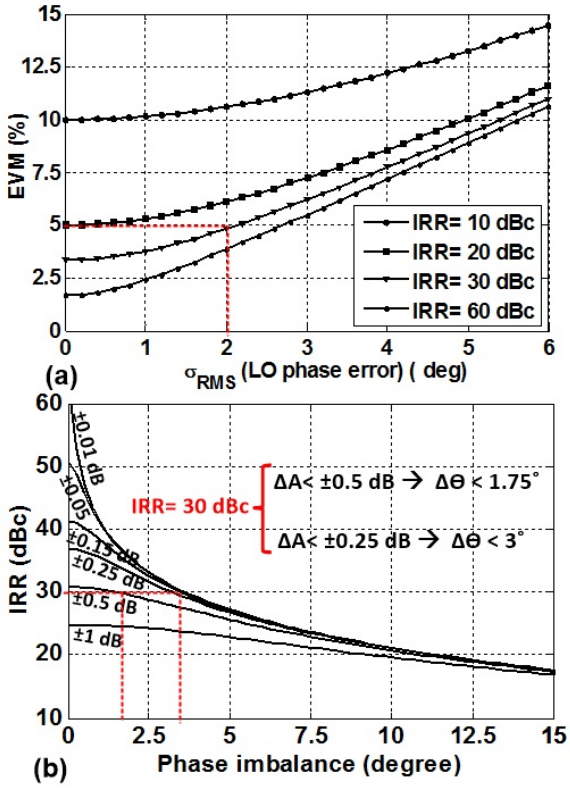


Figure 4.2: EVM and circuit impairments: a) EVM dependence to IRR and RMS value of LO phase noise, b) IRR dependence to I/Q amplitude and phase imbalance.

$$EVM \approx \sqrt{\frac{1}{IRR^2} + \sigma_{PN}^2} \tag{4.4}$$

Where σ_{PN}^2 is the RMS value of the LO phase error caused by LO phase noise.

4.1.1 Phase Noise

The rms LO phase error can be calculated from the phase noise spectrum:

$$\sigma_\phi^2 = 2 \times 10^{(\int_{f_{min}}^{\infty} L(f)\, df)/10}. \tag{4.5}$$

The phase noise power spectral density $L(f)$ directly determines the integrated phase error. For mm-wave applications that desire to cover a large frequency

band such as E-band which covers 10 GHz bands over 15 GHz frequeny spectrum, a large fractional bandwidth of LO is required to both tune the RF band and channel bandwidth. For instances, recent work [17, 45–48, 61] required a tuning range of more than 15 GHz for the RF quadrature mixer to tune the IF signals to E-band. This wide band width requirement of tuning range of LO has the severe effect on both LO phase noise and IRR and therefore the EVM according to (4.4). The phase noise is dependent to frequency and quality factor as:

$$L(f) \propto \frac{1}{Q_L^2}(\frac{f_0}{f_m})^2 = \alpha(\frac{B_{FR}}{f_m})^2, \tag{4.6}$$

where f_0 is the oscillator carrier frequency, f_m is the frequency offset from the carrier, B_{FR} is the fractional bandwidth of oscillator, and Q_L is the loaded Q of the resonator and is assumed to be directly related to the tuning range requirements of the VCO, i.e. $Q \propto {}^{f_0}/_{B_{FR}}$. From (4.6), the phase noise of the oscillator increases with the tuning range requirements and, consequently, increases the EVM. For this reason, many E-band solutions consist of separate frequency synthesizer solutions for the upper band and lower band. Fig. 4.2a) demonstrates the EVM versus rms phase noise for different IRR ratios. As it is shown, for a typical 30 dB IRR, the rms phase error of less than 2 degrees is desired to achieve the required 5% EVM for 64 QAM modulation. This 2 degree corresponds to an average from -115 dBc/Hz to -120 dBc/Hz at 1 MHz offset for LO phase noise according to (4.5). Therefore, it will add stringent requirement on the oscillator design to meet the phase noise requirement. Previous chapter proposed injection-locked technique to achieve this low phase noise criteria for multi Gb/s data rate at E-bands.

4.1.2 Image Rejection Ratio

The IRR is related to the amplitude mismatch, ΔA, and phase mismatch, $\Delta\theta$ between the I and Q signal paths [57, 67].

4.1

$$IRR = \frac{1 + 2(1+\Delta A)\cos(\Delta\theta) + (1+\Delta A)^2}{1 - 2(1+\Delta A)\cos(\Delta\theta) + (1+\Delta A)^2} \tag{4.7}$$

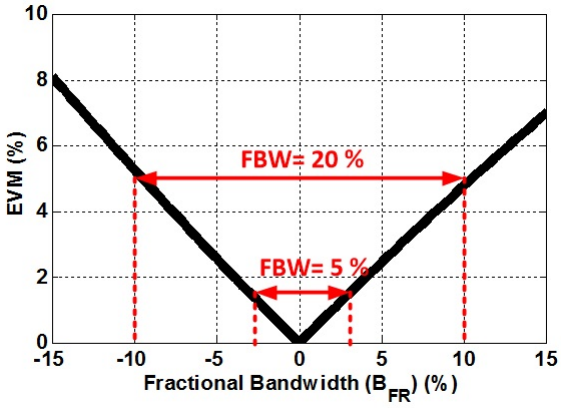


Figure 4.3: EVM versus LO fractional bandwidth.

For achieving an IRR of 30 dB, the for amplitude mismatch of ± 0.5 and ± 0.25 the phase mismatch must be lower than 1.75° and 3° according to (4.7) , Fig.4.2 b) illustrates this.

To learn the impact of large FBW on the I/Q imbalances and IRR, the quadrature generation circuitry should be analyzed. The transfer function of single-stage PPF for positive and negative frequencies are

$$H(\pm\omega) = \frac{1 \mp \tau\omega}{1 + j\tau\omega} \tag{4.8}$$

where $\tau = RC$ defines the pole of the filter. The magnitude of positive transfer function shows the desired signal band-passing through the filter while the negative part corresponds to the image attenuation, therefore the IRR equals to:

$$IRR(\omega) = \left|\frac{1 - \tau\omega}{1 + \tau\omega}\right| \tag{4.9}$$

Fig. 4.3 illustrates the EVM versus fractional bandwidth, as the fractional bandwidth increases from 5% to 20%, the EVM increases from 1.3% to 5.3% multiplied by 4. If a 10% RC variation is accounted for, the EVM increases to 10% and 4% for 20% and 5% FBW respectively.

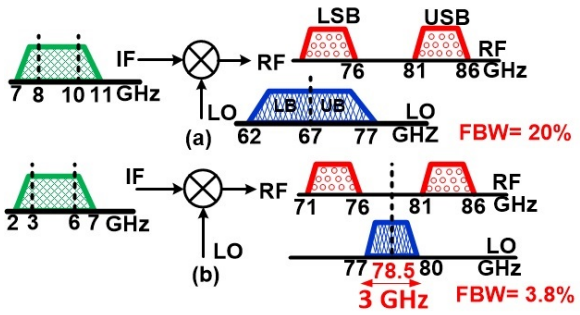


Figure 4.4: Frequency planning of E-band systems, a) conventional architecture, [17, 45–48, 61], b) proposed image-selection architecture.

4.2 Frequency Plan for Low Fractional Bandwidth

The previous work on mm-wave transceivers and, in particular, for E-band use the LO fractional bandwidth in the order of 20% [17, 45–48, 61]. Fig. 4.4 illustrate the frequency planning comparison between the conventional architecture such as proposed in the previous work, [17, 45–48, 61], and our proposed image selection scheme. In the proposed architecture, the LO frequency should be placed between the two upper (81-86 GHz) and lower band (71-76 GHz) of E-band. Since 77 GHz is commonly used for automotive radar, this frequency band is not required and can be filtered out. The feature of the image selection architecture is that lower and upper bands are images of each other,and selecting one band or the other allows us to access both frequency bands with little tuning range variation. Therefore, the image-selection architecture is a modification of a traditional image-rejection architecture where a phase inversion is introduced to select either the upper and lower band. The proposition of this idea is that this frequency plan reduces the tuning range to less than 3 GHz and results in more uniform circuit performance in terms of conversion gain and IRR. The IRR is also subject to a smaller tuning range and therefore is not prone to bandwidth induced amplitude and phase mismatch, which relaxes the PPF requirements and, therefore the EVM.

4.2.1 Image Selection Architecture

For an image rejection architecture, the RF signal must be operated with quadrature mixers operate such that the two RF bands, 71-76 GHz and 81-86 GHz are the images to each other. The most common image-rejection architectures are Hartley and Weaver [57]. The Hartley architecture requires a quadrature phase generation circuitry such as RC polyphase filter at the IF signal path for RX mode or at the RF signal path in TX mode. Therefore it is an architecture that is sensitive to the RF/IF signal path mismatches and gain flatness. The Weaver architecture removes the Hilbert transform from the RF/IF signal path by adding another quadrature mixer to the architecture. This relaxes the image-rejection ratio (IRR) challenges as the quadrature generation is shifted to the LO path and does not affect the direct IF/RF signal path.

In addition, the Weaver architecture is symmetric for both RX and TX modes as the quadrature generation occurs at both RF and IF mixers LO paths. Fig. 4.5 shows the proposed image-selection architecture for bidirectional operation. It employs sliding IF architecture using multiplier by four for driving the LO port of RF-mixer and divider by four for driving the LO-port of IF-mixer. By changing the quadrature LO phases of either RF mixer, $4f_{lo}$-drived mixer, or IF mixer, $f_{lo}/4$-derived mixer, the upper and lower band can be selected. Since the $f_{lo}/4$-derived mixer operates at lower frequency, implementing phase inverter at this path save the overall DC power consumption of the system.

By this sliding-IF architecture, the required tuning range of the local oscillator is less than 1 GHz centered at 19.625 GHz, which gives the $4f_{lo}$ centered at 78.5 GHz within bandwidth from 77 to 80 GHz and $f_{lo}/4$ frequency detuning between 4.5 to 5 GHz. The first RF mixer in down-conversion path, RX mode, move the RF frequency band to the center of 4.5 GHz within 3 GHz bandwidth which is also the operation bandwidth of the bandpass filter. The bandpass filter filter out the other unwanted mixing product such as the 15 GHz mixing product from IF mixer in TX mode. The second down-converter mix the first IF, f_{IF1} , with the $f_{lo}/4$, and move the signal to the second IF as $f_{IF1} \pm f_{lo}/4$. This gives the second IF to low IF or 10 GHz-centered frequency. To remove the interference

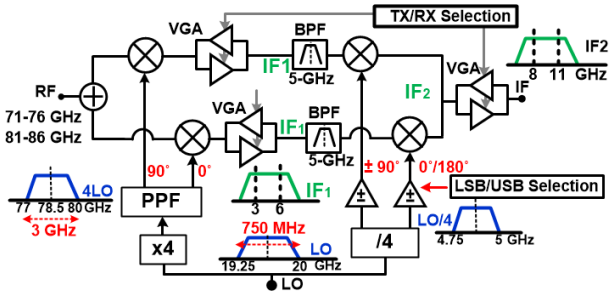


Figure 4.5: The proposed bidirectional 71-86 GHz image-selection transceiver uses sliding-IF Weaver architecture with phase selector in $f_{lo}/4$-path to select the USB and LSB signals.

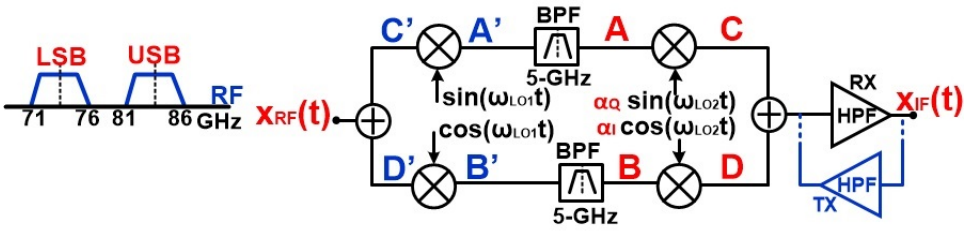


Figure 4.6: Analytical model of proposed E-band image-selection architecture.

with the other microwave bands such as 2.4 or 5 GHz, the 10 GHz-centered one is buffer by using a high pass filter.

To explain the principle operation of the image-selection system analytically, first the system in RX-mode considered. Fig. 4.6 shows the conceptual model of the proposed system, where the ω_{LO1} and ω_{LO2} represents the first and second mixer's LO frequencies and α_I and α_Q represents the phase inverter function. For RX mode, the input signal, $x_{RF}(t)$ can be represented as:

$$x_{RF}(t) = A_{UB}cos(\omega_{UB}t) + A_{LB}cos(\omega_{LB}t) \tag{4.10}$$

Where A_{UB}, ω_{UB}, A_{LB}, and ω_{LB}, are the amplitude and angular frequency of upper band (UB) and lower band (LB) of the input signal, respectively. Multiplying the input received signal, $x_{RF}(t)$, by the LO quadrature phases and filtering the high-frequency components, the signals at points A and B are:

$$x_A(t) = -\frac{A_{UB}}{2} sin((\omega_{UB} - \omega_{LO1})t) + \frac{A_{LB}}{2} sin((\omega_{LO1} - \omega_{LB})t) \tag{4.11}$$

$$= -\frac{A_{UB}}{2} sin(\omega_{IF1}t) + \frac{A_{LB}}{2} sin(\omega_{IF1}t) \tag{4.12}$$

Where $\omega_{UB} > \omega_{LO1} > \omega_{LB}$, therefore the first IF frequency, ω_{IF1}, equals to $\omega_{UB} - \omega_{LO1} = \omega_{LO1} - \omega_{LB}$. For simplification, a unity amplitude of LO is assumed. The signal at point B is:

$$x_B(t) = \frac{A_{UB}}{2} cos((\omega_{IF1})t) + \frac{A_{LB}}{2} cos((\omega_{IF1})t) \tag{4.13}$$

After performing the second quadrature mixing function, the signals at points C, and D are expressed as:

$$\begin{aligned} x_C(t) = &- \alpha_Q \frac{A_{UB}}{4} cos((\omega_{UB} - \omega_{LO1} - \omega_{LO2})t) \\ &+ \alpha_Q \frac{A_{LB}}{4} cos((\omega_{LO1} - \omega_{LB} - \omega_{LO2})t) \\ &+ \alpha_Q \frac{A_{UB}}{4} cos((\omega_{UB} - \omega_{LO1} + \omega_{LO2})t) \\ &- \alpha_Q \frac{A_{LB}}{4} cos((\omega_{LO1} - \omega_{LB} + \omega_{LO2})t) \end{aligned} \tag{4.14}$$

$$\begin{aligned} x_D(t) = &\alpha_I \frac{A_{UB}}{4} cos((\omega_{UB} - \omega_{LO1} - \omega_{LO2})t) - \alpha_I \frac{A_{LB}}{4} cos((\omega_{LO1} - \omega_{LB} - \omega_{LO2})t) \\ &+ \alpha_I \frac{A_{UB}}{4} cos((\omega_{UB} - \omega_{LO1} + \omega_{LO2})t) \\ &+ \alpha_I \frac{A_{LB}}{4} cos((\omega_{LO1} - \omega_{LB} + \omega_{LO2})t) \end{aligned} \tag{4.15}$$

The signals at points C and D are summed and passed through to the high-pass filter:

$$\begin{aligned} x_{IF}(t) = &(\alpha_I + \alpha_Q) \frac{A_{UB}}{4} cos((\omega_{UB} - \omega_{LO1} + \omega_{LO2})t) \\ &+ (\alpha_I - \alpha_Q) \frac{A_{LB}}{4} cos((\omega_{LB} - \omega_{LO1} - \omega_{LO2})t) \end{aligned} \tag{4.16}$$

The phase inverting function at the $f_{lo}/4$ - LO path, α_I and α_Q, can change between +1 and -1. Therefore based on the phase of the I and Q signals, α_I and α_Q, the upper or lower bands can be selected as:

$$\begin{cases} \alpha_I = \alpha_Q \ \ (USB - sel) \Rightarrow x_{IF}(t) = \frac{A_{UB}}{2} cos((\omega_{UB} - \omega_{LO1} + \omega_{LO2})t) \\ \alpha_I = -\alpha_Q (LSB - sel) \Rightarrow x_{IF}(t) = -\frac{A_{LB}}{2} cos((\omega_{LB} - \omega_{LO1} - \omega_{LO2})t) \end{cases} \tag{4.17}$$

Where ω_{IF2} centered around 10 GHz can span:

$$\omega_{IF2} = \omega_{UB} - \omega_{LO1} + \omega_{LO2} = \omega_{LO1} + \omega_{LO2} - \omega_{LB} \tag{4.18}$$

Another main challenges of the Weaver architecture which is particular for the receive mode is the secondary image problem. This problem originates when a interfere component is located at $2\omega_{LO2} - \omega_{RF} + 2\omega_{LO1}$ at the input of the receiver. This component will down-convert to $2\omega_{LO2} - \omega_{RF} + \omega_{LO1}$ after the first RF down-conversion while the in-band input signal down-convert to $\omega_{RF} - \omega_{LO1}$. As a results, these two signals are image to each other with respect to the LO signal of the second mixer, ω_{LO2}. This secondary image and the main signal will down-convert to the same IF_2 frequency, $\omega_{LO2} - \omega_{RF} + \omega_{LO1}$, after the second down conversion. Using the band-pass filter centered at 5 GHz between the two mixers remove this images problem.

Based on the analytical model of the system depicted in Fig. 4.6 for TX-mode, the input signal at IF can be represented as:

$$x_{IF}(t) = \ A_{IF}\, cos(\omega_{IF2} t) \tag{4.19}$$

Where A_{IF} and ω_{IF2} are the amplitude and angular frequency of the transmitted signal at IF frequency which is amplified through the 10 GHz high-pass filter. This high-pass filter also rejects the image of the input signal located at the $f_{lo}/2 - \omega_{IF2}$, which is at low-IF region. After the first quadrature mixing in TX mode, the signals

at points A' and B' can be written as:

$$x_{A'}(t) = -\alpha_Q \frac{A_{IF}}{2} sin((\omega_{IF2} - \omega_{LO2})t) + \alpha_Q \frac{A_{IF}}{2} sin((\omega_{IF2} + \omega_{LO2})t) \quad (4.20)$$

$$x_{B'}(t) = \alpha_I \frac{A_{IF}}{2} cos((\omega_{IF2} - \omega_{LO2})t) + \alpha_I \frac{A_{IF}}{2} cos((\omega_{IF2} + \omega_{LO2})t) \quad (4.21)$$

The second terms of the above equations containing $\omega_{IF2}+\omega_{LO2}$ mixing products. This product will be filtered out by the band-pass filter between the mixers centered at 5 GHz . The band-pass filter which is bidirectional is a RLC filter centered at $\omega_{IF2} - \omega_{LO2}$. After the second quadrature mixing operation, the signals at points C' and D', can be expressed as:

$$\begin{aligned} x_{C'}(t) = &-\alpha_Q \frac{A_{IF}}{4} cos((\omega_{IF2} - \omega_{LO2} - \omega_{LO1})t) \\ &+ \alpha_Q \frac{A_{IF}}{4} cos((\omega_{IF2} - \omega_{LO2} + \omega_{LO1})t) \end{aligned} \quad (4.22)$$

$$x_{D'}(t) = \alpha_I \frac{A_{IF}}{4} cos((\omega_{IF2} - \omega_{LO2} - \omega_{LO1})t) + \alpha_I \frac{A_{IF}}{4} cos((\omega_{IF2} - \omega_{LO2} + \omega_{LO1})t) \quad (4.23)$$

Adding the two signals will give the output signal at RF as:

$$\begin{aligned} x_{RF}(t) = &(\alpha_I + \alpha_Q) \frac{A_{IF}}{4} cos((\omega_{IF2} - \omega_{LO2} + \omega_{LO1})t) \\ &+ (\alpha_Q - \alpha_I) \frac{A_{IF}}{4} cos((\omega_{IF2} - \omega_{LO2} - \omega_{LO1})t) \end{aligned} \quad (4.24)$$

According to (4.18) the first term of RF signal contains the ω_{UB} and the second them contains the lower band frequency, ω_{LB}. Similar to the RX-mode analysis, based on the sign of the phase inverter of f_{lo}/4-path, the IF signal will

move to the upper or lower band as:

$$\begin{cases} \alpha_I = \alpha_Q \ \ (USB - sel) \Rightarrow x_{RF}(t) = \frac{A_{IF}}{2} cos((\omega_{IF2} - \omega_{LO2} + \omega_{LO1})t) \\ \alpha_I = -\alpha_Q (LSB - sel) \Rightarrow x_{IF}(t) = -\frac{A_{LB}}{2} cos((\omega_{IF2} - \omega_{LO2} - \omega_{LO1})t) \end{cases} \tag{4.25}$$

where the relations of ω_{UB} and ω_{LB} with the ω_{IF2} ,ω_{LO2}, and ω_{LO1} are expressed in (4.18).

Note in both the RX and TX modes, the image selection depends on the gain in the I and Q paths being equalized according to

$$IRR = \left| \frac{\Delta\alpha + \alpha_I + \alpha_Q}{\Delta\alpha + \alpha_I - \alpha_Q} \right| \approx \left| \frac{2\alpha}{\Delta\alpha} \right|. \tag{4.26}$$

The IRR will be shown to be improved with a VGA in the I and Q signal paths.

4.2.2 Multi-element Architecture Extension

The proposed image selection architecture can extended to multi-element systems such as multiple input multiple output (MIMO) or phased array systems. Fig. 4.7 a) illustrates the block diagram for a 4-element system incorporating image-selection architecture. The system can employ an IF path or LO-path phased shifting techniques With a single LO port centered at 19.625 GHz with less than 1 GHz tuning range. The IF signal is located between 9-11 GHz routed to each element will make the the implementation of IF or LO phase shifter feasible. For instance, each channel can have an injection-locked oscillator (ILO) phase shifter that locks from the LO port injection. The low tuning range requirement of LO will relax the local oscillator design as explained in chapter 2 and 3.

However, using two lossy passive mixer in each elements requires more power consumption to achieve the desired conversion gain for transmitter/receiver. The system is revised as shown in 4.7 b) to share the second conversion quadrature mixer between the elements. The detailed block diagram of image-selection for a multi-channel system shown in 4.7 b). Each element has a $4\,f_{LO}-$derived quadra-

ture mixer and passive mixer needed for have bidirectional operation.

The bidirectional variable gain amplifiers, A_1, are used in each elements to compensate both amplitude mismatch of I and Q path and the mixer pass loss and improve the IRR according to 4.26. The bidirectional operation of the VGA is enabled by a biasing circuit of one VGA while disabling the complementary VGA. The IF signals are at ω_{IF1} and are combined/split in RX/TX mode to each other to share the second down/up conversion quadrature mixer and its bandpass filter in the image-selection block. Since ω_{IF1} is between 3-6 GHz and the wavelength of the signal is larger than the chip size, the associated routing loss and the I/Q mismatches of IF_1 through the chip are negligible. The active combiner/ splitter used in image-selection block to interface between the $f_{LO}/4$ quadrature mixer with other elements and their associated parasitics. In addition, they provide additional gain to the transmit/receive path. The RLC bandpass filter is bidirectional and shared between the combiner/splitter to filter out the unwanted mixing spurs and provide matching between the combiner/splitter and the $f_{LO}/4$ quadrature mixer. The high pass filter, A_1, also employed to both provide further variable gain to the system while matching the system IF port. The equivalent block diagram of each channel in TX and RX mode with their correspondence linearity and conversion gain requirements are illustrated in 4.8 a) and b). Both A1 and A2 amplifiers have stringent requirements for linearity in TX and RX mode, respectively.

4.3 Bidirectional Circuit implementation

4.3.1 Passive Mixer and VGA

The block diagram of E-band front-end of each element is shown in Fig. 4.9 a). The quadrature mixer composed of double-balanced passive mixer where each of them consists of four n-MOS transistors in a ring configurations. The double-balanced structure has the advantage of low RF to LO leakage and low even-order harmonic distortion. The passive mixers are inherently bidirectional and therefore suitable for the bidirectional operation of the transceiver. Despite that, they could suffer from the trade-offs between conversion loss and isolation between RF, LO

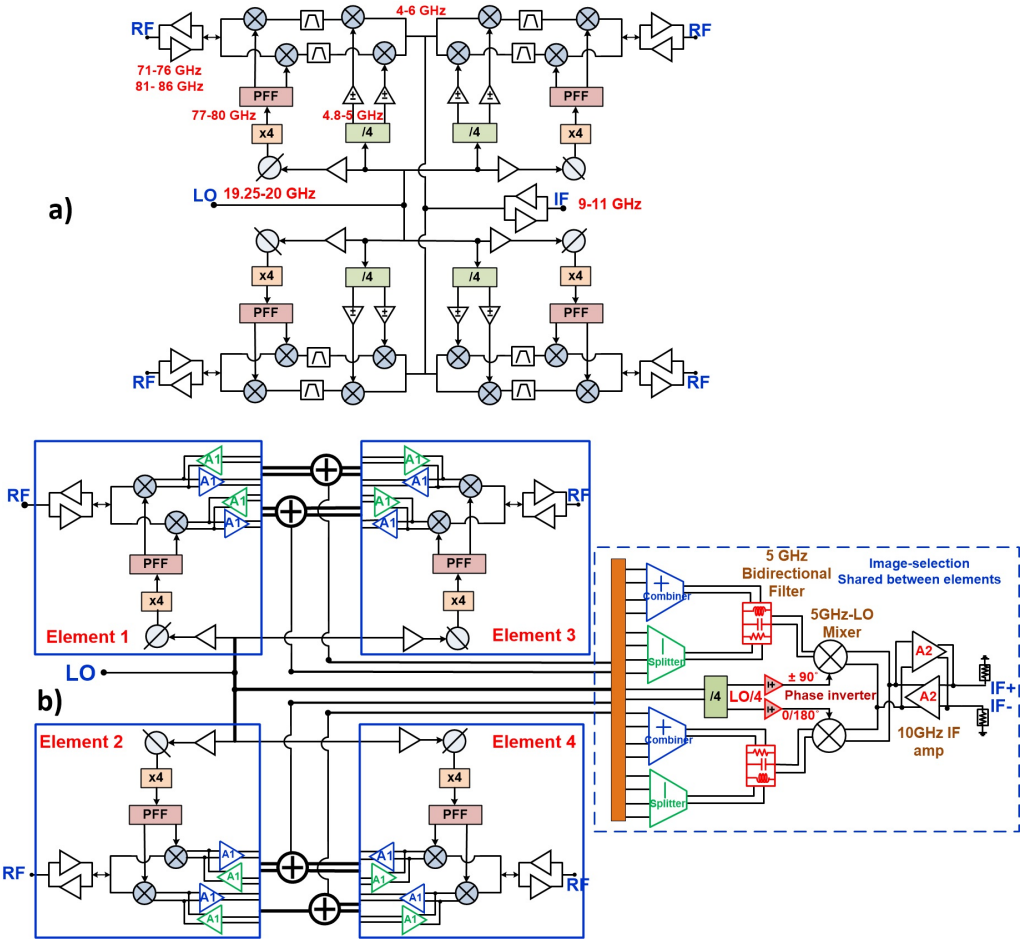


Figure 4.7: Image-selection implementation on multi-element system, a) image-selection block used in each single channel, b) image selection block shared between elements.

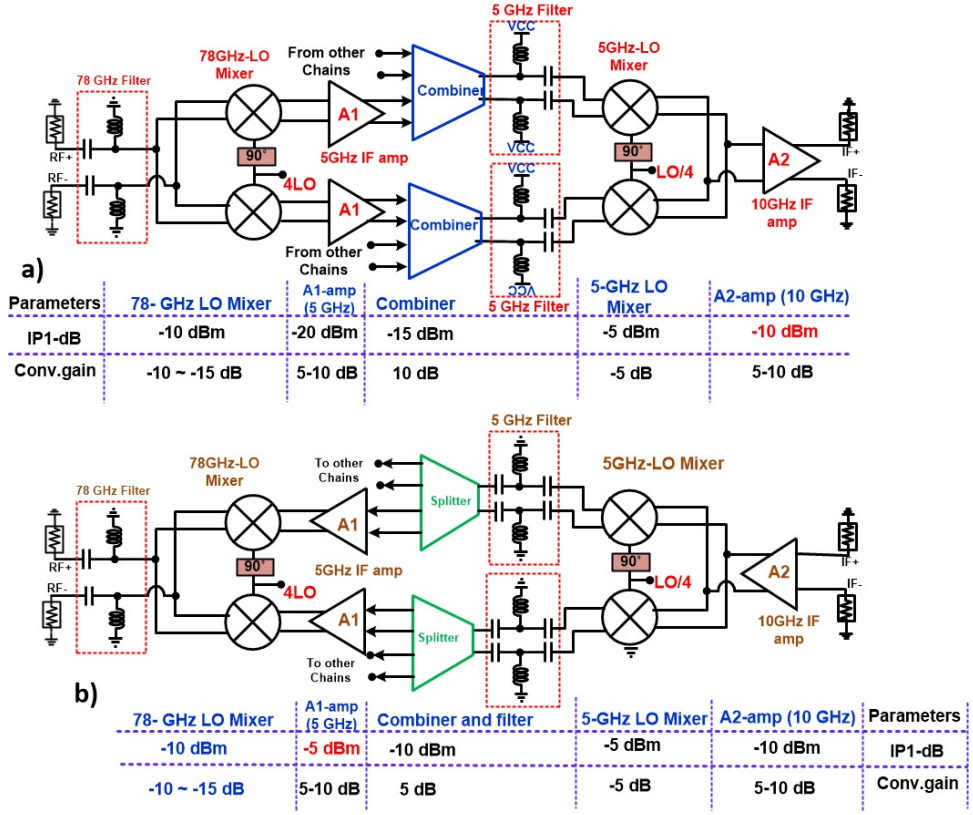


Figure 4.8: Equivalent block diagram of transceiver for one channel, a) RX mode, b) TX-mode.

and IF ports. As the transistors are switching on/off with the period of LO, choosing larger sizes of transistors improves the conversion loss while reducing the isolation between the ports. Therefore, the size of transistors designed with the width of $40\mu m$ ($16 \times 2.5\mu m$) equivalent to $R_{on} = 12.5\,\Omega$, and the minimum length of $100\,nm$. The gate of transistors are also biased with 0.6-V DC voltage through the $10\,k\Omega$ resistors to provide minimum conversion loss. The IF port of mixers are also shunted with $15\,k\Omega$ resistors to prevent floating nodes.

The bidirectional VGAs at IF ports are also shown in Fig. 4.9b). The amplifier is using Heterojunction bipolar transistors (HBT) with emitter degeneration configuration for obtaining better linearity. Since the HBT transistor provides high transconductance, g_m, the emitter degeneration resistor improves the linearity proportional to $(1 + g_m R_E)^{3/2}$. The HBT transistor length are $8\mu m$ with the average collector current of $4\,mA$ from $2\,V$ supply voltage. To acquire the variable DC current, the current source of the amplifier, $M_1 - Q_3$, varies from $150\,\mu A$ to $1.2\,mA$ by using 3-bit switching current mirror transistors. This current amplified by 10 through the MOSFET current mirror, $M_1 - M_2$. MOSFET current mirror is chosen to prevent the DC base current dissipation inherent in HBT transistors. In addition to variable current biasing, there is also a series TX/RX enabling switch in the current source branch of $M_1 - Q_3$ to enable ON/OFF the current mirror based on the operation mode of transceiver. As shown in 4.9a), the output of the amplifier in TX mode is connected to the input of amplifier in RX mode and vice versa. In each mode of operation, while the desired mode amplifier's biasing is ON, the complementary amplifier's biasing becomes OFF. When each of the amplifier get disabled, they should provide high impedance at the interface node with the other amplifier. The load of the VGA is resistive as it operates at low IF frequency, 5 GHz. For example, In RX mode, while the VGA of TX amplifier is OFF, its correspondence load resistors, R_L, with a series capacitance, C_s, create a shunt path to the input of RX-VGA. This changes the matching impedance condition at the IF and RF ports of the quadrature mixer. To reduce the loading effect and the matching variation in each mode, the R_L value of $230\,\Omega$ is chosen. In addition, the load resistor should be chosen such a way that guarantee the linear operation

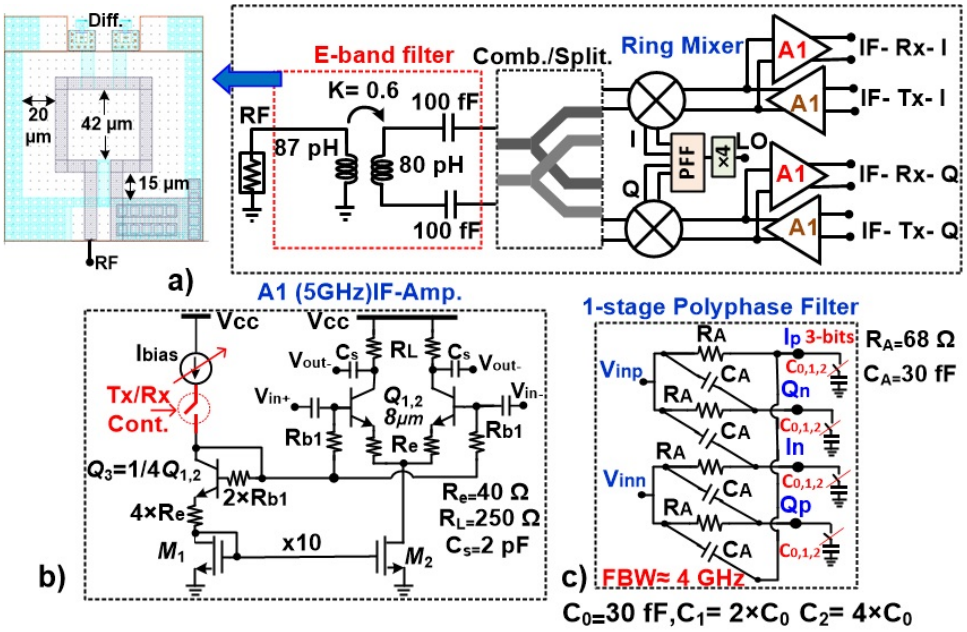


Figure 4.9: E-band front-end for each element a) block diagram, b) 5-GHz IF VGA, c) the LO one-stage PPF is trimmed with 3-bit switched capacitor bank.

regime within the variable gain range. Using the 230 ohm value for R_L will set the output DC voltage of the amplifier and consequently the linear voltage swing ranges in the minimum and maximum gain states. With the degeneration resistor, R_e, of 40 Ω, the Spectre simulation predicts 5.5 -10 dB variable gain with 7 dB power gain within 13 GHz 3-dB bandwidth. The simulated input P_{1-dB} is around 7 dBm in the maximum gain state. This desired input P_{1-dB} and variable gain are compatible with the expected gain and linearity requirements of each block shown in Fig. 4.8, where the linearity of TX-mode VGA is stringent. This amplifier are also used to compensate the I/Q amplitude imbalances. The 3-bit switchable current-biasing provides the minimum gain resolution of 0.2 to 0.5 dB.

Two quadrature mixers are connected at the RF ports in TX mode with a simple T-junction layout. The input impedance at IF ports matches this impedance to 50 ohm at the single RF port. The quadrature LO phases of the mixer have square-shaped signals with 25% duty cycle. This assumption is valid under large swing of LO, where the rise time is negligible. Under this assumption, the impedance at the RF-port of quadrature mixer is approximated as [68]:

$$Z_{in}(\omega) = \quad R_{SW} + \tfrac{2}{\pi^2} Z_{IF}(\omega - \omega_{IF}) \tag{4.27}$$

where R_{SW} and Z_{IF} are the mixer's switch impedance and Z_{IF} is the impedance seen from the IF port of mixer at ω_{IF}. Given these impedance values, the input impedance at RF port according to (4.27) is $(7.5 - j3.5)\Omega$ at 78.5 GHz. A differential to single-ended balun with series capacitance is used for matching as shown in Fig. 4.9a). The series capacitance of 100 fF with the shunt inductance of 80 pH will move the low impedance of quadrature mixer's RF port to 100 ohm differential output. The 100 fF capacitance employs the MIM capacitor for high density layout to minimize routing and parasitic inductance. The differential port of the inductance uses the second top metal layer of the technology with the width of $7\,\mu m$, thickness of $3\,\mu m$, and $1.25\,\mu m$ vertical spacing between the top and second top metal layers. The single-ended coil uses the $4\,\mu m$ thickness top aluminum layer, LD, with the width of $7\,\mu m$ and inner dimension of $42\,\mu m$. The EM simulation predicts the inductance of 87 pH at 78.5 GHz and the mutual coupling of 0.6 between the primary and secondary coils. Also, the EM simulation indicates the overall RF balun loss below 1 dB with the gain imbalance of 0.65 dB and phase imbalance of 5.4°at 78.5 GHz.

The simulated RF-port matching, S_{11}, is plotted in Fig. 4.10 a) and is below -15 dB S_{11} over 10 GHz bandwidth of E-band. The simulated S-parameters at quadrature IF ports of mixer are also illustrated in Fig. 4.10 b). TThe IF port matching is below -10 dB. The large signal simulation shows 12.5 dB conversion loss and input P_{1dB} larger than 0 dBm of the whole E-band front-end block. The simulation performed on the circuit from the IF port of mixer including VGAs to the single-ended 50 ohm matched RF port.

4.3.2 Multiply by 4 Quadrature Frequency Generation

The LO generation circuit block diagram of each element is shown in Fig. 4.11. It acquires the same topology for multiplier by four frequency generation as

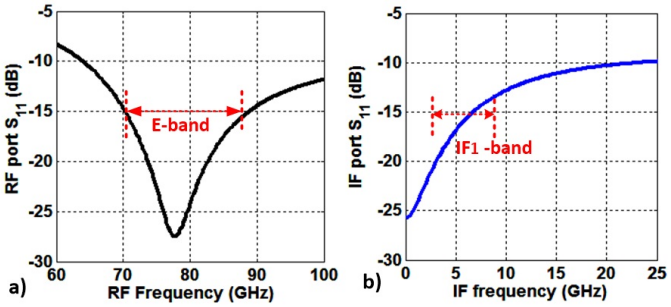


Figure 4.10: Simulation of E-band front-end matching, a) RF-port, b) IF-port.

described in chapter. 3. The first stage is the LC tuned load amplifier centered at 19.5 GHz. This amplifier provides enough swing to compensate the 9 dB loss of the following RC PPF. The PPF employs one-stage PPF as the tuning range of the LO is below 1 GHz. The center frequency, 19.5 GHz, defines the resistance and capacitance value equal to 88Ω and $92.6\,fF$, respectively. This PPF generates the quadrature waveforms to drive the trans-conductance devices of quadrupler, $Q_1 - Q_4$. The four common-emitter transconductance are $4\,\mu m$ long and combined in their collector output to generate the 4th harmonic. The output of the quadrupler is buffered to the $10\,\mu m$ long common-base amplifier, Q_5, consuming 4 mA current from 2-V supply voltage. The quadrupler provides single-ended output with 1-dB gain. To increase the power gain and provide differential signal, an additional common-emitter amplifier is used, employing a single-ended to differential balun as a load. The differential signals are needed to drive the PPF centered at $4 \times f_{LO}$, 78.5 GHz. The common-emitter transistor, Q_6, has the length of $8\,\mu m$ and biased with 8 mA current. The inter-stage matching between the quadrupler's output and the buffer's input , Q_6, is also depicted in Fig. 4.11, consisting of a series and shunt inductance with the length of $105\,\mu m$ and $85\,\mu m$. The balun designed for matching the input PPF uses the top metal layer with the width of $7\,\mu m$ and inner dimension of $42\,\mu m \times 42\,\mu m$ for the single coil. The differential coil has the same size and width but uses the second top metal layer with the series capacitance of 90 fF. This buffer, Q_6, and its load provides 8 dB gain at 78.5 GHz.

The one-stage PPF used for quadrature generation at the $4 \times f_{LO}$ utilizes the resistance and capacitance values of 65 ohm and 30 fF, respectively. To minimize

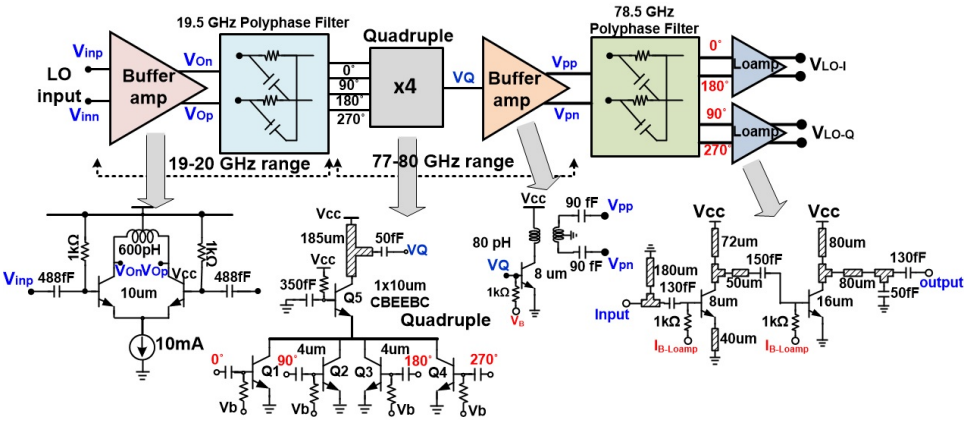


Figure 4.11: Multiplier by four circuitry generation

the I/Q imbalance originated from the layout and process variations, ΔR and ΔC, each resistors are constructed by three parallel resistors and each capacitor is constructed by two series resistors [69], Fig. 4.12 shows this layout configuration technique. Acquiring larger elements reduces process variations and in consequence improve the circuit tolerance to the mismatches. Moreover, dummy resistors and capacitors surrounds the PPF layout cell. The RC extraction for the cells and EM simulations for the routing of PPF show $\pm 5°$ phase imbalance and ± 1.5 dB amplitude imbalance at 78.5 GHz. This value corresponds to IRR less than 20 dB. To improve the IRR and the amplitude and phase calibration, 3 bits switchable n-cap varactor are employed at each positive and negative I and Q signal path, Fig 4.12 illustrates this. The n-cap varactor has the width of $3\,\mu m$ and length of $0.5\,\mu m$, providing minimum capacitance of 10 fF for $V_{GS} = 0\,V$ and maximum capacitance of 30 fF for $V_{GS} = 1.5\,V$. The simulation results clarifies that the 3-bit calibration circuit can offer $\pm 4°$ phase tuning with $\pm 0.25°$ phase resolution and less than 0.25 dB to 0.5 dB amplitude mismatch. The PPF and the calibration circuit has around 10 dB loss within operational bandwidth.

The differential output signal of PPF are amplified by two-stage amplifiers to increase the power gain and the resulting conversion gain of the mixer. The minimum required LO power for saturating the mixer conversion gain is 5 dBm. The first and second stage amplifier consist of HBT transistors with the length of $8\,\mu m$ and $16\,\mu m$ and biased at 10 mA and 20 mA, respectively. This two stage

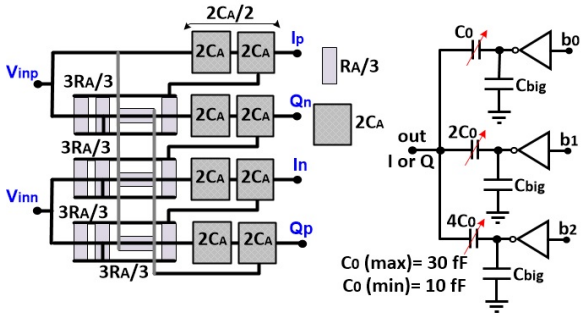


Figure 4.12: $4 \times f_{LO}$ PPF layout and the calibration circuitry.

amplifier provides 15 dB voltage gain.

The simulation results for differential I/Q output signals of the LO-chain illustrates in Fig. 4.13 a) and b) for before and after calibration conditions, respectively. The average peak to peak voltage amplitude is 0.6 volt with 1 dB amplitude mismatch and 5° phase mismatch before calibration. This can be improved to 0.25 dB and 2° amplitude and phase mismatch which required for obtaining an IRR of 30 dB.

4.3.3 Image Selection Circuit

The image selection block is shown in Fig. 4.14 and is shared between elements. The combiner and splitter share the bidirectional bandpass filter (BPF) connected to the $f_{LO}/4$ mixer. The BPF loads the combiner in RX mode while producing an input matching network for the splitter in TX mode. In each mode of operation, the complementary circuit is switched off with the TX/RX mode. For the RX mode, the impedance seen at the $f_{LO}/4$ quadrature mixer creates a low impedance path for the current combiner. For the TX mode, large-signal simulations indicate that differential 100Ω matching is the optimum impedance for both linearity and conversion gain purposes. The BPF centered at 5 GHz, ω_{IF1}, requires to match the combiner output to 100Ω differential at the $f_{LO}/4$ quadrature mixer port, plane A. Simultaneously it should match the input of splitter to the 100Ω differential impedance at this interface node, plane A.

Fig. 4.14 a) shows this bidirectional matching concept. Fig. 4.14 b) and c)

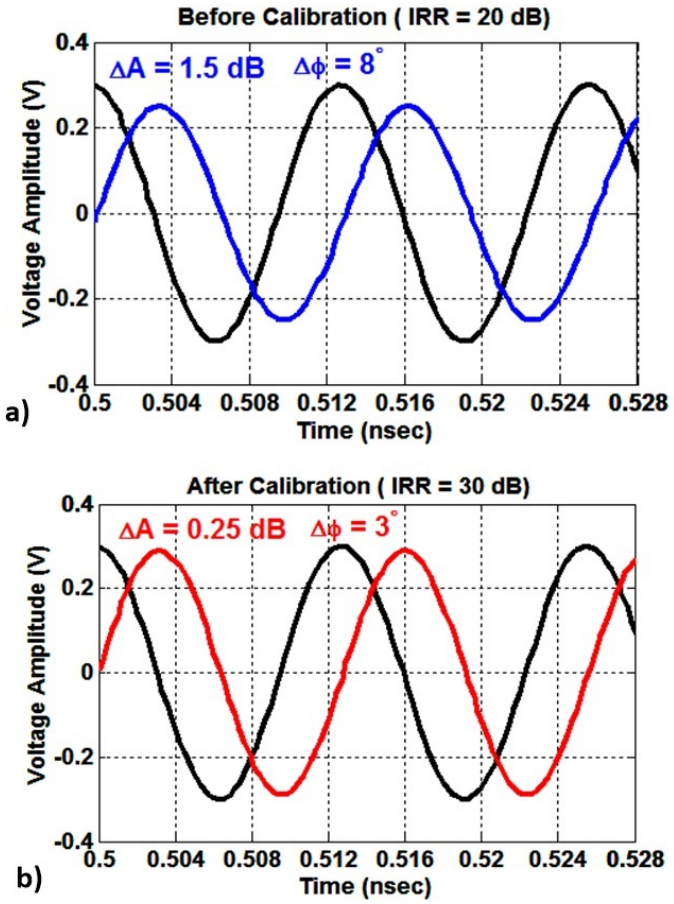


Figure 4.13: $4 \times f_{LO}$ PPF simulation results, a) before I/Q calibration with IRR = 20 dB, b) after I/Q calibration with IRR= 30 dB.

illustrates the combiner and splitter circuit schematic, respectively. The combiner's transconductance transistors, Q_{1-2}, use emitter-degeneration configurations with $4-\mu m$ length. The emitter-degeneration resistance is 70 ohm to improve the linearity of combiner. The transistor, Q_3, amplifying the combined current has the length of $8-\mu m$ and biased at 10 mA wfrom 2-V supply voltage. For the splitter circui, shown in Fig. 4.14 c), the transistor Q_3 divides the current between common-base transistors, Q_{1-2}. These transistor employs 30 ohm emitter degeneration resistance. The Q_{1-2} are $5-\mu m$ long and use resistive load, R_L , of 150 ohm to set the common-mode output DC-voltage to 1.2-V. The splitted current in Q_{1-2} flows to R_L and convert to voltage. The voltage signals routes through the chip to each element as I and Q signals. Since the quadratured routing signals are at 5 GHz, ω_{IF1}, the simulated associate loss is below 2 dB for 1-mm long routing path. The normalized input impedance of splitter is at placed at $0.8-j1.8$ on smith chart while the output impedance of combiner is at $0.8-j0.8$ at 5 GHz. The BPF components value, R, L, and C which are shared is illustrated in Fig. 4.14 d). A series capacitance of 130 fF will move the splitter normalized impedance from $0.8-j1.8$ to the combiner's output impedance at $0.8-j0.8$. Consequently, the remaining elements of BPF can be shared for each mode. Applying the shunt resistance of 450-ohm parallel with single-ended inductance of 3.5 nH move the impedance from $0.8-j0.8$ to $(1+j2.6)$. Employing a series capacitance of 250 fF move this resultant impedance to a single-ended 50 ohm at the mixer interface node, plane A. The inductor used in the BPF has 4-turns utilizing top aluminium-metal layer of the technology. To have the differential inductance of 7 nH, the inductor outside diameter is $300-\mu m$ with the width of $7-\mu m$ and turn space of $5-\mu m$. The simulated S-parameter result for matching at interface node, plane A, is shown in Fig. 4.15 a). The BPF provides better than 10 dB S_{11} for the required 3 GHz bandwidth.The large signal simulation of the bidirectional image selection block is depicted in Fig. 4.15 b) when only one channel is ON. The large signal simulation was performed on the block composed of quadrature mixer, combiner and splitter with their bidirectional BPF matching network. The simulated power gain of TX mode is 3.5 dB with -6.5 dBm input P_{1-dB}, however a 3 dB lower power

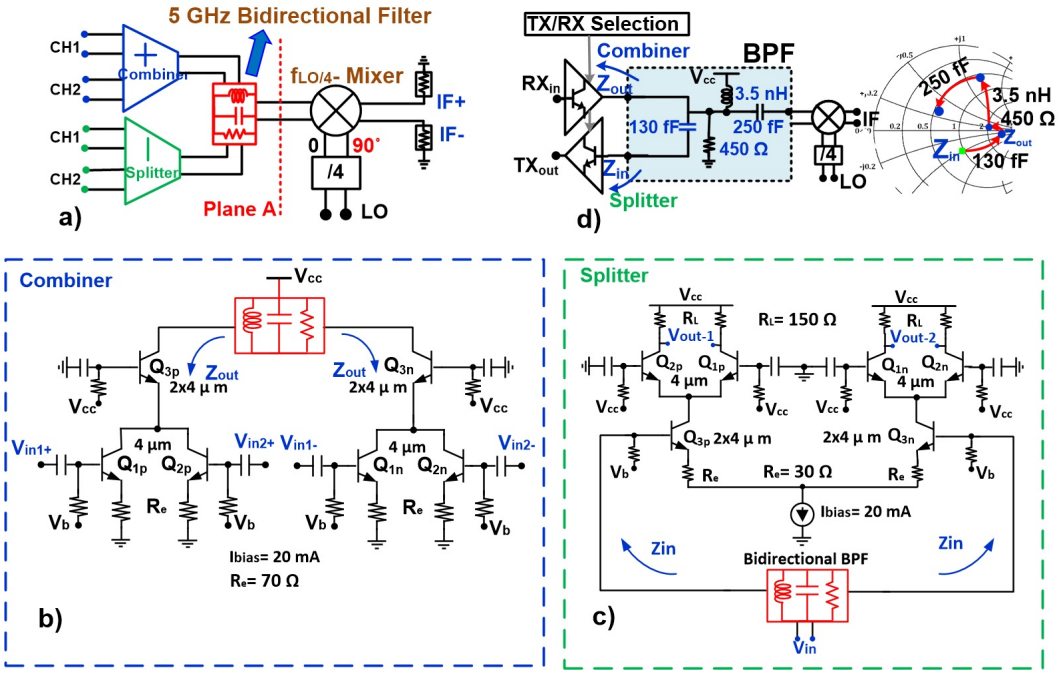


Figure 4.14: Image selection bock, a) shared interface between combiner and splitter, b) combiner circuit, c) splitter circuit, d) bidirectional shared band-pass filter.

gain should be accounted for splitter dividing function. The power gain for combiner is around 7 dB with -5.5 dBm input P_{1-dB}. In the simulations, the passive components, such as capacitors and inducto used in BPF are either extracted or EM simulated.

The $f_{LO}/4$-derived mixer is also passive using n-MOS transistors as a switch in a ring configuration. The size of transistors are $40\,\mu m/100\,nm$. This passive mixer has an average loss of 5 dB over the IF_1 bandwidth. The 10 GHz high pass filter (HPF) is applied after this mixer to further compensate this loss in addition to filter the unwanted image and mixing spurs. Moreover, the HPF provide matching at the IF port of the chip. Fig. 4.16 a) illustrates the bidirectional configuration of the filter with the schematic of each amplifier. The circuit employs the miller-feedback configuration to improve the linearity of circuit in addition to provide a resistive matching at mixer's interface node, plane B. For example for RX mode, to create 100 ohm differential input matching at mixer interface port, plane B, the miller feedback is chosen to $200\,\Omega$. The amplifier itself is a common-emitter HBT

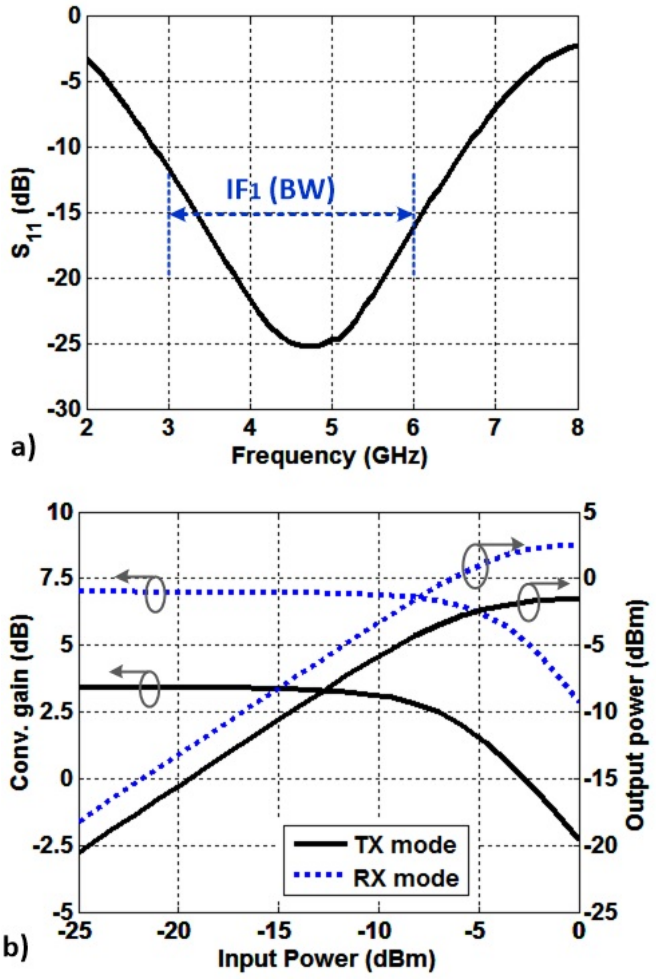


Figure 4.15: Simulation results for image selection block, a) S_{11}, b) Large signal simulation results of image selection block (combiner/splitter and quadrature 5 GHz mixer).

transistor with the width of $4\,\mu m$ and biasing at $650\,\mu A$ with the load resistance of $310\,\Omega$. This values provide 1.8 V DC output voltage and 6 dB voltage gain, A_v. This will result in an input impedance of $66\,\Omega$ at the input of amplifier in RX mode:

$$Z_{in} = \frac{Z_{RF}}{1+A_v} = \frac{200}{1+2} = 66.6\,\Omega \tag{4.28}$$

This equivalent $Z_{in}$of the miller amplifier in RX mode is shunted with the output load, R_L, of the complementary amplifier in TX mode. Having TX load resistance, R_L equals to $200\,\Omega$ provides the mixer impedance at interface node of B as:

$$Z_{in,plane-B} = Z_{in} \parallel R_{L-TX} = 200 \parallel 66.6 = 49.6\,\Omega \tag{4.29}$$

which is the desired 50 ohm single-ended matching. Note that similar to the other bidirectional block of the system, the biasing circuitry of each amplifier are switched ON and OFF based on the TX/RX operation mode. In addition to that, another TX/RX enabling switches are applied in the miller feedback path to prevent loading effect of the miller resistance of the disabled amplifier to the complementary enabled amplifier. The switch size which is also shown in Fig. 4.16 is $W/L = 60\,\mu m/100nm$ to create small ON-resistance of $15\,\Omega$. It is also required to provide large impedance in the OFF state.

This scenario is the same for TX-mode amplifier. To create 50-ohm input impedance at IF port of the chip in addition to the amplification function, the miller feedback resistance is set to $150\,\Omega$ for TX mode. Biasing the amplifier's transistor of $4\,\mu m$ length with 1.3 mA DC current and the R_L of $200\,\Omega$ provides the amplifier's equivalent input miller impedance as:

$$Z_{in} = \frac{Z_{RF}}{1+A_v} = \frac{150}{1+2} = 50\,\Omega \tag{4.30}$$

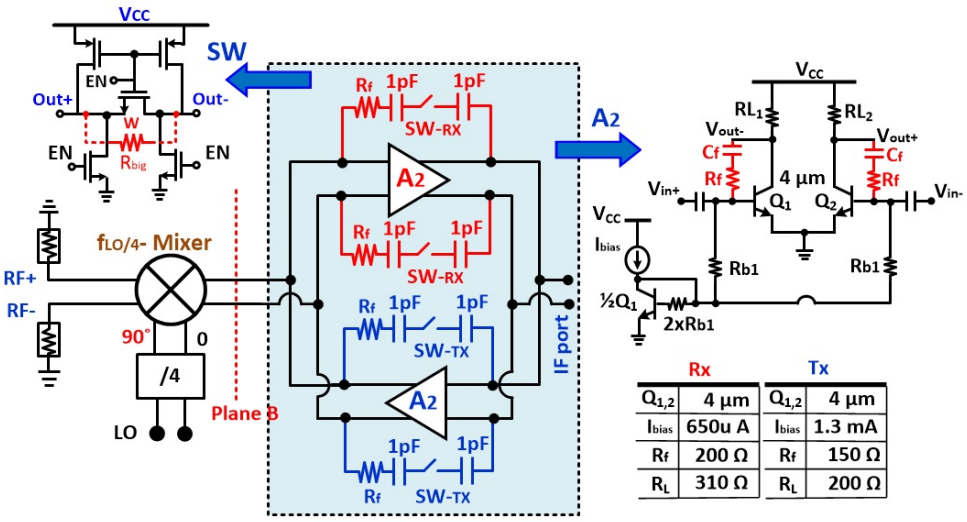


Figure 4.16: a) bidirectional TX and RX configuration of 10 GHz HPF filter with its schematic.

Considering the parallel loading effect of the RX- amplifier, R_L of 310 Ω will reduce this impedance to around 45 Ω. The small signal simulation result for input, S_{11}, of TX amplifier at IF-port and S_{11} of the input of RX-amplifier at mixer interface port, plane B, are demonstrated in 4.17 a). The resistive miller feedback amplifier provides band-pass filter performance with S_{11} better than 10 dB within 3 to 22 GHz bandwidth. The large signal simulation illustrates in Fig. 4.17 c) for each mode of operation. Each amplifier provides an average gain of 6 dB with input $P_{1-dB}$of -8.5 dBm.

The large signal simulation for a whole designed Weaver building block from IF port to LO port is shown in Fig. 4.18 at of 73.5 GHz. For this simulation the VGAs are tuned to provide the same amount of maximum P_{sat} and conversion gain, -2.5 dB, for both TX or RX states. This leads to the same P_{1-dB} value. The input P_{1-dB} of both system is around -10 dBm which is near the expected systematic analysis provided in Fig. 4.8. The simulation results for entire system for one channel versus frequency are demonstrated in Fig. 4.19. By changing the VGA current states from the low to high, the system provides the minimum and maximum gain of -1.6 dB to 4 dB for TX mode and maximum and minimum gain of -3 to 2.5 dB in RX-mode . The conversion gain variation over bandwidth is

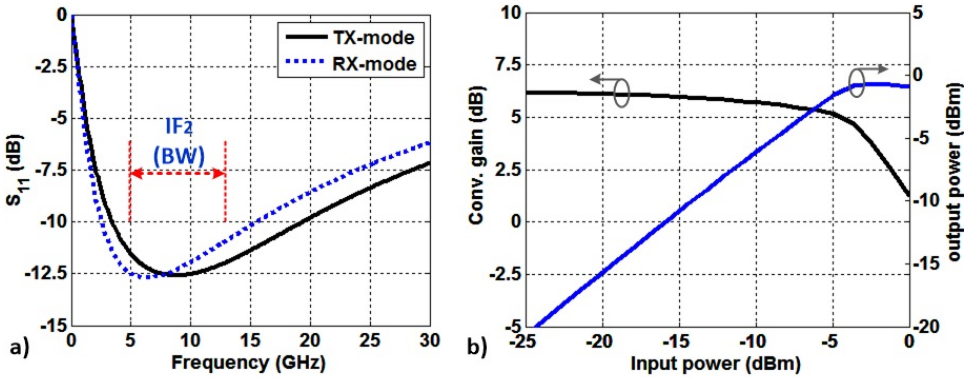


Figure 4.17: Simulation results: a) small signal S-parameter bidirectional simulation, b) bidirectional large signal simulation.

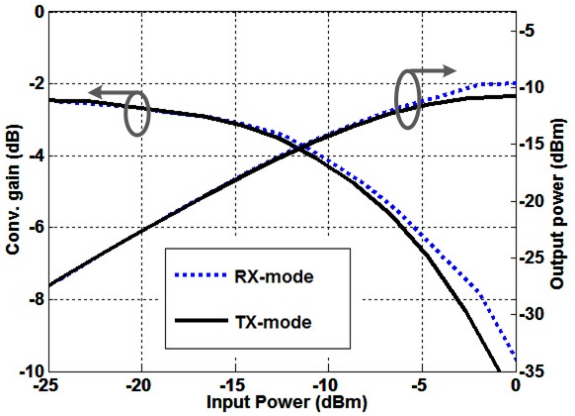


Figure 4.18: Large signal simulation of one channel from IF to RF ports for TX and RX mode.

less than $\pm 0.4\,dB$ in each VGA state. The simulated IRR is also around 29 dB corresponding to 2° phase imbalance and 0.25 dB amplitude imbalance at $4f_{LO}$ quadrature mixer LO-path.

4.3.4 Divider by four and USB/LSB selection block

Fig. 4.20 demonstrates the block diagram of the quadrature LO frequency generation of the second IF up/down converter. The LO generation block consists of divider by four block and phase inverter to select the upper or lower band. The dividing by four circuit is composed of two cascaded divider by two with two input and output buffers operating at 19.5 GHz and 5 GHz, respectively.

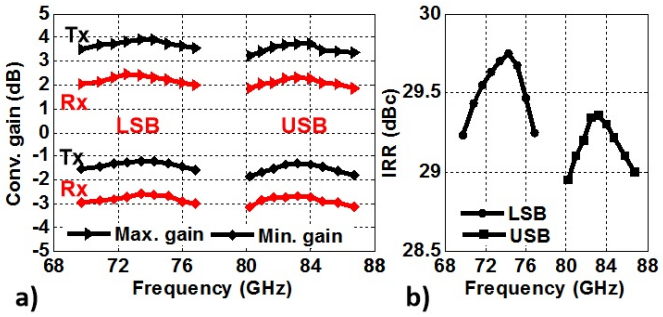


Figure 4.19: Simulation results for entire channel a) conversion gain versus frequency, b) calibrated image-rejection ratio over frequency.

The divider by two is also composed of the D-latch current-mode logic (CML) blocks. Fig. 4.20 illustrates the circuit schematic of the divider by two and the buffers with their component values. The CML divider has moderate swing at the input and output, where the output swing is proportional to $R_D I_{SS}$ equivalent to 300 mV. The amplifier stage transistors, $M_{1D,2D}$, are sized such that avoiding the divider to enter the triode region and ensuring full swing experience. The size of transistors, $M_{3D,4D}$, are chosen to assure enough small-signal gain to exceed the unity for regenerative mode operation. The circuit schematic of the input and output buffers of the divider block is also presented in 4.20. The transistors and component values are designed to set the divider input and output common-mode DC voltages. The input buffer operates at 19.5 GHz and match each element LO port to 50 ohm. Moreover, this buffer provide isolation between the large input capacitance of divider by four and the LO port each element and as a result the LO port of chip. The phase inverter schematic is also depicted in Fig. 4.21 a). The phase inverter is composed of cascode amplifiers with common-emitter transistor length of $8-\mu m$ and common-gate transistor length of $4-\mu m$. The phase of the circuit is enabled by switching the base voltage of four common-gate amplifiers to the ground or V_{cc} . The phase inverter can provide variable gain of 17 dB to 23 dB based on the variable DC current flowing through the current-mirror, $Q_s - M_s$. The variable gain can compensate the I/Q amplitude mismatch and reduce the third-harmonic tone, $3f_{LO}/4$, generated from divider by four path. The third-harmonic tone can produce undesired spurs falling into the IF2 band. For

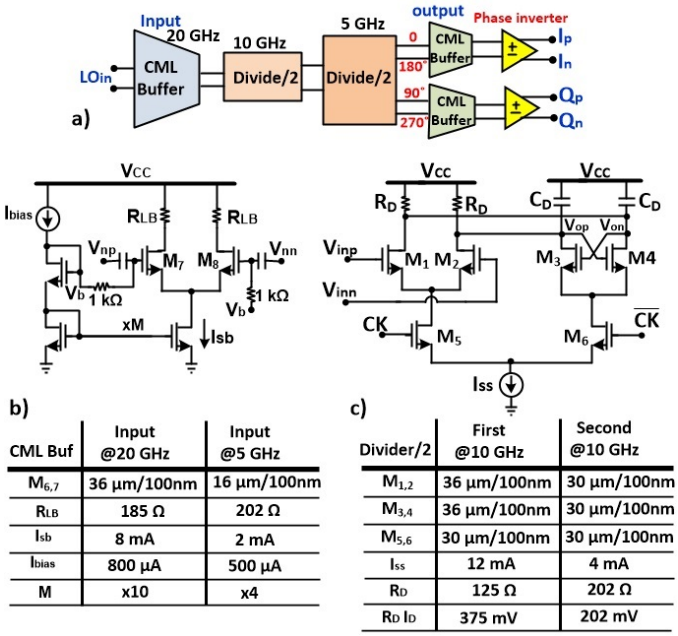
example for a 85 GHz input RF frequency, using 20 GHz LO frequency ($4\,f_{LO} = 80$ GHz, $f_{LO}/4 = 5$ GHz, and $3\,f_{LO}/4$ =15 GHz) will move the mixing spurs products generated from $f_{LO}/4$ and $3f_{LO}/4$ to the same IF_2 frequency as $f_{RF} - 4f_{LO} + f_{LO}/4$ and $f_{RF} - 4f_{LO} - 3f_{LO}/4$ which is 10 GHz. To reduce the 3rd harmonic tone effect, the phase inverter needs to operate in linear region at the expense of lower gain and the resultant transceiver overall conversion gain. Increasing the current of the phase inverter distorts the amplifiers transistor and increased the 3rd harmonic tone. Fig. 4.21 b) shows the output voltage of the phase inverter versus frequency for two collector current biasing of 2 mA and 4 mA. The large signal simulation results for output power and the 3rd harmonic tone output power versus input power is illustrated in 4.21 c). As 4.21 b) and c) illustrates, biasing the transistor with lower current reduce the gain but improve the 3rd harmonic suppression.

The $f_{LO}/4$-derived mixer requires a minimum 0.6 V_{p-p} voltage swing at its LO port for having 5 dB conversion loss. The simulated output quadrature LO signals of the divider by four block is shown in Fig. 4.21 a). The simulation shows 0.65 V_{p-p} output voltage swing for I and Q signals with less than 1 dB amplitude mismatch and 2 degree quadrature phase mismatch. The averaged overall gain of the $f_{LO}/4$ frequency generation block is around 10 dB. The divider sensitivity to the input voltage swing versus frequency is illustrated in Fig. 4.21 b). Fundamentally, the divider circuit should oscillate at $f_{LO}/4$ using minimum input power to be injection-locked. The simulation shows this condition occurs at 19.5 GHz for the designed divider. In other words, to injection-locking the divider within the desired LO bandwidth, 19-20 GHz, it requires below 0.2 V_{p-p} input voltage swing. This corresponds to the simulated 10 dB voltage gain of $f_{LO}/4$ path.

4.4 Measurement results

4.4.1 Assembly

The chip micrograph mounted on a PCB board is shown in Fig. 4.23. The system contains two channels and was implemented in 90-nm SiGe BiCMOS process. Each channel contains a separate 71-86 GHz I/Q mixer, 4×LO quadrature



CML Buf	Input @20 GHz	Input @5 GHz
$M_{6,7}$	36 µm/100nm	16 µm/100nm
R_{LB}	185 Ω	202 Ω
I_{sb}	8 mA	2 mA
I_{bias}	800 µA	500 µA
M	x10	x4

Divider/2	First @10 GHz	Second @10 GHz
$M_{1,2}$	36 µm/100nm	30 µm/100nm
$M_{3,4}$	36 µm/100nm	30 µm/100nm
$M_{5,6}$	30 µm/100nm	30 µm/100nm
I_{ss}	12 mA	4 mA
R_D	125 Ω	202 Ω
$R_D I_D$	375 mV	202 mV

Figure 4.20: Divider by four quadrature frequency generation path, a) block diagram, b) input and out put CML buffer schematic, c) divider by two schematic.

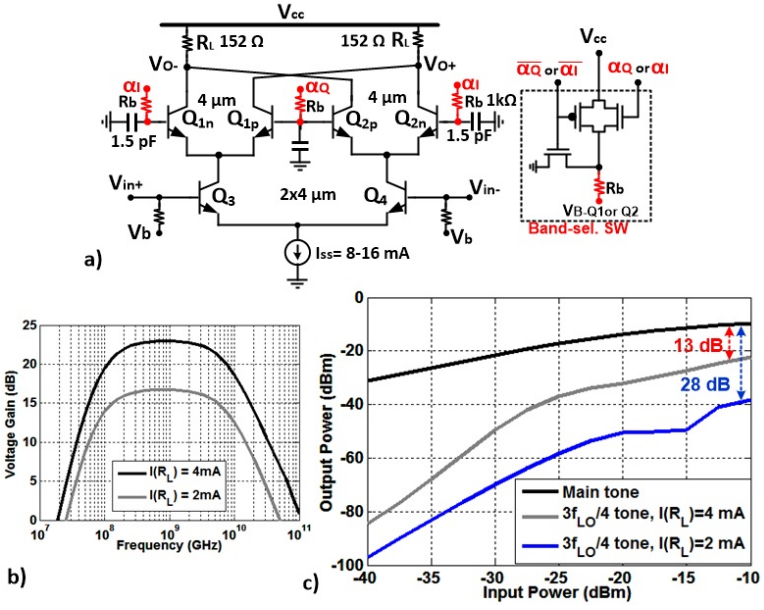


Figure 4.21: a) The USB/LSB selection (phase inverter) schematic, b) ac-simulation results for two biasing conditions c) Large-signal simulations for main tone and third harmonic tones versus input power for two biasing conditions.

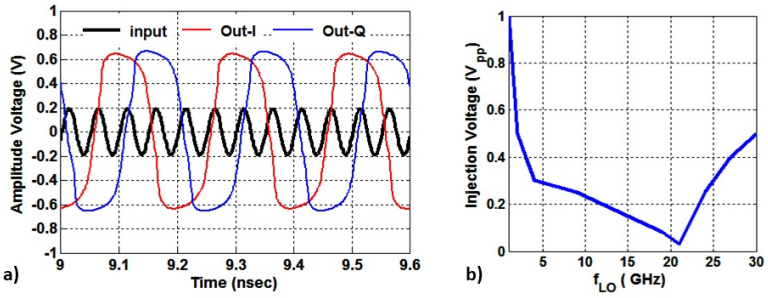


Figure 4.22: Transient time simulation results for divider by four and phase inverter LO-path, a) The output I and Q signals and input differential signal, b) Divider sensitivity.

generation chain, and 5 GHz bidirectional VGAs. The 5-GHz I/Q IF signals of each channel are combined and connected to the 5-GHz BPF and 5-GHz I/Q mixer. The chip occupies $2.1 \times 1.9\,mm^2$ including pads and ESD. The DC pads, LO and IF pads are wire-bonded to the PCB, while the first layer of PCB uses 10 mil thickness Rogers 5880 material for the high-frequency signal routing, i.e, IF (6-11 GHz) and LO (19-20 GHz). As the IF and LO ports of the chip are differential, hybrid baluns are designed on the board with less than 3 dB loss and under 1 dB amplitude imbalance and 8° phase imbalance within 3 GHz bandwidth.

The RF signal chain consumes between 120 and 150 mW for the IF VGAs and 250 mW for the 4×LO and LO/4 circuitry.

4.4.2 TX measurements

To demonstrate the image selection concept, the state of the system is configured for either USB ($\alpha_I\alpha_Q = 00/11$) or LSB ($\alpha_I\alpha_Q = 01/10$) modes. The TX spectrum is plotted in Fig. 4.24 a) and b) for USB and LSB mode, respectively, with phase inversion in the image-selection circuit. The IF and LO signals of chip are located at 9 GHz and 20 GHz, respectively, equivalent to 84 GHz at USB and 76 GHz at LSB bands and $4f_{LO}$ leakage signal at 80 GHz. Using the 87 GHz LO of the down-converted external mixer in measurement set-up will move the USB, LSB and $4f_{LO}$ leakage signals to 3 GHz, 11 GHz and 7 GHz, respectively. The LO leakage and IRR ratio in Fig. 4.24 are around 23 and 25 dB, respectively, without

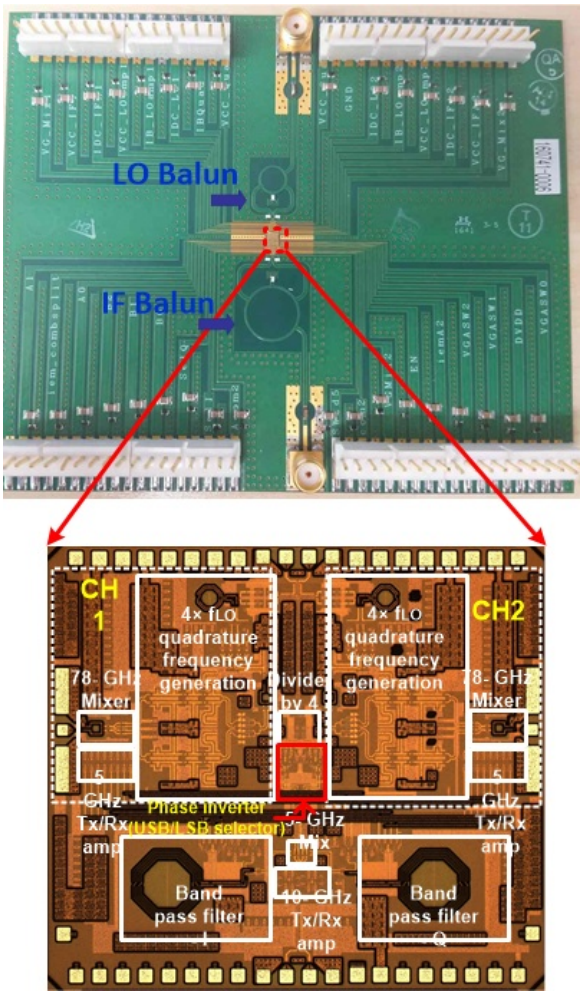


Figure 4.23: The designed board and chip micrograph.

calibration. The output power is also around -15 dBm which is near output P_{1-dB} of transmitter.

Large signal measurements results for continuous wave (CW) source versus input power for the USB-mode and LSB-mode are shown in Fig. 4.25. Fig. 4.25 a) plots the output power of the main signal, image signal and the LO-leakage, while Fig. 4.25 b) plots the main and image signal conversion gain. The conversion gain is plotted in Fig. 4.25 b) is approximately 2.5 dB in both modes and compresses for an input power of around -15 dBm. For this equal conversion gain state, the

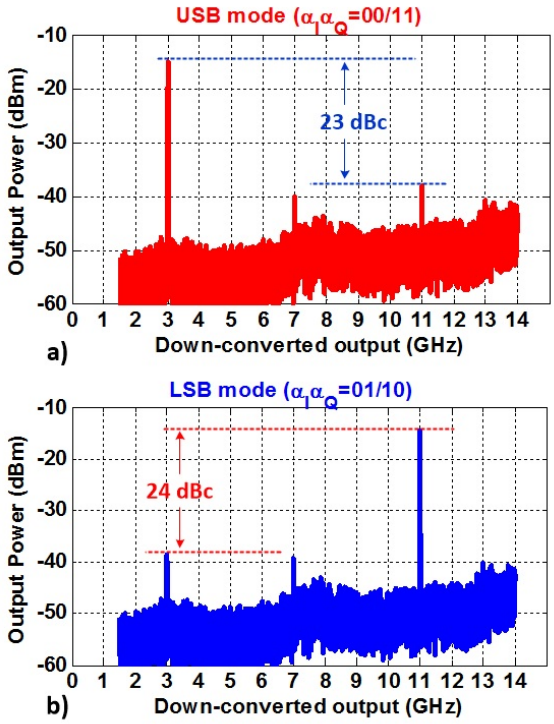


Figure 4.24: Image selection performance for TX, a) USB mode, b) LSB mode with f_{IF} =9 GHz, f_{LO} =20 GHz.

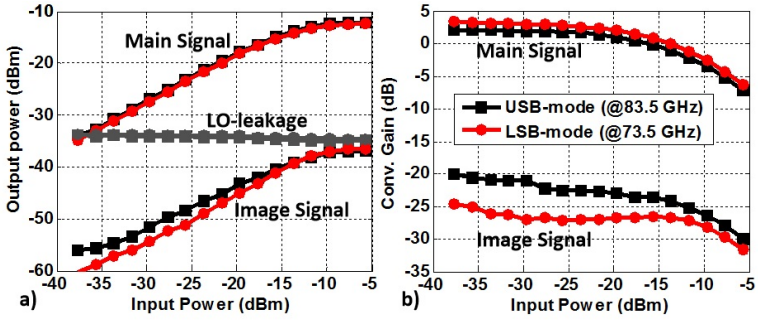


Figure 4.25: Measured TX performance versus input power for 73.5 GHz as LSB and 83.5 GHz as USB, a) main signal and image signal output power and $4f_{LO}$ LO-leakage power. b) main signal and image signal conversion gain.

measurements shows the IRR is 25 dB for the LSB mode and 23 for the USB mode without optimizing the calibration conditions (VGA/PPF). The LO leakage is less than -35 dBm across the power, however, the double-conversion architecture allows the LO leakage to be easily filtered.

The conversion gain variation is measured at the 9-GHz IF signal of the chip while the LO signal varies from 19 GHz to 20 GHz to sweep the LSB from 71.75 GHz- 76 GHz and the USB band from 81 GHz to 84.75 GHz. The large signal performance versus input power, conversion gain and output power are plotted in Fig. 4.26, illustrating the negligible variation of output result ($<$1 dB).

Fig. 4.27 a) and b) show respectively the output conversion gain and power versus input power under two maximum and minimum gain conditions of the VGAs. The VGA provides gain variation of TX front-end from -2.25 dB to 3 dB with the input P_{1-dB} from -13.5 dBm to -17.5 dBm. The maximum saturated output power that the front-end provides under these two extreme conditions varies from -16 dBm to -12 dBm.

The output performance of the transmitter versus frequency for the two extreme VGA states are presented in Fig. 4.28. The conversion gains across the LSB and USB bands are plotted in Fig. 4.28 a) and compared with simulation results from Fig. 4.19. The gain variation in the LSB mode is less than $\pm$0.4 dB at the minimum and maximum VGA states while the gain variation is $\pm$0.5 dB in the USB band for each of these VGA states. The conversion gain variation over the entire 71-86 GHz band is around $\pm$0.75 dB. Fig. 4.28 b) illustrates the input P_{1-dB} variation over frequencies for the USB and LSB modes of the two VGA states. The P_{1-dB} values over the entire USB and LSB band vary less than $\pm$0.75 for max. VGA state and less than $\pm$1 dB for min. VGA state. The saturated output power of the TX front-end varies from the minimum of -16 dBm to the maximum of -12 dB, Fig.4.28 c) shows this. The variation of P_{sat} of entire band is approximately less than $\pm$0.6 dB for the both max. and min. states of VGA.

The IRR for both USB and LSB modes are plotted over the frequency band in Fig. 4.29 a) for the before and after optimum calibration conditions. Before using the 3-bit VGA and PPF calibration, the IRR at 73 GHz was measured to be

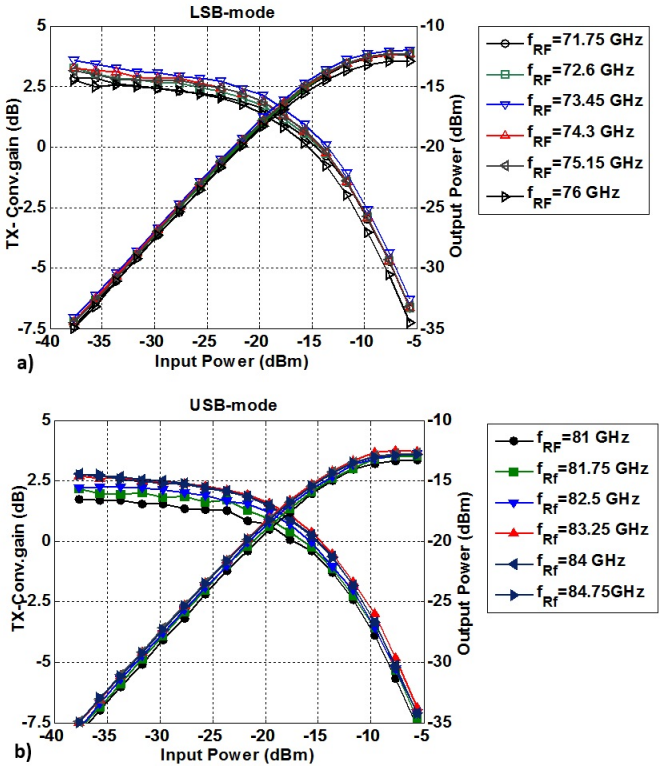


Figure 4.26: Transmitter measured output power and conversion gain versus input power for different frequencies for ($f_{LO} = 19\,to\,20\,GHZ$ and $f_{IF} = 9\,GHZ$) a) LSB mode, b) USB mode.

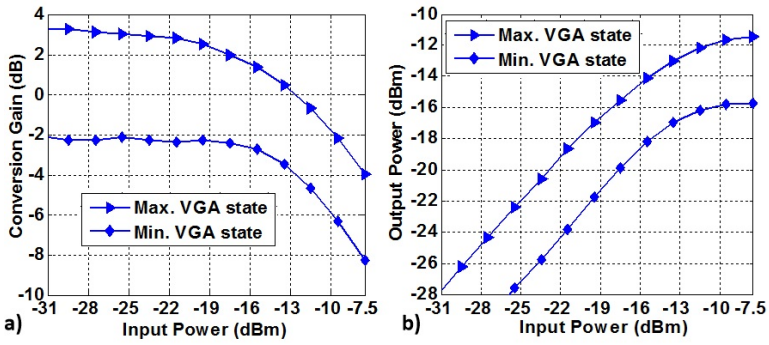


Figure 4.27: TX performance for two maximum and minimum VGA setting, a) Conversion gain, b) output power at 83.25 GHz.

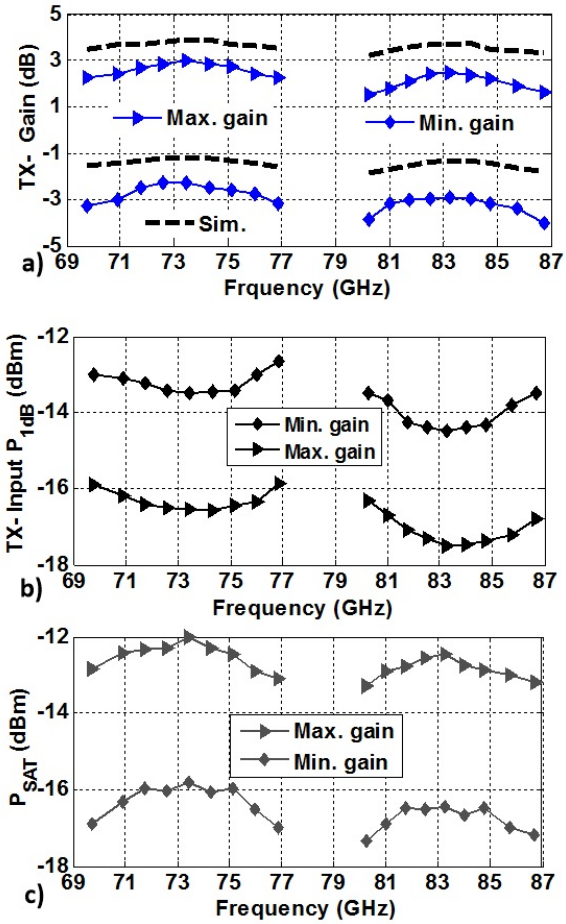


Figure 4.28: The transmitter performance versus frequency for the maximum and minimum states of VGA settings a) conversion gain, b) input P_{1-dB}, c) saturated output power.

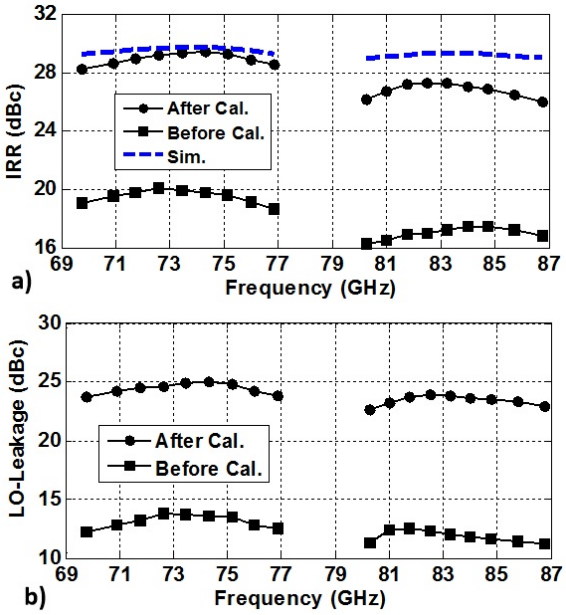


Figure 4.29: Before and after calibration performance for a) Image-rejection ratio versus frequency, b) LO-leakage versus frequency.

19 dB. After calibration, the IRR increases to maximum 29 dB. At 83 GHz, the minimum IRR is 17 dB and increases to 27 dB after calibration as illustrated in Fig.4.29 a). The IRR measurements shows that these results provide reasonable agreement with simulation in LSB mode under the assumption of 2° / 0.25 dB phase and amplitude imbalance. The LO-leakage of the transmitter which arises from the multiplication of four path, $4f_{LO}$, are presented in Fig. 4.29 b) for before and after calibration. The LO-leakage at 73 GHz improves from 14 dBc before calibration to 25 dBc after calibration, while at 83 GHz improves from 12 dBc to 24 dBc. In other words, an optimum calibration condition improves the LO-leakage by 10 dB.

4.4.3 RX CW measurements

The measured output spectrum of the receiver is shown in Fig. 4.30. The chip sets at USB mode where $\alpha_I\alpha_Q = 00/11$. The RF input frequencies of 82 GHz, USB, and 72 GHz, LSB, inserted to the RF port. As the block diagram of frequency conversion in Fig. 4.30 illustrates, using the LO of chip at 19.25 GHz,

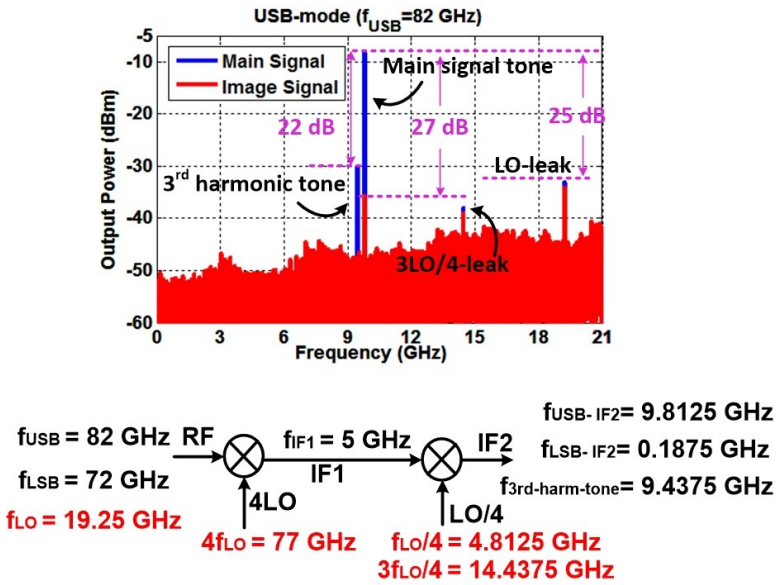


Figure 4.30: Output spectrum of receiver and the and the frequency conversion block diagram for USB mode with f_{USB} at 82 GHz and f_{LSB} at 72 GHz using f_{LO}=19.25 GHz.

move these USB and LSB signals at 5 GHz at IF1 band. This IF1 will mix with $f_{LO}/4$ equals to 4.8125 GHz and $3f_{LO}/4$ equals to 14.4375 GHz. This conversion generates IF output signals at $(f_{IF1} + f_{LO}/4) \approx 9.8$ GHz, $(f_{IF1} - f_{LO}/4) \approx 0.18$ GHz and the third harmonic spur tone at $(3f_{LO}/4 - f_{IF1}) \approx 9.43$ GHz.

Ideally, based on the USB/LSB mode, the desired RF band will move the in-band signal to $(f_{IF1} + f_{LO}/4)$. On the other hand, the image band will move the signal to $f_{IF1} - f_{LO}/4$, sec. 4.2.1 explained this. The second conversion term, $f_{IF1} - f_{LO}/4$ will be filtered out as the system has a high pass filter centered at 10 GHz after the second down-conversion. Therefore, in order to measure the IRR performance in RX mode, the input RF frequency should be located at the image band while the front-end is set to the complementary USB/LSB state. This will move the image signal at $(f_{IF1} + f_{LO}/4)$ which is in the IF2 band and hence will not be filtered out through the HPF. Fig. 4.30 shows the measured output spectrum of the signal at image band in a red-colored plot. The image signal is at 72 GHz, LSB band, while the system sets to USB mode. Applying the same f_{LO} of 19.25 GHz moves the signal at image band to the IF2 band, 9.812 GHz. The measurement shows 27 dB attenuation on a signal at image band, equivalent

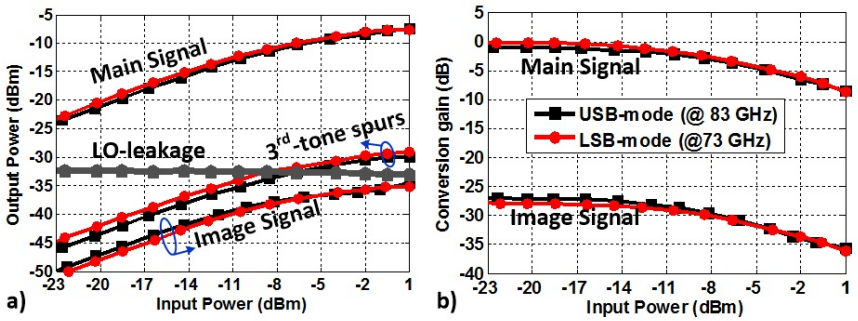


Figure 4.31: Measured RX performance versus input power for 73 GHz as LSB and 83 GHz as USB a) main signal, 3rd harmonic tone and image signal output power and $4f_{LO}$ LO-leakage power. b) main signal and image signal conv. gain.

to IRR of 27 dB. Moreover, under the same calibration condition, the RX system provides LO-leakage rejection better than 25 dBc. However, the unwanted mixing supers product generated by the 3rd harmonic tone of LO/4 circuitry, $3f_{LO}/4$, only get suppressed by 22 dBc. This rejection of 3rd harmonic spur is less than the LO-leakage rejection and IRR. This demonstrates the importance of linear operation regime of the divider by four path and its phase inverter block, which was explained in sec.4.3.4. Reducing the overall gain of the divider by four circuitry will reduce the overall conversion gain but improve the 3rd harmonic spur rejection.

The RX large signal performance for the USB signal at 83 GHz and LSB signal at 73 GHz are illustrated in Fig. 4.31 versus input power. The output power and the conversion gain of the main tone and unwanted 3rd harmonic mixing product tone versus input power are shown in Fig. 4.31 a) and b) respectively. The maximum output power at IF frequency of both USB and LSB modes is around -7.7 dBm. The suppression amounts for the LO-leakage , $3f_{LO}/4$ mixing spur, and image reject ratio are around 25 dBc, 22 dBc and 27 dB, respectively. Furthermore, Fig. 4.32 a) and b) presents the conversion gain and output power respectively versus input power for the two maximum and minimum setting of VGA. The measured conversion gain varies from -4.65 dB to -0.25 dB for the max and min states while the P_{sat} changes from -11.66 dBm to -7.43 dBm in these two states, respectively. The input P_{1-dB} reduced from -8.11 dBm for the min. VGA state to -10.6 dBm for the max. VGA state.

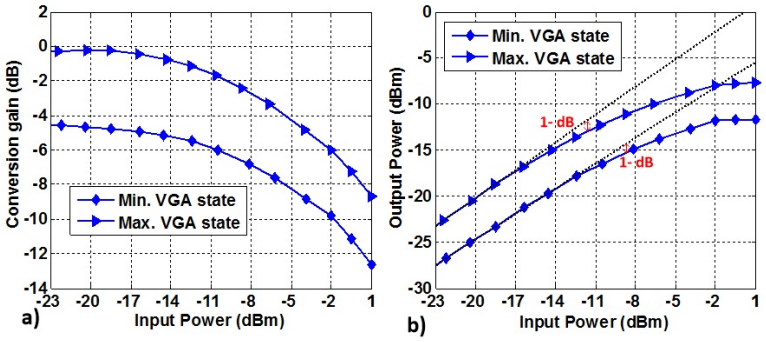


Figure 4.32: RX performance for two maximum and minimum VGA setting, a) Conversion gain, b) output power at 73 GHz.

The performance of the receiver over the frequency for the maximum and minimum states are illustrated in Fig. 4.33. The conversion gain shown in Fig. 4.33 a). The result shows the averaged value of -5.5 dB for the min. state and the -1 dB value for the max. state. The gain variation is less ±0.75 at the minimum and maximum VGA power levels in LSB band while the gain variation is ±0.8 dB in the USB band. The conversion gain variation over the entire the 71-86 GHz band is around ±1 dB for RX mode. The maximum output power of IF signals has an average power value of -12.5 dB for min. state and an average power level of -8 dBm for max state. The amount of power variation is less than ±0.5 dB for each band and ±1 dB for entire band, Fig. 4.33 b) shows this. Fig. 4.33.c) depicts the input P_{1-dB} of the receiver that has the average magnitude of -10.5 dBm for the maximum gain state which degrades to the averaged value of -8 dBm for the minimum gain state. The input P_{1-dB} variation over entire band is less than ±0.75 dB. The NF is also represented in Fig. 4.33 d). It changes from a NF_{min} of 14 dB for the min. gain state to NF_{min} of 20 dB for the max. gain state. The variation over entire band is ±1 dB.

The inter-modulation characteristic of the RX front-end is also measured by applying two-tone test located at 83 GHz and 83.1 GHz at the RF port of the receiver. Fig.4.34 a) illustrates the output IF spectrum for the -18 dBm input RF power. The main tone and the inter-modulation tone down-convert to 9.975 GHz and 10.075 GHz, respectively. The measured output power of main tone and the inter-modulation tones as the input power changes are plotted in Fig. 4.34 b),

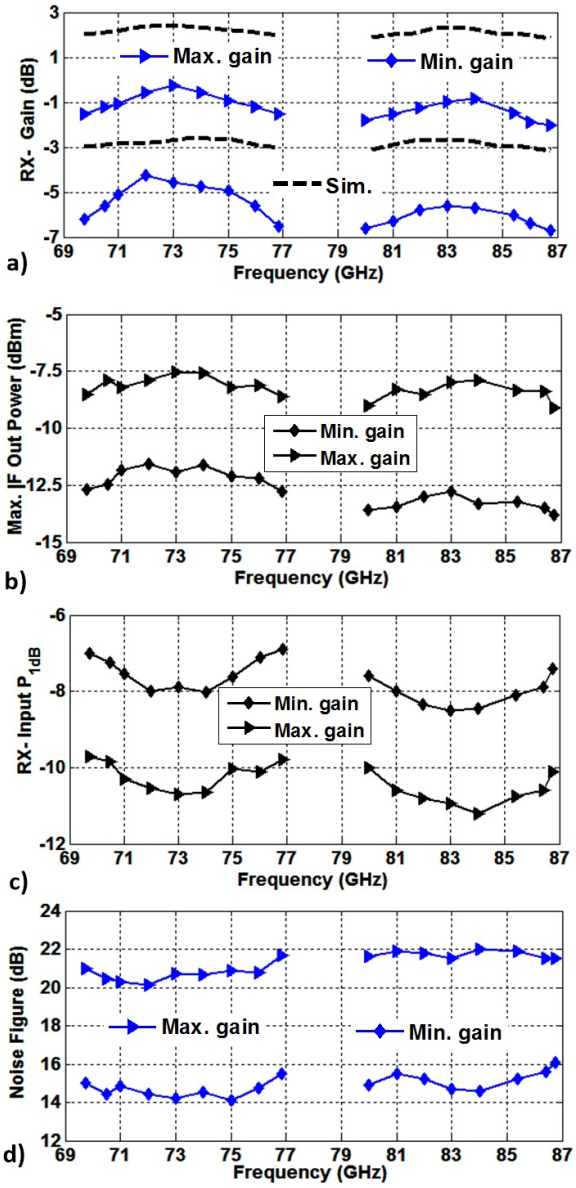


Figure 4.33: The receiver performance versus frequency for the maximum and minimum states of VGA settings a) conversion gain, b) maximum IF output power, c) input P_{1-dB}, and d) noise figure (NF).

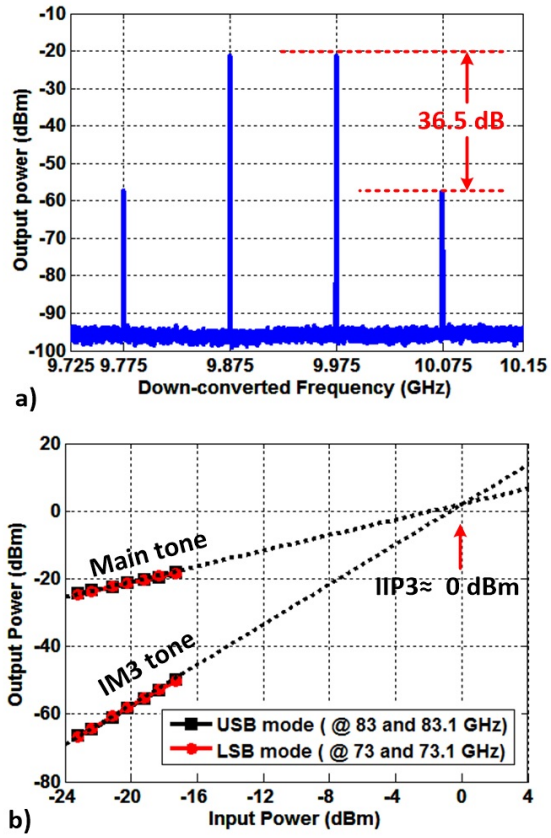


Figure 4.34: Measured third-order intercept point performance, a) output spectrum at the 83-GHz RF frequency for USB mode with -18 dBm input RF power, b) measured IIP3 results for both USB and LSB mode.

showing an IIP3 equals to 0 dB for the front-end.

Fig. 4.35 a) and b) shows the channel to channel isolation performance of the chip. For TX mode, the IF signal was inserted to the IF port of the chip while one of the channel was ON and the other was ON or OFF. In other words, the CH2 were probed and its output power measured while CH1 is ON and CH2 becomes ON or OFF. When both channels are ON, the maximum output power reduced by 1 dB compared to the situation when only one of them is ON, Fig. 4.35 a) shows this. In addition, when one of the channel is OFF while the other is ON, the output RF signal and the $4f_{LO}$-leaked signals at the RF port of ON channel will leak to the other channel's RF port. Fig. 4.35 a) also shows the amount of leaked power of CH1 as ON channel to CH2 as OFF channel in TX mode versus IF input power. As it is illustrated, the system has good amount of isolation, around

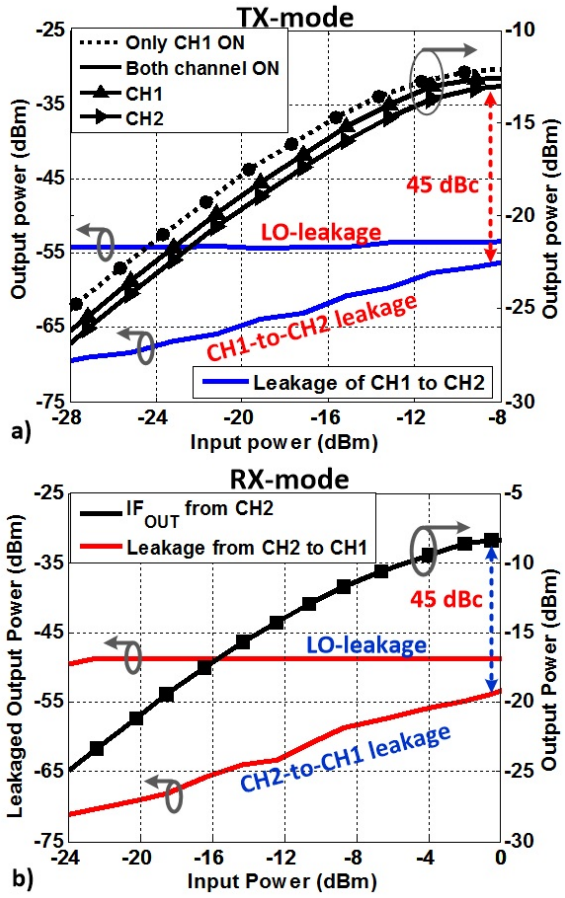


Figure 4.35: Measurement results for channel to channel isolation performance, a) TX mode, CH1 was ON and leaked to CH2 port, b) RX mode, CH2 was ON and leaked to CH1.

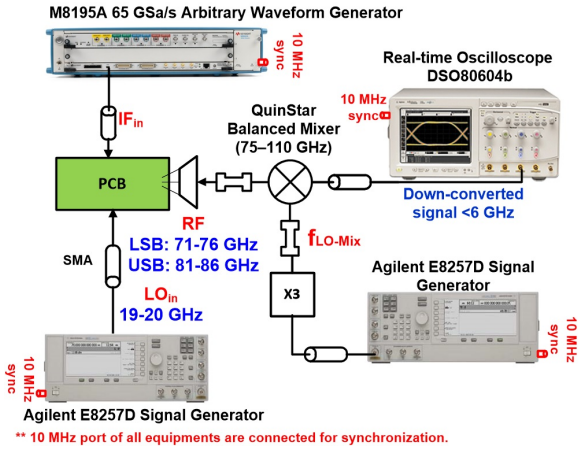


Figure 4.36: Modulation setup using 65 GSa/s Arbitrary Waveform Generator.

40 dBc for $4f_{LO}$ leakage and 45 dBc for main signal leakage.

For RX-mode the same setup were performed. The RF signal was inserted to the RF port of one of the channel which was ON while the other was OFF. Fig. 4.35 b) shows the output IF power variation of the ON channel, CH2, versus input RF power and the amount of leaked power, RF and $4f_{LO}$ signals, to the OFF channel's RF port, CH1. As it is shown, for RX mode, the signals at the RF port of ON channel will leak to the RF port of OFF channel. However it has the rejection around 45 dBc , which shows very significant isolation performance.

4.4.4 QAM Modulation Measurements

The QAM modulation for transmitter are performed using the measurement setup shown in Fig. 4.36. The modulated signal send to IF port using the 65 GSa/s arbitrary waveform generator. The RF output signal is captured using DSO80604b real-time oscilloscope which operates below 6 GHz. Therefore an external down conversion mixer with LO frequency named f_{LO-mix} in the figure is used for this down conversion function. The output captured data were analyzed using the 89600 VSA software to characterize the modulation performance. The 89600 VSA software is a comprehensive set of tools for signal demodulation and vector signal analysis.

Figure. 4.37 shows the output measurement result for the modulated signal

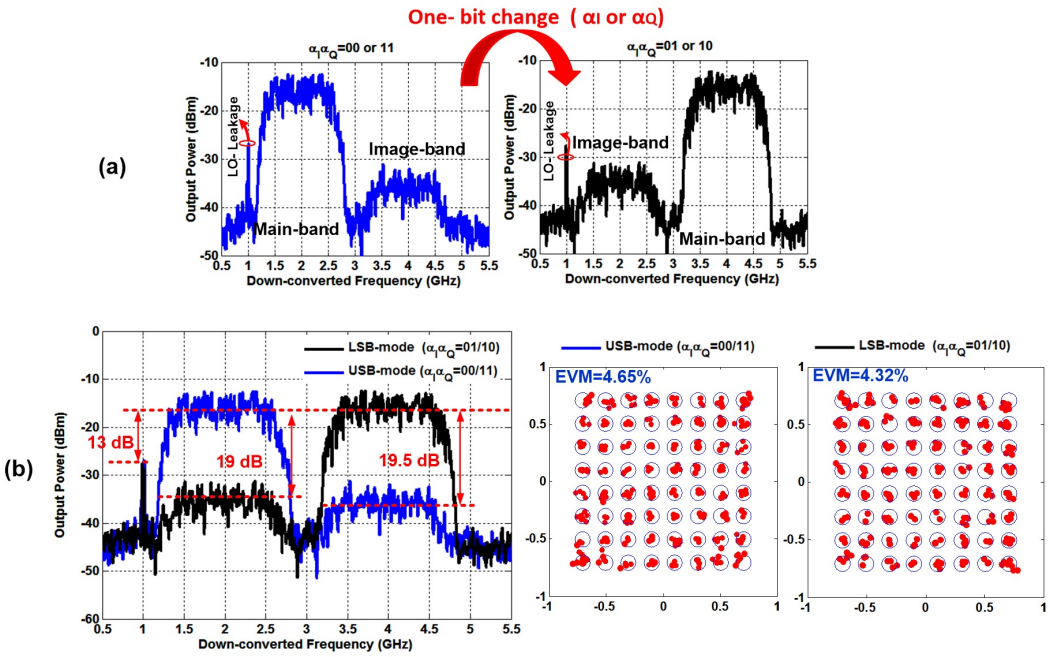


Figure 4.37: TX modulated output power with symbol rate of 1.25 GHz at 64 QAM (7.5 Gb/s), for f_{IF}= 7.875 GHz, f_{LO}= 19.5 GHz ($4f_{LO}$= 78 GHz) a) one bit change, b) USB/LSB EVM.

at f_{IF} of 7.875 GHz with the symbol rate of 1.25 GHz (7.5 Gb/s) at 64 QAM when only one bit of USB/LSB selection unit changes. Using the $f_{LO} = 19.5$ GHz sends the IF signals to the RF frequency of 75 GHz in LSB band and 81 GHz for USB band. Setting the LO frequency of the external down-converter mixer to 79 GHz will move the USB, LSB and $4f_{LO}$ signals at the frequencies of 2 GHz, 4 GHz and 1 GHz, respectively. Changing the one-bit of phase selection unit, α_I or α_Q, will move the IF signal from LSB band to USB band. In other words, it move the down-converted signals from the 4 GHz IF frequency to 2 GHz. Fig. 4.37 b) shows the two spectrum of USB and LSB modes on top of each other. The calibration conditions are set to have a medium IRR of 19.5 dB and LO-leakage of 13 dB. As it is illustrated, the proposed system provides a flat and constant power over the 1.25 GHz bandwidth on both modes. Fig.4.37 b) also illustrates the EVM characteristics for USB mode and LSB mode which are around 4.65% for USB mode and 4.32 % fore LSB mode

By applying the optimum calibration condition, using the 3-bits PPF and

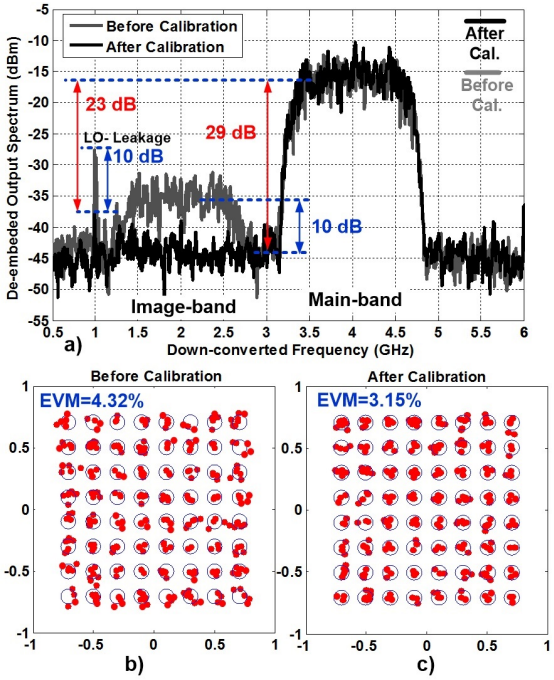


Figure 4.38: Calibration effect on TX modulated signal at LSB-mode with sampling rate of 1.25 GHz at 64 QAM, a) output spectrum before and after calibration, b) EVM before and after calibration.

VGA, the IRR can improve from 19 dB to 29 dB and the LO-leakage from 13 dBc to 23 dBc. Fig. 4.38 a) presents the calibrated down-converted spectrum of RF signal at 75 GHz (LSB mode). The optimum calibration effect on the EVM is also shown in Fig. 4.38 b). The EVM improves from 4.5 % for 7.5 Gb/s to 3.5 %.

The output EVM of the TX front-end over entire frequency bands (USB and LSB bands) were measured by changing the IF from 8 to 11 GHz and LO signal from 19 GHz to 20 GHz. As it was mentioned, the available real-time oscilloscope operates below 6 GHz. This will move all the RF port signals located at RF band, image band and $4f_{LO}$ band to below than 6 GHz down-converted IF frequencies. Therefore, the spectrum distances between the RF and image signals or RF and LO-leakage tone are reduced to less than 2 GHz. This limitation is the main restriction source of getting the highest possible modulated bandwidth and the data rate of the system.

For example, for a f_{IF} =8 GHz and f_{LO} =20 GHz and set-up mixer LO of 79 GHz, the USB, LSB, and $4f_{LO}$ signals are at 83, 77 and 80 GHz respectively. The

external mixer will move these tones to 2 GHz, 4 GHz and 1 GHz, respectively. The spectrum space between $4f_{LO}$-leakage and USB main signal is only 1 GHz, which restricts the symbol rate modulation to 1 Gb/s. Utilizing smaller LO, f_{LO} =19 GHz for the same IF, will move the USB, LSB, and $4f_{LO}$ to 2 GHz, 4.5 GHz and 1.25 GHz, respectively, which reducing the spectrum space between LO-leakage and USB main signal to below 0.75 GHz. This means that for frequency and band tuning which requires LO-tuning, the smaller LO value will limit the symbol rate and the resultant data rate. Therefore, due to this limitation of measurement equipment, the IRR and LO-leakage effects on the modulated signals for 64 QAM and 16 QAM were investigated by applying modulated signal with the symbol rate (bandwidth) of 1.25 GHz and 0.75 GHz. The results are shown in Fig. 4.39 for the USB and LSB bands which are tuned by f_{LO} from 19 GHz to 20 GHz. As it is illustrated in 4.39 a), for the higher bandwidth modulation (1.25 GHz), the lower LO frequency which is required to tune to the lower range of each USB and LSB band (71 or 81 GHz), the EVM deteriorates as the space between the down-converted main signal and the LO-leakage reduced. However, for the smaller bandwidth modulation (0.75 GHz), the space between the LO-leakage and main signal is enough that only IRR affect the modulation performance, Fig. 4.39 b) shows this. As it can be seen, the variation on EVM for this situation changes as the IRR varies over frequencies. Fig. 4.29 shows the IRR versus frequency that varies by $\pm$ 0.5 dB on each band and $\pm$1 dB between USB and LSB band. This leads to the EVM variation of less than 0.3 % of each band and less than 0.5% EVM variation over entire band.

The maximum achievable data rate or modulated signal bandwidth of the transmitter for 16 QAM and 64 QAM at 83 GHz is plotted in Fig. 4.40 a). As it is illustrated, the maximum achieved bandwidth for 16 QAM was around 3 GHz and for 64 QAM was around 2 GHz. The exact screen shot from the VSA software for 64 QAM modulation with 1.5 GHz bandwidth (9 Gb/s data rate) is shown in Fig. 4.40 b) which has below 4% EVM.

Fig. 4.41 a) and b) shows the result for the output EVM versus data rate for two conditions of IRR and LO-leakage. As it is shown, for IRR of 20 dB and

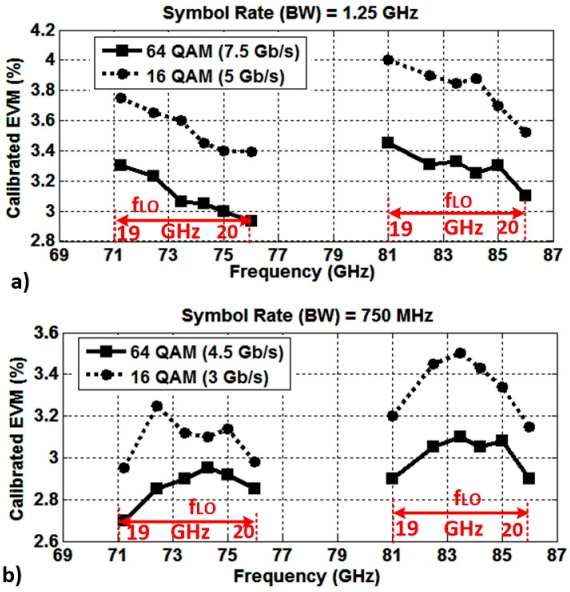


Figure 4.39: The calibrated EVM effect for 16 QAM and 64 QAM VS frequency as $f_{LO} tuned from$ 19 GHz to 20 GHz, a) BW=1.25 GHz, b) BW= 0.75 GHz.

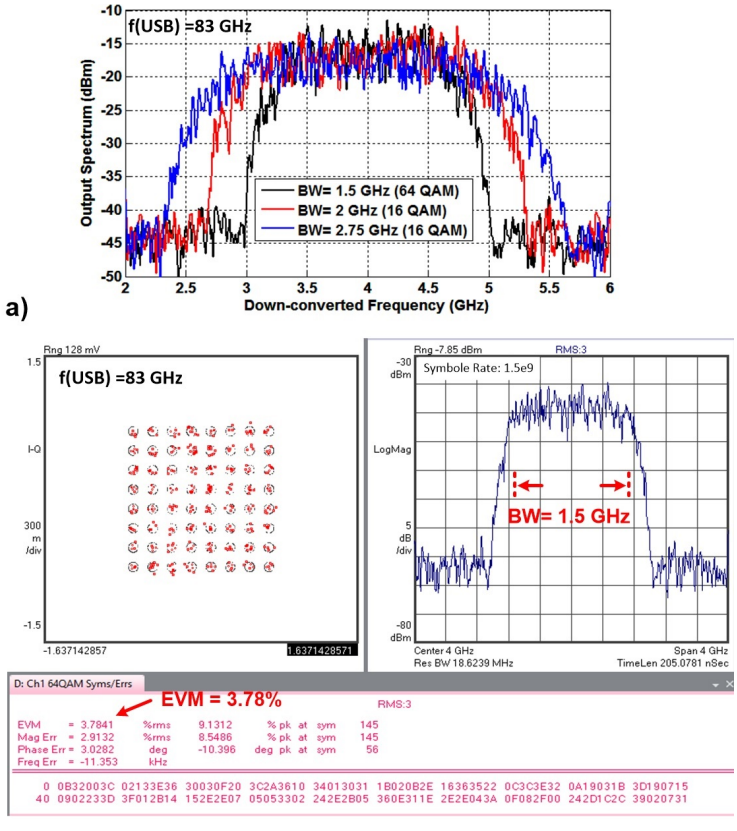


Figure 4.40: Maximum modulated bandwidth at 83 GHz USB band, a) for 16 QAM and 64 QAM, b) EVM and output spectrum for 9Gb/s 64 QAM.

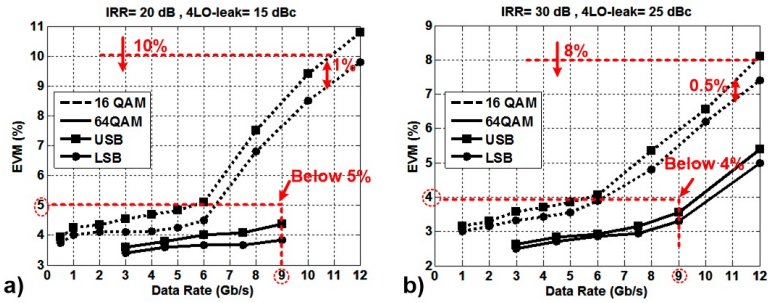


Figure 4.41: EVM versus data rate for two sets of IRR and LO-leakage calibration conditions a) IRR= 20 dB LO-leak 15 dBc, b) IRR=30 dB and LO leak 25 dBc.

LO-leakage of 15 dBc, the maximum data rate for 16 QAM is 12 Gb/s with EVM of 11 %. For EVM below 5% required for 5 G applications, the maximum data rate can go up to 6 Gb/s. For 64 QAM, the maximum data rate is 9 Gb/s for EVM below 4%. Optimizing the calibration condition to an IRR of 30 dB and LO-leakage of 25 dBc, will improve the EVM of the highest data rate by 2 %. In other words, for 16 QAM, the maximum data rate is 12 Gb/s with 8% EVM. In addition, the 64 QAM can reach to 12 Gb/s data rate with 5.5 % EVM. The other significant effect of the optimized calibration condition is improving the difference between the EVM of the USB and LSB modes.As shown in 4.41, the improved IRR of 30 dB boost the EVM difference of two bands from 1% to 0.5%.

The EVM dependence to the transmitter output power is also plotted in Fig. 4.42 for 16 QAM with data rate of 8 Gb/s and 4 Gb/s, and 64 QAM with data rate of 9 Gb/s and 6 Gb/s. The EVM is larger near the lower and higher output power levels. This is because of the degradation of the signal to noise (SNR) ratio under the lower power level and highly non-linear and distorted signals under higher power level. The EVM has the lowest value near the output P_{1-dB}.

4.4.5 Performance Summery and comparison

A comparison of this work with the other recent quadrature E-band or W-band transceiver [17,45–48,61] is shown in Table 4.1. The result indicates that this work requires the lowest LO tuning range to cover the 10 GHz RF band at 71-76

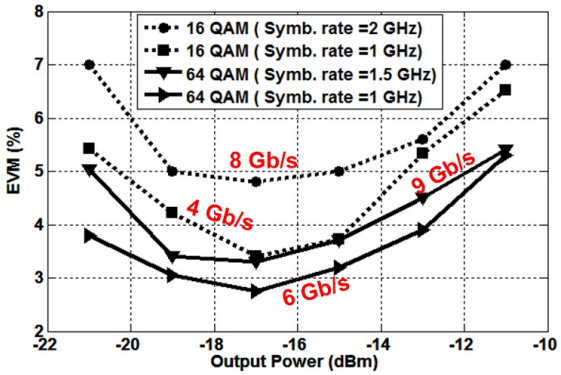


Figure 4.42: EVM for different output power for 16 QAM and 64 QAM with different data rates.

and 81-86 GHz and has the lowest EVM for both 16 QAM and 64 QAM as well as the highest data rate, 12 Gb/s and 9 Gb/s, respectively. It also demonstrates low conversion gain variation over the entire bandwidth. Note that this work is only a transceiver and requires a LNA and PA for further amplification of the RF output.

Acknowledgment

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Table 4.1: Comparison with other W-band and E-band transceiver

	[46]	[45]	[61]	[48]	[47]	[17]	**This Work**
Frequency (GHz)	70-90	71-76 81-86	71-86	71-86	64-84	70-100	**71-86**
Function	RX	TX/RX	TX/RX	TX	TX	TX/RX	**TX/RX**
LO-tuning range (GHz)	>25	>14	>10	>15	>20	>15	**3**
11inConversion Gain / element (dB)	**>19	**>36	**>20	**<11	0	**>25	**TX:-2.5to+3 RX: -4 to 0**
Gain Variation (dB)	8	N/A	>10	4	±1	>10	**TX:±0.75, RX:±1**
TX OP_{1-dB}/	N/A	**16.6	**7.5	**>7	**8.3	**5	[0]***> **-15**
RX input P_{1-dB} (dBm)	**-22	**-22	**-30.6	N/A	N/A	**-35	[0]***> **-10.5**
RX NF_{min} / element (dB)	**<11	**6	**9	N/A	N/A	**>7	**>14**
IRR (dB)	N/A	N/A	N/A	36-40	40	N/A	**30**
LO-leakage (dBc)	N/A	N/A	N/A	30	50	N/A	**25**
Constellation Data rate Gb/s EVM (%)	N/A	128 QAM 0.7 Gb/s 3%	256 QAM 6 Gb/s 3%	64 QAM (4.5 /6.3%) 16 QAM (14/12.6%)	256 QAM 0.04 /2%	16 QAM (10/ 8.1%) 32 QAM (8.75/ 6.6%)	**64 QAM (9/ 3.85%) 16 QAM (12/ 10.3%)**
DC Power (mW)	[1]*760	RX: 600 TX: 1800	RX: 286 TX: 386	[2]*102	40.8	500	[3]***<400**
Area (mm^2)	2.48	RX: 6.1 TX: 9.7	7.1	[4]*0.22	0.86	[5]*3.4	[6]***2.8**
Technology	0.35µm SiGe	0.13µm SiGe	90 nm SiGe	40 nm GP CMOS	65 nm CMOS	0.18 µm SiGe	**90 nm SiGe**
Architecture	Heterodyne	Sliding-IF Heterodyn	Heterodyne	Direct Conversion	Sub-harmonic	Direct Conversion	**Sliding-IF Weaver**

** containing PA for TX or LNA for RX transceiver. 0* Without any PA or amplifier to amplify this value. 1* with VCO and prescalor. 2* w/o LO frequency generation block. 3* 250 mW for LO-path. 4* w/o considering PADs. 5* 4-element phased-array. 6* PADs are considered but the repetitive blocks of second element is excluded.

Chapter 5

Conclusions and Future Work

This dissertation has focused on developing new architectures for scalable and wide-bandwidth multi-element systems and phased arrays for backhaul point-to-point communication in 5G technology, specifically at E-band.

Firstly, the high frequency implementations of injection-locked oscillator phase shifter on Silicon substrate were analytically investigated. The nonlinear dynamics of a LC injection-locked oscillator are derived based on the ILO circuit parameters. The linear and simplified model of ILO phase shifter under weak injection is presented and the effective circuit parameters such as locking bandwidth, injected current ratio, quality factor, and frequency detuning are discussed. The silicon substrate parasitic coupling effects on the ILO phase shifter were considered. The effects of substrate parasitics, $R_{\text{sub}}C_{\text{sub}}$, and transistor device parasitic capacitor, C_p, on amplitude and phase error of two neighboring ILOs were discussed. Two new amplitude and phase equations were derived and compared with the simulations and measurement results. A new injection circuitry called folded-cascode scheme is proposed that move the high-sensitive high parasitic injection node from the output node of the ILO to the source of injection transistor. The proposed injection scheme improves the locking range of the ILO as desired for arrays of ILO phase shifters.

Next, an E-band phased array operated over 71-86 GHz are designed that uses four injection-locked oscillator phase shifters for beam-forming. The phase shifters employed the proposed parasitic insensitive folded cascode architecture

for wide-band injection locking that improve the locking bandwidth of the 4 elements ILOs significantly, 250 MHz. This phased array architecture provides a power-efficient solution for scalable mm-wave phased array as the 4 ILOs in the array operates 1/4th of the required LO tuning range. A frequency multiplier increases the tuning range and provides 23-dB power gain to drive the bidirectional down/up conversion mixers. The phase shift that each element provides is $\pm 300^{\circ}$ phase range with less than 1-dB amplitude mismatch. The proposed folded cascode based phase shifter architecture provides high isolation between each phased array element improving the channel-to-channel isolation to under 0.5 dB. The phase noise variation over the steering angle is less than 2 degree with -112 dBc/Hz at 1 MHz offset. The low phase noise and low amplitude varition feature of the implemented phase array provide 6-Gb/s, 256-QAM modulation for the implemented ILO system.

An interesting future research direction is to investigate the most efficient number of array elements and coupled oscillators which can be implemented on lossy silicon substrates at mm-wave frequencies. In fact, as the number of elements increases, the required link budget for long-range communication also increases at the cost of more complexity and power consumption due to mm-wave loss. Moreover, packaging technology for multiple silicon chips connected to antenna arrays at mm-wave regimes is another challenging and interesting research problem, as shown in Fig. 5.1. The challenge arises from the transition between chips and antennas in different packaging approaches, such as the traditional wire bond technique and the flip chip technique, and from the use of new materials such as PolyStrata, which adds a different loss to the system's overall performance, limiting the number of phased array elements as well as beamformer scanning resolution.

However, as the number of coupled oscillator phase shifters in large-element phase arrays increases, their related locking range decreases because of a loss in the injection current distribution network at mm-wave frequencies. To extend the locking range, closed-loop architecture for ILO phase shifters, called phase-locked loop (PLL), can be used. In other words, for larger-element phased arrays (>4) exploiting coupled oscillator architectures at high frequency a PLL-based phase

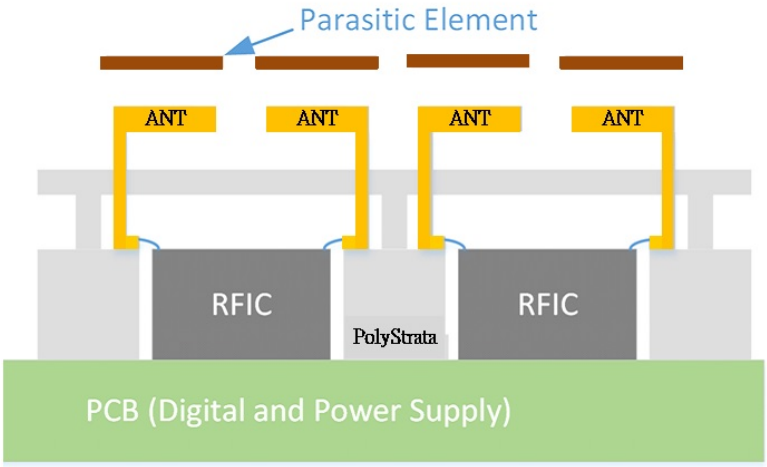

Figure 5.1: An example of packaging of multiple phased-array silicon chips integrated with antenna arrays.

shifter needs to be investigated, Fig. 5.2 elaborates this idea. The coupled PLL-based phase array could potentially conquer the bandwidth and injection power limitations of mm-wave band and could be considered as an interesting future research direction.

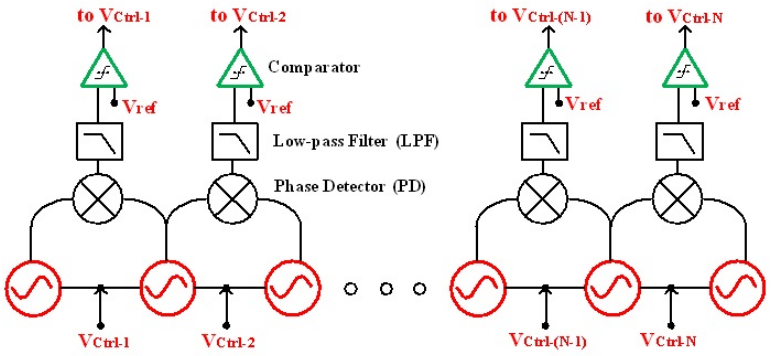

Figure 5.2: Proposed phase shifting technique for 5G large-elements beamforming transceiver using coupled oscillators in a phased-locked loops configuration.

In addition to research problems regarding system scalability, circuit building blocks must be optimized so as to operate more efficiently and to meet 5G

and IoT requirements. In the final chapter of this dissertation, a wideband E-band transceiver architecture that requires only 3 GHz LO-tuning range for the RF up/down converter is proposed. The architecture employs sliding-IF Weaver scheme, which is the first implementation above 60 GHz frequency. Requiring only 3 GHz LO tuning range needs only one-stage PPF for quadrature frequency generation which mitigates the amplitude/phase imbalance originated from the quadrature generation circuitry, PPF. Therefore, the resultant front-end provides a flat conversion gain and input/output P_{1dB} over entire wide-band operation, 71-86 GHz. These significant feature leads to the highest data rate for 64 QAM (9 Gb/s) with below 5\% EVM. The architecture can be applied to multiple input/output (MIMO) and phased-array systems.

Another interesting future research direction is that achieving higher data rate for the point-to-point communications such as 40 Gb/s. For this purpose, different channel multiplexing techniques needs to be investigated. The required antenna gain, system phase noise, maximum output power, and the digital signal processing blocks could be the limiting factors for getting high data rate communication systems. In other words, it is still unknown that what is the most limiting factor in the integrated wireless system to achieve a data rate near optical communication link such as 40 Gb/s.

Chapter 2 and 3 of this dissertation used and studied the synchronization characteristics of arrays of oscillators to create mm-wave beamformers for the next generation of ultra-high-data-rate wireless communications. In addition to this particular application in electronics, synchronized oscillators have various other applications in optical communications, secure wireless communications, and recently in neural network modeling and implementation. Oscillator behavior has been observed in different phenomena, such as bird migration and seasonal flora in the natural world, charge-density waves and Josephson junctions in condensed-matter physics, pendulum mechanisms in mechanics, and, significantly, firing neurons and sleep–wake cycles in biology [70], as illustrated in Fig. 5.3. The syn-

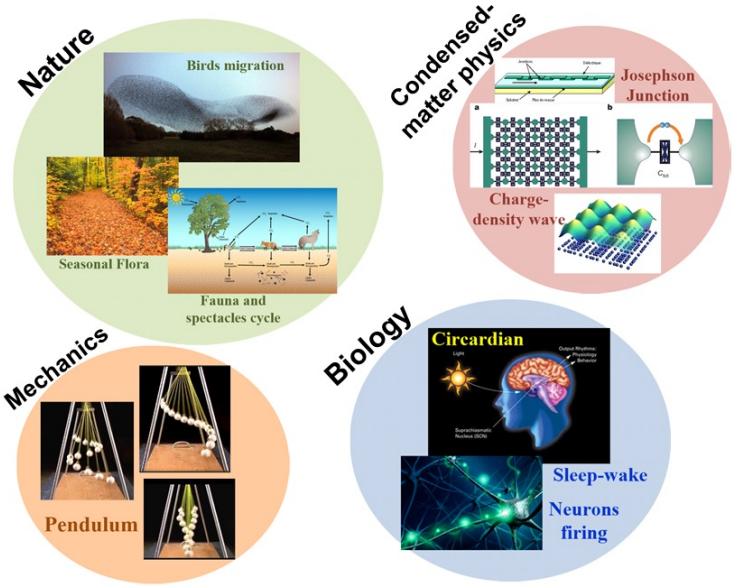

Figure 5.3: Oscillatory behaviors in various phenomena, nature, physics, mechanics, and significantly biology.

chronized behavior of neural firings explains many periodic human activities and related brain processing functions. Models of neuron behavior in neural networks can be used for image or speech recognition, where the fastest and most accurate computers and processors have been beaten by human intelligence functionality. In fact, emulation of neuron behavior for image or speech recognition necessitates an accurate dynamic model of neural networks. There are several ongoing research directions in the modeling of neural network activities. Some researchers consider the non-oscillatory behavior of neurons by averaging the firing rates of spikes. Others consider clusters of neuron action as oscillatory signals related to their phases, with the frequency dependent on the periodic timing of spikes [71]. Therefore, an array of coupled oscillators can be used to model brain processing functions such as pattern recognition. In [72], the authors propose a coupled oscillator associative memory array (COAMA) to recognize memorized input patterns encoded as oscillator parameters. If an input pattern is close to one of the memorized data, the oscillator phases synchronize, and they consequently enter a recognition state. However, if the input pattern is not predictable, the oscillators enter an error state.

Therefore, the material investigated in chapter 2 and 3 of this dissertation can be used to implement the brain processing functions such as pattern recognition on a silicon integrated circuit as an array of coupled oscillators.

Bibliography

[1] T. S. Rappaport and S. Sun and R. Mayzus and H. Zhao and Y. Azar and K. Wang and G. N. Wong and J. K. Schulz and M. Samimi and F. Gutierrez, "Millimeter Wave Mobile Communications for 5G Cellular: It Will Work!," in IEEE Access, vol. 1, 2013.

[2] A. Puglielli and A. Townley and G. LaCaille and V. MilovanoviÄĞ and P. Lu and K. Trotskovsky and A. Whitcombe and N. Narevsky and G. Wright and T. Courtade and E. Alon and B. NikoliÄĞ and A. M. Niknejad, "Design of Energy- and Cost-Efficient Massive MIMO Arrays," in Proceedings of the IEEE, vol. 104, March 2016.

[3] C. S. Wang, J. W. Huang, K. D. Chu and C. K. Wang, "A 60-GHz Phased Array Receiver Front-End in 0.13- μm CMOS Technology," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 10, pp. 2341-2352, Oct. 2009.

[4] K. Scheir and S. Bronckers and J. Borremans and P. Wambacq and Y. Rolain, "A 52 GHz Phased-Array Receiver Front-End in 90 nm Digital CMOS," in *IEEE Journal of Solid-State Circuits*, vol.43, pp.2651-2659, Dec. 2008.

[5] W.L. Chan, J.R. Long., "A 60-GHz Band 2x2 Phased-Array Transmitter in 65-nm CMOS, in *IEEE Journal of Solid-State Circuits*, vol.45, pp.2682-2695, Dec. 2010.

[6] Y. Yu, P. G. M. Baltus, A. de Graauw, E. van der Heijden, C. S. Vaucher, and A. H. M. van Roermund, " A 60 GHz phase shifter integrated with LNA and PA in 65 nm CMOS for phased array systems," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1697–1709, Sep. 2010.

[7] A. Valdes-Garcia, S. T. Nicolson, L. Jie-Wei, A. Natarajan, C. Ping-Yu, S. K. Reynolds, Z. Jing-Hong Conan, D. G. Kam, L. Duixian, and B. Floyd, "A fully integrated 16-element phased-array transmitter in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 45, pp. 2757–2773, 2010.

[8] E. Cohen, C. G. Jakobson, S. Ravid, and D. Ritter, "A bidirectional TX/RX four-element phased array at 60 GHz with RF-IF conversion block in 90-nm CMOS process, *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 5, pp. 1438–1446, May 2010.

[9] M. Tabesh, C. Jiashu, C. Marcu, K. Lingkai, K. Shinwon, A. M. Niknejad, and E. Alon, "A 65 nm CMOS 4-element sub-34 mW/element 60 GHz phased-array transceiver," *IEEE J. Solid-State Circuits*, vol. 46, pp. 3018–3032, 2011.

[10] A. Natarajan, S. K. Reynolds, T. Ming-Da, S. T. Nicolson, J. H. C. Zhan, K. Dong Gun, L. Duixian, Y. L. O. Huang, A. Valdes-Garcia, and B.A. Floyd, "A fully-integrated 16-element phased-array receiver in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 46, pp. 1059–1075, 2011.

[11] S. Emami, R. F.Wiser, E. Ali, M.G. Forbes, M. Q. Gordon,G.Xiang, S. Lo, P. T. McElwee, J. Parker, J. R. Tani, J. M. Gilbert, and C. H. Doan, "A 60 GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2011, pp. 164–166.

[12] M. Tabesh and J. Chen and C. Marcu and L. Kong and S. Kang and A. M. Niknejad and E. Alon, "A 65 nm CMOS 4-element sub-34 mW/element 60 GHz phased-array transceiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3018–3032, Dec. 2011.

[13] A. Natarajan, A. Komijani, G. Xiang, A. Babakhani, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Transmitter and local LO-path phase shifting," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2807–2819, 2006.

[14] A. Babakhani, G. Xiang, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2795–2806, 2006.

[15] S. Woorim, O. Inac, O. Yu-Chin, K. Bonhyun, and G. M. Rebeiz, "A 108–112 GHz 4 4 wafer-scale phased array transmitter with high-efficiency on-chip antennas," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, 2012, pp. 199–202.

[16] Bon-Hyun Ku; Inac, O.; Chang, M.; Hyun-Ho Yang; Rebeiz, G.M., "A High-Linearity 76–85-GHz 16-Element 8-Transmit/8-Receive Phased-Array Chip With High Isolation and Flip-Chip Packaging," *IEEE TMTT* , vol.62, no.10, pp.2337-2356, Oct. 2014.

[17] S. Shahramian and Y. Baeyens and N. Kaneda and Y. K. Chen, "A 70–100 GHz Direct-Conversion Transmitter and Receiver Phased Array Chipset Demonstrating 10 Gb/s Wireless Link," in IEEE JSSC, vol. 48, no. 5, pp. 1113-1125, May 2013.

[18] S. Y. Kim, O. Inac, C. Y. Kim, D. Shin and G. M. Rebeiz, "A 76–84-GHz 16-Element Phased-Array Receiver With a Chip-Level Built-In Self-Test System," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 3083-3098, Aug. 2013. doi: 10.1109/TMTT.2013.2265016.

[19] P. Wang, Y. Li, L. Song and B. Vucetic, "Multi-gigabit millimeter wave wireless communications for 5G: from fixed access to cellular networks," in IEEE Communications Magazine, vol. 53, no. 1, pp. 168-178, January 2015.

[20] J. Wells, "Faster than fiber: The future of multi-G/s wireless," IEEE Microw. Mag., vol. 10, no. 3, pp. 104–112, May 2009.

[21] "Fixed radio systems: Characteristics and requirements for point-topoint equipment and antennas," ETSI, Sophia Antipolis, France, ETSI EN 302 217-2-2 V2.0.0, Sep. 2012.

[22] D. Lockie and D. Peck, "High-data-rate millimeter-wave radios," IEEE Microw. Mag., vol. 10, no. 5, pp. 75–83, Aug. 2009.

[23] A. Oreskovic, "Facebook is using 'experimental' technology from Raytheon in latest aircraft tests," in *Businessinsider.com, Nov.16, 2015.*

[24] J. Kim, and J. F. Buckwalter, "A switchless, Q-Band bidirectional transceiver in 0.12-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol.47, no.2, pp.368–380, Feb. 2012.

[25] S. P. Voinigescu and A. Tomkins and E. Dacquay and P. Chevalier and J. Hasch and A. Chantre and B. Sautreuil, "A Study of SiGe HBT Signal Sources in the 220–330-GHz Range," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2011-2021, Sept. 2013.

[26] P. Chevalier and C. Fellous and L. Rubaldo and F. Pourchon and S. Pruvost and R. Beerkens and F. Saguin and N. Zerounian and B. Barbalat and S. Lepilliet and D. Dutartre and D. Celi and I. Telliez and D. Gloria and F. Aniel and F. Danneville and A. Chantre, "230-GHz self-aligned SiGeC HBT for optical and millimeter-wave applications," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 10, pp. 2025-2034, Oct. 2005.

[27] H. Fotsin, S. Bowong, and J. Daafouz, Chaos, Solitons & Fractals 26, 215 (2005).

[28] S. Strogatz, Sync: the emerging science of spontaneous order (Hyperion Books, New York, 2003).

[29] P. Colet and R. Roy, "Digital communications with synchronized chaotic lasers," Opt. Lett., vol. 19, no. 24, pp. 2056–2058, Dec. 1994.

[30] C. R. Mirasso, P. Colet, and P. GarcÃŋa-FernÃąndez, "Synchronization of chaotic semiconductor lasers: Application to encoded communication," IEEE Photon. Technol. Lett., vol. 8, no. 2, pp. 299–301, Feb. 1996.

[31] G. D. VanWiggeren and R. Roy, "Communication with chaotic lasers," Science, vol. 279, no. 5354, pp. 1198–1200, 1998.

[32] J. F. Buckwalter and A. Babakhani and A. Komijani and A. Hajimiri, "An Integrated Sub-harmonic Coupled-Oscillator Scheme for a 60-GHz Phased-Array Transmitter," in IEEE TMTT, vol.54, pp.71-80, Dec. 2006.

[33] Liao & R. A York, "A new phase-shifterless beam-scanning technique using arrays of cou-pled oscillators," IEEE TMTT, vol.41, no.10, pp.1810-1815, Oct 1993.

[34] F. Tzeng, A. Jahanian, D. Pi, and P. Heydari, "A CMOS code-modulated path-sharing multi-antenna receiver front-end," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1321–1335, May 2009.

[35] Y. A. Atesal, B. Cetinoneri, K. M. Ho, and G. M. Rebeiz, "A two-channel 8–20-GHz SiGe BiCMOS receiver with selectable IFs for multibeam phased-array digital beamforming applications," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 3, pp. 716–726, Mar. 2011.

[36] H. Krishnaswamy and H. Hashemi, "A variable-phase ring oscillator and PLL architecture for integrated phased array transceivers," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2446–2463, Nov. 2008.

[37] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2311–2320, Dec. 2004.

[38] O. Inac, D. Shin and G. M. Rebeiz, "A Phased Array RFIC With Built-In Self-Test Capabilities," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 1, pp. 139-148, Jan. 2012.

[39] J. Birkeland and T. Itoh, "A 16 element quasi-optical FET oscillator power combining array with external injection locking," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 3, pp. 475-481, Mar 1992.

[40] Liao & R. A York, “A new phase-shifterless beam-scanning technique using arrays of coupled oscillators,” *IEEE TMTT*, vol.41, no.10, pp.1810-1815, Oct 1993.

[41] J. F. Buckwalter and A. Babakhani and A. Komijani and A. Hajimiri, “An Integrated Sub-harmonic Coupled-Oscillator Scheme for a 60-GHz Phased-Array Transmitter,” in *IEEE TMTT,* vol.54, pp.71-80, Dec. 2006.

[42] S. Patnaik, R. Harjani, “A 24-GHz phased-array receiver in 0.13-µm CMOS using an 8-GHz LO,” in Radio Frequency RFIC, *2010 IEEE*, pp.465-468, 23-25 May 2010.

[43] Wu. Liang, A. Li, H.C. Luong, “A 4-Path 42.8-to-49.5 GHz LO Generation With Automatic Phase Tuning for 60 GHz Phased-Array Receivers,” in *IEEE Journal of Solid-State Circuits*, vol.48, pp.2309-2322, Oct. 2013.

[44] R. Adler, “A study of locking phenomena in oscillators,” in Proceedings of the *IEEE*, vol.61, Oct. 1973.

[45] R. Levinger and R. B. Yishay and O. Katz and B. Sheinman and N. Mazor and R. Carmon and D. Elad, "High-Performance E-Band Transceiver Chipset for Point-to-Point Communication in SiGe BiCMOS Technology," in IEEE TMTT, vol. 64, April 2016.

[46] I. Nasr and B. Laemmle and K. Aufinger and G. Fischer and R. Weigel and D. Kissinger, "A 70-90-GHz High-Linearity Multi-Band Quadrature Receiver in 0.35-µm SiGe Technology," in IEEE TMTT, vol. 61, no. 12, pp. 4600-4612, Dec. 2013.

[47] W. H. Lin and H. Y. Yang and J. H. Tsai and T. W. Huang and H. Wang, "1024-QAM High Image Rejection E-Band Sub-Harmonic IQ Modulator and Transmitter in 65-nm CMOS Process," in IEEE TMTT, vol. 61, Nov. 2013.

[48] D. Zhao and P. Reynaert, "A 40 nm CMOS E-Band Transmitter With Compact and Symmetrical Layout Floor-Plans," in IEEE JSSC, vol. 50, no. 11, Nov. 2015.

[49] I. Nasr, M. Dudek, R. Weigel, and D. Kissinger, “A 33% tuning range high output power -band superharmonic coupled quadrature VCO in sige technology,” in IEEE Radio Freq. Integr. Circuits Symp., Montreal, QC, Canada, Jun. 2012, pp. 301–304.

[50] D. Sanderson, R. Svitek, and S. Raman, “A 5-6-GHz polyphase filter with tunable I/Q phase balance,” IEEE Microw. Wireless Compon. Lett., vol. 14, no. 7, pp. 364–366, Jul. 2004.

[51] S. Galal, H. Ragaie, and M. Tawfik, “RC sequence asymmetric polyphase networks for RF integrated transceivers,” IEEE Trans. Circuits Syst. II, Analog Digti. Signal Process., vol. 47, no. 1, pp. 18–27, Jan. 2000.

[52] S. Kim and H. Shin, “A 0.6-2.7 GHz semidynamic frequency divide- by-3 utilizing wideband RC polyphase filter in 0.18 m CMOS,” IEEE Microw. Wireless Compon. Lett., vol. 18, no. 10, pp. 701–703, Oct. 2008.

[53] B. Laemmle, K. Schmalz, C. Scheytt, A. Koelpin, and R. Weigel, “Directional couplers from 30 to 140 GHz in silicon,” in Proc. Asia–Pacific Microw. Conf., Yokohama, Japan, Dec. 2010, pp. 806–809.

[54] https://en.wikipedia.org/wiki/Q_factor

[55] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrazi and A. A. Abidi, “The Quadrature LC Oscillator: A Complete Portrait Based on Injection Locking,” in IEEE Journal of Solid-State Circuits, vol. 42, no. 9, pp. 1916-1932, Sept. 2007.

[56] B. Razavi, “A study of injection locking and pulling in oscillators,” in IEEE Journal of So id-State Circuits, vol. 39, no. 9, pp. 1415-1424, Sept. 2004.

[57] B. Razavi, *RF Microelectronics, Second Edition.* Upper Saddle River, NJ: Prentice Hall, 2012.

[58] S. Fregonese, R. D’Esposito, M. De Matos, A. KÃűhler, C. Maneux and T. Zimmer, "Sub-strate-coupling effect in BiCMOS technology for millimeter wave applications," New Cir-cuits and Systems Conference (NEWCAS), 2015 IEEE 13th International, Grenoble, 2015, pp. 1-4.

[59] M. Pfost and H. M. Rein, "Modeling and measurement of substrate coupling in Si-bipolar IC’s up to 40 GHz," in IEEE Journal of Solid-State Circuits, vol. 33, no. 4, pp. 582-591, Apr 1998.

[60] N. Ebrahimi, M. Bagheri, P. y. Wu and J. F. Buckwalter, "An E-band, scalable 2×2 phased-array transceiver using high isolation injection locked oscillators in 90nm SiGe BiCMOS," 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Francisco, CA, 2016, pp. 178-181.

[61] N. Ebrahimi, P. Y. Wu, M. Bagheri and J. F. Buckwalter, “A 71–86-GHz Phased Array Transceiver Using Wideband Injection-Locked Oscillator Phase Shifters,” in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 2, pp. 346-361, Feb. 2017.

[62] Najme Ebrahimi, James Buckwalter, Lecture Notes in Networks and Systems, vol. 6, pp. 245, 2017, ISSN 2367-3370, ISBN 978-3-319-52620-1.

[63] P. Y. Wu; T. Kijsanayotin; J. F. Buckwalter, "A 71-86-GHz Switchless Asymmetric Bidirectional Transceiver in a 90-nm SiGe BiCMOS," in *IEEE Transactions on Microwave Theory and Techniques* , no.99, pp.1-12, 2016.

[64] J. Kim and K. Konstantinou, "Digital predistortion of wideband signals based on power amplifier model with memory," in *Electronics Letters*, vol. 37, no. 23, pp. 1417-1418, 8 Nov 2001.

[65] P. Y. Wu, Y. Liu, B. Hanafi, H. Dabag, P. Asbeck and J. Buckwalter, "A 45-GHz Si/SiGe 256-QAM transmitter with digital predistortion," 2015 *IEEE MTT-S International Microwave Symposium*, Phoenix, AZ, 2015, pp. 1-3.

[66] J.G.Proakis, and M. Salehi, "Digital Communications. 5th Edition, McGraw-Hill, New York, 2008.

[67] F. Haddad, L. Zaid, W. Rahajandraibe, and, O. Frioui, . "Polyphase Filter Design Methodology for Wireless Communication Applications" 2010.

[68] A. Mirzaei and H. Darabi, "Analysis of Imperfections on Performance of 4-Phase Passive-Mixer-Based High-Q Bandpass Filters in SAW-Less Receivers," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, no. 5, pp. 879-892, May 2011.

[69] P. Y. Wu, A. K. Gupta and J. F. Buckwalter, "A Dual-Band Millimeter-Wave Direct-Conversion Transmitter With Quadrature Error Correction," in IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 12, pp. 3118-3130, Dec. 2014.

[70] R. Moussounda, "Analysis and Design of Coupled-oscillator Arrays for Microwave Systems", Ph.D. dissertation, Ohio-state university, 2013.

[71] F.C. Hoppensteadt and E. M. Izhikevich, "Pattern recognition via synchronization in phase-locked-loop neural networks," in IEEE Transactions on Neural Networks, vol. 11, May 2000.

[72] D. E. Nikonov and G. Csaba and W. Porod and T. Shibata and D. Voils and D. Hammerstrom and I. A. Young and G. I. Bourianoff, "Coupled-Oscillator Associative Memory Array Operation for Pattern Recognition," in IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, vol. 1, Dec. 2015.