Title
Hybrid Switched-Capacitor Converter Design: State-Space Dynamical Modeling and Passive Device Characterization

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Publication Date
2023

Peer reviewed|Thesis/dissertation

Hybrid Switched-Capacitor Converter Design: State-Space Dynamical Modeling and Passive Device Characterization

By

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A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering — Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

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Summer 2023

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Abstract

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Power electronics design best configures available electrical devices—transistors, inductors, and capacitors—to realize a theoretical power conversion function in the smallest, lightest, cheapest, and most efficient manner. In particular, hybrid switched-capacitor converters are a contemporary and high-performance class of circuit topology utilizing both inductors and capacitors. To better understand how these converters behave and are realized in practice, this manuscript will explore several contributing design aspects—modeling, passive devices, and practical printed circuit board layout—applied to a particular circuit topology of active research interest.

First, the thesis will explore the results of a comprehensive survey of commercial passive components and how their figures-of-merit might be used to inform converter design. The survey explores the capabilities of prominent types of discrete capacitors and inductors. Then this manuscript applies this survey to the design of an aluminum electrolytic capacitor bank on the dc-link of a single-phase power conversion system.

Second, this thesis analyzes dynamical modeling for the flying capacitor multilevel (FCML) power converter, a topology with nearly inexhaustible switching state combinations. It presents a simplified derivation and abstraction of a conventional averaged Fourier-derived model for this FCML switching-circuit topology, and it provides extensions to existing work and explores design implications. Next, this manuscript outlines a methodology for deriving a functional, accurate, and computationally efficient discrete-time state-space dynamical model for the FCML converter; this model is validated with results measured from a high-performance hardware prototype.

Finally, the thesis investigates the usage of multilevel converters to demonstrate the underlying feasibility of the single-stage buck-type power factor correction (PFC) rectifier. A high-performance multilevel converter prototype is developed with an especial focus on com-

pactness, high efficiency, and low-inductance layout in the switching commutation loops. Then the theoretic input current harmonics, power factor, and total harmonic distortion of the buck PFC are derived and compared to the prevailing regulatory IEC current emission standards.

"Great are the works of the Lord, studied by all who delight in them." Psalm 111:2

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Acknowledgments

This is an extensive list of acknowledgements, but each person mentioned has had a marked influence on my life these past years in graduate school. I would not be who I am today without them.

First, thank you to all of those people who aided me in my research these last few months. You have helped me accomplish so much in too little of an amount of time, and my present vocational goals are possible due to your charitiable efforts. An especial thanks to Finn Giardine, Jiarui Zou, Sam Coday, Nathan Ellis, Bradley Bowles, Elissa Krause, Ting Ge, Rahul Iyer, Nathan Biesterfeld, my advisor Robert Pilawa-Podgurski and my other thesis committee members for their significant editing and contributions towards the writings that invariably became part of this thesis.

This first section acknowledges the past and present members of my research group who have shared so much life with me. Thank you to my graduate student mentors during my earliest years in graduate school: Shibin Qin, Enver Candan, and Zitao Liao. I know that mentoring a barely capable junior graduate student must have had its frustrations, but I appreciate all of your patience. You were and still are each wonderful role models, and continue to inspire me in the ways I engage with and mentor others. I also appreciate the additional past alumni and visitors of our research group: Ting Ge, Zichao Ye, Pourya Assem, Chris Barth, Wen-Chuen (Joseph) Liu, Nathan Pallo, Andrew Stillwell, Yutian Lei, Pei Ng, Sophia Chou, Thomas Foulkes, Yizhe Zhang, Michelle Rentauskas, Yong-Long (Max) Syu, Ivan Petric, Mads Taul and several members prior to my time who I have never had the pleasure of meeting. Our research group's most vital and wonderful feature is its people, and you have all cultivated an especially collaborative, enjoyable, and enduring group culture. The research group today owes to you much of the expectations for joviality and passion towards engineering and study.

I especially want to thank all of the current members of my research group. First, there is my senior cohort: Sam Coday, Maggie Blackwell, Rose Abramson, Kelly Fernandez, as well as postdoctoral student Nathan Ellis. It was great fun to work and struggle diligently together to create something enduring. And thank you to the other members: Logan Horowitz, Rahul Iyer, Yicheng Zhu, Rod Bayliss, Finn Giardine, Jiarui Zou, Sahana Krishnan, Haifah Sambo, Elisa Krause, Nathan Biesterfeld, Nagesh Patel, Jospeh Schaadt, Ben Liao, Will Vavrik, Marrin Nerenberg, and Shalin Shah. I do not have space to acknowledge all of you independently, but just know that many of you have profoundly impacted my life. You have each been a true pleasure to work with and I wish the best for you all as you accomplish your aspirations and succeed in your life's endeavors.

There are several of these individuals I must highlight in particular. Thank you Sam Coday (and your husband, Chance) for your constant willingness to answer my questions about research and teaching. You have always been one step ahead of me, and my path is made easier following in your footsteps. Thank you for being such a personal role model and motivating me to strive towards the best professional I can be: capable and dependable in the eyes of others.

Thank you Shalin Shah for trusting both me and my initially flimsy research vision for large-scale passive component characterization. Your dedicated commitment has strengthened and ultimately realized this now shared vision.

Without Rahul Iyer, Rod Bayliss, Logan Horowitz, and Ivan Petric, the components of my research and thesis relating to the flying capacitor multilevel converter (FCML) would not have materialized as soon. Their efforts in writing, theorizing, and experimenting were instrumental to my success. I am deeply pleased with my time in graduate school and the results of my PhD research, and much of what you read in this thesis is owed to their sincere collaborative efforts. I will further acknowledge these four individuals in particular.

Firstly, Rahul Iyer—a man with an innately adventurous nature. Your kindness, thoughtfulness, and helpfulness have greatly elevated the validity and rigor of my research. I hope your future excursions into the modeling and control of multi-phase power converters can be as impactful to the power electronics field as I dream they can be.

Rod Bayliss, your passion is infectious. You have (quite successfully) encouraged me to more fully engage with the world, something for which I am eternally grateful. And although prudence is certainly important, you have demonstrated to me a more active and less circuitous approach to practice engineering. In having spent much time with you, I suspect the synapses within my brain are now rewired more efficiently.

Logan Horowitz, thanks for being an open, honest friend and sharing so much of your time and your passions. You have an unusually quirky and creative approach to engineering and I look forward to witnessing the future path your life will take.

Ivan Petric, you are without doubt uniquely gifted at making deep friendships. And your technical competence and precision inspires me. I have particularly enjoyed our every past conversation on life, and look forward to every future one.

Now on to other acknowledgments. Thank you to Rose-Hulman, my undergraduate alma matter, for building me a firm foundation of engineering knowledge. There are more than several qualities especially endearing about that school, and it well prepared me for the graduate school. I am especially excited to be working there as a teaching professor after my graduation, surrounded by teachers and a community I hold in such high esteem. I owe a specific thanks to Professors Ed Wheeler, Tina Hudson, and Daniel Moore for being fantastic academic and research advisors.

Thank you to the University of Illinois at Urbana-Champaign for patronizing my early graduate school studies. And thank you Professor Subhonmesh Bose at the University of Illinois for guiding me through my first proper experience as a teaching assistant.

I am greatly appreciative to the University of California, Berkeley for providing me the multitude of opportunities to explore and participate in the pursuit of learning. Thank you Shirley Salanio for being an ever-present advocate and helping me meet my graduation requirements.

Thank you Professors Miki Lustig, Laura Waller, Rikki Mueller, and especially Professor Ana Arias for providing me the wonderful opportunity to be a teaching assistant for the introductory electrical engineering course at Berkeley: EECS 16A. In particular, Ana and Miki inspired me while I watched their unique, lively lectures and educated me as we delib-

erated course logistics and content. I have learned from you two so much of what a professor can and should be. And you also personally taught me the life-altering impact of just a few encouraging words, and I will forever be grateful for your faith in my untempered abilities.

Much thanks to Alfredo De Goyeneche, Tiffany Chien, Anniruddh Khanwale, Anvitha Kachinthaya, Anish Dhanashekar. As teaching assistants, you inspire as you pursue the best possible experience for students, and I greatly enjoyed those moments we worked together.

Thank you Robert Pilawa for being the best advisor, mentor, and supervisor I could ever hope for. I have grown and matured tremendously under your care, and I truly have few complaints after seven years. You are a role model as a professor, an engineer, a teacher, a husband, and a father. And I would be bereft to not acknowledge your wife, Brooke, and your children. Thank you for supporting him as he rassles our unwieldy research group.

And now into the last section of my acknowledgements. Thank you Josh Hanlon, Mike Hanlon, and Travis Luther for our shared efforts to learn more about the world through literature. Our journey has transformed me.

Thank you Fawaaz Shaffeeullah, Elijah Stanger-Jones, and David Kornfeld: three impressively talented engineers and friends who share with me a penchant for merry competition and tomfoolery. Your dependable camaraderie has uplifted me these past few years.

Thank you Joe Millitello, Max Kelly, Peter and Julianne Larson, Kirsten Sullivan, Nithin Perumal, Daniel McGarry, Alec Tiefenthal, Tyler Miller, Jacob Knispel, and Tim Smith. You have been present during my most joyous and some of my most despairing moments and I treasure our uniquely enduring friendships. Thank you Alex and William for forever changing the course of my life for the better. Now I know the difference between good and evil, and I have sufficient conviction to stand up for what is right when it most matters.

Thank you to my dearest friends these many years: Thomas Jansen, Jonathan Class, Bradley Bowles, and Josh Hanlon. It is commonly said that one's friends are a reflection of their character, but in truth they shape it. I am blessedly overjoyed and gratified knowing you are the people who have shaped me. Thank you especially to Thomas (and your wife Hannah) Jansen. You are a sincere man of faith, family, and friendship. You are the best man I know, you are always there for me, and I am blessed to be your brother.

I appreciate all of the members of my immediate and extended family, as well as family friends. You who have consistently supported and encouraged me since before I could even speak. Thank you Aaron, my (biological) brother, who knows me better than anyone else. I am immeasurably proud of you and your accomplishments and you have always inspired me to be a better man. Thank you Mom and Dad. You have always been the wind in my sails—loving and supporting me in every stage of my life. I owe this wonderful life to you.

I thank You most above all, Jesus Christ my Lord and Savior, whose love has no bound. I share a certainty with a greater man than I who once said, "What is done by what is called myself is, I feel, done by something greater than myself in me." [156]. That 'something' is You, God who, with grace, designed and created this wondrous world and its incomprehensible majesty—including both my mind's capacity for understanding and those marvelous and intensely peculiar phenomenon of electronics I consider with awe and exuberance. For all who read this thesis, please enjoy His work.

Chapter 1

Introduction

1.1 Introduction

This thesis culminates research of several disparate subtopics aimed at the high-performance design of hybrid switched-capacitor power converter circuit topologies. The formation of semi-meaningful solutions to this design objective requires intensive characterization of presently available capacitors and inductors (Part I); accurate modeling of the periodic, multi-state switching circuits (Part II); and improvements in hardware implementation such as the printed circuit board layout (Part III). This work is by no means definitive, however, it does form a reasonable foundation and highlights avenues of future approach.

1.2 Organization of Thesis

Part I: Passive Components in Power Electronics

High performance power electronics design requires a firm characterization of active and passive components. This part presents a framework for quantifying passive component performance by reviewing existing device characterization methods and applying robust device figures-of-merit.

Chapter 2: Passive Component Survey and Characterization

Assemblage of a comprehensive survey yields aggregated data for nearly 700,000 commercial capacitors and inductors of all types. To supplement deficiencies in this data, this chapter proposes and validates several empirical expressions to estimate passive component energy storage and mass. Estimation of volumetric mass density per component type allows the approximation of component mass from accessible box volume. Estimation of energy-equivalent capacitance in nonlinear Class II ceramic capacitors facilitates the evaluation of stored energy and related energy density figures-of-merit. A phenomenological analysis of

the comprehensive component data produces several conclusory determinations about peak energy density capabilities—with respect to volume, mass, and cost—across capacitor and inductor technologies.

Chapter 3: Application of Passive Component Data to DC-Link Buffering Capacitor

The conventional dc-link aluminum electrolytic capacitor bank simply, efficiently, and cost-effectively decouples the instantaneous power mismatch inherent to all single-phase ac-dc power converters. However, the practical realization of the capacitor bank remains largely qualitative and dependent on the opaque performance capabilities of the capacitor technology. This chapter presents an exhaustive survey of commercial aluminum electrolytic capacitors and defines both quantitative and justly comparative device-level figures-of-merit (FOM). By configuring the relative voltage ripple ratio specification α of the dc bus, these device FOM enable the determination of minimal dc-link capacitor volume, cost, and/or mass. Graphical illustration demonstrates that the set of commercially available yet viable components diminishes as specification α increases; the realized dc-link capacitor bank volume and cost will grow appreciably for $\alpha > 10\,\%$ and $\alpha > 5\,\%$, respectively.

Part II: Modeling of the Flying Capacitor Multilevel Converter

In recent decades the flying capacitor multilevel (FCML) converter has been demonstrated to be a highly compact and efficient substitute for conventional switched inductive topologies. However, the fundamental dynamical behavior of the additional flying capacitor voltages has not been well characterized to a predictable level for phase-shifted PWM modulation strategies.

Chapter 4: Review of Continuous-Time State-Space Modeling for the FCML Converter

The dynamical behavior of the flying capacitors in the FCML are unable to be modeled using conventional small-signal linearization and averaging techniques for periodically switched power converters. This chapter revisits the derivation of the frequency-domain generalized average model proposed in [114]. It both simplifies and extends the original analysis and assumptions, and it affirms prior intuition for effects of circuit parameter dependence and duty ratio instability on dynamic performance.

Chapter 5: Discrete-Time State-Space Modeling for the FCML Converter

With the context of previously defined averaged circuit model, this chapter presents an accurate and computationally efficient analytical model for the buck-type FCML converter which includes the critical influences of parasitic resistance and transistor output capacitance C_{oss}.

The complete modeling methodology produces a discrete-time state-space dynamical representation applicable to converters with multiple switching states. Analysis of the model eigenvalues elucidates the impacts of parameter variation on capacitor voltage balancing performance—including input-to-state disturbance rejection—in the time and frequency domains. The model is validated against a high-performance 5-level hardware prototype.

Part III: Multilevel Converters for Buck-Type Power Factor Correction

This final part investigates several practical considerations enabling the use of multilevel converters in buck-type power factor correction (PFC) conversion systems.

Chapter 6: PCB Layout Improvements for the Buck PFC FCML Converter

Proper utilization of GaN devices generally necessitates ultra-low inductance printed circuit board (PCB) layout in the main commutation loop or switching cell of a power converter. The flying capacitor multilevel (FCML) topology in particular contains many of these switching cells, thus design optimization becomes critical. A novel asymmetrical cell layout design with sub-1 nH commutation loop inductance is proposed for the FCML converter and characterized with a transient- and impedance-based measurement technique in conjunction with 3D field simulation. To validate its efficacy, this switching cell design is demonstrated within a prototype high performance step-down intermediate bus converter supply ($v_{\text{out}} = 48\,\text{V}$) with wide input voltage range ($v_{\text{in}} = 48$ to $340\,\text{V}$).

Chapter 7: Power Factor and Harmonic Limitations of the Buck PFC Converter

The single-phase buck-type PFC converter is incapable of achieving unity power factor because it cannot conduct near the zero-crossing of the ac line. However although imperfect, this conversion system still ably meets current harmonic benchmarks in most practical cases. This chapter investigates the theoretical conversion limitations of the buck-type PFC power converter—including the impact of phase displacement—and derives expressions for fundamental limits according to IEC current harmonic emissions standards.

Part I

Passive Components in Power Electronics

Chapter 2

Passive Component Survey and Characterization

2.1 Introduction

Modern power electronic converters comprise active semiconductor devices (e.g., diodes and transistors), and passive devices to electromagnetically store and release energy (e.g., capacitors, inductors, transformers). A comprehensive understanding of the breadth and capabilities of these devices is required to design and realize a physical converter of desired conversion efficiency, volume, mass, cost, lifetime, and dynamic performance. Both novel and mature component technologies constantly improve over time, and the best-suited device for a particular application depends on the system specification and, even more intricately, on other selected devices.

The choice of optimal circuit topology varies when scrutinizing the passive devices in particular. The most mature switched-mode circuit topologies primarily rely on inductors for energy storage (e.g., buck; boost; buck-boost; flyback; and dual-active bridge, DAB, converters). Since they are difficult to miniaturize [167], inductors continue to demand intense research focus for the device-level design of power converters. The comparably lower losses and higher energy densities of capacitors [133, 42, 203] have motivated the investigation and development of more inductive/capacitive circuit topologies in recent decades: multilevel converters [144] (e.g., modular multilevel converter, MMC [158, 127, 48]; flying capacitor multilevel, FCML, converter [115, 107, 88]); hybrid switched capacitor converters [11, 87, 154, 108] (e.g., series-capacitor buck [121, 74, 157]); and isolated resonant converters [162] (e.g. series-resonant [76, 91]; LLC [100, 49]). These families of power converter topologies are each high-performance and can maximally utilize the energy storage and power throughput capabilities of both capacitors and inductors.

This chapter extends our previous conference paper [203] by aggregating a comprehensive set of device data and motivating useful figures-of-merit (FOM) for comparison and extension to design. Section 2.2 describes general methods for device-level characterization and

introduces a framework for producing robust, or maximally applicable, device FOM. Employing comprehensive data collection, this chapter surveys a useful breadth of over 606,000 commercial capacitors and 88,000 commercial inductors as detailed in Section 2.3. Additional sampled data is garnered to supplement and augment particular deficiencies in this large data set. To enable complete characterization of energy storage metrics—the critical benchmark of capacitive and inductive energy storage elements—a sampled set of capacitor data is collected and extrapolated to the full data set as described in Section 2.4. To estimate component mass, a sampled set of components is measured and extrapolated to the full data set as described in Section 2.5. After applying the supplements to energy storage and mass, Section 2.6 investigates several device FOM for all surveyed components. As a demonstration, the analysis compares the energy densities of various capacitor and inductor technologies, specifies the conditions for voltage overrating in capacitors and current overrating in inductors, and examines the quality factor capabilities of inductors.

2.2 Characterizing Components and Defining Performance

Making reductive determinations from millions of passive components requires careful consideration of how data is collected and then manipulated into useful quantitative metrics that describe comparative performance trade-offs. The goal is to produce founded statements such as "based on the present available technology, the smallest possible capacitor solution for this application has volume X." To substantiate these claims, this chapter first introduces viable methods of data aggregation and analysis, then motivates useful device FOM.

Data Analysis Methods

There are three general methods to determine the broad capabilities of a set of circuit components, where sets are classified by the distinctive 'type' or 'technology' of the component.

Analytically derived performance

Utilizing a first principles approach based in physics, one can derive analytical expressions for the lumped circuit model of an electrical device from its internal geometries and constituent material properties. Further determinations are either made directly from the analytical expressions, iteratively fit to measured data, or generated using a probabilistic Monte Carlo simulation. Examples of analytic methods include estimation of the 'macroscopic' hysteretic losses of Class II ceramic capacitors from 'microscopic' properties in [110, 111, 75]; quality factor prediction of air core inductors in [159]; derivation of frequency-dependent volume and loss scaling trends in inductors in [167]; and estimation of parasitics for transistors in [12].

Sampled data and extrapolation

Data collection, often measured, can completely characterize circuit phenomenon for small data sets. However for large sets of intractable or unknown data, intelligent data sampling can yield exceedingly meaningful qualitative and quantitative insight. With additional care, the sampled data extrapolates to larger supersets of data—especially with the advent of recent machine-learning (ML) techniques. This sampled data method is applied to predict capacitor ESR and quality factor in [42, 15]; capacitor lifetime in [70, 10, 109]; power loss in inductors in [68, 159]; and power FET losses in [12, 57]. Another variation of this sampled data approach trains ML models to predict core losses in broadly excited inductors [89, 90] and to predict losses in transistors [137].

Comprehensive data collection

The proliferation of digitized data and its increasing ease of access enables large-scale, comprehensive, and practically exhaustive collection of component information. Distributors of electrical components have consistently lead efforts to aggregate and disseminate quantitative component information, however, many individual manufacturer/suppliers have drastically broadened their interactive design tools and consumer interfaces as well. A comprehensive consideration of data necessarily enables conclusive interpolative—rather than extrapolative—quantification of performance and a holistic cognizance of notoriously mercurial metrics such as cost. A comprehensive data collection approach in [28] is used to benchmark performance amongst commercial high power switch technologies ($> 1\,\mathrm{kV}$ and $> 1\,\mathrm{kA}$). A recent approach in [137] uses data from commercial capacitors, inductors, and transistors to train ML models and produce optimal converter designs [138].

This chapter primarily employs the *comprehensive data collection* approach for device characterization. In aspects where this method stalls, *sampled data and extrapolation* is utilized to augment the comprehensive data set.

Defining Useful Device Figures-of-Merit

Meaningful device metrics, deemed figures-of-merit (FOM), must be developed in conjunction with bulk device characterization. A good FOM is a quantitative measure of performance and indisputably indicates better performance for larger (or smaller) values, similar performance for equivalent values, and worse performance for smaller (or larger) values. Although not often accentuated, the FOM philosophy intrinsically permeates the field of engineering and enables quantitative benchmark and comparison of complex systems [82]. These metrics provide a common language for engineers to judge a solution's capabilities or the evolution of a technology [22]. Applied to power electronics—a system comprised of many smaller subsystems—it is possible in principal to relate converter-level FOM to constituent device-level FOM to constituent material-level FOM [69, 12].

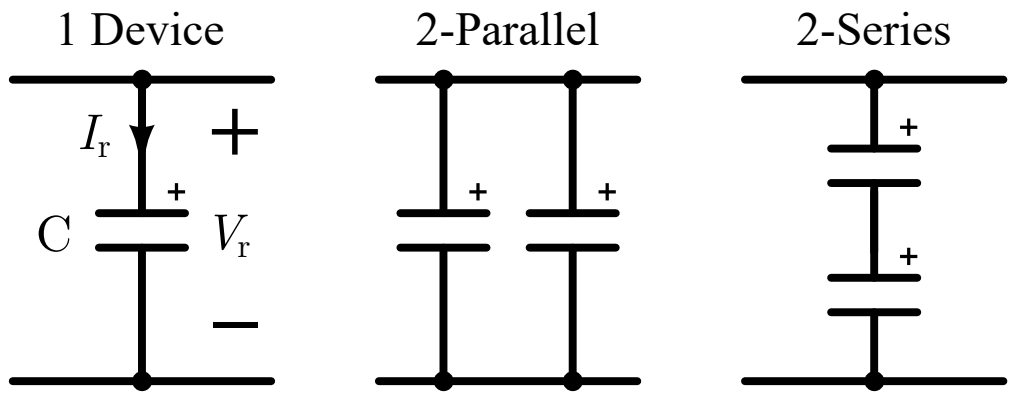


Figure 2.1: Schematic denoting series and parallel bank configurations of a capacitor component.

The 'system scope' in this chapter is a discrete passive component. Others have motivated specific FOM for quantifying the performance of individual electronic devices: capacitors [136], inductors [68], and transistors [94, 12], with the intention of characterizing component application to larger circuits, however, no work has generalized a method for conceiving useful device FOM.

To accomplish this, consider how these devices are utilized. Two-terminal passive devices are commonly configured into series and/or parallel connected component banks to meet specified requirements often relating to energy storage or power throughput. Series-parallel modularity is even common for electrical systems such as power conversion circuits [82, 80] and photovoltaic (PV) panels [61, 19]. Consequently, any metric defined as a FOM in this thesis critically adheres to the following proposed property:

> **Property of Series-Parallel Modular Invariance:** A device metric invariant to series and/or parallel configuration of the device.

If a metric adheres to this property, then it is a FOM that can fairly compare devices of various voltage and current ratings and is deemed 'robust'.

The series-parallel modular invariance property is demonstrated schematically in Fig. 2.1 and generalized in Table 2.1 for a series and parallel configuration of a capacitor with specified capacitance C, rated dc voltage V_r, rated rms current I_r, equivalent series resistance ESR, box volume, cost, and mass. In this context, combinations of these base attributes yield some robust FOM which satisfy this property and are agnostic to both series and parallel component configurations—e.g., volumetric energy density γ_v, gravimetric power density ρ_m, and loss tangent $\tan\delta$ (or dissipation factor DF).

Table 2.1: Generic capacitor bank specifications and constructed figures-of-merit

Total Specification	1 Device	2-Parallel	2-Series	n-Series/ m-Parallel
C_{tot}	C	$2C$	$\frac{1}{2}C$	$\frac{m}{n}C$
$V_{\text{r,tot}}$	V_{r}	V_{r}	$2V_{\text{r}}$	nV_{r}
$I_{\text{r,tot}}$	I_{r}	$2I_{\text{r}}$	I_{r}	mI_{r}
ESR_{tot}	ESR	$\frac{1}{2}$ESR	2 ESR	$\frac{n}{m}$ESR
Vol_{tot}	Vol	2 Vol	2 Vol	nm Vol
Mass_{tot}	Mass	2 Mass	2 Mass	nm Mass
Cost_{tot}	Cost	2 Cost	2 Cost	nm Cost
$E_{\text{r,tot}} = \frac{1}{2}CV_{\text{r}}^2$	E_{r}	$2E_{\text{r}}$	$2E_{\text{r}}$	nmE_{r}
$P_{\text{r,tot}} = V_{\text{r}}I_{\text{r}}$	P_{r}	$2P_{\text{r}}$	$2P_{\text{r}}$	nmP_{r}
$\gamma_{\text{v,tot}} = \frac{E_{\text{r,tot}}}{\text{Vol}_{\text{tot}}}$	γ_{v}	γ_{v}	γ_{v}	γ_{v}
$\rho_{\text{m,tot}} = \frac{P_{\text{r,tot}}}{\text{Mass}_{\text{tot}}}$	ρ_{m}	ρ_{m}	ρ_{m}	ρ_{m}
$(\tan\delta)_{\text{tot}} = \omega C\,\text{ESR}$	$\tan\delta$	$\tan\delta$	$\tan\delta$	$\tan\delta$

Examples of Robust FOM

Conventional capacitor FOM satisfying the series-parallel modular invariance property include charge-discharge efficiency $\frac{E_{\text{discharge}}}{E_{\text{charge}}}$ [150, 182, 92]; loss tangent or dissipation factor $\tan\delta$ or quality factor $Q = \frac{1}{\tan\delta}$ [150, 52, 15]; dielectric loss density $\frac{P_{\text{loss}}}{\text{Vol}}$ [111]; the Ohms-Farad product $C \cdot \text{ESR}$ [150, 136]; packaging efficiency, the proportion of active volume within the device to total device volume [136, 65]; energy density of the dielectric material [182, 86, 34, 35]; energy density of the whole capacitor $\frac{E_{\text{r}}}{\text{Vol}}$, $\frac{E_{\text{r}}}{\text{Mass}}$, or $\frac{E_{\text{r}}}{\text{Cost}}$ [102, 130, 77, 182, 85, 37, 15, 92, 151, 45, 155, 52]; power density $\frac{P_{\text{r}}}{\text{Vol}}$ or $\frac{P_{\text{r}}}{\text{Mass}}$ [77, 24]; volumetric mass density or specific volume $\frac{\text{Mass}}{\text{Vol}}$ [203, 22]; and lifetime L_0 [10, 180].

Conventional inductor FOM satisfying the series-parallel modular invariance property includes the ac quality factor Q_{ac} [67, 72, 78, 98, 193, 18, 159]; relative dissipation factor or relative loss factor $\frac{\tan\delta}{\mu_{\text{r}}}$ [72, 55]; the volumetric core (eddy current or hysteresis) loss $\frac{P_{\text{loss}}}{\text{Vol}}$ [68, 78]; and the specific loss density $\frac{P_{\text{loss}}}{\text{Mass}}$ [146].

These capacitor and inductor FOM are suitable candidates for component comparison

across the entire device subspace. Future research explorations of these metrics could consider trade-offs and derive connections to the devices' broader system application [24].

Limited or Operating Condition Specific Capacitor Metrics

Some common-use device metrics, especially for capacitors, are only parallel modular and thus partially satisfy the series-parallel modular invariance property. These metrics can be utilized for device comparison, but require a more restrictive and judicious context, most commonly by only comparing capacitors of a specific rated voltage V_r. Some examples include current density $\frac{I_\mathrm{r}}{\mathrm{Vol}}$ and $\frac{I_\mathrm{r}}{\mathrm{Mass}}$ [150, 38]; capacitance-related current density $\frac{C}{I_\mathrm{r}}$ [38]; volumetric efficiency or charge density $\frac{C \cdot V_\mathrm{r}}{\mathrm{Vol}}$ [150]; capacitance density, volumetric capacitance, or capacitance volumetric efficiency $\frac{C}{\mathrm{Vol}}$ [125, 119, 84, 10, 37]; capacitance voltage product per rated current $\frac{C \cdot V_\mathrm{r}}{I_\mathrm{r}}$ [150]; cost per farad $\frac{\mathrm{Cost}}{C}$ [151]; and specific capacitance $\frac{C \cdot V_\mathrm{r}}{\mathrm{Mass}}$ [65, 136, 22].

Limitations of Series-Parallel Device Configurations

Arbitrarily configuring discrete components in series and in parallel has associated practical limitations: increased layout inductance, asymmetrical current distribution, unbalanced voltage distributions, and lower packing factor [37, 59, 3]. For the purposes of this FOM analysis, these shortcomings—which can be mitigated with conscientious design—are neglected.

2.3 Commercial Capacitor and Inductor Data

Desired device FOM are constructed from base metrics, and thus the greater acquisition of base metrics directly enables the determination of more FOM. This section describes the availability and extent of the surveyed data for discrete commercial passive components. It also delineates the capacitor and inductor typologies used throughout this thesis.

Extent of Available Data – Capacitors

The present distributor data sets contain certain practicable information with varying degrees of consistency: (near) fully available, partially available, or not available. Satiating a partially or unavailable component attribute can enable the determination of secondary metrics (e.g., rated stored energy E_r and volume) and tertiary FOM (e.g., energy and power density). As discussed in Section 2.2, this requires either supplemental measured data with extrapolation, or theoretic generalization of the component derived from material properties.

The comprehensive data set consists of an aggregation of roughly 606,000 distinct capacitors from the prominent distributor Digikey Electronics.

Fully Available Data

Readily available data includes several primary attributes: capacitor rated voltage V_r; the zero-voltage differential capacitance $C(0)$ [110]; the dimensional parameters: length, width, height, diameter; and the cost per unit. The secondary attribute 'box' or enclosure volume is computed from the dimensional attributes. For linear capacitors, the secondary attribute of rated stored energy E_r is calculable in aggregate from these base attributes. However, the prominent Class II ceramic capacitor technology has a nonlinear voltage-dependent capacitance characteristic [110], and thus E_r cannot be calculated for all capacitor technologies without additional analysis presented in Section 2.4.

Partially Available Data

The equivalent series resistance (ESR); loss tangent or dissipation factor $\tan\delta = \mathrm{DF}$; rated rms current I_r; and lifetime L_0 are all critical attributes for any quantitative performance analysis of capacitor loss and reliability, however, these metrics are unavailable in the overall distributor data set for most capacitor technologies except for some aluminum electrolytic capacitors. Some of these base attributes also maintain a pertinent frequency and temperature dependence, and are inconsistently standardized across manufacturers. Thus even though correction factors are sometimes disclosed, the oftentimes singular values for ESR, $\tan\delta$, I_r, and L_0 common to catalogs and datasheets are often inadequate for involved electronics design.

To generalize and predict losses, some have collected sampled measurements for realistic, large-signal operating conditions and abstracted broad capacitor trends as a function of frequency, dc voltage bias, and temperature [42]. Others propose an empirical loss equation for capacitors [110, 75, 111], being the dual of the venerable Steinmetz equation for inductors [163, 179]. These models depend on the capacitor's excitation waveforms, and could directly integrate with a comprehensive component data set to generalize loss, however, this requires more extensive data sampling and more study.

Unavailable Data

Some primary attributes are essentially unavailable in the distributor data set. For instance, the component mass would be invaluable for quantitative evaluation of weight-optimized power conversion systems, however, presently this information is digitally available for only a select few suppliers. To reconcile the deficiency in mass data, Section 2.5 applies sampled measured data to estimate the mass of all capacitor components as a function of its type, rated voltage V_r, and capacitance C.

Summary – Capacitors

Commercially viable capacitors are constructed in a variety of technologies best suited for particular electrical applications [150, 152]. Technologies are most easily distinguished by

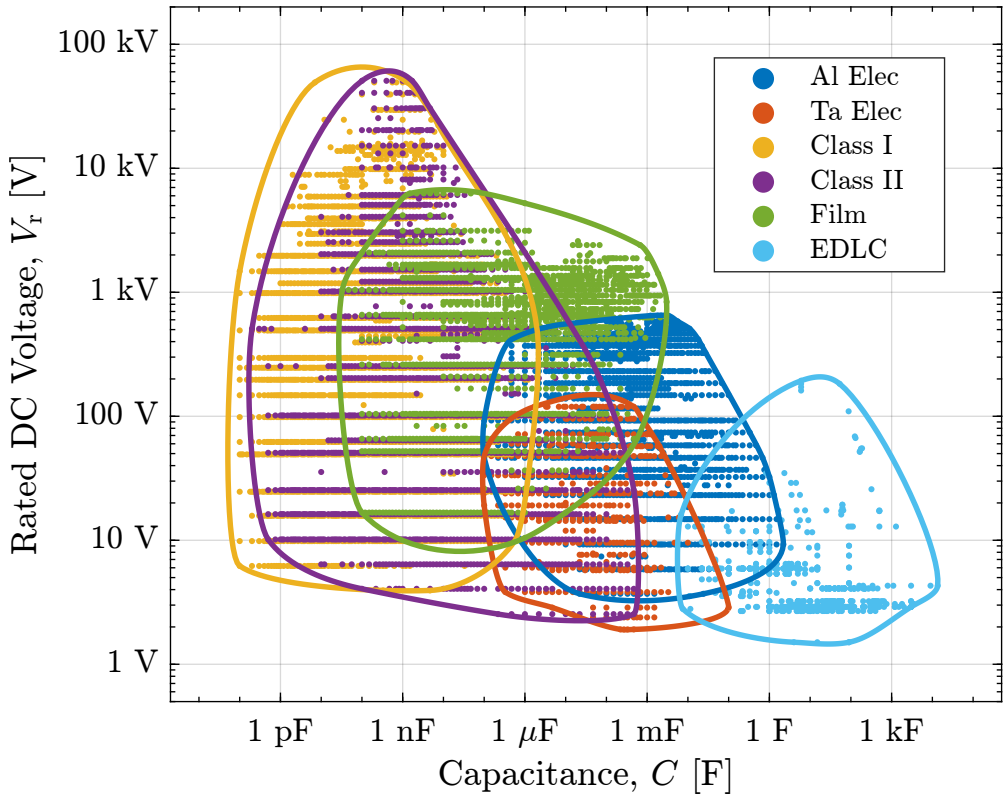


Figure 2.2: Survey of component rated capacitance C versus rated dc voltage V_r across all capacitor technologies including aluminum electrolytic, tantalum electrolytic, Class 1 ceramic, Class II ceramic, film, and electrolytic double-layer capacitors (EDLC).

the dielectric material where certain capacitor types excel in cost, reliability, high-frequency capability, voltage and current ratings, mass, and volume. In this thesis, the capacitors in the comprehensive data set are classified into subsets with distinct elements. Fig. 2.2 illustrates, for the surveyed data, a conventional differentiator between capacitor technologies: the range of possible capacitance C and rated dc voltage V_r.

Aluminum Electrolytic Capacitor

This capacitor technology is voltage unipolar and known for its relatively low cost and weight; and often comes in a can-style package. Relative to other capacitor technologies, aluminum electrolytic capacitors tend to have high values of ESR correlating to the lowest temperature limits of around 85 °C, low current ratings, and shorter lifetime. Aluminum electrolytic capacitors are made in three distinct varieties: 1) the most common liquid (or wet) electrolyte, 2) a solid polymer electrolyte, and 3) a hybrid liquid-solid electrolyte [22].

Tantalum Electrolytic Capacitor

A type of unipolar capacitor rated for lower voltages than aluminum electrolytic capacitors. The rated voltage also derates up to 50% at the maximum rated temperature [65]. Tantalum capacitors are relatively costly yet suitable for high-reliability applications. They are produced in either a 'wet' or solid polymer electrolyte variety.

Ceramic Capacitor

The most prolific capacitor technology in production, having the highest dielectric permittivities and utilized in a broad range of applications [125]. They are bipolar and come in different 'classes' dictated by standards [32]. Class I capacitors are distinctly highly stable with voltage and temperature and are suitable for resonance applications. Class II capacitors have ferroelectric dielectric materials—typically barium titanate dielectric ($BaTiO_3$)—and are more unstable, having a nonlinear capacitance with respect to applied voltage, operating temperature, and degradation with aging, but have the highest capacitance per volume [10, 192]. Class III capacitors are similar to Class II capacitors but have even greater voltage-temperature instability. Colloquially, Class II and Class III capacitors are often both classified as Class II type ceramic capacitors; this chapter employs the same grouping. Although not considered in this chapter, in recent years ceramic capacitors with antiferroelectric dielectric material—namely lead lanthanum zirconate titanate (PLZT)—are becoming increasingly economical and have competitive performance relative to other capacitor types [31, 35, 37]. As Class I and Class II ceramic capacitors differ greatly in performance, they are always explicitly differentiated within this chapter.

Film Capacitor

These capacitors typically have a plastic or polymer dielectric material, the most common being polypropylene (PP) or polyethylene terephthalate (PET), a type of polyester [45]. They are also constructed in metallized and non-metallized variants where the former dominates production and has smaller size, lower costs, and self-healing properties [3]. Compared to other capacitor types, film capacitors are bipolar and generally have large volumes, yet are lightweight and very stable. This chapter classifies all film capacitors into one grouping.

Electrolytic Double-Layer Capacitor (EDLC)

EDLC capacitors, supercapacitors, or ultracapacitors are a unique capacitor technology suited for high-capacity energy storage and applications where batteries would be inconvenient, such as pulsed power. They come in the largest capacitance denominations and are rated for less than 5 V at the device-level [81, 118, 53, 9]. The data set includes EDLC capacitors configured into large series-parallel banks and sold as a single discrete unit.

Other Capacitor Technologies

Niobium electrolytic, mica, and silicon capacitors are other notable capacitor technologies. For these types, the quantity of commercial devices is small and the relevant data is sparse, thus, they are not considered in greater detail within this thesis.

Extent of Available Data – Inductors

Similar to capacitor components, the base attributes for inductors have varying degrees of availability in the comprehensive data set. Data on roughly 88,000 distinct inductors were aggregated in total from the distributor Digikey Electronics.

Fully Available Data

Readily available data includes several primary attributes: inductance at zero bias current L; inductor thermal rated rms current I_{rms} (conventionally at a 40 °C increase in temperature); peak saturation current limit I_{sat} (often defined at either 20% or 40% inductance derating); the dc resistance DCR; the dimensional parameters: length, width, height, diameter; and the cost per unit. The 'box' volume and the rated stored energy E_{r} are calculable in aggregate from these base attributes.

Partially Available Data

The ac quality factor $Q_{\text{ac}} = \frac{2\pi f L}{R_{\text{ac}}}$ FOM quantifies the ideality and damping of the inductor and predicts losses [67]. Manufacturers measure and report Q_{ac} for a small-signal excitation at a singular test frequency f, however, this attribute is only partially available (roughly 60% of aggregated inductors) in the comprehensive data set. Additionally, roughly 20% of surveyed inductors have undefined or poorly defined core material; these were discarded from the analysis.

Unavailable Data

As with capacitors, the component mass of inductors is largely absent from the comprehensive data set. In Section 2.5, sampled measured data is used to estimate the mass of all inductor components as a function of its type, rated current I_{r}, and inductance L.

Summary – Inductors

Analogous to capacitors, inductors are most distinguishable by the type of core material: ferrite, metal, or non-magnetic/air. The core material significantly impacts suitable operating frequency ranges, core losses, and saturation limits for magnetic flux. Fig. 2.3 illustrates the inductance L and rated current I_{r} for each commercial inductor technology.

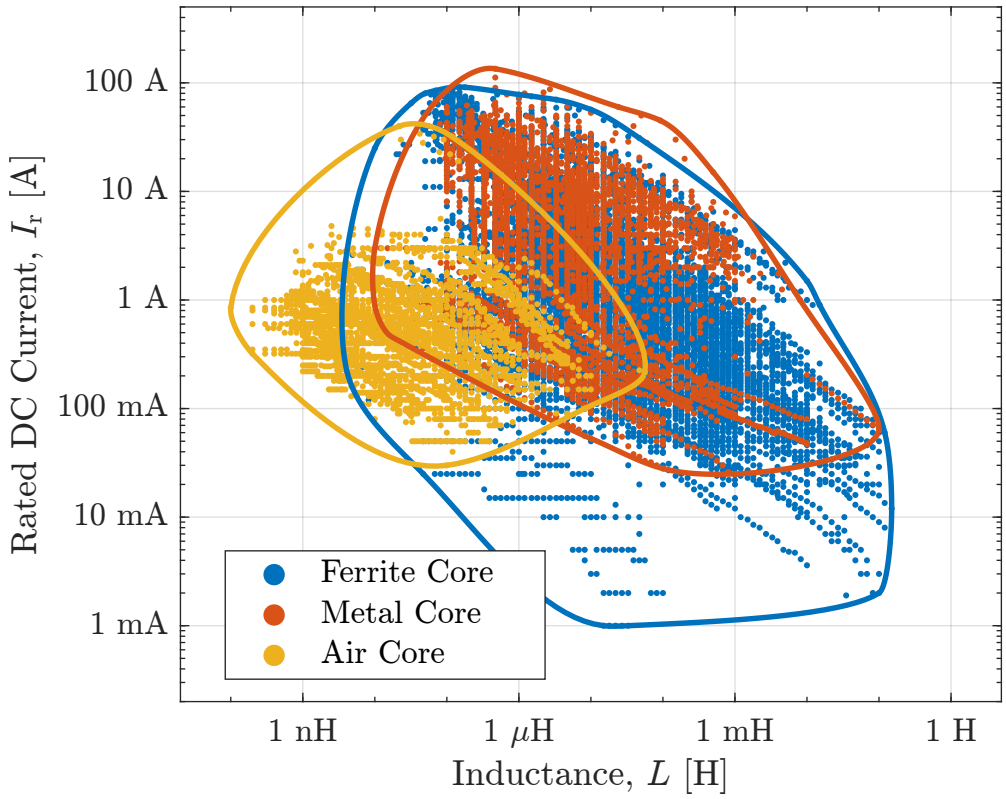


Figure 2.3: Survey of component rated inductance L versus rated dc current I_r across all inductor technologies including ferrite core, metal (including powdered) core, and air core.

Ferrite Core

Ferrite is a ceramic material with relatively high permeability when used in traditional power converter applications. Inductors with a ferrite core come in fixed shapes, have low core losses, and typically have a hard saturation limit with applied current, although soft ferrites are also in use [174, 54].

Metal Core

This core material can consist of ferromagnetic metals or their alloys. The two most common constructions of metal cores in inductors are 1) electrically insulated laminated sheets and 2) a powdered form mixed with epoxy to achieve an effectively distributed air gap with consistent soft-saturation properties [174]; both variants reduce eddy currents compared to a homogeneous metal core. Within this chapter, these magnetizable metal variants are all aggregated and categorized as a single 'metal core' technology.

Air / Ceramic Core

A non-magnetic material such as ceramic, phenolic (polymer), metal (e.g., alumina), and plain air are all classified as 'air core' inductor technology in this chapter. Inductors with non-magnetic cores do not have saturation current limits, but they also have near-unity relative permeability, resulting in lower inductance values.

2.4 Sampled Data and Extrapolation: Stored Energy of Class II Ceramic Capacitors

Class II ceramic capacitors are a unique component type that requires special consideration in data analysis. Their significant voltage, temperature, and age dependence makes the determination of certain metrics circuitous compared to stable capacitor technologies. However, Class II multilayer ceramic chip (MLCC) capacitors are a particularly good capacitor choice for electronics due to their comparatively low losses, high energy density, and widespread applicability [111, 42]. A discussion of the best capacitor technologies is markedly incomplete without the inclusion of this capacitor type, thus intentional effort is exerted to determine their rated stored energy E_r and compute energy density FOM γ.

In this section, an empirically derived fit is shown to accurately estimate the voltage-dependent stored-energy-equivalent capacitance $C_\mathrm{E}(v)$ at any dc voltage v, specifically at the rated dc voltage $v = V_\mathrm{r}$. This fit only depends on the differential capacitance $C(v)$ known at two values: $v = 0\,\mathrm{V}$ and $v = V_\mathrm{r}$. The approximation is validated by using datasheet information from a sampling of 2,550 MLCC capacitors manufactured by the TDK Corporation.

Standards

Class II ceramic capacitors are primarily distinguished by an associated alphanumeric code indicating some information about the temperature characteristic (TC) or temperature-voltage characteristic (TVC). There are three primary standards codifying these nonlinear characteristics:

1. EIA RS-198: the most common in use (e.g., X6S, Y5V, C0G) but only specifies TC information [32].

2. IEC/EN 60384-1: less commonly used (e.g., NP0, 2X1) and specifies information about TC and TVC [56].

3. MIL-C-11015: military standard which specifies TVC information [60].

For all standards, codes indicate information about temperature range, expected capacitance derating at these temperature limits, and expected capacitance derating at rated voltage. Unfortunately, when using the prominent EIA standard, any two capacitors with the same

code (e.g., X6S) and thus similar TC do not necessarily have similar or even necessarily correlated TVC [110].

Defining Capacitance and Stored Energy

Regardless of the TC or TVC, a coherent definition of energy storage for nonlinear capacitors is necessary to eventually deduce energy-related FOM. For a general capacitor, the stored energy E is completely defined at an applied dc voltage V_a as

$$E_\mathrm{a} = E(V_\mathrm{a}) := \int_{q(0)}^{q(V_\mathrm{a})} v \,\mathrm{d}q = \int_0^{V_\mathrm{a}} v\, C(v)\,\mathrm{d}v \tag{2.1}$$

where $C(v)$ is the characteristic incremental, small-signal, or differential capacitance [110, 111, 47, 79] defined as

$$C(v) := \frac{i}{(\frac{\mathrm{d}v}{\mathrm{d}t})} = \frac{\mathrm{d}q}{\mathrm{d}v}. \tag{2.2}$$

For a linear capacitor, the differential capacitance C is constant with applied voltage (and temperature). Thus by evaluating (2.1), the integral equation for stored energy at an applied dc voltage V_a simplifies to

$$E_\mathrm{a,linear} = \frac{1}{2} C V_\mathrm{a}^2 \tag{2.3}$$

which is notably invalid for voltage-dependent capacitors:

$$E_\mathrm{a,nonlinear} \neq \frac{1}{2} C(V_\mathrm{a}) V_\mathrm{a}^2. \tag{2.4}$$

since the $C(v)$ varies with voltage.

The stored energy E_a of a nonlinear capacitance at an applied voltage V_a can instead be equivalently defined using an effective energy-equivalent capacitance C_E at V_a

$$E_\mathrm{a} = \frac{1}{2} C_\mathrm{E}(V_\mathrm{a}) V_\mathrm{a}^2. \tag{2.5}$$

Equating (2.1) and (2.5), the energy-equivalent capacitance $C_\mathrm{E}(v)$ [47] can be computed as a function of the differential capacitance curve $C(v)$:

$$C_\mathrm{E}(V_\mathrm{a}) = \frac{2E_\mathrm{a}}{V_\mathrm{a}^2} = \frac{2}{V_\mathrm{a}^2} \int_0^{V_\mathrm{a}} v\, C(v)\,\mathrm{d}v. \tag{2.6}$$

For linear capacitors with voltage-invariant capacitance C, the energy-equivalent capacitance reduces simply to $C_\mathrm{E} = C$.

Data Acquisition

Within the context of programmatic data acquisition, there are varying degrees of information available that can help determine the energy-equivalent capacitance $C_{\mathrm{E}}(V_{\mathrm{r}})$, and thus rated stored energy E_{r} and energy density γ.

- $C_0 = C(0)$ – The zero-voltage differential capacitance
- V_{r} – Rated dc voltage
- TC – Temperature characteristic code
- TVC – Temperature-voltage characteristic code
- $C(v)$ – Characteristic C-V curve (differential capacitance)
- $C_{\mathrm{r}} = C(V_{\mathrm{r}})$ – Differential capacitance at rated voltage

The first three attributes: C_0, V_{r}, and TC code, are defining characteristics of every capacitor and are readily available in the comprehensive distributor data set. The full $C(v)$ curve as well as differential capacitance C_{r} at rated voltage are not directly available from distributors, however they are often available on datasheets. The TVC code is rarely available anywhere, including datasheets.

The TDK Corporation, a prominent capacitor manufacturer, publicly provides digitized differential capacitance $C(v)$ data for their Class II MLCC components in conjunction with C_0, V_{r}, and TC. Although not a sufficiently comprehensive survey of all Class II ceramics, a sampling of roughly 2,550 TDK Class II MLCC components informs several meaningful insights for the Class II ceramic capacitor technology as a whole.

Stored Energy Approximation: Using Temp. Characteristic

It would be convenient to approximate rated energy E_{r} in (2.1) or the rated energy-equivalent capacitance $C_{\mathrm{E}}(V_{\mathrm{r}})$ in (2.6) without express requirement of the entire $C(v)$ characteristic curve which cannot presently be attained en masse. One potential method is to identify general trends in the $C(v)$ curves of capacitors with specific temperature characteristics (e.g., X6S, X7R). For instance, X6S capacitors could have an approximate 70-90% capacitance derating at V_{r}, whereas X5R capacitors could have an approximate 60-70% capacitance derating. Such an identifiable relationship would aid estimation of E_{r} with sparse information. Prior work has investigated the existence of a practicable linkage between TC and capacitance-voltage dependence [122, 176].

The relative shapes and values of the $C(v)$ curves are aggregately visualized in Fig. 2.4 to identify patterned correlations with the TC and determine whether a TC-dependent scheme has plausible utility. All C-V curves are normalized as $C(v)/C(0)$, and the differential capacitances generally derate with a characteristic logistic or mirrored 'S' shape (for a log-linear plot). Visual inspection yields some groupings or families of $C(v)$ curves for similar

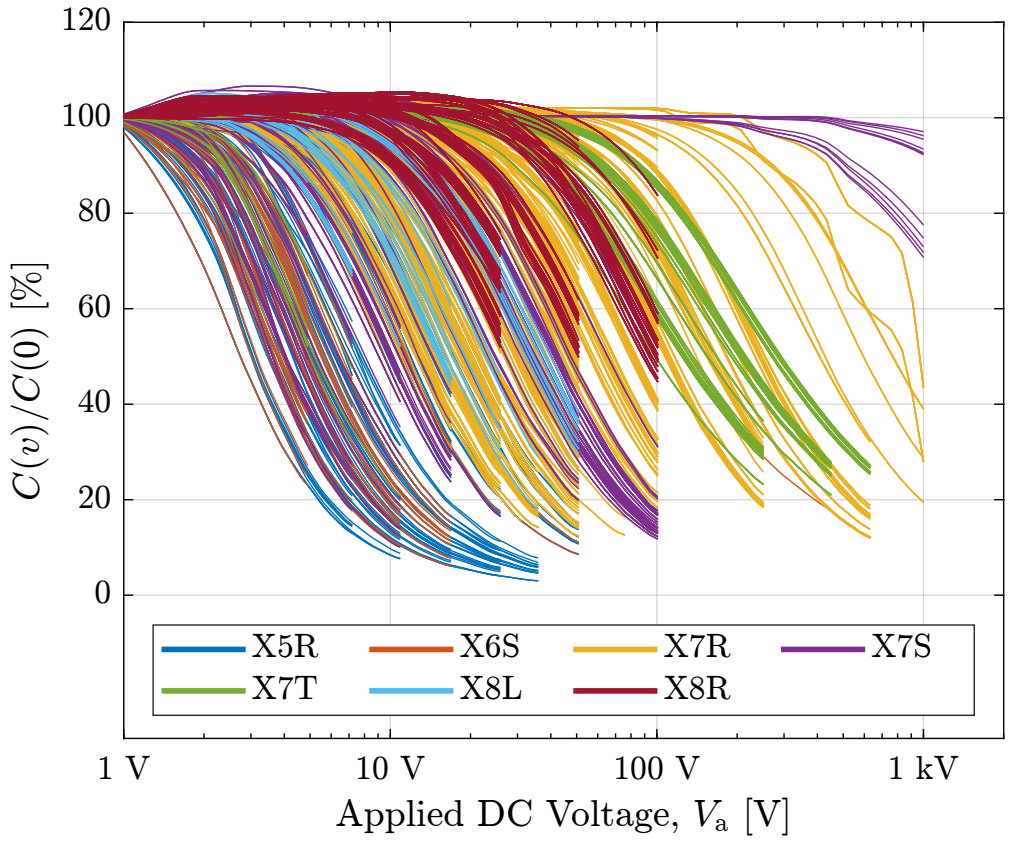


Figure 2.4: Applied dc voltage V_a versus normalized differential capacitance $C(v)/C(0)$ and distinguished by temperature characteristic. Data is sampling of 2,550 TDK Class II MLCC capacitors.

TC indicating similar dielectric materials, however they are not visibly distinctive enough to determine any generalized correlations between TC and $C(v)$; consequently, a different method must be employed to approximate E_r.

Stored Energy Approximation: Using $C(0)$ and $C(V_a)$

The effective energy-equivalent capacitance $C_E(V_a)$ at applied voltage V_a could possibly be estimated knowing only at most two values: $C(0)$ and $C(V_a)$. Different approximations of $C_E(V_a)$ are presented and evaluated compared to the exact value in (2.6).

Table 2.2: Percentage Error for $C_{\mathrm{E}}(V_{\mathrm{r}})$ Approximations

Error	$C(0)$	$C(V_{\mathrm{r}})$	$\frac{2}{3}C(V_{\mathrm{r}}) + \frac{1}{3}C(0)$	$M_{-0.5}\big(C(0), C(V_{\mathrm{r}})\big)$
Mean	98.8%	32.4%	16.0%	3.1%
Median	64.3%	33.9%	5.2%	1.8%

Zeroth-order approximation

Most simply, the energy-equivalent capacitance C_{E} at an applied voltage V_{a} can be approximated evaluating $C(v)$ at its limits as

$$C_{\mathrm{E}}(V_{\mathrm{a}}) \approx C(0) \tag{2.7}$$

or as

$$C_{\mathrm{E}}(V_{\mathrm{a}}) \approx C(V_{\mathrm{a}}). \tag{2.8}$$

These estimates roughly serve as upper and lower bounds, respectively, on the actual $C_{\mathrm{E}}(V_{\mathrm{a}})$.

First-order approximation

For this approximation of $C_{\mathrm{E}}(v)$ the differential capacitance $C(v)$ is approximated by a linear fit, or first-order approximation, between the zero-voltage capacitance $C(0)$ and the differential capacitance at the applied voltage $C(V_{\mathrm{a}})$.

$$C(v) \approx \frac{C(V_{\mathrm{a}}) - C(0)}{V_{\mathrm{a}} - 0} v + C(0) \tag{2.9}$$

Directly evaluating (2.6) using (2.9) yields

$$C_{\mathrm{E}}(V_{\mathrm{a}}) \approx \frac{2}{3}C(V_{\mathrm{a}}) + \frac{1}{3}C(0). \tag{2.10}$$

Power mean approximation

Finally, $C_{\mathrm{E}}(V_{\mathrm{a}})$ is approximated with a special average function. The power mean (or Hölder mean) M_p is a family of functions which averages n positive numbers $x_1, x_2, ..., x_n$ as

$$M_p\left(x_1, x_2, ..., x_n\right) := \left(\frac{x_1^p + x_2^p + ... + x_n^p}{n}\right)^{\frac{1}{p}} \tag{2.11}$$

where the exponent p is some real nonzero number [27, 172]. This power mean is equivalent to other well-known means for particular values of p: the arithmetic mean for $p = 1$, the

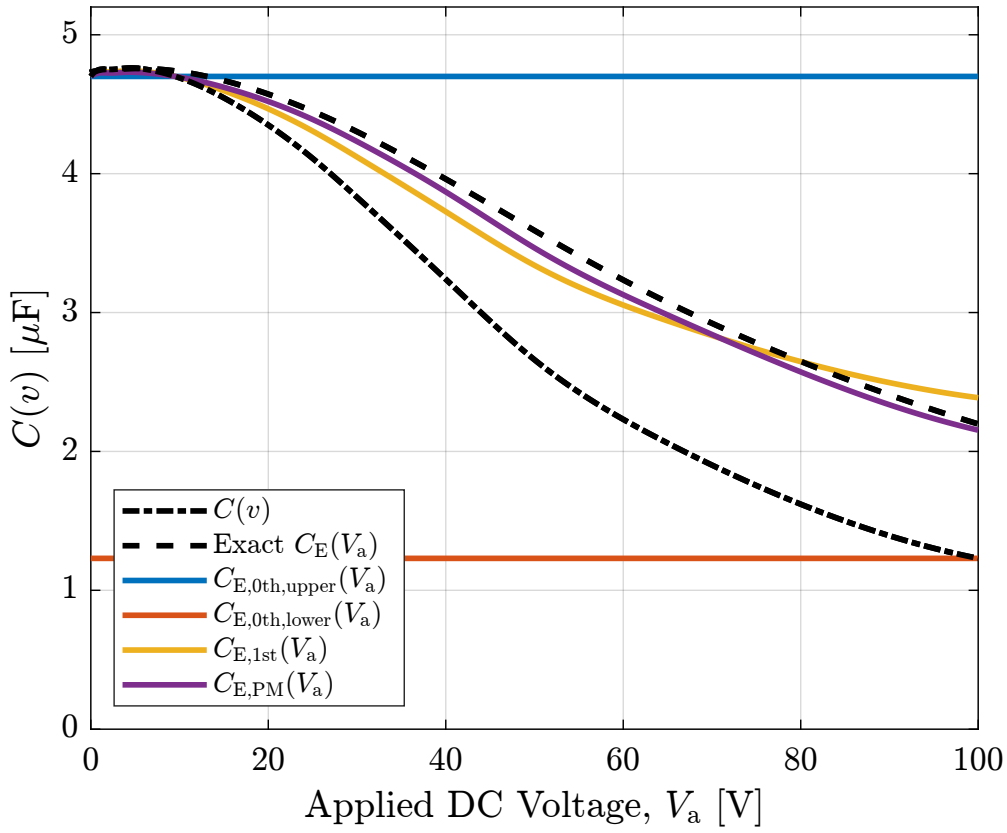


Figure 2.5: Applied dc voltage versus differential capacitance $C(v)$ for C5750X7R2A475K230KA device: $C(0) = 4.7\,\mu\text{F}$, $V_r = 100\,\text{V}$, X7R. Demonstrates comparison of approximations for energy-equivalent capacitance $C_E(V_a)$.

quadratic mean or root mean square (RMS) for $p = 2$, and the harmonic mean for $p = -1$; it is also related to the ℓ^p-norm of a vector for integer $p \geq 1$ [165];

A good value of p results in the best approximation of $C_E(V_a)$ at every applied dc voltage $0 < V_a < V_r$ utilizing only the endpoints of the differential capacitance curve $C(0)$ and $C(V_a)$ or as $C_E(V_a) \approx M_p(C(0), C(V_a))$. Using (2.6), the energy-equivalent capacitances at rated voltage $C_E(V_r)$ are computed for all 2,550 sampled Class II MLCC capacitors from TDK. Then regression is applied to fit this data to (2.11) yielding a best fit value $p = -0.504 \approx -0.5$ and an empirically derived approximation

$$\begin{aligned} C_E(V_a) &\approx M_{-0.5}\big(C(0), C(V_a)\big) \\ &= \frac{4C(0)C(V_a)}{\Big(\sqrt{C(0)} + \sqrt{C(V_a)}\Big)^2}. \end{aligned} \tag{2.12}$$

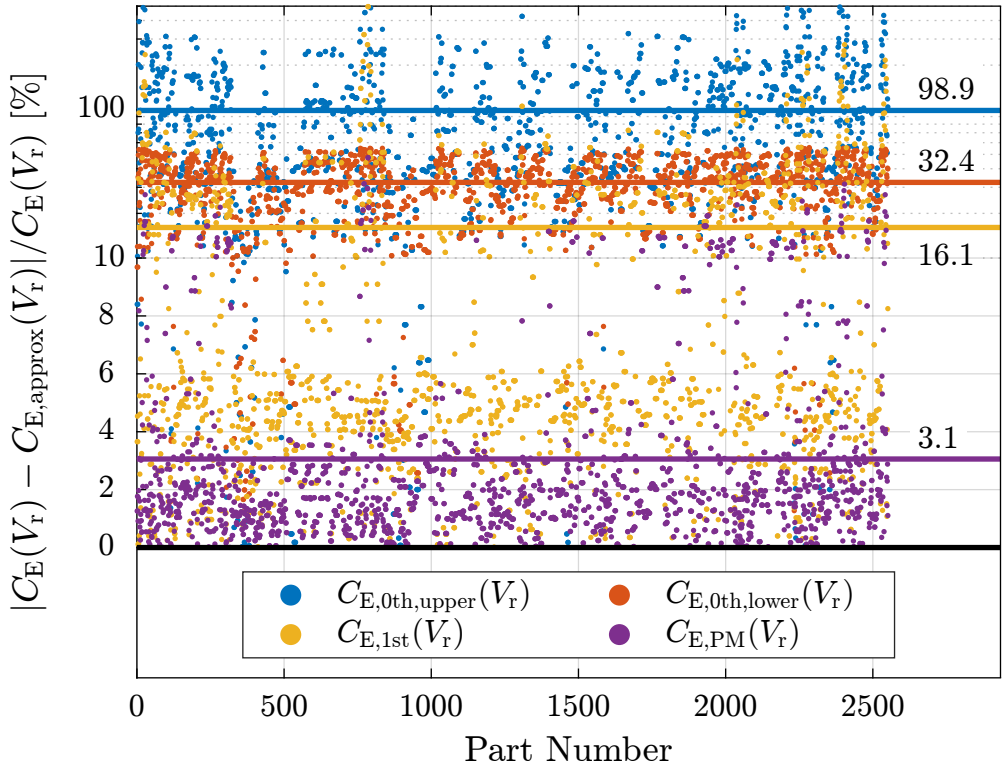


Figure 2.6: Percentage error for approximations of energy-equivalent capacitance $C_{\mathrm{E}}(V_{\mathrm{r}})$ at rated dc voltage V_{r}. Solid horizontal lines indicate the mean percentage error for each corresponding approximation. Data is sampling of 2,550 TDK Class II MLCC capacitors.

Results

All $C_{\mathrm{E}}(v)$ approximations are graphically compared for a particular device in Fig. 2.5 across applied voltage V_{a}. From inspection, the proposed first-order and power mean approximations in (2.10) and (2.12) very nearly match the general waveshape of the actual $C_{\mathrm{E}}(v)$ curve evaluated from (2.6).

To prove their efficacy, these estimates must also be validated for the entire sampled data set—not just a single component. The relative accuracy of an estimate is judged by its mean percentage error

$$\mathrm{MPE} = \frac{1}{N}\sum_{i=1}^{N}\frac{|x_{\mathrm{actual},i} - x_{\mathrm{predicted},i}|}{x_{\mathrm{actual},i}} \tag{2.13}$$

for N elements in a set where $x = C_{\mathrm{E}}(V_{\mathrm{r}})$. Fig. 2.6 presents the percentage error of each $C_{\mathrm{E}}(v)$ approximation for all 2,550 sampled TDK components; the resulting mean and median percentage error of each approximation are tabulated in Table 2.2. The zeroth-order

approximations (2.7) and (2.8) result in prohibitively high estimation inaccuracy, but the power mean approximation in (2.12) has a low MPE of 3.1% (median percentage error of 1.8%), sufficiently validating its usage amongst the others.

This method suggests if ever a manufacturer, supplier, or distributor reports the differential capacitance values of Class II ceramic capacitors at both zero dc voltage bias $C(0)$ and at rated dc voltage bias $C(V_\mathrm{r})$, then the rated stored energy E_r, and consequently energy densities γ, at rated voltage V_r could be estimated with a relatively high degree of accuracy using (2.12) without requiring the full $C(v)$ curve, temperature characteristic, or temperature-voltage characteristic.

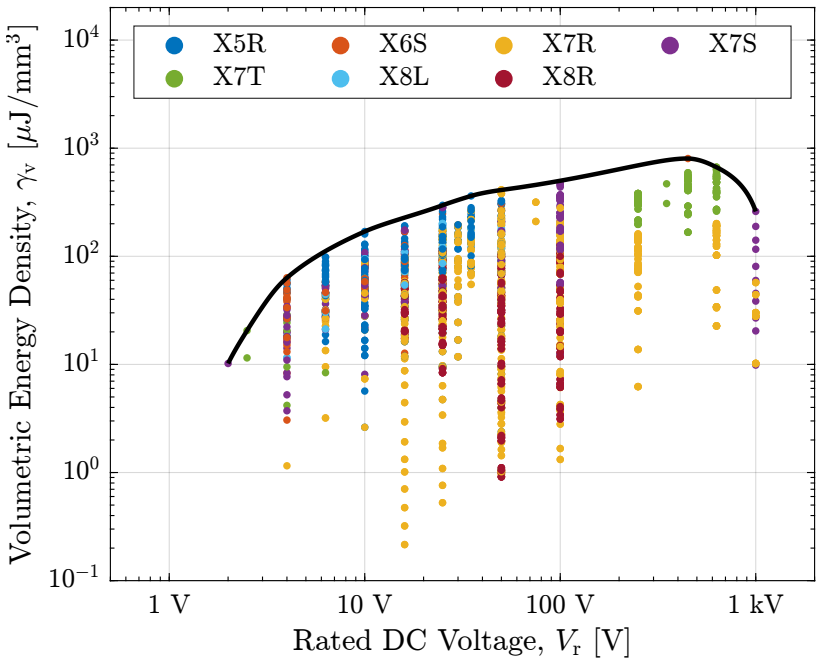
Investigating Energy Density FOM of Sampled Data

The FOM framework proposed in Secion 2.2 can be applied to the sampled TDK data set. The exact rated stored energy E_r, as well as the volumetric energy density $\gamma_\mathrm{v} = \frac{E_\mathrm{r}}{\mathrm{Vol}}$, of each capacitor is computed as (2.1). Recall that the series-parallel modularity invariance property of a FOM allows every capacitor, regardless of rated voltage, to be fairly compared.

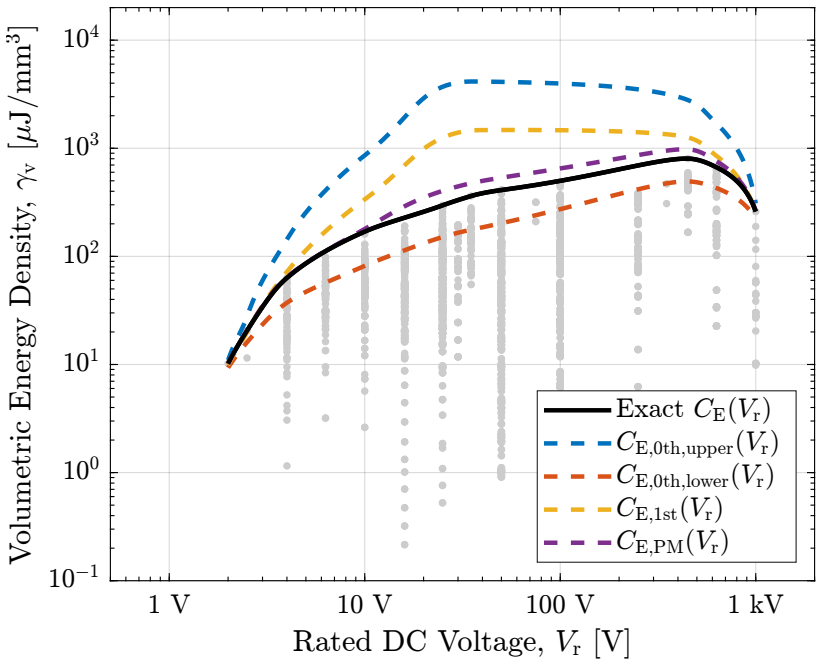
Fig. 2.7 shows the consequent impact of TC and energy-equivalent capacitance $C_\mathrm{E}(V_\mathrm{r})$ approximation on γ_v with respect to rated voltage V_r. Despite some TC clustering, the relationship between TC and γ_v in Fig. 2.7a is not correlative enough to predict a TC code that has the smallest volume nor the γ_v of any individual capacitor based on its TC. The associated Pareto fronts for each approximation method are also included relative to the exact Pareto front of volumetric energy density γ_v in Fig. 2.7b. If using the simplest zeroth-order approximation in (2.7), the highest energy density capability of Class II ceramic capacitors can be overestimated by as much as 1000×. The recommended power approximation in (2.12) sufficiently estimates γ_v.

Extrapolating Sampled Data to the Full Data Set

This analysis concludes that energy storage estimation of Class II ceramic capacitors is possible if the differential capacitance at two voltages, 0 V and V_a, are known. However, as previously mentioned, the comprehensive data set only contains $C(0)$ data for all capacitors. Thus for the remainder of this chapter, the energy equivalent capacitance $C_\mathrm{E}(V_\mathrm{r})$ at rated voltage is uniformly approximated as 60 % of $C(0)$—an improvement over the zeroth-order estimate in (2.7)—to estimate the rated energy storage E_r of Class II ceramic capacitors. This approximation has a mean percentage error MPE of 40% applied to the TDK data set. This is an inaccurate and dissatisfying estimate, but reasonable considering the logarithmically wide breadth in energy densities across the technology as shown in Fig. 2.7. If capacitor manufacturers, suppliers, and distributors begin to report values for $C(V_\mathrm{r})$—doubly useful because it conveys small-signal capacitance at rated voltage—then $C_\mathrm{E}(V_\mathrm{r})$ can be estimated with a high degree of accuracy using the power mean in (2.12), fully enabling estimation of rated energy storage E_r for all capacitors, both linear and nonlinear, and satisfyingly quantifying those device FOM related to energy.



(a)



(b)

Figure 2.7: Rated dc voltage V_r versus volumetric energy density γ_v for TDK Class II MLCC capacitors where (a) components are delineated by temperature characteristics and (b) the Pareto front varies depending on the approximation for $C_E(V_r)$.

2.5 Sampled Data and Extrapolation: Capacitor and Inductor Mass

Although minimized volume and cost are often desired, minimizing the system mass can also be a critical need for electronics applications. In particular, innovations in the mass reduction for mobile electronics—most commonly electric aircraft or automobiles—are driven by sustainable energy targets for the growing electric propulsion industry [104, 184]. Electronics for space applications also prioritize lightweight designs. In these applications, even the choice of converter topology is informed by the achievable mass of the system and the requisite masses of the constituent devices [124, 117, 43, 44]. The mass of commercially available capacitors and inductors remains largely indeterminable en masse as few manufacturers supply this information. Thus, an insufficient proportion of component mass is known for the comprehensive data set surveyed in this work.

This section summarizes the analysis introduced in [203] and expounded in [25]. Determining the volumetric mass density (mass per volume) D of a broadly sampled set of passive devices through measurement yields sufficient information to extrapolate and transform readily available volume data to an estimated value of mass for each component. These works present generic fits for both capacitor and inductor density D, with relevant empirical parameters provided for all major capacitor and inductor technologies as described in Section 2.3.

FOM Transformation – Theory

The volumetric mass density (or density) of any component

$$D = \frac{\text{Mass}}{\text{Vol}} \tag{2.14}$$

is an intrinsic FOM relating its mass to its volume. Incidentally, the density D (as well as mass) for every component in the comprehensive data set is unknown. However, a single estimated value of D may apply to an entire component technology by relying on homogeneity in material composition and construction. This value of D can be further refined by empirically fitting its dependence to known component attributes: the capacitance C and rated dc voltage V_r for capacitors, and inductance L and rated dc current I_r for inductors. Once a reliably accurate density mapping D is known, then a volume-related FOM for an individual component can be transformed into a mass-related FOM as

$$\gamma_\text{m} = \frac{1}{D}\,\gamma_\text{v}. \tag{2.15}$$

The volumetric energy density FOM γ_v for each passive component is defined as a ratio of rated energy E_r and volume:

$$\gamma_\text{v} = \frac{E_\text{r}}{\text{Vol}} \tag{2.16}$$

whereas the gravimetric energy density FOM γ_{m} is defined as a ratio of rated energy E_{r} and mass:

$$\gamma_{\mathrm{m}} = \frac{E_{\mathrm{r}}}{\mathrm{Mass}}. \tag{2.17}$$

The rated stored energy metric E_{r} is computed for capacitors from the energy-equivalent capacitance C_{E} in (2.6) and rated dc voltage V_{r}

$$E_{\mathrm{r}} = \frac{1}{2} C_{\mathrm{E}}(V_{\mathrm{r}}) V_{\mathrm{r}}^2 \tag{2.18}$$

and is computed for inductors from the inductance L and rated dc current I_{r}

$$E_{\mathrm{r}} = \frac{1}{2} L I_{\mathrm{r}}^2 \tag{2.19}$$

The inductor's rated dc current I_{r} is defined as the minimum of the thermal rms current rating I_{rms} and the peak saturation current rating I_{sat} as specified on the datasheet, or

$$I_{\mathrm{r}} = \min(I_{\mathrm{rms}}, I_{\mathrm{sat}}). \tag{2.20}$$

Empirically Fitting Density Measurements

Two empirically derived fits are proposed by utilizing the measured density data: 1) a mean or constant fit and 2) a power fit dependent on base electrical attributes.

Mean Fit Estimate

Passive components are separated by type, then a mean fit for density D is calculated for each with a zeroth-order linear regression. These mean densities are indicated in Table 2.3. By ranking of least to most dense, the component technologies are ordered as film capacitor, air core inductor, aluminum electrolytic capacitor, ferrite core inductor, tantalum electrolytic capacitor, Class I ceramic capacitor, metal core inductor, and Class II ceramic capacitor.

The relative accuracy of a fit is judged by its mean percentage error MPE defined in (2.13) where x is the density D. The computed MPE is less than 30% for every mean fit tabulated in Table 2.3, indicating a fairly accurate fit between the measured and the mean fit approximation. The MPE can be further reduced by utilizing a more accurate power fit model dependent on base component attributes (e.g., C, V_{r}, L, I_{r}) fully available in the comprehensive data set as described in Section 2.3.

Power Fit Estimate

Taking inspiration from classical empirical fits for loss in passive components [111, 179] while remaining conscientious of statistical uncertainty in inferential models [33], a power fit expression for density D is expressed as

$$D = k \cdot V_{\mathrm{r}}^{\alpha} \cdot C^{\beta} \quad \left[\frac{\mathrm{mg}}{\mathrm{mm}^3}\right] \tag{2.21}$$

with inputs V_r and C, and empirical parameters k, α, and β. An analagous power fit expression is proposed for inductors

$$D = k \cdot I_\mathrm{r}^{\alpha} \cdot L^{\beta} \quad \left[\frac{\mathrm{mg}}{\mathrm{mm}^3}\right] \tag{2.22}$$

with inputs rated dc current I_r and inductance L, and similar empirical parameters k, α, and β.

Linear regression, applied to the logarithm of 2.21 and 2.22, is used to determine the best fit parameters k, α, and β which minimize the MPE [2]. Table 2.3 tabulates the resultant parameters of the power fit for each component technology as well as the associated statistical p-values and mean percentage error MPE.

The p-value indicates the occurrence probability of the best-fit parameters when assuming the null hypothesis—in this case, a constant fit D with $\alpha = 0$ and $\beta = 0$—to be true. All statistical p-values—except for ferrite and air core inductors—are much lower than a typical significance threshold of 0.05, confirming the modeled power fits, with the specified parameters, are statistically significant [62].

FOM Transformation – Application

Now buttressed with substantive estimates for component density D, the transformation theory introduced in Section 2.5 is applied to extrapolate box volume to mass for the comprehensive passive component data set introduced in Section 2.3.

Table 2.3: Results of proposed mean fit and empirical power fit for capacitor/inductor volumetric mass density (mass/volume).

		Mean Fit		Power Fit				
Component Technology	Quantity	$D\left[\frac{\text{mg}}{\text{mm}^3}\right]$	**MPE**	k	α	β	p-value	**MPE**
Aluminum Electrolytic Capacitor	47	1.49	**9.16%**	1.522	-0.0710	-0.0257	4.29e-04	**7.80%**
Tantalum Electrolytic Capacitor	64	3.38	**12.87%**	4.928	0.0482	0.0498	4.40e-08	**8.49%**
Class I Ceramic Capacitor	46	4.39	**13.97%**	11.66	0.0558	0.0665	1.02e-09	**10.0%**
Class II Ceramic Capacitor	66	5.41	**10.17%**	8.406	-0.0045	0.0272	1.29e-04	**8.46%**
Film Capacitor	92	1.26	**7.70%**	1.152	-0.0411	-0.0222	1.44e-08	**5.98%**
Ferrite Core Inductor	34	3.12	**21.03 %**	2.385	-0.0466	-0.0280	0.5029	**19.86%**
Metal Core Inductor	87	5.04	**11.90%**	7.330	0.0903	0.0464	4.83e-14	**7.71%**
Air Core Inductor	11	1.45	**25.45 %**	1.951	0.1659	0.0453	0.0250	**14.40 %**

2.6 Analyzing the Data

The comprehensive data set of commercial passive components has been clearly defined and its energy and mass deficiencies bolstered in Section 2.4 and Section 2.5, respectively. With this foundation set and a utilitarian FOM framework established, the data can be freely interpreted and analyzed. It is possible to infer fundamental limitations intrinsic to a component technology as well as quantified comparisons between technologies, even between capacitors and inductors. The prototypical question posed in Section 2.2 ("Based on the present available technology, the smallest possible capacitor solution for this application has volume X.") now has a determinable answer. From Fig. 2.8, Class II ceramic capacitors are the capacitor technology with the smallest volume (with respect to energy storage), since they have the highest volumetric energy density. Similar quantifiably supported claims will be made throughout this section, including application to optimally choosing capacitors (or inductors) with an overrated voltage (or current).

Capacitor Voltage Overrating

For an applied capacitor voltage V_a, selecting a capacitor with a greater rated voltage V_r—called 'voltage overrating'—is often necessary depending on temperature and lifetime requirements [4] but, interestingly, can also be worthwhile to improve the realized capacitor volume, mass, or cost. The following analysis quantitatively determines when this design strategy has likely volume, mass, or cost benefit.

Recall from (2.3), the stored energy in a particular (linear) capacitor at an applied voltage V_a is expressed as

$$E_\mathrm{a} = \frac{1}{2} C V_\mathrm{a}^2 \tag{2.23}$$

thus the consequent applied volumetric energy density $\gamma_{\mathrm{v,a}}$ of the *underutilized* capacitor is

$$\gamma_{\mathrm{v,a}}(V_\mathrm{a}) = \frac{E_\mathrm{a}}{\mathrm{Vol}} = \frac{\gamma_\mathrm{v}}{V_\mathrm{r}^2} V_\mathrm{a}^2. \tag{2.24}$$

This derated energy density $\gamma_{\mathrm{v,a}}$ scales quadratically with the applied voltage V_a justifying its $+40\,\mathrm{dB}$/decade slope indicated by the dashed lines in Fig. 2.8.

Besides enabling juxtaposition of individual capacitors, the empirical data also indicates the peak performance capability of the whole technology. The 'best' capacitor has the best FOM and lies on the Pareto front of the comprehensively surveyed data set. Figure 2.8 illustrates the empirically derived Pareto fronts $f_\mathrm{P}(V_\mathrm{r})$ for volumetric energy density γ_v as a function of rated voltage V_r for major capacitor technologies: aluminum electrolytic, tantalum electrolytic, Class I ceramic, Class II ceramic, and film. For each capacitor data set, the derivative of its Pareto curve $f'_\mathrm{P}(V_\mathrm{r})$ can exceed $\gamma'_{\mathrm{v,a}}(V_\mathrm{a})$, the derivative of the derated

Table 2.4: Summary of Critical Voltages for Capacitor Overrating

	Al Elec	Ta Elec	Class I	Class II	Film
Volume	N/A	5 V	10 V	5 V	11 V
Mass	N/A	5 V	10 V	5 V	12 V
Cost	12 V	4 V	12 V	4 V	300 V

energy density curve in (2.24), below a specific critical rated voltage $V_{\mathrm{r,crit}}$:

$$f'_{\mathrm{P}}(V_{\mathrm{r}}) > \gamma'_{\mathrm{v,a}}(V_{\mathrm{a}}) = \frac{\mathrm{d}}{\mathrm{d}V_{\mathrm{a}}}\left(\frac{\gamma_{\mathrm{v}}}{V_{\mathrm{r}}^2}V_{\mathrm{a}}^2\right) = \frac{2\gamma_{\mathrm{v}}}{V_{\mathrm{r}}^2}V_{\mathrm{a}}. \tag{2.25}$$

Evaluating this inequality for components on the Pareto curve ($\gamma_{\mathrm{v}} = f_{\mathrm{P}}(V_{\mathrm{r}})$) and at a rated voltage application ($V_{\mathrm{a}} = V_{\mathrm{r}}$) yields

$$f_{\mathrm{P}}(V_{\mathrm{r,crit}}) = \frac{1}{2}V_{\mathrm{r,crit}}\, f'_{\mathrm{P}}(V_{\mathrm{r,crit}}). \tag{2.26}$$

The critical rated voltage $V_{\mathrm{r,crit}}$ is the rated voltage satisfying this equality comprised of the Pareto curve and its gradient.

In Figure 2.8, every capacitor (not just Pareto optimal components) with voltage rating less than the critical inflection point $V_{\mathrm{r}} < V_{\mathrm{r,crit}}$ has a larger volume than the highest volumetric energy density γ_{v} capacitor with rated voltage $V_{\mathrm{r}} = V_{\mathrm{r,crit}}$ when derated to any applied voltage. In summary to minimize volume, an overrated capacitor with $V_{\mathrm{r}} = V_{\mathrm{r,crit}}$ should always be sought when $V_{\mathrm{a}} < V_{\mathrm{r,crit}}$. For capacitors with rated voltages above this critical inflection point $V_{\mathrm{r}} > V_{\mathrm{r,crit}}$, it is preferable to avoid voltage derating beyond that which is practically necessary; the volume-minimized capacitor has a voltage rating nearer to the applied voltage or $V_{\mathrm{r}} = V_{\mathrm{a}}$.

A similar process yields the critical rated voltage for the gravimetric (or specific) energy density $\gamma_{\mathrm{m}} = \frac{E_{\mathrm{r}}}{\mathrm{Mass}}$ and the energy per cost $\gamma_{\mathrm{c}} = \frac{E_{\mathrm{r}}}{\mathrm{Cost}}$ as shown in Fig. 2.9 and Fig. 2.10, respectively. All critical rated voltages $V_{\mathrm{r,crit}}$ for energy density γ with respect to volume, mass, and cost are tabulated in Table 2.4. Inspection of Fig. 2.8 reveals aluminum electrolytic capacitors notably do not have a critical rated voltage with respect to volume or mass, thus efficient component selection should nearly always adhere to $V_{\mathrm{r}} = V_{\mathrm{a}}$ for this capacitor technology. Interestingly, Fig. 2.10 reveals that film capacitors with $V_{\mathrm{r}} < 300\,\mathrm{V}$ should not be selected to minimize cost since the best $V_{\mathrm{r}} = 300\,\mathrm{V}$ device proves to be more cost effective, even when derated to lower voltages.

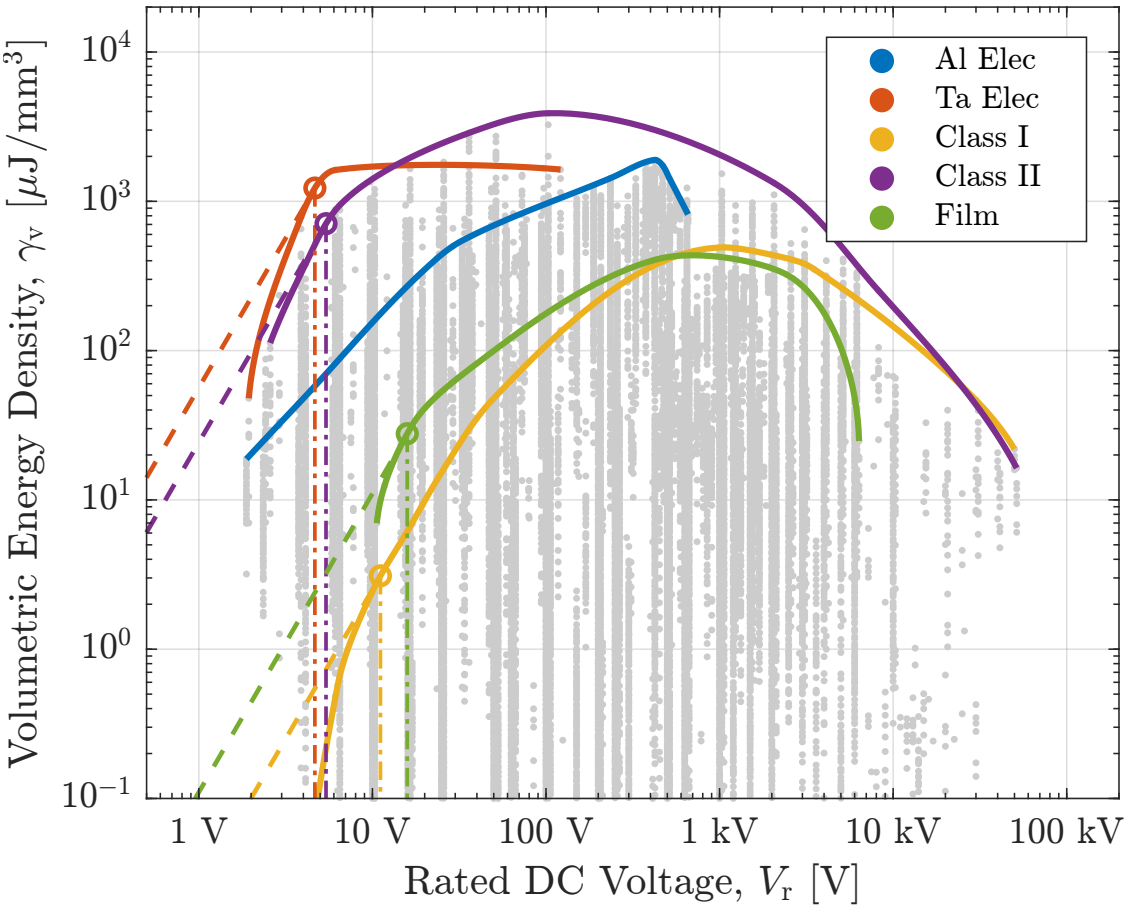


Figure 2.8: Commercial capacitor volumetric energy density FOM γ_v across rated dc voltage V_r. The Pareto fronts are highlighted as well as the critical rated voltage $V_{r,crit}$ where capacitor overrating becomes useful.

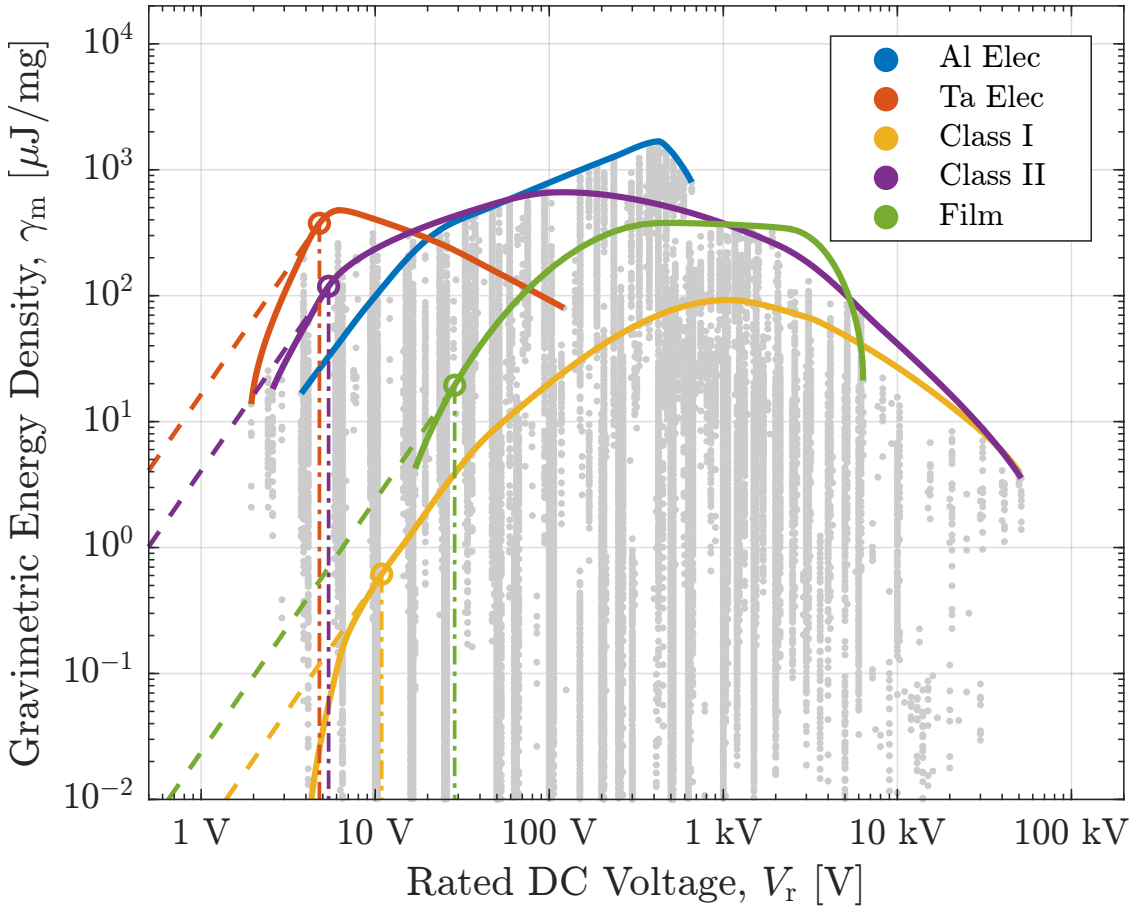


Figure 2.9: Commercial capacitor gravimetric energy density FOM γ_m across rated dc voltage V_r. The Pareto fronts are highlighted as well as the critical rated voltage $V_{r,crit}$ where capacitor overrating becomes useful.

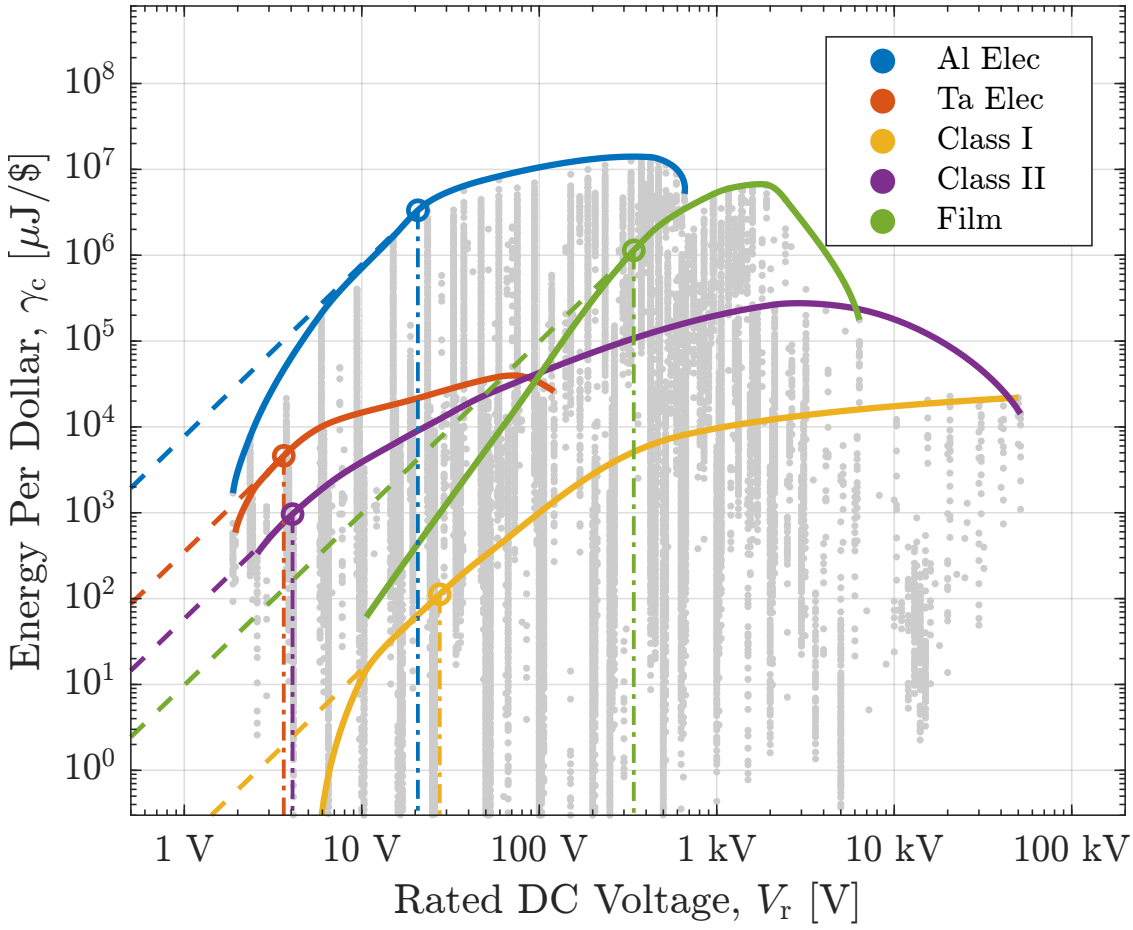


Figure 2.10: Commercial capacitor energy per cost FOM γ_c across rated dc voltage V_r. The Pareto fronts are highlighted as well as the critical rated voltage $V_{r,crit}$ where capacitor overrating becomes useful.

Capacitor Energy Density

The comprehensive data allows consideration of energy density trends in particular capacitor technologies. For instance, as mentioned in [150], the achievable volumetric and gravimetric energy density γ_v and γ_m of aluminum electrolytic capacitors approximately increases linearly with rated voltage V_r; this trend is confirmed by the Pareto fronts (for $V_\mathrm{r} < 450\,\mathrm{V}$) in Fig. 2.8.

The acquired data also allows comparison in the energy storage capabilities of different capacitor technologies. The Pareto curves in Fig. 2.8, 2.9, and 2.10 indicate certain capacitor technologies dominate at various rated voltages with respect to volume, mass, and cost. For $V_\mathrm{r} < 10\,\mathrm{V}$, tantalum electrolytic capacitors have the largest energy densities and thus the smallest volume and mass. In the $10\,\mathrm{V} < V_\mathrm{r} < 700\,\mathrm{V}$ range, aluminum electrolytic capacitors are the lightest and Class II ceramic capacitors are the smallest. Above $V_\mathrm{r} > 1\,\mathrm{kV}$, both Class II ceramic and film capacitors are superior with respect to mass, while only Class II ceramic capacitors are superior with respect to volume. Aluminum electrolytic capacitors are the lowest cost solution to fulfill system energy requirements for $V_\mathrm{r} < 700\,\mathrm{V}$ as claimed in [150, 22], whereas film capacitors are the lowest cost for $700\,\mathrm{V} < V_\mathrm{r} < 6\,\mathrm{kV}$, and ceramics are the lowest cost for $V_\mathrm{r} > 6\,\mathrm{kV}$. Class I ceramic capacitors are ubiquitously poor performers with respect to energy density except at the highest rated voltages $V_\mathrm{r} > 10\,\mathrm{kV}$.

Inductor Current Overrating

The comprehensive data set can also produce the conditions for useful inductor current overrating. By following an analogous derivation as Section 2.6, the critical rated current $I_\mathrm{r,crit}$ is derived for ferrite, metal, and air core inductor technologies since the energy stored in a linear inductor at an applied dc current I_a is

$$E_\mathrm{a} = \frac{1}{2} L I_\mathrm{a}^2. \tag{2.27}$$

Fig. 2.11, 2.12, and 2.13 illustrates the technological subsets and their Pareto fronts for rated current I_r versus volumetric energy density γ_v, gravimetric energy density γ_m, and energy per cost γ_c, respectively. Table 2.5 tabulates the resulting critical current ratings $I_\mathrm{r,crit}$ for each technology, i.e., the lower limit below which no advantage is gained for devices with a reduced current rating.

Inductor Energy Density

The comprehensive data reveals the energy storage capabilities of inductors with respect to core material. Ferrite cores are the most energy-dense core type with respect to mass. With respect to volume and cost, ferrite core inductors are the most energy-dense for rated current $I_\mathrm{r} < 1\,\mathrm{A}$, while above $I_\mathrm{r} > 1\,\mathrm{A}$, both ferrite and metal core technologies dominate. The best air core inductors have a consistent 10–100× lower energy density (with respect to volume,

Table 2.5: Summary of Critical Currents for Inductor Overrating

	Ferrite	Metal	Air
Volume	2.0 mA	N/A	60 mA
Mass	2.5 mA	N/A	65 mA
Cost	20 mA	150 mA	200 mA

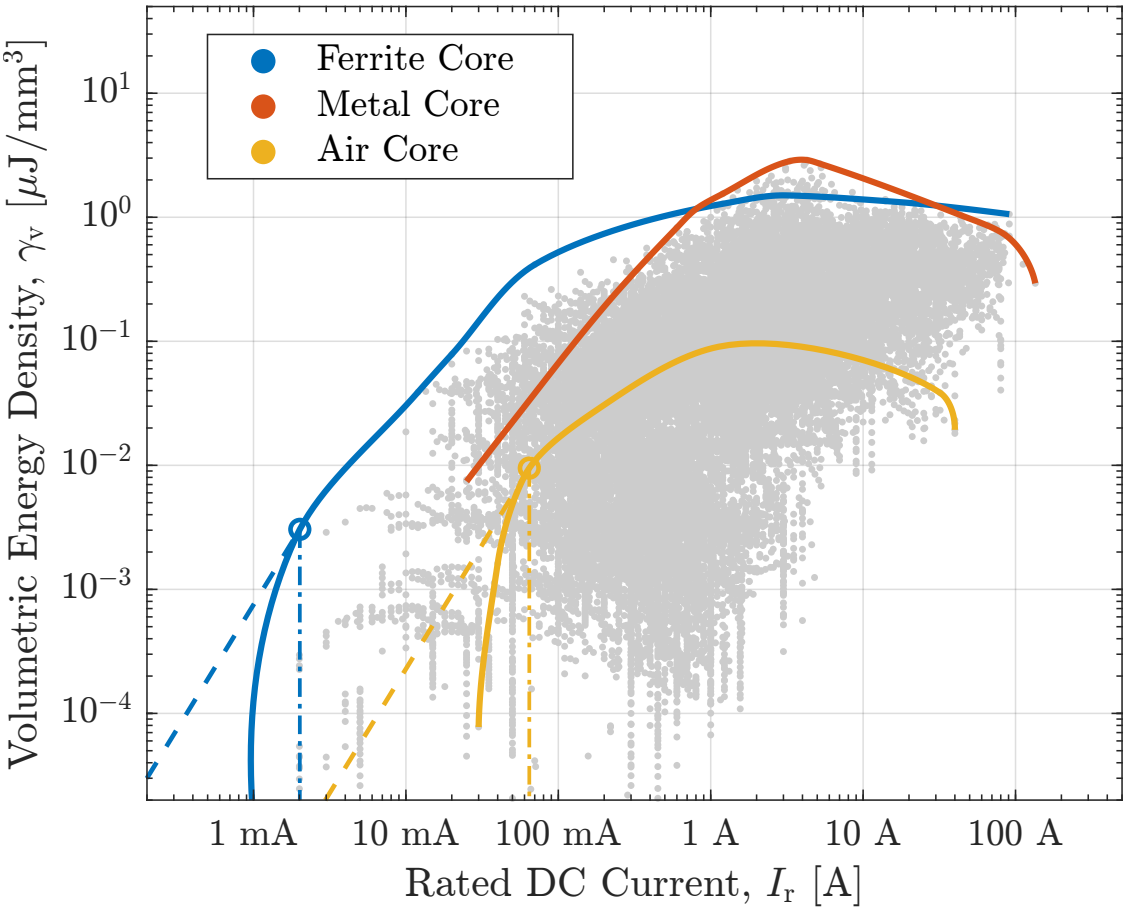


Figure 2.11: Commercial inductor volumetric energy density FOM γ_v across rated dc current I_r. The Pareto fronts are highlighted as well as the critical rated current $I_{r,crit}$ where inductor current overrating becomes useful.

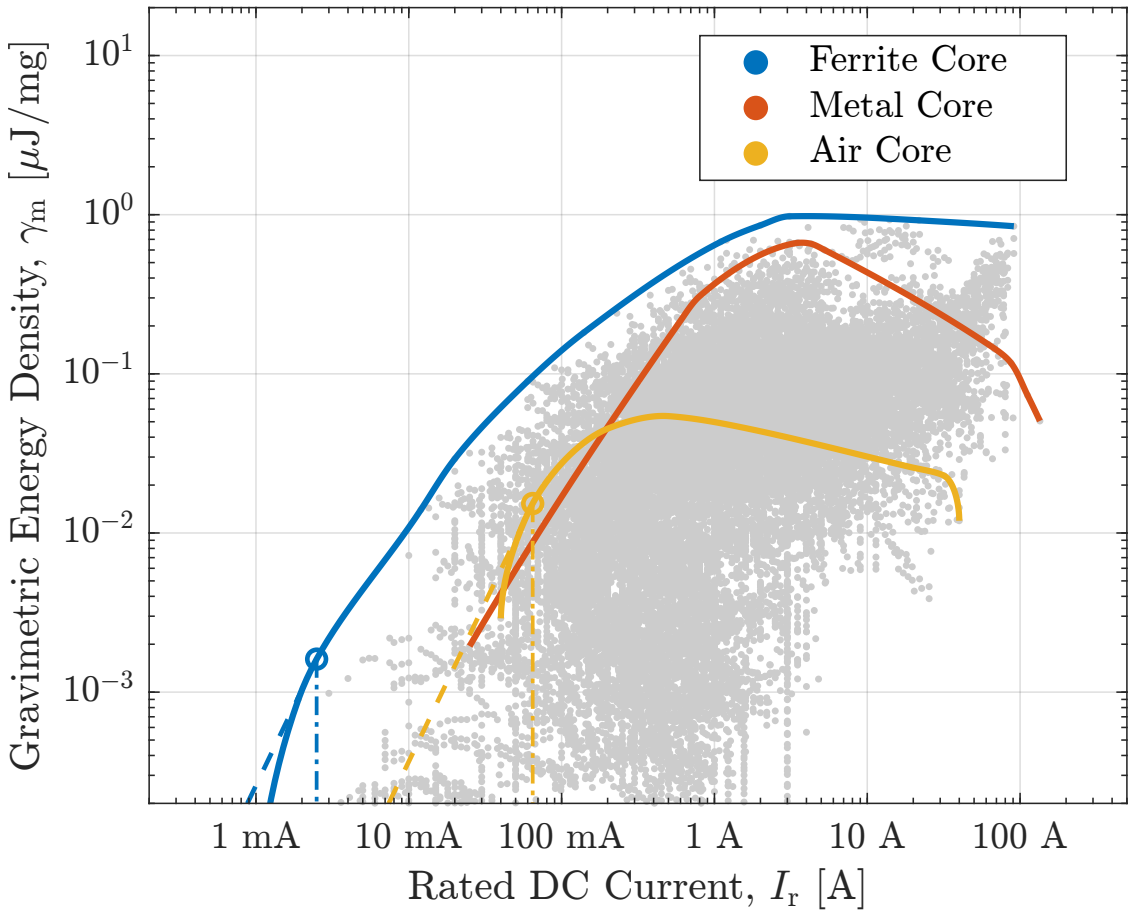


Figure 2.12: Commercial inductor gravimetric energy density FOM γ_m across rated dc current I_r. The Pareto fronts are highlighted as well as the critical rated current $I_{r,crit}$ where inductor current overrating becomes useful.

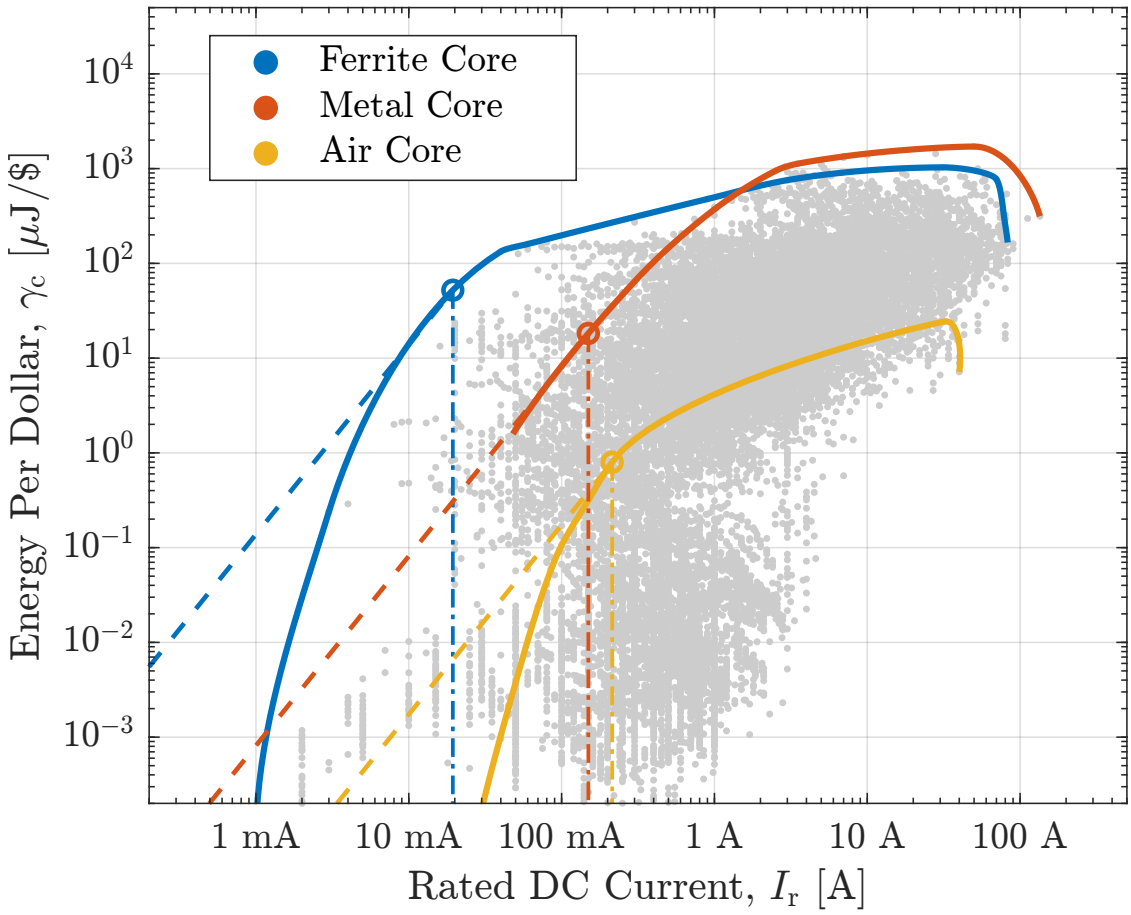


Figure 2.13: Commercial inductor energy per cost FOM γ_c across rated dc current I_r. The Pareto fronts are highlighted as well as the critical rated current $I_{r,crit}$ where inductor current overrating becomes useful.

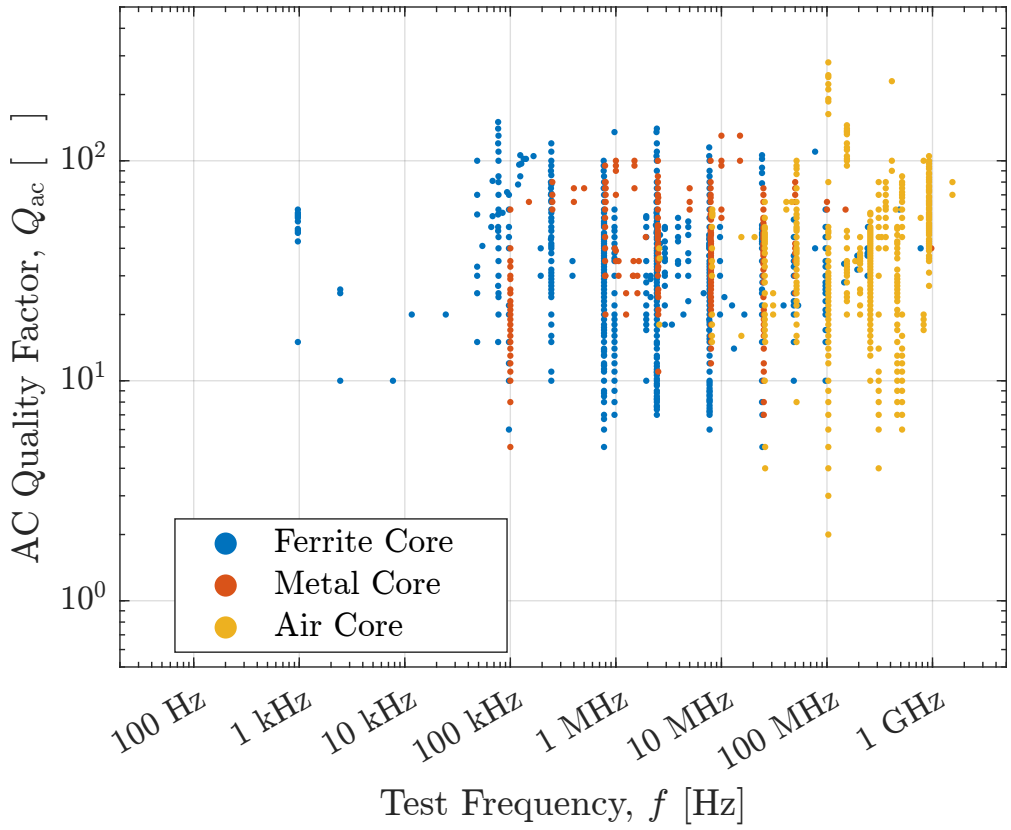


Figure 2.14: Quality factor FOM $Q_{ac} = \frac{2\pi f L}{R_{ac}}$ for all commercially surveyed inductors at respective reported test frequency f. Data is distinguished by common core types.

mass, and cost) than the best-performing ferrite and metal core inductors, although they compete equally with metal core inductors with respect to mass for current ratings below $I_r < 200\,\text{mA}$.

Inductor Quality Factor

The ac quality factor Q_{ac} is a conventional metric for benchmarking power inductor loss performance [67]. It furthermore satisfies the series-parallel invariance property in Sec. 2.2 and can be considered a suitable FOM for fairly comparing all inductors, regardless of current ratings. As mentioned in Sec. 2.3, the ac quality factor is reported, infrequently, on datasheets at a particular test frequency and this severely limits its design utility since inductor performance depends heavily on the operating frequency. Fig. 2.14 illustrates the reported testing frequency f and the associated ac quality factor Q_{ac} for the comprehensive data set. As expected, commercial air core inductors are designed to operate at higher frequencies of $f > 8\,\text{MHz}$ while ferrite and metal core inductors are designed to operate at lower

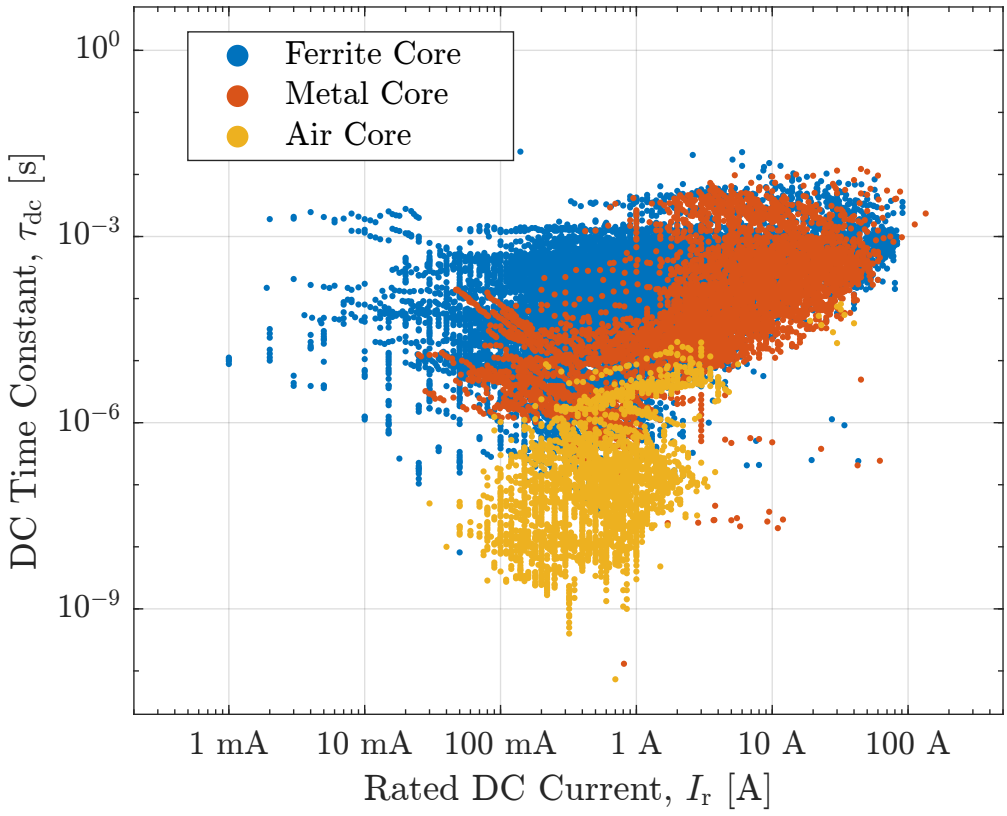


Figure 2.15: Rated dc current I_r versus dc quality factor $\tau_{dc} = \frac{L}{DCR}$ for all commercially surveyed inductors. Data is distinguished by common core types.

frequencies of $50\,\text{kHz} < f < 100\,\text{MHz}$ Additionally, the peak ac quality factor capability of commercial inductors is roughly $100 < Q_{ac} < 200$ across all frequencies and technologies.

Considering the attributes readily available in the full data set (see Sec. 2.3), a new FOM is devised to partially characterize the loss performance of inductor devices. The dc time constant

$$\tau_{dc} = \frac{L}{DCR} \tag{2.28}$$

is similar to the conventional ac quality factor Q_{ac} except that it is defined at dc frequency $f = 0\,\text{Hz}$, thus there is no notion of test or operating frequency and the equivalent series resistance only includes the dc winding resistance or DCR.

The dc time constant τ_{dc} satisfies the series-parallel modular invariance property in Section 2.2 although it is a limited metric for predicting losses as it neglects proximity effect, skin effect, eddy current, and hysteresis. In high current applications like telecommunications and datacenters, the dc time constant τ_{dc} has greater pertinence than the ac quality factor Q_{ac} since at heavy loads, the dc winding loss dominates the ac losses. The equivalent

ac resistance R_{ac}—a surrogate for the ac power losses—is often expressed as a proportion [128] or a superposition [14] of the DCR. Thus, the dc time constant τ_{dc} is also intrinsically related to the expected loss performance under large-signal, high frequency, high flux operating conditions.

Fig. 2.15 illustrates the dc time constant τ_{dc} as a function of rated dc current I_{r} (2.20) across different inductor technologies defined in Sec. 2.3. Ferrite and metal core inductors have overlapping performance regions and dominate across the full range of current ratings. Air core inductors have significantly lower τ_{dc} than ferrite and metal core inductors because they have much lower inductance L for the same DCR (i.e., winding geometry).

Comparing Capacitors and Inductors

Modern power converter topologies increasingly leverage the performance of capacitors versus inductors: hybrid switched-capacitor converters such as the FCML converter [88, 117, 13], series-capacitor buck converter [121, 74, 157], and switching bus converter [181, 202]. The fundamental trade-off between these energy storage elements requires the careful quantification of realizable device performance.

Some passive component FOM are jointly applicable to both capacitors and inductors—two fundamentally different circuit elements—and once these FOM are identified, these components can be justly compared. Energy density γ is one such generic FOM, as rated energy storage is well defined for both capacitors in (2.18) and inductors in (2.19). From the comprehensive data set, Fig. 2.16, 2.17, and 2.18 convey that there is a marked difference in the energy density capabilities of commercial capacitors and inductors. As a whole, the highest volumetric energy density γ_{v} commercial capacitor devices are nearly 1,000× greater than that of the highest γ_{v} commercial inductors. For volume-sensitive applications, choosing a circuit topology that heavily utilizes capacitors as energy transfer elements can result in a more volume efficient design [87, 88, 13, 196, 51].

Similarly for gravimetric energy density γ_{m} and energy per cost γ_{c}, the best commercial capacitors outperform the best commercial inductors by a factor of nearly 2,000 and 10,000, respectively. Thus, capacitor-dominant circuit topologies are even more heavily favored for cost and mass-optimized designs than for volume-optimized designs.

It should be noted that, unlike capacitors, custom inductors are capable of achieving markedly higher performance than their commercial counterparts [166, 167, 193, 18]; this is true with respect to energy density and quality factor. Further work may subsequently explore the capabilities of custom inductor constructions, with the benchmarks for commercial inductors firmly established in this thesis as reference.

Future Applications

Now armed with precisely quantitative intuition for inductor and capacitor performance, various device FOM can be further incorporated into analytical and procedural design methodologies for power electronics design. This work compliments recently developed analyses

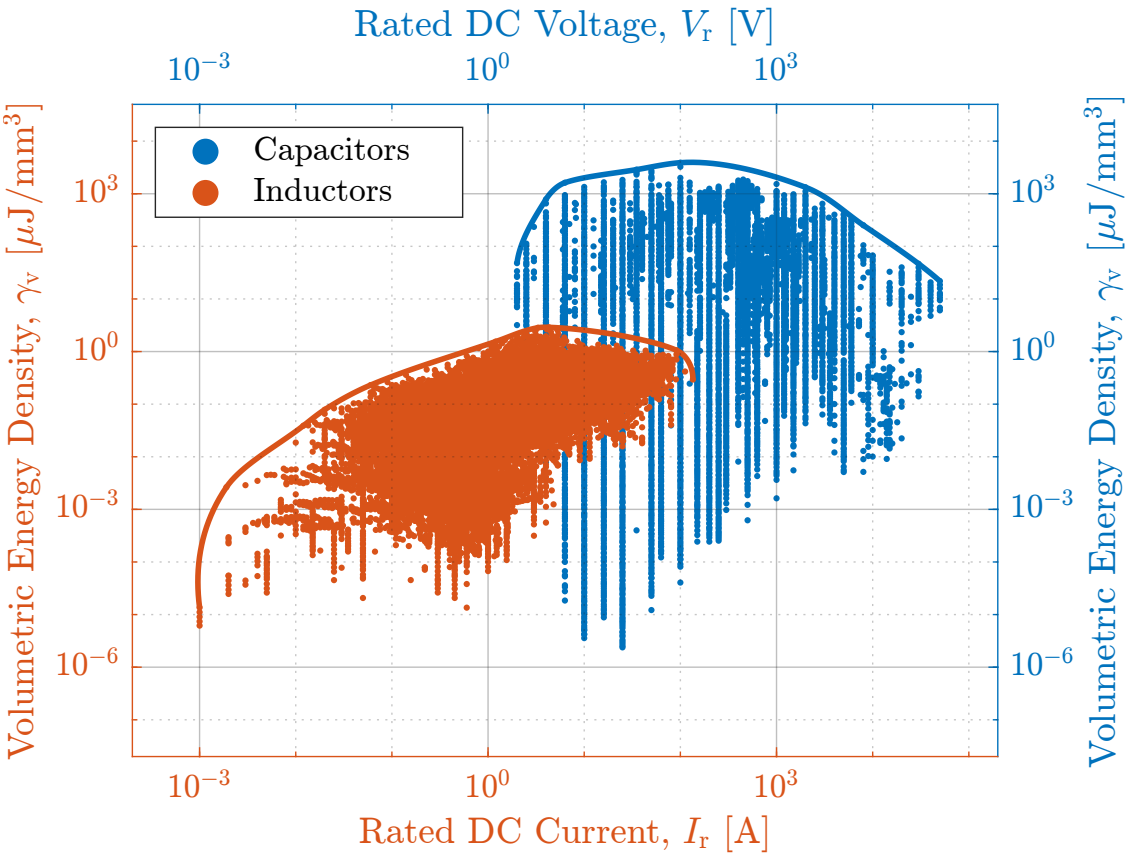


Figure 2.16: Commercial capacitor versus inductor volumetric energy density FOM γ_v across rated dc voltage V_r / current I_r. From the highlighted Pareto fronts, commercial capacitors have a roughly $1,000\times$ better maximum volumetric energy density capability compared to commercial inductors.

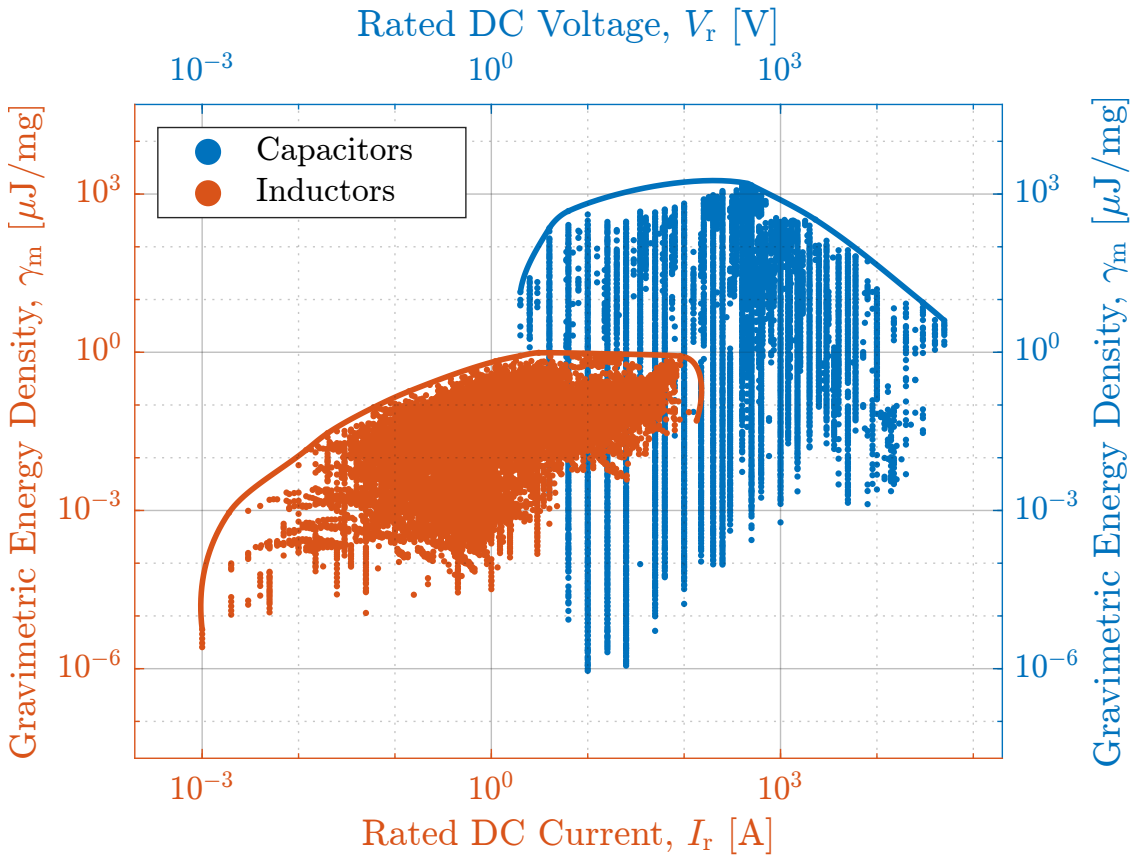


Figure 2.17: Commercial capacitor versus inductor gravimetric energy density FOM γ_m across rated dc voltage V_r / current I_r. From the highlighted Pareto fronts, commercial capacitors have a roughly $2,000\times$ better maximum gravimetric energy density capability compared to commercial inductors.

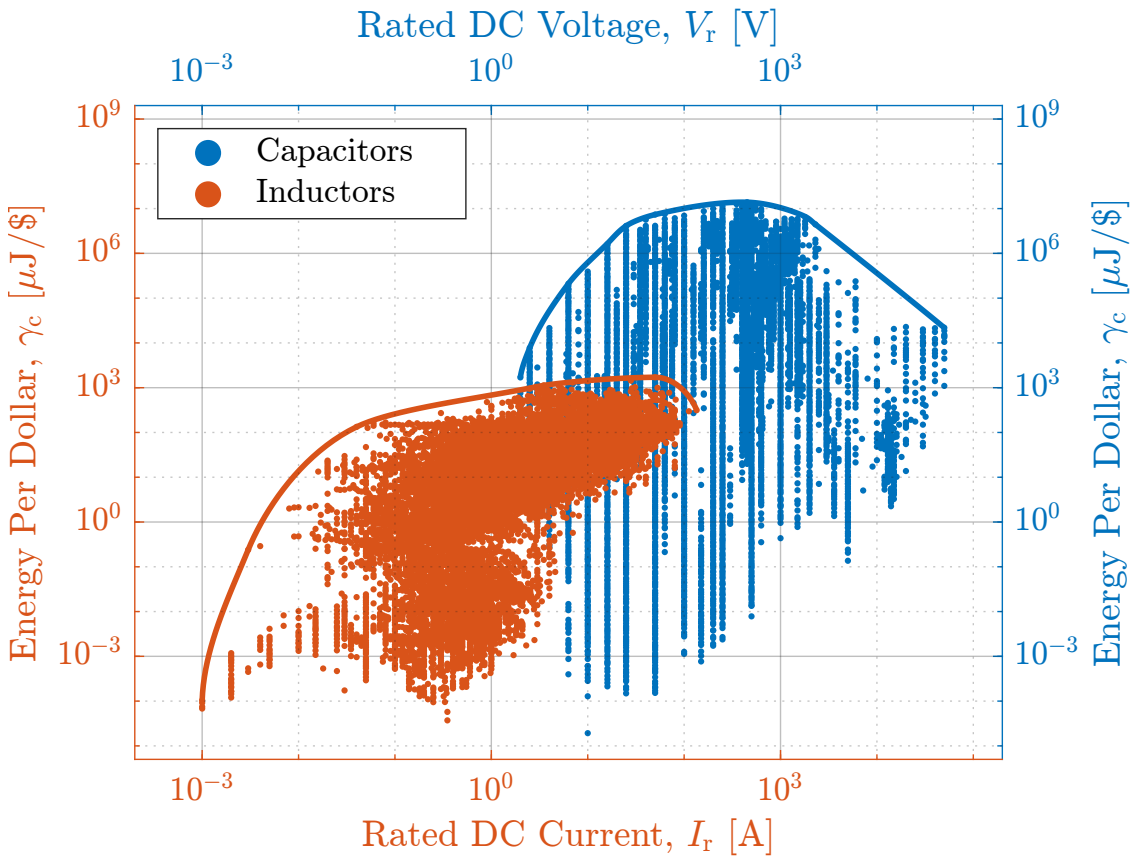


Figure 2.18: Commercial capacitor versus inductor energy per cost FOM γ_c across rated dc voltage V_r / current I_r. From the highlighted Pareto fronts, commercial capacitors have a roughly $10,000\times$ better maximum gravimetric energy density capability compared to commercial inductors.

allowing for the design of optimized hybrid switched-capacitor converters [126, 108, 196, 51]. Work in [24] analytically links capacitor energy density FOM and power density FOM to the operating waveforms of an aluminum electrolytic dc-link capacitor bank designed for single-phase twice-line frequency power buffering. Both of these applications, and many others, require actual device FOM and demonstrate the utility of the data presented in this chapter.

Finally, the comprehensive data set can continue to be improved as manufacturers and distributors standardize and digitally disseminate more passive component information.

2.7 Conclusion

The true technological capabilities of electrical devices are historically difficult to quantify due to the immense variety of components currently in development, commercially available to consumers, or entirely obsolete. Utilizing modern advancements in the accessibility of public, large-scale, and digitized component data, a phenomenological framework is developed yielding definitive and quantified component performance. This chapter reviews methods of broad passive component characterization and it presents a methodology for developing robust device figures-of-merit (FOM) to benchmark and compare passive—capacitor and inductor—components. This framework is directly applied to the data for 606,000 commercial capacitors and 88,000 commercial inductors.

Sampled data collection and measurement are used to supplement deficiencies in the comprehensive data set. To generate information on energy storage, this chapter presents an empirical fit for estimating the energy-equivalent capacitance of Class II (and Class III) ceramic capacitors. The fit was validated on 2550 datasheet characteristic capacitance (or C-V) curves and produces a mean error of 3.1% for energy-equivalent capacitance at rated voltage $C_{\mathrm{E}}(V_{\mathrm{r}})$. This chapter also presents empirical constant and power expression fits in Table 2.3 for estimating the volumetric mass density $D = \frac{\mathrm{Mass}}{\mathrm{Vol}}$ of a passive component from its rated voltage and capacitance for capacitors in (2.21), and rated current and inductance for inductors in (2.22). The empirical fits are generated from 447 device volume and mass measurements across various capacitor and inductor technologies, and produce a worst-case mean percentage error of 20%.

This chapter then specifically investigates trends in capacitor and inductor stored energy density with respect to volume, mass, and cost. Analysis of the entire data set for each component technology reveals the minimum useful capacitor rated voltage for the purposes of voltage overrating; similar critical rated currents are derived for inductor technologies. Recommendations for minimum useful component overvoltage/overcurrent ratings are tabulated in Table 2.4 and Table 2.5. Besides energy density metrics, this chapter also proposes and investigates a dc time constant FOM ($\tau_{\mathrm{dc}} = \frac{L}{\mathrm{DCR}}$) for inductors.

This chapter aims to justify particular device FOM and provides an explicit reference for practicing engineers when selecting passive components and designing circuits.

Chapter 3

Application of Passive Component Data to DC-Link Buffering Capacitor

3.1 Introduction

Single-phase (ac-dc or dc-ac) electric power converters have a fundamental discrepancy between the instantaneous dc power and the instantaneous ac power pulsating at twice the ac line frequency. The most common solution is an aptly named 'dc-link' capacitor tied in parallel across the dc bus of the converter. For sufficiently large capacitance C, this capacitor can decouple much of the ac power fluctuations from the dc port of the system.

Aluminum electrolytic capacitors in particular serve as an excellent choice for buffering in single-phase applications at low distribution voltages (50–1000 V) as they are manufactured in the largest capacitance denominations near the required voltage ratings as shown in Fig. 2.2; exhibit minimal losses (ESR) at grid frequencies [99]; maintain high energy density by both volume and mass [203]; and remain commercially competitive with low cost per unit energy [175]. However, the technology also has lower rms current rating resulting in relatively poor reliability and lifetime [180].

This chapter takes a subset of the comprehensive commercial component survey introduced in Chapter 2—aluminum electrolytic capacitors; reconsiders as well as introduces several useful device figures-of-merit (FOM); and applies these metrics to single-phase dc-link design. The results reveal the performance limitations of aluminum electrolytic capacitors for this application and yield quantifiable engineering insight.

3.2 Defining Performance Metrics

Exhaustive data aggregation and robust FOM are both required to characterize the actual performance limitations of dc-link capacitors and relate them to the single-phase application.

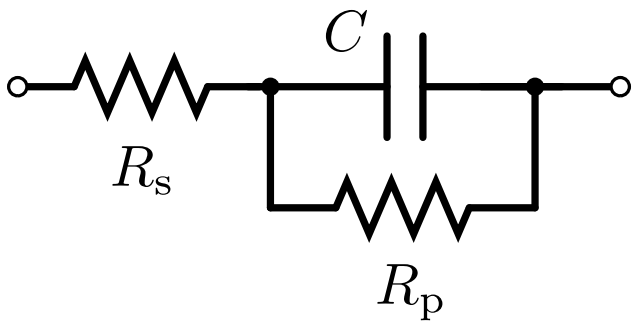


Figure 3.1: Conventional capacitor lumped circuit model including primary loss and leakage parasitics.

Internally Derived Characteristics

One approach to comprehensive device characterization is to assess internal properties and relate them to the macroscopic device performance or FOM [12]. Consider the aluminum electrolytic capacitor conventionally modeled with the circuit shown in Fig. 3.1; loss and leakage characteristics are captured with a lumped series R_s and parallel R_p parasitic resistance. At any particular frequency, these resistances jointly contribute to an equivalent series resistance ESR.

Within the capacitor, reducing plate separation increases the capacitance C and decreases the ESR and volume, but the worsened breakdown threshold of the thinner dielectric reduces the rated voltage V_r. Increasing the effective plate area also increases capacitance C and decreases ESR, but subsequently increases the volume. Larger volume and lower ESR both generally correlate to an increased rated current I_r. Internal design trade-offs influence realizable FOM and several of these trends have been explored for aluminum electrolytic capacitors in prior literature [112, 150].

Externally Derived Characteristics

The internal device characterization approach is limited since each capacitor is unique, and internal specifications are difficult to ascertain. Device performance is better determined by utilizing a component survey that externally considers all possible commercially viable capacitor variants. Additionally, an accurate assessment of trends is only possible by investigating the entire breadth of the capacitor technology. Consequently, this chapter aggregates all aluminum electrolytic capacitors which are available for purchase from the prominent distributor Digi-Key Electronics. In total, the data extensively surveys nearly 29,000 unique capacitors produced by twenty distinct manufacturers and thus represents the entire component technology in aggregate.

Robust FOM

Before considering the essential attributes of a valuable capacitor FOM, consider first how whole power converters are benchmarked. A comparative study of power conversion systems necessitates FOM with invariance to series and parallel configurations; conventional examples include input/output efficiency, volumetric and gravimetric power density, loss density, relative power per cost. All realizable values for these metrics form a feasible range of performance—or performance space—for power converters and are used to ultimately identify trade-offs and inform design [82]. One viable technique—Monte-Carlo optimization—has been utilized to identify the feasible performance space for the dc-link capacitor and several active buffering alternatives within the full single-phase conversion system [119].

Series and parallel modular invariance should also apply to device-scale FOM. Capacitors connected in series effectively increase the voltage rating of the capacitor bank, and likewise paralleled configurations increase the current rating. To adequately relate physical capacitors of various capacitance, voltage, current, volume, mass, and cost, all comparative metrics must be agnostic with respect to bank configurations of parallel and/or series connected components. For example, a bank configured as ten parallel branches of two series-connected capacitors each (i.e., twenty total capacitors) should have the same overall FOM as a single constituent capacitor.

In this chapter, three series-parallel invariant and easily calculable figures-of-merit are derived from base component metrics of rated (peak) voltage V_r, rated (rms) current I_r, capacitance C, box volume, and cost [85]:

1. Volumetric dc energy density $\rightarrow \gamma_\mathrm{v} = \frac{E_\mathrm{r}}{\mathrm{Vol}}$
   - The rated 'released energy' E_r from rated dc voltage to zero is defined as $E_\mathrm{r} = \frac{1}{2}CV_\mathrm{r}^2$ for a linear voltage-independent capacitance [45, 151, 182].
2. Volumetric power density $\rightarrow \rho_\mathrm{v} = \frac{P_\mathrm{r}}{\mathrm{Vol}}$
   - The rated power P_r is defined as $P_\mathrm{r} = V_\mathrm{r}I_\mathrm{r}$ at the rated peak voltage and rated rms current [77].
3. Energy per unit cost $\rightarrow \gamma_\mathrm{c} = \frac{E_\mathrm{r}}{\mathrm{Cost}}$
   - The per unit cost is defined as a single-unit cost rather than widely varying bulk pricing.

This chapter defines the rated power $P_\mathrm{r} = V_\mathrm{r}I_\mathrm{r}$ at the conditions maximizing leakage current and at the same operating conditions where the rated current I_r is specified—at rated voltage with a sinusoidal excitation at a specified frequency. Additionally, the rated rms current I_r depends heavily on the equivalent series resistance ESR of the capacitor and it is not a hard upper limit but rather a rating which guarantees a particular lifetime at

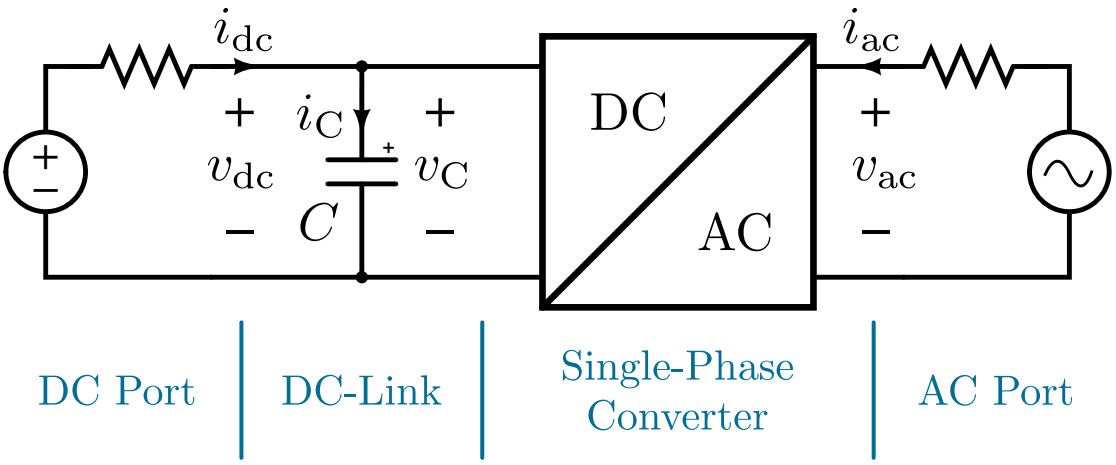


Figure 3.2: Circuit diagram of dc-link capacitor in a single-phase power conversion system.

rated voltage V_r and temperature [103]. This particular definition for power rating derives from both its simplicity and the deficiencies in the surveyed data.

The presented energy and power density device-level FOM—γ_v, ρ_v, and γ_c—are not immediately useful until they can be connected to the capacitor's application. The following analysis analytically relates these FOM to the energy and power requirements of the single-phase dc-link application.

3.3 Constraining the DC-Link Capacitor

Consider the general single-phase system with dc-link capacitor in Fig. 3.2. The dc-link capacitor is quantifiably constrained with respect to its energy and power requirements.

Single-Phase Buffering Requirement

To fully decouple the instantaneous power difference between the ac and dc ports, a fundamental peak energy E_{buf} must be buffered within a quarter of each line cycle

$$E_{buf} = \frac{P_o}{\omega_g} \tag{3.1}$$

where P_o is the system apparent power rating and ω_g is the angular frequency of the ac line [83, 132].

Assuming the dc-link capacitor buffers the entire energy requirement in (3.1), a design relationship between capacitance C and peak-to-peak dc bus (i.e., capacitor) voltage ripple

ΔV_{dc} can be derived for particular system specifications:

$$E_{\mathrm{buf}} = \frac{1}{2} C\, V_{\mathrm{C,max}}^2 - \frac{1}{2} C\, V_{\mathrm{C,min}}^2 = C\, V_{\mathrm{dc}}\, \Delta V_{\mathrm{dc}} \tag{3.2}$$

where V_{dc} is the dc bus voltage and the midrange average of the fluctuating capacitor voltage [83, 132].

A pertinent design specification is the bus voltage ripple ratio

$$\alpha := \frac{\Delta V_{\mathrm{dc}}}{V_{\mathrm{dc}}} \tag{3.3}$$

where limits are typically constrained by the source/load of the single-phase converter system. A photovoltaic (PV) panel can tolerate values up to roughly $\alpha = 10\,\%$ on the dc port before a significant degradation in the delivery of the maximum available power [83, 183].

Fig. 3.3 illustrates the instantaneous voltage $v_{\mathrm{C}}(t)$ and current $i_{\mathrm{C}}(t)$ of the dc-link capacitor across a full ac line cycle. The peak instantaneous capacitor voltage $V_{\mathrm{C,max}}$ and system power P_{o} are constrained while the ripple ratio α (and thus capacitance C) is varied for an approximate 400 V, 1 kW application. Additionally, in the small ripple approximation (i.e., $\alpha < 10\,\%$), the instantaneous capacitor or dc port voltage is analytically expressed as

$$v_{\mathrm{dc}}(t) = v_{\mathrm{C}}(t) \approx V_{\mathrm{dc}} + \frac{1}{2} \Delta V_{\mathrm{dc}} \cos(2\omega_{\mathrm{g}} t) \tag{3.4}$$

with a dc component and a sinusoidal ripple at twice the line frequency.

Energy Rating

A link between the capacitor's rated dc energy E_{r} and the required buffering energy E_{buf} must be determined to relate the rated energy density γ_{v} or γ_{c} of the component to its application.

If the peak instantaneous capacitor voltage is constrained to its rated voltage $V_{\mathrm{C,max}} = V_{\mathrm{r}}$ as shown in Fig. 3.3, then the dc bus voltage V_{dc} is alternatively expressed as

$$V_{\mathrm{dc}} = V_{\mathrm{r}} - \frac{1}{2} \Delta V_{\mathrm{dc}} = (1 - \frac{1}{2} \beta)\, V_{\mathrm{r}}. \tag{3.5}$$

where an intermediate ripple variable β is defined

$$\beta := \frac{\Delta V_{\mathrm{dc}}}{V_{\mathrm{r}}} = \frac{2\alpha}{(2+\alpha)} \tag{3.6}$$

and incidentally forms a bijective function with the ripple ratio α. By substituting (3.5) and (3.6), the buffered energy E_{buf} in (3.2) is identified as linearly proportional to the capacitor rated energy metric E_{r}:

$$E_{\mathrm{buf}} = (2 - \beta)\, \beta \cdot \left(\frac{1}{2} C\, V_{\mathrm{r}}^2 \right) = \frac{8\alpha}{(2+\alpha)^2} E_{\mathrm{r}}. \tag{3.7}$$

For a specified α, this expression describes the maximum energy buffering capability of a dc-link capacitor bank with rated energy E_{r}.

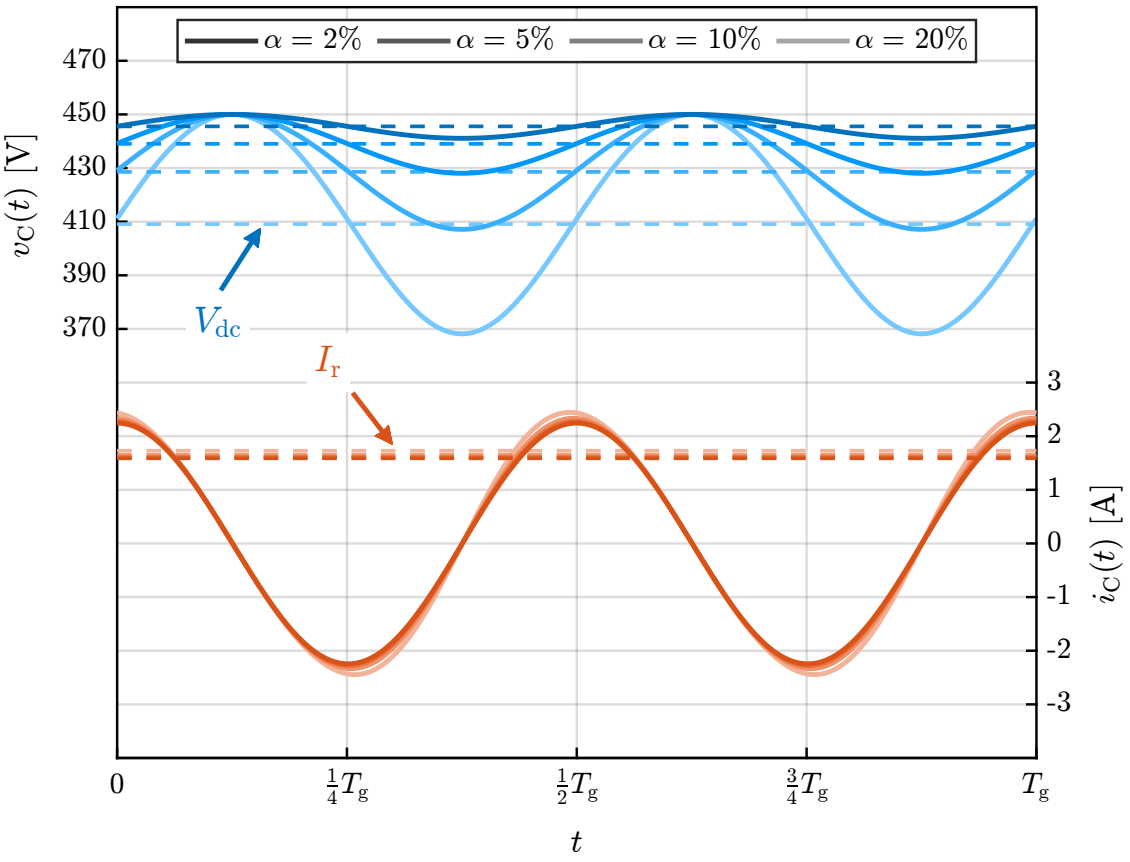


Figure 3.3: Dc-link capacitor voltage and current waveforms across one full line cycle with period T_g and with increasing specification of dc bus voltage ripple ratio α. As the ripple ratio increases, the capacitor is constrained with the same rated voltage V_r and a decreasing average bus voltage V_{dc}.

Power Rating

Similar to the energy requirements, a capacitor's rated power P_r and the system power rating P_o must be related to utilize the capacitor's power density metric ρ_v.

An expression for the peak-to-peak dc bus voltage ripple ΔV_{dc} of the system is determined by substituting (3.1) into (3.2):

$$\Delta V_{dc} = \frac{P_o}{\omega_g C V_{dc}}. \tag{3.8}$$

The instantaneous current $i_C(t)$ through the dc-link capacitor is derived from the small-ripple approximation for voltage $v_C(t)$ in (3.4)

$$i_C(t) = C\frac{d}{dt}v_C(t) \approx \omega_g C \Delta V_{dc} \cos(2\omega_g t) \tag{3.9}$$

which, with (3.8) substituted, has rated rms current value

$$I_{\mathrm{r}} \approx \frac{1}{\sqrt{2}}\omega_{\mathrm{g}} C\,\Delta V_{\mathrm{dc}} = \frac{P_{\mathrm{o}}}{\sqrt{2}\,V_{\mathrm{dc}}}. \tag{3.10}$$

The system power P_{o} is identified as linearly proportional to the capacitor rated power metric P_{r} by using (3.3) and (3.6) to perform a change of variable from V_{dc} to V_{r} in (3.10)

$$P_{\mathrm{o}} = \frac{2\sqrt{2}}{2+\alpha} \cdot (V_{\mathrm{r}} I_{\mathrm{r}}) = \frac{2\sqrt{2}}{2+\alpha} P_{\mathrm{r}}. \tag{3.11}$$

For a specified α, this expression describes the maximum system power capability for a dc-link capacitor bank with rated power P_{r}.

Energy Versus Power

The single-phase energy buffering requirement E_{buf} and the system power rating P_{o} are fundamentally related as in (3.1). Consequently, (3.7) and (3.11) can be substituted and simplified to produce a preferred relationship between the rated energy E_{r} and rated power P_{r} of a capacitor

$$P_{\mathrm{r}} = \frac{4\alpha}{\sqrt{2}\,(\alpha+2)}\omega_{\mathrm{g}} E_{\mathrm{r}} = k E_{\mathrm{r}}. \tag{3.12}$$

A capacitor or bank of capacitors lying on this contour will have an rms current rating I_{r} perfectly suited to its voltage rating V_{r} and capacitance C for a specified dc voltage ripple ratio α. However, capacitor solutions with rated power $P_{\mathrm{r}} > kE_{\mathrm{r}}$ will also satisfy the requisite buffering requirements.

Normalizing (3.12) with respect to volume, cost, or mass yields a minimum constraint between the energy density and power density of a capacitor for the dc-link application. These metrics are series-parallel invariant figures-of-merit and thus can be used to compare all configurations of capacitor banks regardless of individual component voltage or current ratings.

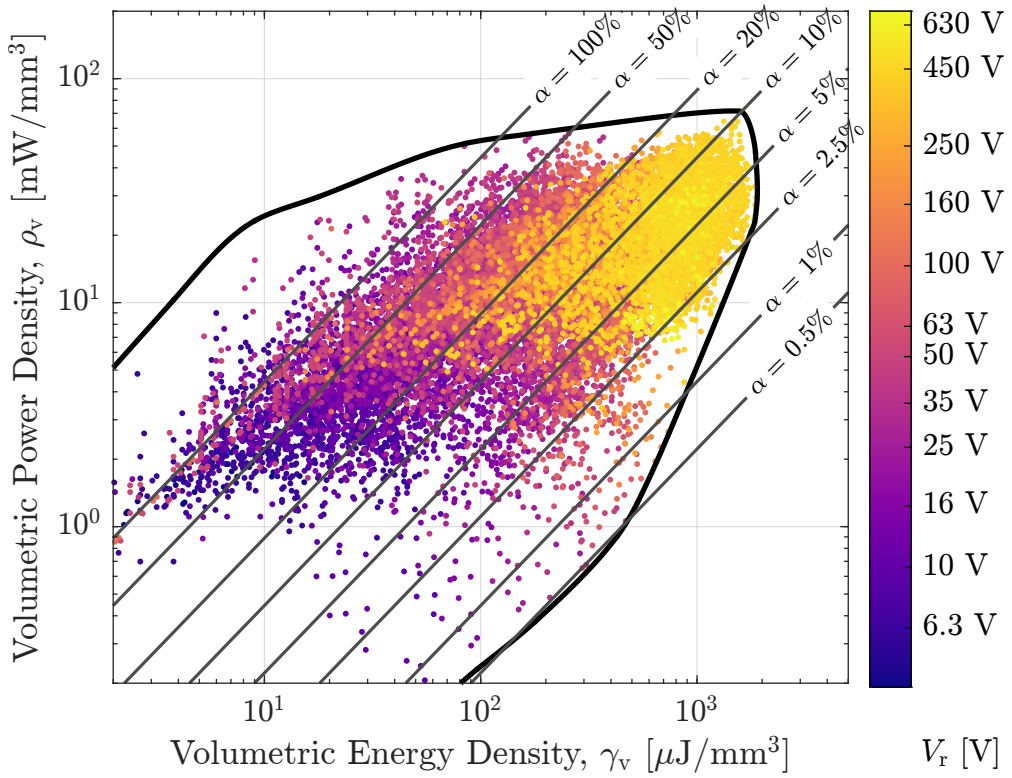


Figure 3.4: Volumetric energy density γ_v versus power density ρ_V versus rated dc voltage V_r for all commercially available aluminum electrolytic capacitors. The dc-link capacitor rated energy versus rated power isocline is shown for various ripple ratio α at line frequency $\omega_g = 2\pi \cdot 60\,\text{rad/s}$. For a specific α, capacitor banks formed with components lying above the isocline satisfy energy buffering requirements.

3.4 Analysis

The dc-link capacitor constraint derived in (3.12) between the desired rated energy and power at $2\omega_g$ frequency can be applied to the entire breadth of surveyed commercially available aluminum electrolytic capacitors.

Application to Volume

Fig. 3.4 presents a large spread of component volumetric energy and power densities, γ_v and ρ_v, computed directly from datasheet specifications. The data set illustrates that the highest performance capacitors—with superior energy and power density in the upper-right quadrant—tend to be those rated for the highest voltages (e.g., $400\,\mathrm{V} \leq V_r \leq 630\,\mathrm{V}$) dissuading series configurations of lower voltage rated capacitors and motivating power conversion architectures with high voltage dc-links. The energy-power constraint in (3.12) is superimposed as an isocline for various bus voltage ripple ratio α. For each isocline, all components with simultaneous energy and power density FOM above the contour will satisfy both the energy and power requirements dictated by dc-link twice-line frequency energy buffering. The entire set of isoclines reveal that the pool of applicable highest performance capacitors begins to shrink for $\alpha > 2.5\,\%$. Above $\alpha = 10\,\%$, the realized capacitor bank solution which still meets fundamental requirements will grow significantly in volume since the highest achievable volumetric energy density drops below $\gamma_v = 150\,\mu\mathrm{J/mm}^3$.

Application to Cost

Fig. 3.5 illustrates the rated dc voltage V_r versus energy per cost FOM γ_c across all commercially available aluminum electrolytic capacitors. Capacitors with relatively high voltage rating (e.g., $V_r = 450\,\mathrm{V}$) have the lowest costs relative to their rated energy storage capability, and there is a sharp increase in cost for capacitors with rated voltage below $V_r < 50\,\mathrm{V}$.

In addition to volume, the rated energy-power constraint in (3.12) also informs the lowest realizable costs for the practical dc-link capacitor bank. The full component data set reduces to a subset with quantitatively lower performance once a desired maximum relative ripple $\alpha = \alpha_{max}$ at P_o is specified. As the ripple ratio α on the dc bus increases, the Pareto set of compliant capacitors diminishes, and is dramatically reduced for $\alpha > 5\,\%$. For cost-constrained designs, this insight can narrow the set of viable capacitor choices and aid determination of cost-optimal dc-link capacitor solutions.

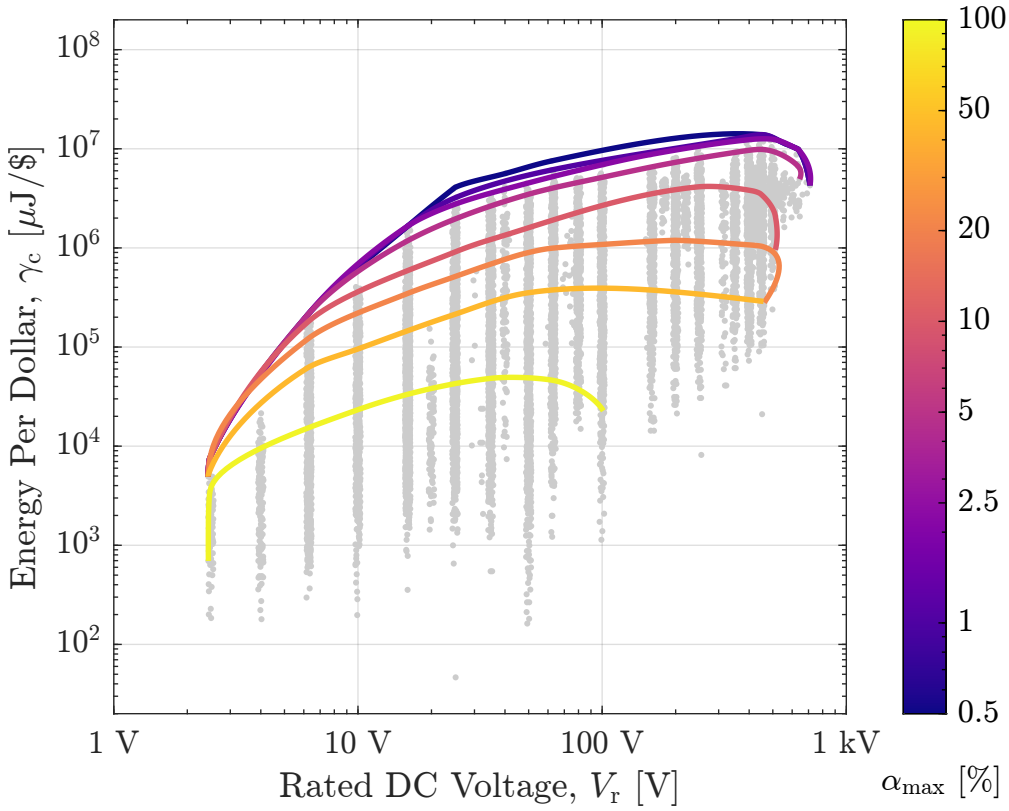


Figure 3.5: Rated dc voltage V_r versus energy per unit cost γ_c for all commercially available aluminum electrolytic capacitors. For increasing bus ripple ratio rating α_{max}, the full data set reduces to only those components satisfying rated energy and power requirements and the best performers in each subset are indicated with Pareto fronts.

3.5 Conclusion

Design of a dc-link capacitor bank for single-phase applications presently requires a component search based largely on ad hoc procedures, and existing generalizations about capability (i.e., density, cost, loss) are primarily qualitative. This work presents a set of easily calculable device figures-of-merit—volumetric energy density, volumetric power density, and energy per cost—all with the special property requisite for invariance to arbitrary series or parallel component configurations. An exhaustive survey of commercial aluminum electrolytic capacitors is performed to enable empirical quantitative measures. Additionally, the dc-link capacitor's rated energy and power are analytically related for the single-phase buffering application with respect to the relative voltage ripple ratio α on the dc bus. This analysis supplements visualization of the surveyed data and demonstrates the range of practicable dc-link capacitor solutions. The data reveals meaningful design insights such as unavoidably

high volume solutions for bus voltage ripple ratio $\alpha > 10\,\%$ and inevitable high cost solutions for $\alpha > 5\,\%$.

Part II

Modeling of the Flying Capacitor Multilevel Converter

Chapter 4

Review of Continuous-Time State-Space Modeling for the FCML Converter

4.1 Introduction

Power electronics interface electrical systems and enable efficient energy transference. Reliable operation of these power conversion systems requires controllability of voltages and currents, stability across different operating points, and robustness in the presence of underlying parameter variation and exogenous disturbances. A substantial body of literature has studied theoretical and practical aspects of modeling and control of power converters to achieve both improved performance (e.g., reduced loss and improved lifetime) and higher function (e.g., fast regulation and better waveform quality). As power converters are switched systems, engineers often encounter a fundamental tradeoff between model accuracy and practical utility. Standard "averaging" approaches [116] accurately capture low frequency behavior of many simple converters, but fail to describe dynamical behavior of topologies where voltages and currents have significant harmonic content at and above the switching frequency [149]. Naturally, the most accurate models account for the time-varying nature of the system's dynamics. This typically involves modeling the voltage and current behavior in the presence of switching and developing accurate models of pulse-width modulation schemes native to power converter control. Though such models are difficult to derive and analyze compared to averaged models, they find increasing utility with modern computational tools. Furthermore, modern digital control enables practical implementation of controllers designed from such models, and allows realization of complex yet highly attractive new power converter topologies.

One such topology, the flying capacitor multilevel (FCML) converter has been shown to be a compact and efficient converter in applications requiring a wide voltage conversion range [88, 117, 30]. Alongside the improvements in practical implementation, there have

been a number of efforts to model the dynamic and steady-state behavior of the converter, particularly the behavior of the flying capacitor voltages: termed flying capacitor voltage balancing [114, 186, 106, 147, 113, 140, 188, 197, 199]. Balanced operation is crucial because it enables the use of lower voltage rated switches ($v_{\mathrm{ds}} \approx \frac{1}{N-1}\, v_{\mathrm{i}}$) which generally have higher figures-of-merit [12]. Presently, any FCML converter which does not employ an active balancing feedback control scheme must rely on the natural balancing dynamics—the inherent tendency of the average flying capacitor voltages v_{C_j} to converge to their 'balanced' fractional values of the input voltage, $v_{\mathrm{C}_j} = \frac{j}{N-1}\, v_{\mathrm{i}}$. However, unlike the steady-state capacitor voltage behavior—investigated in great depth in [197, 141]—quantitative measures of the natural balancing dynamics (e.g., settling time, bandwidth, dominant resonant modes) are not sufficiently understood or characterized beyond measurement of physical systems. Use of low-voltage rated transistors for high performance FCML converter design and synthesis of accurate plant models for voltage balancing controllers are both predicated upon understanding and characterizing these dynamics.

This chapter further investigates and develop the ideas introduced by Meynard in [114] regarding the *averaged* flying capacitor voltage dynamics of the FCML. In his work, Meynard proposes a equivalent circuit model for multilevel converters and an associated frequency domain formulation to represent the flying capacitor voltages as an LTI state-space system of ordinary differential equations. Meynard develops the state-space systems by performing a Fourier series decomposition of time domain waveforms of his proposed circuit model. Meynard's model methodology could be usefully applied to other multilevel and hybrid switched-capacitor circuit topologies, however this chapter exclusively considers the FCML converter.

First, the key defining features of the model in [114] are recounted in Section 4.2. Then in Section 4.3, this state-space model will be simplified for symmetric phase-shifted pulse-width modulation in practical applications for the general N-level case and the 3-level case. Next in Section 4.4, a key metric characterizing system dynamics—the dominant time constant—is introduced and evaluated based upon the previously derived simplifications.

4.2 Background

The critical ideas presented by Meynard in [114] must be introduced and relayed before elucidating simplification and further analysis. This section summarizes his key results and addresses some of their practical applications. The notation used throughout this chapter is localized entirely to this chapter to remain consistent with the notation of the original work.

There will be a heavy reliance on linear algebra and the associated nomenclature includes some visual identifiers

- Non-scalar variables (i.e., vectors and matrices) are uppercase.
- Scalar elements of matrices are uppercase and additionally denoted with the subscripts i and k.

- Scalar elements of vectors are uppercase and additionally denoted with the subscript k.
- Scalar variables are lowercase and always lack the denotation k (and i).
- Superscripts indicate a harmonic order, not an exponent.

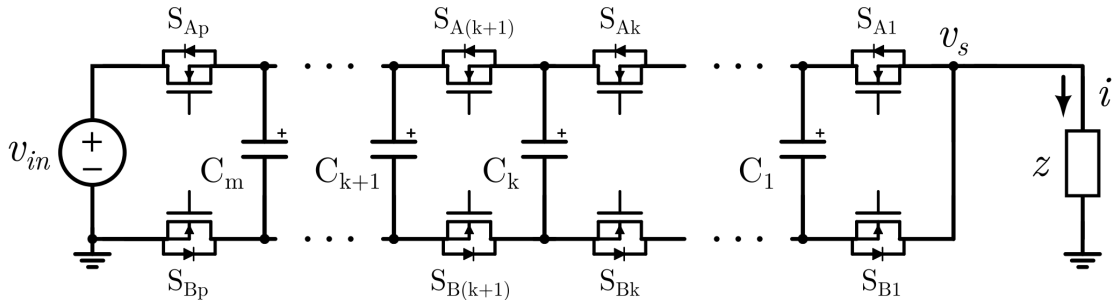


Figure 4.1: N-level buck-type FCML converter schematic. $m = p - 1 = N - 2$.

Key Analytical Result in [114]

The general N-level buck-type with arbitrary output impedance is shown in Fig. 4.1. Derived from his equivalent circuit model of this converter, Meynard's primary analytical building block is the Fourier series coefficients of a zero to one rectangular waveform with duty cycle D_k and phase shift Φ_k. The subscript k denotes each switch pair (or cell) from $k = 1, \ldots, p$. For the rectangular waveform of each cell k, the Fourier series coefficient of harmonic n can be expressed as

$$G_k^n = \frac{1}{n\pi} \sin(n\pi D_k)\, e^{jn\Phi_k} \qquad \text{for } k = 1, \ldots, p \tag{4.1}$$

The purely rectangular waveform assumes the high frequency (non-average) components of the flying capacitor voltages do not change appreciably each switching cycle. In other words, the flying capacitances cannot be arbitrarily small to ensure a small-ripple approximation.

The second building block comes about from the "chopping" nature of the FCML and is the difference between the rectangular waveforms of adjacent phase-shifted switch pairs

$$H_k^n = G_{k+1}^n - G_k^n \qquad \text{for } k = 1, \ldots, m \tag{4.2}$$

where $m = p - 1 = N - 2$ denotes the number of flying capacitors.

The key result of Meynard's work is a dynamical state-space representation of the average flying capacitor voltages

$$\dot{V}_\mathrm{C} = A(D, \Phi)\, V_\mathrm{C} + B(D, \Phi)\, v_\mathrm{in} \tag{4.3}$$

with an m-by-1 state vector (one for each flying capacitor)

$$V_{\mathrm{C}} = \begin{bmatrix} V_{\mathrm{C_1}} \\ \vdots \\ V_{\mathrm{C_m}} \end{bmatrix}, \tag{4.4}$$

a m-by-m state matrix A, an m-by-1 input matrix B, and a scalar input v_{in}. Matrices A and B are notably generalized as functions of a duty cycle and phase shift vector with arbitrary elements, which is implied throughout this work unless stated otherwise. A and B are expressed as a finite sum of contributive matrices at each harmonics n of the switching frequency as

$$A = \sum_{n=1}^{r} A^n \tag{4.5}$$

$$B = \sum_{n=1}^{r} B^n \tag{4.6}$$

where finite r harmonics reduces model complexity and individual harmonics n are expressed by

$$A^n = -2 \ \mathrm{Re} \left(\frac{1}{z^n} \overline{\begin{bmatrix} \vdots \\ \frac{1}{c_k} H_k^n \\ \vdots \end{bmatrix}} \begin{bmatrix} \cdots & H_k^n & \cdots \end{bmatrix} \right) \tag{4.7}$$

$$B^n = -2 \ \mathrm{Re} \left(\frac{1}{z^n} \overline{\begin{bmatrix} \vdots \\ \frac{1}{c_k} H_k^n \\ \vdots \end{bmatrix}} G_{\mathrm{p}}^n \right) \tag{4.8}$$

where z^n is the converter output impedance for each harmonic n and each flying capacitance is denoted as c_k, and the overbar symbol denotes the complex conjugate operator of a matrix/vector (without transpose).

For additional details and justifications regarding this derivation, please refer to [114] and Appendix E of [185]. Another foundational work modeling multilevel converters presented in [191] has a similar state-space formulation based on Fourier series decomposition.

Practical Usefulness

After deriving the averaged flying capacitor voltage model in (4.3), Meynard also considers several practical implications.

Steady-state imbalance

The steady-state values of V_{C_k} can be determined with the stable equilibrium of (4.3) by setting $\dot{V}_C = 0$ or

$$V_C(\infty) = -A^{-1}B\ v_{in} \tag{4.9}$$

Meynard's steady-state solution in 4.9 always evaluates as

$$V_{C_k}(\infty) = \frac{k}{p}\ v_{in} \qquad \text{for } k = 1, \ldots, m \tag{4.10}$$

assuming a symmetric phase-shifted pulse-width modulation (PSPWM) strategy with equal duty cycle in each switching cell and circularly symmetric phase shift between adjacent switching cells. which seemingly neglects much of the perceived imbalancing concerns of the practical topology [194, 140]. This circuit model is thus too idealized for the purposes of accurately incorporating and estimating steady-state imbalance in the flying capacitor voltages. Isolating steady-state imbalancing contributions such as input capacitance, incorporating them into a more comprehensive circuit model, and then applying Meynard's generalized frequency-domain methodology can lead to a maturer state-space representation.

Dynamic imbalance

The benefit of an explicit state-space representation is the application of eigenanalysis and control theory. Control theory concepts such as stability, controllability, and observability would be an advanced application of these principles since linearization of a extraordinarily nonlinear system is required, but elementary eigenanalysis is well within the scope of possibility.

The set of complex eigenvalues of A (or spectrum), denoted as $\lambda_i = \sigma_i + j\omega_i \in \lambda_A$, characterize the natural behavior of the flying capacitor voltage dynamics. The dominant eigenvalue λ_d, which here denotes the "rightmost" value on the complex plane with the largest real value [145], has the greatest impact on the rate of balancing or the dynamic imbalancing.

The dominant time constant τ_d of the flying capacitor dynamics can be approximated by the dominant time constant of A, denoted by τ_A, which is calculated from the dominant eigenvalue by

$$\tau_d \approx \tau_A = -\frac{1}{\sigma_d} = -\frac{1}{\max(\mathrm{Re}(\lambda_A))} \tag{4.11}$$

and assumes an asymptotically stable system where $\sigma_d < 0$. The effective time constant provides a single metric which adequately describes the convergence of the slowest dynamics to steady-state values.

Choices in circuit components such as the flying capacitance c_k and the output impedance z which contains information about the inductance, output capacitance, load resistance, and switching frequency will directly impact A and thus the eigenvalues and effective time constant.

Time-variance

Any discussion of eigenvalues is only valid for linear time-invariant systems (LTI) where A (and consequently B) is constant with time. Although Meynard does not actually distinguish between time-variance and time-invariance, his state-space model is generalized for both and the application of the FCML dictates the delineation.

The relatively few conditions for which the system is linear time-variant (LTV) can identify the valid conditions for which the system is LTI. By considering the formulation of A and B in conjunction with the practical use of the FCML with traditional PSPWM, continuous time-variance only occurs when the duty ratio vector D is continuously time-varying such as in a single-phase inverter or rectifier. In this case, $A(t)$ and $B(t)$ are both continuous functions of time and system stability becomes difficult to assess. Note that the time-variance of $v_{\text{in}}(t)$ which dictates the steady-state values of V_{C_k} according to (4.10) does not impact the overall time-invariance of the model.

If an LTV system can be approximated as a piecewise LTI system, then it is a unique case where a dominant time constant can be identified for each piecewise segment of operation. An operational example is any which alters A between piecewise segments such as level or mode transitioning and/or step changes in duty cycle and phase shift.

The traditional concepts of eigenvalues and dominant time constants applicable to LTI systems do not apply directly to LTV systems. Continuously LTV systems are better suited to the derivations in [185, 187, 186] which seek to characterize time-varying $D(t)$ into the Fourier decomposition directly as a modulation signal. The result of these techniques is to create a more complex and comprehensive LTI state-space representation than presented in [114].

Simulation

The primary validation technique of a state-space model is through time domain simulation. Meynard presents results for various FCML operating conditions and transient responses. Although not mentioned explicitly, it can be assumed that the continuous-time state-space system (4.3) was discretized and simulated step-by-step to achieve these results. This chapter utilizes this same discrete-time simulation to visualize the dynamics of the flying capacitors in time.

It should be noted that discretization does not work explicitly for generalized LTV systems. However if the time-varying dynamics of the circuit are smooth and sufficiently slower than the sampling rate, then the system can be roughly approximated as piecewise continuous LTI [178].

4.3 Simplified Model

Meynard's state-space formulation is notably valid for any general case of phase-shifted pulse-width modulation (PSPWM) where the duty cycle and phase shift for each switch pair

k is arbitrary. The two common categorizations of PSPWM are symmetric and asymmetric [191]. With particular choice of D_k and Φ_k, this general case of PSPWM encompasses certain asymmetric or "actively balanced" PSPWM strategies which can be validly represented by A and B [139, 164]. The simplest known method for stably controlling the FCML is colloquially termed symmetric or "passively balanced" PSPWM and is a special case worth investigating further.

For symmetric PSPWM, A and B can be factored and simplified to better understand: 1) which switching current harmonics i^n influence dynamic imbalance in the flying capacitors; 2) what circuit parameters influence the effective time constant; and 3) can the state-space model be equivalently reduced for purposes of simulation and estimation?

Assumptions

There are a number of assumptions which must be made to reduce and simplify the state-space formulations in (4.5)−(4.8) to the symmetric case of PSPWM. First assume every switch pair is controlled with the same duty cycle d or

$$D_k = d \qquad \text{for all } k = 1, \ldots, p \tag{4.12}$$

Next, assume the phase shift between adjacent switch pairs is evenly spaced or

$$\Phi_k = \frac{2\pi}{p} k \qquad \text{for } k = 1, \ldots, p \tag{4.13}$$

The final assumption is not specifically associated with the modulation scheme but is reasonable and aids in simplification of A and B. Assume each flying capacitor has equivalent capacitance

$$c_k = c \qquad \text{for all } k = 1, \ldots, m \tag{4.14}$$

Output Impedance

The output impedance z is critical to the evaluation of (4.5) and (4.6) as its magnitude and phase as a function of harmonics of the switching frequency strongly influence the eigenvalues of A and thus the effective time constant of the flying capacitor voltages.

The standard output impedance model for a buck converter as shown in Fig. 4.2 includes a standard buck inductor, output capacitor, load resistor, and an additional parasitic series resistance for the inductor. The associated frequency domain expression for z is derived as

$$\begin{aligned} z^n &= |z^n| \cdot e^{j\phi_{zn}} \\ &= z(jn\omega_\mathrm{s}) = jn\omega_\mathrm{s} L + R_\mathrm{e} - \frac{jR_\mathrm{L}}{(n\omega_\mathrm{s} R_\mathrm{L} C_\mathrm{out} - j)} \end{aligned} \tag{4.15}$$

where ω_s denotes the switching frequency (in radians) of the converter. It should be noted here that other series resistance parasitics within the converter such as the on-state resistance

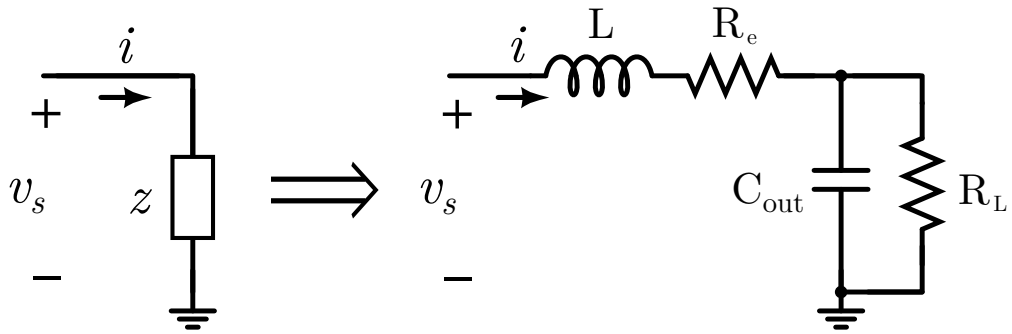


Figure 4.2: Buck converter circuit schematic of traditional output impedance.

of the transistors and the high-frequency winding and core resistances of the inductor can be lumped into R_e; the significance of these other loss mechanisms are investigated with hardware validation in Section 5.4 of Chapter 5.

Assuming proper buck converter design, parameter choices within the model for z in (4.15) can be constrained. These constraints will ultimately provide an accurate approximation for $|z^n|$ and ϕ_{zn}. Firstly, to operate as a "hard-switched" (non-resonant) converter to properly attenuate switching harmonics in the output voltage, the switching frequency must be well above the resonant frequency of z

$$\omega_\mathrm{s} \gg \omega_\mathrm{r} = \frac{1}{\sqrt{L \cdot C_\mathrm{out}}}. \tag{4.16}$$

Secondly, the load resistance R_L should be significantly greater than the characteristic impedance R_0 of z otherwise switching harmonics will bypass the output capacitor directly to the load resistance

$$R \gg R_0 = \sqrt{\frac{L}{C_\mathrm{out}}}. \tag{4.17}$$

Finally, parasitic resistance R_e should be significantly less than the reactance ωL of the inductor when $\omega \geq \omega_\mathrm{s}$

$$\omega_\mathrm{s} L \gg R_\mathrm{e}. \tag{4.18}$$

The models for impedance z in [114, 191, 148] are actually a simplification of the proposed model in Fig. 4.2 as they do not include C_out and R_e. This discrepancy has significant impact on the system characterization. The constraint on load resistance in (4.17) highlights the key difference between previous works and this work. The model in [114] is characterized for medium-voltage (kV) and high power (MW) applications where $R < R_0$ and thus C_out is effectively neglected in the overall output impedance in (4.15). However, for medium-voltage (kV) and medium power (kW) applications the constraint on the load resistance in (4.17) remains valid.

The following approximation for z at and above the switching frequency (i.e., z^n) results from applying the three parameter constraints in (4.16)−(4.18)

$$z^n \approx jn\omega_s L + R_e \tag{4.19}$$

$$|z^n| \approx n\omega_s L \tag{4.20}$$

$$\phi_{zn} \approx \arctan\left(\frac{n\omega_s L}{R_e}\right) \tag{4.21}$$

Figure 4.3 illustrates that at relevant frequency harmonics $n\omega_s$, the output impedance in (4.15) can be approximated by (4.20) and (4.21). Notice the large disparity in phase between the circuit modeled with and without output capacitance C_{out}. This difference if not accounted for can cause drastic system mischaracterization.

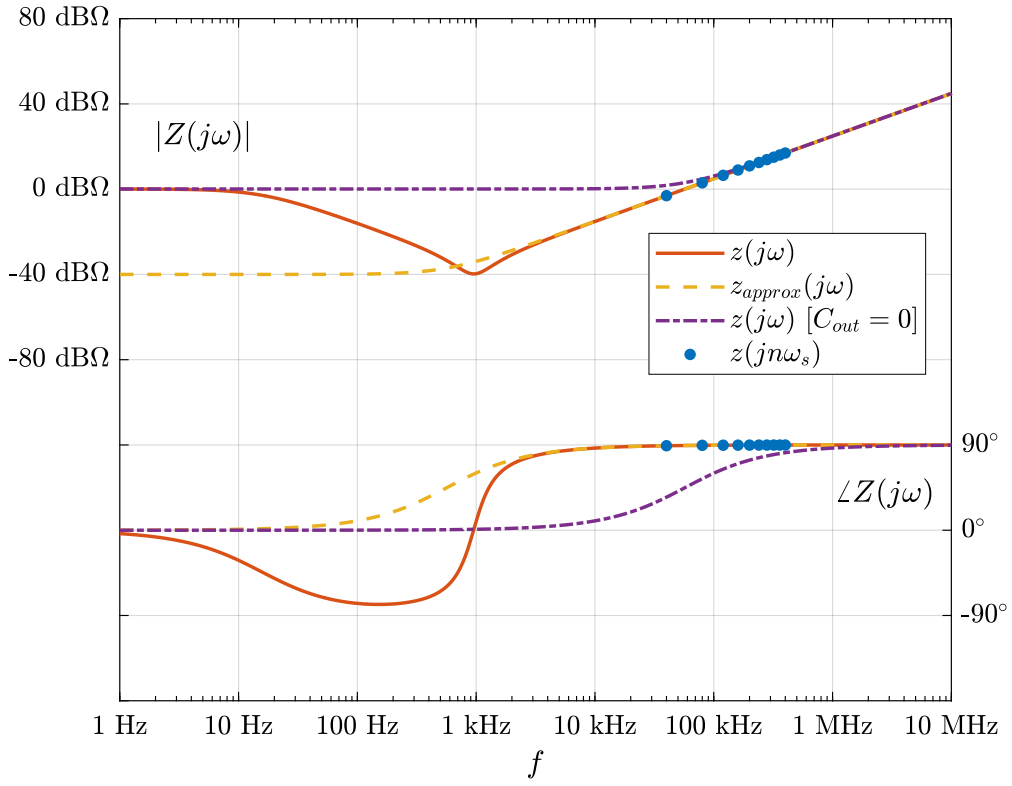


Figure 4.3: Output impedance z as a function of frequency. Includes critical harmonics z^n, approximation pf z, and modeled z without output capacitance. Parameters: $L = 2.8$ μH, $R_e = 10$ mΩ, $C_{out} = 10$ mF, $R = 1$ Ω, $f_s = 40$ kHz.

Symmetric PSPWM Analysis

The following analysis extracts and combines scalar terms to analytically simplify the matrix expressions in (4.7) and (4.8). The resulting formulations isolate the individual contributions of circuit parameters on time-variance and eigenvalues. Recall that superscripts throughout this chapter denote the harmonic number and not an exponent.

Considering the assumptions for symmetric PSPWM in (4.12) and (4.13) as well as assuming equivalent flying capacitance in (4.14), each harmonic n of the characteristic matrix A can be separated into a product of a scalar and a matrix as

$$A^n = \gamma^n \, Q^n \tag{4.22}$$

where

$$\gamma^n = -\frac{8}{n^2\pi^2} \frac{\sin^2(n\pi d) \, \sin^2\left(\frac{n\pi}{p}\right)}{c \, |z^n|}, \tag{4.23}$$

and each element $k, i = 1, \ldots, m$ of the matrix Q^n is

$$Q^n_{ki} = \cos\left(\frac{2n\pi}{p}(i-k) - \phi_{zn}\right) \tag{4.24}$$

Each harmonic n of the input matrix B can also be separated as

$$B^n = \gamma^n \, R^n \tag{4.25}$$

where each element $k = 1, \ldots, m$ of the vector R^n is

$$R^n_k = \cos\left(\frac{2n\pi}{p}(2k+1) - \phi_{zn} + \frac{\pi}{2}\right) \tag{4.26}$$

Unfortunately since the scalar γ^n is a function of n, additional simplification of (4.5) and (4.6) requires additional approximation of the output impedance z^n. Utilizing the approximations for output impedance in (4.20) and (4.21), an expression for

$$\gamma^n = \alpha \, \beta^n \tag{4.27}$$

in (4.23) can be separated as

$$\alpha = \frac{8}{\pi^2 c \, \omega_s L} \tag{4.28}$$

$$\beta^n = -\frac{1}{n^3} \sin^2(n\pi d) \, \sin^2\left(\frac{n\pi}{p}\right) \tag{4.29}$$

Figure 4.4 shows β^n as a function of duty ratio d and harmonic n. From the contours, one can note the contribution of each A^n to the net sum of A with increasing harmonics—proportionally diminishing with $\frac{1}{n^3}\sin(\frac{n\pi}{p})^2$—as well as for specific duty ratios. This validates

the notion that harmonics of the load current i^n which are integer multiples of the effective switching frequency of the converter $f_\mathrm{e} = p \cdot f_\mathrm{s}$ do not influence capacitor balancing. Conversely, if the flying capacitor voltages are perfectly balanced then the only frequency content of i^n should be integer multiples of f_e.

It can be shown that if z is purely resistive (i.e., $\phi_{zn} = 0°$) then Q^n in (4.22) is symmetric and nonsingular, and if z is purely inductive (i.e., $\phi_{zn} = 90°$) then Q^n is skew-symmetric (anti-symmetric) and singular. Furthermore, since the sum of symmetric matrices is symmetric and the sum of skew-symmetric matrices is skew-symmetric, the aforementioned conditions for ϕ_{zn} also apply to A. These properties imply more inductive loads have slower balancing dynamics.

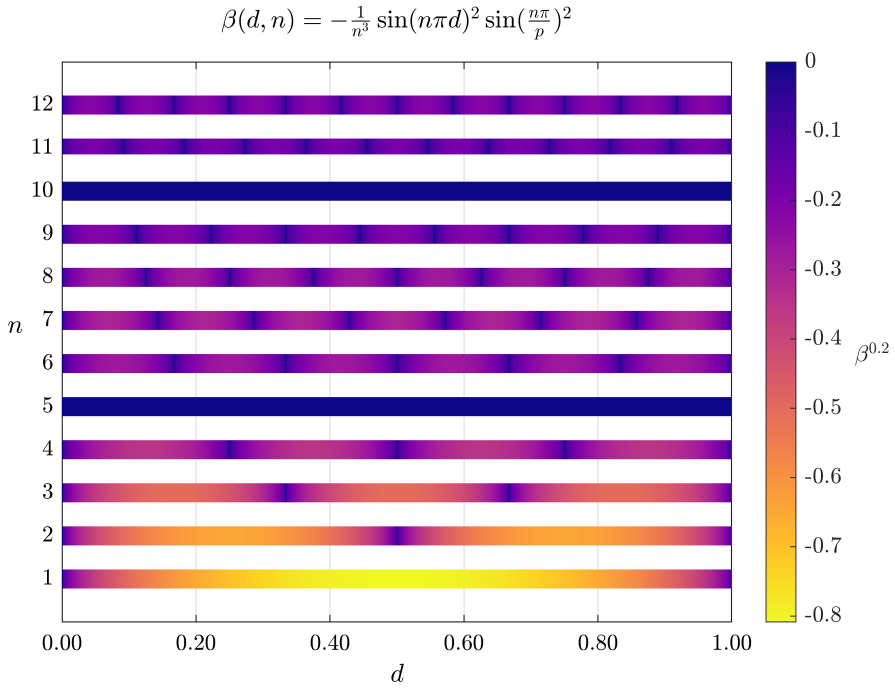


Figure 4.4: Values of $\beta(d, n)$ for the 6-level ($p = 5$) FCML.

3-Level Case

In the 3-level FCML case ($p = 2$), the state-space system becomes a first-order ordinary differential equation. Simplification and approximation of Q^n in (4.24) results in

$$\begin{aligned} Q^n &= \cos(\phi_{zn}) = \cos\left(\arctan\left(\frac{n\omega_\mathrm{s}L}{R_\mathrm{e}}\right)\right) \\ &\approx \frac{R_\mathrm{e}}{n\omega_\mathrm{s}L} \end{aligned} \tag{4.30}$$

thus A^n evaluates to

$$\begin{aligned} A^n &= \gamma^n \, Q^n = (\alpha \, \beta^n) \cdot Q^n \\ &= -\frac{8R_\mathrm{e}}{\pi^2 c \; \omega_\mathrm{s}^2 L^2} \cdot \frac{1}{n^4} \; \sin^2(n\pi d) \; \sin^2\!\left(\frac{n\pi}{p}\right) \end{aligned} \tag{4.31}$$

further evaluation of the net sum A simplifies to

$$\begin{aligned} A &= \sum_{n=1}^{r} A^n \\ &= \frac{-8R_\mathrm{e}}{\pi^2 c \; \omega_\mathrm{s}^2 L^2} \sum_{n=1}^{r} \left(\frac{1}{n^4} \; \sin^2(n\pi d) \; \sin^2\!\left(\frac{n\pi}{p}\right)\right) \\ &\approx -\frac{8R_\mathrm{e}}{\pi^2 c \; \omega_\mathrm{s}^2 L^2} \cdot \sin^2(\pi d) \end{aligned} \tag{4.32}$$

where the infinite sum is approximated with its first term harmonic ($n = 1$) since $0.01 \cdot A^1 \geq (A^3 + A^5 + \ldots)$ for all d.

This final result of A in (4.32) corresponds to the eigenvalue of the system (since $m = 1$). It also demonstrates that for the 3-level FCML, Meynard's state-space model can be fully reduced to describe the flying capacitor voltage dynamics as a function of circuit parameters and duty ratio. The proportionality of specific terms within the expression indicate the expected change in dynamics.

4.4 Dominant Time Constant

The dominant time constant τ_d of a high-order dynamical system is a real-valued scalar which indicates the time constant of decay for its equivalent first-order representation. This chosen value corresponds to the exponential decay rate from the dominant (or slowest) eigenvalue in the system. The goal is to analytically determine an expression for the dominant eigenvalue of A as a function of circuit parameters. If this cannot be done, then a viable approximation would be sufficient.

From inspection of (4.5) and (4.6) one can immediately come to the conclusion that a single analytical expression for the dominant eigenvalue of A is difficult. The infinite summation of harmonic matrices A^n ensures that even if eig$[A^n]$ can be evaluated, it cannot be used to evaluate eig$[A]$ itself. It can further be determined from inspection that A can be Hurwitz ($\mathrm{Re}(\lambda_i) < 0$ for all $\lambda_i \in \lambda_\mathrm{A}$, i.e., stable) while its harmonic components A^n are themselves not Hurwitz (unstable). There are however some harmonic contributions A^n which dominate the dominant eigenvalue of A and this expectation could lead to a finite approximation of eig$[A]$. The relative contribution of each harmonic A^n to the overall eigenvalue of A is correlated to the scaling function β^n in (4.29).

To demonstrate the effective time constant of the system is approximately the dominant time constant τ_{A} of A, consider the general analytical solution for the instantaneous voltages $V_{\mathrm{C}}(t)$. First consider the general solution of the state-space system in (4.3) and then the homogeneous solution for the LTI system which describes natural dynamics without external input (i.e., $v_{\mathrm{in}} = 0$)

$$\begin{aligned} V_{\mathrm{C}}(t) &= \Phi(t, t_0)\ V_{\mathrm{C}}(0) + \int_{t_0}^{t} \Phi(t, \xi) B(\xi) v_{\mathrm{in}}(\xi) d\xi \\ &= e^{A(t-t_0)}\ V_{\mathrm{C}}(0) + \cancel{\int_{t_0}^{t} e^{A(t-\xi)} B\ v_{\mathrm{in}}(\xi)\ d\xi} \\ &= e^{At}\ x(0) \end{aligned} \tag{4.33}$$

By evaluating the matrix exponential e^{At}, each flying capacitor voltage $k = 1, \ldots, m$ then has the form

$$\begin{aligned} V_{\mathrm{C}_k}(t) &= \sum_{\lambda_{\mathrm{A}}} a_{i,k}\ e^{\lambda_i t} = \sum_{\lambda_{\mathrm{A}}} a_{i,k}\ e^{\sigma_i t} \cos(\omega_i t) \\ &\approx a_{d,k}\ e^{\sigma_{\mathrm{d}} t} = a_{d,k}\ e^{-\frac{t}{\tau_{\mathrm{A}}}} \end{aligned} \tag{4.34}$$

for each real or complex-pair eigenvalue $\lambda_i = \sigma_i \pm j\omega_i$ in λ_{A} and where $a_{i,k}$ is an arbitrary scalar. Since at least one of these eigenvalues must be dominant, each flying capacitor voltage can be approximated as a first-order LTI system with a single exponential function with decay equivalent to the dominant time constant. Approximation of the state-transition matrix in (4.33) utilizing (4.34) yields

$$\Phi(t, t_0) = e^{A(t-t_0)} \approx e^{-\left(\frac{t-t_0}{\tau_{\mathrm{A}}}\right)} \cdot I \tag{4.35}$$

where I is an m-by-m identity matrix. A similar first-order reduction of the system is implied in [186].

Figure 4.5 represents an exemplar discretized simulation of the state-space model. Superimposed on these waveforms is the first-order reduced model determined by substituting (4.35) into (4.33) with time constant equivalent to the effective time constant of the higher order system.

Additional Simplification of Symmetric PSPWM

By revisiting the case of symmetric PSPWM, the expression for A^n in (4.22) can be further condensed. The overall characteristic matrix A can be simplified by substituting (4.28) and (4.29) into (4.22) and then subsequently (4.5)

$$A = \sum_{n=1}^{r} A^n = \alpha \sum_{n=1}^{r} \beta^n\, Q^n = \alpha \sum_{n=1}^{r} A'^{\,n} = \alpha A'. \tag{4.36}$$

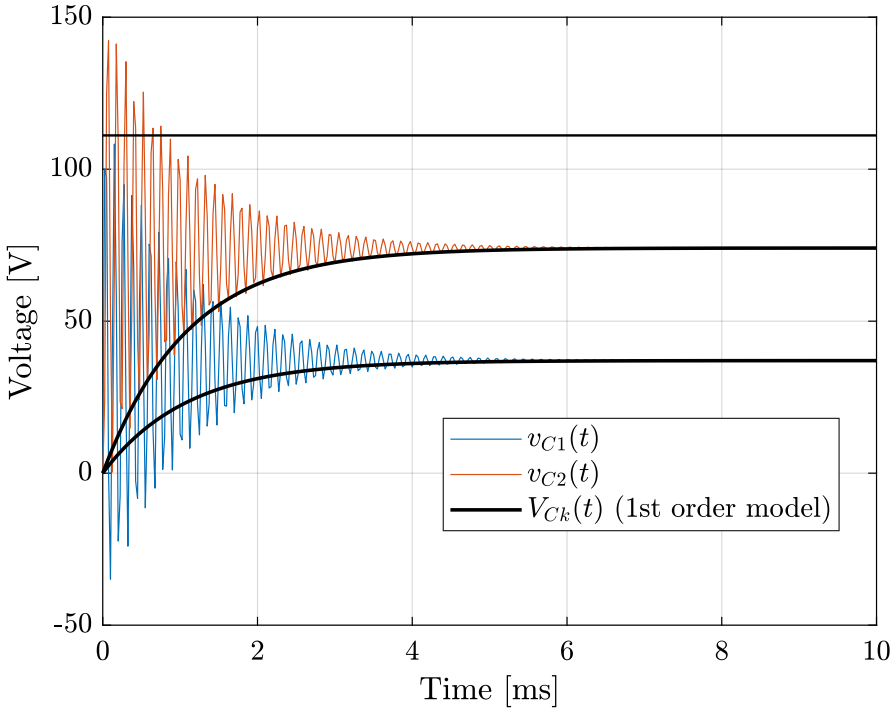


Figure 4.5: Simulated results for the 4-level FCML with symmetric PSPWM. Includes first-order reduced model with effective time constant $\tau = 1.09$ ms. Parameters: $v_{\text{in}} = 100\,\text{V}$, $d = 0.45$, $L = 2.8\,\mu\text{H}$, $R_{\text{e}} = 10\,\text{m}\Omega$, $C_{\text{out}} = 10\,\text{mF}$, $R_{\text{L}} = 1\,\Omega$, and $f_{\text{s}} = 40\,\text{kHz}$.

The following theorem relates the eigenvalues of scalar multiples of a matrix:
Theorem 1: Suppose X is a square matrix, λ_X is the spectrum of X, and α is a scalar. Then $\alpha\lambda_X$ is the spectrum of αX.

By utilizing this theorem

$$\lambda_{\text{A}} = \text{eig}[\alpha A'] = \alpha \cdot \text{eig}[A'] = \alpha \cdot \lambda_{A'}. \tag{4.37}$$

This factorization can be extended to the dominant time constant by substituting (4.37) into (4.11)

$$\tau_{\text{A}} = \frac{1}{\alpha}\tau_{A'} = \frac{\pi^2 c\ \omega_{\text{s}} L}{8}\tau_{A'}. \tag{4.38}$$

There is currently not an explicit symbolic formula for $\tau_{A'}(d, N)$, but by numerically evaluating eigenvalues of A' we can visually inspect this function and determine unstable duty ratios d_u. The results of this analysis for every $N \leq 10$ are shown in Fig. 4.6. Although not demonstrated here, adjustment of circuit parameters L, R_{e} and ω_{s}, which impact ϕ_{zn} from (4.21), merely shift the magnitude of $\tau_{A'}(d, N)$ and not the function shape. This implies that the wave shapes in Fig. 4.6 are unique to the FCML converter topology and its chosen modulation strategy—in this case symmetric PSPWM.

Also because of the nonlinear nature of the minimum function in (4.11), the function $\tau_{A'}(d, N)$ for some N is not completely differentiable with d. This property represents different eigenvalues dominating for different regions of d and further complicates explicit symbolic formulation.

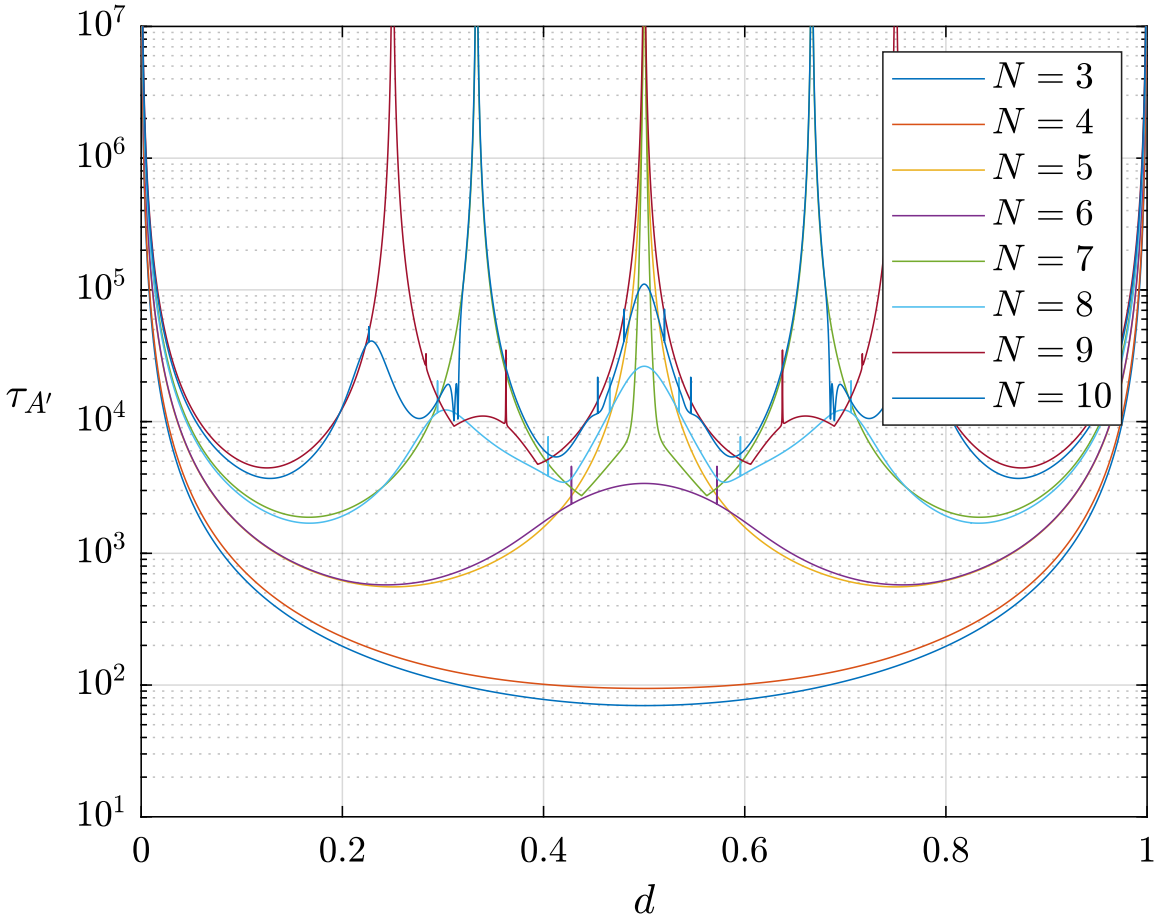


Figure 4.6: Functions of $\tau_{A'}(d, N)$ for duty ratio d and number of FCML levels N with symmetric PSPWM. Parameters: $L = 2.8$ μH, $R_e = 10$ mΩ, and $f_s = 40$ kHz.

Unstable Duty Ratios

Depending on the number of levels N, there are certain duty ratios which result in system instability ($\tau_A \to \infty$). For example, by inspecting Fig. 4.6 it can be determined that an FCML circuit operating at a $d = \frac{1}{3}$ duty cycle has unstable flying capacitor voltages ($\tau_{A'} \to \infty$) for the $N = 7$ and 10 levels converters but is stable for $N = 3$, 4, 5, 6, 8, and 9 level

converters. From inspection, for non-prime $p = N - 1$ there is always at least one unstable duty ratio besides the trivial values of $d = 0$ or 1. Stated another way, FCML converters with prime $p = N - 1$ are the most consistently stable for all duty ratios. Additionally, for larger N the function of $\tau_{A'}(d, N)$ becomes generally more complicated and contains more unstable duty ratios.

These results are partially, but not entirely consistent with those found by Wilkinson in [185, 186] which states that

- If $p = N - 1$ is prime: the only unstable duty ratios occur at 0 and 1.
- If $p = N - 1$ is not prime: In addition to $d = 0$ and 1, unstable duty ratios occur at multiples of the reciprocal of prime factors q of p. More specifically, for each prime factor q of p, then $d = \frac{i}{q}$ for $i = 0, \ldots, q$ are unstable duty ratios.

From inspection of $\tau_{A'}(d, N)$ in Fig. 4.6, these constraints are found to be too strict. For example in the 13-level converter ($p = 12$), the conclusion in [185] results in unstable duty ratios at $d = \{0, \frac{1}{3}, \frac{1}{2}, \frac{2}{3}, 1\}$. However from inspection of $\tau_{A'}(d, 13)$, unstable duty ratios occur at $d = \{0, \frac{1}{6}, \frac{1}{4}, \frac{1}{3}, \frac{1}{2}, \frac{2}{3}, \frac{3}{4}, \frac{5}{6}, 1\}$. This disparity likely arises from Wilkinson's limitation on FCML converters with "practical" level count as he only considered cases where $N < 8$.

Generally, for every N-level converter unstable duty ratios d_u occur at multiples of the reciprocal of the factors q of $p = N - 1$. In other words for each factor q of p,

$$d_u = \frac{1}{q}\, i \qquad \text{for all } i = 0, \ldots, q \tag{4.39}$$

This result can be used to determine appropriate choice of N in the design of an FCML operating at a desired conversion ratio (and thus duty ratio).

Special Cases

There are specific cases of effective time constant τ_{A} worth investigating further. For the 3-level converter case, τ_{A} can be explicitly derived by substituting (4.32) into (4.11)

$$\tau_{\mathrm{A}}(d, 3) = \frac{\pi^2 c\ \omega_{\mathrm{s}}^2 L^2}{8\ R_{\mathrm{e}}} \csc^2(\pi d) \tag{4.40}$$

This appears to be the simplification of the effective time constant τ within [187] when assuming the output impedance as (4.20) and (4.21).

This result appears notably different in form to [148] which maintains that $\tau_{\mathrm{A}}(d, 3)$ is a rational rather than a transcendental function of d derived in (4.40), however closer inspection yields these two results are approximately equal.

For the 4-level case, the numerically evaluated solutions for τ'_{A} in Fig. 4.6 can be visually inspected to realize $\tau_{\mathrm{A}}(d, 4)$ is directly proportional to $\csc^2(\pi d)$ or

$$\tau_{\mathrm{A}}(d, 4) \propto (\alpha\ \csc^2(\pi d)). \tag{4.41}$$

For the 5-level case, a similar process of visual inspection can be used to determine $\tau_{\mathrm{A}}(d,5)$ is directly proportional to $\csc^2(2\pi d)$ or

$$\tau_{\mathrm{A}}(d,5) \propto (\alpha \csc^2(2\pi d)). \tag{4.42}$$

The function $\tau_{\mathrm{A}}(d,5)$ notably has a vertical asymptote at $d = 0.5$ which corresponds to an unstable duty ratio value.

4.5 Future Improvements and Conclusions

This chapter introduces and simplifies the state-space averaged dynamical model derived in [114]. The model excels in many regards: its simple reproducibility, ability to account for complicated load impedances, ability to derive closed-form approximations for time-constants for low level counts, possibility for numerically estimating steady-state imbalance, and most importantly its ability to produce nontrivial dynamical behavior for the flying capacitor voltages. There are a number of further improvements which can be made to the analysis presented in this work.

A number of asymmetric PSPWM techniques have been proposed and validated in literature, but it remains to be seen whether the associated state-space model accurately represents the actual dynamics. One such desirable test case is the use of asymmetric (versus passive symmetric) modulation to increase the rate of flying capacitor balancing during level transitioning [20, 164].

Meynard's averaged model excels at accommodating complicated variations of the output impedance since it is lumped. Cleverly adjusting the output impedance z of the FCML results in a reduction of the effective or dominant time constant τ_{d} and higher-order dynamics. The balance booster is one such circuit proposed in [114] and analyzed further in [187, 153, 160] which acts as a physical method to short a particular harmonic n of z^n. Proper choice in the harmonic (typically $n = 1$) effectively eliminates the contribution of that harmonic to the overall spectrum λ_{A}. Physically, the balance booster circuit is shunting a single current harmonic directly to ground instead of letting it pass through the buck inductor L. Shunted harmonic currents are still present in the flying capacitors as they are necessary for faster voltage balancing.

Often the dominant eigenvalue(s) of A are a complex conjugate pair since ϕ_{zn} is primarily inductive. Consequently, a second-order reduced model of the state-space system which describes the dominant oscillations and overshoot of the flying capacitor voltages is possible. Such an analysis has been performed and experimentally validated in [105]. Chapter 5 further investigates numerical computation for the frequency of this dominant resonance mode.

Adjustment of Meynard's FCML circuit model could also help quantify the impact of non-idealities on steady-state voltage error. Incorporation of the voltage harmonics on the input capacitor would be an example [194, 140].

Finally, work in [113] also delves into implications of the model presented in [114] and identifies similar extensions and simplification compared to those presented in this chap-

ter. These serve as an alternatively expressed, yet independent validation of the principles presented in this chapter.

Chapter 5

Discrete-Time State-Space Modeling for the FCML Converter

5.1 Introduction

In the previous Chapter 4, a prominent and easily implementable averaged modeling approach for the FCML converter is presented. However, although powerful in significant respects, the major shortcoming to this model is that it does not adequately describe certain practical realizations of the FCML converter, especially at duty ratios of theoretical instability as noted in [185, 16]. Inspired by the work in [189, 188, 190], this chapter proposes a different modeling approach. It derives analytical expressions which both accurately characterize the buck-type FCML circuit dynamics and clarify aspects of the natural behavior of the FCML topology. Although the derived model presupposes conventional symmetric phase-shifted pulse-width modulation (PS-PWM), the employed modeling methodology applies to any arbitrary switching scheme, including those corresponding to resonant operation of the converter [141, 26, 1, 51] or those with redundant switching states [188, 66]. The resultant discrete-time LTI state-space model fully captures the dynamical behavior of the FCML converter, especially through its ability to model critical time-domain behaviors of the transistors such as output capacitance C_{oss} charge redistributions [17] and clamping of the reverse conduction diodes. Section 5.2 describes the full methodology of the proposed model from derivation of the reduced circuit to the final cycle-to-cycle LTI state-space form. Section 5.3 analyzes the eigenvalues of the resultant discrete-time LTI system, garnering insight into the operating point dependence of natural balancing as well as practical limits on natural balancing performance. Section 5.4 validates the analytical model against measured results from a high-performance hardware prototype.

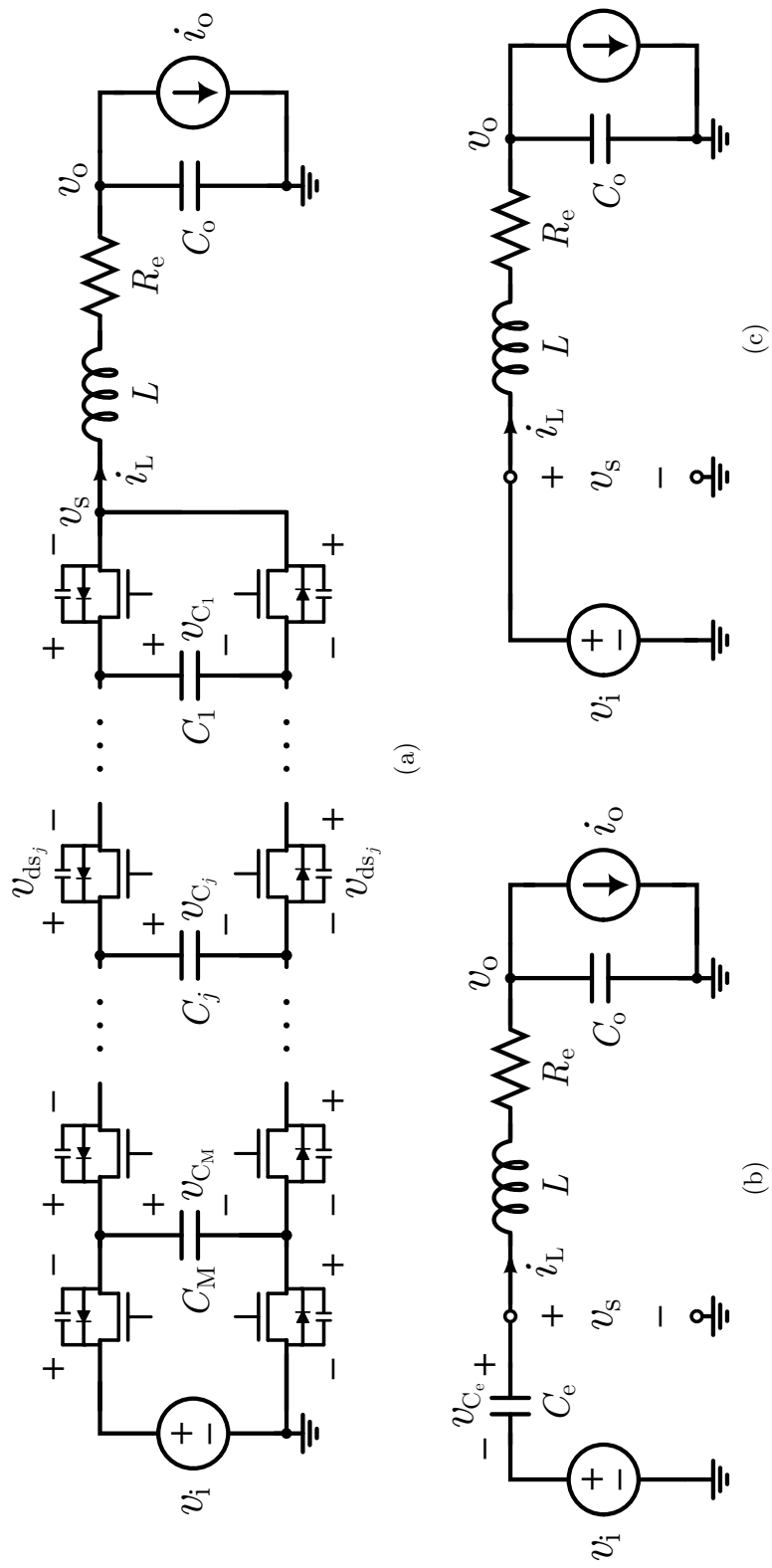


Figure 5.1: (a) General N-level FCML circuit schematic and its equivalent reduced circuit model for switching state (b) with ('Circuit A') and (c) without series connected flying capacitor ('Circuit B').

5.2 Modeling Methodology

Under PS-PWM—wherein the PWM waveforms applied to complimentary switch pairs have various duty ratios and phase-shifts [114]—the FCML topology shown in Fig. 5.1a is a switched periodic system. Thus its natural dynamics are described by a linear time-varying (LTV) state-space representation

$$\dot{\vec{x}}(t) = \vec{A}(t) \cdot \vec{x}(t) + \vec{B}(t) \cdot \vec{u}(t) \tag{5.1}$$

where the impact of switching is captured by the time-dependence of $\vec{A}$ and $\vec{B}$. For this system, the state vector $\vec{x} = [v_{\mathrm{C_1}},\ ...,\ v_{\mathrm{C_M}},\ i_{\mathrm{L}},\ v_{\mathrm{o}}]^\top$ comprises voltages and currents of the energy storage elements and the input vector $\vec{u} = [v_{\mathrm{i}},\ i_{\mathrm{o}}]^\top$ comprises the input voltage and the load current.

Analytically solving this LTV system is a nontrivial ordeal and generally does not yield a closed-form result. However, since $\vec{A}(t)$ and $\vec{B}(t)$ are piecewise-constant with respect to individual switch states, the problem is divided into more tractable time-cascaded linear time-invariant (LTI) circuits of each switching phase (or 'per-phase'). These per-phase LTI circuits may be solved numerically using expressions involving matrix exponentials (of the form $e^{\vec{A}t}$) of the constant matrices over their respective on-time intervals. However, this approach often requires numerical methods to compute diagonalizations or Jordan decompositions. By contrast, the proposed modeling process constructs a minimum-complexity FCML circuit model that is second-order and derives an algebraic solution for the per-phase state dynamics.

Regardless of the utilized method, once the instantaneous per-phase dynamics are derived, they are evaluated at the phase transitions by discretization and recombined—by a process referred to in this work as "lifting"—into a discrete-time LTI state-space representation per switching cycle (or 'per-cycle') k:

$$\vec{x}[k+1] = \vec{A}_{\mathrm{d}} \cdot \vec{x}[k] + \vec{B}_{\mathrm{d}} \cdot \vec{u}[k]. \tag{5.2}$$

This general discrete per-cycle LTI representation has enormous utility, as it describes the dynamical properties of the converter via eigenanalysis of $\vec{A}_{\mathrm{d}}$; allows for analytical determination of steady-state error, a significant concern highlighted in [197, 140]; and presents a discrete-time plant model for subsequent controller design.

This section details the modeling process from a generic FCML circuit to a cycle-to-cycle discrete-time state-space description of the state voltage and current dynamics.

Step 1: Analytically Describe Circuit

First, the multiple switching phase (or multi-phase) FCML circuit is abstracted into a reduced circuit model. Assuming linear circuit components, the voltage and current dynamics of the FCML circuit in Fig. 5.1a constitute a piecewise-linear system abruptly transitioning between many switched circuits. The system is equivalently reduced to either 'Circuit A' in

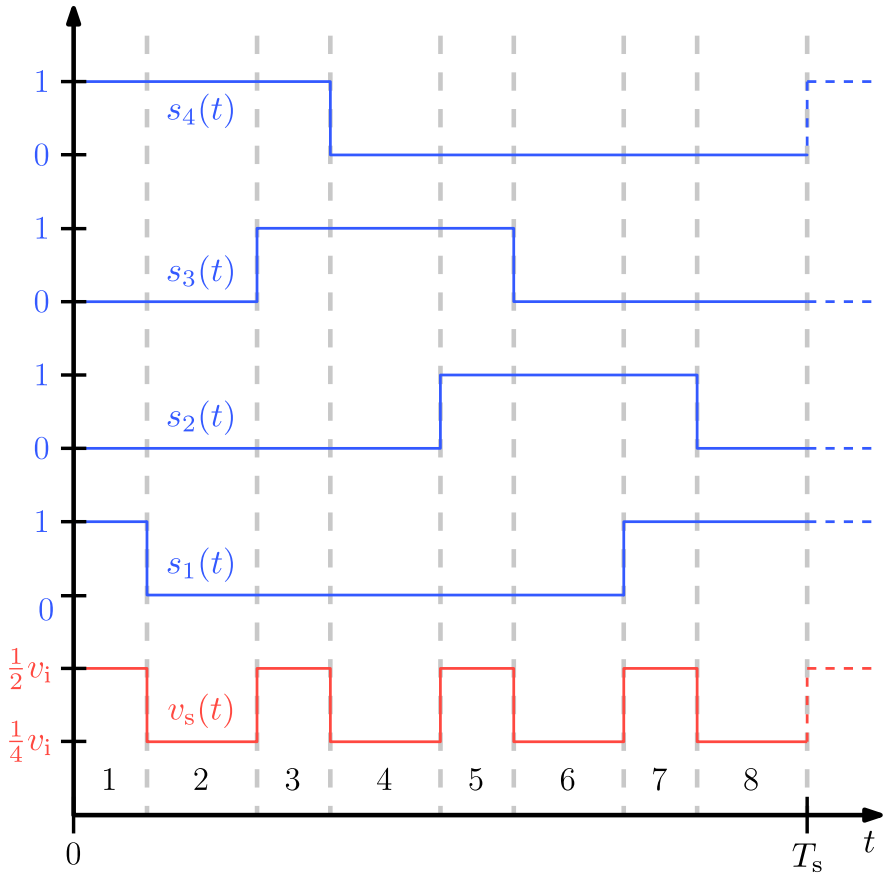


Figure 5.2: Timing diagram of FCML modulation in symmetric PS-PWM. Illustration of switching signals $s_j(t)$ and switching node voltage $v_\mathrm{s}(t)$ for exemplar $N = 5$ level count and $D = 0.35$ duty ratio.

Fig. 5.1b or 'Circuit B' in Fig. 5.1c depending on the state of the converter switches; and the input voltage v_i is equal to 0 V in switching states where it is not connected. This reduction holds for every possible switching phase as long as the equivalent flying capacitor C_e is constructed appropriately from its constituent flying capacitors C_j. The ordinary differential equations (ODEs) describing the reduced circuits are derived as

$$L\frac{\mathrm{d}}{\mathrm{d}t}i_\mathrm{L} + R_\mathrm{e}i_\mathrm{L} + v_\mathrm{o} - v_\mathrm{i} - v_{\mathrm{C_e}} = 0 \tag{5.3}$$

$$C_\mathrm{o}\frac{\mathrm{d}}{\mathrm{d}t}v_\mathrm{o} - i_\mathrm{L} + i_\mathrm{o} = 0 \tag{5.4}$$

The converter cycles through several combinations of switch states over a switching period. Each distinct combination of switch states is deemed a unique *switching phase*. Similar

to the procedures described in [188, 173, 129], the sequence of switching phases over a switching period and the corresponding capacitor connections are constructed from a given set of switching signals applied to the converter. This procedure is fully exemplified here.

Fig. 5.2 shows switching signals and the corresponding switched node voltage waveform for a 5-level FCML converter operating at duty ratio of $D = 0.35$. The switching phases, numbered 1 through 8, are annotated on the switched node voltage waveform. In the nth switching phase, the switch states—taking a value of 0 or 1—can be collected into a switching state vector $\vec{s}[n] := [s_1, s_2, \ldots, s_{\text{N-1}}]^\top$. The distinct switching state vectors for all P distinct switching phases are collected into a switching state matrix $\vec{S}$:

$$\begin{aligned}\vec{S} &:= \begin{bmatrix} \vec{s}[1] & \vec{s}[2] & \vec{s}[3] & \vec{s}[4] & \vec{s}[5] & \vec{s}[6] & \vec{s}[7] & \vec{s}[8] \end{bmatrix} \\ &= \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}.\end{aligned}$$

As described in [188] and [129], the row-difference of the matrix $\vec{S}$ yields the capacitor connection matrix $\vec{C}$:

$$\begin{aligned}\vec{C} &:= \begin{bmatrix} \vec{c}[1] & \vec{c}[2] & \vec{c}[3] & \vec{c}[4] & \vec{c}[5] & \vec{c}[6] & \vec{c}[7] & \vec{c}[8] \end{bmatrix} \\ &= \begin{bmatrix} 1 & 0 & 0 & 0 & -1 & -1 & 0 & 1 \\ 0 & 0 & -1 & -1 & 0 & 1 & 1 & 0 \\ -1 & -1 & 0 & 1 & 1 & 0 & 0 & 0 \end{bmatrix}.\end{aligned} \tag{5.5}$$

The columns $\vec{c}[n]$ of this matrix indicate the connection and orientation of series-connected capacitors to the switching node v_{s} in each switching phase. Similarly, an input connection row vector $\vec{j}$—dependent on the state of switching signal $s_{\text{N-1}}$—indicates whether the input voltage source v_{i} is connected to the series-capacitor branch in each phase n. For the example above, this vector $\vec{j}$ is given by

$$\begin{aligned}\vec{j} &:= \begin{bmatrix} j[1] & j[2] & j[3] & j[4] & j[5] & j[6] & j[7] & j[8] \end{bmatrix} \\ &= \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}\end{aligned} \tag{5.6}$$

Finally, a matrix of flying capacitor *elastances* [21] (the inverse of capacitance) is defined as

$$\vec{E} := \begin{bmatrix} \frac{1}{C_1} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & \frac{1}{C_{\text{M}}} \end{bmatrix} \tag{5.7}$$

and used to subsequently define the charge transfer matrix, $\vec{G}$ as

$$\begin{aligned}\vec{G} &:= \vec{E}\vec{C} \\ &:= \begin{bmatrix} \vec{g}\,[1] & \vec{g}\,[2] & \vec{g}\,[3] & \vec{g}\,[4] & \vec{g}\,[5] & \vec{g}\,[6] & \vec{g}\,[7] & \vec{g}\,[8] \end{bmatrix} \\ &= \begin{bmatrix} \frac{1}{C_1} & 0 & 0 & 0 & -\frac{1}{C_1} & -\frac{1}{C_1} & 0 & \frac{1}{C_1} \\ 0 & 0 & -\frac{1}{C_2} & -\frac{1}{C_2} & 0 & 1 & \frac{1}{C_2} & 0 \\ -\frac{1}{C_3} & -\frac{1}{C_3} & 0 & \frac{1}{C_3} & \frac{1}{C_3} & 0 & 0 & 0 \end{bmatrix}\end{aligned} \tag{5.8}$$

In switching phases reducible to Circuit A in Fig. 5.1b, the instantaneous charge $q(t)$ stored on the equivalent flying capacitance C_e

$$q(t) = -C_\mathrm{e}\, v_{\mathrm{C_e}}(t) \tag{5.9}$$

is related to the charge and current flow through the inductor

$$i_\mathrm{L}(t) = \frac{\mathrm{d}}{\mathrm{d}t} q(t) \tag{5.10}$$

where $q(0)$ indicates the charge stored on the equivalent flying capacitor at the start of the nth switching phase. The capacitance of C_e in the nth switching phase is derived from the nth column of the charge-transfer matrix $\vec{G}$ as

$$C_\mathrm{e} := \left(\left\|\vec{g}\,[n]\right\|_1\right)^{-1} \tag{5.11}$$

where $||\cdot||_1$ is vector the L^1-norm. The equivalent capacitor voltage $v_{\mathrm{C_e}}(t)$ is algebraically constructed from the nth column of the capacitor matrix $\vec{C}$ and the vector of flying capacitor voltages $v_\mathrm{C}(t)$:

$$v_{\mathrm{C_e}}(t) = \vec{c}\,[n]^\top \vec{v}_\mathrm{C}(t). \tag{5.12}$$

$$a(t) = \frac{\omega_\mathrm{o}}{\omega_\mathrm{d}} e^{-\alpha t} \cos(\omega_\mathrm{d} t + \theta) \tag{A1}$$

$$b(t) = \frac{1}{\omega_\mathrm{d} L} e^{-\alpha t} \sin(\omega_\mathrm{d} t) \tag{A2}$$

$$c(t) = -\frac{1}{\omega_\mathrm{d} L} e^{-\alpha t} \sin(\omega_\mathrm{d} t) \tag{A3}$$

$$d(t) = -\frac{C_\mathrm{z}}{C_\mathrm{o}} \left(\frac{\omega_\mathrm{o}}{\omega_\mathrm{d}}\, e^{-\alpha t} \left(\frac{2\alpha}{\omega_\mathrm{o}} \sin(\omega_\mathrm{d} t) + \cos(\omega_\mathrm{d} t + \theta) \right) - 1 \right) \tag{A4}$$

$$e(t) = \frac{1}{C_\mathrm{o}} \tag{A5}$$

$$f(t) = -\frac{1}{C_\mathrm{o}} t \tag{A6}$$

$$\mathcal{A}(t) = \frac{1}{\omega_\mathrm{d}} e^{-\alpha t} \sin(\omega_\mathrm{d} t) \tag{A7}$$

$$\mathcal{B}(t) = -C_\mathrm{z} \left(\frac{\omega_\mathrm{o}}{\omega_\mathrm{d}}\, e^{-\alpha t} \cos(\omega_\mathrm{d} t - \theta) - 1 \right) \tag{A8}$$

$$\mathcal{C}(t) = C_\mathrm{z} \left(\frac{\omega_\mathrm{o}}{\omega_\mathrm{d}}\, e^{-\alpha t} \cos(\omega_\mathrm{d} t - \theta) - 1 \right) \tag{A9}$$

$$\mathcal{D}(t) = \frac{C_\mathrm{z}}{C_\mathrm{o}} \left(\frac{1}{\omega_\mathrm{d}}\, e^{-\alpha t} \left(\frac{2\alpha}{\omega_\mathrm{o}} \cos(\omega_\mathrm{d} t - \theta) - \sin(\omega_\mathrm{d} t) \right) + t - \frac{2\alpha}{\omega_\mathrm{o}^2} \right) \tag{A10}$$

$$C_\mathrm{z} = \begin{cases} \dfrac{C_\mathrm{e} C_\mathrm{o}}{C_\mathrm{e} + C_\mathrm{o}} & \text{Circuit A} \\ C_\mathrm{o} & \text{Circuit B} \end{cases} \tag{B1}$$

$$\alpha = \frac{R_\mathrm{e}}{2L} \tag{B2}$$

$$\omega_\mathrm{o} = \frac{1}{\sqrt{L C_\mathrm{z}}} \tag{B3}$$

$$\omega_\mathrm{d} = \sqrt{\omega_\mathrm{o}^2 - \alpha^2} \tag{B4}$$

$$\theta = \arcsin\left(\frac{\alpha}{\omega_\mathrm{o}} \right) \tag{B5}$$

$$\vec{\phi}_n(t,0) = \begin{bmatrix} \left(\vec{I} + \mathcal{B}(t)\,\vec{g}\,[n]\,\vec{c}\,[n]^\top\right)\left(\vec{I} + \vec{X}[n]\right) & \mathcal{A}(t)\,\vec{g}\,[n] & \mathcal{C}(t)\,\vec{g}\,[n] \\ b(t)\,\vec{c}\,[n]^\top\left(\vec{I} + \vec{X}[n]\right) & a(t) & c(t) \\ e(t)\,\mathcal{B}(t)\,\vec{c}\,[n]^\top\left(\vec{I} + \vec{X}[n]\right) & e(t)\,\mathcal{A}(t) & 1 + e(t)\,\mathcal{C}(t) \end{bmatrix} \tag{C1}$$

$$\vec{\psi}_n(t,0) = \begin{bmatrix} \mathcal{B}(t)\,\vec{g}\,[n]\left(j[n] + \vec{c}\,[n]^\top\vec{y}\,[n]\right) + \vec{y}\,[n] & \mathcal{D}(t)\,\vec{g}\,[n] \\ b(t)\left(j[n] + \vec{c}\,[n]^\top\vec{y}\,[n]\right) & d(t) \\ e(t)\,\mathcal{B}(t)\left(j[n] + \vec{c}\,[n]^\top\vec{y}\,[n]\right) & f(t) + e(t)\,\mathcal{D}(t) \end{bmatrix} \tag{C2}$$

Step 2: Construct Per-Phase Model – Switching Network

For each phase n, the full continuous-time solution for all relevant voltages and currents is expressed as a system of impedance equations and a system of switching equations [188] relative to the beginning of the switching phase at $t = 0$.

The system of switching equations

$$v_{\mathrm{s}}(t) = \vec{c}\,[n]^\top\vec{v}_{\mathrm{C}}(t) + j[n]\,v_{\mathrm{i}} \tag{5.13}$$

$$\vec{v}_{\mathrm{C}}(t) = \vec{v}_{\mathrm{C}}(0) + \vec{g}\,[n]\,\Delta q(t) + \left(\vec{X}[n]\,\vec{v}_{\mathrm{C}}(0) + \vec{y}\,[n]\,v_{\mathrm{i}}\right) \tag{5.14}$$

fully describes the switched-capacitor network where $v_{\mathrm{s}}(t)$ is the instantaneous switching node voltage and v_{i} is the input voltage. The net change in charge throughout the phase, $\Delta q(t) = q(t) - q(0)$, aids the formulation of the switched-capacitor circuit equations since it is related algebraically, rather than differentially, to the change in voltages of the flying capacitors as in (5.9). Matrix $\vec{X}[n]$ and vector $\vec{y}\,[n]$ incorporate the influence of C_{oss} impulse charge redistribution among the flying capacitors and general formulations are expressed in Section 5.5. Additional work in [17] explores the impact of finite C_{oss} on the capacitor voltages as a crucial balancing mechanism.

Step 3: Construct Per-Phase Model – Impedance Network

A general analytical solution can be explicitly derived for the circuit states (i.e., $v_{\mathrm{C_1}}$,..., $v_{\mathrm{C_M}}$, i_{L}, v_{o}) because the system of ODEs for the reduced circuits are second-order and the inputs (i.e., v_{i} and i_{o}) are assumed constant within each switching phase. To solve this system, the

inductor current ODE in (5.3) is expressed in terms of cumulative charge flowing through the inductor as defined in (5.10).

Integrating the output voltage ODE in (5.4) produces a general solution for the output voltage $v_\mathrm{o}(t)$

$$\begin{aligned} v_\mathrm{o}(t) &= v_\mathrm{o}(0) + \frac{1}{C_\mathrm{o}} q(t) - \frac{1}{C_\mathrm{o}} q(0) - \frac{1}{C_\mathrm{o}} t \cdot i_\mathrm{o} \\ &= v_\mathrm{o}(0) + \boldsymbol{e}(t)\, \Delta q(t) + \boldsymbol{f}(t)\, i_\mathrm{o}. \end{aligned} \tag{5.15}$$

Substitution of (5.15) and (5.10) into (5.3) produces a second-order ordinary differential equation

$$\frac{\mathrm{d}^2}{\mathrm{d}t^2} q(t) + \frac{R_\mathrm{e}}{L} \frac{\mathrm{d}}{\mathrm{d}t} q(t) + \frac{1}{LC_\mathrm{z}} q(t) = \frac{1}{L} v_\mathrm{i} + \frac{1}{LC_\mathrm{o}} q(0) - \frac{1}{L} v_\mathrm{o}(0) + \frac{1}{LC_\mathrm{o}} t\, i_\mathrm{o}. \tag{5.16}$$

The solution to this ODE

$$\Delta q(t) = \boldsymbol{\mathcal{A}}(t)\, i_\mathrm{L}(0) + \boldsymbol{\mathcal{B}}(t)\, v_s(0) + \boldsymbol{\mathcal{C}}(t)\, v_\mathrm{o}(0) + \boldsymbol{\mathcal{D}}(t)\, i_\mathrm{o} \tag{5.17}$$

is defined in terms of initial conditions at the beginning of the phase ($t = 0$) and scalar functions of time in (A1) – (A10) with parameters (B1) – (B5). Time-differentiating the continuous-time charge expression $\Delta q(t)$ in (5.17) results in the solution for the continuous-time inductor current

$$i_\mathrm{L}(t) = \boldsymbol{a}(t)\, i_\mathrm{L}(0) + \boldsymbol{b}(t)\, v_s(0) + \boldsymbol{c}(t)\, v_\mathrm{o}(0) + \boldsymbol{d}(t)\, i_\mathrm{o} \tag{5.18}$$

For Circuit B without equivalent flying capacitor C_e, the solution is of similar form to that of Circuit A except the total capacitance C_z is only the output capacitance: $C_\mathrm{z} = C_\mathrm{o}$.

In summary, the switching network in (5.13) and (5.14) and the impedance network in (5.15), (5.17), and (5.18) are coupled only by the flow of charge $\Delta q(t)$ through the flying capacitors and the switching node voltage $v_\mathrm{s}(t)$ applied across the output impedance. The necessary model inputs are the characteristic 'switching matrix' $\vec{S}$ in (5.5) and a vector comprised of phase durations $\Delta t[n]$—both generated from a periodic modulation strategy; initial conditions for state voltages and currents $\vec{x}(0)$; the input voltage v_i and output current i_o; and the circuit parameters: C_1, C_2, …, C_M, L, R_e, C_o, C_oss.

Step 4: Convert to Per-Phase Continuous State-Transition Matrix

The system of equations in (5.13), (5.14), (5.15), (5.17) and (5.18) are algebraically converted to an analytical solution represented by a state-transition equation

$$\vec{x}(t) = \vec{\phi}_n(t, 0) \cdot \vec{x}(0) + \vec{\psi}_n(t, 0) \cdot \vec{u} \tag{5.19}$$

where $\vec{\phi}_n(t, 0)$ and $\vec{\psi}_n(t, 0)$ are concisely expressed as (C1) and (C2), respectively. The state and input-transition matrices $\vec{\phi}_n(t, 0)$ and $\vec{\psi}_n(t, 0)$ describe the evolution of the circuit states

throughout phase n. Note the influence of the switching information in $\vec{c}\,[n]$, $j[n]$, $\vec{g}\,[n]$, $\vec{X}[n]$, and $\vec{y}[n]$, which update the state and input-transition matrices according to the particular switching phase. This vector equation describes the continuous circuit behavior in each switching phase without loss of information.

The continuous-time state-space solution (5.19) is conventionally evaluated using a more general (but computationally intensive) matrix exponential method [29]. Section 5.6 outlines this analysis for an a FCML circuit model with load resistance and input capacitance—an augmentation of interest for voltage balancing [197].

Step 5: Discretize the Per-Phase Continuous Dynamics

Given the eventual goal of cycle-to-cycle converter dynamics, the continuous-time per-phase dynamics are discretized at switching transitions by evaluating (5.19) at the time duration of each phase, $\Delta t[n]$:

$$\begin{aligned} \vec{x}[n+1] = &\quad \vec{\phi}_n(\Delta t[n], 0) \cdot \vec{x}[n] &+ &\quad \vec{\psi}_n(\Delta t[n], 0) \cdot \vec{u}[n] \\ = &\quad \vec{\phi}[n] \cdot \vec{x}[n] &+ &\quad \vec{\psi}[n] \cdot \vec{u}[n]. \end{aligned} \tag{5.20}$$

This result is a discrete-time system that is variable-rate since the switching phases are not typically of equal duration.

Note this discretization procedure presumes a zero-order-hold (ZOH) discretization of the per-phase continuous-time dynamics in (5.19) [29]. For time-varying inputs $v_{\mathrm{i}}(t)$ and $i_{\mathrm{o}}(t)$, the lifted model is valid below frequencies where the error contributed by the ZOH operation is acceptably small [134].

Step 6: Lift the Phase-to-Phase to a Cycle-to-Cycle Solution

Assuming a constant input $\vec{u} = [v_{\mathrm{i}},\ i_{\mathrm{o}}]^\top$ throughout each full switching cycle k, then the $n = 1, \ldots, P$ per-phase state transition matrices $\vec{\phi}[n]$ and $\vec{\psi}[n]$ are recursively accumulated (as portrayed in Fig. 5.3) to lift the discrete-time LTI variable-rate system to a discrete-time LTI fixed-rate system with period $T_{\mathrm{s}} = \sum \Delta t_n$.

The result is the desired expression in (5.2) where the discrete-time transition matrices $\vec{A}_{\mathrm{d}}$ and $\vec{B}_{\mathrm{d}}$ are

$$\vec{A}_{\mathrm{d}} = \vec{\phi}[P] \cdot \ldots \cdot \vec{\phi}[2] \cdot \vec{\phi}[1] \tag{5.21}$$

$$\vec{B}_{\mathrm{d}} = \vec{\phi}[P] \cdot \vec{\phi}[P-1] \cdot \ldots \cdot \vec{\phi}[2] \cdot \vec{\psi}[1] + \vec{\phi}[P] \cdot \vec{\phi}[P-1] \cdot \ldots \cdot \vec{\phi}[3] \cdot \vec{\psi}[2] + \ldots + \vec{\psi}[P] \tag{5.22}$$

This final state-space form tracks the evolution of the state variables sampled at the beginning of each switching period k.

The aforementioned procedure for constructing a discrete-time LTI model applies to any alternative choice of sampling instant within the switching period, and the analysis in Section 5.7 derives some interesting consequent properties: namely the eigenvalues of A_{d} in (5.21) remain invariant to choice of arbitrary per-cycle sampling instant.

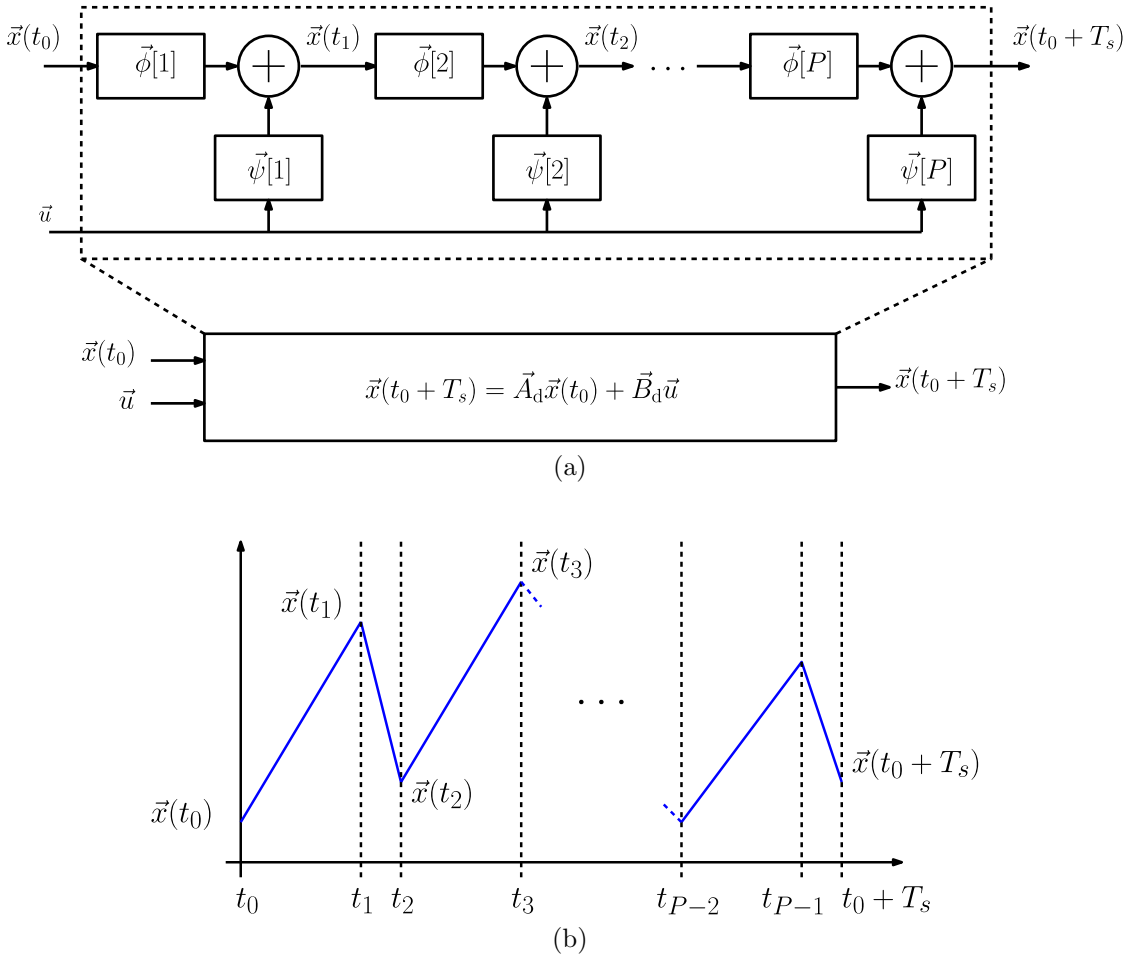


Figure 5.3: Block diagram showing the circuit state $x_i(t)$ accumulated across each switching phase into a full switching period.

5.3 Eigenanalysis

Conventional eigenvalue analysis (or eigenanalysis) and transfer function analysis apply to the derived LTI system of (5.2). This analysis enables quantification of key dynamic performance metrics including settling time, dominant resonance frequency, sensitivity to parameter variation, and disturbance rejection.

Continuous-Time Equivalent System

Except for the ZOH approximation of the input vector $\vec{u}$, the per-cycle discrete-time state-space system in (5.2) is an exact expression for a periodic sampling of the state dynamics. This system can be approximated by a continuous-time equivalent; this aids eigenvalue

Table 5.1: Nominal Circuit Parameters

Parameters:	N	5
	D	0.25
	f_{sw}	75 kHz
	C_{1-4}	8.8 µF
	L	10 µH
	R_{e}	0.40 Ω
	C_{o}	44 µF
	C_{oss}	2.34 nF
Inputs:	v_{i}	7.5 V to 30 V
	R_{o}	8.0 Ω

analysis to directly yield dynamic performance metrics such as the settling time and frequency of the dominant resonant mode. Using a bilinear transform (Tustin) approximation [123], the state-space system is reasonably described—for frequencies well below the sampling/switching period T_{s}—by the approximate continuous-time state dynamics $\vec{x}_{\mathrm{a}}$ as

$$\dot{\vec{x}}_{\mathrm{a}}(t) = \vec{A}_{\mathrm{c}}\,\vec{x}_{\mathrm{a}}(t) + \vec{B}_{\mathrm{c}}\,\vec{u} \tag{5.23}$$

where

$$\vec{A}_{\mathrm{c}} = \frac{2}{T_{\mathrm{s}}}\big(\vec{A}_{\mathrm{d}} + \vec{I}\big)^{-1}\big(\vec{A}_{\mathrm{d}} - \vec{I}\big) \tag{5.24}$$

$$\vec{B}_{\mathrm{c}} = \frac{2}{T_{\mathrm{s}}}\big(\vec{A}_{\mathrm{d}} + \vec{I}\big)^{-1}\vec{B}_{\mathrm{d}}. \tag{5.25}$$

A derivation for this continuous-time equivalent state-space system is provided in Section 5.8.

Dominant Time Constant

The dominant time constant τ_{d} is one useful metric for characterizing the FCML converter's multi-variate state dynamics [113, 200]. Using $T_{\mathrm{settle}} \approx 4\tau_{\mathrm{d}}$, the time constant reveals the transient settling time in the state dynamics to a step-response of the input [120, 58]. The value of τ_{d} is derived from the eigenvalues of the continuous-time equivalent $\vec{A}_{\mathrm{c}}$ in (5.24) as

$$\tau_{\mathrm{d}} := \frac{-1}{\max\big(\mathrm{Re}\big(\lambda_{\vec{A}_{\mathrm{c}}}\big)\big)} \tag{5.26}$$

where $\lambda_{\vec{A}_{\mathrm{c}}}$ is the set of eigenvalues (or spectrum) of $\vec{A}_{\mathrm{c}}$. The dominant time constant τ_{d} corresponds to the slowest system eigenvalue which bottlenecks the convergence of the transient response.

Dominant Resonant Frequency

The eigenvalues $\lambda_{\vec{A}_\mathrm{c}}$ of the continuous-time equivalent matrix $\vec{A}_\mathrm{c}$ in (5.24) also relay the dominant resonant modes of the system. The dominant resonant frequency f_d (in units of Hz) is the frequency of the slowest complex conjugate (i.e., non-real) eigenvalue pair where the 'slowness' of an eigenvalue corresponds to its closeness to the imaginary axis or $\mathrm{Re}\big(\lambda\big) = 0$. The mathematical representation is

$$f_\mathrm{d} := \frac{1}{2\pi} \mathrm{Im} \left(\underset{\left\{ \lambda_{\vec{A}_\mathrm{c}} \,\middle|\, \mathrm{Im}\left(\lambda_{\vec{A}_\mathrm{c}}\right) \neq 0 \right\}}{\mathrm{argmax}} \mathrm{Re}\big(\lambda_{\vec{A}_\mathrm{c}}\big) \right). \tag{5.27}$$

The dominant resonant frequency f_d corresponds to the dominant oscillatory component in the flying capacitors' underdamped step-response. It also occurs at the least damped complex-conjugate pole pair of the system.

Root Locus

The set of eigenvalues $\lambda_{\vec{A}_\mathrm{c}}$ define much of the dynamical behavior of the system. They are shown to allow computation of the dominant time constant τ_d in (5.26) and the dominant resonant frequency in (5.27). These eigenvalues—and consequently the full state-space dynamical system—are also markedly influenced by variation in system parameters: duty ratio D, inductance L, flying capacitance C_j, output capacitance C_o, equivalent series resistance R_e, transistor output capacitance C_oss, and switching frequency f_sw; the eigenvalues for parametric sweeps can be visualized in the real-imaginary axis of a root-locus diagram.

Fig. 5.4 shows the eigenvalues of $\vec{A}_\mathrm{c}$ for a continuous sweep of duty ratio D from 0 to 1; increments of $D = 0.1$ are denoted with markers. The leftmost eigenvalue conjugate pair in Fig. 5.4 is invariant to the duty ratio D and is strongly associated with the state variables of the output impedance network i_L and v_o. The other three eigenvalues are strongly associated with the three flying capacitor voltages and approach the origin along the real-axis as duty ratio changes outwards from $D = 0.5$ to $D = 0$ and $D = 1$.

Input-to-State Transfer Functions

Discrete-time transfer functions are derived by applying the z-transform to the system of discrete difference equations in (5.2). After some simplification, an input-to-state transfer function matrix is evaluated as

$$\vec{G}_\text{u-to-x}(z) = \left(z\vec{I} - \vec{A}_\mathrm{d} \right)^{-1} \vec{B}_\mathrm{d} \tag{5.28}$$

using the $\vec{A}_\mathrm{d}$ and $\vec{B}_\mathrm{d}$ matrices in (5.21) and (5.22), respectively. Each element of $\vec{G}_\text{u-to-x}(z)$ is a transfer function relating an input u to a state x:

$$G_\text{u-to-x}(z) = \frac{x(z)}{u(z)}. \tag{5.29}$$

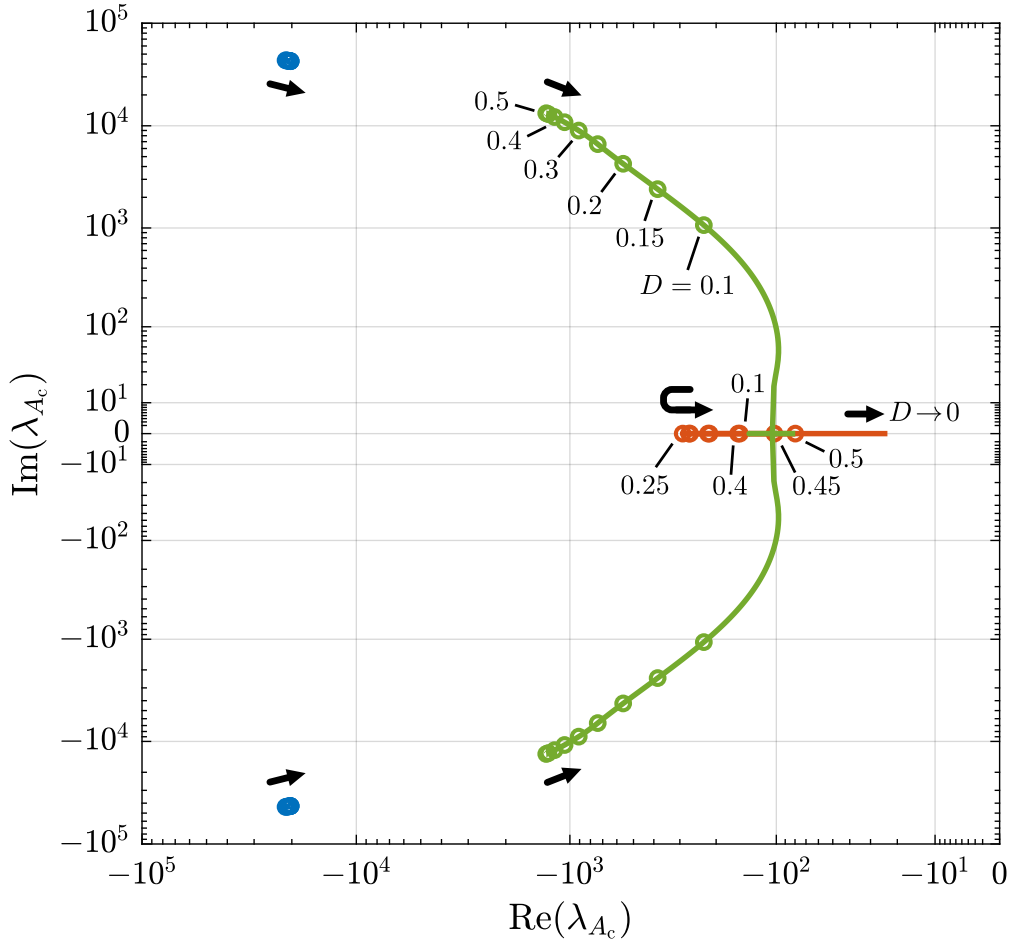


Figure 5.4: Root-locus diagram for eigenvalues of modeled $\vec{A}_c$ with swept duty ratio D for the $N = 5$ level FCML circuit with parameters in Table 5.1. The system and consequent eigenvalues are symmetric about $D = 0.5$ (i.e., $D = 0.2$ is equivalent to $D = 0.8$).

The frequency responses for these transfer functions are visualized via Bode plots which also indicate the locations of zeros and poles. Fig. 5.5 illustrates the magnitude $|G(\exp(j\omega))|$ and phase $\angle G(\exp(j\omega))$ of the input voltage v_i to flying capacitor voltage v_{C_j} transfer functions for each flying capacitor v_{C_1}, v_{C_2}, and v_{C_3}. The input voltage v_i to flying capacitor voltage v_{C_j} transfer functions have dc gains of -2.5, -6.0, and -12.0 dB corresponding to the expected balanced dc gains for the flying capacitor voltages of 0.75, 0.5, and 0.25 (i.e., $\frac{j}{(N-1)}$), respectively. This balanced distribution persists with increased frequency up to a certain bandwidth when the gain $|G_{v_\mathrm{i}\text{-to-}v_{\mathrm{C}_3}}(\exp(j\omega))|$ begins to attenuate.

The drain-source voltages $v_{\mathrm{ds},j}$ of the transistors underscore motivations for adequate flying capacitor voltage balancing in the FCML converter. The converter cannot function if any $v_{\mathrm{ds},j}$ surpasses the transistor ratings, and competitive FCML converter designs achieve

Table 5.2: Hardware Component Details

Component	Description	Part Name
Transistors	100 V, 1.8 mΩ GaN-FET	EPC2302
C_{1-10}	4 × 2.2 µF, X6S, 450 V	C5750X6S2W225K250KA
C_{o}	20 × 2.2 µF, X6S, 450 V	C5750X6S2W225K250KA
L	10 µH	IHLP5050CEER100M01
R_{GATE}	15 Ω, 0603	ERJ-2GEJ150X
Gate Driver	5 V, 7.6 A / 1.3 A	LM5114
Isolator	Power and Signal	ADUM5240

improved performance by choosing devices with the lowest possible ratings for the application [131, 88, 117, 13]. For the 5-level FCML converter, the drain-source voltages of the transistors (when off) are linear combinations of the instantaneous flying capacitor voltages and the input voltage:

$$v_{\mathrm{ds,1}} = v_{\mathrm{C_1}} \tag{5.30}$$

$$v_{\mathrm{ds,2}} = v_{\mathrm{C_2}} - v_{\mathrm{C_1}} \tag{5.31}$$

$$v_{\mathrm{ds,3}} = v_{\mathrm{C_3}} - v_{\mathrm{C_2}} \tag{5.32}$$

$$v_{\mathrm{ds,4}} = v_{\mathrm{i}} - v_{\mathrm{C_1}} \tag{5.33}$$

Linear transformation of the flying capacitor transfer functions in (5.28) yields the input voltage to drain-source voltage transfer functions. Fig. 5.6 exhibits the magnitude response for each $G_{v_{\mathrm{i}}\text{-to-}v_{\mathrm{ds},j}}(z)$. The conjugate pole pair at the dominant resonance frequency f_{d} is clearly visible in the transfer function characteristics. From the Bode diagram, there is a frequency above which the drain-source voltages of some transistors will surpass their ratings. This implies that in open-loop operation with symmetric PS-PWM, the flying capacitor voltages do not track input variations with sufficient accuracy when the input variation surpasses a particular frequency, a phenomenon motivating the design of an active voltage-balancing controller in [73]. Capacitor balancing under large-signal input voltage variation is of particular concern in ac grid-tied converters where the input varies at twice-line-frequency [161, 30, 16].

Steady-State Solution

The steady-state solution $\vec{x}_{\mathrm{ss}}$ for the sampled state vector $\vec{x}[k]$ for constant input $\vec{u}$ is analytically computed from manipulation of (5.2) as

$$\vec{x}_{\mathrm{ss}} = \lim_{k\to\infty} \vec{x}[k] = \left(\vec{I} - \vec{A}_{\mathrm{d}}\right)^{-1} \vec{B}_{\mathrm{d}} \cdot \vec{u}. \tag{5.34}$$

The steady-state $\vec{x}_{\text{ss}}$ does not describe the typical time-averaged state variables, but captures the steady-state of a fixed-rate per-cycle sample. Thus, this steady-state depends upon choice of sampling instant and incorporates switching ripple content. Work in [114, 187, 186, 46] demonstrates that the FCML converter operated in open-loop under symmetric PS-PWM is always asymptotically stable for strictly positive values of R_{e} and a unique steady-state solution exists for the state voltages and currents.

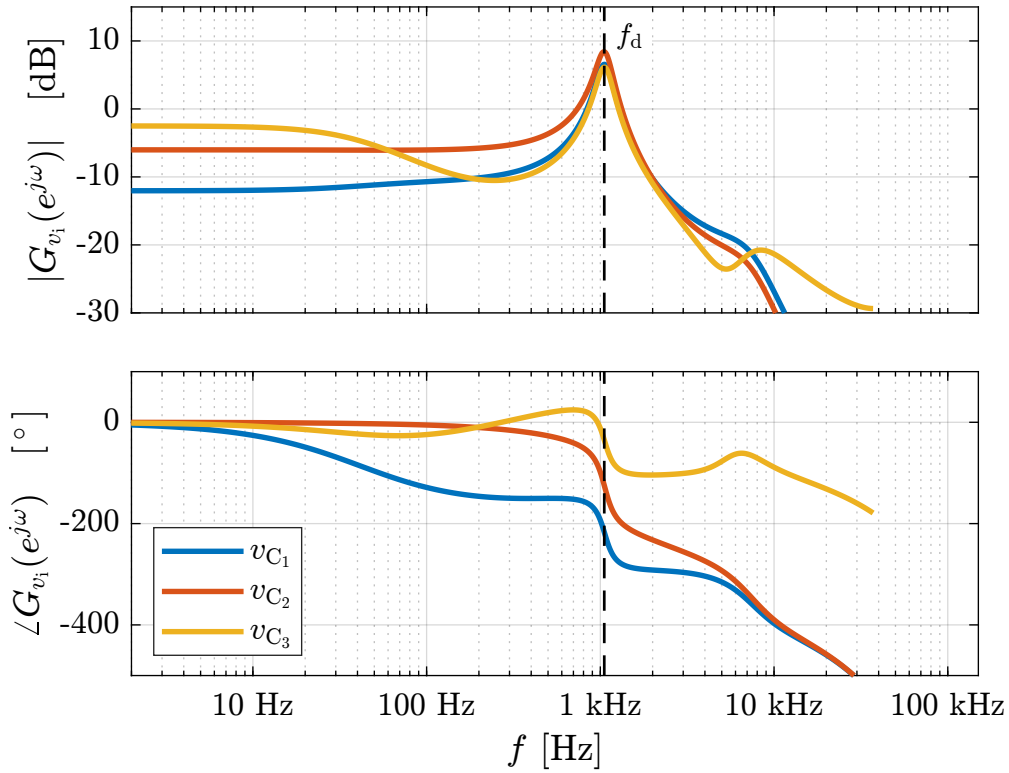


Figure 5.5: Modeled input voltage v_i to flying capacitor v_{C_j} small-signal transfer function magnitude $|G(e^{j\omega})|$ and phase $\angle G(e^{j\omega})$ for the $N = 5$ level FCML circuit with parameters of Table 5.1. The dominant resonant frequency f_d is highlighted.

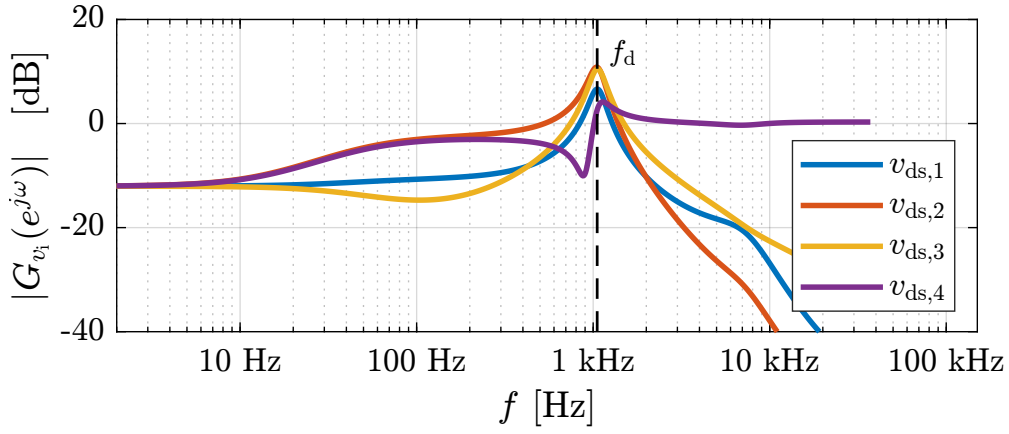


Figure 5.6: Modeled input voltage v_i to drain-source voltage $v_{\mathrm{ds},j}$ transfer function magnitude $|G(e^{j\omega})|$ for the $N = 5$ level FCML circuit with parameters of Table 5.1. The dominant resonant frequency f_d is highlighted.

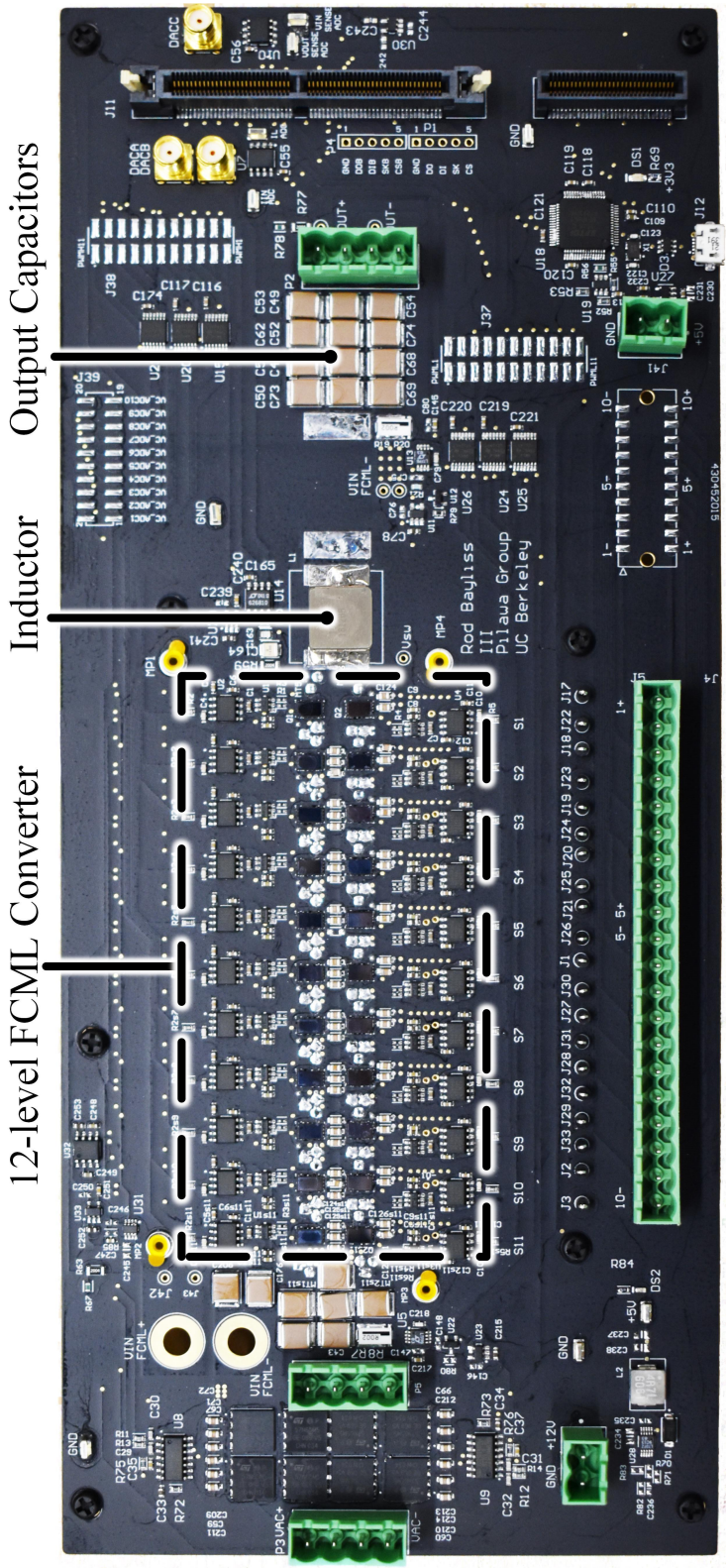


Figure 5.7: Hardware prototype of a high performance 12-level buck FCML converter.

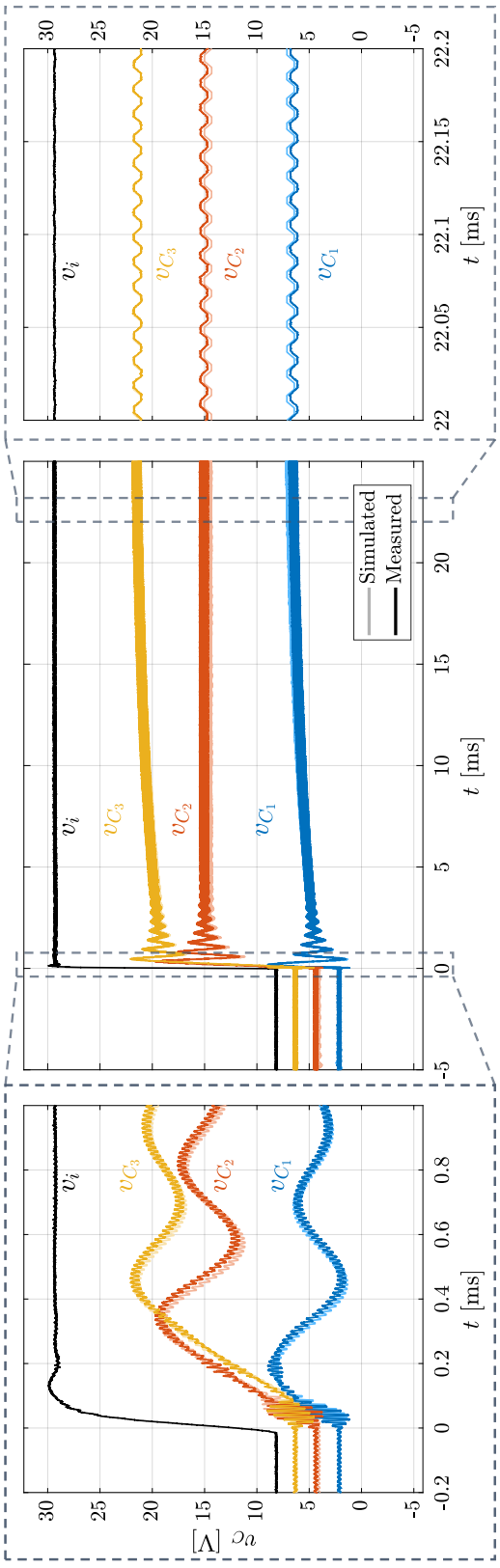


Figure 5.8: Measured versus modeled voltage dynamics for a $v_i = 7.5$ to 30 V step response at $\boldsymbol{D = 0.5}$ (leading symmetric PS-PWM). Highlights include (a) the initial higher-order transients; (b) the full simulation with emphasis on the dominant (slowest) system time constant; and (c) the steady-state switching ripple.

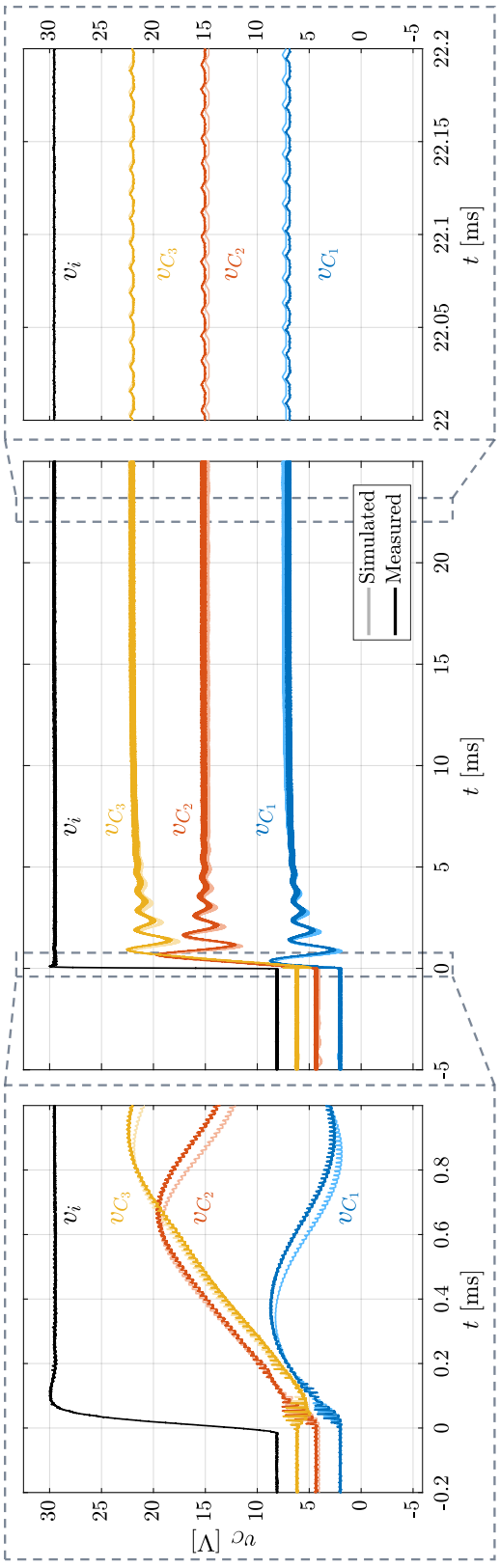


Figure 5.9: Measured versus modeled voltage dynamics for a $v_\mathrm{i} = 7.5$ to 30 V step response at $\boldsymbol{D = 0.25}$ (leading symmetric PS-PWM). Highlights include (a) the initial higher-order transients; (b) the full simulation with emphasis on the dominant (slowest) system time constant; and (c) the steady-state switching ripple.

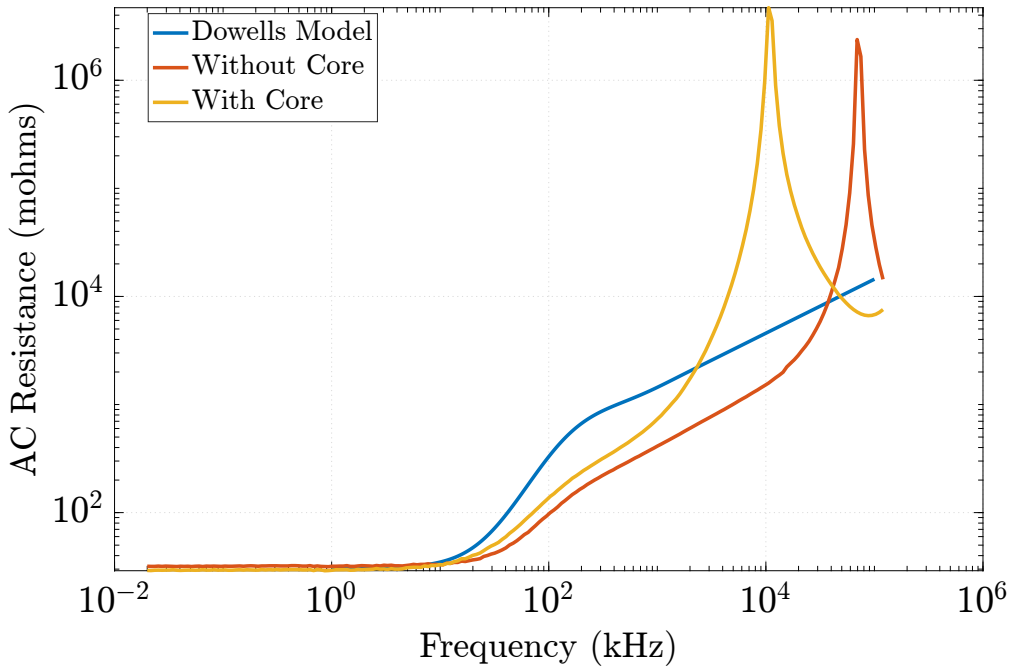


Figure 5.10: Measured small-signal resistance of the IHLP5050CEER100M01 inductor across frequency. Compared to modeled proximity resistance using Dowell's formula [50].

5.4 Experimental Validation

The full continuous per-phase model derived in Section 5.2 is compared against the high-performance FCML hardware in Fig. 5.7 with the components outlined in Table 5.2. This hardware prototype is reconfigurable to any level count $N \leq 12$; in this work it is configured as 5-level FCML converter.

Input Voltage Step-Response

The hardware is compared to the model for an input voltage step response as illustrated in Fig. 5.8 and Fig. 5.9 at $D = 0.5$ and $D = 0.25$, respectively, and the simulation parameters in Table 5.1. Beyond the conventional time-average dynamics, the model also captures the switching behavior of the flying capacitor voltages and agrees remarkably well with measurements. Such excellent agreement between a model and hardware has never been achieved for the FCML converter and is a notable contribution of this work. However, there are also a number of additional complexities to the piecewise-linear circuit simulation which are considered to capture the behavior of a practical system.

Diode Clamping

In a practical FCML converter the switches are implemented with FETs. The reverse conduction diodes on every FET (denoted in Fig. 5.1a) effectively clamp and saturate neighboring flying capacitors. This phenomenon is evident in Fig. 5.8a and Fig. 5.9a where $v_{C_2}(t)$ and $v_{C_3}(t)$ clamp together around $t = 0.20\,\text{ms}$. In this case, the clamping ensures $v_{C_3}(t) - v_{C_2}(t) \geq -V_{\text{diode}}$, where the forward voltage drop of the diodes is $V_{\text{diode}} \approx 2\,\text{V}$ for GaN HEMTs. This saturation effect forcefully redistributes charge amongst the flying capacitors and reduces overshoot and ringing in the transient response.

C_{oss} Charge Redistribution

As discussed in Section 5.2, with each switching commutation, charging/discharging of the parasitic transistor output capacitance C_{oss} redistributes small amounts of charge within flying capacitors and is crucial to accurately model FCML converter dynamics. The transistor output capacitance C_{oss} varies with applied voltage, so the charge-equivalent capacitance is derived and used in the model [47]. Without consideration of C_{oss}, the flying capacitors would not balance at $D = 0.5$ for an $N = 5$ level converter nor at other particular co-prime conversion ratios [187, 17].

Equivalent Series Resistance

The equivalent series resistance R_{e} for the FCML circuit models in Fig. 5.1 is a lumped combination of practical parasitic resistances: 1) on-state resistance $R_{\text{ds,on}}$ of the transistors, 2) capacitor equivalent series resistance ESR, and 3) the small-signal resistance of the inductor including skin and proximity effect of the winding. In all switching phases, the same quantity of $N-1$ switches conduct, thus all $R_{\text{ds,on}}$ can be lumped into the output impedance network. The ESR of ceramic capacitors at high frequencies is small [42] and is thus neglected. Besides the series dc resistance DCR, the inductor has a frequency-dependent resistance due to the proximity effect [50]. The small-signal resistance as a function of frequency is both calculated and corroboratively measured for the IHLP5050CEER100M01 inductor with an impedance analyzer as shown in Fig. 5.10. The measured small-signal resistance at the effective switching frequency $f_{\text{e}} = (N-1)\, f_{\text{sw}} = 300\,\text{kHz}$ is a factor of $F_{\text{prox}} = 11$ times the inductor DCR. The sum of all the resistive parasitics yields an equivalent series resistance of

$$\begin{aligned} R_{\text{e}} &\approx (N-1) \cdot R_{\text{ds,on}} + F_{\text{prox}} \cdot \text{DCR} \\ &\approx 11 \cdot 1.8\,\text{m}\Omega + 11 \cdot 34\,\text{m}\Omega \\ &\approx 0.4\,\Omega \end{aligned} \tag{5.35}$$

for the FCML converter.

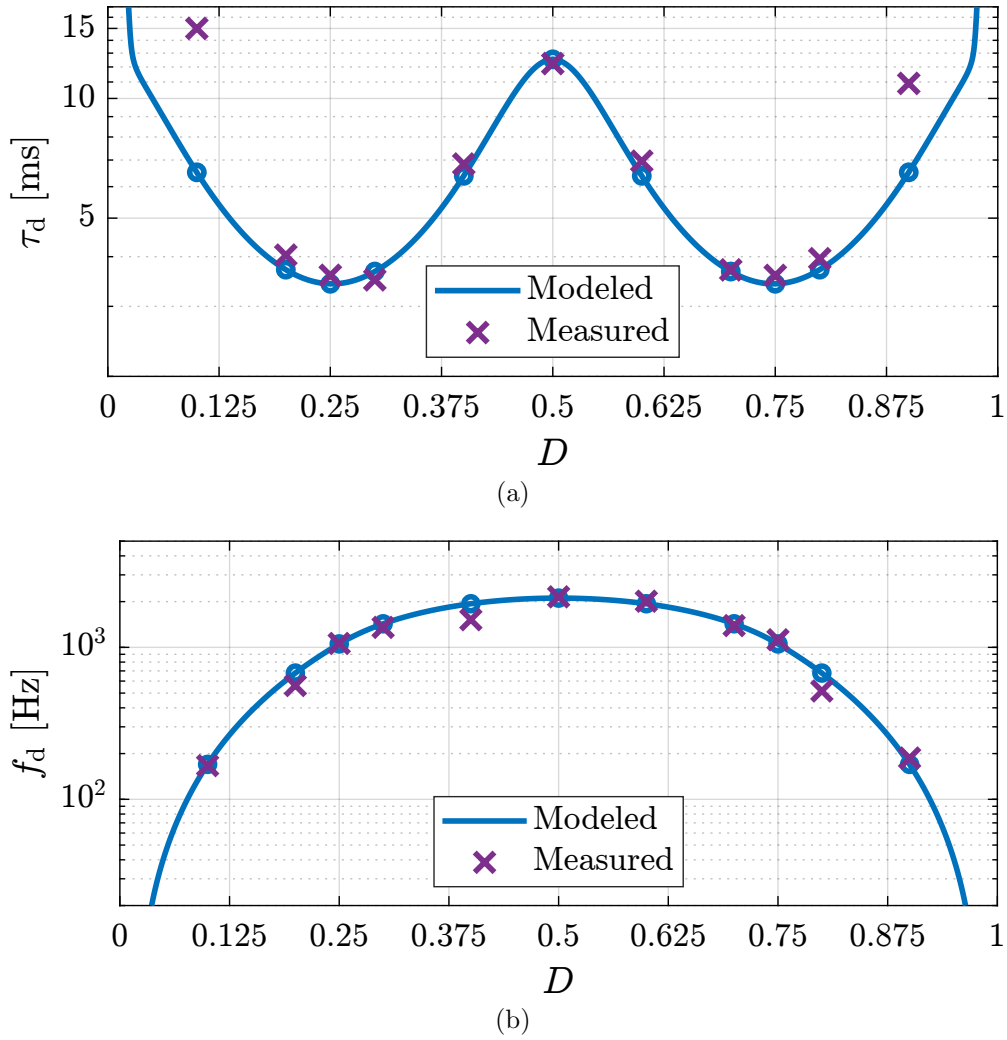


Figure 5.11: Measured versus modeled (a) first-order dominant time constant τ_d and (b) dominant resonant frequency f_d across duty ratio D for the $N = 5$ level FCML converter described in Table 5.1.

Resistive Load

To consider a resistive load R_o instead of an ideal current sink i_o, the model is adjusted by substituting $i_o = v_o/R_o$. This modification is justified because the dynamics of v_o vary slowly with respect to the notable state dynamics. For sufficiently large output capacitance $C_o \gg C_j$, the difference between a resistive load and an ideal current sink become negligible, especially when estimating the dominant time constant τ_d or dominant resonance frequency f_d. In cases where these conditions cannot be satisfied, Section 5.6 describes a more complete approach which can capably model the load as a resistance.

Validation of Dominant Eigenvalue Behavior

The hardware is excited by an input voltage step of $v_\mathrm{i} = 7.5\,\mathrm{V}$ to $30\,\mathrm{V}$. Post-processing the measured step-responses of the flying capacitor voltages yields the dominant time constant τ_d and the dominant resonant frequency f_d. The process is repeated for all duty ratios between $D = 0.1$ and 0.9 in increments of 0.1. Measured values of τ_d and f_d are compared to model-derived calculations in (5.26) and (5.27), respectively.

Dominant Time Constant

Fig. 5.11a shows a comparison of analytical dominant time constant τ_d from the model and a measured τ_d approximated from a first-order exponential fit. There is good consequent agreement showing the significant variation in the speed of the slowest dynamics at various duty ratio D.

Dominant Resonance Frequency

Similarly, Fig. 5.11b shows a comparison of analytical dominant resonant frequency f_d from the model and a measured f_d based on an FFT analysis. For this measurement, there is also consequent agreement with the model for swept duty ratio D.

5.5 Impact of Switch Output Capacitance on Flying Capacitor Balancing

The non-zero capacitance across the drain-source terminals of the power transistors introduces a path by which charge is redistributed between flying capacitors during a switching event [17]. This charge transfer occurs at the timescale of a switching transition, rather than a full switching phase or period. Thus it is modeled as an instantaneous impulse of charge transfer and can be represented by a matrix system describing the capacitor voltages before (i.e., $t = 0^-$) and after (i.e., $t = 0^+$) the switching transition.

$$\vec{v}_C(0^+) = \vec{v}_C(0^-) + \vec{X}[n]\,\vec{v}_C(0^-) + \vec{y}\,[n]\,v_i \tag{5.37}$$

Work in [17] derives the charge transfer equations in detail. These equations are compactly represented in matrix $\vec{X}[n] \in \mathbb{R}^{\mathrm{M}\times\mathrm{M}}$ in (5.36) and vector $\vec{y}[n] \in \mathbb{R}^{\mathrm{M}\times 1}$, given as

$$\vec{y}[n] = \frac{\big|s_{\text{N-1}}[n] - s_{\text{N-1}}[n-1]\big| \cdot C_\mathrm{oss}}{C_\mathrm{M} + C_\mathrm{oss}} \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 1 \end{bmatrix} \tag{5.38}$$

$$\vec{X}[n] = \frac{\left|s_1[n] - s_1[n-1]\right| \cdot C_{\text{oss}}}{C_1 + C_{\text{oss}}} \begin{bmatrix} -1 & 0 & 0 & \cdots \\ 0 & 0 & 0 & \cdots \\ 0 & 0 & 0 & \cdots \\ \vdots & \vdots & \vdots & \ddots \end{bmatrix} + \frac{\left|s_2[n] - s_2[n-1]\right| \cdot C_{\text{oss}}}{C_1C_2 + (C_1 + C_2)\, C_{\text{oss}}} \begin{bmatrix} -C_2 & C_2 & 0 & 0 & \cdots \\ C_1 & -C_1 & 0 & 0 & \cdots \\ 0 & 0 & 0 & 0 & \cdots \\ 0 & 0 & 0 & 0 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \ddots \end{bmatrix} + \frac{\left|s_3[n] - s_3[n-1]\right| \cdot C_{\text{oss}}}{C_2C_3 + (C_2 + C_3)\, C_{\text{oss}}} \begin{bmatrix} 0 & 0 & 0 & 0 & \cdots \\ 0 & -C_3 & C_3 & 0 & \cdots \\ 0 & C_2 & -C_2 & 0 & \cdots \\ 0 & 0 & 0 & 0 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \ddots \end{bmatrix} + \cdots + \frac{\left|s_{\text{N-1}}[n] - s_{\text{N-1}}[n-1]\right| \cdot C_{\text{oss}}}{C_{\text{M}} + C_{\text{oss}}} \begin{bmatrix} \ddots & \vdots & \vdots & \vdots \\ \cdots & 0 & 0 & 0 \\ \cdots & 0 & 0 & 0 \\ \cdots & 0 & 0 & -1 \end{bmatrix} \tag{5.36}$$

where all C_{oss} are assumed equivalent and linear and $s_j[n]$ represent elements of the switching matrix $\vec{S}$ as defined in (5.5).

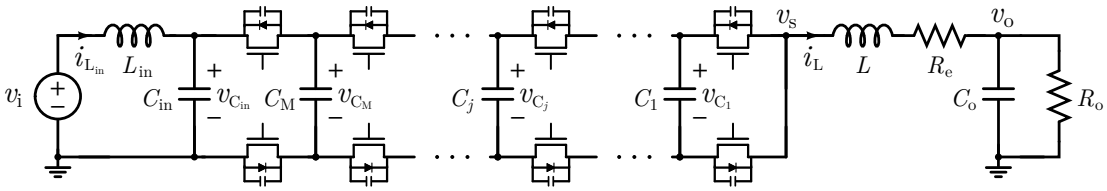


Fig. 5.12. FCML circuit schematic with input filter and resistive load.

$$\vec{x} := \begin{bmatrix} v_{\mathrm{C_1}} \\ \vdots \\ v_{\mathrm{C_M}} \\ i_\mathrm{L} \\ v_\mathrm{o} \\ i_{\mathrm{L_{in}}} \\ v_{\mathrm{C_{in}}} \end{bmatrix} \tag{5.39}$$

$$\vec{A}(t) := \begin{bmatrix} 0 & \cdots & 0 & \vdots & 0 & 0 & 0 \\ \vdots & \ddots & \vdots & \frac{s_{j+1}(t)-s_j(t)}{C_j} & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \vdots & 0 & 0 & 0 \\ \cdots & \frac{s_j(t)-s_{j+1}(t)}{C_j} & \cdots & -\frac{R_\mathrm{e}}{L} & -\frac{1}{L} & 0 & \frac{s_{\mathrm{N\text{-}1}}(t)}{L} \\ 0 & \cdots & 0 & \frac{1}{C_\mathrm{o}} & -\frac{1}{R_\mathrm{o}C_\mathrm{o}} & 0 & 0 \\ 0 & \cdots & 0 & 0 & 0 & 0 & -\frac{1}{L_\mathrm{in}} \\ 0 & \cdots & 0 & -\frac{s_{\mathrm{N\text{-}1}}(t)}{C_\mathrm{in}} & 0 & \frac{1}{C_\mathrm{in}} & 0 \end{bmatrix} \tag{5.40}$$

$$\vec{B}(t) := \begin{bmatrix} 0 \\ \vdots \\ 0 \\ 0 \\ 0 \\ \frac{1}{L_\mathrm{in}} \\ 0 \end{bmatrix} \tag{5.41}$$

5.6 Including Input Capacitance and Load Resistance in the Model

The model presented in this work is derived from second-order ordinary differential equations, with the general solution described in Section 5.2. To model additional phenomena not captured by the equivalent circuits of Fig. 5.1, additional circuit elements must be incorporated—e.g., converter input capacitance, load resistance. These elements increase the order of the equivalent circuits corresponding to each switching phase.

To model the effect of the converter input capacitance on the steady-state balancing (shown to be a significant influence in [201, 197]), the state-space must be extended to include an input filter as shown in Fig. 12. The output current sink i_o can also be replaced with a load resistor R_o; the system correspondingly only has one (rather than two) input $\vec{u} = v_\mathrm{i}$. As mentioned in Section 5.2, matrices $\vec{A}(t)$ and $\vec{B}(t)$ for the system in (5.1) are piecewise-constant, so the lifted dynamics can be computed as

$$\begin{aligned} \vec{x}[n+1] &= e^{\vec{A}[n]\,\Delta t[n]} \cdot \vec{x}[n] + \left(\int_0^{\Delta t[n]} e^{\vec{A}[n](\Delta t[n]-t)}\,\mathrm{d}t \right) \vec{B}[n] \cdot \vec{u}[n] \\ &= \vec{\phi}[n] \cdot \vec{x}[n] + \vec{\psi}[n] \cdot \vec{u}[n] \end{aligned} \tag{5.42}$$

where for switching phase n, $\vec{A}[n]$ and $\vec{B}[n]$ are constant-valued and $\Delta t[n]$ denotes the phase

duration.

Numeric computation of these matrix exponentials and integrals is significantly slower than evaluating the analytical solution derived for the reduced second-order circuit in (C1) and (C2).

5.7 Alternative Per Cycle Sampling Instants

The modeling method presented in Section 5.2 obtains a sampled-data model of the continuous-time system by assuming a specific sequence of switching phases over one period. In this section, it is shown that the choice of the sampling instant (i.e., the choice of which switching phase occurs first and where in the switching phase the system is sampled) does not affect eigenvalues of the discrete LTI state-transition matrix $\vec{A}_{\mathrm{d}}$.

The lifted per-cycle model is defined over the corresponding time interval $[t_0, t_0 + T_{\mathrm{s}})$ where the initial sampling instant is denoted t_0 and the switching period is T_{s}. The matrix $\vec{A}_{\mathrm{d}}$ of the lifted model, given by (5.21), can be alternatively represented as a periodic sampling of the state-transition matrix of the time-varying system in (5.1) as

$$\vec{A}_{\mathrm{d}} \equiv \vec{\Phi}(t_0 + T_{\mathrm{s}}, t_0) \tag{5.43}$$

since $\vec{\Phi}(t_0 + T_{\mathrm{s}}, t_0)$ satisfies the periodicity property $\vec{\Phi}(t_0 + T_{\mathrm{s}} + nT_{\mathrm{s}}, t_0 + nT_{\mathrm{s}}) = \vec{\Phi}(t_0 + T_{\mathrm{s}}, t_0), \forall n \in \mathbb{Z}$ [23].

Consider a shift to a new sampling instant t_{x} that satisfies $t_0 < t_{\mathrm{x}} < t_0 + T_{\mathrm{s}}$. The corresponding state vector at this new instant $\vec{x}(t_{\mathrm{x}})$ can be reached from the initial state vector $\vec{x}(t_0)$ by using the state-transition matrix

$$\vec{x}(t_{\mathrm{x}}) = \vec{\Phi}(t_{\mathrm{x}}, t_0)\, \vec{x}(t_0) \tag{5.44}$$

alternatively expressed as

$$\vec{x}(t_0) = \vec{\Phi}(t_{\mathrm{x}}, t_0)^{-1}\, \vec{x}(t_{\mathrm{x}}). \tag{5.45}$$

Additionally, the periodicity of the system also implies

$$\vec{x}(t_0 + T_{\mathrm{s}}) = \vec{\Phi}(t_{\mathrm{x}}, t_0)^{-1}\, \vec{x}(t_{\mathrm{x}} + T_{\mathrm{s}}). \tag{5.46}$$

The discretized per-cycle state-space model in (5.2) can be more completely expressed as

$$\begin{array}{rccc} \vec{x}[k+1] = & \vec{A}_{\mathrm{d}}\, \vec{x}[k] & + & \vec{B}_{\mathrm{d}}\, \vec{u}[k] \\ \vec{x}(t_0 + T_{\mathrm{s}}) = & \vec{\Phi}(t_0 + T_{\mathrm{s}}, t_0)\, \vec{x}(t_0) & + & \vec{\Psi}(t_0 + T_{\mathrm{s}}, t_0)\, \vec{u}(t_0) \end{array} \tag{5.47}$$

and transformed by substituting the similarity transformation from (5.45) and the periodicity property from (5.46) into (5.47)

$$\vec{\Phi}(t_{\mathrm{x}}, t_0)^{-1}\, \vec{x}(t_{\mathrm{x}} + T_{\mathrm{s}}) = \vec{\Phi}(t_0 + T_{\mathrm{s}}, t_0)\, \vec{\Phi}(t_{\mathrm{x}}, t_0)^{-1}\, \vec{x}(t_{\mathrm{x}}) + \vec{\Psi}(t_0 + T_{\mathrm{s}}, t_0)\, \vec{u}(t_0). \tag{5.48}$$

Pre-multiplying both sides by $\vec{\Phi}(t_\mathrm{x}, t_0)$ yields a new discrete LTI system of the form

$$\vec{x}(t_\mathrm{x} + T_\mathrm{s}) = \vec{A}_\mathrm{d,x}\, \vec{x}(t_\mathrm{x}) + \vec{B}_\mathrm{d,x}\, \vec{u}(t_0) \tag{5.49}$$

where

$$\begin{aligned} \vec{A}_\mathrm{d,x} &= \vec{\Phi}(t_\mathrm{x}, t_0)\, \vec{\Phi}(t_0 + T_\mathrm{s}, t_0)\, \vec{\Phi}(t_\mathrm{x}, t_0)^{-1} \\ &= \vec{\Phi}(t_\mathrm{x}, t_0)\, \vec{A}_\mathrm{d}\, \vec{\Phi}(t_\mathrm{x}, t_0)^{-1} \end{aligned} \tag{5.50}$$

and

$$\begin{aligned} \vec{B}_\mathrm{d,x} &= \vec{\Phi}(t_\mathrm{x}, t_0)\, \vec{\Psi}(t_0 + T_\mathrm{s}, t_0) \\ &= \vec{\Phi}(t_\mathrm{x}, t_0)\, \vec{B}_\mathrm{d} \end{aligned} \tag{5.51}$$

From (5.49) and (5.50), it is clear that the two state transition matrices $\vec{A}_\mathrm{d}$ and $\vec{A}_\mathrm{d,x}$ corresponding to different choices of sampling instants are related by a similarity transformation, so their eigenvalues are identical. This finding is crucial, as it demonstrates that any eigenanalysis of the lifted model is valid for all choices of cycle-periodic sampling instant t_x.

5.8 Continuous Approximation of the Discrete State-Space System

Consider the discrete-time sample-update equation given by

$$\vec{x}(t_0 + T_\mathrm{s}) = \vec{A}_\mathrm{d}\, \vec{x}(t_0) + \vec{B}_\mathrm{d}\, \vec{u}(t_0) \tag{5.52}$$

A continuous-time approximation of the dynamics of $\vec{x}$ that fits the points $\vec{x}(t_0)$ and $\vec{x}(t_0+T_\mathrm{s})$ takes the general form

$$\dot{x}(t) = \vec{A}_\mathrm{c}\vec{x}(t) + \vec{B}_\mathrm{c}\vec{u}(t) \tag{5.53}$$

with the solution

$$\vec{x}(t_0 + T_\mathrm{s}) = e^{\vec{A}_\mathrm{c} T_\mathrm{s}}\, \vec{x}(t_0) + \int_{t_0}^{t_0+T_\mathrm{s}} e^{\vec{A}_\mathrm{c}(t_0+T_\mathrm{s}-\tau)}\, \vec{B}_\mathrm{c}\, \vec{u}(\tau)\, \mathrm{d}\tau \tag{5.54}$$

Assuming the inputs are constant over a sampling period (ZOH approximation) the following equalities hold

$$\begin{aligned} \vec{x}(t_0 + T_\mathrm{s}) &= e^{\vec{A}_\mathrm{c} T_\mathrm{s}} \vec{x}(t_0) + \int_{t_0}^{t_0+T_\mathrm{s}} e^{\vec{A}_\mathrm{c}(t_0+T_\mathrm{s}-\tau)}\, \mathrm{d}\tau \vec{B}_\mathrm{c} \vec{u}(t_0) \\ &\equiv \vec{A}_\mathrm{d}\vec{x}(t_0) \quad + \quad \vec{B}_\mathrm{d}\vec{u}(t_0) \end{aligned} \tag{5.55}$$

The matrix $\vec{A}_{\mathrm{c}}$ must be invertible for the system to have a unique equilibrium, a property which has been verified for practical FCML converters in [186, 113, 197, 46]. Thus, it can also be shown from (5.55) that

$$\begin{aligned}\int_{t_0}^{t_0+T_{\mathrm{s}}} e^{\vec{A}_{\mathrm{c}}(t_0+T_{\mathrm{s}}-\tau)}\,\mathrm{d}\tau\vec{B}_{\mathrm{c}} &= \left(e^{\vec{A}_{\mathrm{c}}T_{\mathrm{s}}}-\vec{I}\right)\vec{A}_{\mathrm{c}}^{-1}\vec{B}_{\mathrm{c}}\\ &= \left(\vec{A}_{\mathrm{d}}-\vec{I}\right)\vec{A}_{\mathrm{c}}^{-1}\vec{B}_{\mathrm{c}}\\ &\equiv \vec{B}_{\mathrm{d}}. \end{aligned} \tag{5.56}$$

From (5.55), it is clear that $\vec{A}_{\mathrm{c}}$ is related to $\vec{A}_{\mathrm{d}}$ as

$$\vec{A}_{\mathrm{d}} = e^{\vec{A}_{\mathrm{c}}T_{\mathrm{s}}} \tag{5.57}$$

Therefore, the continuous-time approximation $\vec{A}_{\mathrm{c}}$ can be obtained from $\vec{A}_{\mathrm{d}}$ by relating the following undriven systems (i.e., $\vec{u}=\vec{0}$)

$$\dot{\vec{x}} = \vec{A}_{\mathrm{c}}\vec{x} \tag{5.58}$$

$$\vec{x}[k+1] = \vec{A}_{\mathrm{d}}\vec{x}[k] \tag{5.59}$$

and equivalently by deriving the Laplace transform of (5.58) and the z-transform of (5.59),

$$s\vec{x} = \vec{A}_{\mathrm{c}}\vec{x} \tag{5.60}$$

$$z\vec{x} = \vec{A}_{\mathrm{d}}\vec{x}. \tag{5.61}$$

To approximate the relationship between the two systems, the bilinear transform (Tustin) approximation is applied to the variable z

$$z = e^{sT_{\mathrm{s}}} \approx \frac{1+\frac{sT_{\mathrm{s}}}{2}}{1-\frac{sT_{\mathrm{s}}}{2}} \tag{5.62}$$

yielding

$$\vec{A}_{\mathrm{c}} = \frac{2}{T_{\mathrm{s}}}\left(\vec{A}_{\mathrm{d}}+\vec{I}\right)^{-1}\left(\vec{A}_{\mathrm{d}}-\vec{I}\right). \tag{5.63}$$

Then using (5.63), the matrix $\vec{B}_{\mathrm{c}}$ is obtained from (5.56) as

$$\vec{B}_{\mathrm{c}} = \frac{2}{T_{\mathrm{s}}}\left(\vec{A}_{\mathrm{d}}+\vec{I}\right)^{-1}\vec{B}_{\mathrm{d}}. \tag{5.64}$$

This result elucidates the continuous-time equivalent system introduced in Section 5.3.

5.9 Conclusion

This work proposes a computationally efficient discrete-time state-space model for the buck-type FCML converter which capably functions irrespective of the modulation scheme, level count, or conversion ratio. The model is shown to have excellent agreement with practical measurements and is demonstrated to accurately predict the natural dynamical behavior of this topology. Furthermore, both the dominant time constant τ_{d} and dominant resonant mode frequency f_{d} of the measured system can be predicted from the model, providing estimates of the expected balancing speed and oscillation frequency of the flying capacitors to transient disturbances.

Part III

Multilevel Converters for Buck-Type Power Factor Correction

Chapter 6

PCB Layout Improvements for the Buck PFC FCML Converter

6.1 Introduction

Compared to traditional "two-level" converter topologies (e.g., buck, boost), hybrid switched capacitor topologies in general can achieve excellent simultaneous reduction in loss and volume by redistributing the energy processing requirements of bulky inductors to more energy dense capacitors and active switch components [87]. Hybrid switched capacitor converters also utilize lower voltage rated transistors, which can have improved performance in aggregate compared to two full system voltage rated transistors [13]. In particular, the flying capacitor multilevel (FCML) topology excels for regulated applications and remains competitive for wide input range conversion ratios as demonstrated by the high-performance prototypes in [88, 117, 93, 198]. However, with multilevel topologies comes a greater quantity of active switching components, so maximizing switching speed and minimizing switching loss becomes critical. This work investigates the application of a standard low-inductance hybrid switching cell layout [64, 142, 170] to the FCML buck converter shown in Fig. 6.1 while simultaneously improving efficiency with the use of paralleled low-side FETs as shown in Fig. 6.2a. The remainder of the chapter is organized as follows: Section 6.2 presents innovations in the switching cell layout highlighting the asymmetry in the complimentary switch pairs and the ultra-low commutation loop inductance; and Section 6.3 demonstrates experimental validation—both the commutation loop and the overall converter—with a high-performance multi-purpose hardware prototype.

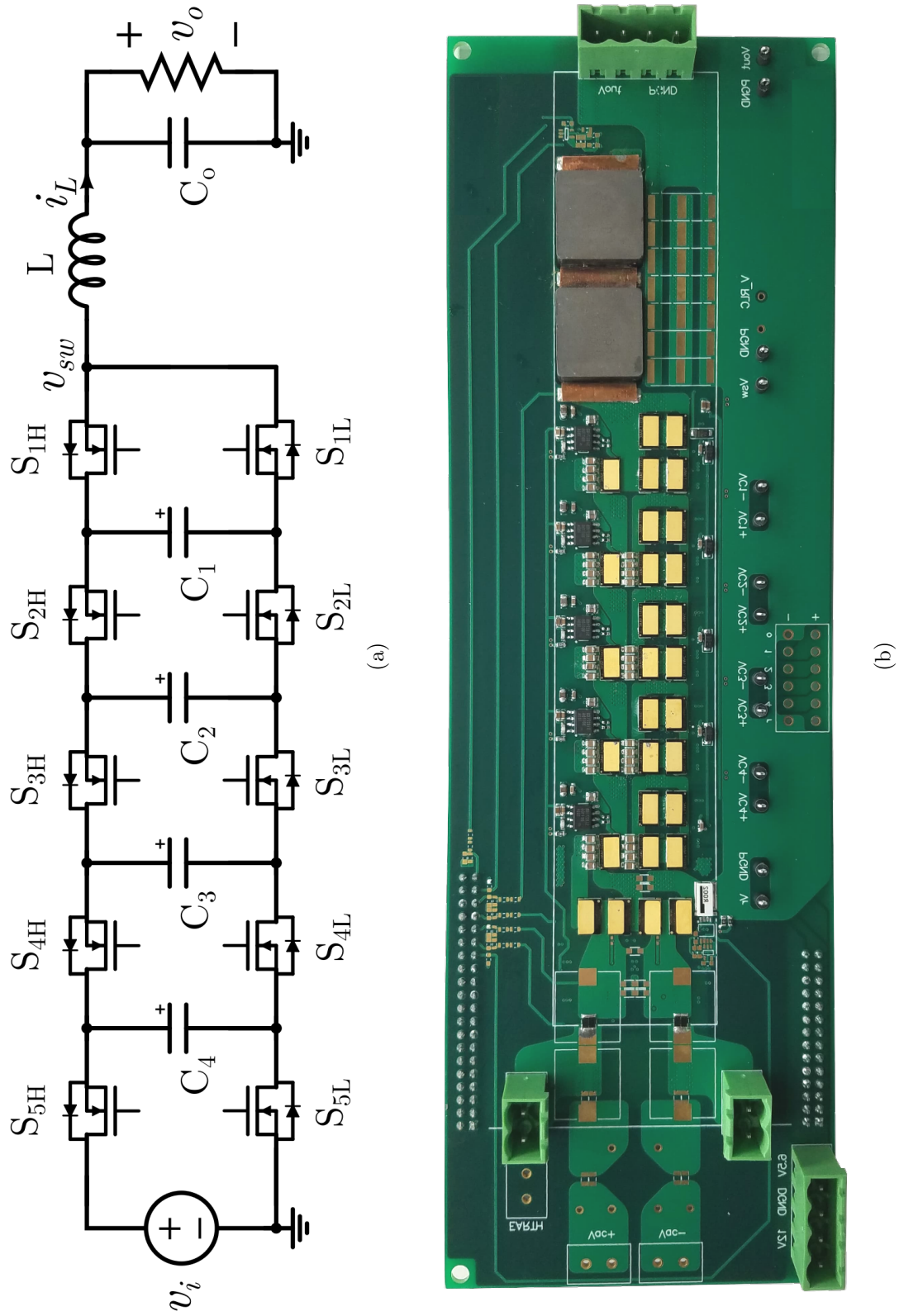


Figure 6.1: Full 6-level FCML buck converter. (a) Simplified schematic and (b) hardware prototype photograph (front-side).

6.2 Switching Cell Layout

The FCML switching cell is distinct from a typical half-bridge as the high-side (HS) source and low-side (LS) drain of complimentary FETs are not equipotential. There are instead two flying capacitors adjacent to the FETs as indicated in Fig. 6.2a which altogether define the commutation loop of a single switching cell. The cascaded modularity of the FCML implies any inefficacy in the cell compounds with the number of levels. Thus, to markedly improve overall system performance for a large voltage step-down application, the core cell layout as illustrated in Fig. 6.2b is designed to be asymmetrical with low commutation loop inductance to optimize conduction losses and improve switching speed, respectively.

The utilization of GaN—instead of Si—devices enables improved converter performance considering system trade-offs in switching frequency, losses, and volume. GaN HEMTs have an inverse transconductance versus temperature relation which benefits current sharing when paralleling discrete components [5]. In addition, the GS61008T (GaN Systems) top-side-cooled GaN HEMT contains two symmetric interchangeable gate pins on either side of the package which specifically aids layout parallelization and allows for equivalent parasitic gate-loop inductance between all FETs [177]. GaN FETs also have high dv/dt transitions thus layouts with low parasitic inductances, especially when paralleling FETs, better enable full utilization of the devices. With sub-optimal layout, high gate resistance becomes necessary to dampen overshoot in V_{ds} during turn-on to prevent fatal over-voltages; this in turn increases switch overlap losses.

Many layout aspects are critically dependent on application voltage creepage and clearance requirements. Other FCML switching cell designs in [117, 39] implement various *vertical* layouts necessary at 1000 V and/or for high altitude applications whereas the *hybrid* layout proposed in this work meets a 400 V compatibility requirement in less stringent environmental conditions.

Asymmetrical Switching Cell

An asymmetrical switching cell—broadly defined by unequal on-state resistances between the HS and LS switches—aids in minimizing the overall conduction losses. In the case of a buck converter, as the voltage conversion ratio increases and the duty ratio D decreases, the rms current in the LS switches becomes much larger than the rms current in the HS switches, i.e., $I_{\mathrm{LS}} = \sqrt{1-D} \cdot I_{\mathrm{L}}$ and $I_{\mathrm{HS}} = \sqrt{D} \cdot I_{\mathrm{L}}$. Consequently, ohmic conduction losses in the LS switches quickly dominate and thermally limit the converter as the load increases. So for each cell, LS switches should optimally have equal losses to the HS switches. To best achieve this, the LS on-state resistance $R_{\mathrm{ds,LS}}$ should be smaller than the HS $R_{\mathrm{ds,HS}}$ to offset the relative difference in rms current. For a specified input/output conversion ratio $M = 1/D$, the conduction losses in each cell can be equated as

$$P_{\mathrm{cond,HS}} = I_{\mathrm{HS}}^2 \; R_{\mathrm{ds,HS}} = I_{\mathrm{LS}}^2 \; R_{\mathrm{ds,LS}} = P_{\mathrm{cond,LS}} \tag{6.1}$$

to derive an ideal HS to LS on-state resistance ratio K as

$$K = \frac{R_{\text{ds,HS}}}{R_{\text{ds,LS}}} = \frac{1-D}{D}. \tag{6.2}$$

To achieve switching cell asymmetry, the desired K is achieved either using a single device for each side with different intrinsic $R_{\text{ds,on}}$ [143] or with discrete parallel devices. This design implements the latter method with one HS FET and K paralleled LS FETs utilizing a single discrete device type. EPC manufactures a series of monolithic integrated GaN half-bridge cells, and various options are LS/HS asymmetric ($K = 4$) meant for high conversion ratio applications [6, 143].

The primary drawback to parallelization is increased switching overlap losses associated with the greater number of switches. For K parallel switches, each switch sees the full rated voltage and only $1/K$ of the rated current. However, the source and sink currents of the gate driving circuit must charge and discharge a larger effective input capacitance $C_{\text{iss,K}} = K \cdot C_{\text{iss}}$ and output capacitance $C_{\text{oss,K}} = K \cdot C_{\text{oss}}$ resulting in slower overall switching transitions. Thus determination of total losses when paralleling FETs is a multi-faceted optimization dependent on the gate driving layout and circuitry. With proper cell design, an asymmetric cell can achieve only marginally worse switching losses compared to a non-paralleled design, especially when conduction losses dominate within the overall converter as in the aforementioned high power, wide-conversion-ratio application.

Despite a larger cell area due to parallelization, small cell volume is obtained by fully utilizing the available surface area on the back-side to minimize overall converter height. For this layout, there is ample room on the back-side of the printed circuit board (PCB) to incorporate a sufficient amount of flying capacitance necessary for FCML operation. Although this bulk flying capacitance is too electrically distant to achieve fast switching commutation (i.e., large commutation loop) by itself, small bypass capacitors can be used locally to alleviate potential impairments in switching performance.

Compared to a conventional two-level power converter, hybridized switch-capacitor topologies tend to be ultra-low profile with distributed lower-voltage switches and lower inductance requirements. To maintain consistency in the converter height throughout, the primary buck inductor tends to also be low-profile. For this design a standard 1.6 mm PCB thickness makes up almost a quarter of the overall converter height, and thus an inset inductor becomes a reasonable consideration to maximize the fill factor of the hardware. The inductor with lateral fins is inspired by an existing series of "winged" IHLW™ inductors manufactured by Vishay; however, no commercially available options were rated for large enough saturation currents to fulfill the design needs of this work and a custom assembly utilizing commercial products[1] was constructed.

[1] $L = 2 \times 3.3\,\mu\text{H}$, 28 A, Vishay IHLP6767GZER3R3M01

Table 6.1: Measurement and simulation results of commutation loop inductance L_c at $f = 100\,\text{MHz}$

FET(·)	A	AB	ABC	ABCD
Q3D sim.	0.40 nH	0.38 nH	0.38 nH	0.38 nH
Impedance meas.[1]	1.00 nH	0.93 nH	0.93 nH	0.94 nH
Transient meas.[2]	1.09 nH	0.94 nH	—	—

[1] Measurement error in L_c is approximately ±50 pH at 1 nH.
[2] Measurement error in L_c is approximately ±100 pH at 1 nH.

Commutation Loop Inductance

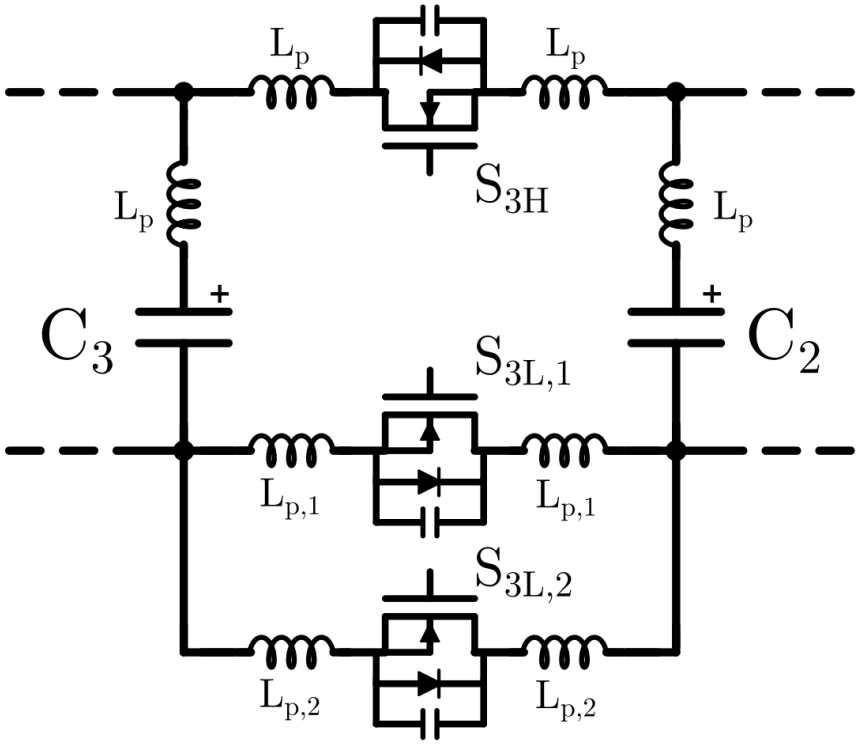
Reducing the commutation loop inductance diminishes voltage overshoot during switch transitions and can indirectly decrease switching losses, through purposeful reduction of deadtime and gate resistance; this is especially pertinent in a design with paralleled FETs. Overall, minimization of the various parasitic inductances in the switching cell layout were prioritized accordingly: (i) the common-source inductance in the paralleled LS FETs, (ii) the commutation loop inductance formed by the complimentary switch pair, and (iii) the gate loop inductance(s). These judgements are ultimately underscored by minimum voltage clearance requirements. A different prioritization of parasitics would result in a differently designed layout.

The *hybrid* switching cell as defined in [117, 64, 169, 168, 143] remains a competitive layout choice since all pertinent components are on the front-side of the PCB and the commutation loop path forms a low impedance path between the first (front-side) and second copper layers as denoted in Fig 6.2b. For low-profile GaN HEMT devices, the commutation loop trace width can be as wide as the component itself. In this 4-layer PCB design, the first copper layer is 70 µm (2 oz.), the inner prepreg layer is 110 µm, and the second copper layer is 35 µm (1 oz.) which forms a relatively small loop area. Maximization of trace width and minimization of loop area are first-order optimizations which reduce the overall commutation loop inductance L_c.

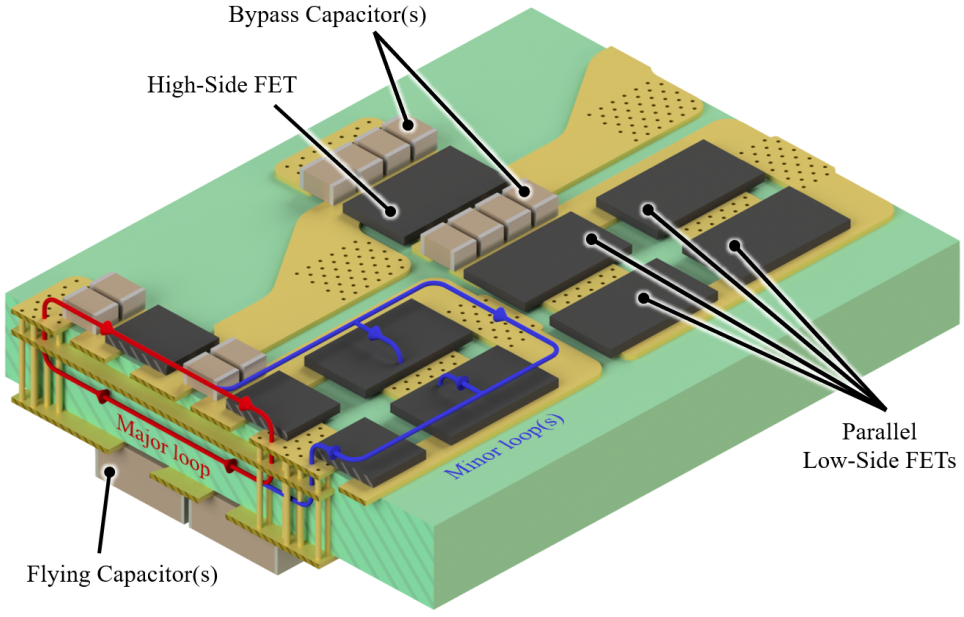
The proposed cell design uses only through vias which minimizes manufacturing complexity and cost; a more complex design with blind and buried vias could potentially utilize both the front and back-sides of the board to increase cell density without significant clearance concerns. An example of this extension to the hybrid cell layout design is presented in [64].

Two primary layout innovations—the asymmetrical switching cell and low commutation loop inductance—have been thus far discussed as mostly mutually exclusive design considerations. Typically in symmetric switching cell designs, the HS and LS FET(s) are evenly distributed to the greatest extent possible which equalizes the parasitic gate and commutation

loop inductances of paralleled FETs [5, 8, 101, 7]. For the choice of GS61008T GaN FETs in a 6-level FCML at peak input voltage $v_{\text{in}} = 340\,\text{V}$, the system design fully utilizes (with adequate margin) the device's voltage rating limit ($V_{\text{ds,nom}} = 68\,\text{V}$ versus $V_{\text{ds,max}} = 100\,\text{V}$), however it notably underutilizes the device's continuous current rating limit ($I_{\text{ds,nom}} = 17\,\text{A}$ versus $I_{\text{ds,max,cont}} = 65\,\text{A}$ at $T_{\text{c}} = 100\,^{\circ}\text{C}$). The underutilized current capacity presents an opportunity—because of the asymmetric quantity of HS versus LS FETs—to also make the commutation path relative to each paralleled FET asymmetric (i.e., $L_{\text{p,1}} \neq L_{\text{p,2}}$ in Fig. 6.2a). Assuming symmetrical common-source inductance, gate inductance, and gate resistance, the closest LS FET $S_{\text{L,A}}$ which forms a *major* commutation loop with the HS FET S_{H} (see Fig. 6.2b) turns on slightly before the other LS FETs $S_{\text{L,B-D}}$ which form *minor* commutation loop paths. Thus for a short period, most current $I_{\text{ds,nom}}$ flows through $S_{\text{L,A}}$ until $S_{\text{L,B-D}}$ turn on and redistribute it equally.



(a)



(b)

Figure 6.2: Asymmetrical switching cell defintion, implementation, and characterization. (a) Exemplar asymmetrical switching cell with inductive parasitics. (b) Rendered switching cell with delineations for major and minor commutation paths (exaggerated PCB layer thicknesses).

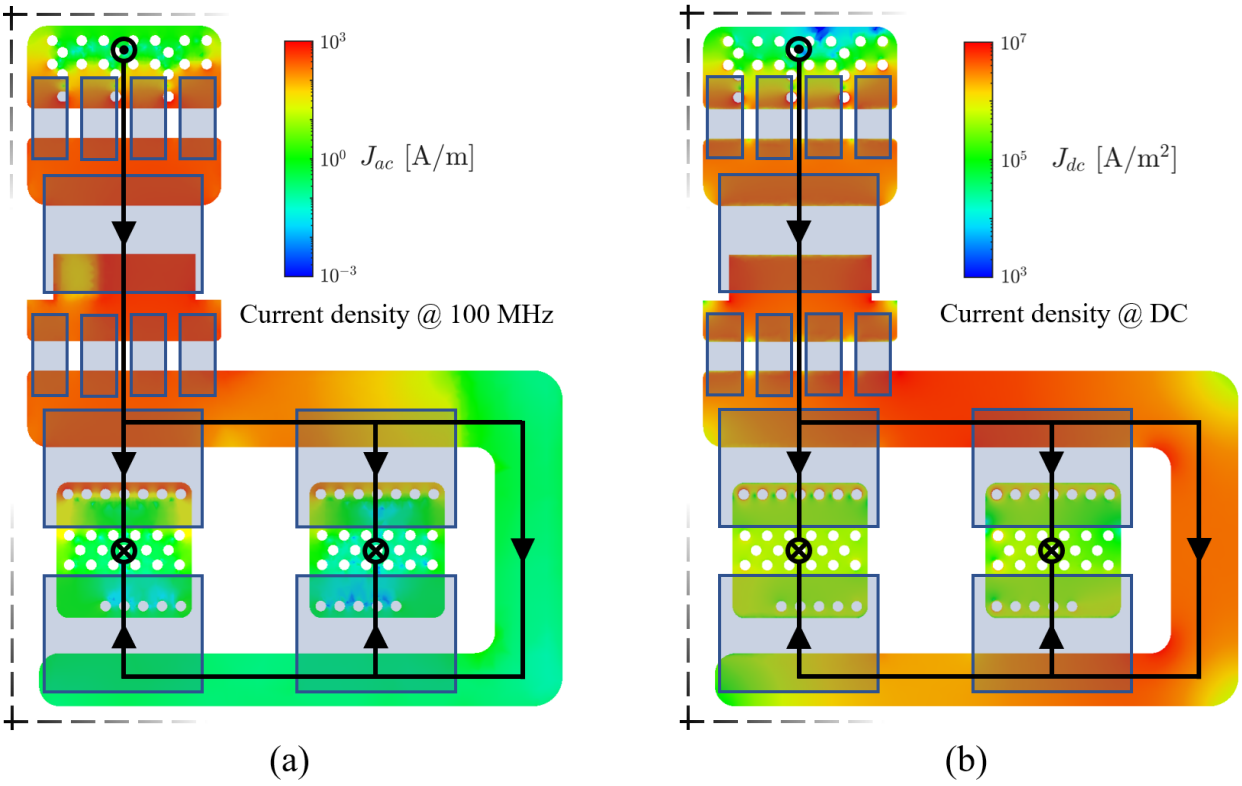


Figure 6.3: Switching cell simulation (Q3D ANSYS) of front-side layer with excitation current $I_e = 1\,A$. (a) Illustration of surface current density distribution at a commutation frequency of $f = 100\,MHz$ readily indicates the major and minor commutation paths. (b) Surface current density distribution at dc demonstrating proper current distribution between parallel FETs.

6.3 Experimental Validation

Utilizing preceding developments, a multi-purpose PCB hardware prototype capable of dc-dc and ac-dc operation as shown in Fig. 6.1b is designed to validate the switching cell efficacy. The converter is functionally a step-down intermediate bus converter supply ($v_{\text{out}} = 48\,\text{V}$) with wide input voltage range ($v_{\text{in}} = 48$ to $340\,\text{V}$) and an output current rating of $14\,\text{A}$ (or $650\,\text{W}$). The necessity of an asymmetrical switching cell structure is especially attractive for a high voltage step-down (or step-up) application, and a near-median input voltage of $240\,\text{V}$ corresponds to a 5-to-1 conversion ratio where the conduction loss in the single HS and four paralleled LS FETs are ideally equivalent according to (6.2). The gate drive design is a cascaded bootstrap structure as outlined in [195] using one Silicon Labs Si8271 isolated gate driver to drive each side of each switching cell.

Switching Cell Evaluation

The overall commutation loop inductance L_{c} serves as a reductive but fair metric for quantifying switching cell performance as it is geometrically rather than operationally dependent. However, target inductances below $1\,\text{nH}$ are especially difficult to measure with reasonable accuracy and so several simulation tools and experimental testbeds have been utilized for validation. Different circuit configurations are enumerated simply as a combination of low-side FETs A, B, C, and D as designated in Fig. 6.6. For instance, configuration "FET(AB)" denotes the device-under-test (DUT) which contains both low-side FET A and FET B, while "FET(B)" denotes the DUT containing only low-side FET B.

3D field simulation

Simulation using ANSYS Q3D, a 3D electromagnetic field solver, extracts values of L_{c} from the physical PCB geometry and these values are reported for different parallel quantities in Table 6.1. Figures 6.2 and 6.2 are illustrations of current density at $100\,\text{MHz}$ and dc frequencies, respectively, in the front-side copper plane. Current distribution at $f = 100\,\text{MHz}$ illustrates a major (dominant) commutation path and weaker minor commutation paths, while at dc all current is shared equally amongst the paralleled LS FETs as expected.

Transient-based measurement

The pulse-based measurement captures a transient step-response in the HS V_{ds} of the switching cell for a LS turn-on transition. The FCML switching cell can be considered a more complex variation of the typical half-bridge cell except with an additional bypass capacitor between the HS drain and LS source. Consequently, a double-pulse test circuit [5] typically used for the latter is incompatible with the former. A specialized test circuit introduced in [117] and reproduced in Fig. 6.4, generates a ground-referenced voltage transient across a FET for a near-zero current I_{ds}. This voltage transient is then captured with a high-

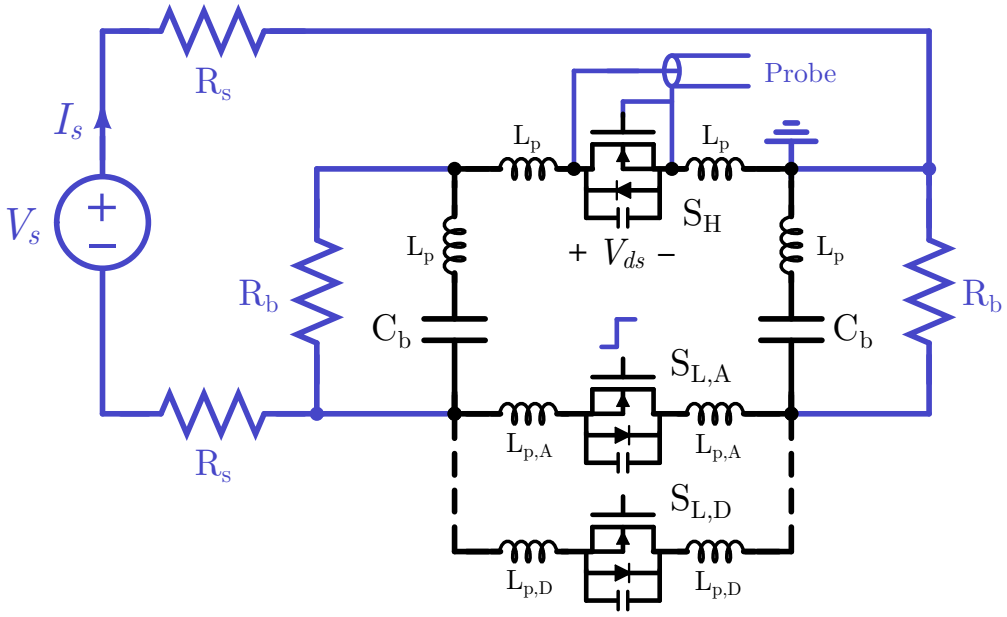


Figure 6.4: Transient-based measurement test circuit schematic. $R_\mathrm{s} = 100\ \Omega$, $R_\mathrm{b} = 100\ \mathrm{k}\Omega$.

bandwidth oscilloscope utilizing a low-inductance probe[2]. In principle, the dc voltage V_s is set to the desired steady-state value of V_ds; the source resistors R_s ensure the auxiliary circuit path is higher impedance than the sensitive commutation loop; and the bypass resistors R_b dissipate energy in the bypass capacitors after the initial transient of the step response. Although not truly representative of the switching dynamics of the full system since $I_\mathrm{ds} \approx 0$ and gate resistance $R_\mathrm{g} = 4\ \Omega$, the transient measurement does provide some intuition regarding the switching rise time and relative voltage overshoot at nominal operating conditions.

Figure 6.5 depicts measured HS drain-source voltage $V_\mathrm{ds,HS}$ after LS FET turn-on for different configurations of paralleled LS FETs. The frequency of the observed resonance in $V_\mathrm{ds,HS}$ yields a relationship for extracting L_c indirectly by utilizing the HS FET parasitic output capacitance $C_\mathrm{oss,HS}$ (derated for operating voltage) if approximated as a second-order LC circuit as

$$L_\mathrm{c} \approx \frac{1}{(2\pi f_\mathrm{r})^2\ C_\mathrm{oss}} \tag{6.3}$$

assuming minimal damping and a linear C_oss throughout the damped oscillation. If the waveform oscillations are heavily distorted, then an FFT can estimate the fundamental frequency component of resonance. Observed waveform distortion arises from changes in the transient impedance associated with dynamic $R_\mathrm{ds,on}$ [57] as well as possible non-linearities in the capacitor ESR during large voltage swings [40, 41]. Evaluated results of (6.3) yield $L_\mathrm{c} = 0.93\,\mathrm{nH}$ including all paralleled FETs as shown in Table 6.1. Measurements are highly

[2]Keysight MSOX4154A (1.5 GHz, 5 GSa/s) oscilloscope with N2894A (700 MHz) passive probe.

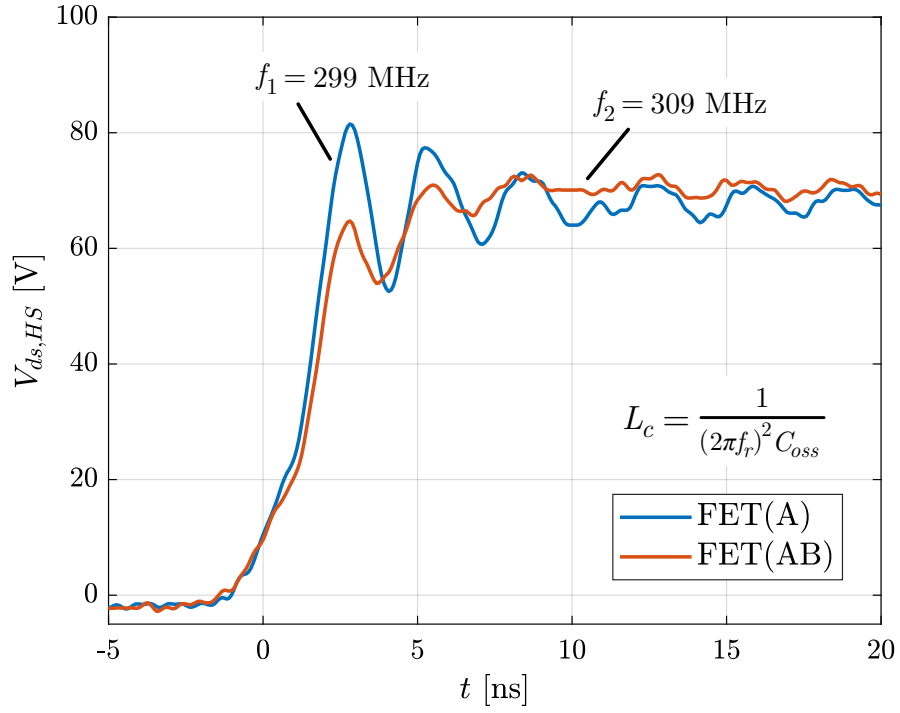


Figure 6.5: Measured high-side V_{ds} during LS turn-on for varied configurations of paralleled low-side FETs. Input voltage $V_s = 70\,\text{V}$, sink current $I_s = 2$ mA, and per-FET turn-on gate resistance $R_{\text{g,on}} = 4\Omega$.

repeatable, however uncertainty in resonant frequency and C_{oss} (taken from datasheet) reduce inductance estimation accuracy to within $\pm 100\,\text{pH}$ using this transient-based method at 1 nH.

Impedance-based measurement

With proper calibration and configuration, the impedance analyzer[3] testbed provides relatively accurate measurements of impedance (magnitude and phase) across frequency. Measured data can be used to directly compute loop inductance as

$$L_{\text{c}} \approx \frac{1}{\omega} \cdot \left(X_{\text{meas}} + \frac{1}{\omega C_{\text{b}}} \right) \tag{6.4}$$

by assuming an equivalent series RLC circuit model, where the series (bypass) capacitance is a known quantity set by discrete components[4] and X_{meas} is the measured reactance of the

[3] Keysight E4990A impedance analyzer with 42941A impedance probe.
[4] $C_{\text{b}} = 4 \times 47\,\text{nF}$, 450 V, TDK C2012X7T2W473K125AA

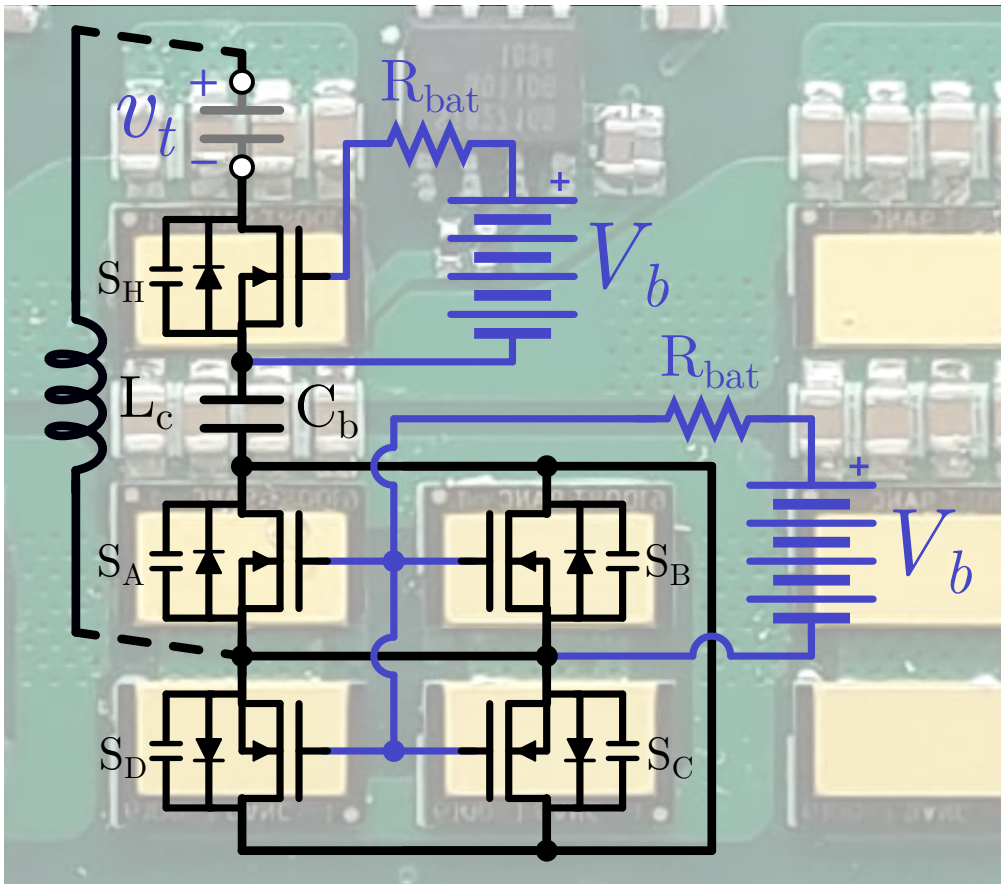


Figure 6.6: Impedance-based measurement testbench and overlayed circuit schematic of the switching cell commutation loop across v_t. Batteries ($V_\mathrm{b} = 6\,\mathrm{V}$, $R_\mathrm{bat} = 1\,\mathrm{k\Omega}$) keep the GaN FETs in the on-state.

loop. For these measurements, the DUT is a single switching cell configured similarly to the actual hardware during normal power conversion operation. This includes the HS GaN FET, some combination of the paralleled LS GaN FETs, and one set of bypass capacitors as shown in Fig. 6.6. To maximize capacitance per unit volume, the bypass capacitor(s) in this DUT is a Class II dielectric and thus de-rates with applied voltage. The value of C_b used in (6.4) closely matches the manufacturer's zero-voltage-bias specifications, however it can be refined by examining X_meas at low frequencies where the impedance of C_b dominates as

$$X_\mathrm{meas} \approx X_{C_\mathrm{b}} = -\frac{1}{\omega C_\mathrm{b}}. \tag{6.5}$$

All the GaN FETs are held in an ohmic "on" state by utilizing two batteries which provide a stable, isolated, and noiseless $V_\mathrm{b} = 6\,\mathrm{V}$ dc voltage across each of the gate-source terminals, V_gs, for the HS and LS as shown in Fig. 6.6. Much of the loop area is defined

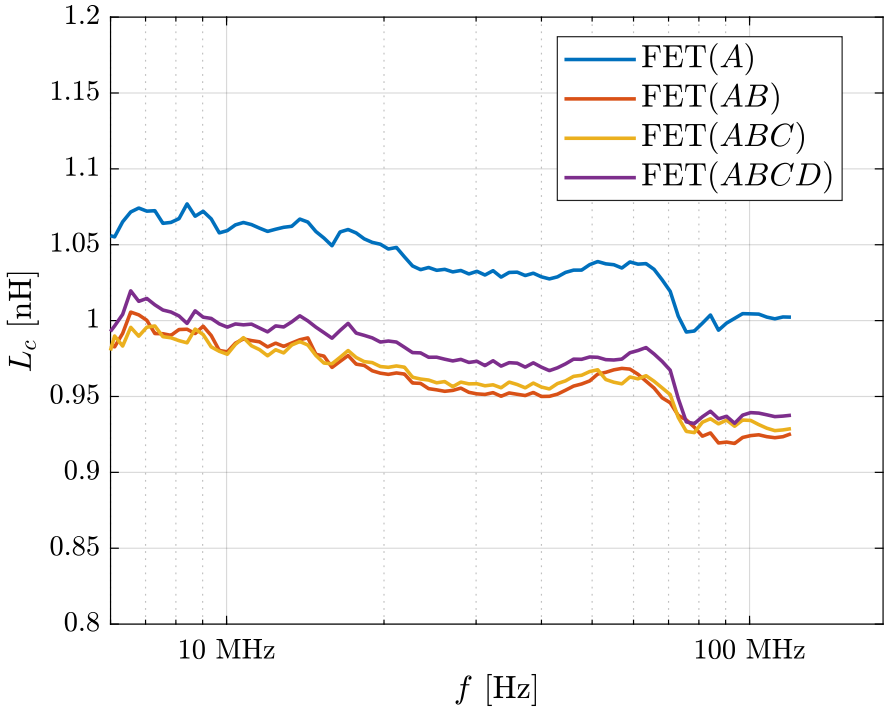


Figure 6.7: Measured commutation loop inductance across frequency, $L_c(f)$, processed from direct impedance measurement of the DUT using an impedance analyzer. Results are shown for increasingly paralleled quantities of low-side FETs.

by the GaN FETs, thus a testbench incorporating the FETs in an on-state captures the essential interactions of package inductance with the PCB traces including the solder joint to the pad, internal wire bonding to the die, and the die itself. These FETs must be in the on-state otherwise the impedance of C_{oss} irrevocably dominates the measurement and extraction of L_c becomes impractical.

Results for the inductance of the commutation loop across frequency, L_c, are shown in Fig. 6.7 for different circuit configurations. This data demonstrates that after the addition of the first minor loop path (FET B) to the major loop (FET A), additional paralleled LS FETs (FET C and D) negligibly reduce L_c. Evaluated results of (6.5) yield $L_c = 0.94\,\text{nH}$ at $f = 100\,\text{MHz}$ including all paralleled FETs as shown in Table 6.1. Repeated measurements indicate accurate inductance measurement to within $\pm 50\,\text{pH}$ using this method, however accuracy degrades quickly for values below 1 nH and approaches the minimum resolution of the utilized impedance analyzer.

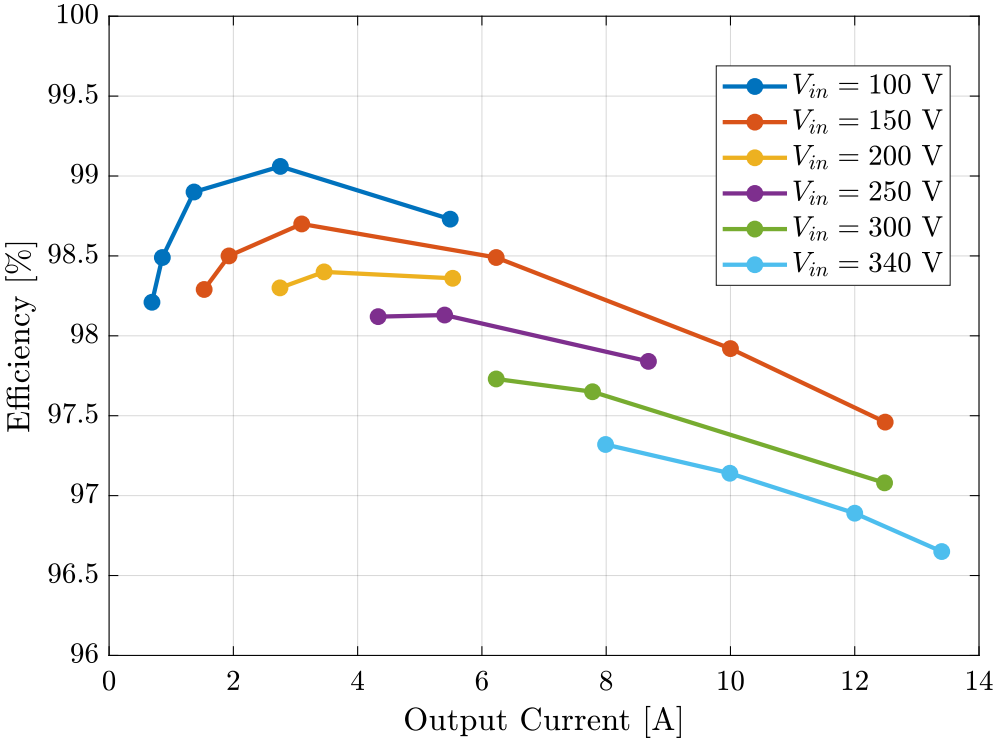


Figure 6.8: Measured dc-dc efficiency measurements across various input voltages and resistive loads for the 6-level FCML buck converter with asymmetrical switching cell design. Switching frequency $f_s = 100$ kHz and output voltage $V_o = 48$ V.

Summary of experimental results

Based on the results in Table 6.1, the commutation loop inductance for the full system is approximately $L_c \approx 1.0$ nH especially considering the implicit reduction from the additional large but non-negligible minor commutation paths afforded by each parallel FET. For variations in experimental and simulation testbeds, the actual DUT differs slightly: the transient and impedance tests include all FETs and bypass capacitors while the Q3D simulation includes no real components but merely homogeneous rectangular segments. Inspection of Table 6.1 indicates increasing L_c for testbeds with additional physical components. This trend is expected, especially when considering device parasitics and consequential package height compared to an ideal copper short that is flush with the PCB surface. There is also good agreement between measurements taken utilizing the transient-based and impedance-based experimental methods.

Dc-dc Efficiency Evaluation

Although a multi-purpose prototype, the converter remains a highly volume-optimized design effective across a wide range of voltage conversion ratios with an enclosed box volume of 45 cm^3 (2.7 in^3) at a rated power throughput of 650 W resulting in an 14 W/cm^3 (240 W/in^3) volumetric power density. The input/output efficiency for dc-dc operating conditions are recorded in Fig. 6.8 for a fixed output voltage across a range of input voltages and resistive loads. The present full-load efficiency at $P_o = 650\,W$ for a 7-to-1 conversion ratio is $\eta = 96.6\,\%$. Additionally, the efficiency results presented in Fig. 6.8 are thermally limited at $P_o = 650\,W$ with forced air cooling (400 LFM) and no heatsink.

6.4 Conclusion

The proposed asymmetrical hybrid PCB layout design for the switching cell of flying capacitor multilevel (FCML) converter jointly utilizes the fast switching transitions of GaN semiconductors while minimizing conduction losses in high step-down dc-dc applications. Paired with the inherent benefits of a multilevel topology—lower voltage rated switches and smaller overall passive component volume—marked improvement of the layout, quantified by experimentally validated sub-1 nH commutation loop inductance, results in a simultaneously high step-down, high power density, high efficiency power converter. This chapter produces an improved layout structure for a buck dc-dc converter with wide input voltage and conversion ratio range, which is well suited to the buck PFC converter application.

Chapter 7

Power Factor and Harmonic Limitations of the Buck PFC Converter

7.1 Introduction

The conventional single-phase boost PFC [171] is capable of achieving near-unity power factor, and this converter type is appropriate when the dc-side is a higher voltage than the ac-side voltage. However in several applications with eventual low-voltage loads—such as datacenter rectifiers—a single-stage step-down rectifier, or a buck PFC rectifier, could yield system level volume and efficiency improvements [30]. Unfortunately, the buck PFC rectifier is incapable of achieving ideally unity power factor or null harmonic distortion as it has a nonzero cutoff angle near the zero-crossing of the ac-side voltage.

This chapter comprehensively explores the theoretical limitations of power factor and current harmonics for the general buck-type PFC converter. Non-zero cutoff angle has been investigated for a variable switching frequency boost PFC circuit [36]. Other work has thoroughly analyzed the harmonic compliance capabilities of buck PFC input current, but for a different waveshape [71]. This chapter specifically considers the truncated buck PFC current waveform as shown in Fig. 7.1 and generalizes analytical expressions dependent on both the cutoff angle and displacement angle. It also derives the conditions for which the ideal truncated waveform conforms to grid-tied regulatory limits of the IEC current harmonic emissions standards.

7.2 Framing the Problem

For a general buck (direct step-down) ac-dc converter, the input current i_{in} becomes truncated when the rectified ac input voltage v_{in} is instantaneously less the dc output voltage

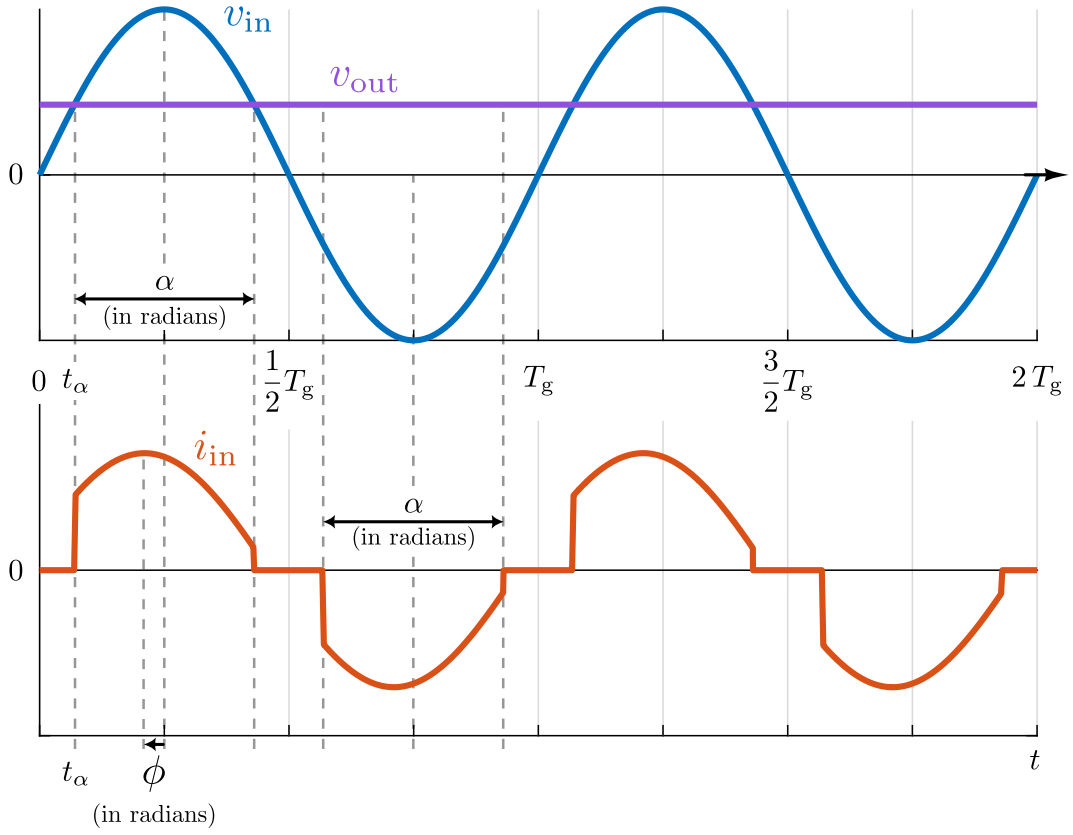


Figure 7.1: Theoretical voltage and current waveforms for the buck PFC. The conduction angle α and displacement angle of the current ϕ are denoted.

$v_{\text{out}} \approx V_{\text{out}}$. It can be expressed analytically as

$$i_{\text{in}}(t) = \begin{cases} I_{\text{in}} \sin(\omega t + \phi) & : \ |v_{\text{in}}| > v_{\text{out}} \\ 0 & : \ |v_{\text{in}}| < v_{\text{out}} \end{cases} \tag{7.1}$$

and shown graphically in Fig. 7.1. The displacement angle ϕ (in radians) is the displacement between the ideal line frequency voltage and non-truncated current waveform. The conduction angle α indicates the "on" time (in radians) of the converter in each half-period and where the input (ac) voltage is instantaneously greater than the output (dc) voltage. Deriving the time t_α at which $v_{\text{in}}(t) = v_{\text{out}}(t)$

$$\begin{aligned} v_{\text{in}}(t_\alpha) &= v_{\text{out}}(t_\alpha) \\ V_{\text{in}} \sin(\omega t_\alpha) = V_{\text{in}} \sin\left(\frac{\pi}{2} - \frac{\alpha}{2}\right) &= V_{\text{out}} \end{aligned} \tag{7.2}$$

and solving for the conduction angle α yields

$$\alpha = \pi - 2\arcsin\left(\frac{V_{\text{out}}}{V_{\text{in}}}\right). \tag{7.3}$$

Simple analysis of rms value and power factor

To derive the rms value and power factor of (7.1), first consider the terms

$$x = \frac{\alpha}{\pi} \tag{7.4}$$

$$y = \frac{1}{\pi}\sin(\alpha) \tag{7.5}$$

which will become useful in later derivations.

The RMS value of the buck PFC input current waveform is

$$\begin{aligned} I_{\text{rms}} &= \sqrt{\frac{1}{T}\int_0^T i_{\text{in}}^2(t)\,\mathrm{d}t} \\ &= \sqrt{\frac{\omega}{2\pi}\int_0^{\frac{2\pi}{\omega}} i_{\text{in}}^2(t)\,\mathrm{d}t} \\ &= \sqrt{\frac{\omega}{\pi}\int_{\frac{\pi-\alpha}{2\omega}}^{\frac{\pi+\alpha}{2\omega}} I_{\text{in}}^2\sin^2(\omega t+\phi)\,\mathrm{d}t} \\ &= \frac{1}{\sqrt{2}}I_{\text{in}}\sqrt{\frac{1}{\pi}\alpha + \frac{1}{\pi}\sin(\alpha)\cos(2\phi)} \\ &= \frac{1}{\sqrt{2}}I_{\text{in}}\sqrt{x + y\cos(2\phi)} \end{aligned} \tag{7.6}$$

which simplifies when $\phi = 0$ to

$$I_{\text{rms}} = \frac{1}{\sqrt{2}}I_{\text{in}}\sqrt{x+y} \tag{7.7}$$

Next, to find the rms value of the fundamental frequency component of $i_{\text{in}}(t)$, the fundamental Fourier coefficients can be evaluated as

$$\begin{aligned} a_1 &= \frac{4}{T}\int_{\frac{\pi-\alpha}{2\omega}}^{\frac{\pi+\alpha}{2\omega}} I_{\text{in}}\sin(\omega t+\phi)\cdot\cos(\omega t)\,\mathrm{d}t \\ &= I_{\text{in}}\sin(\phi)\cdot(x-y) \end{aligned} \tag{7.8}$$

and

$$\begin{aligned} b_1 &= \frac{4}{T}\int_{\frac{\pi-\alpha}{2\omega}}^{\frac{\pi+\alpha}{2\omega}} I_{\text{in}}\sin(\omega t+\phi)\cdot\sin(\omega t)\,\mathrm{d}t \\ &= I_{\text{in}}\cos(\phi)\cdot(x+y) \end{aligned} \tag{7.9}$$

which simplifies when $\phi = 0$ to

$$a_1 = 0 \tag{7.10}$$

and

$$b_1 = I_{\text{in}}\cdot(x+y) \tag{7.11}$$

Then the RMS of the fundamental of $i_{\text{in}}(t)$ when $\phi = 0$ is

$$I_{1,\text{rms}} = \frac{\sqrt{a_1^2+b_1^2}}{\sqrt{2}} = \frac{1}{\sqrt{2}}I_{\text{in}}\cdot(x+y) \tag{7.12}$$

Finally the power factor (when $\phi = 0$) can be derived as

$$\text{PF} = \frac{I_{1,\text{rms}}}{I_{\text{rms}}} = \frac{\frac{1}{\sqrt{2}}I_{\text{in}}\cdot(x+y)}{\frac{1}{\sqrt{2}}I_{\text{in}}\sqrt{x+y}} = \sqrt{x+y} = \sqrt{\frac{\alpha}{\pi}+\frac{1}{\pi}\sin(\alpha)} \tag{7.13}$$

At a $V_{\text{out}} = 48$ V average output voltage the conduction angle α evaluates at high line ($V_{\text{in,rms}} = 240$ V_{rms}) as $\alpha = 2.8578$ radians and at low line ($V_{\text{in,rms}} = 120$ V_{rms}) as $\alpha = 2.568$ radians. Consequently, the theoretical maximum power factor (PF) achievable is PF = 0.999396 at high line and PF = 0.995066 at low line input voltage. These theoretically attainable values are nearly unity which corresponds to the intuition that minimal instantaneous power flows into the converter near the line voltage zero-crossing.

7.3 Fourier Series Decomposition

The Fourier series decomposition of the input current (7.1) is defined in sine-cosine form as

$$i_{\text{in}}(t) = \frac{a_0}{2}+\sum_{n=1}^{\infty} a_n\cos(n\omega t)+b_n\sin(n\omega t) \tag{7.14}$$

The Fourier series coefficients a_n and b_n—which are functions of the conduction angle α and nominal fundamental phase displacement ϕ—of the truncated input current $i_{\text{in}}(t)$ in (7.1) can be evaluated as

$$a_0 = \frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} i_{\text{in}}(t)\,\mathrm{d}t = 0 \tag{7.15}$$

$$
\begin{aligned}
a_n &= \frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} i_{\text{in}}(t)\cdot\cos(n\omega t)\,\mathrm{d}t \\
&= \frac{\omega}{\pi}\int_{\frac{\pi-\alpha}{2\omega}}^{\frac{\pi+\alpha}{2\omega}} I_{\text{in}}\sin(\omega t+\phi)\cdot\cos(n\omega t)\,\mathrm{d}t + \frac{\omega}{\pi}\int_{-\frac{\pi+\alpha}{2\omega}}^{-\frac{\pi-\alpha}{2\omega}} I_{\text{in}}\sin(\omega t+\phi)\cdot\cos(n\omega t)\,\mathrm{d}t \\
&= \begin{cases}
I_{\text{in}}\cdot\dfrac{4\pi}{n^2-1}\sin\Big(n\dfrac{\pi}{2}\Big)\Big(\cos\Big(\dfrac{\alpha}{2}\Big)\sin\Big(n\dfrac{\alpha}{2}\Big) \\
\qquad\qquad -n\sin\Big(\dfrac{\alpha}{2}\Big)\cos\Big(n\dfrac{\alpha}{2}\Big)\Big)\cdot\sin(\phi) & :\ n\in\mathbb{Z}, n>1 \\
I_{\text{in}}\cdot\dfrac{1}{\pi}\big(\alpha-\sin(\alpha)\big)\cdot\sin(\phi) & :\ n=1
\end{cases}
\end{aligned}
\tag{7.16}
$$

and

$$
\begin{aligned}
b_n &= \frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} i_{\text{in}}(t)\cdot\sin(n\omega t)\,\mathrm{d}t \\
&= \frac{\omega}{\pi}\int_{\frac{\pi-\alpha}{2\omega}}^{\frac{\pi+\alpha}{2\omega}} I_{\text{in}}\sin(\omega t+\phi)\cdot\sin(n\omega t)\,\mathrm{d}t + \frac{\omega}{\pi}\int_{-\frac{\pi+\alpha}{2\omega}}^{-\frac{\pi-\alpha}{2\omega}} I_{\text{in}}\sin(\omega t+\phi)\cdot\sin(n\omega t)\,\mathrm{d}t \\
&= \begin{cases}
I_{\text{in}}\cdot\dfrac{4\pi}{n^2-1}\sin\Big(n\dfrac{\pi}{2}\Big)\Big(n\cos\Big(\dfrac{\alpha}{2}\Big)\sin\Big(n\dfrac{\alpha}{2}\Big) \\
\qquad\qquad -\sin\Big(\dfrac{\alpha}{2}\Big)\cos\Big(n\dfrac{\alpha}{2}\Big)\Big)\cdot\cos(\phi) & :\ n\in\mathbb{Z}, n>1 \\
I_{\text{in}}\cdot\dfrac{1}{\pi}\big(\alpha+\sin(\alpha)\big)\cdot\cos(\phi) & :\ n=1
\end{cases}
\end{aligned}
\tag{7.17}
$$

For the sine-cosine form in (7.14), the magnitude-phase form of the Fourier Series is defined as

$$
i_{\text{in}}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} c_n\sin(n\omega t+\phi_n) \tag{7.18}
$$

where

$$
c_n = \sqrt{a_n^2+b_n^2} \tag{7.19}
$$

and

$$
\phi_n = \arctan(a_n,b_n) = \begin{cases}
\arctan\Big(\dfrac{a_n}{b_n}\Big) & :\ b_n\geq 0 \\
\pi+\arctan\Big(\dfrac{a_n}{b_n}\Big) & :\ b_n<0
\end{cases}
\tag{7.20}
$$

Displacement Factor

There are two primary independent measures of waveform quality, displacement factor k_i and distortion factor k_d. Displacement factor indicates how much of the fundamental frequency component of current contributes to active versus reactive power. Greater reactive power increases losses in the power converter circuit without increasing the real power throughput of the system. The greater percentage of current which contributes to real power throughput, the less adverse impact on the downstream converter and the upstream grid utility which must filter and compensate current pollution.

The truncation of $i_{\text{in}}(t)$ results in a slight shift in the phase displacement of the fundamental harmonic from the non-truncated ideal (i.e., $i_{\text{in}}(t) = I_{\text{in}} \sin(\omega t + \phi)$). Evaluating the phase (7.20) at the fundamental frequency yields

$$\phi_1 = \arctan\Big(\frac{\alpha - \sin(\alpha)}{\alpha + \sin(\alpha)} \cdot \tan(\phi)\Big) \tag{7.21}$$

Although a non-sensical operating case for a buck PFC, if the conduction angle is maximized as $\alpha = \pi$ (no truncation), then the phase displacement of the desired input current, ϕ, and actual truncated current, ϕ_1, are equivalent as shown by evaluating (7.21). As the conduction angle α decreases from π to zero, the effective fundamental phase displacement of the truncated input current deviates further from the expected ϕ and this relationship is visualized in Fig. 7.3. For the full range of possible, albeit likely unrealistic, operating parameters α and ϕ, investigation of (7.21) yields a constraint on ϕ_1 of

$$0 < |\phi_1| < |\phi| \ : \ -\frac{\pi}{2} \leq \phi \leq \frac{\pi}{2}, \ 0 < \alpha < \pi \tag{7.22}$$

which indicates more truncation of the input current always favorably diminishes the fundamental phase displacement to the grid.

The displacement factor of the truncated input current is defined as the cosine of the fundamental phase displacement and can be simplified to

$$\begin{aligned} k_i &:= \cos(\phi_1) \\ &= \cos\left(\arctan\Big(\frac{\alpha - \sin(\alpha)}{\alpha + \sin(\alpha)} \cdot \tan(\phi)\Big)\right) \\ &= \frac{\alpha + \sin(\alpha)}{\sqrt{\big(\alpha + \sin(\alpha)\big)^2 - 4\alpha \sin(\alpha) \cdot \sin^2(\phi)}} \cdot \cos(\phi) \end{aligned} \tag{7.23}$$

Displacement factor is a unity normalized performance metric which means it is best when $k_i = 1$ and worst when $k_i = 0$. Truncation of the input current always improves the displacement factor relative to a non-truncated ideal. However, truncation also permits any phase displacement to couple into and degrade the distortion factor.

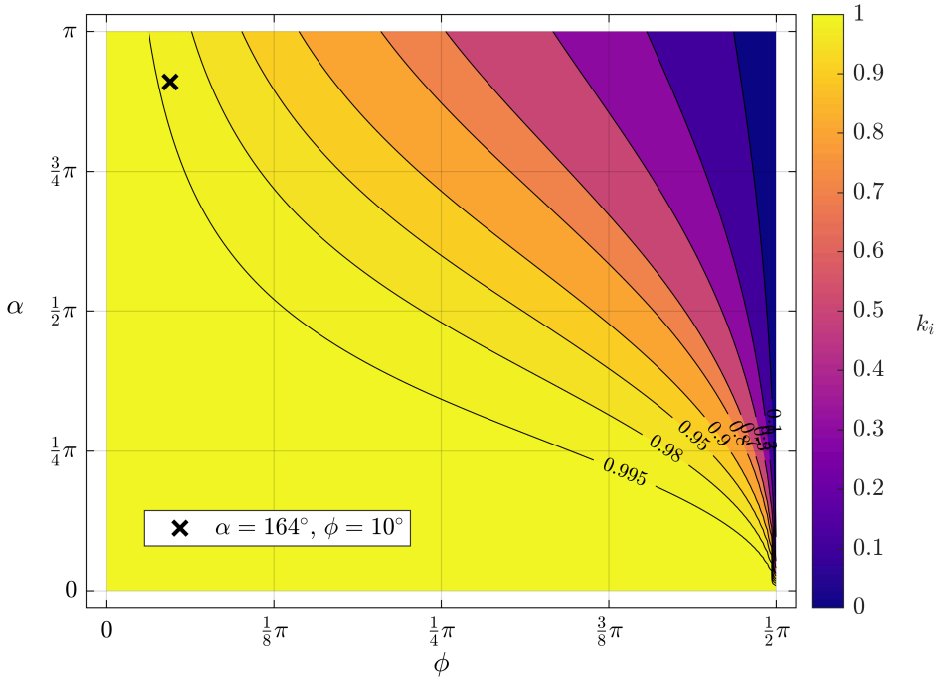
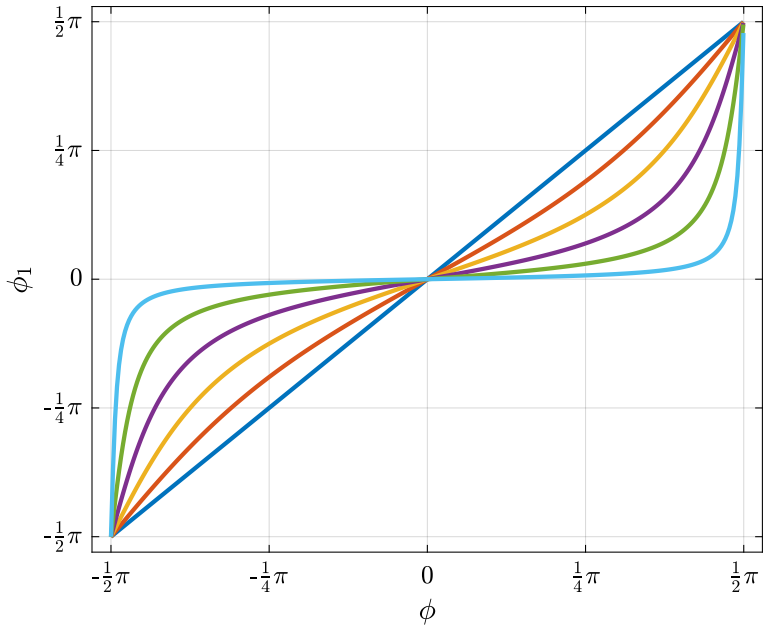
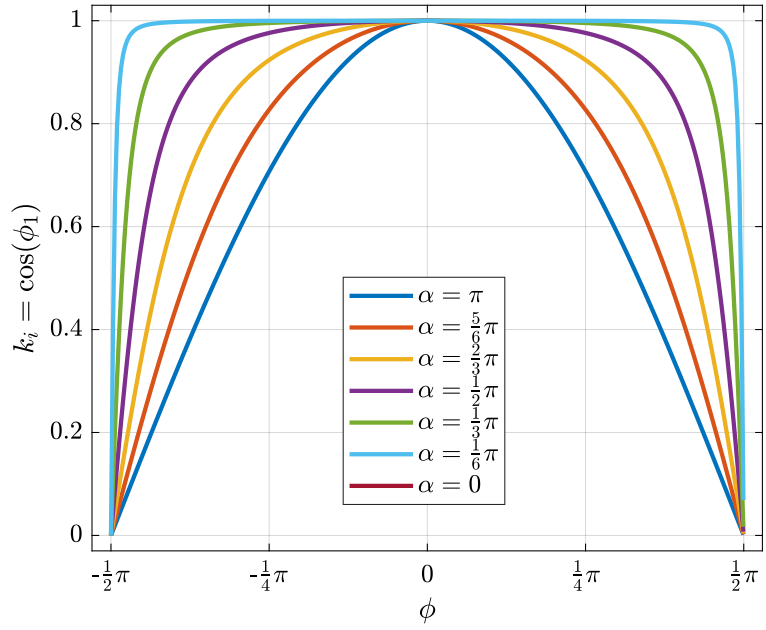


Figure 7.2: Displacement factor k_i as a function of α and ϕ.



(a)



(b)

Figure 7.3: Change in fundamental phase ϕ_1 and displacement factor k_i as a function of ϕ for varied α.

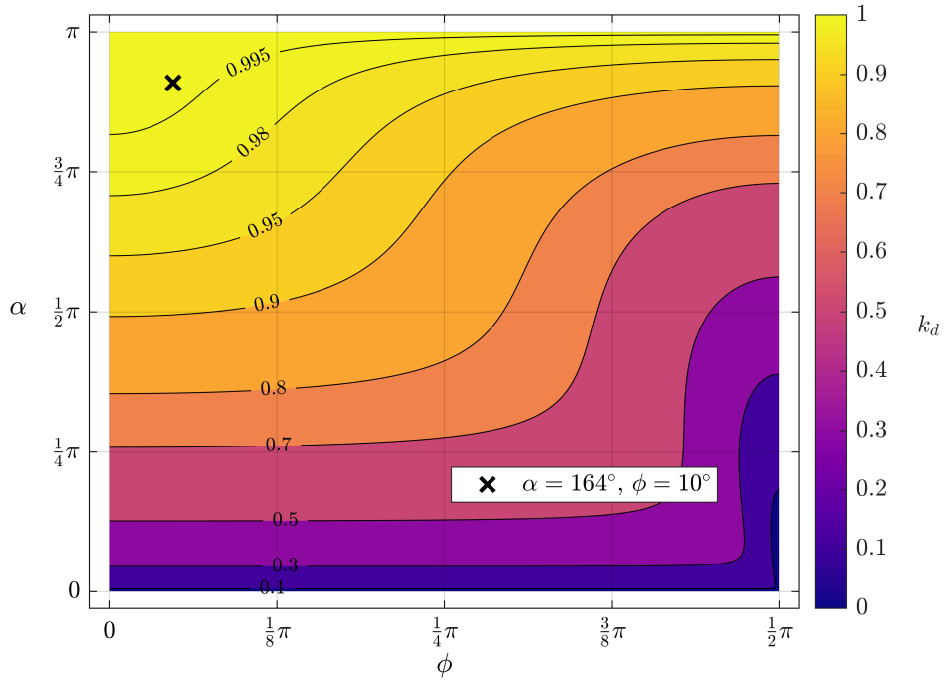


Figure 7.4: Distortion factor k_d as a function of α and ϕ.

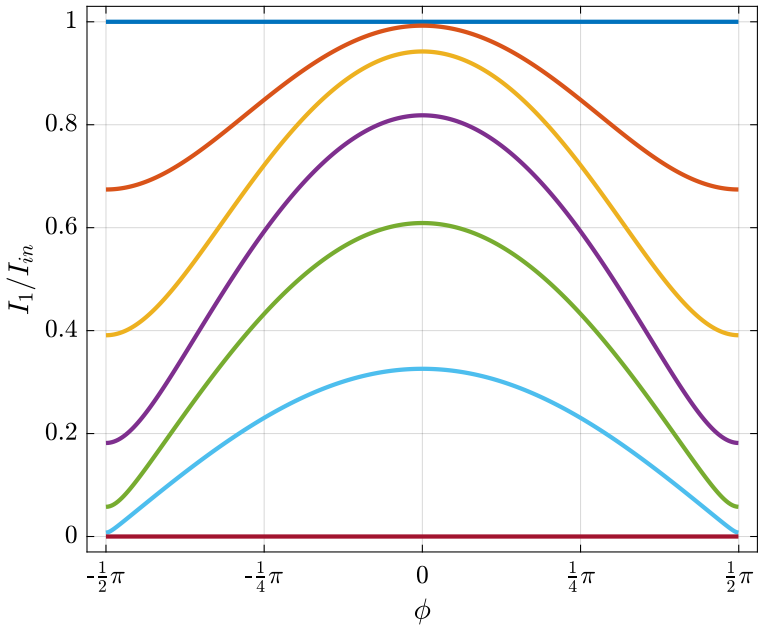
Distortion Factor

The RMS value of the truncated buck PFC input current waveform in (7.1) is

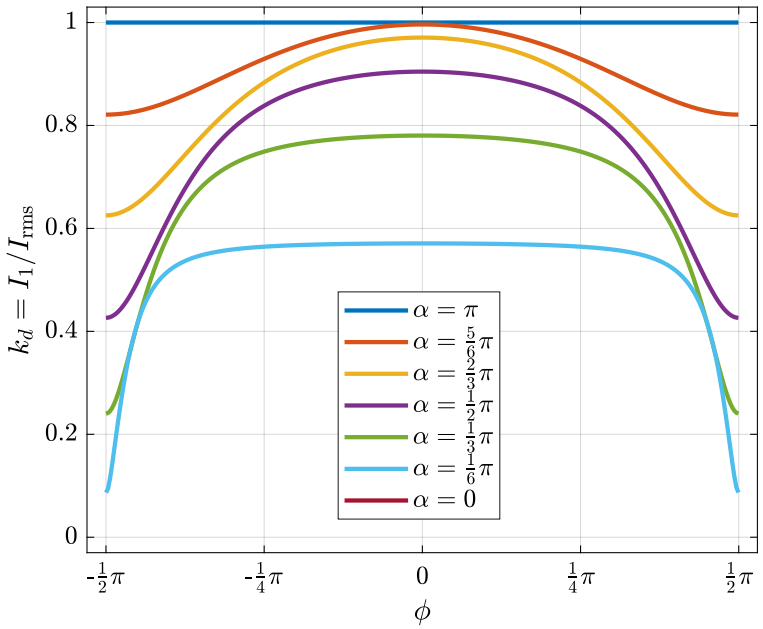
$$\begin{aligned} I_{\text{rms}} &= \sqrt{\frac{1}{T}\int_0^T i_{\text{in}}^2(t)\,\mathrm{d}t} \\ &= \sqrt{\frac{\omega}{\pi}\int_{\frac{\pi-\alpha}{2\omega}}^{\frac{\pi+\alpha}{2\omega}} I_{\text{in}}^2 \sin^2(\omega t+\phi)\,\mathrm{d}t} \\ &= \frac{1}{\sqrt{2}} I_{\text{in}} \sqrt{\frac{1}{\pi}\alpha + \frac{1}{\pi}\sin(\alpha)\cos(2\phi)} \end{aligned} \tag{7.24}$$

The magnitude of the truncated input current's fundamental frequency component $c_1(\alpha,\phi)$ is simplified by substituting (7.16) and (7.17) into (7.19) and reducing to

$$\begin{aligned} c_1(\alpha,\phi) &= \sqrt{a_1^2+b_1^2} \\ &= \frac{1}{\pi} I_{\text{in}} \sqrt{\big(\alpha+\sin(\alpha)\big)^2 - 4\alpha\sin(\alpha)\cdot\sin^2(\phi)} \end{aligned} \tag{7.25}$$



(a)



(b)

Figure 7.5: Change in fundamental magnitude I_1 and displacement factor k_d for varied α.

From inspection of (7.25) the magnitude of the truncated input current's fundamental frequency component $c_1(\alpha, \phi)$ is constrained by its maximum when $\phi = 0$

$$c_1(\alpha, \phi) \leq c_1(\alpha, 0) \ : \ -\frac{\pi}{2} \leq \phi \leq \frac{\pi}{2}, \ 0 \leq \alpha \leq \pi \tag{7.26}$$

since $4\alpha \sin(\alpha) \cdot \sin^2(\phi) > 0$ over the domain of α and ϕ.

The (peak) magnitude of each harmonic n of the input current $i_{\text{in}}(t)$ is defined as

$$I_n := c_n(\alpha, \phi) \tag{7.27}$$

and the rms of each harmonic is consequently defined as

$$I_{n,\text{rms}} := \frac{1}{\sqrt{2}} I_n \tag{7.28}$$

The total harmonic distortion is a measure of the harmonic pollution of a waveform. Substituting (7.24) and (7.27) evaluated at $n = 1$ yields

$$\begin{aligned} \text{THD}_i &:= \sqrt{\frac{\sum_{n=2}^{\infty} I_n^2}{I_1^2}} = \sqrt{\frac{I_{\text{rms}}^2 - \frac{1}{2} I_1^2}{\frac{1}{2} I_1^2}} \\ &= \sqrt{\frac{\pi\big(\alpha + \sin(\alpha)\big) - \big(\alpha + \sin(\alpha)\big)^2 + (4\alpha - 2\pi)\sin(\alpha) \cdot \sin^2(\phi)}{\big(\alpha + \sin(\alpha)\big)^2 - 4\alpha \sin(\alpha) \cdot \sin^2(\phi)}} \end{aligned} \tag{7.29}$$

The distortion factor is another unity normalized metric component of waveform pollution.

$$\begin{aligned} k_d &:= \frac{1}{\sqrt{1 + \text{THD}_i^2}} = \frac{I_{1,\text{rms}}}{I_{\text{rms}}} \\ &= \frac{\frac{1}{\sqrt{2}} I_{\text{in}} \sqrt{\frac{1}{\pi^2}\big(\alpha + \sin(\alpha)\big)^2 - \frac{4}{\pi^2}\alpha \sin(\alpha) \cdot \sin^2(\phi)}}{\frac{1}{\sqrt{2}} I_{\text{in}} \sqrt{\frac{1}{\pi}\alpha + \frac{1}{\pi}\sin(\alpha) \cdot \cos(2\phi)}} \\ &= \sqrt{\frac{1}{\pi} \cdot \frac{\big(\alpha + \sin(\alpha)\big)^2 - 4\alpha \sin(\alpha) \cdot \sin^2(\phi)}{\big(\alpha + \sin(\alpha)\big) - 2\sin(\alpha) \cdot \sin^2(\phi)}} \end{aligned} \tag{7.30}$$

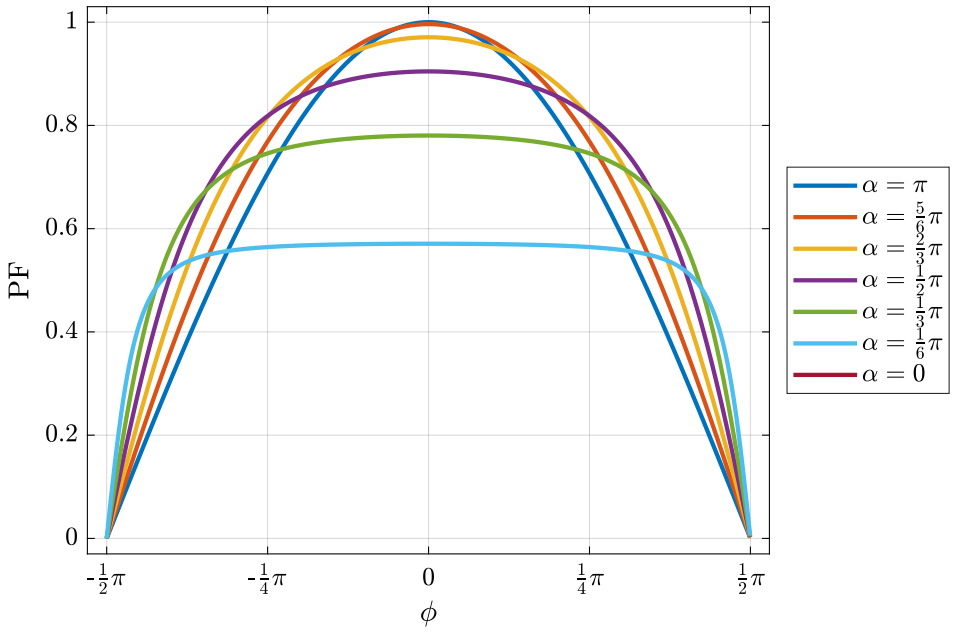


Figure 7.6: Total power factor PF as a function of ϕ for varied α.

Finally the overall power factor (another unity normalized metric) is defined as the product of the distortion factor k_i and and displacement factor k_d as

$$
\begin{aligned}
\mathrm{PF} &:= k_d \cdot k_i \\
&= \left(\sqrt{\frac{1}{\pi} \cdot \frac{\big(\alpha + \sin(\alpha)\big)^2 - 4\alpha \sin(\alpha) \cdot \sin^2(\phi)}{\big(\alpha + \sin(\alpha)\big) - 2\sin(\alpha) \cdot \sin^2(\phi)}} \right) \cdot \left(\frac{\big(\alpha + \sin(\alpha)\big) \cdot \cos(\phi)}{\sqrt{\big(\alpha + \sin(\alpha)\big)^2 - 4\alpha \sin(\alpha) \cdot \sin^2(\phi)}} \right) \\
&= \sqrt{\frac{1}{\pi} \cdot \frac{\big(\alpha + \sin(\alpha)\big)^2 \cdot \cos^2(\phi)}{\alpha + \sin(\alpha) \cdot \cos(2\phi)}} \\
&= \frac{\big(\alpha + \sin(\alpha)\big) \cdot \cos(\phi)}{\sqrt{\pi\alpha + \pi \sin(\alpha) \cdot \cos(2\phi)}} \quad : \quad -\frac{\pi}{2} \leq \phi \leq \frac{\pi}{2}, \; 0 < \alpha < \pi
\end{aligned}
\tag{7.31}
$$

Investigation of Fig. 7.6 shows that although input current truncation does diminish the maximum possible power factor from unity, it also helps alleviate some of the adverse impacts of phase displacement. A truncated input current waveform can achieve similar harmonic pollution over a range of displacement. The lower the conduction angle, the greater invariability to displacement.

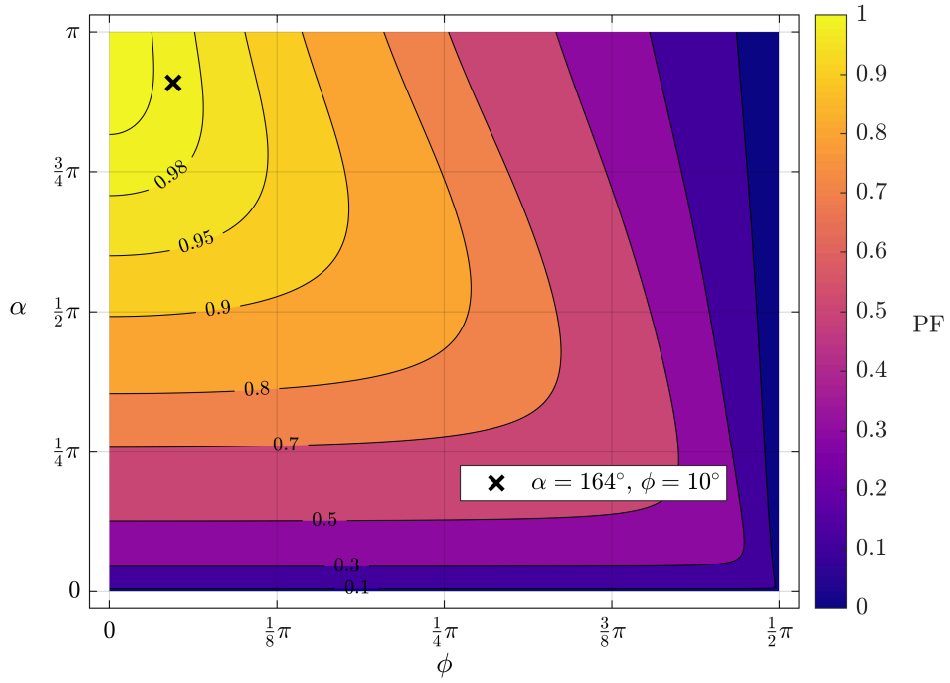


Figure 7.7: Total power factor PF as a function of α and ϕ.

When $\phi = 0$

In the case of no phase displacement when $\phi = 0$, the Fourier coefficients simplify to

$$a_n(\alpha, 0) = 0 \tag{7.32}$$

and

$$b_n(\alpha,0) = \begin{cases} I_{\text{in}} \cdot \dfrac{4\pi}{n^2-1} \sin\left(n\dfrac{\pi}{2}\right)\left(n\cos\left(\dfrac{\alpha}{2}\right)\sin\left(n\dfrac{\alpha}{2}\right) - \sin\left(\dfrac{\alpha}{2}\right)\cos\left(n\dfrac{\alpha}{2}\right)\right) & : \ n \in \mathbb{Z}, n > 1 \\ I_{\text{in}} \cdot \dfrac{1}{\pi}\big(\alpha + \sin(\alpha)\big) & : \ n = 1 \end{cases} \tag{7.33}$$

Thus,

$$c_n(\alpha, 0) = b_n(\alpha, 0) \tag{7.34}$$

Other terms simplify to

$$\phi_1 = \phi \tag{7.35}$$

$$k_i = 1 \tag{7.36}$$

$$I_{\text{rms}} = \frac{1}{\sqrt{2}} I_{\text{in}} \sqrt{\frac{1}{\pi}\alpha + \frac{1}{\pi}\sin(\alpha)} \tag{7.37}$$

$$I_n = b_n(\alpha, 0) \tag{7.38}$$

$$\begin{aligned} \text{THD}_i &= \sqrt{\frac{\pi\big(\alpha + \sin(\alpha)\big) - \big(\alpha + \sin(\alpha)\big)^2}{\big(\alpha + \sin(\alpha)\big)^2}} \\ &= \sqrt{\frac{\pi}{\alpha + \sin(\alpha)} - 1} \end{aligned} \tag{7.39}$$

$$k_d = \sqrt{\frac{1}{\pi}\alpha + \frac{1}{\pi}\sin(\alpha)} \tag{7.40}$$

$$\text{PF} = k_d = \sqrt{\frac{1}{\pi}\alpha + \frac{1}{\pi}\sin(\alpha)} \tag{7.41}$$

7.4 Regulatory Standards

There is presently no international regulatory standard for single-phase systems with voltage less than 220 V_{rms}. However due to unique technical differences in its electric power system, Japan created a standard in 2001 which could be applied to lower voltage grids (namely 110 V_{rms}). This standard was prepared by Japan's Ministry of Economy, Trade and Industry (METI) and issued by the IEC SC77A Japanese National Committee [63]. In 2003, the IEC SC77A Japanese National Committee was superseded by the Japanese Industrial Standards (JIS) Committee as a standardizing body. The present Japanese standard for current harmonic emissions (JIS C 61000-3-2:2019) issued by JIS [96] adheres very closely to the associated international standard (IEC 61000-3-2:2018) [95], however it retains the original unique Japanese provisions for line voltages less than 220 V_{rms} established in the earlier Japanese standard [63].

Table 7.1: IEC 61000-3-2: Limits for Class D equipment (75 W $< P_{in} <$ 600 W)

Harmonic order n	Max. permissible harmonic current per Watt [mA/W]	Max. permissible harmonic current [A]
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13	$\frac{3.85}{13}$	0.21
$15 \leq n$ (odd) ≤ 39	$\frac{3.85}{n}$	$0.15 \cdot \frac{15}{n}$

Similar to the IEC standard, the JIS standard distinguishes electronic equipment into the same A, B, C, and D classifications. The JIC standard additionally scales the Class A and Class D harmonic limits of the IEC standard by a factor relative to the nominal operating voltage, V_{nom}. As an example the Class A limit for harmonic $n = 3$ is computed as

$$I_{3,JIS} = I_{3,IEC} \cdot \frac{(230\ V_{rms})}{V_{nom}} = (2.30\ A) \cdot \frac{(230\ V_{rms})}{V_{nom}} \tag{7.42}$$

which effectively increases current harmonic limits at lower voltages. Additionally, if the nominal system voltage is 220 $V_{rms} \leq V_{nom} \leq$ 240 V_{rms}, then $V_{nom} =$ 230 V_{rms} is used in the limit calculation. In this way the JIS and IEC standards are equivalent for the same relevant application range of $V_{nom} >$ 220 V_{rms} (and $V_{nom} <$ 240 V_{rms}).

There is work [135] that investigates the technical impact of scaling the IEC harmonics limits with system voltage. It was determined some equipment rated as "univeral ac input"

Table 7.2: IEC 61000-3-2: Limits for Class A equipment ($P_{\text{in}} > 600$ W)

Harmonic order n	Max. permissible harmonic current [A]
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
$13 \leq n$ (odd) ≤ 39	$0.15 \cdot \frac{15}{n}$
2	2.30
4	1.14
6	0.77
$8 \leq n$ (even) ≤ 40	$0.23 \cdot \frac{8}{n}$

(i.e., 90 $V_{\text{rms}} \leq V_{\text{nom}} \leq 250$ V_{rms}) and designed for worldwide grids might pass emissions limits according to the JIS standard at low voltage but fail according to the IEC standard at high voltage. Considering the nonlinearity of power electronics equipment, it is not yet clear if a linear scaling (as in the JIS standard) provides a fair methodology for regulating emissions at low voltage. Notably, the IEC standard explicitly states it has not considered (or arbitrated) limits for cases where $V_{\text{nom}} < 220$ V_{rms} which implies there is no common consensus yet.

Additionally the IEC61000-3-12 standard [97] applies for rated input current greater than 16 A_{rms}, which for a $V_{\text{nom}} = 240$ V_{rms} system corresponds to $P_{\text{nom}} = 3840$ W.

Application of Current Emissions Standards

We can define the nominal power throughput assuming a non-truncated input current waveform as

$$P_{\text{nom}} := \frac{V_{\text{in}} I_{\text{in}}}{2} \tag{7.43}$$

The true active input power of the system is defined as the average of the instantaneous power input

$$P_{\text{in}} := \langle p_{\text{in}}(t) \rangle = \frac{1}{T} \int_0^T p_{\text{in}}(t)\, \mathrm{d}t = \frac{1}{T} \int_0^T v_{\text{in}}(t) \cdot i_{\text{in}}(t)\, \mathrm{d}t \tag{7.44}$$

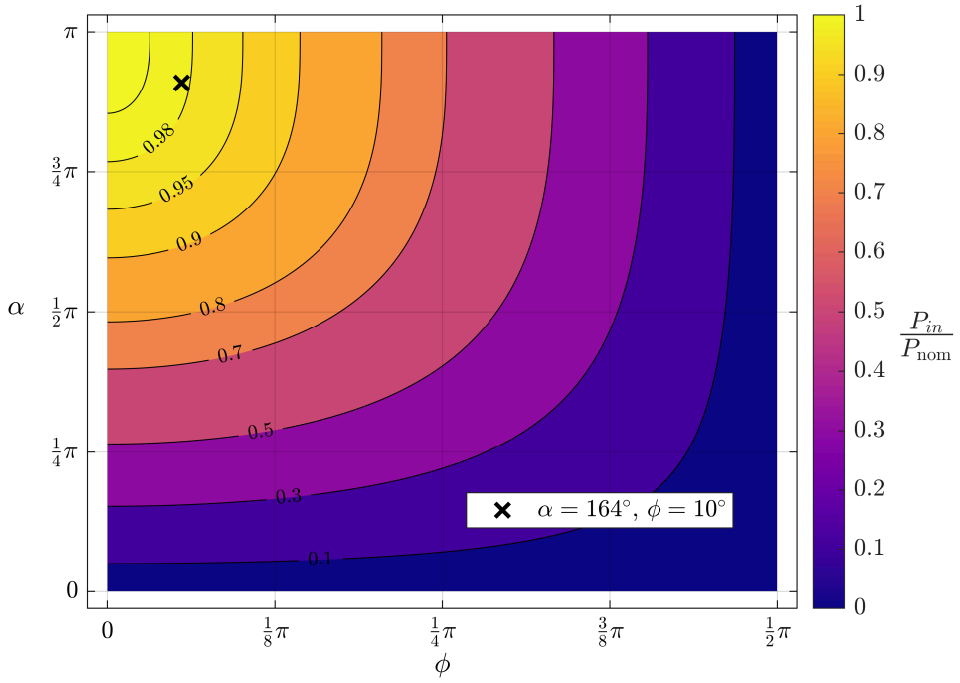


Figure 7.8: Relationship in (7.45) between nominal power throughput P_{nom} and real power throughput P_{in} for the truncated and phase displaced system.

For this system with truncated input current, P_{in} depends on the conduction angle α and the phase displacement ϕ of the system and can be reduced to

$$\begin{aligned} P_{\text{in}}(\alpha,\phi) &= \frac{1}{2}\,V_{\text{in}} \cdot \big(I_1 \cos(\phi_1)\big) \\ &= \frac{V_{\text{in}} I_{\text{in}}}{2} \cdot \frac{1}{\pi}\big(\alpha + \sin(\alpha)\big) \cdot \cos(\phi) \\ &= \frac{1}{\pi} P_{\text{nom}} \cdot \big(\alpha + \sin(\alpha)\big) \cdot \cos(\phi) \end{aligned} \tag{7.45}$$

by substituting (7.21), (7.27), and (7.43). This relationship between the nominal power throughput and real (or active) power throughput is further visualized in Fig. 7.8. The real power throughput $P_{\text{in}}(\alpha,\phi)$ is the value used to compute the IEC Class D harmonic limits, which are expressed in units of milliamp per watt. As the real power diminishes, the emission standards become more stringent per amp for all harmonics.

Defining the bounds of α and ϕ which achieve IEC compliance

In this section, I performed a large (and computationally slow) sweep of viable α and ϕ and determined where any harmonic failed IEC61000-3-2 Class D (for $P_{\text{in}} < 600$ W) and Class A (for $P_{\text{in}} > 600$ W) compliance. From observation of Fig. 7.9 for different nominal power P_{nom}, fascinating trends emerge: generally, the compliance region is roughly rectangular in the domain of α and ϕ. This 'boxy' phenomenon suggests a purposeful reasoning for the harmonic limits within IEC61000-3-2 beyond a simple inverse scaling with harmonic order n, but I could not find literature or resources related to the original formation of these standards. For Class D limits this compliant 'box' is fixed, but for Class A limits the compliance box shrinks in both α and ϕ yet still retains its roughly rectangular shape. Keep in mind that the Class A/D distinction of real power input P_{in} depends on the values of α and ϕ according to (7.45), thus for particular single choices of nominal power (e.g., 600 W $< P_{\text{nom}} \lessapprox 800$ W) there are Class A compliant, Class D compliant, and failing regions in the α, ϕ domain. Figure 7.10 is a consolidated version of all the subplots in Fig. 7.9 as P_{nom} varies.

Taking notice of the distinctly square shape of the compliance region as depicted in Fig. 7.12, a large sweep is performed across all P_{nom} to determine the approximate bounding box of the IEC compliance region. The results of this sweep are depicted in Fig. 7.11. The box approximation comes with the additional benefit of completely decoupled choice of compliant α and ϕ. From the numerical results a curve fit was formed to approximate a bounding $\alpha_b(P_{\text{nom}})$ and $\phi_b(P_{\text{nom}})$ which ensures IEC61000-3-2 compliance. These bounds are expressed as a simple function of the nominal power P_{nom}

The compliant bound α_b for the conduction angle α is

$$\alpha_b(P_{\text{nom}}) \approx \begin{cases} 1.762 & : \ P_{\text{nom}} < 600 \quad \text{(Class D)} \\ \dfrac{1.49 \cdot (P_{\text{nom}} - 600)}{(P_{\text{nom}} - 600) + 787} + 1.762 & : \ P_{\text{nom}} > 600 \quad \text{(Class A)} \end{cases} \tag{7.46}$$

and the compliant bound ϕ_b for the displacement angle ϕ is

$$\phi_b(P_{\text{nom}}) \approx \begin{cases} 0.625 & : \ P_{\text{nom}} < 600 \quad \text{(Class D)} \\ -\dfrac{0.705 \cdot (P_{\text{nom}} - 600)}{(P_{\text{nom}} - 600) + 1020} + 0.625 & : \ P_{\text{nom}} > 600 \quad \text{(Class A)} \end{cases} \tag{7.47}$$

These equations roughly fit the form of the empirical Monod equation, experimental Michaelis-Menten equation, or first-order Hill equation which are all used to describe the growth of micro-organisms in certain biochemistry applications.

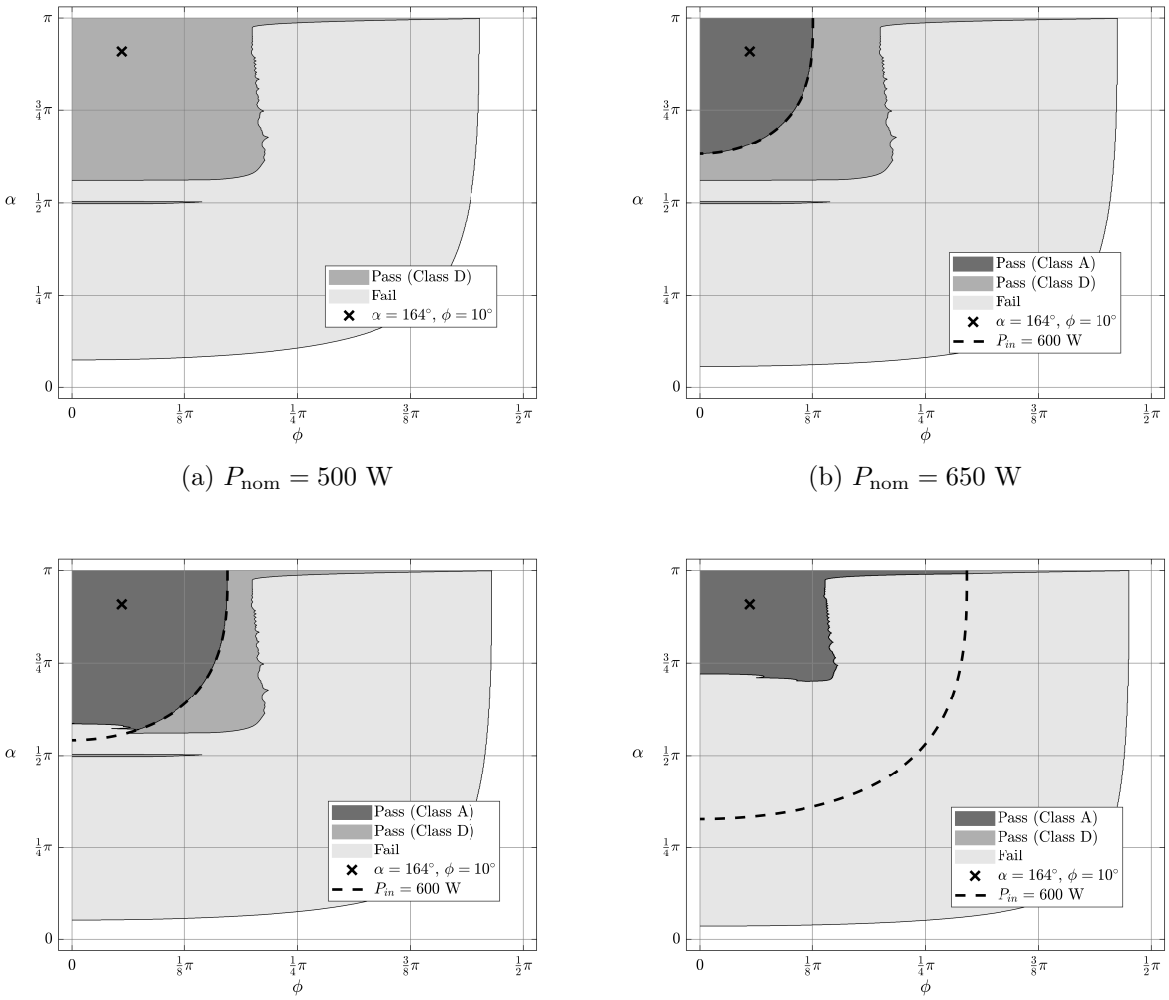
To pass IEC current harmonic emission standards [95] for the input current waveform shape (7.1), the conduction angle α and phase displacement ϕ should be chosen as

$$\pi \geq \alpha \geq \alpha_b(P_{\text{nom}}), \ 0 \leq |\phi| \leq \phi_b(P_{\text{nom}}) \tag{7.48}$$

at a specific nominal operating power P_{nom}.

Sufficient margin should be applied to these bounds in practice. The bounds are a simple approximation for the passing (compliant) region and may under- or over-estimate choices in α and ϕ which might actually belong to this region, both theoretically as shown in Fig. 7.12a or experimentally. Also note the PFC converter is incapable of perfectly generating the ideal truncated input current waveform in (7.1). Finally, an ac-side EMI filter can attenuate the higher order current emmision harmonics and expand the passing compliance region.

Solving (7.46) at the operating conditions of a 240 V_{rms} to 48 V PFC converter, the highest theoretically compliant power rating for the system is $P_{nom} \approx 2790$ W. At this power rating, the max/min tolerable phase displacement derived from (7.47) is $\phi \approx \pm 8.25°$.



(a) $P_{\text{nom}} = 500$ W

(b) $P_{\text{nom}} = 650$ W

(c) $P_{\text{nom}} = 700$ W

(d) $P_{\text{nom}} = 1000$ W

Figure 7.9: Theoretical pass/fail compliance regions of truncated input current according to IEC 61000-3-2 Class A and D equipment. Nominal rated power P_{nom} is varied to show the transition from Class D to Class A standards.

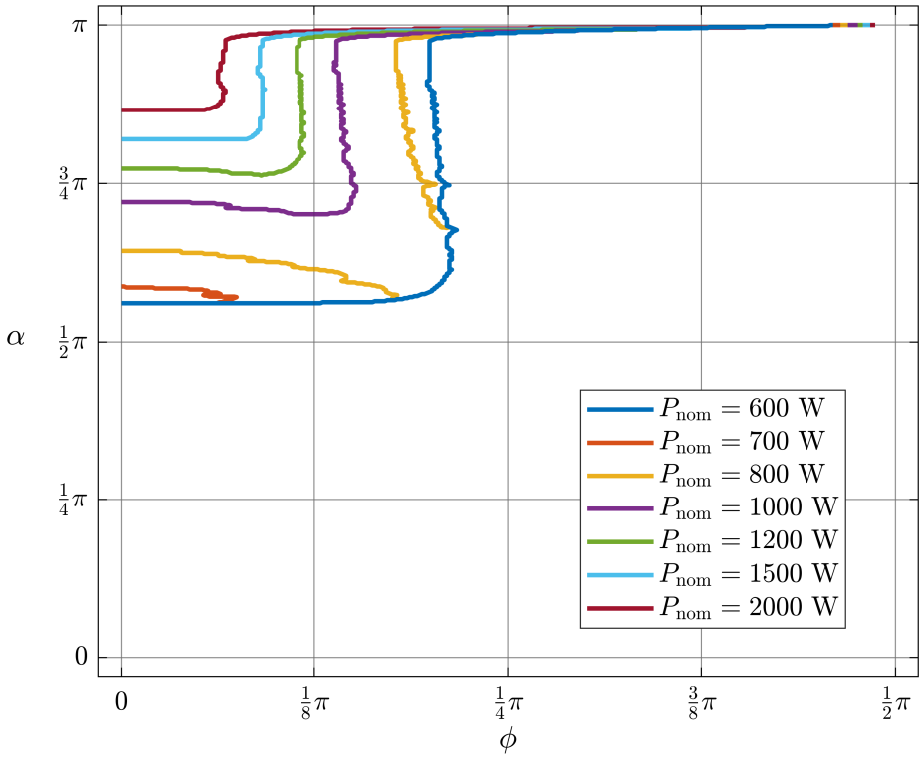


Figure 7.10: Aggregated theoretical pass/fail compliance regions of truncated input current according to IEC 61000-3-2 Class A and D equipment. Nominal rated power P_{nom} is varied to show the transition from Class D to Class A standards.

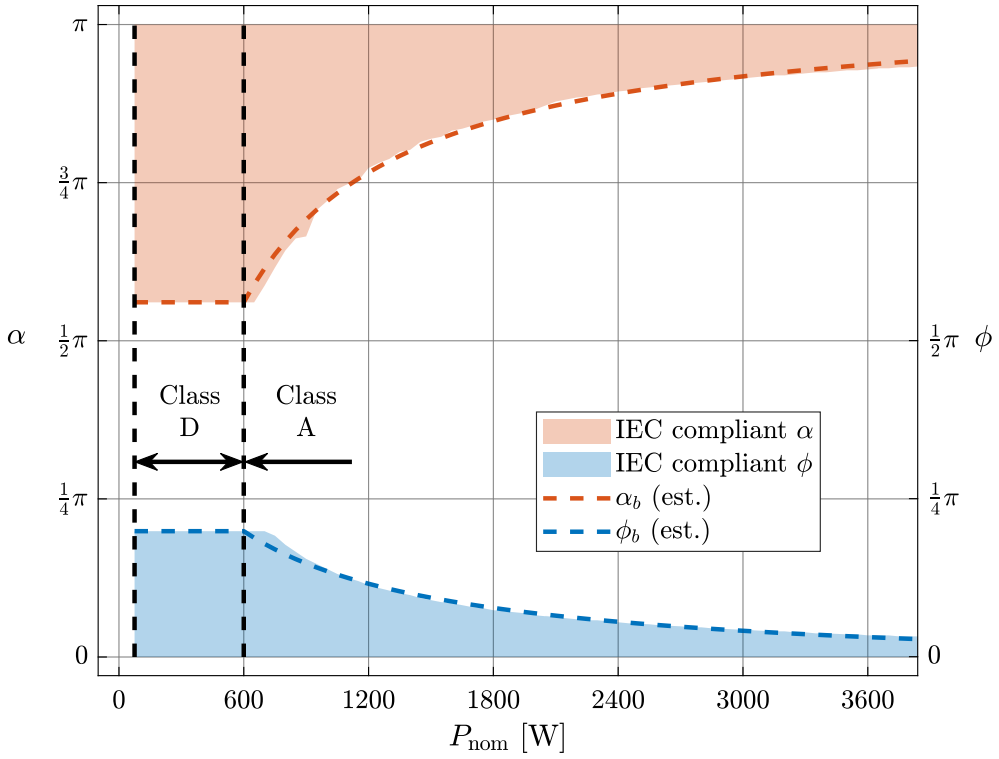
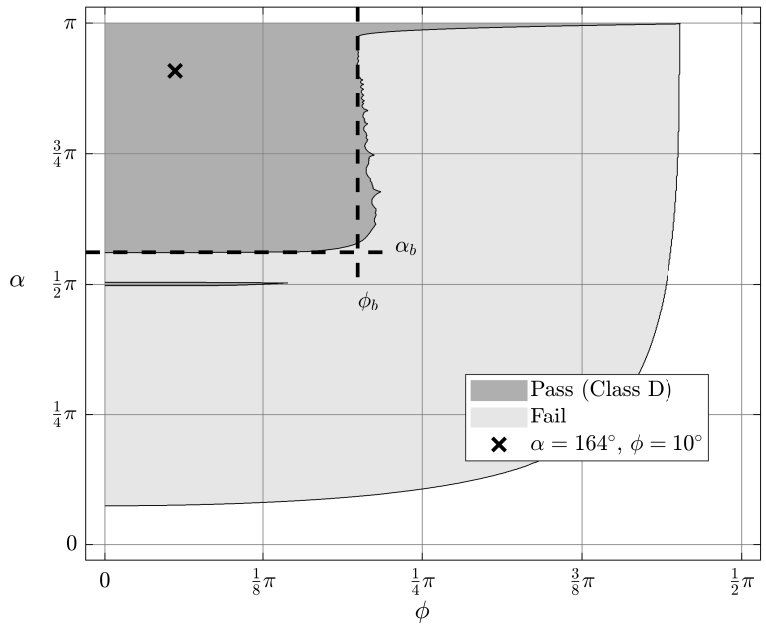
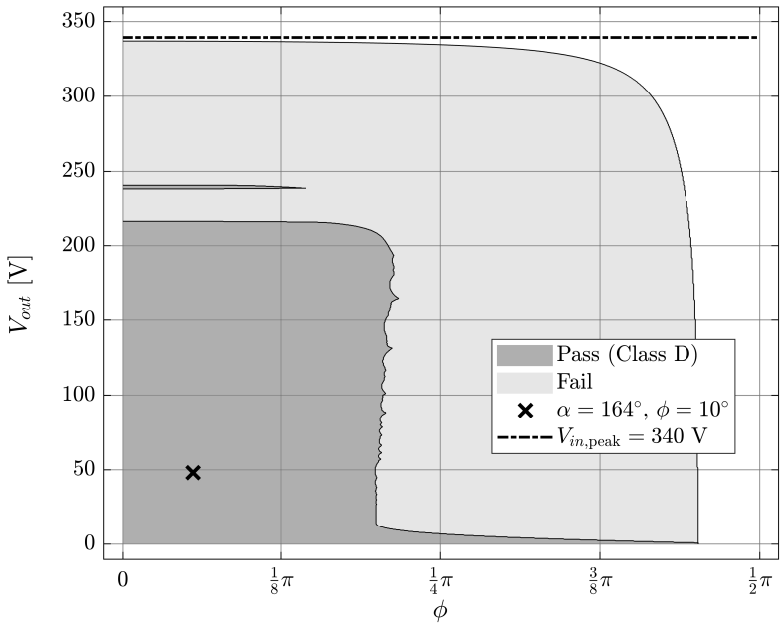


Figure 7.11: Theoretical pass/fail compliance bounds α and ϕ of IEC 61000-3-2 Class A and D equipment. Nominal rated power P_{nom} is varied.



(a)



(b)

Figure 7.12: Theoretical pass/fail compliance of truncated input current according to IEC 61000-3-2 Class D equipment (75 W $< P_{\text{in}} <$ 600 W) standard. $P_{\text{nom}} = 500$ W

7.5 Experimental Results

Input current measurements were performed on the FCML buck PFC in [30] and the measured harmonics are depicted in Fig. 7.14. Even though for this application (240 V_{rms} to 48 V) the value of $\alpha = 164°$ falls well within the theoretically IEC compliant bounds derived in the prior section, the realized current as seen in Fig. 7.13 barely passes compliance. Only the 11th, 15th, and 31st harmonics had less than a 50% margin, with the 11th harmonic being the most troublesome with a 7% margin. Also in the real measurement there are non-neglible frequency contributions at even harmonics whereas for the ideal derivations all even harmonics are null. Even harmonics imply an asymmetry between each half-cycle of the measured current waveform.

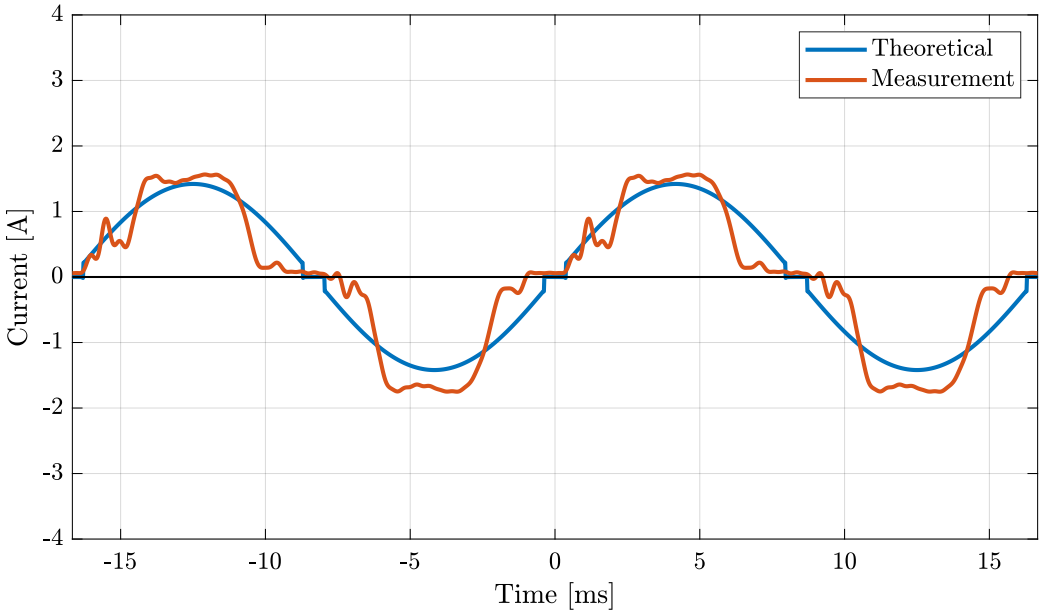
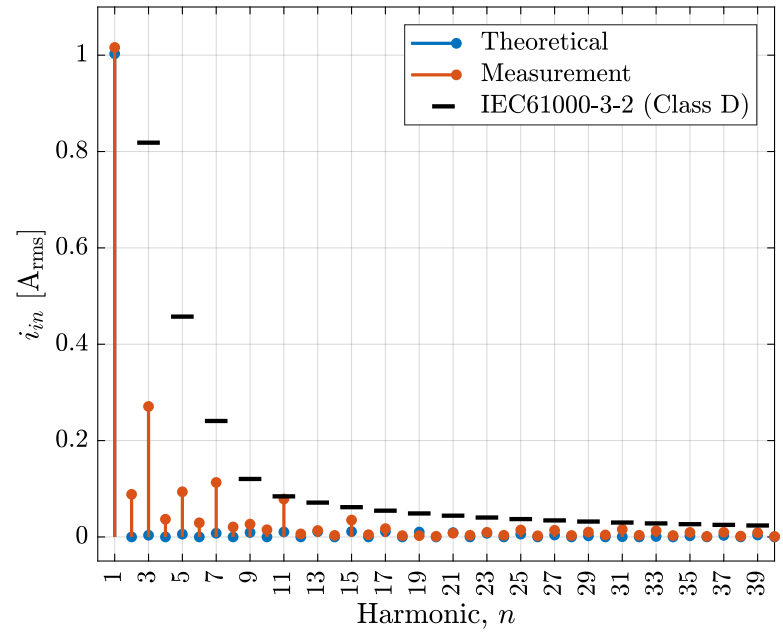
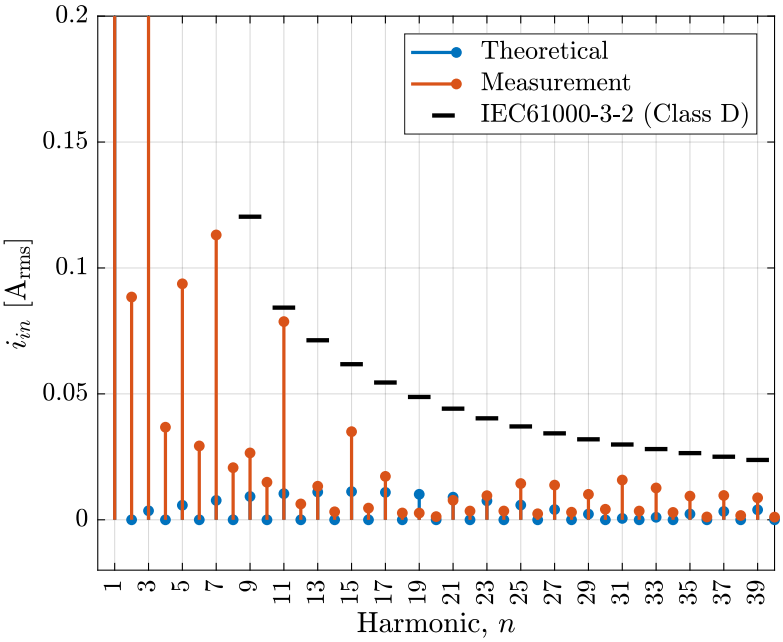


Figure 7.13: Comparison of theoretical and measured input current waveforms at P_{nom} = 216 W.



(a)



(b)

Figure 7.14: Theoretical and measured input current harmonic limits compared to IEC61000-3-2 (Class D) limits at $P_{\text{nom}} = 216$ W. (a) zoomed out and (b) zoomed in.

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