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Breakdown Voltage Mapping of Impurity Concentrations in GaAs Wafers

D.E. Bliss
(M.S. Thesis)

April 1988

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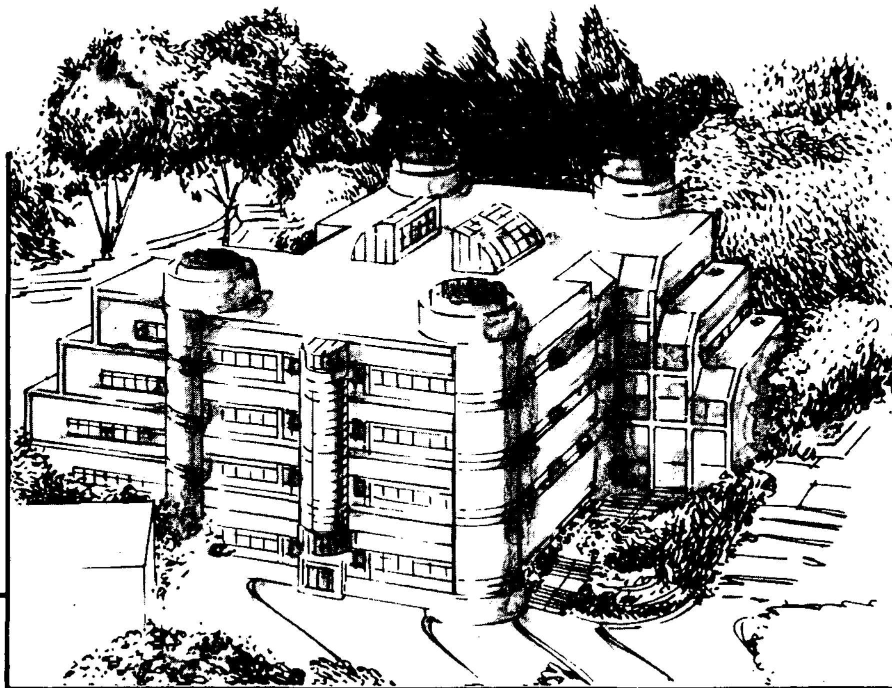

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Breakdown Voltage Mapping of Impurity Concentrations in GaAs Wafers

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Breakdown Voltage Mapping of Impurity Concentrations in GaAs Wafers

By

David Emory Bliss

April 6, 1988

Abstract

Using a modified x-y plotter, spatially resolved breakdown voltage measurements were obtained for a variety of GaAs materials. Breakdown voltage values were calibrated against net impurity concentration using C-V measurements. Spatially resolved Hall effect measurements on GaAs doped with Si correlated well with a breakdown voltage map of the impurity concentration. The technique provides a quick means for determining doping uniformity in epitaxial films and implanted layers as well as dopant incorporation rates in bulk crystals. An inverse correlation between etch pit density and breakdown voltage is shown for LEC wafers.

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Chapter 1

Introduction

Interest in GaAs as a material for integrated circuits has increased tremendously over the past several years. GaAs offers two fundamental advantages over silicon as a substrate material for integrated circuits: 1. GaAs has a higher electron mobility than silicon, 8500 $cm^2V^{-1}s^{-1}$ versus 1500 $cm^2V^{-1}s^{-1}$ at room temperature [1]. 2. GaAs is a direct band gap material with a band gap larger than Si, 1.43 eV versus 1.10 eV. In terms of device performance, higher electron mobility means electrons can travel faster for a given electric field. Even though the saturation velocity of electrons at high fields is comparable for both GaAs and silicon, GaAs has the interesting property of having a higher maximum electron velocity at fields lower than 4 kV cm^{-1} than at saturation. The resulting negative resistance region is the basis for Gunn oscillators [2]. The higher maximum velocity reduces the transit time of electrons through the channel of a GaAs transistor decreasing the switching time. The high resistivity of semi-insulating (SI) GaAs reduces stray capacitance also increasing device speeds. Presently, TTL and ECL compatible 4 kbit random access memories (RAM) made of GaAs have 3-4 ns access times compared to 7-10 ns for the silicon counterparts. For a complete GaAs system that did not need TTL compatible drivers, access times could be reduced by 2 ns [3]. The second advantage, the direct band gap of 1.43 eV, is not as obvious an advantage for GaAs integrated circuits. The larger band gap

allows GaAs devices to operate at higher temperatures without being flooded by intrinsic carriers. Being a direct band gap material, GaAs can readily absorb and emit photons with an energy equal to the band gap. With the strong push today for fiber optic communications, an optically active GaAs integrated circuit would be an ideal interface between optics and electronics [4].

The implication is not that GaAs would ever replace silicon technology, but rather complement it, performing tasks that silicon could not. GaAs has many material problems which counteract its advantages in speed over Si. GaAs being a compound semiconductor made up of alternating gallium and arsenic atoms on a diamond cubic lattice, has the possibility for many more kinds native defects than silicon. GaAs does not form a stable native oxide either. Any dielectric layer required for device functions or protection needs to be deposited and even these are notorious for poor quality and pinholes. And finally, worth mentioning as a disadvantage, is the high vapor pressure of arsenic. High temperature annealing processes such as post ion implantation activation result in the dissociation of GaAs into gallium and arsenic. Precautions must be taken to minimize arsenic loss. GaAs is expensive and has many more materials problems than Si. Even though GaAs has a higher mobility than Si, interest in it would not have been sustained if it were not for the fact that a whole range of III-V compounds can be combined.

A wealth of novel optical and electrical devices are being designed and fabricated based on heterojunctions of different III-V compounds and their ternary alloys. The principle of III-V device design is not only to control the placement and concentration of dopants, as in Si IC design, but to also spatially control the magnitude of the energy gap. The term "Band gap engineering" applies well. Some "Band gap engineered" devices which show promise are

1. Heterojunction lasers [5]

2. Graded bandgap multilayer avalanche photodiodes (APD) [6]

3. High electron mobility transistors (HEMTS) [7,8]

4. Heterojunction bipolar transistors [9]

These are just a few examples of the many devices being conceived of.

The ideas for some of these heterostucture devices are not new. Many were already patented in the 1960's [10]. Material and processing problems limited their development. It was not until the late 1970's and early 1980's with the perfection of high purity thin film epitaxial techniques that reliable devices could be made. Organometallic vapor phase epitaxy (OMVPE) [11], liquid phase epitaxy (LPE) [12], and molecular beam epitaxy (MBE) [13], methods can grow high purity epitaxial layers with thickness control for MBE and OMVPE on the order of a monolayer.

Problems with devices have shifted away from the purity of the layers to intrinsic defect effects. Understanding of the stability and thermodynamics of native defects is needed. Intrinsic native defects result from misplaced or missing atoms in the structure of the crystal. For compound semiconductors, the number of possible defects is much greater than for elemental semiconductors like germanium and silicon. Defects can occur on both the III and V sublattices, as well as antisite defects where an atom is found on the wrong sublattice. For silicon the simple point defects would be the vacancy, V_{Si}, and the interstitial, Si_I. For GaAs, the native point defects are, on the arsenic sublattice, V_{As} and Ga_{As}, on the gallium sublattice, V_{Ga} and As_{Ga}, and the interstitials, As_I^{TD1}, As_I^{TD2}, Ga_I^{TD1}, Ga_I^{TD2}, where TD1 (TD2) is the tetrahedral interstitial site surrounded by As (Ga) atoms. Where there were only two intrinsic point defects in elemental semiconductors, compound semiconductors have eight to form many possible defect combinations.

Native defects can affect the material in a variety of ways. Either by forming electrically active levels directly which degrade the electrical performance or by enhancing the diffusion of other atoms degrading the structure of the device. Examples of native defect effects in GaAs are,

1. Fermi level pinning of irradiated material
2. Reversible type conversion of SI GaAs upon annealing
3. Ion implan tion efficiency
4. Impurity enhanced superlattice mixing
5. Schottky barrier height pinning.

Experimentally verifying the electrical properties of native defects is difficult. No direct electrical experimental identification for native defects exists except for the As_{Ga} antisite [14]. Using electron paramagnetic resonance (EPR) measurements Wagner et. al. identified the characteristic four line spectrum as being due to As_{Ga}^{+}. The physical presence of vacancies in GaAs has been identified by positron annihilation studies [15], but the electrical levels are unknown.

Without direct observation of most native defects, concentrations must be inferred from thermodynamic considerations. The Gibbs free energy changes of defect reactions which establish equilibrium are calculated theoretically [16]. Restrictive assumptions to simplify and make the calculation possible limit the confidence one can place on calculated energies to ±200 meV [17].

Using the calculated energies, one can apply dilute solution thermodynamics to the defects since they exist in small concentrations. For defects in equilibrium, one can write a chemical reaction type of equation,

$$N_A A + N_B B \rightleftharpoons N_C C N_D D \qquad (1.1)$$

where N_x is the concentration of species $x = A, B, C, D$. The mass action relation relating the equilibrium concentrations of the species to the total change in free energy is

$$\frac{[C]^{N_C}[D]^{N_D}}{[A]^{N_A}[B]^{N_B}} = K = \exp - \frac{\Delta G}{kT} \tag{1.2}$$

where K is the equilibrium constant and ΔG is the change in Gibbs free energy for the defect reaction. For GaAs grown under an As overpressure as is the case for undoped SI GaAs, a defect reaction which establishes equilibrium between the native defects associated with excess As is,

$$As_I + V_{Ga} \rightleftharpoons As_{Ga} \tag{1.3}$$

and the mass action relation is

$$\frac{[As_{Ga}]}{[As_I][V_{Ga}]} = \exp\left[-\frac{\Delta G(E_F)}{kT}\right] \tag{1.4}$$

The change in Gibbs free energy depends on the Fermi energy and the Fermi energy is determined by what defects and impurities are present. It is this dependence of the equilibrium constant on the Fermi level that is responsible for some of the defect effects reported, such as Si enhanced interdiffusion in AlGaAs superlattices [18]. The Si on Ga sites raises the Fermi energy near the conduction band, driving the reaction in the direction of forming more V_{Ga}. The vacancies enhance the diffusion of the group III elements destroying the sharp interfaces of the superlattice.

This effect is similar to the suppression of the formation of EL2 by excess free electrons [19]. EL2 is the prominent deep level defect responsible for compensating undoped SI GaAs. Much experimental evidence links EL2 to As_{Ga}, the arsenic antisite defect, but the exact structure of the EL2 defect has yet to be determined. EL2 is found in GaAs grown under As rich conditions [19]. EPR experiments find As_{Ga} and EL2 in the same abundances, $2 - 10 \times 10^{15}$ cm^{-3} with similar energy levels and photoquenching properties [20]. Lagowski reported the

concentration of EL2 could be reduced in bulk crystals by doping with group IV or group VI donors. An increase in the free carrier concentration corresponds to raising the Fermi energy closer to the conduction band. As mentioned before this tends to drive reaction 1.3 to the left, suppressing the formation of antisites. Since EL2 is associated with As_{Ga} it is suppressed also. Thus we see native defects influence the properties of GaAs strongly.

To elaborate more on SI GaAs, it is technologically important as a substrate material since it provides for the isolation of devices. Typical resistivity for SI GaAs is greater than 10^6 Ωcm, while semiconducting (SC) GaAs might have resistivities less than 1 Ωcm. The difference in resistivities is due purely to the position of the Fermi energy; at midgap for SI material and near the conduction or valence band for SC GaAs. Practically, it is impossible to produce GaAs which is intrinsic at room temperature since the number of intrinsic carriers is so low, $n_i(300K) = 10^7$ cm^{-3}. To make a material of this purity, only 1 in 10^{15} atoms could be an impurity. Instead, to produce SI GaAs, the Fermi energy must be "pinned" at midgap by a deep level [21].

To review the history of the development of SI GaAs, in the sixties, SI GaAs was produced by oxygen doping [22] of Horizontal Bridgman (HB) material and by floating zone techniques [23]. Although both techniques were successful at producing SI material they were not reproducible. The next development which started in 1964, made use of the Czochralski (CZ) crystal growth technique and Cr doping [24]. Problems with the rapid diffusion of Cr make the material unsuitable as a substrate for integrated circuits, although it is still in use for the fabrication of discrete optoelectronic devices.

During the late 1970's and early 1980's it became understood how to reliably produce "undoped" SI GaAs which contained no intentionally introduced transition metal impurity to act as a deep level compensator. Martin et. al.

[25] identified EL2 as the native deep level donor compensating excess acceptors and pinning the Fermi level at midgap. EL2 compensation works to produce SI GaAs if the total donor concentration exceeds the total acceptor concentration, and the shallow acceptor concentration exceeds the shallow donor concentration.

$$N_{EL2} + N_{SD} > N_{SA} \tag{1.5}$$

$$N_{SA} > N_{SD} \tag{1.6}$$

where N_{SA} and N_{SD} are the shallow acceptor and donor concentrations. Precautions must be taken during growth to keep the Si contamination below the total acceptor concentration to maintain this SI compensation scheme. One solution is growing from a pyrolitic boron nitride crucible. Holmes [26] found that the EL2 concentration could be varied by controlling the As fraction in the melt. For As fractions greater than .475, a sufficiently high concentration of EL2 was produced to generate SI material. Ta et. al. [27] showed further that SI substrate material could be made more stable to annealing treatments by increasing the As content of the melt.

To produce usable SI substrates, one can not simply grow with high As content. The spatial inhomogeneity of electrical properties across a liquid encapsulated Czochralski (LEC) GaAs wafer is a problem not found with Si or Ge. Uniform properties are critical for the reliable performance of direct implantation fabricated GaAs IC's [28]. Thus, there is a need to measure the spatially resolved electrical and structural characteristics of the substrate. Bulk electrical characterization techniques which can be adapted to very small volumes are given below with a minimum lateral resolution,

1. Cathode luminescence, 5 μm [29]

2. Infrared absorption and spectrometry, 50 μm [30,31]

3. Scanning DLTS, 2 μm [32]

4. Photoluminescence, 10 μm [33]

5. Hall effect, 1 mm [34].

6. Leakage current, 200 μm [35]

7. Dark spot resistivity, 5 mm [36]

Techniques which characterize the structural properties are

1. Preferential etching of dislocations, 10 μm [37]

2. Secondary ion mass spectrometry (SIMS), 10 μm [38]

3. Transmission electron microscopy (TEM), 2 Å

4. X-ray topography, 50 μm [39].

Some of these techniques lend themselves better to spatially resolved studies due to sample preparation being less invasive and destructive.

It is extremely important when doing spatially resolved measurements to combine techniques to get complimentary information on the concentration and charge state of important electrical levels. One measurement might show that the concentration of a particular charge state of a defect is spatially varying. Without other measurements one does not know if the fluctuation is due to changes in the concentration of that defect or due to changes in a compensating level. For instance, the distribution of EL2 was analyzed using IR absorption at 1 and 2 μm [40,25] and a W shaped pattern across an undoped LEC wafer was reported. However, the IR technique used, only detects neutral $EL2^{\circ}$ and not $EL2^{+}$. Electron paramagnetic resonance (EPR) studies could detect the $EL2^{+}$ concentration but not spatially resolved. Recent evidence reported by Walukiewicz et. al. [41] shows that the total EL2 concentration remains roughly

constant across an undoped LEC wafer and the variation in the EL2° is due to concentration fluctuations of donors shallower than EL2.

Although combinations of these techniques yield important information about the physical properties of the substrate, ultimately it is the successful performance of optical or electrical devices that determines what a useful substrate is. Thus it is important that measurement techniques be non-destructive so that device performance parameters can be correlated against material properties on the same substrate.

Miyazawa et. al. [42] investigated the uniformity of FET device performance fabricated on a variety of SI GaAs substrates. The threshold voltage V_{th} and drain source current, I_{ds}, were measured and compared to the proximity of dislocations to the device. The existence of a dislocation was determined by a molten KOH etch. A drop in V_{th} up to .3 V correlated with the presence of a dislocation. Winston et. al. repeated the experiment and found no correlation between dislocations and lower FET threshold voltages. These results are not as entirely contradictory as they might appear. Dobrilla and Blakemore [43] report a correlation between neutral EL2 and V_{th}, with V_{th} increasing from .6 to .8 V as the EL2 concentration increases from 2 to 9×10^{15} cm^{-3}. It is known from infrared imaging [30] and low temperature photoluminescence [33] that EL2 concentrations can be higher in a 100 μm diameter area around dislocations in as grown LEC material. Furthermore, Holmes [26] has shown that EL2 distributions can be homogenized by long term anneals at 900°C. If the wafers used by Winston were thermally treated or subjected to a long post growth cooldown, decoupling the concentration of neutral EL2 from dislocations, then the discrepancy in the results is resolved. This example stresses the importance of knowing the history of experimental samples and combining complementary techniques for a complete characterization.

In the process of combining techniques, one needs quick, rough estimate measurements to provide a focused approach to applying more careful, detailed measurements. Spatially resolved breakdown voltage (SRBV) measurements which are the focus of this work, are a simple technique which can improve the overall efficiency of the characterization process. For semiconducting samples, SRBV measurements provide quick and simple information on carrier type, concentration and distribution. Four point probe measurements which are used commonly on silicon to determine resistivity and implant doses do not work satisfactorily on wide band gap III-V materials. The metal probes form Schottky diodes instead of the needed ohmic contacts. Why not use the Schottky barrier to characterize the material? It saves the effort of preparing samples for Hall effect measurements which are typically used for determining carrier concentration. SRBV measurements give the crystal grower who is developing a growth method a fast characterization tool to reduce the turnaround time between crystal growth runs. SRBV could help minimize the time it takes to characterize epitaxial films while getting an OMVPE or MBE system working.

In the following sections I will discuss the physics of reverse bias diode breakdown as it applies to the measurement. The basic design and operation of the instrument will be outlined. I will analyze the performance of the instrument in terms of measurement range, sources and magnitudes of error, and spatial resolution. Results will be presented and analyzed for Liquid Encapsulated Czochralski (LEC) and Horizontal Bridgman (HB) crystals and AlGaAs epitaxial layers. And finally commercial applications and future research with the instrument will be discussed.

Chapter 2

Physics of Schottky Contacts

A rectifying metal-semiconductor junction is often named after W. Schottky who first proposed a model for the barrier formation in 1938 [44]. The discovery of metal-semiconductor diodes dates back more than a century to F. Braun [45] who in 1874 reported the rectifying properties of metal contacts on Copper-, Iron- and Lead Sulfide crystals.

For the breakdown voltage mapping, the main aspects of a rectifying Schottky contact can de described using the simple model first proposed by Mott and Schottky. It ignores surface states and other effects, considering only a metal and semiconductor with a depletion region devoid of mobile carriers. When a semiconductor and a metal are brought into contact under thermal equilibrium the Fermi levels of the two materials must coincide at the interface and be constant throughout both materials. For the case of a metal and n-type semiconductor as shown in Figure 2.1, upon contact, electrons must flow from the conduction band of the semiconductor to the metal to lower the Fermi energy in the semiconductor. The Fermi level in the semiconductor must be lowered by the difference between the two work functions. The work function is defined as the amount of energy needed to lift an electron from the Fermi level to the vacuum level. The vacuum level is the energy of an electron outside the metal or semiconductor with zero kinetic energy. The electron affinity is the energy needed to raise an

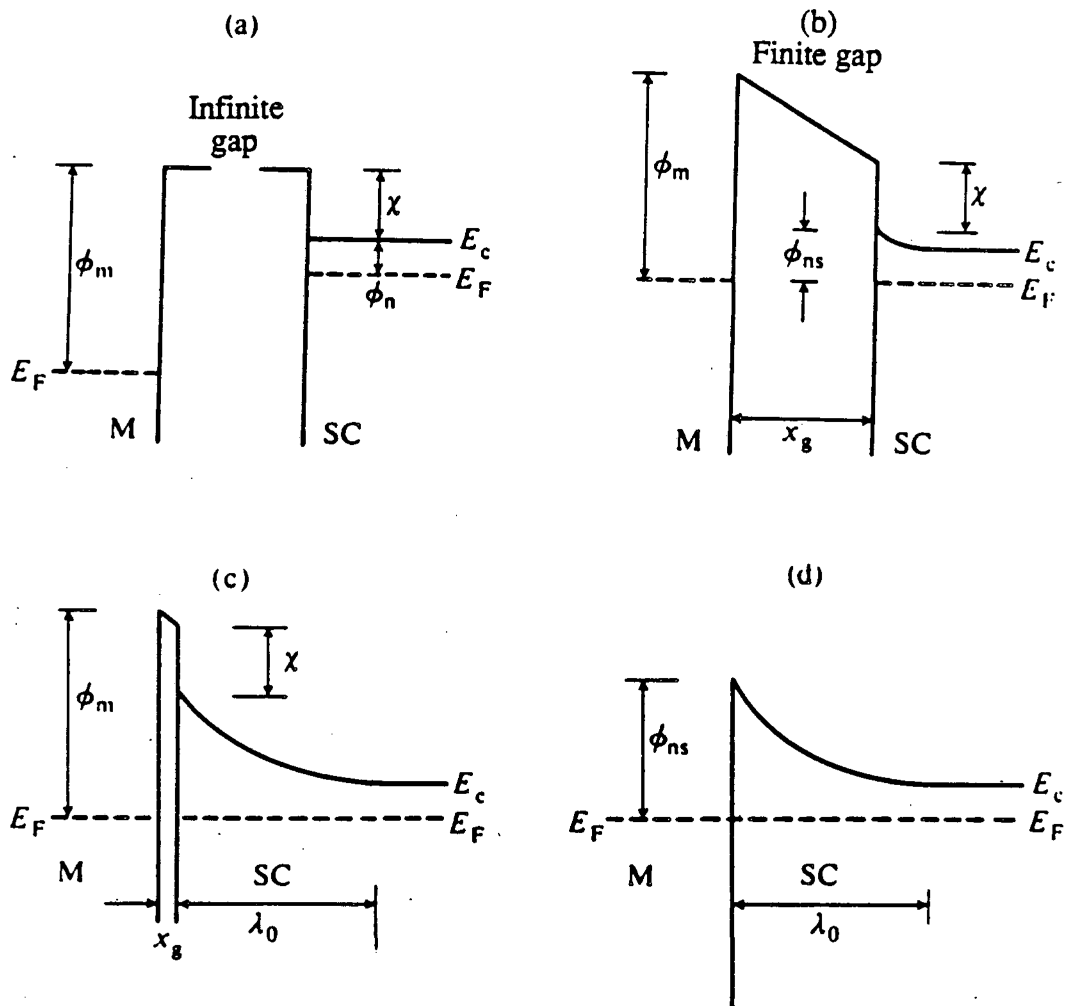


Figure 2.1: Contact barriers due to work function differences. ϕ_m = thermionic workfunction of metal M. χ =electron affinity of semiconductor SC. E_g =band gap.(Reference [46])

electron from the conduction band to the vacuum level. As the electrons flow out of the semiconductor near the boundary region they collect on the surface of the metal. An equal and opposite amount of fixed positive charge remains in the semiconductor due to the ionized donor atoms. This boundary area, devoid of free carriers, is known as the depletion region. The width of the depletion region on the semiconductor side is significantly greater than in the metal due to the relatively low concentration of donor atoms compared to the concentration of electrons in the metal. The depletion width can be approximately one micron for moderately doped GaAs while the Debye length which characterizes the thickness of the electron layer at surface of the metal is approximately 5 Angstroms.

To determine the barrier height, an important reference to start with is the vacuum level. It must remain continuous across the interface. The total band structure is the superposition of the inherent crystal bands and the coulomb field produced by the space charge. If we assume the space charge does not perturb the positions of the the atoms in the solid, then the relative spacing of energy bands remains unchanged so the electron affinity and bandgap are constant throughout. As the two materials are brought into contact and the Fermi levels equilibrate, the amount of bandbending is the same for the valence band, conduction band and vacuum level. Since both Fermi levels coincide at equilibrium, the amount of bandbending of the vacuum level for an ideal semiconductor is simply

$$\phi_m - \phi_{sc} = qV_{bi} \tag{2.1}$$

where ϕ_m, ϕsc are the respective metal and semiconductor work functions and V_{bi} is the *b*uilt *i*n potential or contact potential and is expressed in volts. For a real metal-semiconductor junction the Fermi energy is pinned at the surface so that the barrier height is determined by the interface states. The contact potential is the barrier an electron must surmount in traveling from the metal

to the semiconductor conduction band and is independent of bias. The barrier an electron must overcome moving from the semiconductor to metal depends on bias. Referring to the band diagram, Figure 2.2, that barrier is

$$\phi_B = \phi_{bi} - qV_{app} \tag{2.2}$$

where V_{app} is the applied forward bias.

When considering the current transport properties of the metal semiconductor contact it can be shown that it is a rectifying contact when $\phi_m > \phi_{sc}$. Figure 2.2 shows the four basic mechanisms affecting current transport under forward bias.

1. Thermionic emission
2. Tunneling
3. Recombination
4. Hole Injection

For reverse bias the current mechanisms are the same, but in the opposite direction and the magnitudes will differ. In moderately doped semiconductors (10^{14}–$10^{17} cm^{-3}$) where breakdown voltages can be measured, the predominant transport mechanism across the barrier is thermionic emission as proposed by Bethe [47]. When a bias voltage is applied the amount of current that flows is determined by the number of carriers with sufficient energy to overcome the potential barrier. The difference in the nature of the barrier in going from metal to semiconductor and vice versa is responsible for the rectifying nature. First consider equilibrium (see Figure 2.1). The rate at which carriers cross over the barrier from metal to semiconductor just equals the rate in the opposite direction. Thus no net current flows. When the diode is forward biased the Fermi level of the semiconductor is raised relative to the metal, effectively lowering the barrier from the semiconductor to metal causing an increase in the number of electrons

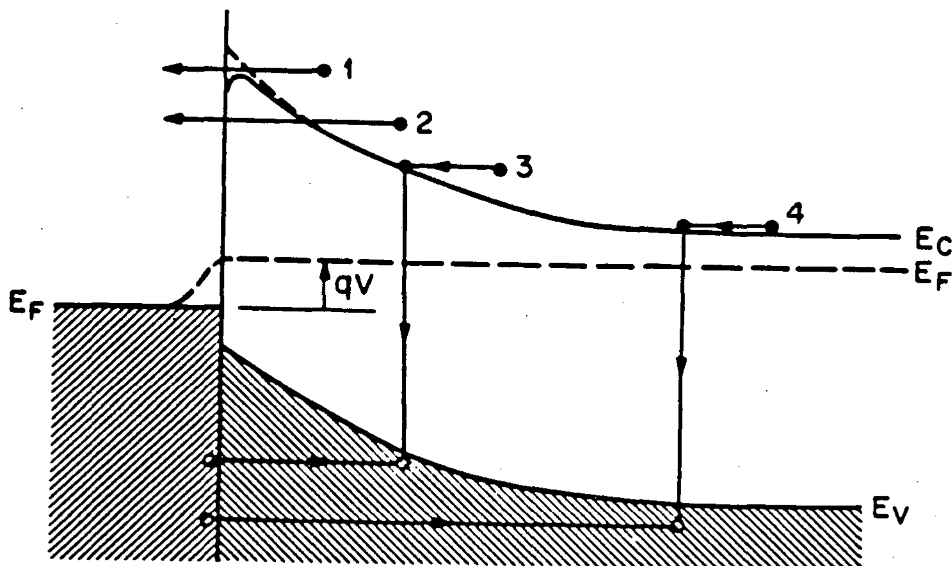


Figure 2.2: Four basic current transport mechanisms across a Schottky diode on an n-type semiconductor under forward bias.

flowing from semiconductor to metal. The barrier from metal to semiconductor however remains unchanged so there is no change in current in that direction. The result is a net flow of current from semiconductor to metal. This current can be quite large since further increase in the forward bias continues to lower the barrier.

When reverse bias is applied, the Fermi level of the semiconductor is lowered with respect to the metal. Again, the barrier height from metal to semiconductor is unaffected so that the same amount of electrons flow from metal to semiconductor and the same amount of minority holes flow from semiconductor to metal as in equilibrium. The barrier height from semiconductor to metal is increased cutting off the flow of electrons from semiconductor to metal while not affecting the hole current. Hence, the net current which flows in reverse bias is equal to the equilibrium flow from the metal to semiconductor. It is commonly called the saturation current and is constant for increasing reverse bias until some other

mechanism for current flow dominates such as tunneling or avalanche breakdown.

When the reverse bias is increased, a value is reached at which the current increases suddenly. This sharp current increase signals breakdown. For heavily doped GaAs, N_D or $N_A \geq 10^{17} cm^{-3}$, tunneling is responsible for breakdown. The high doping gives a high space charge concentration resulting in a narrow depletion width which electrons can tunnel through. Breakdown voltage values for tunneling are below approximately $6E_g/q$ [2] V. This corresponds to breakdown voltages below 9 V for GaAs. For tunneling breakdown, the breakdown voltage is insensitive to doping concentration. Further slight increases in doping drastically increase the tunneling probability, rapidly dropping the voltage to zero setting an upper limit for the determination of concentrations. For breakdown voltages above $6E_g/q$ avalanche multiplication of electrons and holes is the dominant mechanism responsible for breakdown. It is this type of breakdown that we are interested in exploiting to measure the net doping concentration.

Impact ionization of valence electrons by an incident carrier is the microscopic mechanism for generating an avalanche breakdown. If a carrier is accelerated to a sufficient velocity, it can transfer kinetic energy inelastically, generating an electron hole pair upon impact with a valence electron. This occurs if the field is high enough so that the carrier is accelerated to sufficient energy between collisions. Schottky showed that the field in a Schottky barrier is made up of two components, one due to space charge, and one due to image force. The total electric field in the presence of a reverse bias is as a function of the distance from the metal-semiconductor interface, x:

$$\mathcal{E}(x) = \frac{e}{16\pi\epsilon_\infty x^2} + \frac{N_D q}{\epsilon}(x - \omega) \tag{2.3}$$

where ϵ_∞ and ϵ are the high frequency and d. c. dielectric constants respectively. The high frequency dielectric constant is used for the image charge field since the electron (or hole) spends little time near the interface and the semiconductor

does not have enough time to become polarized. The maximum field occurs at $x_m^3 = \epsilon / 8\pi N_d \epsilon_\infty$. The complications of image force lowering of the barrier and high frequency dielectric constants do not change the fact that the maximum field occurs very close to the interface. The field decreases linearly through the semiconductor from the maximum value at x_m to zero at the depletion boundary, $x = \omega$.

We can define an ionizing energy, E_i, such that a carrier with kinetic energy $E > E_i$ will induce an ionizing event. For kinetic energies below E_i, the energy transferred when a carrier is scattered can be dissipated as phonons in the lattice. As the field is increased the carriers become 'hot', which means that their drift kinetic energy is greater than their average thermal energy of $\frac{3}{2}kT$, or 25 meV at room temperature, and then 'very hot' when the kinetic energy is greater than the band gap energy. For these 'very hot' carriers with kinetic energy greater than E_i, scattering events can now generate electron-hole pairs across the bandgap. The energy required to generate an electron-hole pair must be greater than the bandgap.

To sustain breakdown of the junction, the field must exceed the ionizing field not just at the maximum field, but over several *mean free paths* into the depletion region. Avalanche breakdown is the multiplication of free carriers and these carriers need to be built up over some distance. Consider again an n-type semiconductor-metal contact in reverse bias with a single electron entering the depletion region via thermionic emission over the barrier (see Figure 2.3). Along path 1 the electron is accelerated becoming a 'hot' carrier. The electron's elevated energy is indicated by its path leaving the band edge. It should be noted that the real space band diagrams show just the band minimum of an E vs. k diagram. As the electron acquires energy in the electric field, it moves away from the minimum in the E vs. k plot hence moving away from the band edge

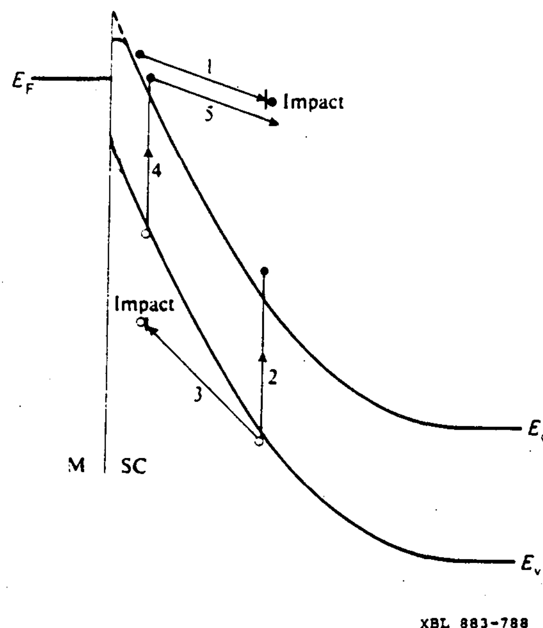


Figure 2.3: Band diagram of a metal-semiconductor interface depicting the mechanism for impact ionization avalanche breakdown. (1) Electron acceleration (2) Generation of an electron hole pair on impact (3) Acceleration of new hole to impact.

in the real space diagram. After traversing a mean free path the 'hot' electron impacts a valence electron generating an electron hole pair, event 2. The new electron and hole are accelerated in opposite directions and can both generate new electron hole pairs, as can the original electron. The hole is accelerated along path 3, impacting a valence electron generating an electron hole pair, event 4. This process of acceleration, impact, and generation repeats itself resulting in a rapid build up of both types of free carriers.

One might be concerned by how a hole, which is the lack of an electron, could cause an ionizing event. One might suspect that only electrons, which have a real mass, could initiate an impact ionization event. However, holes do have charge and can acquire kinetic energy up to the width of the valence band which is 3 eV in GaAs. It will be shown in Equation 2.12 that a rough estimate for the energy required to generate an electron hole pair is $\frac{3}{2}E_g$ which for GaAs is 2.2

eV. Therefore it is actually conceivable that a hole could create an electron hole pair through impact ionization.

The basic dependence of the ionization rate on the applied voltage and hence the dependence of the breakdown voltage on doping concentration can be illustrated using a simplified model by Sze [48]. The ionization rate, α_p or α_n is defined as the number of electron-hole pairs generated per unit length by a moving hole or electron respectively and has units of inverse length.. Given a mean free path, ℓ_s, for free carrier scattering, the probability a carrier travels a distance ℓ without collision is

$$n(\ell) = n_o e^{\frac{-\ell}{\ell_s}} \tag{2.4}$$

In an applied field $\mathcal{E}$, the amount of energy E, acquired by an electron traversing a length ℓ is

$$E = q\mathcal{E}\ell \tag{2.5}$$

Substituting this expression for ℓ in Equation 2.4 gives an expression for the number of electrons acquiring an energy E.

$$n(E) = n_o e^{\frac{-E}{q\mathcal{E}\ell_s}} \tag{2.6}$$

When $E = E_i$ Equation 2.6 gives the probability for an electron to cause an ionizing event. The number of electrons causing ionizing events is proportional to the ionization rate α_i so when the electric field, $\mathcal{E}(x)$ is a function of depth, we can write

$$\alpha_i(x) = \alpha_{io} exp\left[\frac{-E_i}{q\ell_s\mathcal{E}(x)}\right] \tag{2.7}$$

Equation 2.7 is valid when the average electron energy is much less than E_i. This is a restrictive assumption, and not quite true [49]. The average electron energy is not much less than E_i at breakdown, But the main point is that the ionization rate is a strong function of the electric field.

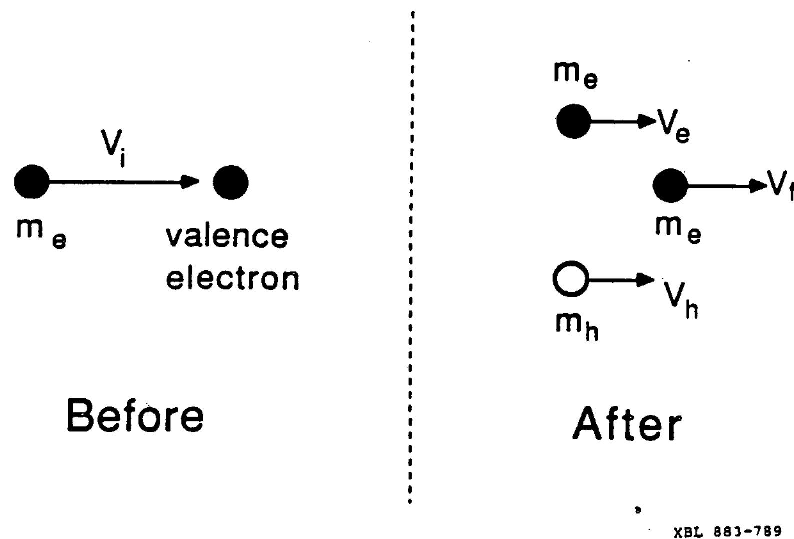


Figure 2.4: Impact ionization event for maximum energy transfer by an incident electron.

A good order of magnitude estimate for an upper limit on the minimum energy, E_i, required by an electron to initiate an ionization event can be obtained from conservation of momentum and energy equations [50]. Consider the three body process of an incident electron generating an electron-hole pair but neglect band structure details such as multiple band minima and anisotropies. The incident electron arrives with a mass m_e and velocity v_i. After the collision the electron has a velocity v_f. The resulting electron-hole pair has velocities and masses v_e, v_h, and m_e, m_h respectively (see Figure 2.4). The conservation of momentum and energy equations are given below.

$$m_e\vec{v}_i = m_e\vec{v}_f + m_e\vec{v}_e + m_h\vec{v}_h \tag{2.8}$$

$$\frac{m_e v_i^2}{2} = \frac{m_e v_f^2}{2} + \frac{m_e v_e^2}{2} + \frac{m_h v_h^2}{2} + E_g \tag{2.9}$$

To maximize the amount of energy the incident electron can transfer to generate the electron–hole pair, the kinetic energy of the three particles after collision must be minimized. This condition gives a threshold for the minimum energy

required for an incident electron to cause an ionizing event. Minimizing Equation 2.9 with the momentum constraints of Equation 2.8 is the same as minimizing the sum of the squares for a normed group. The result is simply that all three velocities are equal.

$$v_f = v_e = v_h \tag{2.10}$$

This result is the case of a purely inelastic collision, which appeals to physical intuition since one knows that maximum energy is transferred for a completely inelastic collision. Equation 2.8 for the conservation of momentum then gives the final velocity as

$$V_f = \left(\frac{2m_e + m_h}{m_e}\right) v_i. \tag{2.11}$$

Substituting Equation 2.11 in Equation 2.9 gives an expression for the minimum energy an incident electron needs to generate an electron-hole pair.

$$E_i = \frac{m_e v_i^2}{2} = E_g \left(\frac{2m_e + m_h}{m_e + m_h}\right). \tag{2.12}$$

If the hole mass equals the electron mass, $m_h = m_e$ then $E_i = \frac{3}{2}E_g$ which puts and upper limit on the ionizing energy. A more accurate model might account for more details and the fact that the electron masses could be different for the incident and newly generated electron but the simple approach gives the order of magnitude for the ionization energy.

Thus far I have shown the basic dependence of the ionization rate on electric field and given an order of magnitude estimate for the ionization energy. The task now is to use this knowledge of the ionization rate to obtain the breakdown voltage as a function of doping concentration. Borrowing from Sze's analysis of breakdown voltages [48] consider a steady state current j flowing through a reverse biased Schottky diode. The total current $j = j_e(x) + j_h(x)$ is constant everywhere, but the electron and hole contributions to the current are functions of the position within the depletion region. Assume that a small number of electrons

enter the semiconductor from the metal contact during reverse bias, making a current of density $j_n(0)$ at the interface. As this current passes through the depletion region it will be multiplied by a factor $\mathcal{M}_n$ through impact ionization events until it reaches the undepleted semiconductor bulk. In the bulk of the semiconductor the current will be entirely due to electrons since it is n-type and single carrier conduction predominates. We can write the total electron current at the boundaries, $x = \lambda$ and $x = 0$ as

$$j = j_n(\lambda) = \mathcal{M}_n j_n(0) \tag{2.13}$$

Breakdown is defined as infinite carrier multiplication or $\mathcal{M}_n = \infty$. The total carrier multiplication $\mathcal{M}_n$ must be integrated across the entire depletion region since the electric field is a function of position. Note that ionizing events generate holes which are also accelerated by the field and can similarly create more electron-hole pairs. Thus the incremental increase in total current density over a distance dx is the sum of both electron and hole ionizing events and can be expressed as

$$d(j_e) = \alpha_{ie} j_e dx + \alpha_{ih} j_h dx. \tag{2.14}$$

Rearranging in terms of the total current and electron current, we get

$$\frac{dj_e}{dx} - (\alpha_{in} - \alpha_{ip}) j_e = \alpha_{ip} j. \tag{2.15}$$

The general solution to Equation 2.15 is given in Sze [2] as

$$j_e(x) = j \left\{ \frac{1}{\mathcal{M}_n} + \frac{\int_0^x \alpha_{ih} \cdot \exp\left[-\int_0^x (\alpha_{ie} - \alpha_{ih}) dx'\right] dx}{exp\left[-\int_0^x (\alpha_{ie} - \alpha_{ih}) dx\right]} \right\}. \tag{2.16}$$

Integrating from $x = 0$ to $x = \lambda$ to get $j_e(\lambda) = j$.

$$1 - \frac{1}{\mathcal{M}_n} = \frac{\int_0^\lambda \alpha_{ih} \exp\left[-\int_0^\lambda (\alpha_{ie} - \alpha_{ih})\, dx'\right] dx}{\exp\left[-\int_0^\lambda (\alpha_{ie} - \alpha_{ih})\, dx\right]}. \tag{2.17}$$

Since breakdown is defined as infinite charge multiplication, $\mathcal{M}_n = \infty$ the right hand integral of Equation 2.17 must equal unity at breakdown. For direct band

gap material with symmetric conduction band minima and valence band maxima such as GaAs, $\alpha_{ie} = \alpha_{ih} = \alpha_i$ so that the integral in Equation 2.17 simplifies to

$$\int_0^{\lambda} \alpha_i dx = 1. \tag{2.18}$$

The ionization rates, α_{ie} and α_{ih} are complicated functions of the electric field which depends on doping concentrations and varies continuously throughout the depletion region. Using experimentally determined ionization rates and numerical computer methods to solve the integral in Equation 2.17 Sze [2] has determined theoretical breakdown voltage values for Ge, Si, and GaAs. These values are plotted in Figure 2.5. Although the calculation is rather complex, the final result is simple. The straight line dependence of the log-log plot indicates an inverse power dependence. The theoretical breakdown voltage dependence on doping concentration for GaAs can be expressed empirically as

$$V_b = 1.1 \times 10^{13} N^{-0.694} \tag{2.19}$$

where V_b is the breakdown voltage and N is the net ionized impurity concentration.

The theoretical breakdown voltage dependence on doping concentration serve as a good reference. For real Schottky barriers, however, the presence of interfacial oxides, interface states and high fringing fields tend to lower the effective barrier. To obtain accurate maps of carrier concentration, values of the breakdown voltage must be calibrated against carrier concentrations measured by other techniques such as Hall effect and C-V techniques.

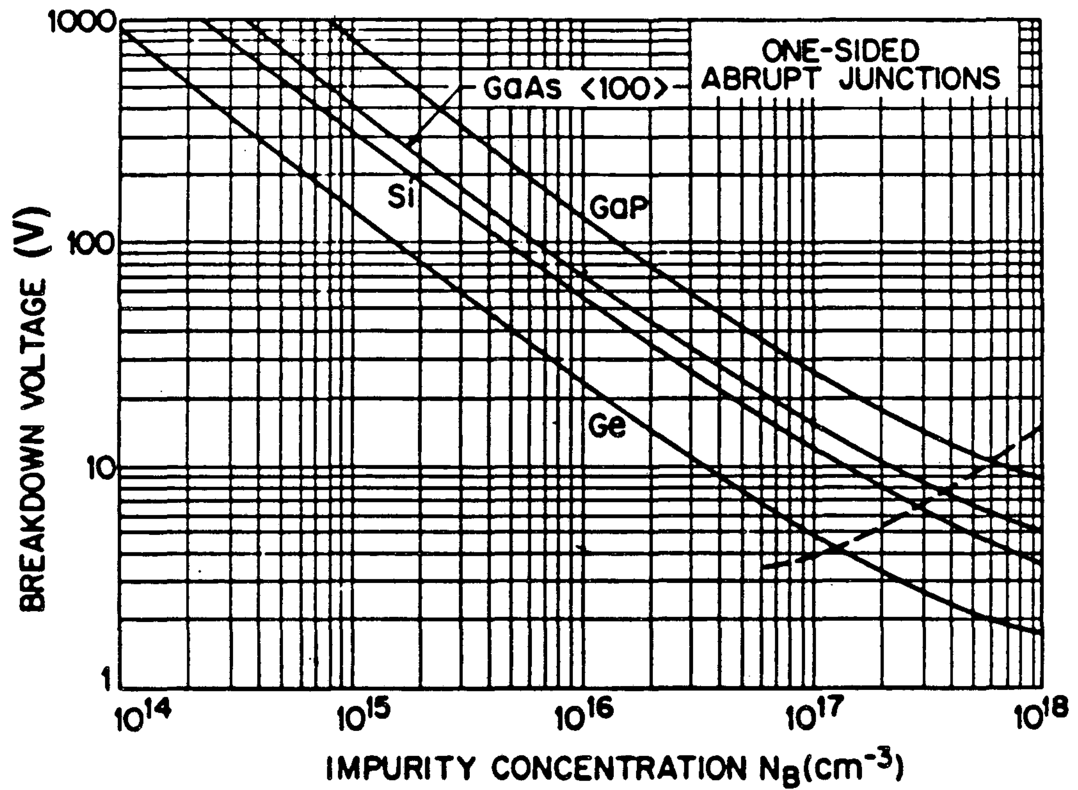


Figure 2.5: Avalanche breakdown voltage versus impurity concentration for one sided abrupt junctions in Ge, Si, GaAs, and GaP The dashed line indicates the doping at which the tunneling current will dominate the voltage characteristics. (Reference [2])

Chapter 3

Description of Apparatus

The test station to measure breakdown voltage consists of three main components,

1. Mechanical: To make electrical contact to the sample and step the probe across the sample
2. Electrical:, To measure the breakdown voltage of the Schottky barrier
3. Computer: To record values of the breakdown voltage, control the probe stepper, and create plots of the breakdown voltage versus position.

In this section I will describe each of these components and the theory behind their design.

The mechanical component is the plotter assembly on which the sample sits. Figure 3.1 shows a simplified schematic of the apparatus and sample geometry. The paper platten and pen actuator of a Hewlett Packard model 7225B plotter were modified to perform the measurement. The electrostatic paper hold down was removed and a new aluminum platten with an electrically isolated section was machined. The new platten was installed such that the old electrostatic hold down could be placed on top and the tester could still function as a plotter if need be. Indium or aluminum foil affixed to the electrically isolated section of the platten serves as the backside ohmic contact. The sample is placed on the foil

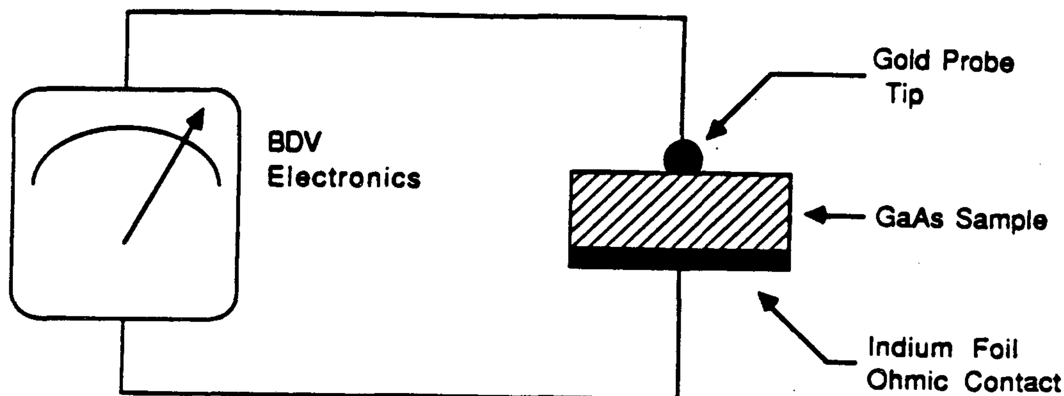


Figure 3.1: Schematic of breakdown voltage apparatus showing sample on a piece of indium foil with the gold probe touching the top surface.

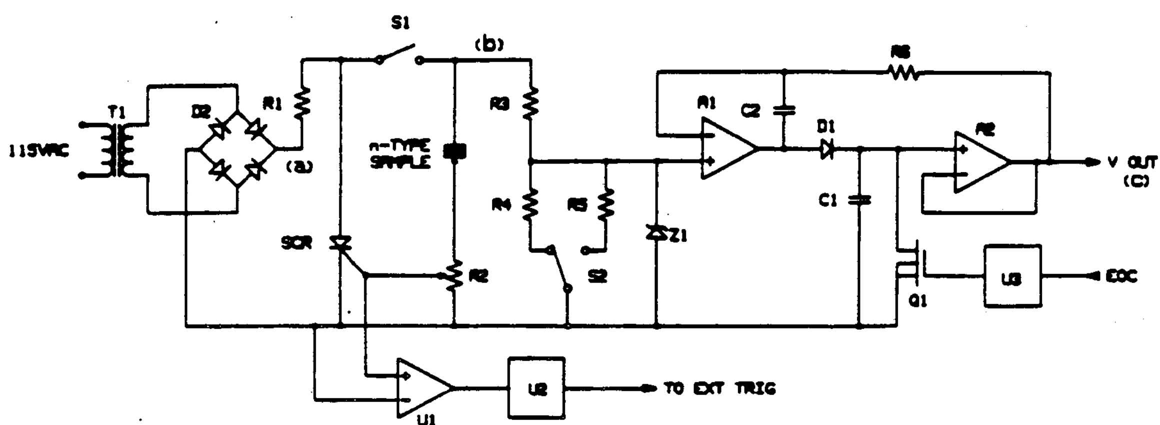
to make the measurement. It should be noted that indium and aluminum both form Schottky contacts to GaAs but can be used as a backside ohmic contacts since they are forward biased during the measurement. The oxide layer on the aluminum foil does not seem to affect the measurement. The pen actuator serves as a probe stepper to bring a gold wire Schottky barrier in contact with the sample. Utilizing a plotter pen, the ink and felt were removed and the outer plastic portion of the pen body was used to mount the gold wire. A quartz capillary tube was drawn out so that the inner diameter was slightly larger than the 5 mil diameter gold wire. The outer diameter of the quartz tube was such that it formed a friction fit within the pen body allowing adjustment of the probe height for samples of different thicknesses. The end of the gold wire was melted with a torch so that surface tension caused it to ball up preventing the wire from receding into the tube. The tip of the probe is a 200 μm diameter gold ball protruding out of the capillary tube. A 100 μm or smaller diameter probe, prepared by different means, could conceivably replace the present probe to increase spatial resolution.

The existing lift and drop mechanism for the pen was actuated by a solenoid. The solenoid action was too sudden so a small graphite dashpot by Airpot was added to damp the lowering of the probe while not affecting how it is lifted. This measure prevented sample breakage and increased the lifetime of the gold probe.

The electronics functions to measure the breakdown voltage. Before the breakdown can be measured one has to define some electrically realizable condition. Breakdown is usually associated with a drastic increase in electrical conductivity, which implies either a sudden increase in current or decrease in voltage. Many measurement techniques exist which could probe either case. Some experimenters determine breakdown by applying a ramped voltage and defining a preset current level. Others use a current source and measure the compliance voltage across the sample as the breakdown voltage. In this work, a preset current value of approximately 100 μA, which is 100 times the dark leakage current at low bias, serves as the definition of breakdown. When the current through the sample exceeds this value the voltage across the sample is measured as the breakdown voltage. This turns out to be relatively easy to implement as a measurement. It should be pointed out that electrical breakdown is nondestructive except when the sample goes into thermal runaway. The sample can be in continuous breakdown and suffer no irreversible effects. To avoid ohmic heating effects, however, which could shift the breakdown value, the the voltage across the sample is pulsed and not continuous.

This section will discuss the general operation of the electronics. Figure 3.2 gives the schematic for the measurement electronics. Table 3.1 gives the components list for the circuit.

First, 60 Hz 110 V line voltage is stepped up to 500 V peak to peak by the transformer. A full wave bridge rectifier turns this into 0–500 V peak pulse train. With relay 1 to the sample open, the wave form at point (a) in the circuit of



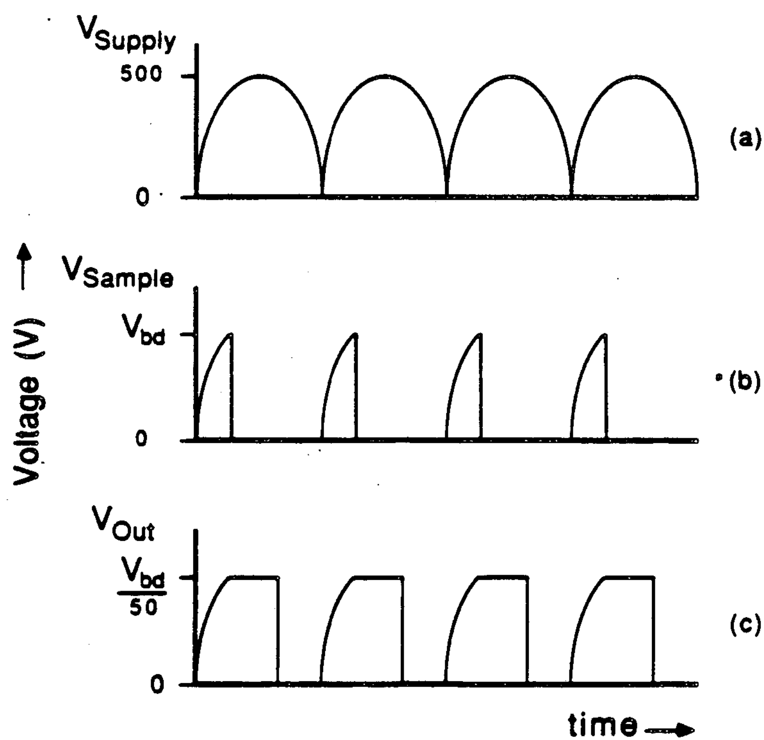


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Figure 3.2: Top is schematic for circuit to measure breakdown voltage of semiconductor samples. Bottom shows voltage waveforms at points a, b, c of breakdown voltage measuring circuit shown above.

Part	Description
R1	Resistor, 20kΩ
R2	Variable Resistor, 50kΩ
R3	Resistor, 5MΩ
R4	Resistor, 90.9kΩ
R5	Resistor, 909kΩ
R6	Resistor, 22kΩ
C1	Capacitor, polycarbonate, 2.2 nF
C2	Capacitor, 22 pF
T1	Transformer, 115V to 500V
D1	Diode, IN3070
D2	Full Wave Bridge Rectifier
Z1	Zener Diode, 12V
Q1	MOSFET, IRFD110
Q2	SCR, 2N2329
A1, A2	Operational Amplifier, FET input LF356BN
U1	Comparator, LM311H
U2	1/2 Multivibrator, 74LS123N
U3	1/2 Multivibrator, 74LS123N
S1	500V Relay, Hg contacts
S2	Relay

Table 3.1: Parts list and description for circuitry to measure breakdown voltage.

Figure 3.2 looks like wave form (a). When the relay is closed the voltage is applied across the sample in reverse bias. When the current flowing through the sample into the variable resistor R2 raises the voltage across R2 above .5 V, the SCR is switched on shunting the current to the sample. The sample is considered to have broken down and is allowed to recover until the SCR switches off at the next zero crossing of the applied voltage and the process begins again. R2 can be adjusted to set the reference current.

During the time the voltage across the sample is ramping up, a divider network, R3, R4 and R5, is registering a reduced value of the voltage. Op–amp 1 is part of an active peak sample and hold circuit which samples the scaled down breakdown voltage. The 15 V zener diode protects the input of the JFET op–amp from any spurious voltage spikes. Both JFET op–amps act as voltage followers. The first one charges the peak hold capacitor, C1, through a diode. If the input voltage ever decreases the diode isolates the capacitor from the output of the op–amp and the voltage across the capacitor remains constant. To minimize the capacitor droop, both the diode and the capacitor must have very low leakage currents. Plastic polycarbonate film capacitors work well for this application. The second op–amp must also have a very high input impedance so the capacitor is not discharged. The second op–amp drives the input of the A/D converter. The MOSFET in parallel with C1 resets the capacitor after each measurement. R6 and C2 couple the output of the first and second op–amp providing some derivative feedback control. Otherwise, the output of op–amp 2 tends to overshoot driving the output of op–amp 1 to the negative rail. The peak hold diode, D1, has the adverse affect of decoupling feedback for negative voltage swings so the derivative feedback prevents overshoot, eliminating this problem.

The timing of the circuit with the A/D board is handled by the comparator and oneshot in the circuit. As the sample begins to break down and the voltage

on R1 rises, comparator 1 detects this and sends a trigger signal to the A/D card to take a measurement. A one shot delays the signal to the A/D ensuring that the sample has broken down. When the A/D is triggered it measures the peak sample and hold voltage and returns an EOC (end of conversion) signal which turns on the MOSFET discharging the capacitor. The biasing pulse train from the full wave rectifier limits the rate of operation, allowing the sample to be broken down at 120 Hz. 50 breakdowns are averaged by the computer to give a value at one point, since breakdown is typically noisy and a single measurement can fluctuate 10-20 percent. The number of points to be averaged can be set from the computer. The magnitude and sources of error which influence how many points should be averaged will be discussed in the next section. Thus a single measurement could take on the order of .5 s. This is no time compared to the five minutes it takes to make a Hall effect measurement which does not include preparing and mounting the Hall sample.

To illustrate how quick SRBV measurements are, consider the case where one wants to determine the impurity concentration at 10 points across a wafer. To make a SRBV measurement, one has to clean the sample surface, bring the sample to the instrument and measure it. The entire process would conservatively take 20 minutes. To do a Hall effect measurement, mounting the wafer and cutting 10 samples would take 1 hour. Applying 4 contacts to the corners of each sample, annealing and waiting for them to cool would take 1 more hour. Attaching wires to the contacts is 1/2 hour. Mounting and measuring each sample would take another 1.5 hours. This very optimistic time estimate for Hall effect measurements on ten samples is 4 hours. So, what takes a moment to do using SRBV takes an entire afternoon with Hall effect and one could have measured 100 breakdown values just as easily with SRBV.

Before discussing results of breakdown voltage measurements made on actual materials, one needs to have an idea of what the instruments limitations are. In this section I will discuss the barrier height of the Schottky diode, the range of doping that can be measured, the resolution for distinguishing differences in doping , the spatial resolution of features that can be seen, how reproducible measurements are, and what factors influence the performance of the instrument and how these parameters can be optimized to get the most accurate measurement possible.

Since the instrument is based on the reverse breakdown of a Schottky barrier, it is important to characterize the barrier height of the diode. The barrier, as discussed in Chapter 2 is the difference between two Fermi levels of the metal and semiconductor at the surface and determines how good a rectifier the diode will be. By characterizing the barrier height we can get an idea of how ideal a contact we are actually getting by placing a wire on the surface of the semiconductor. Two techniques were used to characterize the barrier height; one based on the I-V properties of the diode and the other based on the C-V properties. The C-V determination of the barrier height was made while calibrating the impurity concentration of the samples. To determine the barrier height, one plots $1/C^2$ versus V. For a constant doping concentration this will give a straight line plot. Extrapolating to infinite capacitance, or $1/c^2 = 0$, and reading this voltage at the x-intercept gives the built-in potential. Figure 3.3 shows a plot of $1/C^2$ versus V for moderately doped GaAs, 2×10^{16} cm^{-3}. Checking the x-intercept, the barrier height is 0.86 eV. Using the I-V characteristics of the diode to measure the barrier is almost as straight forward. Using the Bethe [47] expression for forward bias thermionic current:

$$J = A^{**}T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \exp\left(\frac{-qV}{nkT}\right) \tag{3.1}$$

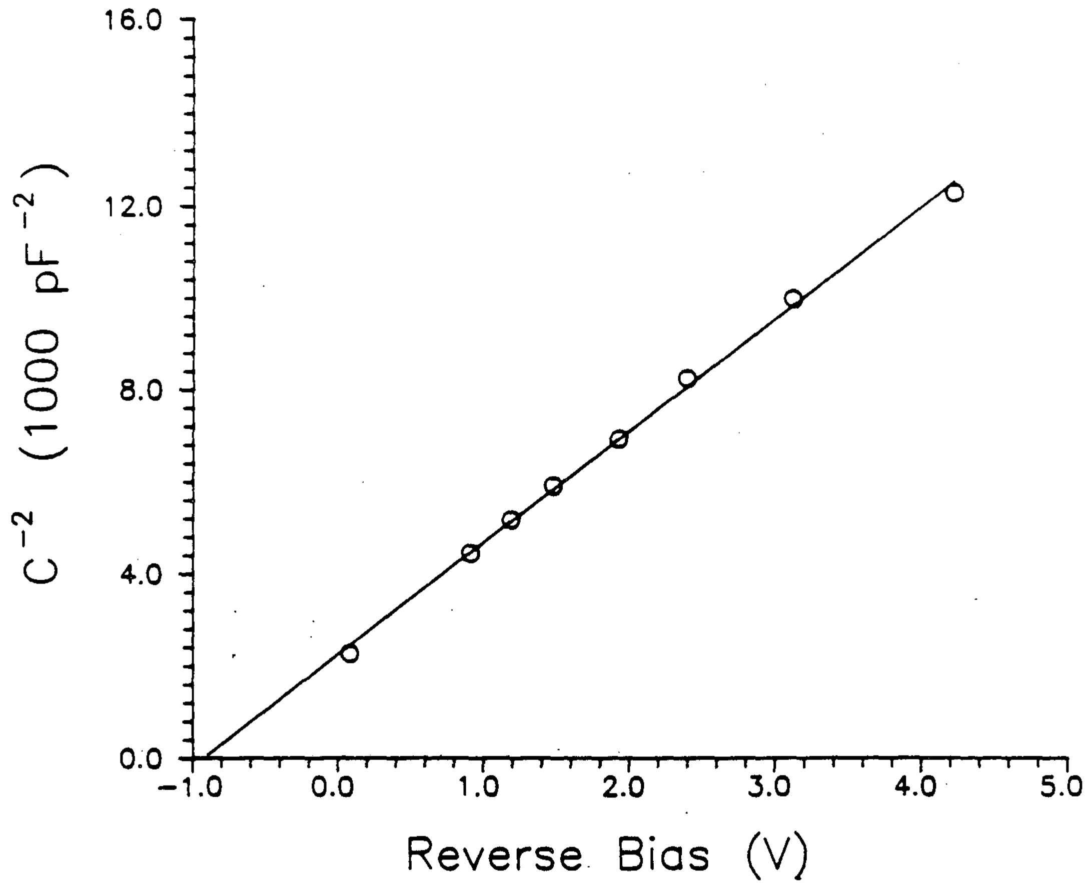


Figure 3.3: Plot of $1/C^2$ versus V for breakdown voltage probe. on moderately doped, $2 \times 10^{16}\mathrm{cm}^{-3}$ GaAs. Barrier height is extrapolated to .86 eV.

where A^{**} is the effective Richardson constant, 144 A cm^{-2}K^{-2} for GaAs and n is the ideality factor. This equation is true for $V_{app} > 3kT$. Thus by extrapolating the linear portion of a ln(j) versus V plot back to V=0 to get J_s, one obtains an expression for the barrier height;

$$J_s = A^{**}T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \tag{3.2}$$

and

$$\phi_B = \frac{kT}{q} \ln\left(\frac{A^{**}T^2}{J_s}\right) \tag{3.3}$$

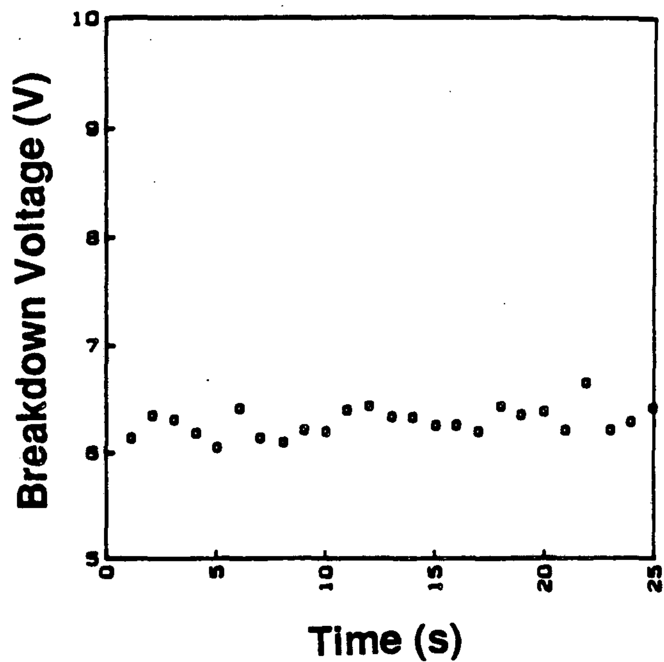
The slope of the curve gives the "ideality factor" n. For an "ideal" Schottky diode, where the barrier height is independent of bias, n equals unity. The measured barrier height and ideality factor for the breakdown voltage probe are in the range of .6 eV and 2.6 as measured by the I-V characteristics. Typical deposited metal GaAs Schottky diodes have ideality factors of n=1-1.1 so n=2.6 is quite large. Factors which would make n greater than unity are high series sample resistance, bias dependent image force lowering of the barrier, electron tunneling through the barrier, carrier generation via deep levels, and the presence of an interfacial insulating area.

The experimentally determined barrier heights are somewhat lower than 0.9 eV which is the expected barrier for gold Schottky diode on GaAs. The fact that the actual barrier is lower than expected is not alarming and can easily be understood. The barrier of 0.9 eV is obtained for the best gold Schottky diode that can be made by an ultra high vacuum gold evaporation on an in-situ cleaved GaAs surface. By placing the wire probe on the surface it is not necessarily in intimate contact, leaving a small insulating gap. Also, it does little to passivate surface states. The presence of an insulating gap at the interface has the effect of lowering the barrier since part of the voltage drop must occur across this layer (see Figure 2.1b). Accumulated charge at surface states can also

be responsible for significant lowering of the barrier height. Accumulated charge at the surface explains the difference between barrier heights determined by C-V and I-V techniques. The measured barrier height is lower for I-V than C-V. The C-V technique projects the barrier height assuming a constant doping and does not account for surface charge. The value of the voltage giving zero depletion must be extrapolated since there is no way to measure infinite capacitance. Thus it ignores the presence of surface charge which could significantly lower the barrier at the surface. I-V techniques, however, directly measure the barrier height at the surface and can account for surface states.

Figure 3.4 also shows evidence for trap states at the interface. The two plots show the breakdown voltage as a function of time for Ge doped GaAs. The sample is being pulsed at 120 Hz and every .1 s a breakdown value is recorded. The top graph is for illumination on, and the bottom is for illumination off. With the light off, it takes approximately two seconds for the traps to reach an equilibrium occupation. With the light on however, the breakdown voltage remains constant over time and is equal to the initial value with the light off. Thus one must be careful about illuminating the sample during a measurement, so that the breakdown voltage has reached equilibrium before taking a reading. Most samples showed a similar time dependence of the breakdown voltage, but none showed as large a shift over such a long time (2 s) as the Ge doped GaAs. To account for the initial shift in the breakdown value, a delay is made after turning on the voltage before taking a reading.

In Chapter 2, a theoretical dependence of the breakdown voltage dependence on doping concentration was developed. Theory gives the general trend of the breakdown voltage dependence on concentration, but in order to make a useful measurement, the instrument must be calibrated. Theory defines breakdown as the infinite multiplication of current through an ideal diode. An actual measure-



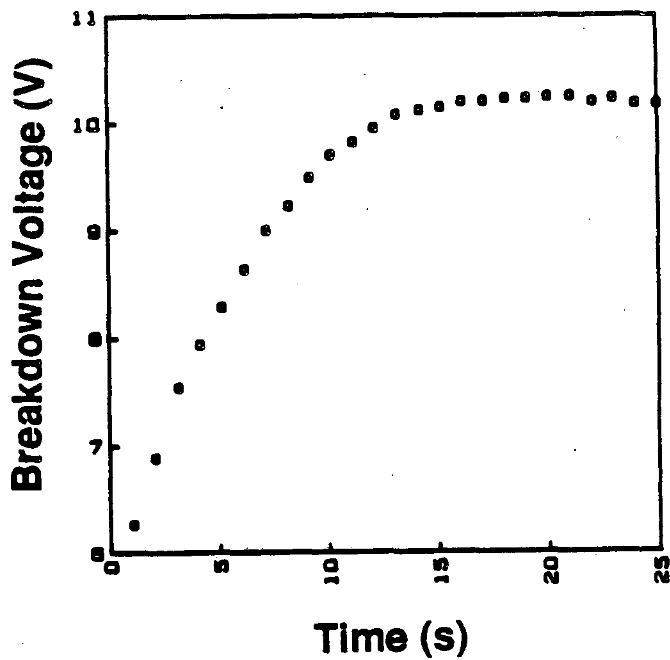


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Figure 3.4: Breakdown voltage versus time for Ge doped GaAs. The top graph is with the sample being illuminated. The bottom is with the illumination off.

ment differs from theory in two areas: 1) Placing a gold wire on the surface of a semiconductor is far from an ideal Schottky contact and has significant leakage current. 2) We measure breakdown at a preset current level, not at infinite charge multiplication. These differences make the measured breakdown voltage lower than predicted by theory since the instrument is sensitive to leakage currents.

The calibration was made by using capacitance-voltage techniques to determine the carrier concentration. I chose C-V over Hall effect to determine the doping concentration since some of the lower doped samples, below 10^{16}cm^{-3} were very inhomogeneous. Hall effect measurements would tend to average the doping concentration across the entire sample, while breakdown voltage measurements are localized. C-V measurements are inherently not as accurate as Hall measurements since one needs to know the capacitor area. 0.5 mm diameter gold capacitive dots were evaporated on the surface of the sample. The plotter modified for the breakdown voltage measurements was also useful probing these capacitors. One moves the probe over the capacitor to be measured and lowers the probe to make contact, eliminating the need to attach a wire to the metallization. Once the C–V characteristics of the diode were measured, the breakdown voltage was then measured in four 90 degree positions around the capacitor and averaged to get the calibration. Figure 3.5 is a log-log plot of the calibration.

Using a power law fit of the data as suggested by the theoretical results in equation 2.19, a least square fit of the data gives

$$N = 1.7 \times 10^{18}\, V_b^{-1.44}. \tag{3.4}$$

Where N is in cm^{-3} and V_b is in V. The straight line fit deviates for lower voltages due to the onset of tunneling breakdown. The lower voltage limit for a measurement, determined by overwhelming tunneling current is 5 V. The upper limit is 500 V, fixed by the maximum Ohmic heating the sample can withstand. This corresponds to a measurable doping range of $5 \times 10^{14} - 5 \times 10^{17}\text{cm}^{-3}$.

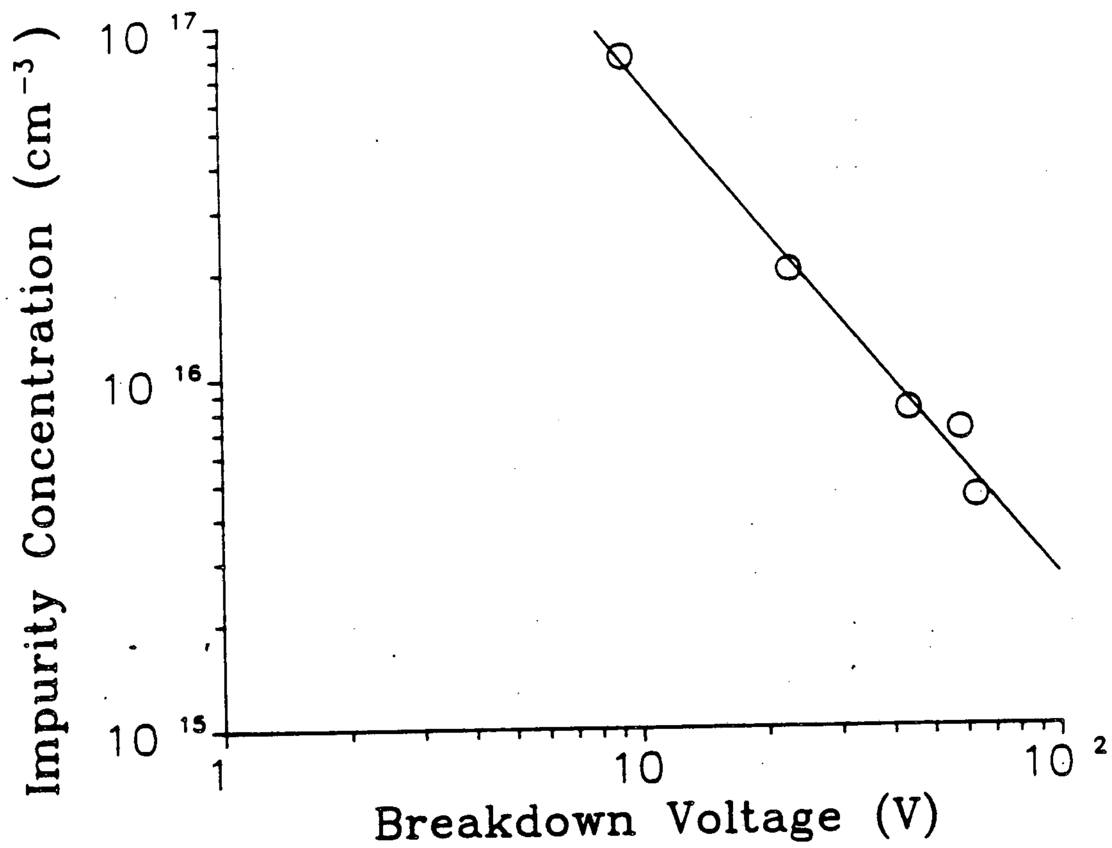


Figure 3.5: Log -log calibration plot for the experimentally determined carrier concentration versus Breakdown voltage. A power law fit of N = (1.7e18)$V^{-1.44}$ is drawn in.

Breakdown of junctions is typically noisy. The sudden current flow associated with breakdown can happen over a range of voltages. Using equation 3.4, the empirical relation between doping and breakdown voltage, the relative error in concentration is

$$\frac{\Delta N}{N} = \frac{\partial \ln N}{\partial V}\Delta V = -1.4\frac{\Delta V}{V} \tag{3.5}$$

which is on the order of the relative voltage error. Despite averaging, errors can be on the order of 2 V at a breakdown voltage of 20 V for successive measurements. This error is not due to averaging since the 40 readings averaged to make one measurement give an error of .1 volt. The error is systematic and due to nonreproducible placement of probe on the GaAs surface. A 2 V error at 20 V corresponds to a 15% error in determining the doping concentration. An error of 2 V at 200 V however is only a 1.5% error. Investigation into how ΔV scales with V determines the accuracy of the instrument over its measurement range. If ΔV is constant then the instrument is more accurate at higher breakdown voltages and has a better doping resolution at lower concentrations. If however ΔV scales with voltage then the accuracy of the instrument remains constant over the measurement range. At 200 V the error is approximately 10 V which corresponds to a 5% error in concentration. So, the instrument is more accurate at lower concentrations of impurities.

Here the sources of error are analyzed to find how ΔV scales with voltage and what can be done to minimize errors. 1. Digitization: 10 bit digitization breaks the 500 V range into approximately .5 V increments. For a 10 V breakdown this corresponds to a 5% error. To minimize digitization error a divider network can be switched by the computer between two ranges, 5-50 and 50-500 V. 2. Probe placement: Since the Schottky barrier probe is a wire placed on the surface of the GaAs, it is not in as intimate contact as an evaporated contact. Differences in contact area and surface properties can occur causing differences in the measured

voltage. The HP pen actuator applies approximately 30 grams of pressure on the probe tip. It is important that as much pressure be applied to the tip as possible without wearing down the probe too quickly. The added force increases the reproducibility of the contact by making the probe less sensitive to contamination on the surface. Another step which lessens the effects of surface contamination is to slide the probe into position. This can be accomplished by either sliding the probe across the surface from the last position, or better, placing the probe in position, turning on the voltage and sliding the pen a small distance away from and then back to the appropriate position. The combined electrical and mechanical action breaks through any contamination or oxide layer giving the probe a direct contact to the semiconductor. Errors associated with poor contact to the semiconductor result in measuring a breakdown voltage higher than predicted. Thus the doping concentration is underestimated. **3.** Differences in surface preparation can also lead to errors in determining the breakdown voltage. The above procedure helps insure a good contact through surface contamination, but a clean surface that is prepared in the same manner for each measurement is best. The procedures for preparing a sample surface are:

- The sample surface is lapped and mechanically polished optically flat.
- If the sample is already polished then it is rinsed in organic solvents TCE, then acetone, then methyl alcohol, then DI H_2O.
- The sample is etched in 5% hydrofluoric acid for two minutes to remove any oxide layer
- Followed by a DI rinse and nitrogen blow dry.

The purpose of the treatment is to measure samples with identical surfaces so that even if they are not ideal they at least introduce the same error and can be

calibrated. Figure 3.6 shows a breakdown voltage map of the impurity concentration for Si doped GaAs grown by the HB technique. Also shown are spatially resolved Hall effect measurements of the free carrier concentration for the same sample. The concentration of the Si is approximately 2×10^{17} cm^{-3} and should all be ionized at room temperature. Therefore the free carrier concentration and net impurity concentration should be the same. The two plots are in good agreement so we can believe the impurity concentration values determined by breakdown voltage.

Position is the other parameter that is measured for spatially resolved breakdown voltage. Distances are measured using the internal position encoder of the plotter. The minimum step size and accuracy specification for the plotter pen is 25 μm. The actual resolution of the machine is worse due to the diameter of the probe, and loose tolerances in the pen lowering mechanism. The pen diameter is 200 μm and the play in the pen mechanism is 50 μm. A rough estimate of the resolution can be made referring to Figure 3.7 which shows the breakdown voltage versus position for HB GaAs grown under a low thermal gradient. The two traces are for the same line across the sample and show the reproducibility of the technique. To determine a lower limit that the reproducibility must be worse than, compare the offset in the breakdown voltage peak at 4.5 mm. The offset in the peak for the two traces is .2 mm, which is on the order of the pen diameter. From 5 to 8 mm the sample develops periodic fluctuations in doping. The period of the fluctuations is .7 mm and is well defined in both traces. Since this is the smallest fluctuations observed yet, it puts an upper limit on the resolution of the instrument at .7 mm.

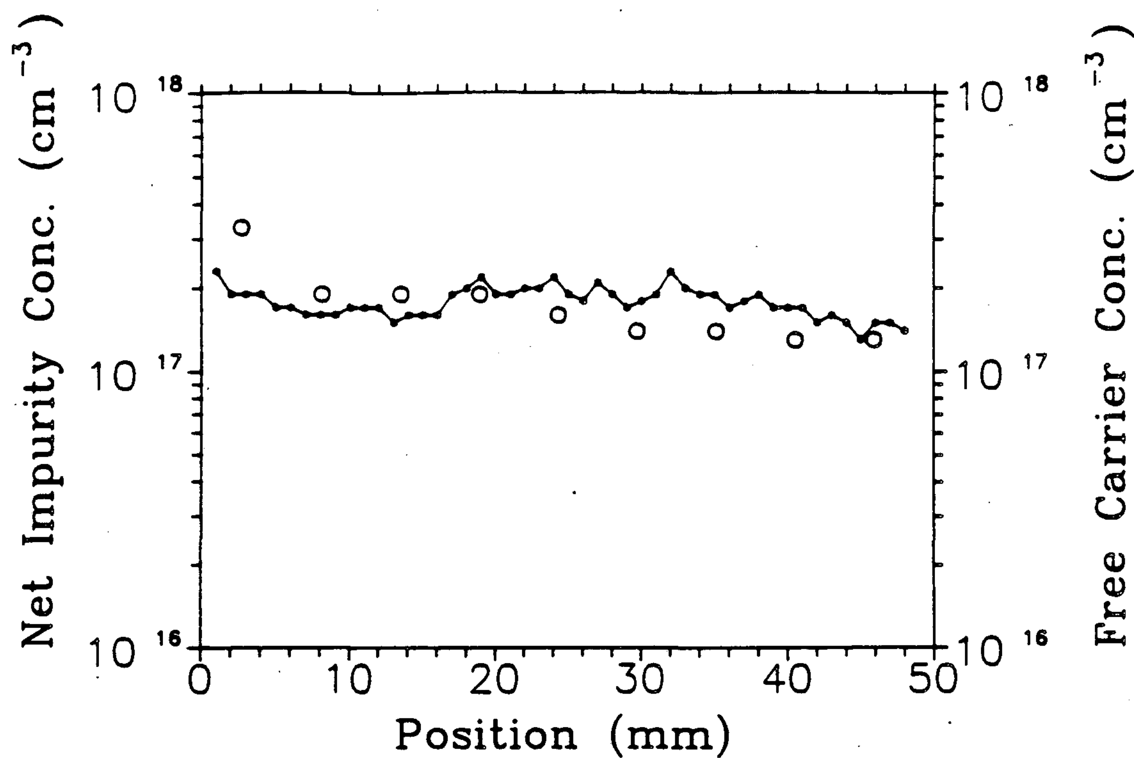


Figure 3.6: Plot of impurity concentration versus position indicated by connected points. Open circles indicate free carrier concentration as determined by Hall effect.

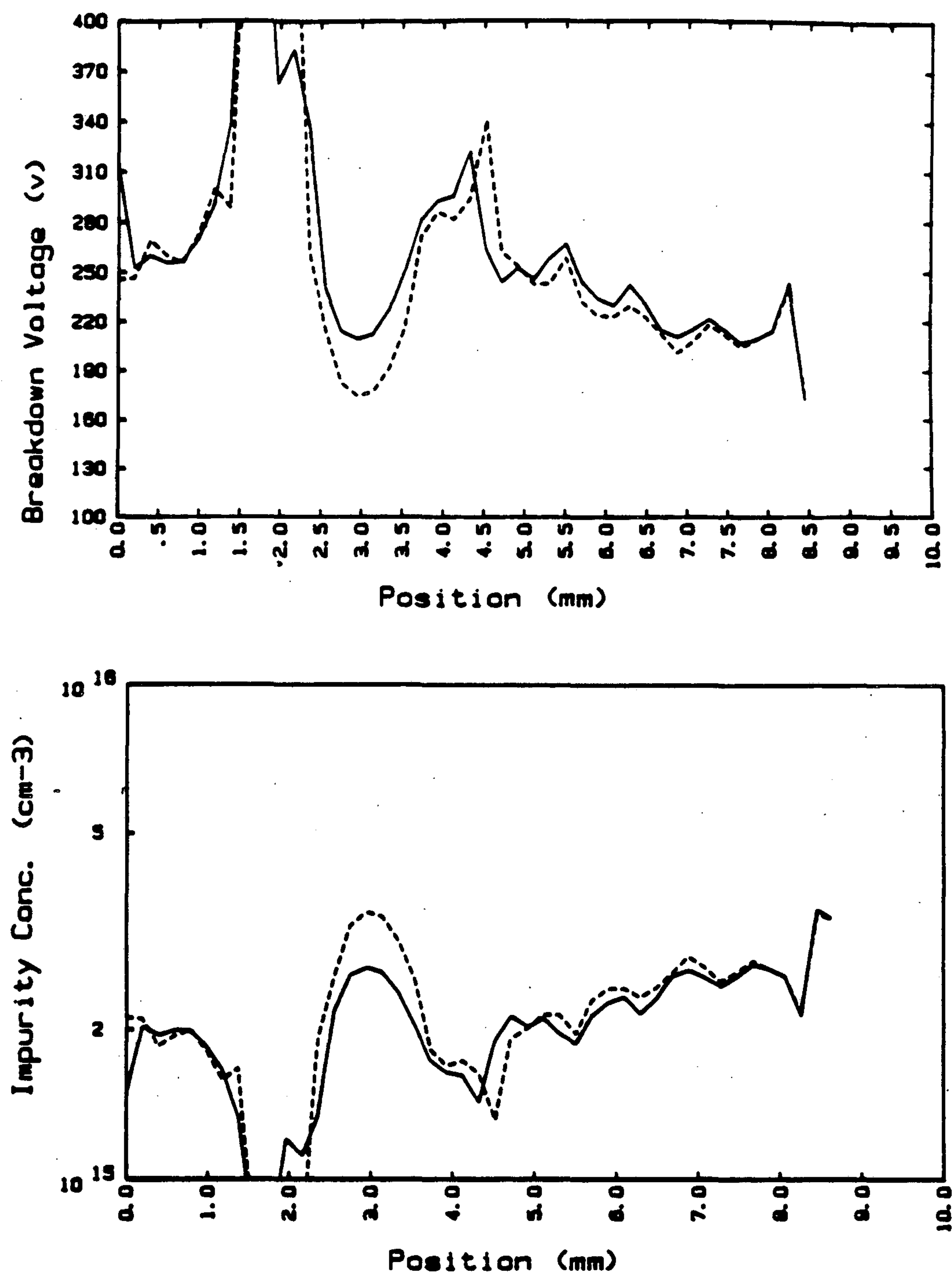


Figure 3.7: Plot of the breakdown voltage and corresponding concentration versus position for HB GaAs grown with a low thermal gradient. The dashed and solid lines are for two independent measurements over the same points on the sample. Note, the correlation between the two traces shows the reproducibility of the technique.

Chapter 4

Results and Discussion

After building the breakdown voltage apparatus, many different GaAs materials were tested to determine the operating range of the instrument. The materials studied were bulk HB crystal grown from quartz boats, carbon boats, and under a small thermal gradient. LEC wafers were measured and the results compared to plots of the etch pit density. Epitaxial layers of AlGaAs were studied as well as Si implanted layers. We did not focus on one particular material since we were interested in knowing the applicability of the measurement to a wide variety of materials. In the future, spatially resolved breakdown voltage measurements can be used in conjunction with other techniques to fully characterize a specific material. The materials studied and the reasons for success or not will be discussed in this section.

The first materials studied were our own HB GaAs crystals grown at the CAM GaAs facility. The resulting material was n-type due to silicon contamination from the quartz boat it was grown in. Figure 4.1 shows a plot of the breakdown voltage versus position for a crystal. The top graph is a horizontal scan from the seed end of the crystal along the top surface of the crystal. The breakdown voltage decreases from 16 V at the seed end to approximately 12 V 45 mm down the crystal. This corresponds to an increase in impurity concentration from 3.6×10^{16} to $5.6 \times 10^{16}\,\text{cm}^{-3}$. Along the bottom surface the breakdown voltage is

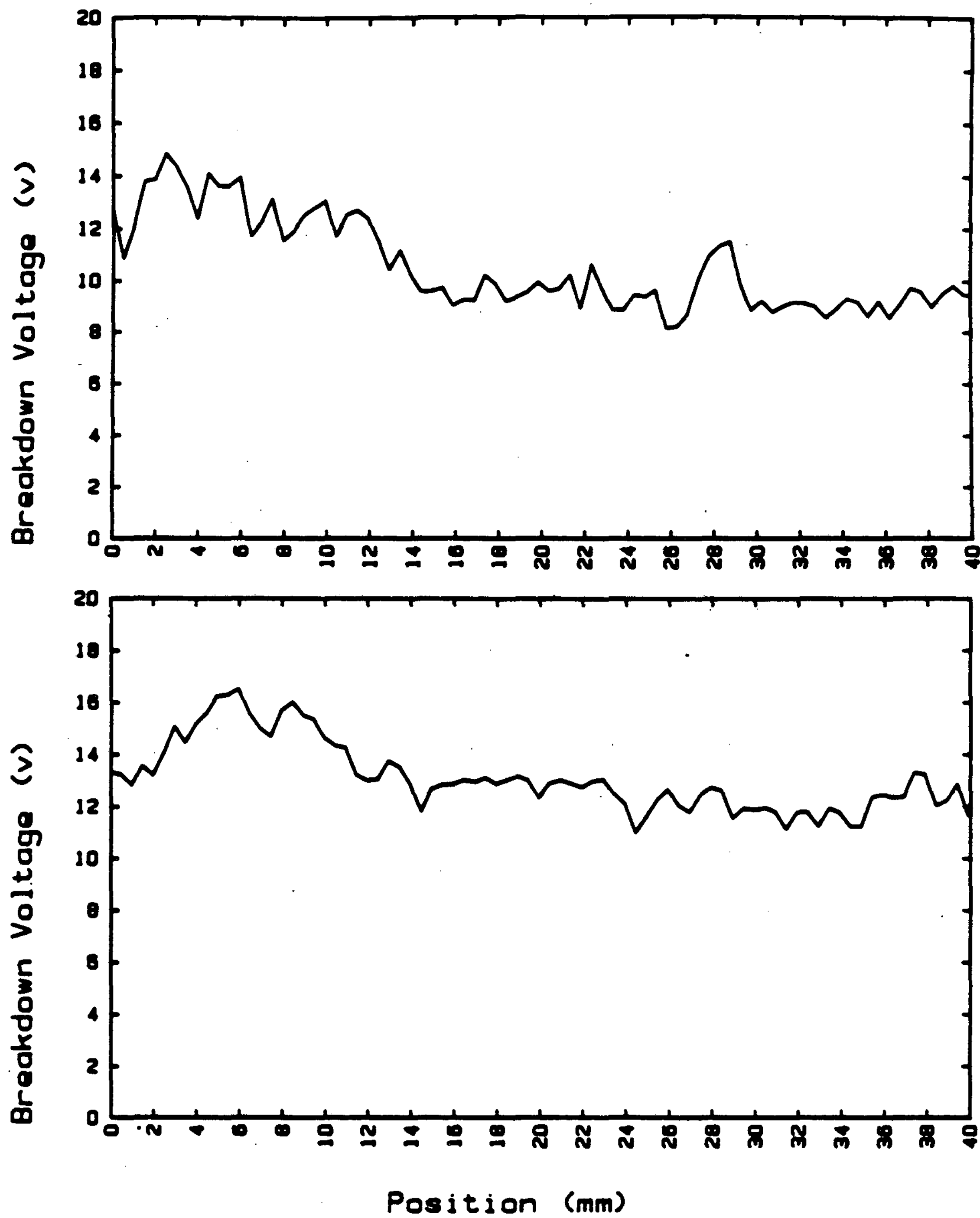


Figure 4.1: Plot of breakdown voltage versus position for HB GaAs. The top plot is from the seed to the tail end of the crystal along the top surface. The lower plot is along the bottom surface near the boat.

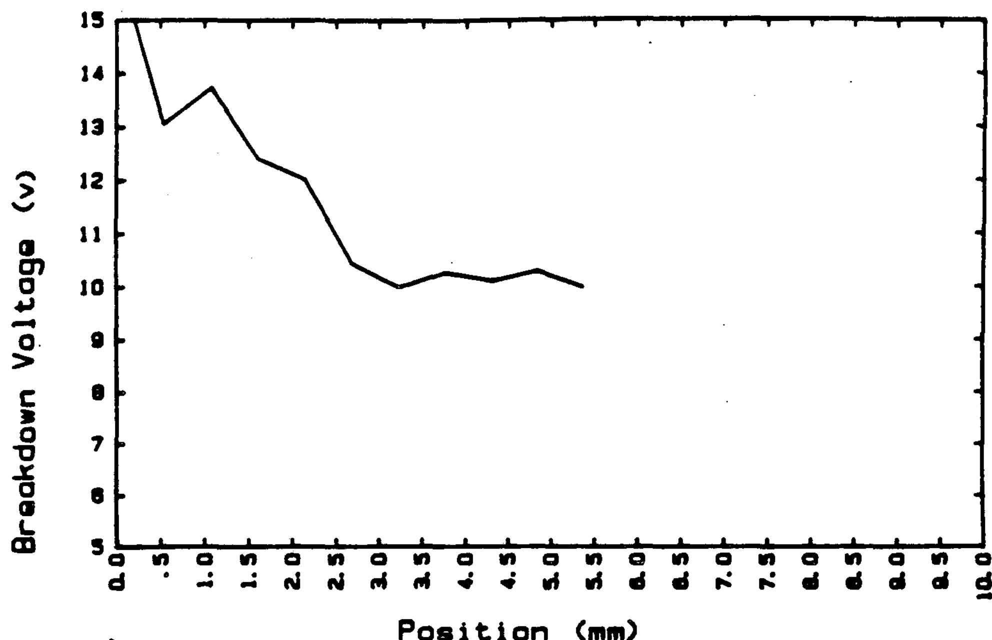


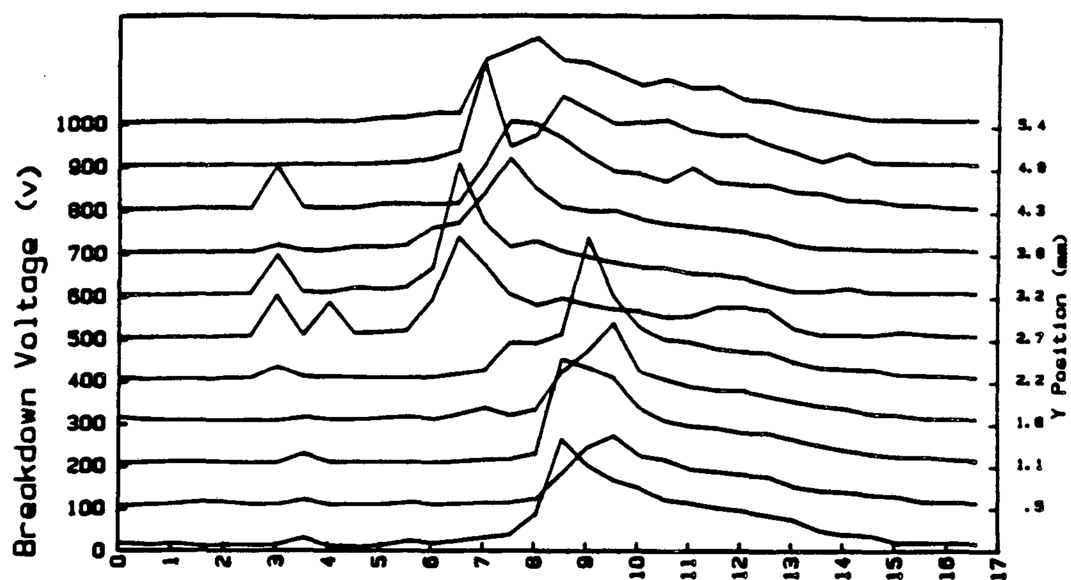
Figure 4.2: Plot of breakdown voltage versus position along a vertical scan of the crystal in Figure 4.1.

consistently less than along the top surface. The impurity concentration increases from 4.5×10^{16} to 8.4×10^{16} cm^{-3}. The rate of increase in impurity concentration exceeds what might be expected from considering only the segregation coefficient of silicon in GaAs. The high rate of silicon incorporation is due to a constant flux of silicon from the silica boat during the entire growth period. Hurd [51] has analyzed the incorporation of impurities from crucible materials, and has found the flux of Si atoms in HB GaAs to be approximately 10^{17} atoms $cm^{-2}hr^{-1}$. Figure 4.2 shows a scan of the breakdown voltage vertically across the crystal from the boat to the free surface of the crystal. The plot indicates that the silicon incorporation is higher near the crucible than at the free surface. Impurity incorporation rates are sensitive to many of the crystal growth parameters such as boat material, As overpressure, and the presence of native defects and other impurities.

The upper portion of Figure 4.3 shows a two dimensional scan of breakdown

voltage for a crystal grown from a graphite boat. Successive scans in the y direction are offset vertically to separate them. The lower plot shows the the corresponding impurity concentration for the uppermost voltage scan. The interesting feature about this crystal is the fact that it switches from p-type to n-type. Carbon is amphoteric in GaAs, but predominantly occupies the As site making it an acceptor. On the basis of the crystal grown in the silicon boat becoming increasingly n-type, one might expect that the crystal grown in graphite would become increasingly p-type, however this is not the case. Carbon appears to enhance the incorporation of Si into the crystal from the quartz ampoule. Hurd found the incorporation rate, defined as the flux of impurities crossing the interface between crucible and crystal, of Si in GaAs grown from graphite boats to be greater than $3 \times 10^{17}\, cm^{-2} hr^{-1}$, almost three times the flux in a silica boat. It is interesting to note that the carbon flux is only $2 \times 10^{16}\mathrm{cm}^{-2}\mathrm{hr}^{-1}$ [51]. The low carbon flux is responsible for the change from p-type to n-type. An increased concentration of carbon acceptors can drive down the Fermi energy making it energetically more favorable to incorporate silicon, and more importantly carbon can reduce SiO, which originated from the ampoule, freeing up a large source of silicon. Figure 4.4 shows the breakdown versus position across a vertical section of the crystal from the carbon crucible to the free surface on the n-type side. The plot shows that the crystal is increasingly n-type towards the free surface. Whether this is due to increased silicon incorporation at the free surface or increased carbon incorporation at the crucible would have to be determined by further studies. However, for the crystal grower who is attempting to reduce silicon contamination by using a graphite crucible, SRBV measurements can determine much more quickly than Hall effect that the graphite is not accomplishing this.

The material scanned in Figure 3.7 which was used to place an upper limit



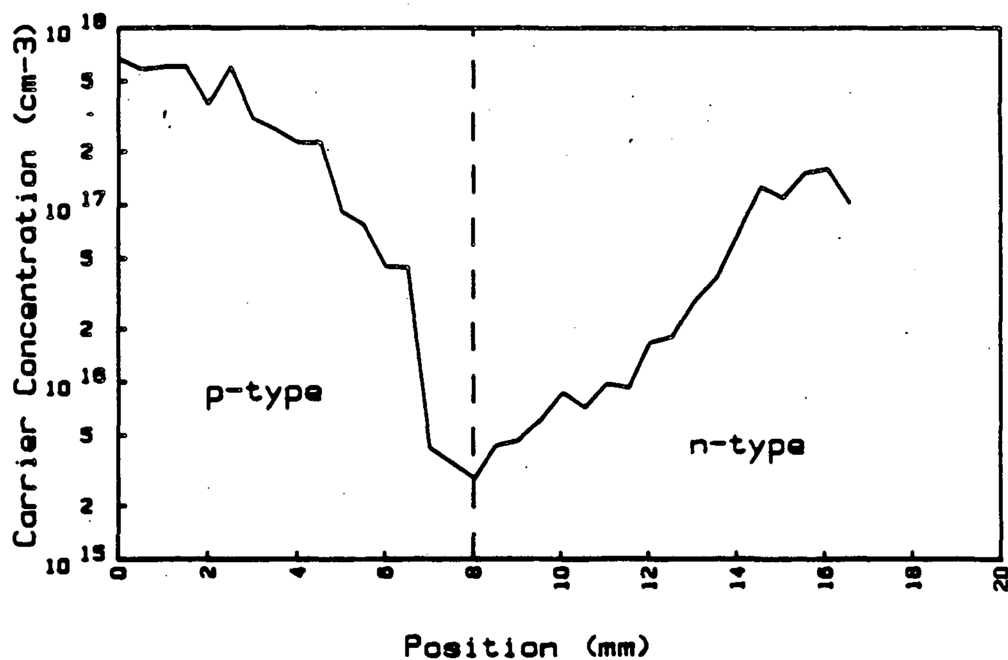


Figure 4.3: Upper plot shows breakdown voltage versus position for a two dimensional scan of a HB crystal grown from a graphite boat. Y position offset is shown to the right. The lower plot shows the concentration versus position for the uppermost scan of the breakdown voltage plot.

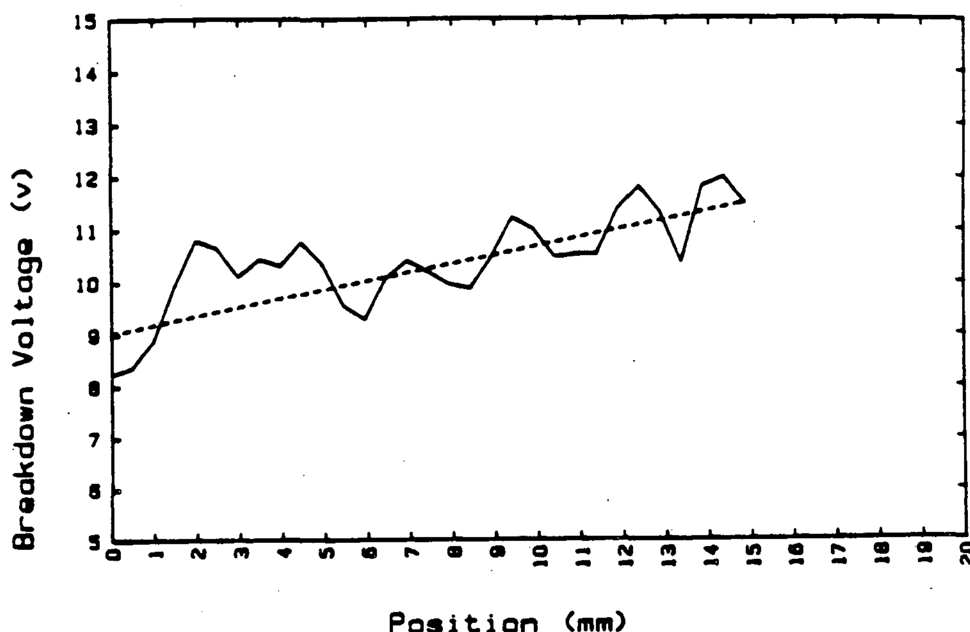


Figure 4.4: Breakdown voltage versus position for a HB GaAs crystal grown from a Graphite boat. The plot is across a vertical section from the boat to the free surface of the crystal.

on the resolution of the instrument, is low gradient freeze HB GaAs. The reason for growing with a small gradient is to reduce thermal stress on the crystal, and thus reduce the dislocation density. The main problem, however is controlling the growth interface. With a small gradient, slight temperature fluctuations can cause the solid-melt interface to advance or recede quite rapidly. Large changes in the solidification rate cause variations in the effective segregation coefficient of impurities resulting in inhomogeneously doped crystals. Low gradient freeze material was used to estimate the resolution of the SRBV instrument because the doping concentration fluctuated strongly.

Another bulk GaAs material tested was LEC GaAs. Most LEC material is semi-insulating and can not be measured by breakdown voltage. Some n-type material was obtained from J. Lagowski at MIT. Figure 4.5 shows the breakdown voltage and corresponding concentration across the diameter of a small crystal. Also shown is the etch pit density (EPD) of dislocations on the surface of the

wafer. The concentration of impurities as determined by SRBV is relatively constant at $6 \times 10^{17}\,\mathrm{cm}^{-3}$ but does increase slightly towards the edge of wafer. This correlates with the associated increase in EPD and indicates the possibility of a donor like defect associated with dislocations in LEC GaAs. In the undepleted bulk of a semiconductor, the charge state of a defect depends on the position of the Fermi level. In n-type material, the Fermi level and free electron concentration are independent of additional deep level donors since they lie below the Fermi level. In the depletion zone, however, all defects are ionized so even deep levels contribute to the space charge. Thus Breakdown voltage measurements are sensitive to the presence of deep level defects in concentrations on the order of the shallow doping. Further measurements would need to be performed to determine the identity of the defect associated with the dislocations. EL2 has been reported near dislocations [40,28] in semi–insulating material, but this material is heavily n-type so it is not likely EL2 exists in high concentrations. It has been found experimentally [52] and shown thermodynamically [16] that free carriers suppress the formation of arsenic antisites and the related EL2 deep donor level. Other possibilities for donors are dangling bond type defects associated with dislocations, or the possibility that silicon preferentially occupies sites near dislocations due to strain fields or the presence of vacancies.

The next group of materials studied were epitaxial layers. An important consideration when performing SRBV measurements on epitaxial layers is the thickness of the film. It must be greater than the depletion width at breakdown so the field does not "punch through" the layer. If the depletion width does punch through, then the substrate will be influencing the breakdown, and the voltage value will reflect the substrate doping as well. The same holds for implanted or any other type of layer one is interested in measuring. Figure 4.7 shows the depletion width at breakdown as a function of doping for a variety of

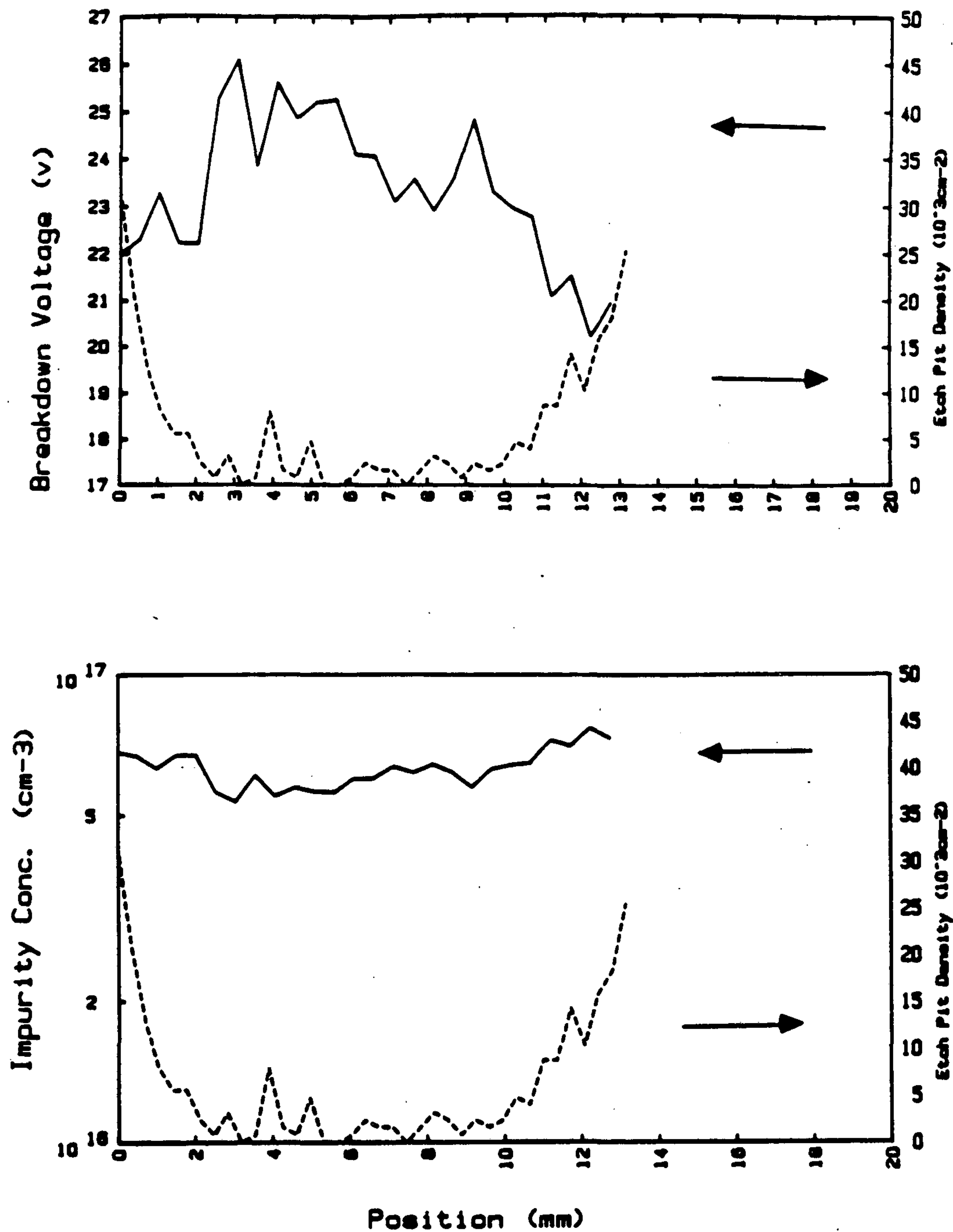


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Figure 4.5: Correlation of breakdown voltage and etch pit density versus position for LEC GaAs. The solid line corresponds to breakdown voltage (impurity concentration) in the upper (lower) plot and the dashed line corresponds to etch pit density.

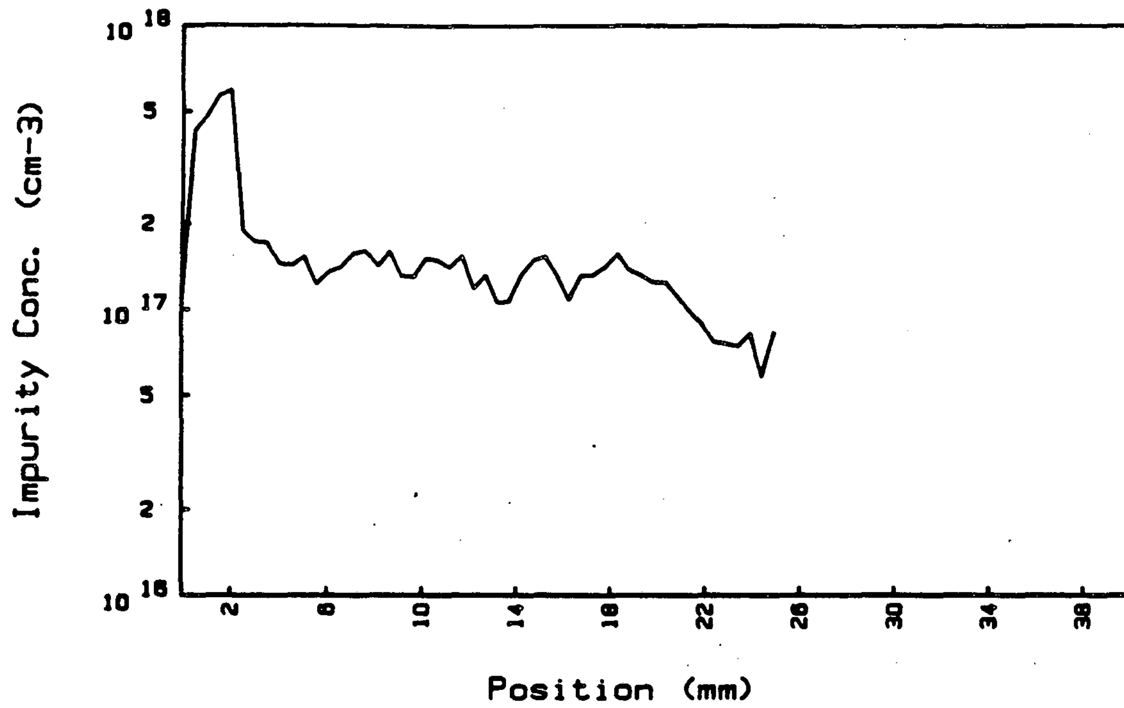

Figure 4.6: Impurity concentration versus position for $Al_{.30}Ga_{.70}As$ epitaxial layer.

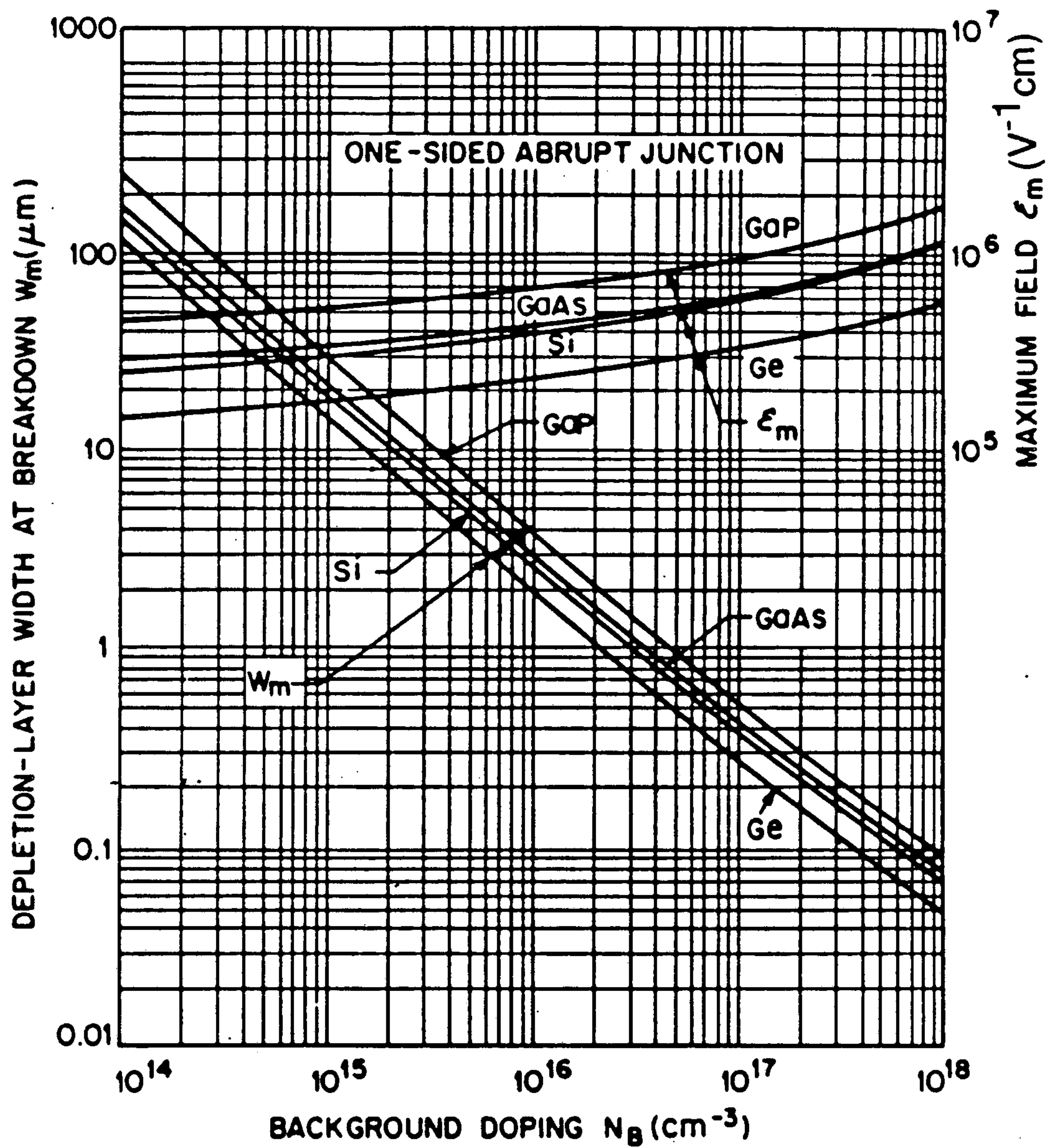

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Figure 4.7: Depletion layer width and maximum field at breakdown for an abrupt single sided Schottky diode in Ge, Si, GaAs, and GaP. (Courtesy of Sze, Ref. [2])

semiconductors.

Figure 4.6 shows the results of a breakdown scan on a 1.4 μm thick MOCVD $Al_{.3}Ga_{.7}As$ epitaxial film on a GaAs substrate. The concentration shown is too small since the calibration curve for GaAs was used. The actual concentration is higher due to the increased bandgap of AlGaAs. Interpreting the data is not as clear for ternary compounds since fluctuations in the breakdown voltage could be due to variations in the band gap energy caused by changes of the Al to Ga composition ratio besides changes in the impurity concentration. The initial peak in concentration is due to a test device built into the layer. The layer is 1.4 μm thick and is relatively uniformly doped at approximately 1.5×10^{17} cm^{-3}. At the edge of the sample the the impurity concentration drops off slightly. This effect could be due to an increase in the Al content of the film near the edge. In an MOCVD reactor both the heat transfer and gas flow characteristics at the edge of the wafer are different than at the center. Thus, film uniformity could be degraded. For a process engineer trying to correct for these edge effects a SRBV instrument could assist him in making quick determinations of film uniformity as he optimized the process.

Our attempt to measure Si implants was unsuccessful. For a typical implant of 60 keV, the projected range in GaAs is .045 μm. This is too shallow a layer to be measured. The minimum thickness for a layer doped at 5×10^{17} is .8 μm. At this point applied Si implants can not be measured. It appears possible to measure high energy implanted layers however. The projected range for a 150 keV implant is 1.3 μm which falls in the measurement range. If the measurement is successful, it appears possible to study the activation efficiency of Si implants in various GaAs materials or under different annealing conditions.

Chapter 5

Summary and Conclusions

Measuring the spatially resolved breakdown voltage of a Schottky diode on a GaAs surface is a very basic technique which provides the researcher with quantitative information about three fundamental material properties: 1. Carrier type. 2. Net impurity concentration. 3. Spatial distribution of impurities. From these quantities, one can then calculate the spatial variation of the Fermi energy. Knowing these important electrical properties first can expedite a full characterization of the material. One can use the technique to choose appropriately doped portions of a crystal for study, analyze dopant incorporation rates during crystal growth, and monitor the uniformity of doping in epitaxial layers, to name a few applications. The technique is far too crude to be the mainstay of a research project (unless of course the project is building and analyzing the technique) but it can be a very informative supporting tool.

In this work we built and analyzed a SRBV instrument and then tested a variety of GaAs materials. Using the instrument to measure HB crystals grown from a silica boat, it was found that Si is continuously incorporated from the boat. Carbon boats were found to enhance the Si incorporation so that a HB crystal will switch from p to n–type. This is contrary to the expectation that the crystal would become increasingly p-type due to C contamination. In n-type LEC GaAs, a correlation was noted between dislocations and a donor defect.

The doping in MBE AlGaAs epitaxial layer was found to decrease at the edge of the wafer. These results on different types of GaAs material show that the technique has a broad range of applications.

The advantages of the technique are that it works on wide band gap III-V materials where standard four point probe techniques fail. It is a very quick measurement to make compared for example to spatially resolved Hall effect measurements. It is sensitive to concentrations of deep levels on the order of the background shallow level concentration regardless of charge state.

The disadvantages of SRBV are the limited range of impurity concentrations which can be measured, $5 \times 10^{14} - 5 \times 10^{17}$ cm^{-3}. Unfortunately, many applied GaAs materials fall outside this range. Semi-insulating substrates for direct implantation fall below this range, and conducting substrates are often above. The accuracy of the technique is not as high as Hall effect measurements. We estimate an error of 20%. When measuring epitaxial films, one is limited by the depletion width at breakdown, so that only relatively thick films, greater than 1 μm can be measured. There is no mobility information. The technique provides no information about the physical or chemical identity of the level either. Given these strengths and limitations it is apparent the technique must fit in as a complimentary tool in a characterization scheme. It would also be a useful instrument in a laboratory for quick conductivity checks of samples.

One possible commercial application for the instrument would be as a monitor for MOCVD processing. Since the technique involves gas flow over heated substrates, controlling film uniformity can be difficult. A SRBV instrument could be located near the CVD reactor to monitor the uniformity of films periodically. Since the technique is nondestructive (a light etch should clean any deposited metal on the surface), devices could be fabricated afterward and their performance could be correlated with material properties. Another application would

be for process engineers setting up a III-V pilot line. SRBV measurements could again determine film uniformities quickly while they adjusted gas flow and temperature parameters. Such a quick technique could reduce the set up time for the line.

Future research involving SRBV measurements could include characterization of special high energy, high dose Si implants. One can not measure the breakdown voltage of standard Si implants since the depletion width "punches through" the implanted layer. High energy would increase the depth of the implant and high dose would decrease the depletion width at breakdown. With this combination it might be possible to measure the breakdown of an implanted layer. If successful, the technique could be used to compare the activation efficiencies of Si implants in HB versus LEC materials. Another interesting study, using other techniques, would be to analyze the donor defect associated with dislocations in LEC GaAs. SRBV measurements will continue to be used to characterize in house HB and vertical Bridgman materials.

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