UNIVERSITY OF CALIFORNIA SAN DIEGO

Energy Efficient Integrated Circuits for Low Power Wireless Communication Applications

A dissertation submitted in partial satisfaction of the
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by

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The dissertation of Dhon-Gue Lee is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

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DEDICATION

To my mother.

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D.-G. Lee, P.P. Mercier, Noise Analysis of Phase-Demodulating Receivers Employing Super-Regenerative Amplification, *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 9, pp. 3299-3311, Sep. 2017.

D.-G. Lee and P.P. Mercier, A 1.65 mW PLL-free PSK Receiver Employing Super-regenerative Phase Sampling, in *Proc. IEEE Biomedical Circuits and Systems Conference*, Oct. 2015.

D.-G. Lee, L.G. Salem, P.P. Mercier, Narrowband Transmitters: Ultra-Low-Power Design, *IEEE Microwave Magazine*, vol. 16, no. 3, pp 130-142, Apr. 2015.*Invited paper*.

ABSTRACT OF THE DISSERTATION

Energy Efficient Integrated Circuits for Low Power Wireless Communication Applications

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Professor Patrick P. Mercier, Chair

Low-power wireless receiver design has been an active area of research during the last decade. One of the most difficult part of the design is generating a spectrally pure clock signal for demodulation in an energy efficient manner. The clock generation is usually done through either a phase-locked loop, and the energy cost of implementing a PLL is usually more power expensive than the the rest of the receiver. Therefore, the solutions thus far have been to use a simple modulation schemes such as On-Off-Keying(OOk). However, such modulation schemes are spectrally inefficient, and as the density of wireless devices grow larger, more stringent spectral efficiency will be demanded even for low-power applications. This dissertation presents a search for an alternative to an envelope-detector. We have investigated a PLL-less coherent detection, as well as an ultra-low power PLL for an alternative to an envelope detector. Chapter 1 describes the general link budget required for such low-power applications. Popular low-power receiver architectures are described in this chapter. Chapter 2 presents a PLL-

less receiver architecture that employs a super-regenerative oscillator as a phase storage element. The chapter details the system level and circuit design as well as the measurement results. Chapter 3 presents a mathematical model for super-regenerative reception of phase-modulated signal. The theoretical model needed to build the receiver presented in chapter 2 was not available at the time of the design. The authors investigated the behavior of super-regenerative receivers when it is used to receive phase-modulated signals employing modulations such as phase-shift-keying (PSK). Chapter 4 describes a low-power PLL architecture that is promising enough to meet both the power and the noise requirement of low-power wireless communication applications at 2.4 GHz. The in-band phase noise of sub-sampling PLL can approach the theoretical limit of the reference phase noise. However, SSPLL can suffer from a significant spurious tone. This chapter presents a sub-sampling PLL architecture that can lower the spurious tone significantly without relying on a power-expensive calibration scheme. Furthermore, the entire loop (except the oscillator) consumes less than 500 microwatts of power, and the total power consumption of the PLL is less than 1 mW, suitable for low-power wireless communication applications.

Chapter 1

Introduction

Recent advancements in integrated radio design have enabled many new applications ranging from wearable healthcare or fitness monitors to Internet of Things (IoT) devices, structural integrity monitors, and beyond. In many of these applications, device size and battery life are of critical importance. Since radios often consume a significant portion of the power budget in small sensing nodes [7], reducing radio power consumption can be an impactful way to effectively decrease device size or increase operational lifetime. Reducing radio power can, however, be challenging, as there are important tradeoffs between power consumption and performance metrics such as radiated output power, linearity, sensitivity, channelization capabilities, and interference sensitivity. Low-power radio designs often sacrifice one or more of these metrics in the pursuit of low overall power consumption. The purpose of this chapter is to briefly introduce the main challenges facing narrowband ultra-low-power (ULP) RX design.

1.1 Link Budgeting

Wireless sensor networks (WSN) and *body area networks* (BAN) are two common areas that generally require short-range ULP transceivers. The purpose of this section is to briefly review path loss models and link budgets for these representative applications to derive minimum required output power.

To come up with a general WSN link budget, consider a representative WSN system operating with a carrier frequency of 2.4 GHz at a communication distance of 10 m. Most WSN nodes operate in peer-to-peer ad-hoc networks, where each node can

potentially act as a relay between other nodes. Consequently, WSN transceivers must balance power specifications evenly between transmit and receive modes in order to optimize system-level energy efficiency. As a result, receivers are typically designed to have an input sensitivity close to -90 dBm. The minimum transmitter output power can then be calculated by preparing a link budget using the Friis equation for free space as a baseline case:

where λ is the carrier wavelength and D is the distance between nodes. This equation tells us that, in free space, a 10 m link suffers from 60 dB of path loss at 2450 MHz. A typical surface-mount antenna at 2450MHz has a gain of 0 dBi, which leads to the minimum transmit power of -30 dBm under ideal condition. However, a WSN transceiver working in a hostile environment could experience as much as 30 dB of additional loss, for a total of 90 dB of path loss [8]. Therefore, a WSN transmitter should have a maximum output power of 0 dBm, our definition of a ULP transmitter.

On the other hand, BAN applications have much lower transmission distances: 1-2 m is often sufficient to communicate information around the human body. This should theoretically result in a lower path loss than in WSNs: 40-46 dB in free space at 2.4 GHz. Unfortunately, the presence of the human body in BANs adds significant attenuation, resulting in a measured path loss that range from 40 to 80 dB [9]. As an added complication, this path loss is highly variable and depends not only on the carrier frequency and the distance between nodes, but also on the relative position of the body and its surrounding environment [9]. Fortunately, the frequency of this variation is limited by the response time of a human (hundreds of milliseconds), enabling relatively low-complexity automatic gain control loops to compensate for such variation. Additionally, while the channel itself has high losses, it can generally be modeled as a non-frequency selective channel with no resolvable multipath, eliminating the requirement for complex multipath cancellation schemes [10]. Other studies have shown slightly lower path loss results (by 10-15 dB) at 900 MHz and 400 MHz [11] as a result of lower tissue conductivity and higher relative permeability. Operating at these frequencies, however, reduces the radiation efficiency of electrically small antennas, which may negate the path loss

advantage when computing the system-level energy efficiency. As a result, there is no clear rule-of-thumb regarding carrier frequency selection in BANs, as the available size and location of the antenna affects this decision dramatically.

To calculate the generally required PA output power range in a BAN, we first exploit a natural property of the system: most BAN users will be wearing a smart-phone or smartwatch platform that is energy-rich, at least in comparison to a wearable or implantable sensor node. Thus, we can utilize these smart de-vices in an energy-asymmetric star topology network, where the smart watch/phone platform acts as a highly-sensitive centralized base-station. Assuming a base-station receiver sensitivity of -100 dBm, as typically encountered in commercial Bluetooth receivers, along with path loss of 40-80 dB and 10 dB link margin, the most efficient PA implementation would dynamically alter its output power between -10 dBm and -50 dBm depending on instantaneous channel conditions; -10 dBm is also the recommended transmit power according to IEEE802.15.6 BAN standard [12].

To put these number in perspective, recall that -10 dBm corresponds to 100 W output power. It is very challenging to design all downstream blocks to consume well under 100 W in order to limit the overall system power con-sumption. The rest of this chapter will thus review architectures and circuits that help address this problem.

1.2 Low Power RX Architectures

The power consumption of a receiver (RX) is highly influenced by the modulation scheme chosen, which then defines the overall receiver architecture. Receivers can be broadly categorized by the following demodulation schemes:

1. Clocked demodulation. Broadly, RF energy is first mixed down to a lower frequency (or two) before demodulation occurs. In general, a low-phase noise LO is desired, though not strictly required. This category can be further sub-categorized into the following architectures:

(a) Super-heterodyne/heterodyne RX. Although the traditional dual down-conversion architecture is extremely robust, as seen in Figure 1 it requires two LOs and an additional mixer and thus has difficulty achieving ULP operation. Section 1.3 discusses several techniques to minimize the power consumption in such architectures.

(b) Homodyne (zero-IF) RX. It is generally more energy-efficient to operate at baseband than at RF, and for this reason, homodyne architectures save power by directly down-converting the input signal to baseband. However, homodyne receivers are well-known to suffer from DC offsets, flicker noise, LO leakage, and other issues. Thus, low-power methods to address these issues are required, several of which are also discussed in Section 1.3.

2. Energy/Envelope detection. A PLL can be amongst the most power hungry blocks in ULP receivers, and as a result, receiver architectures that eliminate the requirement of a PLL can more easily achieve ULP operation. Eliminating the PLL, however, generally either reduces LO precision, making coherent demodulation difficult, or through high-Q resonators precludes multi-channel operation. Instead, it is possible to perform non-coherent demodulation by observing the signals energy level either directly at RF, or after down conversion to an imprecise intermediate frequency. Naturally, doing so relies on less spectrally efficiency modulation schemes (e.g., OOK), and has difficulty dealing with blockers. Section 1.4 describes methods to perform envelope/energy detection in more detail.

3. Super-regenerative receiver. A super-regenerative receiver (SRR) achieves ultra-high gain using a low-complexity unstable network in an efficient and controlled manner. While most SRRs indeed have envelope/energy detectors, SRRs have sufficiently different requirements to consider them separately. Section 1.5 describes the basic operation of a super-regenerative receiver and presents examples from the recent literature.

1.3 Clocked Modulator

The power consumption of a receiver is normally dominated by frequency synthesis, RF amplification, and the LO buffer. Although the dual down-conversion architecture is very robust for demodulating data while rejecting unwanted signals, the requirement of multiple down-conversion mixers and two reference signals is often prohibitively expensive from a power perspective in ULP applications. Consequently, low-IF and zero-IF architectures have gained popularity in ULP radio design due to their low implementation complexity (i.e., the minimal number of blocks that consume power). Image rejection problems associated with low-IF receiver architectures can be solved by using high-Q resonators as image rejection filters. Furthermore, certain low power standards, such as ZigBee, require very loose specifications of image rejection and channel filter [13], potentially saving implementation complexity, though at the expense of an increased chance of interference. Additional power can be saved by adopting simpler modulation schemes such as OOK, FSK, and low-index PSKs, though at the expense of reduce spectral efficiency. While such system-level simplifications can decrease power consumption, they may not be sufficient to meet ULP power budget constraints. Thus, efforts have been made to further lower the power consumption in such architectures by replacing a PLL with a clever method of frequency synthesis [1], [14], lowering the supply voltage [15], [16], [17], and replacing the LNA with a passive mixer front end [15].

Figure 1.1 shows an example of a representative FBAR-based multi-channel super-heterodyne receiver architecture [1]. Here, multi-channel operation has been achieved by first down-converting the whole channel band to a wideband IF (5 to 80 MHz), while using multiple frequency dividers driven by the resonator in order to define all necessary channels in the 2.4 GHz ISM band, as illustrated in Fig 9.

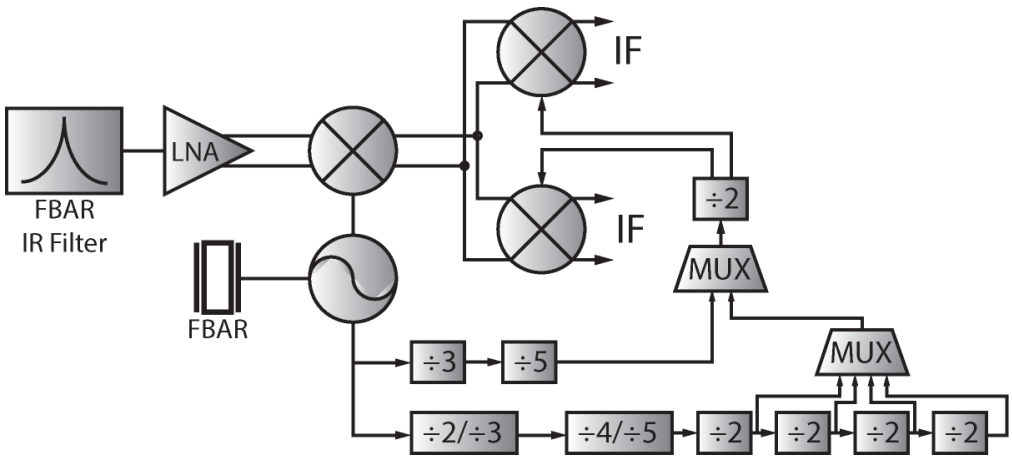


Figure 1.1: PLL-less FBAR-based Super-heterodyne RX schematics [1]

1.4 Energy/Envelope Detector-based RX

The high power consumption associated with coherent demodulation often steers designers to choose simpler non-coherent modulation scheme such as OOK or FSK at the cost of reduced spectral efficiency. Energy or envelope detector-based receiver architectures further save power consumption by removing the need for an accurate high frequency clock. The key difference between energy and envelope detection is whether using a self-mixer or an envelope detector, where the former implements an actual square operation.

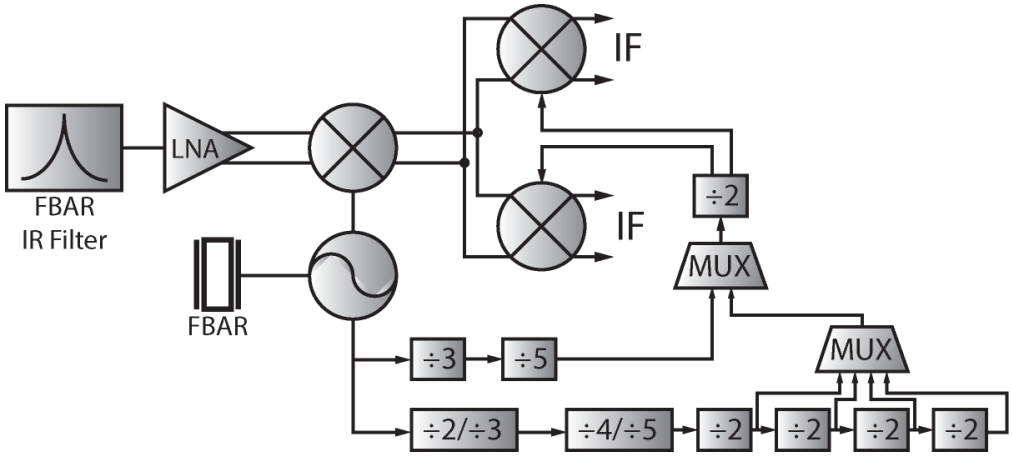


Figure 1.2: Schematics of envelope-detector-based RX frontend

Figure 1.2 shows a schematic of a generic envelope-detector-based receiver. Envelop and energy detectors generally offer extremely low-power operation compared to all other demodulators, though they suffer from poor blocker rejection and SNR due to translation of blockers to DC and minimum detectable signals set by non-linear elements. These problems can potentially be mitigated by using a 2-tone modulation scheme with a high-gain LNA [2], or by using an uncertain-IF architecture [18]. An example 2-tone receiver architecture is shown in Figure 1.3. Unlike a traditional envelope detector that down-converts any signal (potentially including interferers) to DC, in a 2-tone system the signal is transmitted at two separate frequencies with a known frequency offset, such that the intermodulation between these two signals lies at a known-IF, which can then be filtered and demodulated with substantial blocker rejection. The implementation in [2] uses the best phase-aligned LO signal amongst 8 phases in order to demodulate the signal without using a quadrature path.

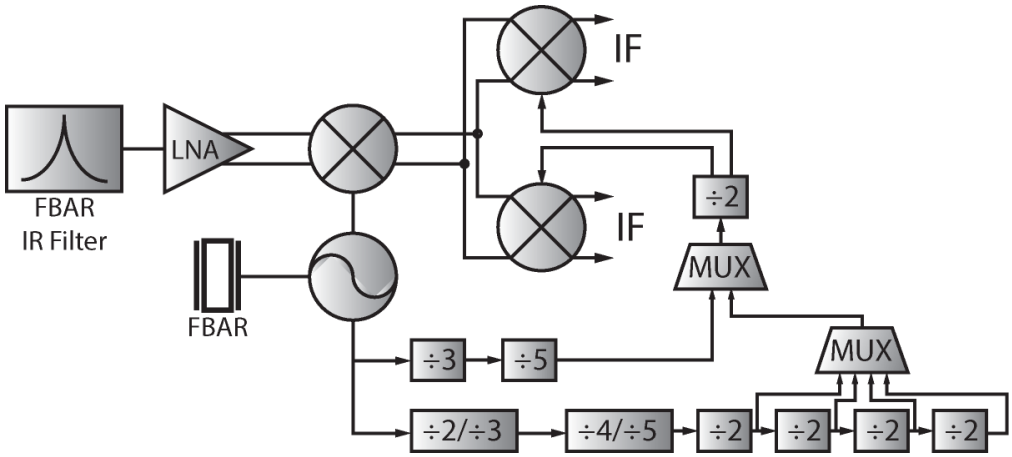


Figure 1.3: Schematics of 2-tone FSK receiver [2]

An uncertain-IF architecture utilizes an imprecise and thus power-efficient LO (e.g., a ring oscillator) to down-convert the desired signal to a wide, uncertain IF to take advantage of the large gain attainable at such frequencies. However, down-conversion introduces image, and a high-Q RF filter, such as bulk acoustic wave resonators (BAW), must be used as image rejection filters [18], which in some cases may be cost or area prohibitive.

1.5 Super-regenerative Receiver

Super-regenerative receivers (SRR) use an oscillator with a variable bias current to steer the two complex poles of the oscillator from the left half plane s-plane to the right half plane, effectively oscillating and quenching the system in a non-linear fashion. During the start-up of the super-regenerative oscillator (SRO), any small signal and noise in the vicinity of the oscillators natural frequency is exponentially amplified, thereby achieving enormous gain - much higher gain than an open loop amplifier. A representative SRR is shown in Figure 1.4. Most SRRs use an envelope detector to demodulate OOK or other amplitude modulated signals. Unlike other envelope-detector-based receivers, an SRR can have an arbitrarily large gain (limited by the quench period and power supply rail) and does not nominally suffer from an envelope detectors low detection threshold. While super-regenerative amplifiers achieve the largest gain-to-current ratio of any competing amplifier topology by exploiting the positive feedback growth characteristics of a building oscillation, any blocker in a nearby channel can force an oscillation independent of the presence of a signal at the desired band. Consequently, SRR architectures are very susceptible to blockers, and the susceptibility is inversely proportional to the rate at which the transconductance of the oscillator, or the quench signal, grows [19]. An effort has been made to mitigate this problem at the cost of additional complexity and data rate by calibrating the quench signal with a digital feedback loop as shown in Figure 1.4 [3].

1.6 Summary of dissertation

Ultra-low-power narrowband radios can open up many unique applications ranging from Internet-of-Things and industrial sensor networks, to wearable sensors, healthcare devices, and beyond. Achieving ultra-low-power con-sumption while maintaining robust operation involves difficult trade-offs be-tween output power, data rate, bandwidth, channel selectivity, sensitivity, and energy efficiency that must be overcome

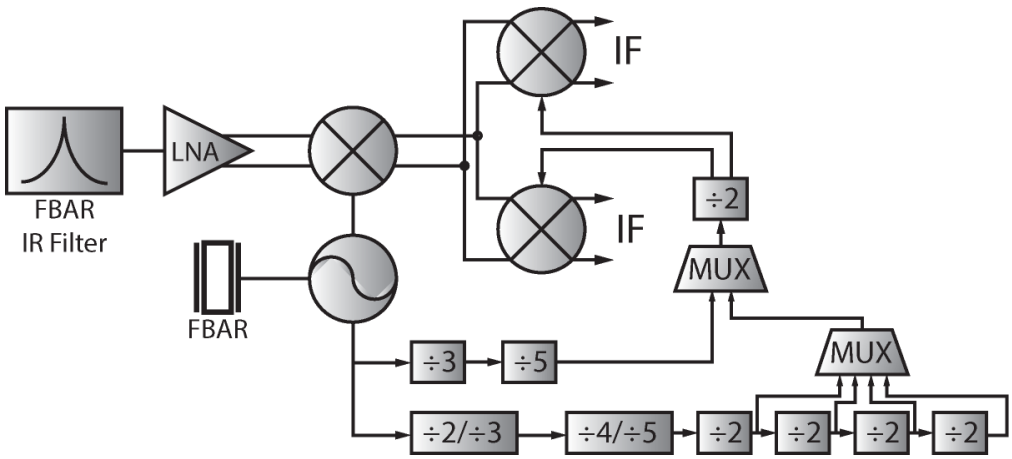


Figure 1.4: Schematics of super-regenerative receiver with BW calibration [3]

through a combination of innovative circuit design, novel architectures, and system-level considerations. This chapter has introduced typical architectures used in ULP radios, discussed their relative merits, and provided some benchmarking data to help identify what architectures might make the most sense given system-level specifications. While optimal implementations depend strongly on the given application, in general the most efficient radios employ low-complexity modulation schemes (e.g., OOK, FSK, and possibly BPSK), and are run by an efficient LO stabilized without a PLL.

This dissertation consists of two main parts. The first part of the dissertation focuses on super-regenerative receivers. In chapter 2, a novel way to use a super-regenerative amplifier as a phase storage device is presented. In chapter 3, a mathematical analysis of the noise behavior of the non-linear and time-variant system when SRAs are used to demodulate phase rather than amplitude is present to help analyze systems such as shown in chapter 2. In the second part of the dissertation, an energy-efficient way to build a PLL for low-power wireless communication is presented. Chapter 4 describes the analysis and design of a sub-sampling PLL architecture that reduces the reference spur without relying on PVT-sensitive techniques. Chapter 5 describes an improvement of the PLL architecture shown in chapter 4 that further reduces the spur by more than 15 dB in simulation.

1.7 Acknowledgement

Chapter 1, in part, is a reprint of the material as it appears in D. Lee and P.P. Mercier, ”Introduction to Ultra Low Power Transceiver Design,” in: P.P. Mercier and A. Chandrakasan , ”Ultra-Low-Power Short-Range Radios. Integrated Circuits and Systems.” Springer, 2015. The dissertation author is the primary author of this paper.

Chapter 2

A 1.65 mW PLL-free PSK Receiver Employing Super-regenerative Phase Sampling

Abstract - This chapter presents a 1.65 mW low-power receiver that uses a super-regenerative oscillator (SRO) to replace power hungry phase lock loops (PLLs) that are conventionally required for phase-demodulation. It is shown that operating an SRO in the amplification mode preserves the phase of incoming RF signals, and thus an SRO is used to periodically sample the phase of two incoming training bits, after which the SRO operates as a local oscillator for a super-heterodyne receiver. Operating at 0.5 V in a 0.18 m process, the receiver achieves -70 dBm of sensitivity at BER of 1e-3 when demodulating an 800 kbps BPSK signal without a PLL. .

2.1 Introduction

The growing interest in wearable health and fitness devices such as smartwatches and medical patches require low power wireless radios that can employ spectrally efficient modulation schemes. For example, a 128- electrode EEG system sampling at 1 kS/s with $>$16 bits of resolution has a raw data rate requirement of $>$2 Mbps. In the congested 2.4 GHz band, where channel bandwidths are limited to 1 MHz and interference with other standards should be avoided at all costs, modulation schemes such as PSKs and QAMs are required. While Bluetooth v2.0 support maximum data rate of 3 Mbps for π/4-DQPSK and 8-DPSK, the power consumption of such radios is large in

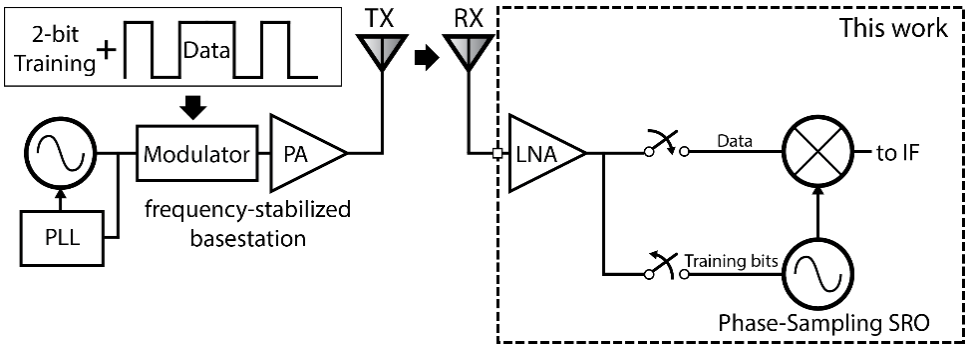


Figure 2.1: Overview of the proposed phase-sampling system.

part due to the requirement of a phase locked loop (PLL), which have difficulty scaling below 1 mW at 2.4 GHz [20], and further have long start-up times that make aggressive duty-cycling for low average power operation difficult.

On the other hand, most low power radios in the current literature only employ schemes such as OOK and FSK due to their low-complexity/low-power implementations [21]. Unfortunately, such low-order modulation schemes are spectrally inefficient and cannot support the high required data rates in the allocated channel bandwidths at 2.4 GHz. The next generation of wearable and medical applications must thus find a way to support higher order modulation schemes at low instantaneous power.

In this chapter, we propose a new PSK receiver architecture that can demodulate phase information without the use of a PLL, thereby enabling ultra-low-power operation. Here we exploit the fact that many wearable biomedical applications operate in an energy-asymmetric star network where a comparatively energy-rich basestation (e.g., smartphone) can easily afford a highly-accurate frequency synthesizer for its transmitter. Transmitted information is thus frequency-stabilized, which can be leveraged at the receiver for in-time calibration of a low-power LO. While prior work has exploited transmitted frequency-stabilized signals to periodically calibrate a PLL [22], the power and slow start-up drawbacks of PLLs remain.

2.2 Architecture Overview

To minimize power and enable rapid duty-cycling, the proposed architecture, shown in Fig. 2.1, utilizes a superregenerative oscillator (SRO) to first amplify two frequency-stabilized training symbols, and then transition to an oscillatory mode where the phase of the oscillator is matched to the incoming training symbols. At this point, the temporarily-stabilized SRO with known phase characteristics acts as an LO for a super-heterodyne receiver. Since the power consumption of an SRO is only marginally higher than a conventional VCO, and no frequency dividers, phase detectors, or loop filters are required, the power overhead of stabilizing the LO can be substantially reduced compared to prior-art.

Naturally, the SRO can only hold its sampled phase and frequency for so long, and thus n training symbols must be transmitted between every m data symbols. It has been shown that the frequency drift of a VCO can be minimized at 2.5 Hz/μs for a low-voltage multi-gigahertz design in modern CMOS processes [23], which is more than sufficient to demodulate upwards of $m = 8$ symbols of data at 1 MSps with $n = 2$. As opposed to a free-running oscillator, the phase sampling oscillator is periodically quenched to mitigate the effects of frequency drift and accumulated jitter, which typically limits D-BPSK systems to have m close to 8.

The phase-sampling receiver architecture, illustrated in Fig. 2.2, operates as follows. A low-noise amplifier (LNA) amplifies incoming RF energy at 2.2 GHz, and drives two time-sequenced buffers. During training, the path selection signal is low and the bottom buffer is turned on, mixing incoming RF energy with a 32 MHz reference to generate a 2.232 GHz signal that is injected into the phase-sampling SRO. The SROs bias current is then ramped-up via a linear quenching function, exploiting the positive-feedback properties of super-regenerative architectures to realize enormous gain. Figure 2.3 illustrates timing diagram of the control signals and the output of the SRO. Though SROs are generally used as high-gain blocks in non-coherent radios, it can be shown that an SRO preserves the phase information of a signal that is injected during the start-up

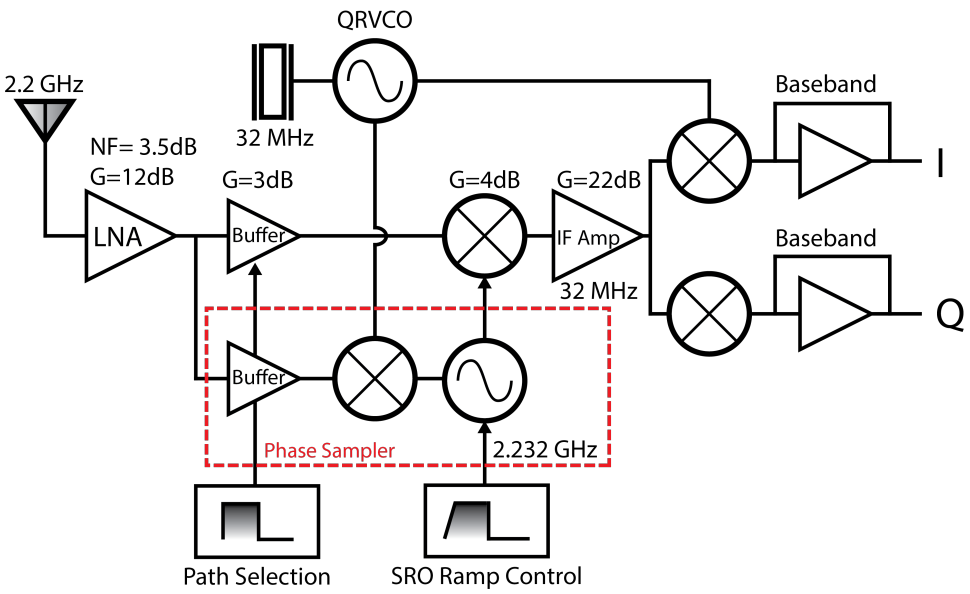


Figure 2.2: Block diagram of the phase-sampling receiver.

of oscillation, as illustrated by simulation results in Fig. 2.4. Thus, when the SROs bias current reaches its maximum value, the SRO enters an oscillatory mode that is phase matched to the incoming RF signal, mixed up by 32 MHz to avoid frequency-pulling.

Figure 2.5 shows the quality of phase sampling as a function of SNR over the bandwidth of the SRO. The bandwidth of the SRO is proportional to the slope of the ramp quenching function. An SNR greater than 13 dB is necessary for good quality phase sampling (i.e., this would result in BER of 1e-4 when demodulating a noiseless signal).

Once the phase of the injected signal is successfully sampled, training is complete and the path selection signal is asserted, turning off the SRO buffer and up-conversion mixer, thereby achieving 40 dB of isolation between the LNA and SRO while saving 0.3 mW of power. At this point, the top path is turned on and operated as a super-heterodyne receiver using the SRO as an LO. The quadrature mixer then enables demodulation of BPSK, QPSK, and QAM signals. Once all data symbols following the training symbols are demodulated, the SRO is quenched, and new training symbols are sampled. Figure 2.6 shows that the number of errors begins to rise 8-10 symbols after

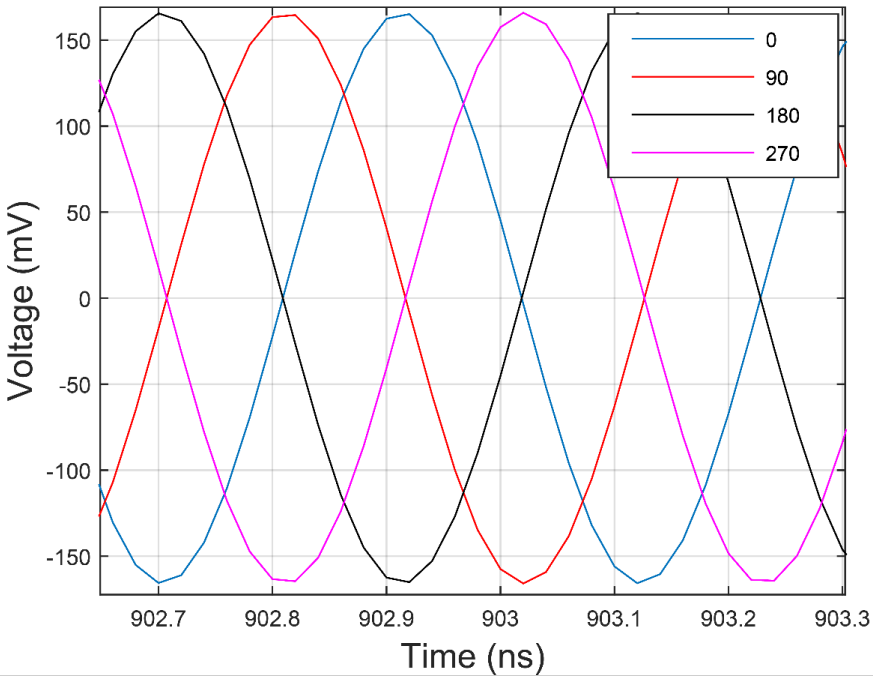


Figure 2.3: Simulation result of phase sampling SROs output waveform given 100 nA inputs of 4 different phases.

the training symbols. Thus, in this work the system is quenched after demodulating $m = 8$ symbols.

2.3 Circuit Implementation

2.3.1 LNA, RF buffers, and down-conversion mixer

A singled-ended inductively degenerated common source LNA and a single-balanced active mixer are employed for their low power consumption. The LNAs simulated noise figure is 3.8 dB. Schematics are shown in Fig. 2.7. The gate, source, and load inductors are all implemented with on-chip inductors. The LNA is followed by two parallel cascode RF buffers used to isolate the output of the LNA from frequency pulling the SRO. As mentioned previously, only one of the two buffers is turned on at all times in order to provide maximum isolation and minimum power consumption.

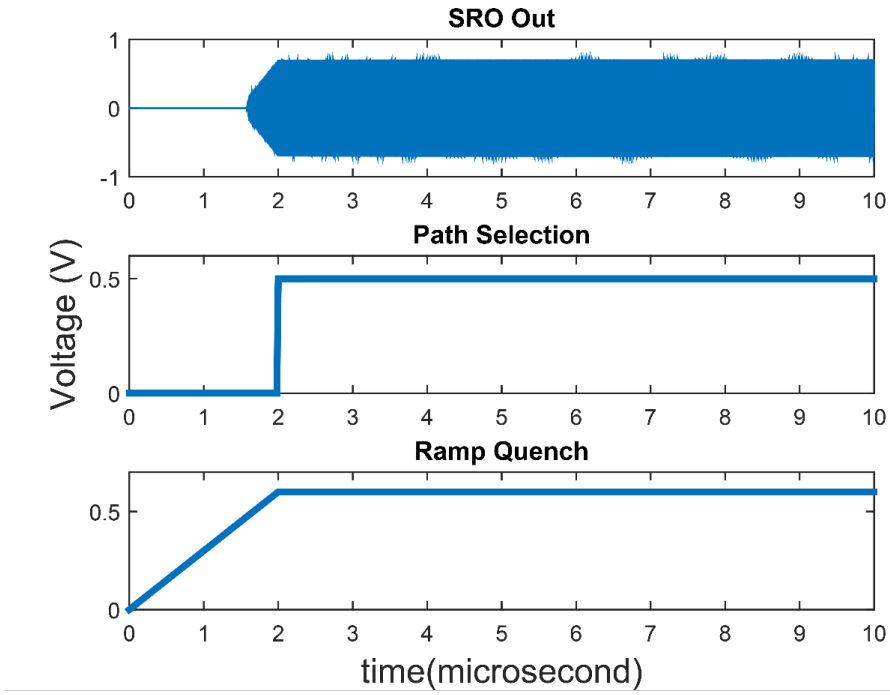


Figure 2.4: Timing diagram of control signals and the output of the SRO .

2.3.2 SRO and Up-conversion Mixer

Figure 2.8 shows the circuit implementation of the SRO and its preceding up-conversion mixer. The periodic ramp function is input into the NMOS current bias transistor to control the SROs bandwidth and quenching rate. A 13-bit digital capacitor bank is used to tune the center frequency of the oscillator across approximately 100 MHz of bandwidth. A switch-capacitor-based digital capacitor bank is used to implement the 9 LSBs [24]. In order to save power, the mixers LO is grounded through a digital MUX during the demodulation phase and is only turned on while sampling the phase.

2.4 Experimental Results

The phase-sampling receiver was implemented in 0.18 μm CMOS SOI process and measured in a Quad Flat Noleads (QFN) package; a die photo is shown in Fig. 2.9. RF performance was characterized by inputting a pseudorandom data sequence into the

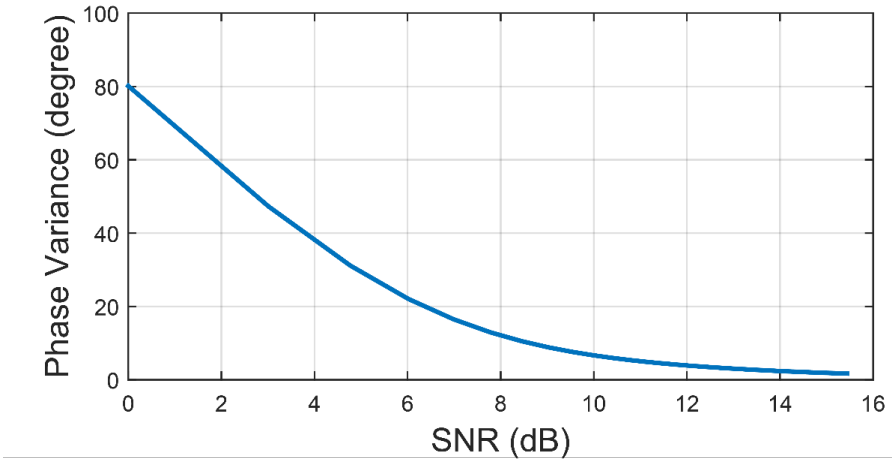


Figure 2.5: Simulated phase variance versus SNR of the SRO.

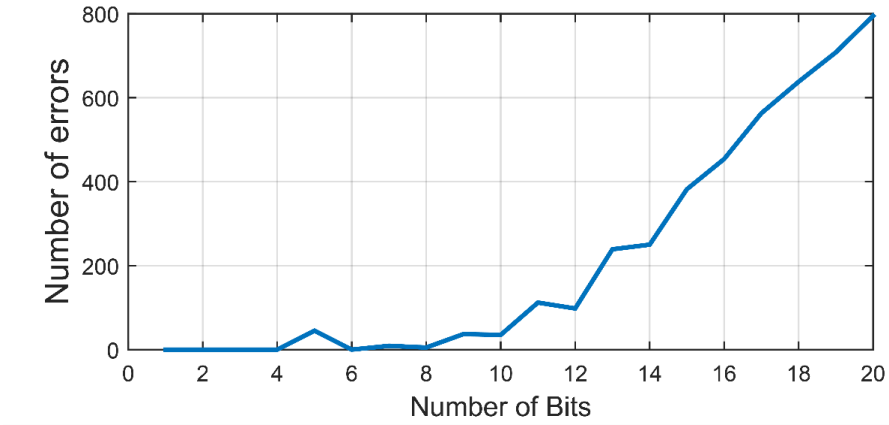


Figure 2.6: Measured number of errors for each bit after the training bit.

chip using a vector signal generator at 2.2 GHz. Due to unintended layout mismatch of the quadrature oscillator, Q channel data was not available during measurement of the fabricated chip. Consequently, while the receiver was intended for demodulating QPSK signals, only BPSK demodulation was tested in this prototype.

The transient waveform of the I-channel during BPSK demodulation is shown in Fig. 2.10. After two symbol periods, the phase is sampled onto SRO, and 8 symbols are subsequently demodulated. The SRO is then quenched after demodulation, and a new 10-symbol cycle is started. Each cycle is 10 microsecond, so that the effective data rate is 800 kbps.

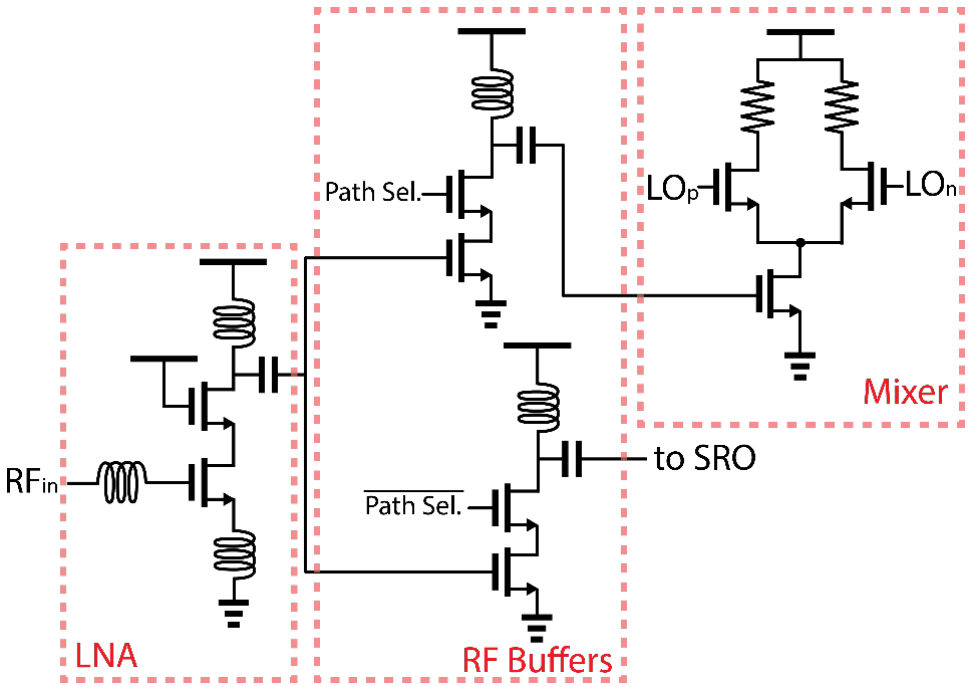


Figure 2.7: Schematics of LNA, RF buffers, and active down-conversion mixer.

The measured BER versus input power is shown in Fig. 2.11, illustrating a -70 dBm sensitivity. Due to a higher than expected parasitics, the super-regenerative oscillator operated at 2.2 GHz instead of its optimal frequency of 2.4 GHz. Consequently, the rest of the RF blocks operated at 2.2 GHz, which led to a degradation in sensitivity due to operation beyond the nominal bandwidth of the designed amplifiers. In order to compensate for the reduced gain, which according to simulations is 6.58 dB away from the nominal tuning range, the power of the LNA and RF was increased: instead of 500 μW, the LNA and RF buffers together consumed 1.22 mW in measurement to increase the gain of the LNA by approximately 6 dB. The baseband circuitry consumed 0.2 mW while the phase sampling SRO consumed 0.41 mW. Digital circuits consume 29.5 μW. The performances of the phase-sampling SRO receiver are summarized and compared to prior-art in Table 2.1. Even though the gain was degraded via frequency mismatch and power was increased to compensate, the chip still achieves performance comparable to, and in some cases exceeding, prior-art, thereby demonstrating that a phase-sampling SRO can be used as a low power alternative to a PLL for coherent detection while con-

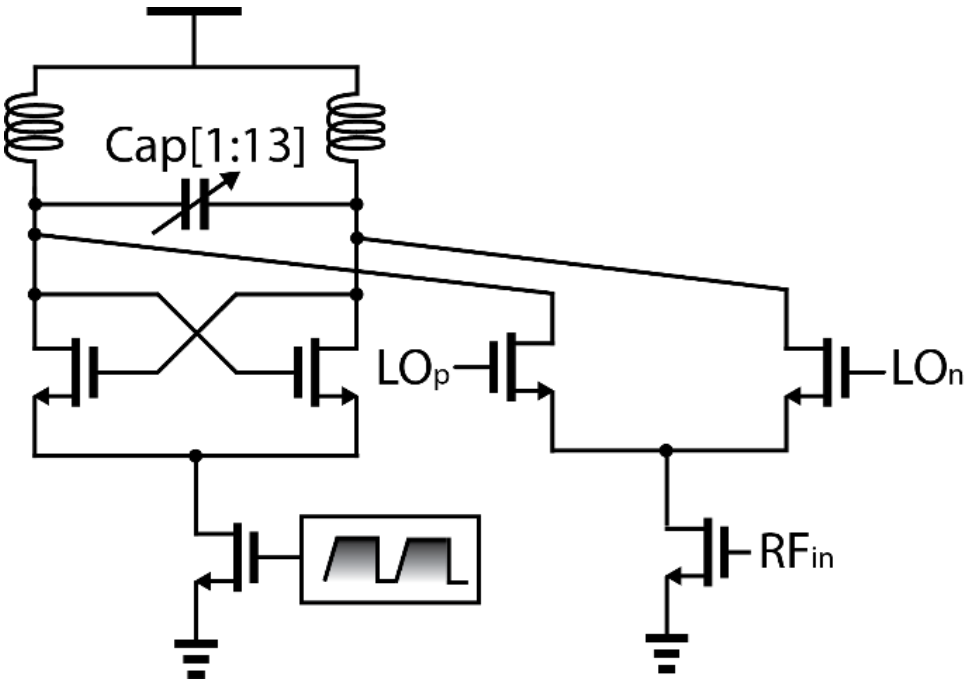


Figure 2.8: Schematics of the SRO (left) and the up-conversion mixer (right).

suming less power.

2.5 Acknowledgement

Chapter 2, in part, is a reprint of the material as it appears in D. Lee and P. P. Mercier, ”A 1.65 mW PLL-free PSK receiver employing super-regenerative phase sampling,” 2015 IEEE Biomedical Circuits and Systems Conference (BioCAS), Atlanta, GA, 2015, pp. 1-4. The dissertation author was the primary author of this paper.

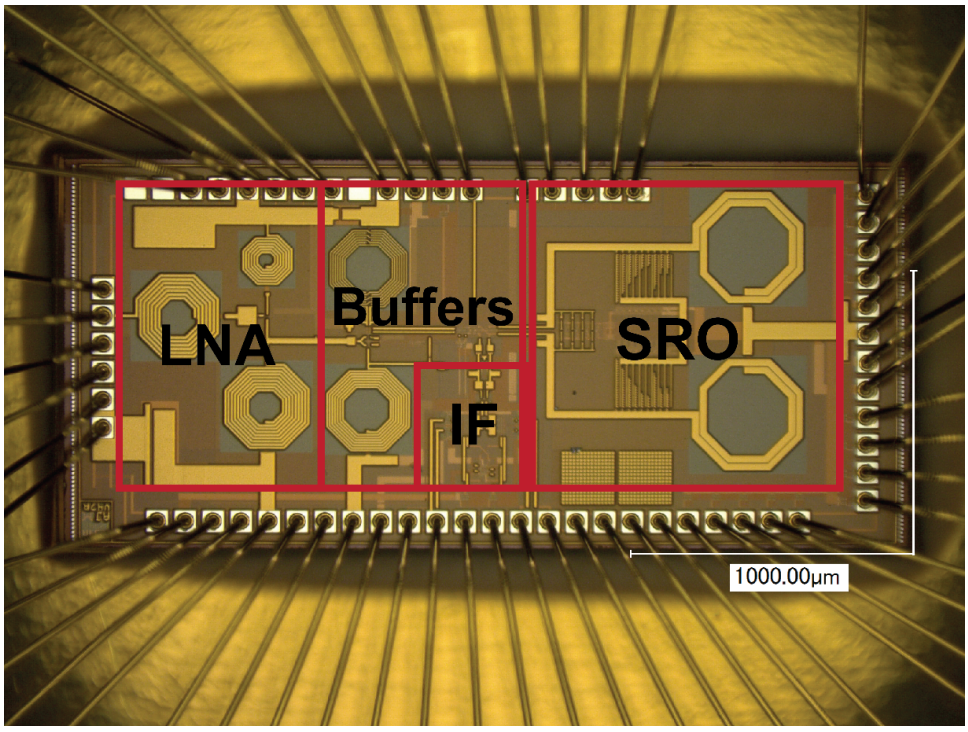


Figure 2.9: Chip microphotography of the receiver.

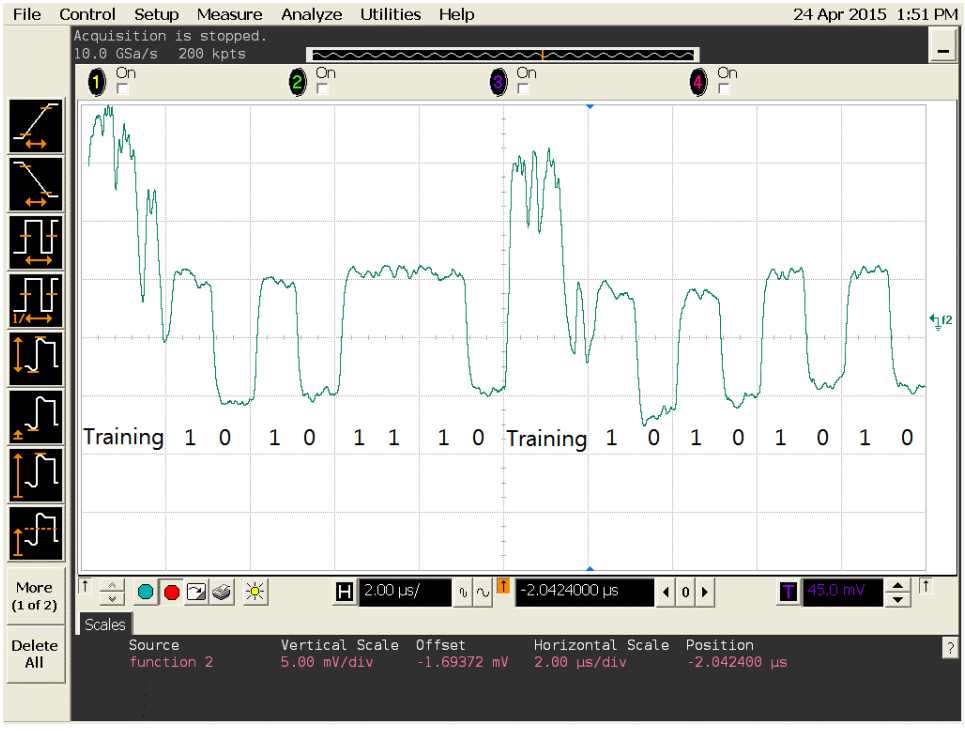


Figure 2.10: Transient waveform of the receivers I channel output.

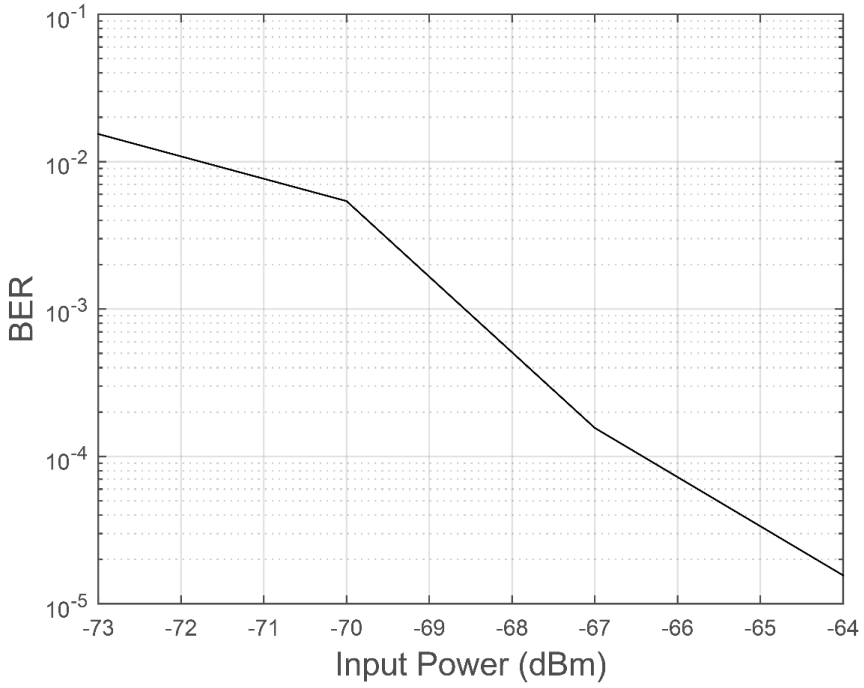


Figure 2.11: Measured Input Power versus BER

Table 2.1: Table to test captions and labels

Comparison of the Measured Performance of Low Power Receivers				
	TCAS '12 [25]	ISSCC [26] '11	ISSCC'14 [27]	This Work
Technology	0.18 μm	90 nm	90nm	0.18 μm
Sensitivity (dBm)	-65	-75	-92	-70
Data Rate (kbps)	1000	5000	2000	800
Architecture	Carrier Recovery Loop	Super-regenerative Receiver	Sliding-IF Phase-to-Digital	Phase-Sampling SRO
Total Power	20.4 mW @ 1.8 V	0.534mW @ 1.2 V	2.4 mW @ 1 V	1.6 mW @ 0.5 V
PLL Power	None	1.098 mW	0.550 mW	None
Receiver Power	20.4 mW	0.534 mW	1.85 mW	1.6 mW
Modulation	QPSK	OOK	HS-OQPSK	DBPSK
Energy-per-bit	20.4 nJ/b	0.1 nJ/b	1.2 nJ/b	2 nJ/b
PLL	None	For Calibration	Yes	None

Chapter 3

Noise Analysis of Phase-Demodulating Receivers Employing Super-Regenerative Amplification

Abstract - Growing interest in ultra-low-power RF receivers has reinvigorated research in super-regenerative amplifier (SRA) architectures, in part due to their ability to achieve enormous gain at very low power. Conventionally, SRAs have been paired with envelop detectors that demodulate amplitude-modulated signals (e.g., OOK); mathematical models have been developed to predict the performance of such systems. Since modern communication applications require more spectrally-efficiency modulation schemes, this chapter develops a mathematical model that predicts the stochastic behavior of SRAs when used in phase-demodulating receivers. This stochastic model is then used to predict the sensitivity of a phase-demodulating receiver employing a Colpitts-based SRA. Results from the developed model are validated with measurements of a discrete prototype, illustrating that SRAs can be used with I/Q mixing to demodulate quadrature phase-shift keying (QPSK) signals with -88 dBm sensitivity when the SRA consumes 1.2 mA at 1.5 V at 45 MHz.

3.1 Introduction

Super-regenerative amplifier (SRAs) are known to have excellent gain and sensitivity while consuming minimal DC power. Invented by Armstrong in 1922 [28], super-regenerative radio frequency (RF) receivers were briefly popular due in part to their

ability to achieve large gain from a single active element. Until the superheterodyne architecture supplanted SRA-based receivers due to their superior channel selectivity and limited self-radiation, SRAs were conventionally deployed with envelope detectors to demodulate amplitude modulation (AM) signals. The recent demand for low-cost and low-power wireless communication systems has re-energized research and development of SRA-based receivers for the same reasons they were popular in the early 1900s: their ability to attain large gain and high sensitivity at low power. However, most modern designs employ SRAs in essentially the same way they were employed in the 1920s: as a high-gain RF amplifier, followed by envelope detection of amplitude-modulated signals such as on-off keying (OOK) [19, 29–33].

Interestingly, there is no fundamental reason why SRAs can only be used along with amplitude demodulation hardware like envelope detectors. In fact, recent work has shown that SRAs can be used in receivers that demodulate frequency shift keying (FSK) signals [34, 35] or phase shift keying (PSK) signals with a conventional I/Q architecture as depicted in Figure 3.1 [36–39]. This is an important development, as many emerging wireless applications require communication with higher-order modulation schemes such as PSK and quadrature amplitude modulation (QAM) schemes. However, while the general theory of super-regenerative reception of OOK has been well analyzed in [18] and augmented in [40] and [41], noise analysis of SRAs in phase demodulating receivers has not yet been presented in the literature.

As a result, the primary purpose of this chapter is to present and experimentally verify a mathematical model of the noise performance of SRAs when used in phase demodulating systems. Leveraging either a conventional frequency-domain stochastic model [40], or a new time-domain stochastic model developed in Appendix A of this chapter, it is shown that the output noise of an SRA can be translated into the variance of the output phase by deriving the probability density function of the phase of the output waveform. The probability density function is then used to find the relationship between the noise figure of an SRA and the bit error rate when used with an m-ary PSK demodulator. Lastly, a discrete prototype of an SRA based on a Colpitts oscillator is

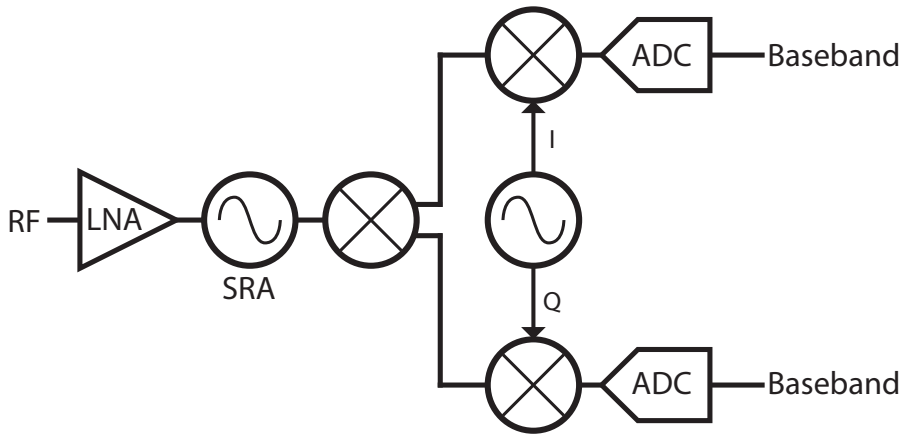


Figure 3.1: A representative PSK receiver architecture employing super-regenerative amplification.

designed in order to validate the theoretical model with experimental results.

The chapter is organized as follows. Section II briefly summarizes the general theory of super-regenerative reception [18] and the result of frequency-domain sensitivity analysis [40]. Section III leverages this prior analysis to develop a model that predicts output phase variance, which is then used to perform sensitivity analysis of QPSK reception. Section IV considers the design of a discrete SRA that can be employed in phase-demodulating receivers, while Section V presents the testbench and measurement result used to validate the developed theoretical work.

The analysis presented in this chapter, along with prior work on this topic, assumes that noise sources in SRAs are time-invariant. Since this is not actually true, this chapter also includes the development of a new time domain model that enables inclusion of time-varying noise sources. This new model is presented in Appendix A, and shows that the time-invariant assumption is indeed satisfactory for most practical data rates.

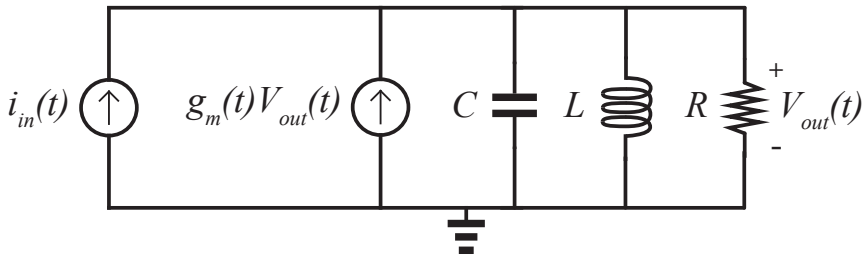


Figure 3.2: One port oscillator circuit model of SRAs.

3.2 Overview of General Super-Regenerative Theory

Much of the work presented in this chapter require a basic understanding of existing SRA theory [18, 40]. The primary purpose of this section is to briefly overview general SRA theory and notation that will be used in later sections.

3.2.1 One Port Oscillator Model

A super-regenerative amplifier is, at its core, an oscillator that is periodically switched on and off between a high-gain start-up phase and a steady-state oscillatory phase. An example of a single-port RLC model is shown in Figure 3.2, with a time-varying transconductance $g_m(t)$ modeling an active element that periodically turns on and off.

The typical behavior of an SRA is illustrated in Figure 3.3. During a single bit period, $g_m(t)$ is gracefully modulated from a value below $1/R$, where no oscillations should occur, to a value above $1/R$, where oscillations should occur at steady state. This modulation is typically described by a *damping function*, $\zeta(t)$. In this chapter a ramp damping function is used throughout, and is given by:

$$\zeta(t) = \zeta_0(1 - g_m(t)R), \tag{3.1}$$

where ζ_0 is the *quiescent damping factor*. When the damping function crosses zero, the

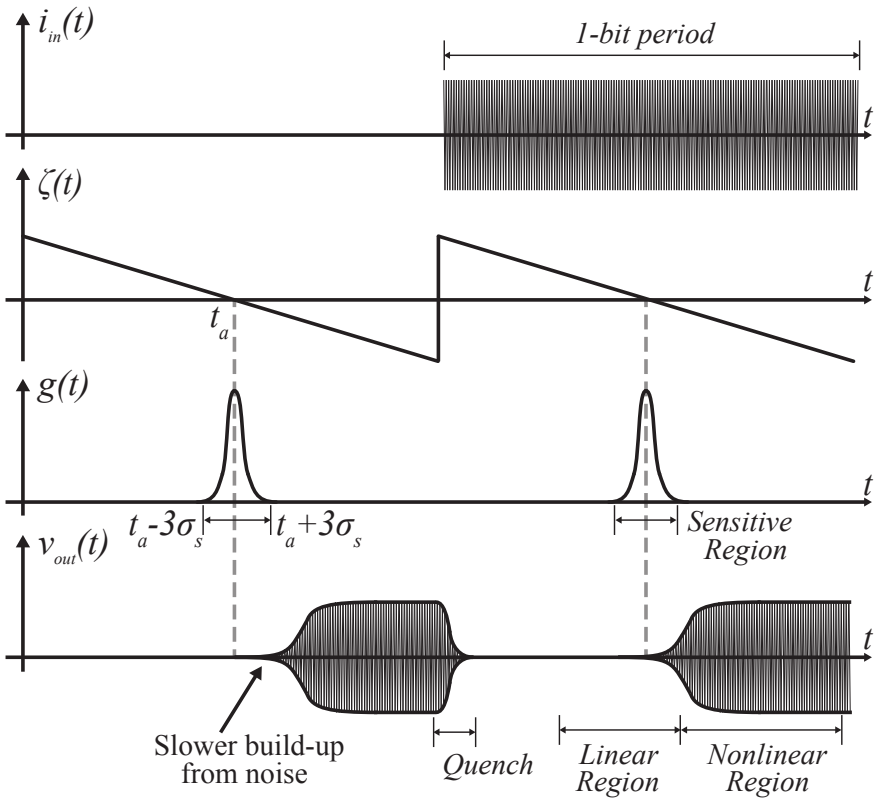


Figure 3.3: Illustration of the operation of an SRA.

amplifier becomes unstable, and its output envelope grows exponentially until it reaches non-linear compression and, eventually, steady-state oscillation.

For a critical period of time around the zero crossing of $\zeta(t)$, the SRA coherently responds to the input RF waveform, serving as a high-gain amplifier. Thus, if an RF signal is present, the input will help excite resonance, serving to build up oscillation quickly. If no RF signal is present, non-coherent noise is responsible for activating oscillation, which is a process that takes longer. RF amplitude information is thus measured by the time it takes to initiate oscillation. Once the oscillation is well established, the SRA no longer strongly responds to changes in input signal, and thus the SRA is rapidly quenched.

3.2.2 Solution of the Differential Equation for the Linear and Time-Variant Model

SRAs can generally be operated in one of two modes: $linear$ or $logarithmic$ [18, 40, 42]. When the output of an SRA remains small enough throughout each quench cycle to not be compressed, the SRA is said to be in linear mode. If the SRA output is left on long enough to the point of compression, the SRA is said to be in the logarithmic mode. Fortunately, it has been shown that, when ignoring noise, the phase of the output is nominally preserved in either mode of operation [41]. Since this chapter is focused on using SRAs in phase demodulating receivers, it is thus reasonable to assume a linear and time-variant SRA model without a loss of generality. It is worth noting, however, that non-linearity in the system may cause non-constant envelope signals to affect the output phase slightly. However, the nature of non-constant input power is usually not random (and often changes more slowly than the data rate of the radio), and can be calibrated by a separate circuit if there is a need.

A 2^{nd} order differential equation describes the linear time-variant one-port oscillator model in Figure 3.2:

$$v_{out}^{''}(t) + 2\zeta(t)\omega_0 v_{out}^{'}(t) + \omega_0^2 v_{out}(t) = 2R\zeta_0\omega_0 i_{in}^{'}(t). \tag{3.2}$$

The solution to the differential equation is given in [18, 40] as:

$$v_{out}(t) = Z_0\mu(t)k(t), \tag{3.3}$$

where $\mu(t)$ and *k(t)* are the *SRA gain* and the *filtering* term respectively, which are described as follows:

$$\mu(t) = e^{-\omega_0 \int_{t_0}^{t} \zeta(\lambda)d\lambda} \tag{3.4}$$

$$g(t) = \mu(t)^{-1} = e^{\omega_0 \int_{t_0}^{t} \zeta(\lambda)d\lambda} \tag{3.5}$$

$$k(t) = \int_{t_0}^{t} i_{in}^{'}(\tau) g(\tau) sin[\omega_0(t-\tau)] d\tau. \tag{3.6}$$

In this case, time t is defined to be zero at the zero crossing of $\zeta(t)$ and t_0 is the initial time of a symbol period.

The reciprocal of SRA gain is termed the *sensitivity function*, $g(t)$, which is only measurably non-zero during a finite window of time near the zero-crossing of $\zeta(t)$. The SRA is only sensitive to the input signal during the period of time when $g(t)$ is large.

Note that $k(t)$ is the only portion of the output, $v_{out}(t)$, that is a function of the input current, whereas the SRA gain $\mu(t)$ is determined only by the circuit parameters and is independent of input current. For this reason, $\mu(t)$ can be neglected during SRA noise analysis.

If the damping function $\zeta(t)$ is a linear ramp function such that:

$$\zeta_{ramp}(t) = -\beta t, \tag{3.7}$$

then the SRA gain and the sensitivity function can be described as follows:

$$\mu_{ramp}(t) = e^{\omega_0 \int_{t_0}^{t} \beta\lambda \, d\lambda} = e^{\frac{t^2}{2\sigma_s^2}} \tag{3.8}$$

$$g_{ramp}(t) = e^{-\omega_0 \int_{t_0}^{t} \beta\lambda \, d\lambda} = e^{-\frac{t^2}{2\sigma_s^2}}, \tag{3.9}$$

where σ_s is the *SRA time constant*. Here, $g(t)$ approaches its peak value as the $\zeta(t)$ tends to zero.

3.2.3 Frequency Domain SRA Noise Model

The output of an SRA is typically sampled when sufficient time has passed from the sensitivity window in order to benefit from the exponential growth of voltage waveform. Therefore, the filtering term $k(t)$ in (3.6) can be approximated by the following convolution:

$$k(t) \approx \int_{-\infty}^{\infty} i_{in}^{'}(\tau) g(\tau) sin[\omega_0(t-\tau)] d\tau, \tag{3.10}$$

or

$$k(t) \approx x(t) * sin[\omega_0 t], \tag{3.11}$$

where

$$x(t) = i_{in}^{'}(t) g(t). \tag{3.12}$$

The output voltage under this approximation is given by:

$$v_0(t) = Z_0 \mu(t) |X(\omega_0)| sin(\omega_0 t + \angle X(\omega_0)), \tag{3.13}$$

where $X(\omega)$ is a Fourier transform of $x(t)$.

The convolution approximation of the SRA model makes it easy to analyze its response to noise in the frequency domain. If the input to the SRA is additive white Gaussian noise (AWGN) with the power spectral density (PSD)

$$I_n(\omega) = \frac{N}{2}, \tag{3.14}$$

then according to (3.12), $x(t)$ is a convolution of the derivative of the input noise and the sensitivity function $g(t)$. The Fourier transform of $x(t)$ is then:

$$\overline{|X(\omega)|^2} = \frac{N\omega^2}{4\pi} * |G(\omega)|^2. \tag{3.15}$$

The overline in (3.15) means *expected value* since $X(\omega)$ is a random variable in this example. If we assume a ramp damping function, then the convolution above, evaluated at ω_0, is given by:

$$\overline{|X(\omega_0)|^2} = \sigma_X^2 = \frac{1}{2} N \omega_0^2 \sigma_s \sqrt{\pi}, \tag{3.16}$$

where σ_X^2 is the variance of random process $X(\omega)$.

The preceding analysis assumed that the noise in the SRA is AWGN with con-

stant single side band power density N_0. In practice, however, a portion of noise injected into the SRA's resonant tank is actually time variant: as the damping function $\zeta(t)$, and thus the transconductance, changes with time, the noise of the active device, typically implemented with a single transistor, changes as well. The frequency domain model presented here and in [40] is not suitable to include time-varying noise sources. Thus, a time-invariant noise source, whose value is computed by the minimum transconductance necessary to enable oscillation, is typically included in such analysis, though mathematical justification for such an assumption has not been previously given. The interested reader can refer to Appendix A, which introduces a new time domain SRA model that enables inclusion of time-varying noise sources in order to quantify over what range of practical implementation parameters this assumption is reasonable.

3.3 Sensitivity Analysis of a PSK SRA

This section develops a stochastic model that enables prediction of the sensitivity of an SRA used in an m-ary PSK demodulating receiver. Since the analysis presented in Appendix A shows that the effect of time variant noise is negligible as long as the data rate is sufficiently small compared to the carrier frequency, which is true in many ramp-damped SRO systems, the analysis presented in this section utilizes the output variance computed in (3.16). Designers interested in wideband systems can follow the same analysis presented below, though starting from (3.84) instead.

3.3.1 Derivation of the probability density function of output phase

The output of an SRA used in a phase demodulating receiver is often sampled when the SRA reaches a stable oscillation in order to benefit from the large gain of the regenerative amplifier. Fortunately, the output phase of the SRA is preserved as the SRA transitions from linear mode to logarithmic mode, and to a stable oscillation

[39, 41]. Therefore, analysis of phase uncertainty in linear mode is valid for all modes of operation.

When the input to the system is a sum of a deterministic input, $i_{i,signal}(t)$, and non-deterministic noise, $i_{i,noise}(t)$, then the output can be given by:

$$v_{out}(t) = v_{o,signal}(t) + v_{o,noise}(t), \tag{3.17}$$

where $v_{o,signal}(t)$ and $v_{o,noise}(t)$ are outputs due to $i_{i,signal}(t)$ and $i_{i,noise}(t)$, respectively. The amplitude of this equation is only valid in the linear region of the SRA.

To ease further analysis, define Z as a complex random variable that represents the value of $v_{out}(t_0)$ at time t_0 when enough time has passed such that the sensitivity function $g(t)$ is practically zero, and yet, the magnitude of the output is sufficiently small for the system to still be linear. When the input is AWGN only, the phase of the output at t_0 should be uniformly distributed from $-\pi$ to π. Therefore, if Z is written as a sum of its vector component X and Y, such that $Z = X + jY$, the variance of X and Y must be the same. Thus, $X \sim N(x_0, \sigma^2)$ and $Y \sim N(y_0, \sigma^2)$, and the variance σ^2 of X and Y is related to the variance σ_k^2 of Z in the following manner: $\sigma_k^2 = 2\sigma^2$. The mean of X and Y, x_0 and y_0, are the vector components of the output due to signal, $v_{o,signal}$.

Now, with a convenient mathematical model defined, the the probability density function of the phase of $v_{out}(t_0)$ can be derived. The magnitude and phase of the random variable Z are then defined by the following, as illustrated in Figure 3.4:

$$R = \sqrt{X^2 + Y^2}, \tag{3.18}$$

and

$$\Theta = \tan^{-1}(\frac{Y}{X}). \tag{3.19}$$

From this model, the pdf of Θ represents the output phase of the SRA. Random variables X and Y can be expressed in terms of Θ and R:

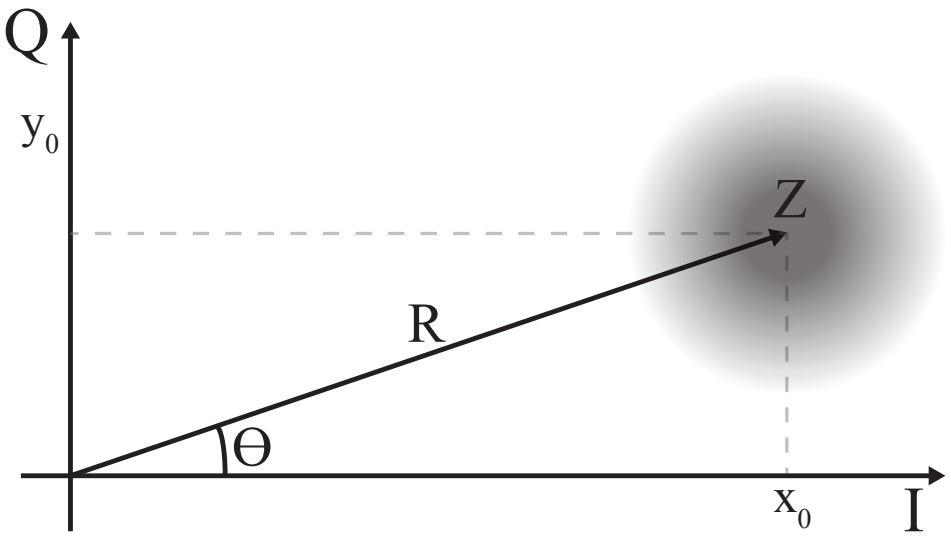


Figure 3.4: Illustration of the random variables in the constellation diagram.

$$X = R\cos(\Theta), \tag{3.20}$$

$$Y = R\sin(\Theta). \tag{3.21}$$

The joint pdf of R and Θ can be expressed as:

$$f_{R,\Theta}(r,\theta) = f_{X,Y}(R\cos(\Theta), R\sin(\Theta))|\Im(r,\theta)|. \tag{3.22}$$

$\Im(r,\theta)$ is the Jacobian of the transformation such that

$$\Im(r,\theta) = det\begin{bmatrix} \frac{\partial x}{\partial r} & \frac{\partial x}{\partial \theta} \\ \frac{\partial y}{\partial r} & \frac{\partial y}{\partial \theta} \end{bmatrix} = det\begin{bmatrix} \cos(\theta) & -r\sin(\theta) \\ \sin(\theta) & r\cos(\theta) \end{bmatrix} = r \tag{3.23}$$

Then the joint pdf of X and Y in (3.22) can be expressed as

$$f_{X,Y}(r\cos(\theta), r\sin(\theta)) = \frac{1}{\sigma^2 2\pi} e^{-\frac{(r\cos(\theta)-x_0)^2+(r\sin(\theta)-y_0)^2}{2\sigma^2}} \tag{3.24}$$

Substituting (3.24) into (3.22) results in:

$$f_{R,\Theta}(r,\theta) = \frac{r}{\sigma^2 2\pi} e^{-\frac{(r\cos(\theta)-x_0)^2+(r\sin(\theta)-y_0)^2}{2\sigma^2}}. \tag{3.25}$$

The terms with r and θ can be separated such that

$$f_{R,\Theta}(r,\theta) = \frac{r}{\sigma^2 2\pi} e^{-\frac{r^2+v_s^2}{2\sigma^2}} e^{\frac{r(x_0\cos(\theta)+y_0\sin(\theta))}{\sigma^2}}, \tag{3.26}$$

where $v_s^2 = x_0^2 + y_0^2$ is the output power due to the deterministic input signal. Lastly, integrating (3.26) with respect to R results in the following expression for the marginal pdf of Θ:

$$f_\Theta(\theta) = \frac{1}{\sigma^2 2\pi} \int_0^\infty r e^{-\frac{r^2+v_s^2}{2\sigma^2}} e^{\frac{r(x_0\cos(\theta)+y_0\sin(\theta))}{\sigma^2}} dr. \tag{3.27}$$

From this, the output SNR can be defined by taking the ratio of signal power to noise power as:

$$SNR_{out} = \frac{v_s^2}{\sigma_k^2} = \frac{v_s^2}{2\sigma^2}. \tag{3.28}$$

Note that (3.27) is no longer Gaussian, which is expected as the probability density function is defined from $-\pi$ to π in Radians, and is uniformly distributed when the SNR is zero (i.e., no signal is present).

While (3.27) has no closed form solution, it can be further simplified:

$$f_\Theta(\theta) = \frac{A(\theta)}{\sqrt{2\pi}\sigma} e^{\frac{A(\theta)^2-v_s^2}{2\sigma^2}} Q(-\frac{A(\theta)}{\sigma}) + \frac{1}{2\pi} e^{-\frac{v_s^2}{2\sigma^2}}, \tag{3.29}$$

where $A(\theta)$ is defined as

$$A(\theta) = x_0\cos(\theta_0) + y_0\sin(\theta_0), \tag{3.30}$$

and $Q(x)$ is the normalized Gaussian tail probability function which is defined as

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-\frac{u^2}{2}} du. \tag{3.31}$$

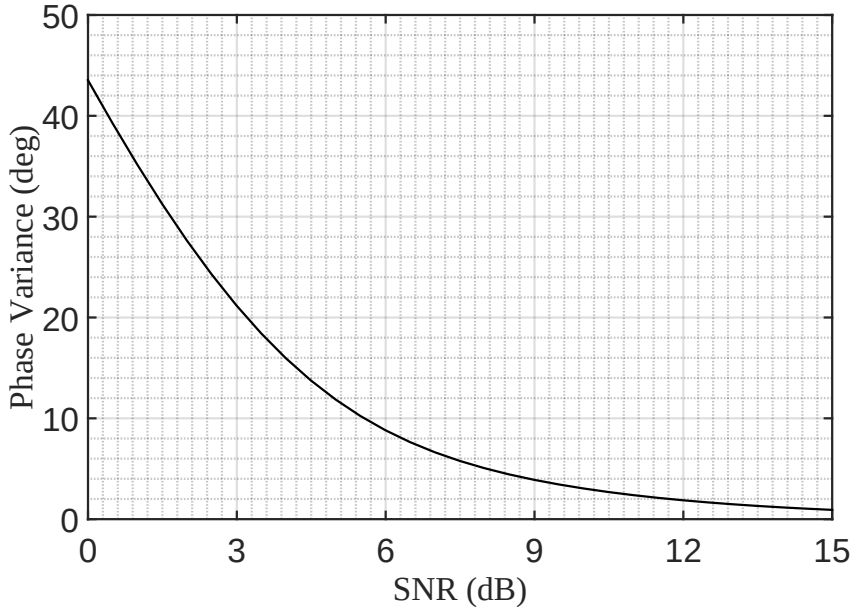


Figure 3.5: SNR vs phase variance of super-regenerative amplifiers.

A detailed derivation of (3.29) can be found in Appendix B.

3.3.2 Sensitivity analysis of super-regenerative phase

Equations (3.27) and (3.29) describe the uncertainty in the output phase of an SRA as a function of SNR. While the integral has no closed form solution, numerical computation can still be used to further analyze, quantify, and predict the performance of phase demodulating SRAs. One way to quantify the performance of an SRA is illustrated in Figure 3.5, which shows a plot of phase variance versus SNR. While useful, phase variance does not provide enough information for designers to conduct a link budget analysis. Ultimately, designers are interested in how much noise figure a system would need to achieve a given bit error rate. Therefore, this subsection derives the relationship between (3.27), noise figure, and bit error rate (BER).

Figure 3.6 illustrates the probability density functions of the output phase when an SRA receives QPSK modulated signals at an SNR_{out} of 5 dB. In the case of receiving a (1,1) symbol, the optimum threshold for detection is located at 0° and 90°. The area

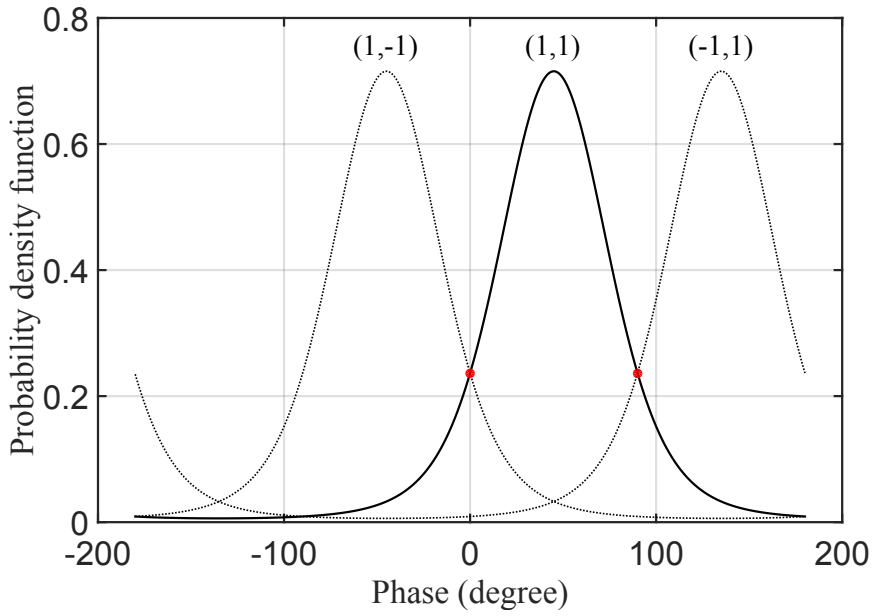


Figure 3.6: Probability density functions of the phase at the SRA output given two different QPSK input signals at SNR_{out} = 5 dB.

outside these two points can be integrated to find the symbol error rate, and the symbol error rate can be divided by the number of bits per symbol to calculate the bit error rate. Figure 3.7 plots the results of this analysis, showing the required SNR for a given BER for QPSK, along with BPSK and 8-PSK. This plot can then be used by designers for link budget analysis.

According to (3.6), (3.11), and (3.13), the filtering term $k(t)$ is the only input-dependent portion of the expression for the output waveform. The magnitude of $k(t)$ is $|X(\omega_0)|$, and the signal-to-noise ratio can be expressed by computing the ratio between $|X(\omega_0)|^2$ due to a signal and that due to noise. The magnitude of $|X(\omega_0)|^2$ due to a sinusoidal input, denoted by I_X^2, is given by:

$$I_X^2 = \frac{\omega_0^2 I_{tank}^2}{2} \frac{\pi}{\Omega_s^2}, \tag{3.32}$$

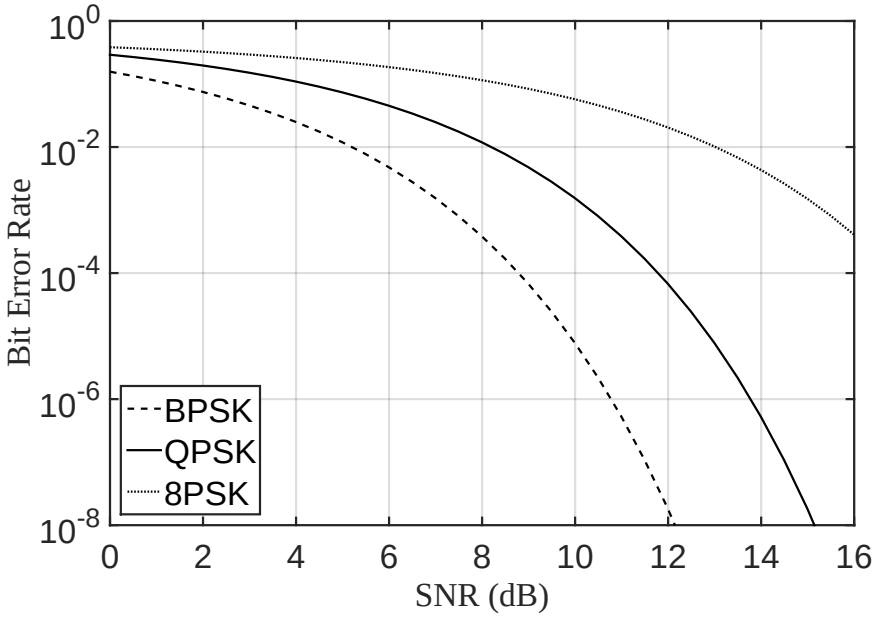


Figure 3.7: SNR vs. BER for various phase modulation schemes.

and $|X(\omega_0)|^2$ due to noise was derived in (3.71) and is repeated here for convenience:

$$\sigma_X^2 = \frac{N_0 \omega_0^2 \sigma_s}{2} \sqrt{\pi}. \tag{3.33}$$

Therefore, the ratio between the two quantities can be used to compute the output SNR of an SRA:

$$SNR_{out} = \frac{I_X^2}{\sigma_X^2} = \frac{I_{tank}^2}{N_0} \frac{\sqrt{\pi}}{\Omega_S}. \tag{3.34}$$

For a high-data rate system concerned with time-variant noise, (3.33) can be replaced with (3.84) in the above analysis.

From (3.34), the SRA shapes the input white noise as if it is filtered by a brick-wall filter with the noise bandwidth

$$BW_n = \frac{\Omega_S}{\sqrt{\pi}}. \tag{3.35}$$

Thus, we can express the sensitivity of the SRA in dB as:

$$P_{in,min} = N_0 + NF + 10\log_{10} BW_n + SNR_{o,min}, \tag{3.36}$$

where N_0 is the noise power at the input to the SRA, NF is the noise figure of the SRA, and $SNR_{o,min}$ is the output SNR required to achieve the desired bit-error-rate which can be found in Figure 3.7. If the SRA were the first block in a receiver, N_0 would be -174 dBm/Hz, for example.

3.3.3 The effect of noise in the saturated oscillation regime on the sensitivity of a super-regenerative receiver

Once super-regenerative amplification is complete, and a phase outcome is decided, an SRA will ideally oscillate while maintaining its initial phase. However, in this regime an SRA is also an oscillator, and its output waveform exhibits a finite amount of jitter which can potentially affect the sensitivity of the receiver. Figure 3.8 shows the simulated effect of phase noise on the SNR vs. BER curve for QPSK modulation. Here it can be seen that 1° of jitter yields nearly identical results to an ideal SRA. Interested readers can refer to Appendix C for a detailed explanation of obtaining the probability density function of output phase in presence of SRA phase noise.

It is worth noting that noise can also amplitude-modulate the output waveform of the SRA in the saturated oscillation regime. This amplitude noise is generally ignored, as it is attenuated significantly by the oscillator's amplitude limiting mechanism [43]. If necessary, these amplitude fluctuations can further be attenuated using a delimiter circuit. For these reasons, amplitude noise is very small in comparison to phase uncertainty that arises from super-regenerative amplification. To put this into perspective, consider a very large 100-mV amplitude noise (or fluctuation) in a 1-V peak-to-peak oscillation: this would translate to 20 dB SNR, which is still 5 dB higher than the SNR required for

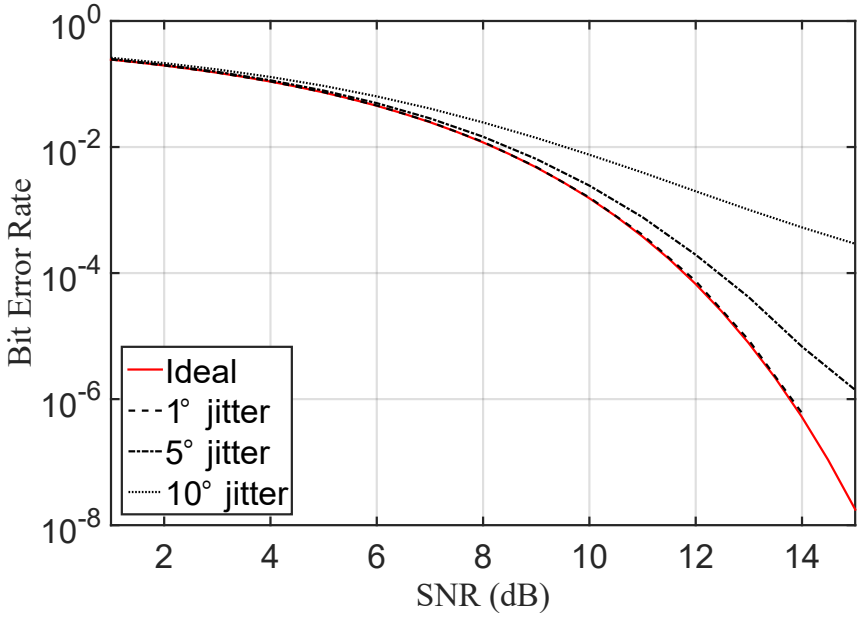


Figure 3.8: SNR vs. BER in the presence of phase noise at different RMS jitter values for QPSK modulation.

BER of 10^{-8}.

3.4 Design and Analysis of a Colpitts-based SRA

The analysis presented in the preceding sections assumed a single-port SRA model as illustrated in Figure 3.2. To translate this analysis to real circuit implementations, it is necessary to analyze the noise figure of such implementations. In this chapter, a common-base Colpitts-based SRA architecture is chosen for analysis and measurement. This section derives the noise figure of this circuit so that it can be compared to measurement results from a discrete BJT prototype that will be presented in Section V.

Figure 3.9 shows the schematic of the common-base Colpitts-based SRA architecture that will be analyzed and prototyped in this chapter. Here, R_S models the antenna (source) impedance, R_D is used to set the DC bias of the oscillator, and R_P is the para-

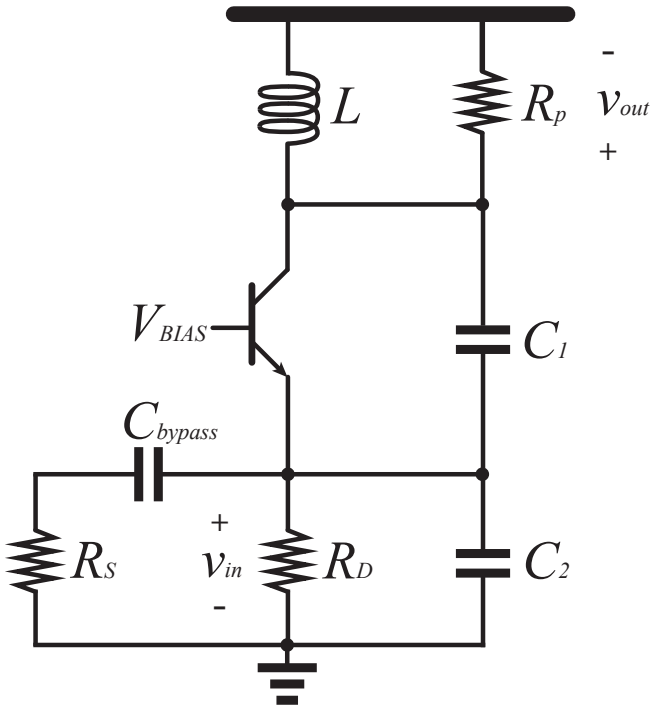


Figure 3.9: A schematic of Colpitts-based SRA.

sitic resistance of the inductor L. It is assumed that the SRA is directly connected to a source such as an antenna for the sake of simplicity in the analysis. However, for better performance, a low noise amplifier should precede the SRA, and the input to the SRA should be a large impedance so as to not degrade the loaded Q of the resonator.

During normal operation, V_{BIAS} is a ramp function, and the transconductance of the active device would change as a function of time. However, as shown in Appendix A, the transconductance of the active device can be assumed to be the minimum transconductance value needed for oscillation without much loss of accuracy as long as the data rate is much lower than the carrier frequency. Therefore, the value of V_{BIAS} is assumed to be set to the value that just starts oscillation. This value can be computed with the help of the start-up model of the Colpitts oscillator, shown in Figure 3.10. All dynamic elements of the transistor are ignored in order to simplify the mathematics to emphasize design intuitions; however, an accurate analysis should take such factors into account.

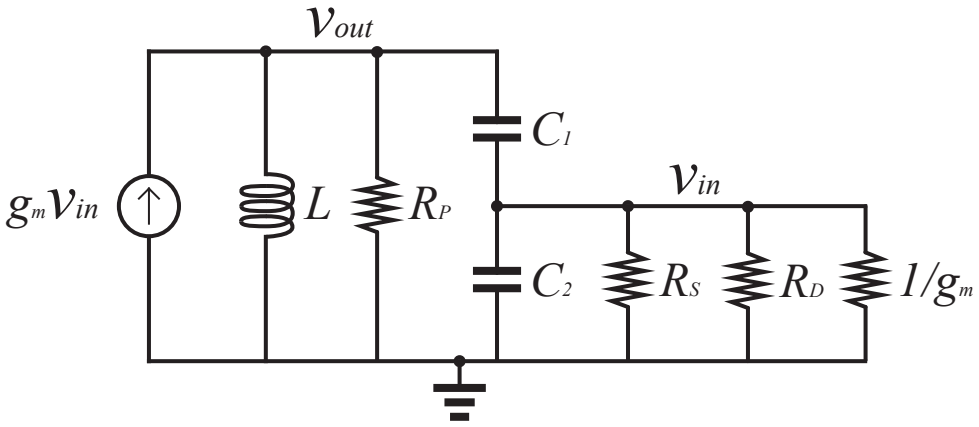


Figure 3.10: Small-signal model of the Colpitts-based SRA.

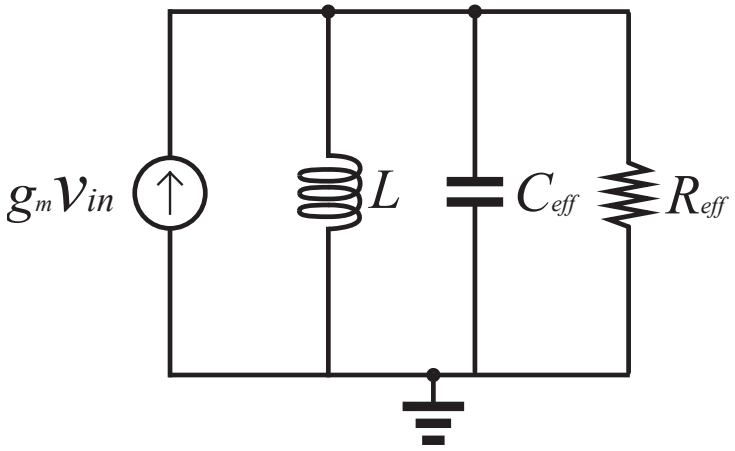


Figure 3.11: One-port equivalent model of the Colpitts-based SRA.

The noise figure analysis can be simplified by first treating Capacitors C_1 and C_2 as an ideal transformer that reflects the input resistors R_S, R_D, and $1/g_m$ to the output node [44]. Then, the circuit in Figure 3.10 can be simplified to the circuit of Figure 3.11, where the effective capacitance C_{eff} across the tank is

$$C_{eff} = \frac{C_1 C_2}{C_1 + C_2}, \tag{3.37}$$

and the effective resistance R_{eff} is

$$R_{eff} \approx R_P \parallel \frac{1}{n^2}(\frac{1}{g_m} \parallel R_S \parallel R_D), \tag{3.38}$$

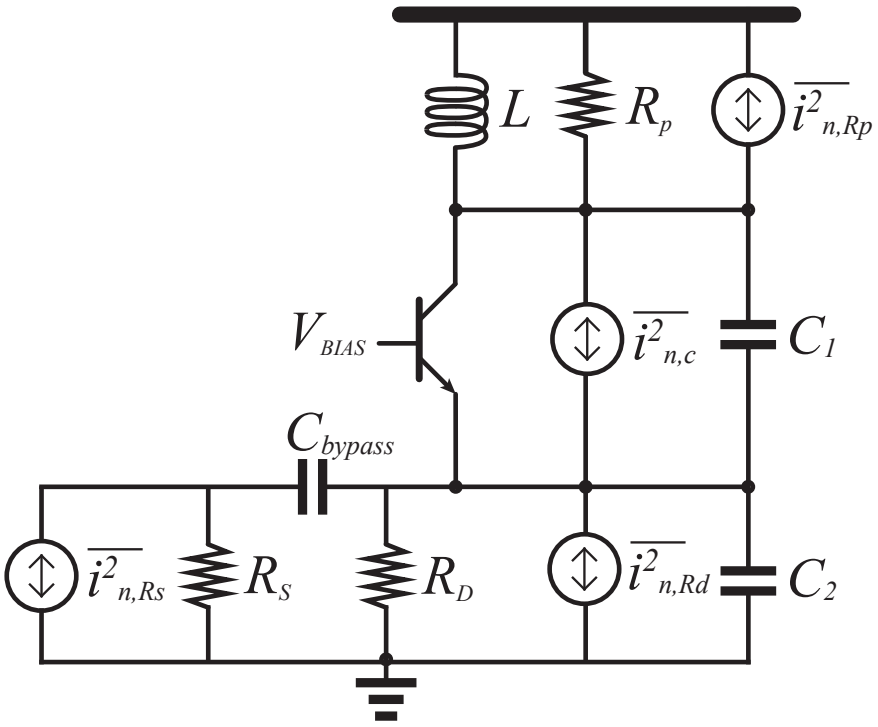


Figure 3.12: Circuit model of the SRA with noise sources.

where n is the ratio between the capacitors,

$$n \equiv \frac{C_1}{C_1 + C_2}. \tag{3.39}$$

The ideal transformer approximation is valid when the carrier frequency is sufficiently high such that impedances of the capacitors C_1 and C_2 are much smaller than that of the three parallel resistors, R_S,R_D, and $1/g_m$ [44]. Furthermore, if a sufficiently high-Q inductor is used, then the value of R_P should be much greater than the other resistors so that R_P can be ignored from (3.38) to enable convenient analysis (though this is not required in a practical implementation). Thus, the output voltage across the tank at resonance is:

$$v_{out} = g_m v_{in} R_{eff} \approx g_m v_{in} (\frac{1}{n^2} (\frac{1}{g_m} \parallel R_S \parallel R_D)). \tag{3.40}$$

The above equation leads to the following expression for the minimum transcon-

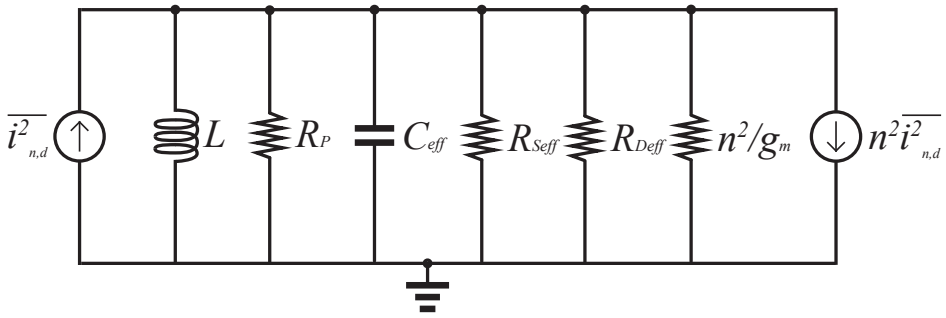


Figure 3.13: Single-port circuit model of the SRA with noise sources.

ductance $g_{m,min}$ to cause an oscillation:

$$g_{m,min} = \frac{n}{R_{in}(1-n)}, \tag{3.41}$$

where R_{in} represents the parallel combination of the physical resistors at the input,

$$R_{in} \equiv R_S \parallel R_D. \tag{3.42}$$

Now that a simple one-port oscillator model of Colpitts-based SRA is obtained, as shown in Figure 3.11, noise sources can be added to derive an expression for the noise figure. Figure 3.12 illustrates the schematic of the SRA with all noise sources included. Assuming a BJT with collector current I_c, the resulting shot noise is given by:

$$\overline{i^2_{n,c}} = 2qI_C\Delta f, \tag{3.43}$$

and can be split into a noise current going into the inductor, and a noise current going into the source node of the transistor. It should be noted that these noise sources are fully correlated, and their polarities are in the opposite direction. Both these noise sources can be output-referred and subtracted from one another to find the true output-referred noise due to the active device. The definition of small-signal transconductance is given as:

$$g_m \equiv \frac{dI_C}{dV_{be}} = I_C/\frac{kT}{q}, \tag{3.44}$$

and thus, (3.43) can be rearranged as

$$\overline{i_{n,c}^2} = 2kTg_m\Delta f, \tag{3.45}$$

which is similar to the thermal noise expression for a MOSFET. Thus, while the proceeding analysis utilizes a BJT shot noise model, the results can be easily adapted to MOSFETs if desired.

The preceding analysis showed that capacitors C_1 and C_2 form an ideal impedance transformer at high frequency. Therefore, the resistors R_S and R_D, and their corresponding noise sources can be reflected to the output via the impedance transformer. Figure 3.13 shows the small signal model of the SRA when the resistors are reflected to the output. The shot/thermal noise sources due to the reflected resistors R_{Seff} and R_{Deff} are omitted from the figure for concise illustration. The value of the impedance transformed resistors are given by:

$$R_{Seff} = \frac{R_S}{n^2}, \tag{3.46}$$

$$R_{Deff} = \frac{R_D}{n^2}. \tag{3.47}$$

The resistor due to the transformed transconductance n^2/g_m is not a physical resistor and is therefore noiseless. The split thermal noise currents of the active device have opposite polarities as shown in Figure 3.12, and their sum is

$$\overline{i_{n,c,sum}^2} = (1-n)^2\overline{i_{n,c}^2}. \tag{3.48}$$

Now that all of the noise sources are output-referred, the noise figure of the SRA can be derived by computing the ratio between all noise sources and the noise due to the source resistor R_S:

$$NF = \frac{\overline{i_{n,c,sum}^2} + \overline{i_{n,Rd_{eff}}^2} + \overline{i_{n,Rs_{eff}}^2} + \overline{i_{n,Rp}^2}}{\overline{i_{n,Rs_{eff}}^2}}. \tag{3.49}$$

Substituting each term with its corresponding value results in the following expression:

$$NF = 1 + \frac{R_S}{R_D} + \frac{R_S}{n^2 R_P} + \frac{g_m R_S (1-n)^2}{2n^2}. \tag{3.50}$$

Substituting (3.41) into (3.50) results in

$$NF = 1 + \frac{R_S}{R_D} + \frac{R_S}{n^2 R_P} + \frac{R_S}{2R_{in}} \frac{1-n}{n}. \tag{3.51}$$

Equation (3.51) shows what matches intuition: a higher Q factor of the inductor leads to a better noise figure of the amplifier. Furthermore, increasing n close to 1 would also result in the lower noise figure. However, (3.41) indicates that increasing n will increase the minimum tranconductance, and therefore the power consumption. Therefore, there is a direct trade-off between power and noise figure.

To validate the equations developed above, a BJT-based Colpitts oscillator was designed in 250 nm BCD (Bipolar-CMOS-DMOS) technology and simulated using Spectre. Here, hand calculation results matched simulations to no worse than 6.25%, even though, for simplicity, the hand calculations did not include transistor on-resistance.

3.5 Measurement Results

A discrete prototype was designed and measured in order to validate the analysis presented in the preceding sections. The schematic of the design and its testing setup, as well as a photograph of the assembled PCB, are shown in Figures 3.14 and 3.15, respectively. Here, a common-base Colpitts oscillator was designed to resonate at 45-MHz using a BJT for ease of implementation. A 45-MHz carrier frequency was chosen to ensure that the operating frequency was high enough to be above the flicker noise corner of the transistor, yet low enough to be easily captured by low-cost instrumentation. A buffer was inserted between the SRA and the oscilloscope to provide isolation. The noise figure of the buffer was found to be negligible as the gain of the SRA is large.

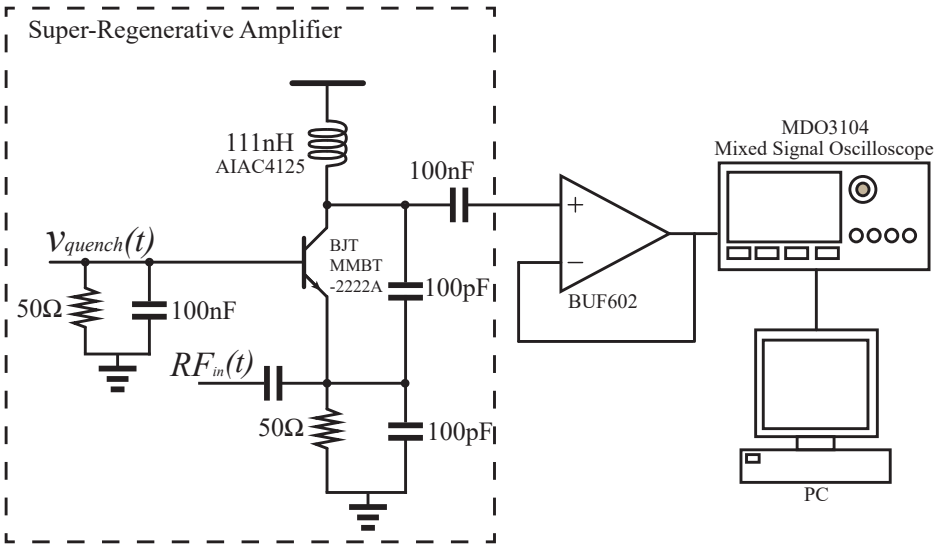


Figure 3.14: Schematic of a discrete SRA prototype used for experimental verification.

A high-Q inductor ($Q \approx 100$) and a small input resistor were used to ensure that the effective resistance across the resonant tank is dominated by a known resistance value rather than the parasitic resistance of the tank. As shown in (3.51), a low resistance would degrade the noise performance of the SRA; however, a well controlled resistance value enables more accurate experimental validation. The discrete SRA consumed 1.2 mA current from 1.5 V.

Figure 3.17 illustrates the shape of the waveforms used in measurements. A sinusoidal input of a known phase from a signal generator was injected into the input of the SRA while a synchronized high-speed oscilloscope acquired the output waveform. The quench signal $v_{quench}(t)$ was generated using an arbitrary waveform generator running at a period of 5 μs, and applied to the base of the transistor. A reference square wave signal was also generated by the arbitrary waveform generator to indicate the beginning of a bit period and serve as a reference time for the purposes of computing phase.

The output of the SRA and synchronous reference square wave are fed to the high-speed oscilloscope. Data sampled by the oscilloscope was then transferred to a computer and processed in MATLAB. Specifically, the phase of the SRA output was

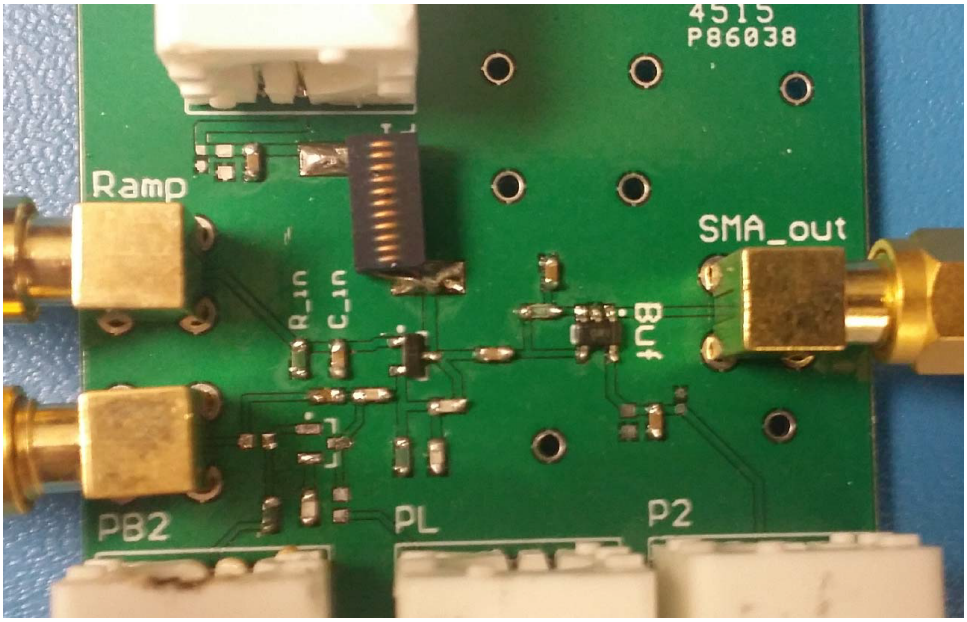


Figure 3.15: Photograph of the discrete SRA prototype used for experimental verification. Fairchild MMBT-2222a BJT, Abracon Co. AIAC-4125 inductor, and TI BUF602 amplifier have been used in the measurement.

compared to the reference square-wave (which was in phase with the input) by first generating a pair of 45 MHz IQ sinusoids in MATLAB, with phase derived from the measured reference square-wave. The IQ sinusoids were then used to downconvert the measured output waveform. The result was then filtered digitally to extract the baseband symbols. In this manner, phase demodulation was performed digitally, and circuits for IQ demodulation, and their noise contributions, were avoided.

Figure 3.18 shows the measured frequency response of the SRA. The frequency response was measured by converting effective amplitude information into the time it takes the SRA's envelope to cross a 10 mV threshold (i.e., the trigger time in [40]). Curve-fitting this response yields an SRA frequency constant of $\Omega_s = 5.3$ MHz$\sqrt{rad}$, and from (3.35) the effective noise bandwidth is computed to be $\frac{\Omega_s}{\sqrt{\pi}} = 2.9$ MHz.

To measure BER, input power to the SRA was swept from -98 dBm to -82 dBm in increments of 2 dB. A 45 MHz unmodulated sinusoid was injected at the input, and at each input power level, 6000 symbols were captured and used to plot output phase histograms. Three representative power levels are shown in Figure 3.19. These samples

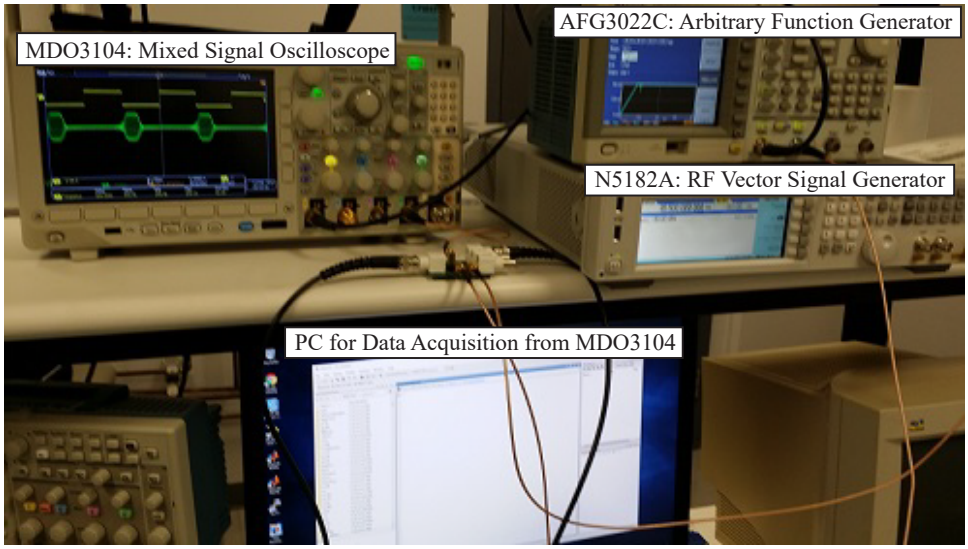


Figure 3.16: Photograph of the experimental set-up (DC supplies not shown).

were then used to compute BER, as shown in Figure 3.20, by integrating the the area under the probability density function curve that fell outside the threshold as described in Section III.

Prediction of BER using the developed model requires precise knowledge of SNR_{out}. Since all possible output phases are distributed from $\{-\pi, \pi\}$, the pdf given by (3.27) and (3.29) is non-Gaussian, making direct computation of SNR_{out} difficult. Instead, the measured histogram at -90 dBm (roughly the middle of the swept range) was curve-fit using (3.27) to infer SNR_{out} at that power level. Then, SNR_{out} was assumed to scale linearly in dB at other power levels, enabling prediction of pdfs and BER curves at all other input power levels. Figures 3.19 and 3.20 plot these theoretical results on top of measurement data, showing excellent matching.

Based on Figures 3.7 and 3.20, the output SNR was 7 dB when the input power from the signal generator was -90 dBm. There is -2.2 dBm additional loss in SNR due to mismatch at the input. Therefore, this suggests that the noise floor was -99.2 dBm. The noise figure from other measured parameters can be calculated as follows. Starting from the definition of noise figure:

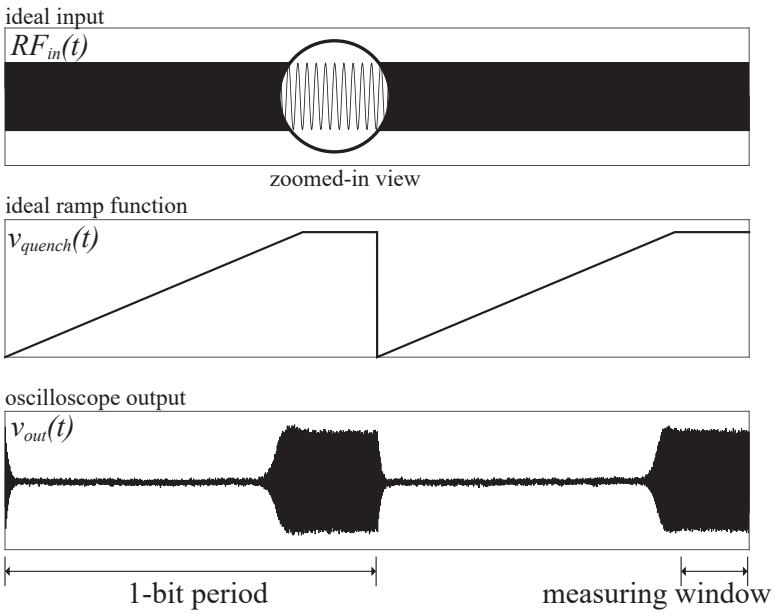


Figure 3.17: Illustration of important waveforms in the measurement.

$$NF_{dB} = SNR_{in,dB} - SNR_{out,dB}, \tag{3.52}$$

and

$$SNR_{in,dB} = P_{in,dB} - 10\log_{10} kT - 10\log_{10} BW_n, \tag{3.53}$$

it follows that

$$NF = P_{in,dB} - 10\log_{10} kT - 10\log_{10} BW_n - SNR_{out,dB}. \tag{3.54}$$

The previously measured value of noise bandwidth, BW_n, was 2.9 MHz, and therefore, the measured noise figure of the system is 10.0 dB at 300K room temperature. Theoretical calculation using (3.49) on the circuit yields a calculated noise figure of 9.5 dB. Note that the impedance of the 100 pF capacitor is not considerably smaller than the impedance of the parallel input resistors, and therefore un-approximated hand calculations were made to obtain the stated value. In this case, the theoretical noise figure and the measured noise figure are within 0.5 dB. The slightly higher measured noise figure

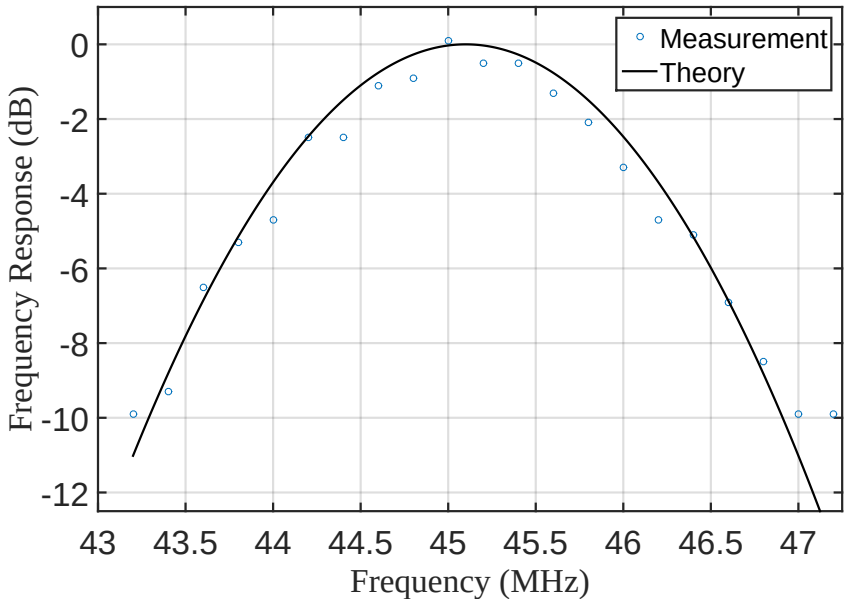


Figure 3.18: Frequency response of the SRA.

is hypothesized to be as a result of unaccounted noise sources such as from the arbitrary signal generator and the supply.

Figure 3.21 shows phase noise measurement of the prototype SRA during oscillation mode. The RMS jitter of the SRA can be estimated by integrating product of the phase noise curve and a weight function, repeated below for convenience [45].

$$\sigma_\tau^2 = \int_0^\infty S_\phi(f) \frac{\sin^2(\pi f/f_0)}{(\pi f_0)^2} df. \tag{3.55}$$

Here, RMS jitter is computed to be 0.68 degrees, which is not high enough to adversely affect the sensitivity significantly as discussed in Section 3.3.3.

3.6 Appendix A: Time-Domain Stochastic Analysis of Super-Regenerative Amplifiers

3.6.1 Time-invariant Noise Input

While the frequency domain analysis in the Section II shows meaningful insight into the behavior of SRAs with AWGN inputs, working in frequency domain inherently assumes time-invariance. To offer a more general model, this section presents a stochastic time-domain model that computes the variance of the output for both AWGN inputs, and time-varying noise inputs.

Starting from (3.3), the output waveform of an SRA due to AWGN input can be expressed as:

$$v_{n,out}(t) = Z_0 \mu(t) k_n(t) \tag{3.56}$$

$$k_n(t) = \int_{t_0}^{t} \frac{\partial s(\tau)}{\partial \tau} g(\tau) sin[\omega_0(t-\tau)] d\tau, \tag{3.57}$$

where $s(t)$ is a random process that represents AWGN input current to the SRA. The auto-correlation $R_k(t_1, t_2)$ of random process $k_n(t)$ is then defined as:

$$R_k(t_1, t_2) = E[k_n(t_1) k_n(t_2)]. \tag{3.58}$$

Since the Gaussian sensitivity function $g(\tau)$ tends to zero before the end of a bit period, and since we are interested in the outcome once the oscillations have grown, integrating over all time renders a good approximation for $k(t)$ for t greater than $3\sigma_s$ [40]:

$$k_n(t) \approx \int_{-\infty}^{\infty} s^{'}(\tau) g(\tau) \sin[\omega_0(t-\tau)] d\tau. \tag{3.59}$$

Then, the auto-correlation function can be expressed as

$$R_k(t_1, t_2) = E[\int_{-\infty}^{\infty} \int_{-\infty}^{\infty} s^{'}(u) s^{'}(v) H(u, t_1) H(v, t_2) du dv]. \tag{3.60}$$

where u and v are dummy variables and

$$H(u,t) = g(u)h(t-u), \tag{3.61}$$

$$h(t-u) = \sin[\omega_0(t-u)]. \tag{3.62}$$

Since $s^{'}(u)$ and $s^{'}(v)$ are the only nondeterministic quantities,

$$R_k(t_1,t_2) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} E[s^{'}(u)s^{'}(v)]H(u,t_1)H(v,t_2)dudv, \tag{3.63}$$

which can be simplified further such that

$$E[s^{'}(u)s^{'}(v)] = \frac{\partial}{\partial u}\frac{\partial}{\partial v}E[s(u)s(v)]. \tag{3.64}$$

The input $s(t)$ is AWGN, and its autocorrelation is therefore:

$$E[s(u)s(v)] = R_n(t_1,t_2) = \frac{N_0}{2}\delta(u-v). \tag{3.65}$$

Here, N_0 is the power density of the AWGN input. Substituting (3.64) and (3.65) into (3.63) results in the following expression:

$$R_k(t_1,t_2) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\frac{N_0}{2}[\frac{\partial}{\partial u}\frac{\partial}{\partial v}\delta(u-v)]H(u,t_1)H(v,t_2)dudv. \tag{3.66}$$

The terms with u can be isolated, and substituting (3.61) into (3.66) yields:

$$R_k(t_1,t_2) = \int_{-\infty}^{\infty} g(v)h(t_2-v) \int_{-\infty}^{\infty}\frac{N_0}{2}[\frac{\partial}{\partial u}\frac{\partial}{\partial v}\delta(u-v)]g(u)h(u-t_1)dudv. \tag{3.67}$$

The following identity of the Dirac delta function $\delta(t)$ is useful for further simplifying

the above expression:

$$\int_{-\infty}^{\infty} f(x)\delta^{'}(x-a)dx = -f^{'}(a). \tag{3.68}$$

Based on (3.68) and (3.61), the latter half of (3.66) can be rewritten as

$$\begin{aligned} &\int_{-\infty}^{\infty} \frac{\partial}{\partial u}\frac{\partial}{\partial v}\frac{N_0}{2}\delta(u-v)g(u)h(t_1-u)du \\ &= \frac{N_0}{2}\frac{\partial}{\partial v}\int_{-\infty}^{\infty} \frac{\partial}{\partial u}\delta(u-v)g(u)h(t_1-u)du \\ &= -\frac{N_0}{2}\frac{\partial^2}{\partial v^2}(g(v)h(t_1-v)). \end{aligned} \tag{3.69}$$

Substitute (3.69) into (3.67) to further simplify the expression:

$$R_k(t_1,t_2) = \int_{-\infty}^{\infty} -\frac{N_0}{2}\frac{\partial^2}{\partial v^2}[g(v)h(t_1-v)]g(v)h(t_2-v)dv. \tag{3.70}$$

Carrying out the integral and equating t_1 to t_2 results in the variance of the random process $k_n(t)$:

$$\sigma_k^2 = R_k(t_1,t_1) = \frac{N_0\omega_0^2\sigma_s}{2}\sqrt{\pi}. \tag{3.71}$$

Satisfyingly, the variance σ_k^2 is identical to the conclusion of the frequency domain analysis, σ_X^2, in [40].

3.6.2 Time-Varying White Noise Model

From Section II, a ramp damping function can be expressed as:

$$\zeta(t) = -\beta t = \zeta_0(1 - g_m(t)R), \tag{3.72}$$

where $\beta = (\omega_0\sigma_s^2)^{-1}$ and $\zeta_0 = Z_0/2R$. Solving for $g_m(t)$ yields:

$$g_m(t) = \frac{\beta}{\zeta_0 R}t + \frac{1}{R} = \frac{2}{\omega_0\sigma_0^2 Z_0}t + g_{m0}, \tag{3.73}$$

where g_{m0} is the minimum transconductance needed to cancel the parallel resistance R of oscillator tank as shown in Fig. 3.2. The underlying assumption is that the same transconductance that provides negative resistance is also generating noise current which is injected into the tank [46]. To simplify analysis, define $\alpha = 2/(\omega_0 \sigma_0^2 Z_0)$ to describe how fast the transconductance is changing in time. Assuming a BJT-based oscillator, the unilateral power spectral density of the shot noise current from the active device can now be described as:

$$2qI_c(t) = 2kTg_m(t) = 2kT(g_{m0} + \alpha t), \tag{3.74}$$

for $t_i \leq t \leq t_f$, where t_i and t_f are the beginning and the end of a symbol period respectively. Thus, the ratio of the time-variant noise to the time-invariant noise at time t can be defined as

$$\frac{2kTg_m(t)}{2kTg_{m0}} = 1 + \frac{\alpha t}{g_{m0}}. \tag{3.75}$$

For simplicity, we define this ratio as:

$$c(t) = 1 + \frac{\alpha t}{g_{m0}}. \tag{3.76}$$

Now the time-varying current input noise $i_{n,tv}(t)$ can be modeled as AWGN current noise with its amplitude changing as a function of time such that $i_{n,tv}(t) = \sqrt{c(t)}s(t)$; the square root shows that the input is not power, but current. In order to reflect the time-varying current input, we replace $s(t)$ with $\sqrt{c(t)}s(t)$ in (3.59). The resulting expression is:

$$k_n(t) = \int_{t_i}^{t} \frac{\partial \sqrt{c(\tau)}s(\tau)}{\partial \tau} g(\tau) sin[\omega_0(t-\tau)] d\tau. \tag{3.77}$$

Using the product rule:

$$\frac{\partial \sqrt{c(\tau)}s(\tau)}{\partial \tau} = \frac{\partial \sqrt{c(\tau)}}{\partial \tau} s(\tau) + \frac{\partial s(\tau)}{\partial \tau} \sqrt{c(\tau)}. \tag{3.78}$$

Because $s(\tau)$ represents white noise, at sufficiently high frequency, $s(\tau)$ is orders of magnitude less than $\partial s(\tau)/\partial\tau$. Therefore, the first term on the right side of the equality in (3.78) can be neglected towards the following expression:

$$\frac{\partial\sqrt{c(\tau)}s(\tau)}{\partial\tau} \approx \frac{\partial s(\tau)}{\partial\tau}\sqrt{c(\tau)}. \tag{3.79}$$

The validity of the above assumption has been verified using numerical computation with practical component values. Thus, similar to the analysis present in the time-invariant noise case, the auto-correlation of $k_n(t)$ can be expressed as:

$$\begin{aligned} R_k(t_1,t_2) = E[\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} s^{'}(u)s^{'}(v) \\ \sqrt{c(u)}\sqrt{c(v)}H(u,t_1)H(v,t_2)dudv]. \end{aligned} \tag{3.80}$$

Note that (3.80) is similar to (3.63), but with two additional terms: $\sqrt{c(v)}$ and $\sqrt{c(u)}$. Therefore, (3.80) can be simplified in a similar manner as follows:

$$\begin{aligned} R_k(t_1,t_2) = \int_{-\infty}^{\infty}\frac{N_0}{2}\frac{\partial^2}{\partial v^2}[\sqrt{c(v)}g(v)h(t_1-v)] \\ \sqrt{c(v)}g(v)h(t_2-v)dv. \end{aligned} \tag{3.81}$$

Under the product rule again,

$$\begin{aligned} \frac{\partial}{\partial v}(\sqrt{c(v)}g(v)h(t_1-v)) = \frac{\partial}{\partial v}(\sqrt{c(v)}g(v))\sin[\omega_0(t_1-v)] \\ +\frac{\partial}{\partial v}(\sin[\omega_0(t_1-v)])\sqrt{c(v)}g(v). \end{aligned} \tag{3.82}$$

The derivative of $h(t_1-v)$ is proportional to ω_0, which at the frequency of interest, is orders of magnitude greater than any other terms in the equation. Therefore, similar to (3.79), the following approximation can be made to simplify the analysis:

$$\frac{\partial}{\partial v}(\sqrt{c(v)}g(v)h(t_1-v)) \approx \frac{\partial}{\partial v}(\sin[\omega_0(t_1-v)])\sqrt{c(v)}g(v), \tag{3.83}$$

and

$$R_k(t_1, t_2) \approx \int_{-\infty}^{\infty} \frac{N_0}{2} \frac{\partial^2}{\partial v^2} [h(t_1 - v)] c(v) g^2(v) h(t_2 - v) dv. \tag{3.84}$$

The variance σ_k^2 of $k(t)$ can be found by equating t_1 and t_2. Unfortunately, the solution to (3.84) is long and unintuitive. Instead, numerical computation given a set of realistic circuit parameters can be used to provide designers with insight.

As an example, consider an SRA circuit built to operate at 40 MHz with a 100 nH inductor with a Q factor of 100, loaded tank Q factor of 10, and a quiescent current of 1.2 mA from a BJT. For this circuit, Figure 3.22 shows the ratio of output variance between the time-variant analysis and the time-invariant analysis plotted against data rate. The modulation scheme is assumed to be either OOK or BPSK such that the data rate is the inverse of the symbol period. In this case, increasing the data rate implies that the transconductance is changing at a faster rate, and the SRA time constant becomes much smaller.

The result of this analysis shows that when the data rate remains sufficiently small compared to the carrier frequency, a time-invariant approximation of the time-variant noise source is appropriate. However, if the damping function changes fast such that the SRA frequency constant, Ω_s, approaches the carrier frequency, then the effect of time-variant noise source can be large. In the extreme case of using a square wave for a damping function as seen in [37], the effect of time-variant noise source should be taken into account in the design of the SRA. For more accurate result, numerical analysis would be needed if the slope of the damping function becomes comparable to the oscillation frequency, as closed form solution to (3.2) would no longer exists.

3.7 Appendix B: Derivation of the pdf of Θ

Equation (3.27) can be rearranged in the following way:

$$f_\Theta(\theta) = \frac{1}{\sigma^2 2\pi} e^{-\frac{v_s^2}{2\sigma^2}} \int_0^{\infty} r e^{-\frac{r^2 - 2r(A(\theta))}{2\sigma^2}} dr, \tag{3.85}$$

which can be further rearranged as:

$$f_\Theta(\theta) = \frac{1}{\sigma^2 2\pi} e^{-\frac{v_s^2}{2\sigma^2}} \int_0^\infty r e^{-\frac{r^2 - 2r(A(\theta)) + A(\theta)^2}{2\sigma^2}} e^{\frac{A(\theta)^2}{2\sigma^2}} dr. \tag{3.86}$$

Completing the square in the exponents results in the following expression:

$$f_\Theta(\theta) = \frac{1}{\sigma^2 2\pi} e^{\frac{A(\theta)^2 - v_s^2}{2\sigma^2}} \int_0^\infty r e^{-\frac{(r - A(\theta))^2}{2\sigma^2}} dr. \tag{3.87}$$

Integration by substitution leads to the following

$$f_\Theta(\theta) = \frac{1}{2\pi} e^{\frac{A(\theta)^2 - v_s^2}{2\sigma^2}} \int_{-\frac{A(\theta)}{\sigma}}^\infty (u + \frac{A(\theta)}{\sigma}) e^{-\frac{u^2}{2}} du, \tag{3.88}$$

where

$$u = \frac{r - A(\theta)}{\sigma}, \tag{3.89}$$

$$du = \frac{dr}{\sigma}. \tag{3.90}$$

From (3.31), the integral with the term $A(\theta)/\sigma$ can be expressed as the $Q(x)$ function such that

$$f_\Theta(\theta) = \frac{1}{2\pi} e^{\frac{A(\theta)^2 - v_s^2}{2\sigma^2}} (\int_{-\frac{A(\theta)}{\sigma}}^\infty u e^{-\frac{u^2}{2}} du + \frac{A(\theta)}{\sigma} Q(-\frac{A(\theta)}{\sigma})). \tag{3.91}$$

The integral in the above expression yields

$$\int_{-\frac{A(\theta)}{\sigma}}^\infty u e^{-\frac{u^2}{2}} du = e^{-\frac{A(\theta)^2}{2\sigma^2}}, \tag{3.92}$$

and thus (3.91) becomes

$$f_\Theta(\theta) = \frac{A(\theta)}{\sqrt{2\pi}\sigma} e^{\frac{A(\theta)^2 - v_s^2}{2\sigma^2}} Q(-\frac{A(\theta)}{\sigma}) + \frac{1}{2\pi} e^{-\frac{v_s^2}{2\sigma^2}}. \tag{3.93}$$

3.8 Appendix C: Effect of Phase Noise on the sensitivity

The distribution of an SRA's output phase after super-regenerative amplification is described by (3.27). Each phase outcome exhibits an additional randomness due to various sources of noise that are typically characterized by phase noise or jitter. The normal distribution of jitter is given by:

$$f_{\Phi}(\phi) = \frac{1}{\sqrt{2\pi}\sigma} e^{\frac{(-\phi)^2}{2\sigma^2}}. \tag{3.94}$$

Then, the total phase uncertainty of the SRA is sum of independent random variables Θ and Φ; their probability density functions are described by (3.27) and (3.94), respectively. The probability density function of a sum of two independent random variables results in a convolution of their respective distributions. Thus, convolving (3.27) and (3.94), and integrating the area under the curve outside of the threshold will yield BER.

3.9 Acknowledgement

Chapter 3, in full, is a reprint of the material as it appears in D. Lee and P. P. Mercier, "Noise Analysis of Phase-Demodulating Receivers Employing Super Regenerative Amplification," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 9, pp. 3299-3311, Sept. 2017. The dissertation author was the primary author of this paper.

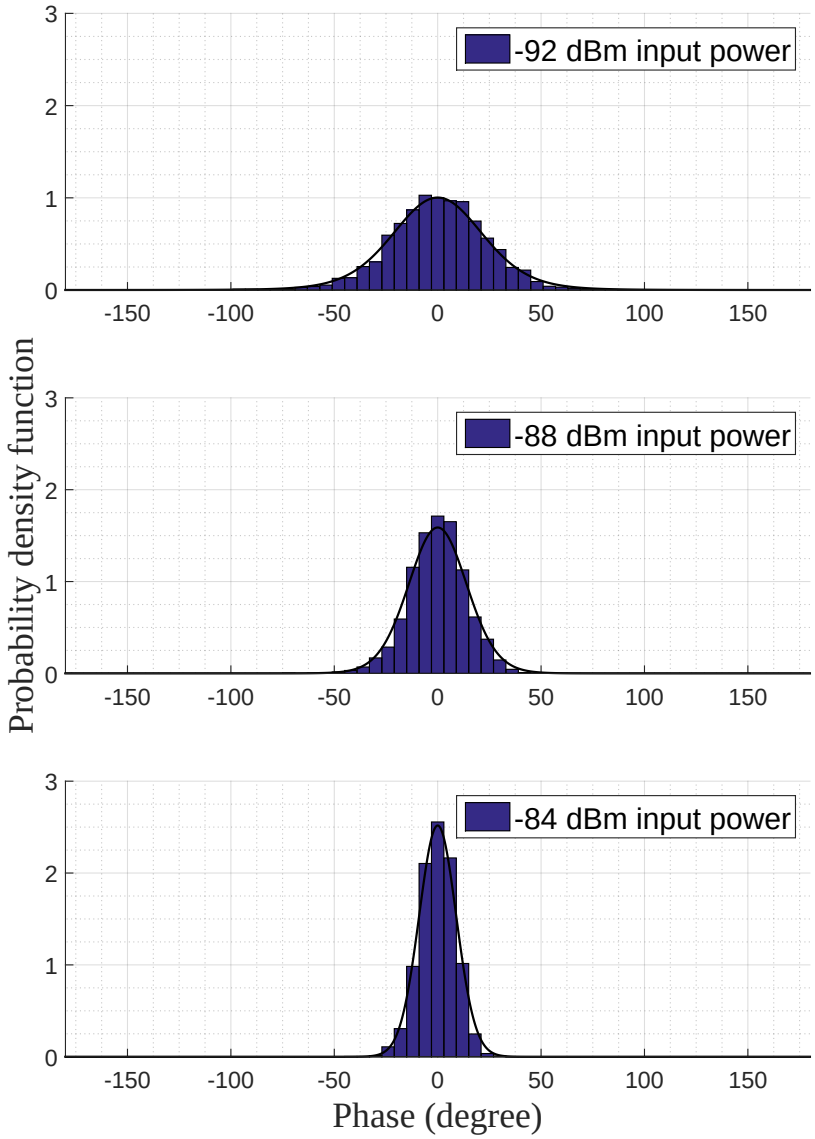


Figure 3.19: Measured and theoretical probability density function of the output waveform at different input powers.

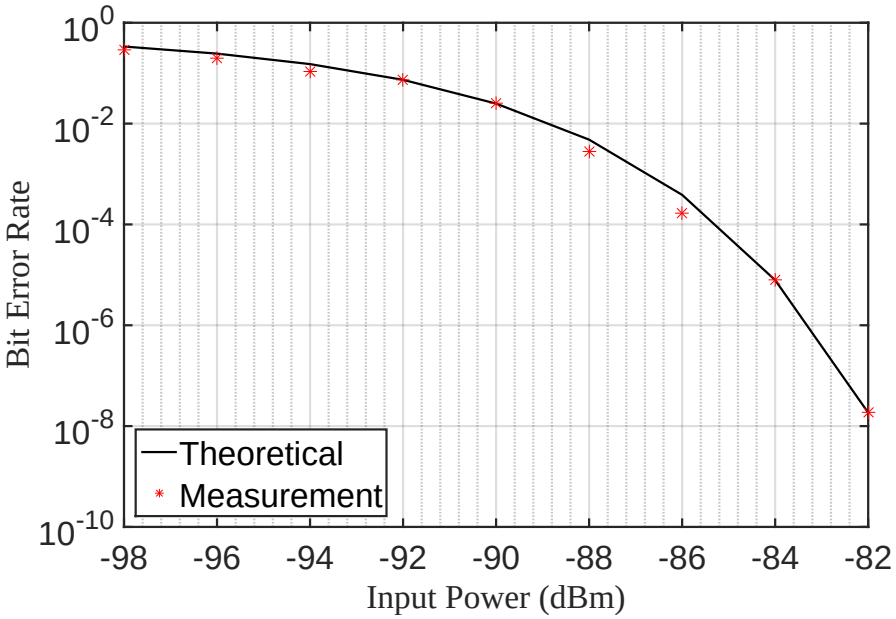


Figure 3.20: A comparison between the measured and predicted bit error rate for QPSK modulation.

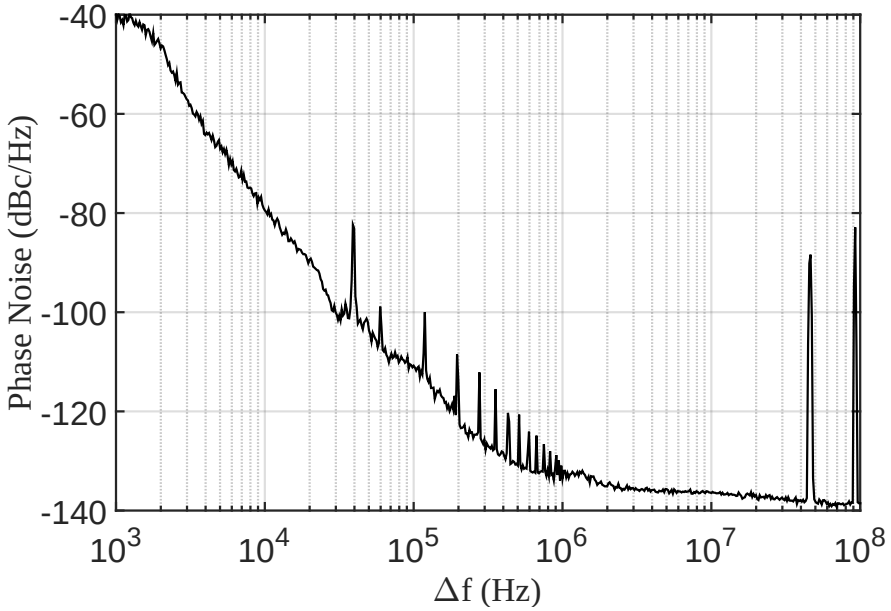


Figure 3.21: Phase noise measurement of the prototype SRA operating in the oscillatory mode.

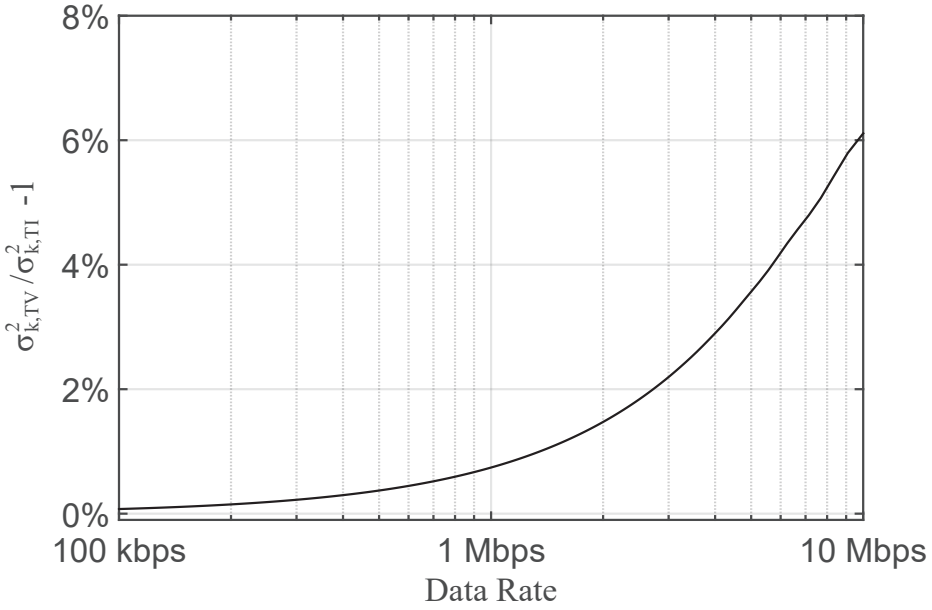


Figure 3.22: Difference between time-variant analysis and time-invariant analysis plotted versus data rate.

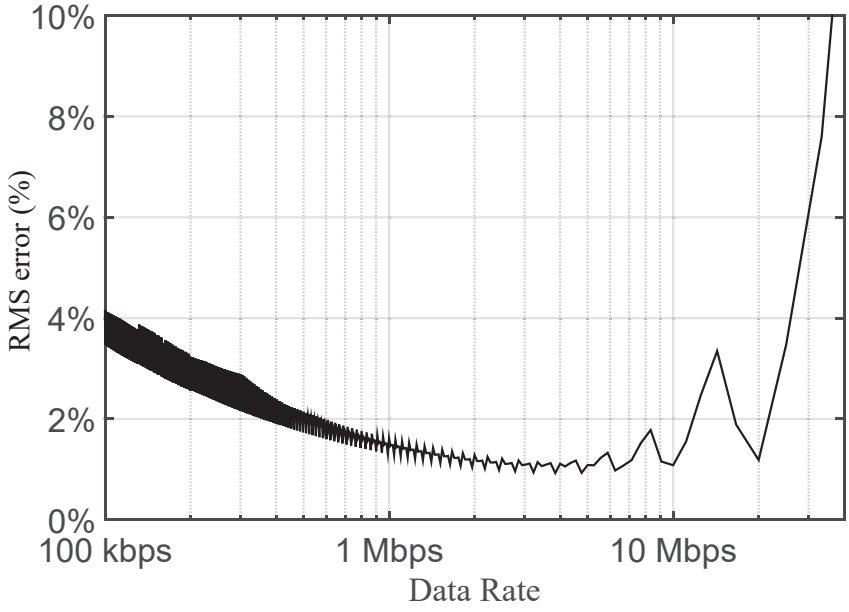


Figure 3.23: The solution (3.3) to the differential equation (3.2) is compared to the solution of the same differential equation based on numerical analysis.

Chapter 4

Active Mixer Adopted Sub-Sampling Phase-Locked Loop

4.1 Introduction

Energy efficient synthesis of high spectral purity reference frequencies and clocks is needed in high performance systems and applications ranging from wireless and wire-line communications to high-speed data conversion. The advent of 5G communication standards further necessitate a continued research in improving spectral purity of clocks in an energy-efficient manner. As a result, there continues to be significant interest in the design of efficient and low noise phase locked loop (PLL) architectures with minimal spurs.

Amongst recent efforts in the literature, two architectures stand out the most: injection-locked PLLs [47–52] and sub-sampling PLLs [5, 6, 53–62]. Both architectures have shown remarkable phase noise performance at potentially lower power than more conventional approaches. Injection-locked PLLs, first introduced in [47] and analyzed further in [48], injects the voltage-controlled oscillator (VCO) in the PLL with a buffered copy of the reference frequency to help reduce phase noise. Analysis and measurements show that in-band phase noise in such sub-harmonically injection-locked PLLs is dominated by the phase noise of the reference and the divisor number, N. Sub-sampling PLLs, on the other hand, eliminate the need for a divider by replacing a phase/frequency detector (PFD) with a sample-and-hold circuit sampling at rate set by the reference frequency; if the VCO is operating at an integer multiple of the reference frequency, no

divider is needed for proper circuit functionality [4]. The lack of divider helps to reduce in-band phase noise by a factor of N^2, while also eliminating the power consumption of the divider.

While the phase noise of these two PLL architectures approach the theoretical lower limit, they both suffer from large spurious tones, which may be problematic in many emerging performance communication systems. Specifically, injection-locked PLLs suffer from a large reference spur because the feedback path of the PLL and the feed-forward path of the injection locking do not work perfectly together without very careful timing calibration. For example, a state-of-art injection-locked PLL work in [63] achieved a 190 fs jitter and 2.3 mW for a figure of merit (FoM) of -251 dB at 6.8 GHz, yet with a spur of -40 dBc. Unfortunately, precise and robust calibration to reduce this spur is difficult, as the injection-locking mechanism is temperature sensitive. Sub-sampling PLLs, on the other hand, exhibit a large spur at the reference frequency due to various effects at the sampler, which will be described in more detail in Section II. For example, [4] achieved an rms jitter of 150 fs and 7.6 mW power for an FoM of -247.6 dB at 2.4 GHz, yet with a spur of -46 dBc. Calibration can help as described in [6], yet the improvement is at the expense of both power and performance.

This chapter presents the design of a sub-sampling PLL that leverages the noise and power benefits of the divider-less structure, yet reduces spurious tone content through an active-mixed-like structure in the phase detector. First presented in [55], this chapter offers a theoretical treatment of the approach, along with significantly expanded circuit design details and measurement results.

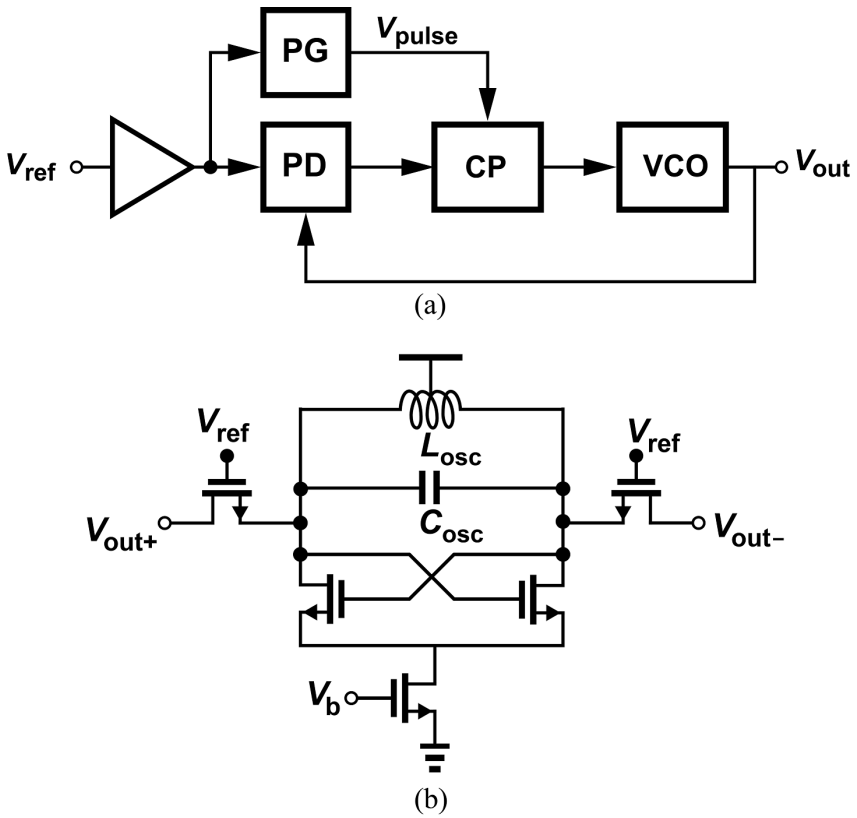


Figure 4.1: (a) A system diagram of conventional sub-sampling PLL [4] and (b) a detailed schematic of the voltage controlled oscillator (VCO) and the phase detector (PD).

4.2 Sources of the Reference Spur in Conventional Sub-Sampling PLLs & Mitigation Strategies

4.2.1 Sources of the reference spur

A conventional sub-sampling PLL architecture is shown in Fig. 4.1(a), while 4.1(b) shows the schematic of the associated VCO and sampling switches, based on [4]. The sub-sampling PLL architecture does not have a divider, and uses a phase detector to sampling the high frequency VCO output directly using a low frequency reference signal. The absence of divider leads to a higher phase detection gain, and thereby reduces the in-band phase noise contribution of the phase detector and charge pump. However,

the sub-sampling phase detector causes a large reference spur largely in three different manners, and Fig. 4.2 illustrates how these affect the VCO output.

The first major cause of the reference spur is the periodic unintended modulation of the VCO's resonant frequency. The sub-sampling phase detector consists of two passive-mixer like switches, and whenever the switches are turned on, the total capacitance of the VCO's resonant tank including all parasitic capacitance, C_1, sees an additional capacitance, C_S, which is the sampling capacitance at the output of the phase detector. This causes the instantaneous frequency (or phase) of the VCO to be modulated in a similar manner to binary frequency shift keying modulation. This is generally the biggest source of the reference spur in sub-sampling PLLs [6]. For example, when the switch is turned on, the resonator sees a total capacitance of:

$$C_{on} = C_{resonator} + C_{sampling} + C_{gd,on} + C_{gs,on}, \tag{4.1}$$

whereas when the switch is turned off, the resonator's total capacitance can be expressed as:

$$C_{off} = C_{resonator} + C_{gd,off}. \tag{4.2}$$

The difference can be expressed as:

$$C_{\Delta} = C_{sampling} + C_{gd,on} + C_{gs,on} - C_{gd,off}, \tag{4.3}$$

and the resulting spur can be calculated as [6]:

$$SP_{modulated} = 20 \log \Big[\sin (\pi \cdot D_{REF}) \cdot \frac{N}{2\pi} \cdot \frac{C_{\Delta}}{C_{tank}} \Big], \tag{4.4}$$

where D_{REF} is the duty cycle of the reference.

The second cause of spur is very much related to cause one: when the sampling switch is on, capacitors $C1$ and C_S share their charge, resulting in amplified spurious content at the reference frequency.

The third major cause of spur is due to the clock feed-through caused by parasitic capacitance across the sampling switch, C_P. While not as dominant as the modulation of the resonator's capacitance [6], this effect can still add considerable amount of spurious content. To put things into perspective, 30 fF of C_P with 3 pF of C_1 would result in 1 mV of clock feed-through at V_{VCO}, which would translate into -60 dBc of reference spur for a 1 V peak-to-peak V_{VCO}.

Clock feed-through is unfortunately difficult to mitigate. The on-resistance of the switching device and the sampling capacitor form an RC-pole, and this pole should be an order of magnitude higher than the loop bandwidth, lest it affect the phase margin of the PLL. In order to increase the corner frequency of this pole, either the switching device can be sized larger, or the sampling capacitance can be made smaller. In order to reduce the reference spur due to switching, the switch device itself can be made small. This means that the sampling capacitance also needs to be made smaller for phase margin concern as mentioned above. However, the size of the sampling capacitance is limited by the parasitic capacitance of input devices of the charge pump. Therefore, the sampling capacitance cannot be arbitrarily small, and the switching device must be kept large enough to drive the charge pump without introducing phase delay, and these large switches introduce significant parasitic capacitance.

The amplitude of the spur due to clock feed-through can be approximated as the voltage across the resonator capacitor C_1 due to the reference signal with amplitude V_{ref}:

$$SP_{modulated} = 20 \log \left[V_{ref} \cdot \frac{C_{parasitic}}{C_{parasitic} + C_1} \right]. \tag{4.5}$$

4.2.2 Prior-art mitigation technique I: VCO buffer

The original sub-sampling PLL work in [4] reports -46 dBc reference spur, and a -247 dB figure-of-merit (7.6 mW power, 150 fs rms jitter) when the switch and the VCO is isolated by a VCO buffer. The buffer can add a significant portion of noise, and its gate-width and current consumption must be kept sufficiently large in order to ensure

that the buffer's noise does not dominate the in-band phase noise. However, if the source follower input device is large, then its capacitance will also vary as the sampling switch alternates between on and off. Therefore, while using a VCO buffer may be the simplest solution, the buffer needs to consume a significant amount of power such that its noise is not affecting the performance of the PLL, and at the same time, its size must be kept small such that the spur is minimized. Furthermore, the buffer should be a power hungry source follower rather than a simple inverter so that the output waveform is sinusoidal for sampling purpose. Otherwise, the sharp transition of the output leads to a narrower lock range of the PLL. For these reasons, simply adding a VCO buffer is not a sufficient solution if power efficiency is also desired.

4.2.3 Prior-art mitigation technique II: a complementary dummy path

A lower-power manner to mitigate the BFSK-like reference spur is to utilize a dummy switch and dummy sampling capacitor, as proposed in [5]. Shown in Fig. 4.3, the phase of the VCO is nominally sampled onto a sampling capacitor C_S by M_1. In order to mitigate the BFSK effect, the total capacitance seen by the VCO should stay constant. Thus, a dummy path formed by M_2 and C_D, where M_2 is driven by an inverted reference clock and C_D is made as close to C_S as possible, will make the total resonator capacitance to be roughly equal to C_S nearly all the time.

While meaningfully effective, it is unfortunately difficult to precisely align the V_{ref} and $\overline{V_{ref}}$, which reduces the impact of the technique. Furthermore, as previously mentioned, C_S is usually kept very small to not degrade the loop phase margin, and is therefore difficult to match the sampling capacitor and the dummy capacitor. By getting rid of the power-expensive VCO buffer and employing the dummy technique, [5] reports a reference spur of -56 dBc, along with an FoM of -251.9 dB (2.5 mW power, 160 fs rms jitter).

4.2.4 Prior-art mitigation technique III: a tertiary delay-locked loop

In [6], the authors show that spur reduction can also be achieved by employing a delay-locked loop to align the falling edge of the Ref with the zero-crossing of the VCO output. If both edges are aligned, the VCO voltages at the rising and falling edges of Ref are ideally the same, and there is no charge-sharing between the VCO and the sampling capacitor, though BFSK-like effects could still occur. Fortunately, the rising edge of Ref is already aligned to the zero-crossing of the VCO by the sub-sampling PLL; unfortunately, without special consideration, the falling edge is not. This can be solved via a delay-locked loop (DLL).

Figure 4.4 shows the block diagram of the PLL in [6] where a DLL, formed by a phase detector (PD), a charge pump (CP), and a loop filter (LF), control the duty cycle of the reference clock so that the rising and falling edges are aligned to the VCO zero-crossing in order to prevent the charge sharing between the sampling capacitor and the resonator capacitor. The authors in [6] claim that if both rising and falling edges are aligned to the VCO's zero-crossing, then the voltage across the sampling capacitor remain the same at both sampling edges, and the charge-sharing effect is mitigated. A reference spur of -80 dBc was reported with an FoM of -244.6 dB (3.8 mW power, 300 fs rms jitter) was reported in [6] using this technique.

While [6] showed a very low reference spur, it should be noted that the reference spur is low even when the delay-locked-loop is turned off. The architecture already employs a VCO buffer and a dummy path technique, the former of which provides a significant spur reduction. However, as explained in the prior subsection, using a VCO buffer comes with a trade-off between noise, power, and reference spur, and this work achieves an excellent spur and power at the expense of phase noise performance.

4.3 Proposed Active-Mixer Adopted Sub-Sampling (AMASS) Phase Detector

4.3.1 Step 1: Rotating the Switch

In order to alleviate the modulation of the resonator's capacitance and the charge disturbance on it, the VCO must be isolated from the sampling system in some way. Rather than add a power-consuming and noise-adding VCO buffer, it can be noted that the sub-sampling phase detector switch is, to a first order, a 3-port multiplier, where the gate and the drain multiply together to create an output at the source. The idea here then, as illustrated in Fig. 4.5, is to change the orientation of the sampling switch so that the VCO output is connected to the gate of the switching device, rather than to its drain or source. This helps to isolate the VCO from the sampling capacitance, reducing BFSK-like effects.

However, simply swapping the inputs of the phase detector without further modifications causes several practical difficulties. Most importantly, the phase detector is supposed to sample the output of the VCO once every reference cycle. However, if the gate of the sampling device is driven by the VCO output, the switch will turn on more than once per reference cycle. More specifically, the switch will turn on even when the phases of the VCO and the reference aren't supposed to be compared, thereby generating false outputs. This also causes bias currents to flow, which increases power consumption. As a result of these issues, this new phase detector needs to be modified to also perform the hold operation in order to ensure that the output voltage only reflect the correct comparison of phases during each reference cycle, while also finding a way to reduce power consumption.

4.3.2 Step 2: Adding a Sampler

Figure 4.6 shows a possible way to solve this problem by employing another switch to perform hold operation. Here, C_1 represents the total capacitance of the VCO, and C_P is the parasitic capacitance of the phase detector. The first sampling device M_1 is now a PMOS, so that the first stage resembles a single-balanced active mixer. R_s and C_s provide the load to attenuate higher harmonic component, while transistor M_2 performs the hold operation.

This new phase detector provides two major advantage over the conventional passive mixer based approach. The first advantage is that the sampling capacitance is now detached from the VCO and its size can be arbitrarily large (at the expense of more power consumption). The second is that there is no more charge sharing between C_1, the resonator capacitor, and other capacitors. Furthermore, the BFSK modulation of the resonator capacitance is significantly reduced because C_1 is no longer periodically connected to any capacitor.

However, two problems still remain. Parasitic capacitor C_p still changes as the gate-to-source voltage of M_1 changes, so that the capacitance modulation effect isn't completely removed. Furthermore, clock feed-through from V_{ref} to V_{vco} still exists.

Equation (4.4) show that the reference spur is a function of the duty cycle of the reference, the division ratio between the reference and the LO, and the ratio between the change in capacitance to the total resonator capacitance. As a designer, it is difficult to control N and C_{tank} for a given PLL architecture and high-performance VCO. Fortunately, D_{ref} does not affect the performance of the sub-sampling PLL and is therefore accessible to change.

Figure 4.7 shows a plot of simulated reference spur of a free-running 2.4 GHz VCO that is driving a sub-sampling phase detector with a 100 MHz sampling frequency. The pulse-width of the 100 MHz reference clock is varied from 100 ps to 5 ns. The resulting plot is not monotonic because the amplitude to phase conversion from clock feed-through is a time varying effect [64], and the phase sampling does not occur at the

same phase of the LO for various pulse-widths in simulation when the VCO is free-running. However, a trend can still be observed that as the pulse-width is reduced, the reference spur is also reduced. This is because reducing the duty cycle of the reference can mitigate two of the three causes of spurs. First, in the extreme case of using a delta function as a reference, the BFSK modulation of the reference frequency also becomes negligible as the reference frequency is changed only for infinitesimal duration. Secondly, a Fourier series expansion of a pulse with pulse width of τ shows that the first harmonic term is:

$$f(t) = \frac{2}{\pi} \sin\left(\frac{\pi\tau}{T}\right) \cos\left(\frac{2\pi t}{T}\right), \tag{4.6}$$

and the amplitude of the first harmonic term is proportional to τ when $\frac{\tau}{T}$ is very small. Therefore, the clock feed-through effect is also mitigated as the duty cycle is reduced according to Eqn. (4.4).

4.3.3 Final Phase Detector Circuit

The actual implementation of the active phase detector is shown in Fig. 4.8. Interestingly, using an active mixer as a phase detector used to be quite common, albeit not necessarily for sub-sampling PLLs [65]. Additionally, the active phase detector employed here is a bit different from a conventional active mixer, as it is heavily duty cycled using an inverter B_1. The inverter is part of a pulse generator that generates a narrow-width pulse from a clean reference source such as a crystal oscillator or another PLL. Transistor M_1 and M_2 form input devices. While not shown, their inputs are biased using a DC bias resistor, and the VCO output is connected to the input devices via coupling capacitors. Transistors M_3 and M_4 perform the hold operation, and R_s is sized such that the DC value of V_{out} is adequate for next stage. Capacitor C_s is sized so that high frequency component is filtered, but the pole formed by R_s and C_s is at least an order of magnitude higher than the PLL loop bandwidth frequency to not affect the loop stability. Since the entire active mixer is duty-cycled by the narrow pulse, its power consumption and spur contribution are low.

4.4 Circuit & System Description

Figure 4.9 shows a schematic of the proposed active-mixer adopted sub-sampling PLL (AMASS-PLL). Compared to the conventional architecture shown in Fig. 4.1(a), the proposed AMASS-PLL uses the output of a pulse generator (PG) as the reference for the entire system. Therefore, the design of the pulse generator is critical to the overall performance of the system. In a conventional SSPLL, a charge pump is used to perform the hold operation. However, both sample and hold operation are performed by the phase detector in AMASS-PLL, and the charge pump is replaced by a G_m-cell. The advantage of using a G_m-cell rather than a charge pump will be described in the following sub-sections. Lastly, a sub-sampling PLL is a type-I PLL, and has a limited locking range. Therefore, an additional frequency locked loop (FLL) is needed, and the VCO used in AMASS-PLL is a hybrid structure with coarse 6-bit digital tuning for frequency locking, while fine analog tuning is reserved for phase locking. A more detailed description will be given in the following sub-sections.

4.4.1 Pulse Generator

Since there are not many sources of noise in an SSPLL, reference noise can easily become the dominant source of in-band phase noise. This is especially true since the in-band noise contribution of the phase detector and charge pump (or G_m cell in the case of AMASS-PLL) are not multiplied by N. Thus, one downside of using a pulse to sample the phase detector is that the pulse generator adds more noise to the possibly dominant source of noise. Therefore, the design of pulse generator becomes critical to the noise performance, and the rise and fall time should be as sharp as possible to reduce the amplitude-to-phase conversion of noise from the pulse generator. In the prototype design, the rise and fall time was designed to be about 10 ps in 65 nm CMOS technology.

Figure 4.10 shows the schematic of the employed pulse generator. The first four parallel inverters are used to transform a sinusoidal signal from an external crystal

oscillator into a square wave. Then, a square wave, Y, and its delayed version, X, are given to a NAND gate to generate an inverted waveform of a narrow-width pulse. Inverter B_1 is then used to transform $\overline{V_{pul}}$ into a narrow pulse and is the same inverter that is used to drive the phase detector in Fig. 4.8. The pulse width can be tuned from 80 ps to 140 ps by a 3-bit control signal, V_{pc}, to a capacitor bank, C_b. The control signal V_{pc} is converted from binary to thermometer code, and eight unit-size capacitors with NMOS switches are used to form the capacitor bank.

It is worth mentioning the sizing choice of the NAND-gate of the pulse generator for optimal rise and fall time of the pulse output. As shown in Fig. 4.10, the rising edge of Y and the falling edge of X determine the falling and rising time of $\overline{V_{pul}}$ respectively. Therefore, it makes sense that M_1 in Fig. 4.11 is sized much bigger than M_2 to ensure that the rising edge of $\overline{V_{pul}}$ is sharp as X is turned off. Similarly, one might think that as X's rising edge arrives earlier than Y's rising edge, it would make sense for M_3 to be located closer to the ground in order to discharge the intermediate node Z earlier. However, in 65-nm process, PMOS is much weaker than the NMOS, and sizing M_1 bigger is not enough to make he rising edge sharper. Therefore, M_3 is placed closer to the output to help $\overline{V_{pul}}$ rise faster as well.

4.4.2 Phase Detector

Figure 4.12 shows a half circuit schematic of the pulse generator of Fig. 4.8, along with waveforms at the nodes of interest. When V_{pul} goes high, transistor M_2 starts to conduct a current with amplitude proportional to $V_{pul} - V_{in}$. V_X is therefore proportional to V_{in} and R_S while the pulse is high. C_s is only meant to filter unwanted high-frequency components and should be kept small to not affect the loop stability. While M_2 conducts a current, M_4 is also on, so that V_{out} is the same as V_X. When V_{pul} becomes low, there is no longer a current flowing into V_X and the charge across C_s is discharged. However, V_{out} remains the same because M_4 also no longer conducts current.

It is important to note that the on-resistance of M_4 can form another pole with the sampling capacitance of the next stage at V_{out}. In AMASS-PLL, the next stage is a G_m cell, and the sizes of its input devices cannot be too big or the stability of the loop is affected. In order to ease the constraint, M_2 and M_4 can be made bigger at the expense of more power consumption.

4.4.3 Gm Cell and Loop Filter

Due to the aforementioned restriction on the size of the input device of the G_m cell, M_1 and M_2 in Fig. 4.13 are kept small. As a result, the overall transconductance is small. In order to increase the effective g_m, a current mirror amplifier topology is used for the first stage of the G_m cell. The first stage amplifies current by ratio between $M_{5,6}$ and $M_{7,8}$, effectively increasing the g_m of the overall structure. $M_{3,4}$ sink current in order for $M_{5,6}$ to be able to conduct more current. M_7, M_8, M_9, and M_{10} form a differential to single-ended amplifier. A pseudo-differential topology without a current source was used to improve the output swing.

The transconductance amplifier is loaded by the PLL's loop filter, which is composed of R_{LF} and C_{LF}. The secondary capacitor is not necessary because of the additional pole introduced by the phase detector's R_s and C_s from Fig. 4.12.

4.4.4 Hybrid VCO/DCO and FLL

Figure 4.14 shows the schematic of the hybrid oscillator used in the PLL design. A PDK inductor was used for L_1. As previously mentioned, a sub-sampling PLL is type-I and require a separate frequency locked loop. Therefore, the oscillator is designed with both analog and digital tunability. Here, C_1 and C_2 are varactors, and V_X is generated from the G_m cell of the PLL to achieve fine tuning, while C_3 and C_4 are each 6-bit digitally tuned capacitor banks, whose control signals are generated by a separate frequency-locked-loop. C_3 and C_4 are sized such that these capacitors achieve coarse tuning with the help of the frequency locked loop.

The FLL is composed of a divider, frequency detector, an accumulator, and a multiplexer (MUX) [66, 67]. The MUX circuit takes an input from the FLL and hold its value for one cycle. Once the SSPLL achieves a lock, the MUX holds its output value, and the FLL can be turned off. The lock range of the AMASS PLL can be estimated as follow:

$$\Delta\omega_{max} = \pi K_{PD} K_{VCO}. \tag{4.7}$$

Since the response of a sub-sampling phase detector is a sinusoidal, the maximum phase difference that can be detected is $\pi/2$. Therefore, the voltage at the input to the VCO becomes $\pi/2K_{PD}$, and the corresponding maximum deviation in frequency is $\pi/2K_{PD}K_{VCO}$. The lock range is twice as the deviation can be either positive or negative.

Figure 4.15 shows a unit cell capacitor used in the 6-bit capacitor banks, C_3 and C_4. The size of M_1 is made sufficiently large so as to ensure that the quality factor of the capacitor bank is high. Otherwise, the capacitor bank will degrade the loaded Q-factor of the VCO and hurt the phase noise performance. The size of the buffer driving the transistor M_1 should also be large or the parasitic capacitance of M_1, C_{gd}, in series with the output resistance of the buffer will form a poor Q-factor parasitic capacitance and hurt the overall Q-factor of the tank. In order to ensure the monotonicity of the capacitance value, the capacitor bank is implemented in thermometer code. A thermometer encoder converts 6-bit binary input to thermometer codes R_N and C_N which represent n^{th} row and n^{th} column, respectively.

4.5 Phase Domain Model

Since there are several material changes to the structure of a conventional SS-PLL, it is worth constructing an analytical model of the proposed AMASS PLL in order to aid the designer in loop optimizations.

A phase-domain model of the AMASS PLL is shown in Fig. 4.16. Here, $F(s)$

represents the combined frequency response of the phase detector, the amplifier (G_m cell), and the loop filter.

The active mixer-based phase detector can be modeled as a sinusoidal phase detector with a pole formed by the load, followed by a zero-order-hold response from its sample-and-hold switches:

$$F_{PD}(s) = \frac{K_{PD}}{1 + s/\omega_{p2}} \frac{1 - e^{-sT}}{sT}, \tag{4.8}$$

where T is the period of the reference, K_{PD} is the phase detector gain, and ω_{p2} is the output pole of the active mixer. The amplifier's frequency response can be expressed as:

$$F_{gm}(s) = \frac{A_0(1 + s\omega_{z1})}{1 + s/\omega_{p1}}, \tag{4.9}$$

and the combined transfer function is:

$$F(s) = \frac{K_{PD}A_0(1 + s\omega_{z1})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}, \tag{4.10}$$

where the zero-order-hold response is ignored as we assume that the frequency of interest is much lower than the reference frequency. It should be noted that the active mixer contributes a pole at ω_{p2} so that the loop filter shown in Fig. 4.13 does not require an additional capacitor in parallel to the series R_{LF} and C_{LF}.

The overall frequency response here is similar to the charge-pump-based type-II PLL; however, the amplifier is not an integrator, and therefore the low-frequency gain is not as high as having a true integrator. Still, a designer can design the location of ω_{p1} to be as low as possible since the thermal noise of the amplifier is no longer the most dominant source of low frequency phase noise, and the only restriction on the amplifier is its frequency domain gain response.

It is straightforward [68] to calculate the loop gain, $T(s)$, to be:

$$T(s) = F(s)\frac{K_{VCO}}{s}, \tag{4.11}$$

and the closed loop transfer function, $H(s)$, to be:

$$H(s) = \frac{T(s)}{1 + T(s)} = \frac{K_{VCO}F(s)}{s + K_{VCO}F(s)}. \tag{4.12}$$

Figure 4.17 shows the phase domain model of the AMASS PLL with noise sources of interests. $\Phi_{n,pg}$ represents the input-referred phase noise of the pulse generator, and $\Phi_{n,amp}$ represents the input referred phase noise of the amplifier and phase detector. $\Phi_{n,vco}$ and $\Phi_{n,pg}$ are the phase noise of the VCO and the crystal oscillator respectively. The transfer function between the output phase noise and each noise source can be calculated. The transfer function between the output noise and the noise of the pulse generator or the input reference is

$$H_1(s) = \frac{\Phi_{out}}{\Phi_{in}} = \frac{N \cdot T(s)}{(1 + T(s))}. \tag{4.13}$$

The transfer function between the amplifier noise and the output phase noise can be expressed as

$$H_2(s) = \frac{\Phi_{out}}{\Phi_{n,amp}} = \frac{T(s)}{(1 + T(s))}. \tag{4.14}$$

Lastly, the transfer function between the VCO and the output phase noise is the error transfer function:

$$H_3(s) = \frac{\Phi_{out}}{\Phi_{n,vco}} = \frac{1}{(1 + T(s))}. \tag{4.15}$$

Figure 4.18 shows a plot of the above transfer functions for the prototype AMASS-PLL designed in 65 nm CMOS, and the phase noise contribution of each block is shown in Fig. 4.19. It is important to note that the reference noise is multiplied by N, and therefore, the reference noise tends to become the most dominant noise source. In light of this, the loop bandwidth should be chosen so that the noise due to the reference is about the same as the noise due to the VCO at the loop bandwidth [69].

Table 4.1: Comparison With State-of-the-Art Integer-N PLLs.

	[4] JSSC '09	[6] JSSC '10	[5] VLSI '10	[63] JSSC '15	[54] JSSC '18	**This Work**
Technology(nm)	180	180	180	65	65	**65**
Supply(V)	1.8	1.8	1.8	0.9	0.8	**1.0**
Power(mW)	7.6	3.8	2.5	2.3	1.1	**0.9**
RMS Jitter(fs)	150	300	160	190	162	**161**
Int. Window(Hz)	10k-40M	10k-100M	10k-100M	10k-40M	10k-100M	**10k-100M**
Spur (dBc)	-46	-80	-56	-40	-65	**-67**
Output Freq.(GHz)	2.21	2.21	2.21	6.8	5.0	**2.4**
Ref. Freq. (MHz)	55.25	55.25	55.25	106.25	100	**100**
Architecture	SSPLL	SSPLL	SSPLL	ILPLL	SSPLL	**SSPLL**
Oscillator	LC	LC	LC	LC	LC	**LC**
Area (mm^2)	0.18	0.2	0.2	0.25	0.01	**0.42**
PLL FOM (dB)	-248	-244	-252	-251	-255	**-256**

4.6 Measurement Results

A prototype of the AMASS-PLL was implemented in 65 nm CMOS process; a die photo is shown in Fig. 4.20. The chip occupies a core area of 0.43 mm^2, nominally operates at 1 V, and consumes 0.93 mW. The pulse generator and the mixer together consume 390 μW, the amplifier consumes 27.5 μW, and the VCO consumes 510 μW. An external crystal oscillator (Sprinter model from Wenzel Associates) was used to supply a 100 MHz reference clock to generate a 2.4 GHz output from the PLL. This same model of crystal oscillator was used for measurement in the original sub-sampling work [5].

Figure 4.21 shows the phase noise of the AMASS PLL measured by an Agilent E5052B signal source analyzer. When integrated from 1 kHz to 100 MHz, the rms jitter is 174 fs, which is the number reported in the original paper in [55] (there was a typo in the frequency range). When integrated from 10 kHz to 100 MHz, which is the same range most other prior art uses, the rms jitter is 161 fs, which results in an FoM of -256 dB. The reference spur was read out directly from the E5052B, and was measured to be -67 dBc.

These measurements shows that the AMASS-PLL improves the prior design in [5] by reducing the spur by at least 10 dB and the figure-of-merit by more than 3 dB simultaneously. Compared to [54], which uses the same dummy path technique as [5],

but with better matching and smaller phase detector devices, AMASS-PLL achieves a 2 dB spur improvement and an FoM improvement of up to 1 dB, albeit at a larger occupied area. Table I summarizes the performance of the AMASS-PLL with other state-of-art integer-N PLLs. To the author's best knowledge, the AMASS-PLL achieves the lowest FoM amongst prior-art, while consuming low power with reasonable spur levels.

Figure 4.22 shows the comparison between the phase noise of the VCO under locked and free-running conditions. The high-frequency phase noise of the PLL is higher than the phase noise of the free-running VCO because the pulse generator adds additional noise, which is then multiplied by N, and not sufficiently low-pass filtered as shown in Fig. 4.19. The overall phase noise is dominated by the pulse generator, and its phase noise can be improved by scaling the devices larger at the expense of consuming more power.

Figure 4.23 shows the measured phase noise and reference spur versus the supply voltage. As the supply voltage decreases, the VCO phase noise adversely affect the noise performance. At higher supply voltage, the loop bandwidth of the system starts to change and degrades the total integrated phase noise. However, the integrated jitter still remains lower than 200 fs for a wide range of supply voltages. On the other hand, the spur is reduced monotonically as the supply voltage is scaled. This is likely due to the fact that the sampling mechanism, which is the dominant source of the spur, does not scale with the supply voltage, whereas the VCO amplitude increases with the supply voltage. Another explanation is that the increased supply voltage increases the linearity of the phase detector, which in turn reduces the reference spur.

Figure 4.24 shows the measured reference spur and the integrated jitter of the PLL as the pulse-width is varied from 80 ps to 150 ps. As previously mentioned, the pulse-width is controlled by tuning 3-bit mim capacitor bank to tune the delay of the pulse generator. The pulse width increases as the control word increases from 0 to 7.

4.7 Conclusion

This paper has presented a new phase detector to reduce the spurious tone of a sub-sampling PLL architecture by replacing the passive mixer switches with a duty-cycled active mixer. By removing unnecessary blocks that may contribute to additional noise and spurs, the fabricated prototype achieves -67 dBc spurious tone and an FoM of -256 dB when the jitter is integrated from 10 kHz to 100 MHz. To the best of the authors' knowledge, this represents the best figure-of-merit reported amongst all PLL architectures, with lower spurious tone performance compared to prior designs with similar FoMs.

4.8 Acknowledgement

Chapter 4, in part, is a reprint of the material as it appears in D. Lee and P. P. Mercier, "AMASS PLL: An Active-Mixer-Adopted Sub-Sampling PLL Achieving an FOM of 255.5dB and a Reference Spur of 66.6dBC," 2018 IEEE Symposium on VLSI Circuits, Honolulu, HI, 2018, pp. 181-182. The dissertation author was the primary author of this paper. The rest of the chapter that is not part of the reprint is in revision process for submission to Journal of Solid State Circuits.

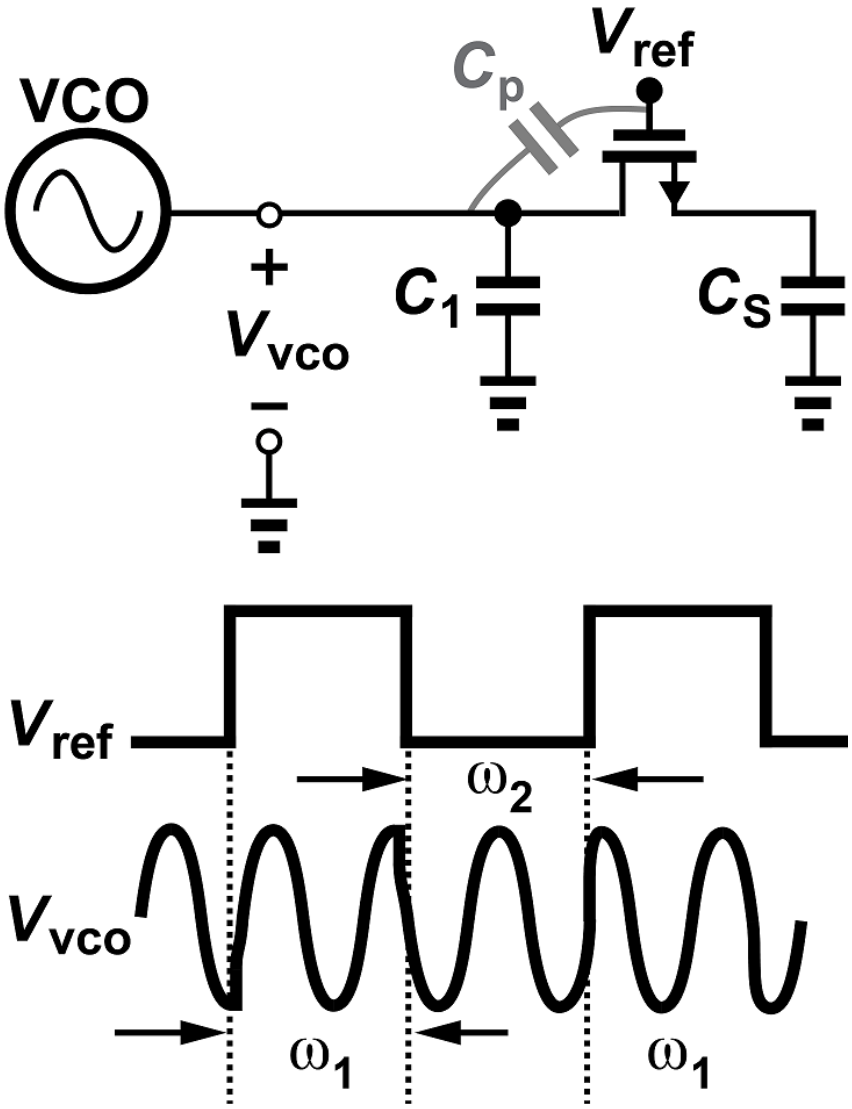


Figure 4.2: Illustration of sources of spur caused by the phase detector.

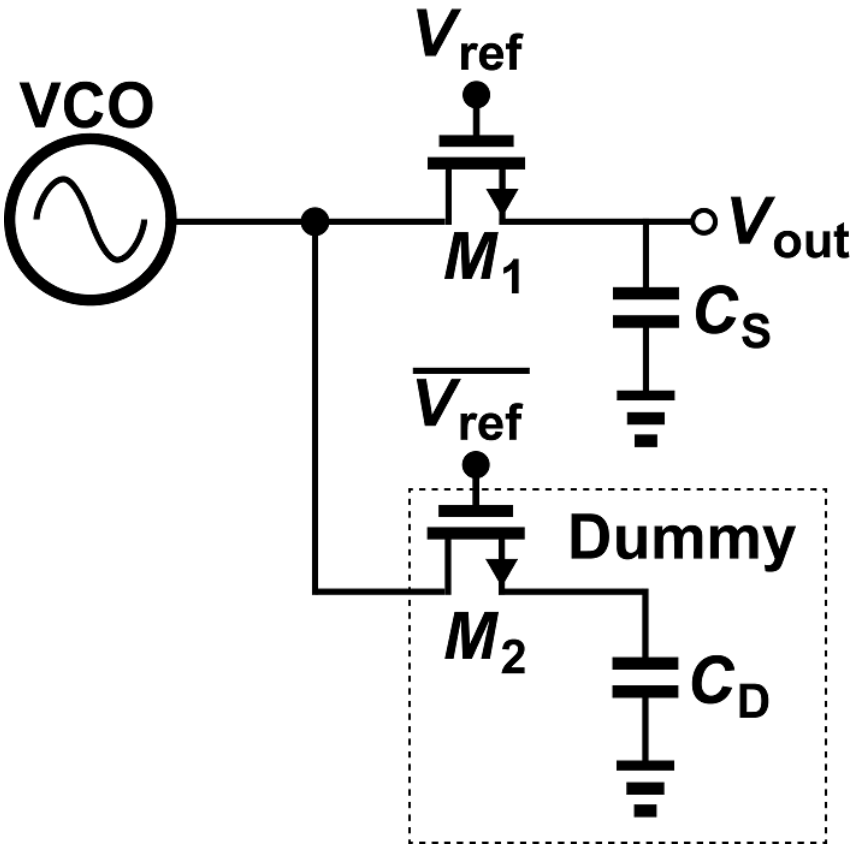


Figure 4.3: A dummy path technique for spur reduction [5].

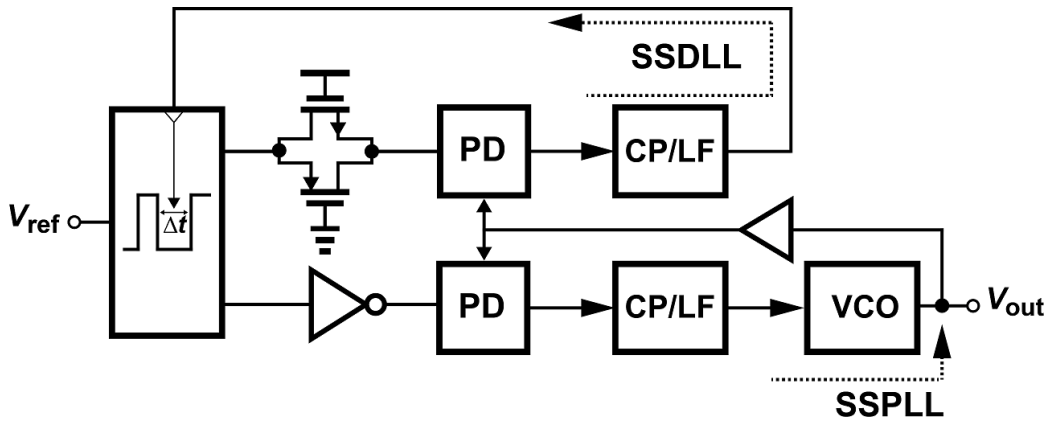


Figure 4.4: A DLL based spur-reduction technique. [6].

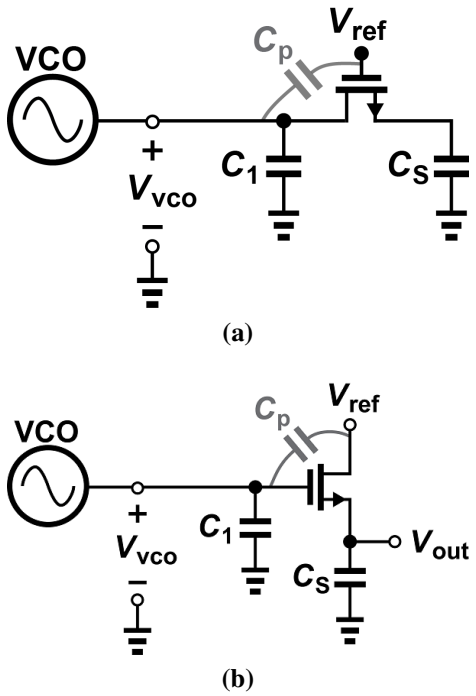


Figure 4.5: (a) A schematic of a conventional sub-sampling phase detector. (b) A schematic of the sub-sampling phase detector with swapped orientations of input and reference

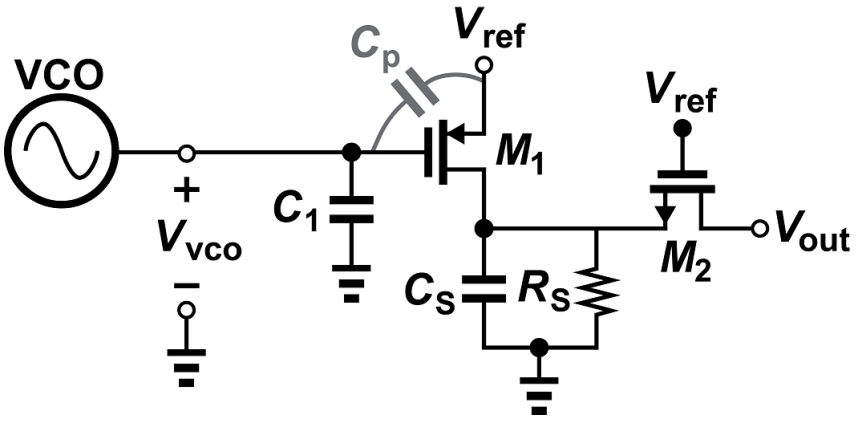


Figure 4.6: The new phase detector with hold operation.

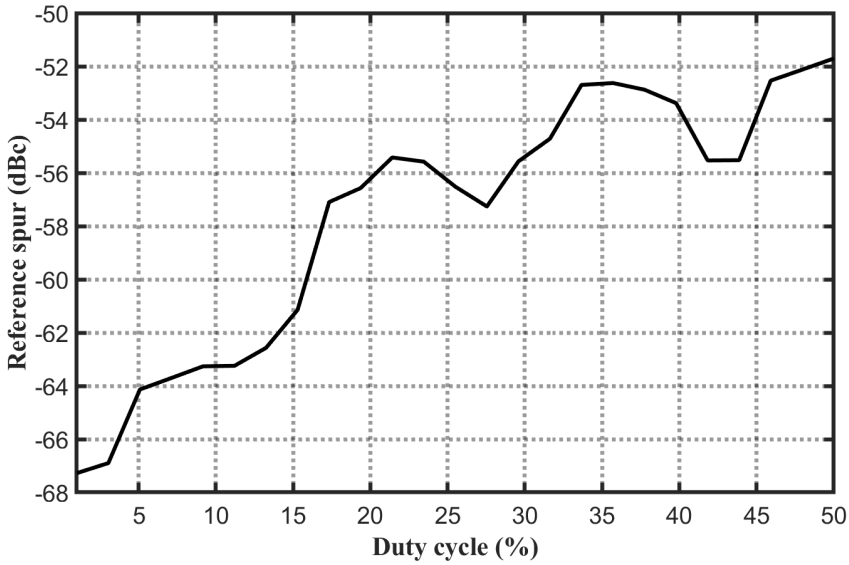


Figure 4.7: A simulated reference spur versus the duty cycle of reference clock

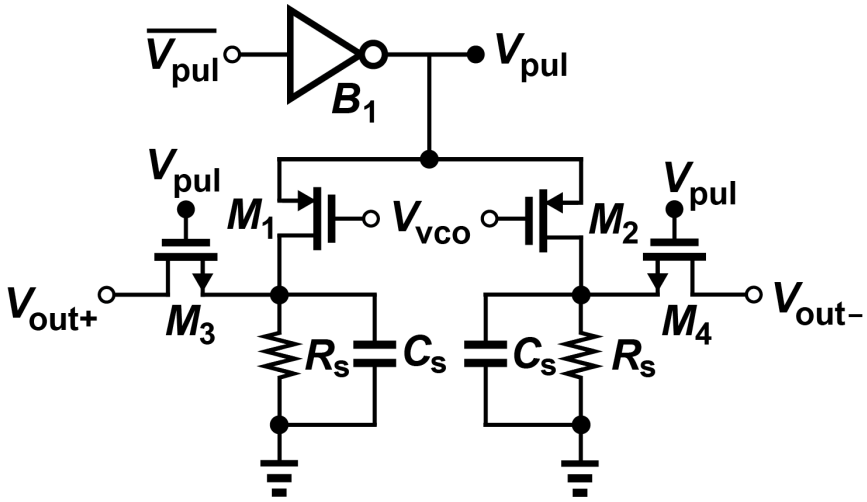


Figure 4.8: The final implementation of the proposed phase detector

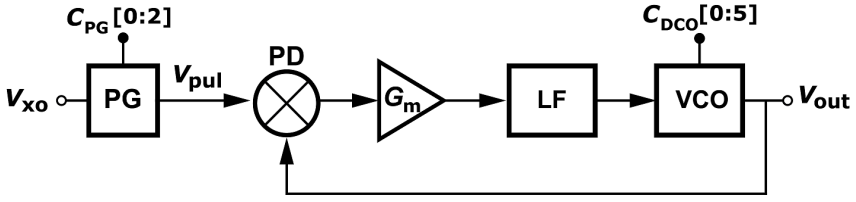


Figure 4.9: A Schematic of the AMASS-PLL

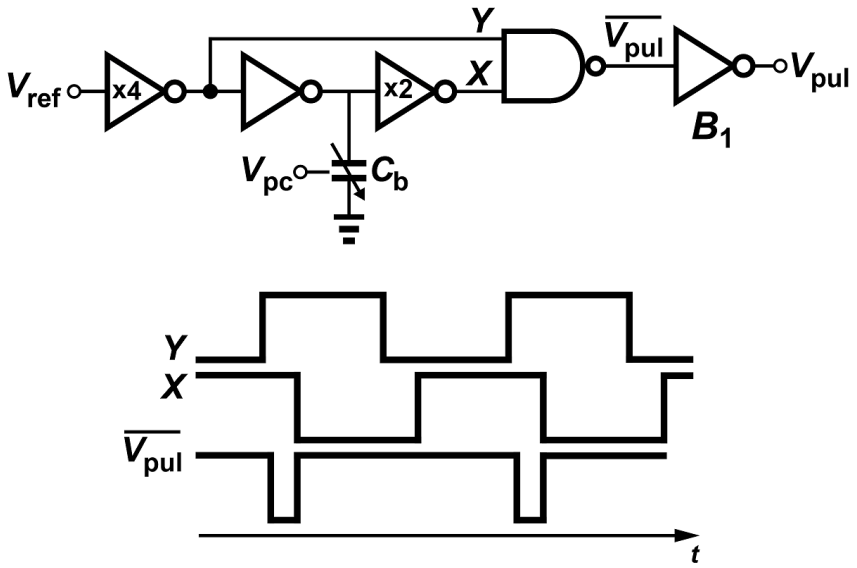
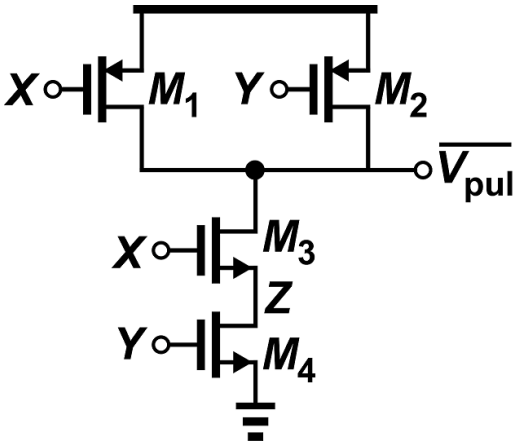


Figure 4.10: A schematic of the pulse generator and waveforms of interest



	$W\ (\mu m)$
M_1	112.5
M_2	22.5
M_3	45.0
M_4	63.0

Figure 4.11: A schematic of the NAND-gate in the pulse generator and the size of each transistor.

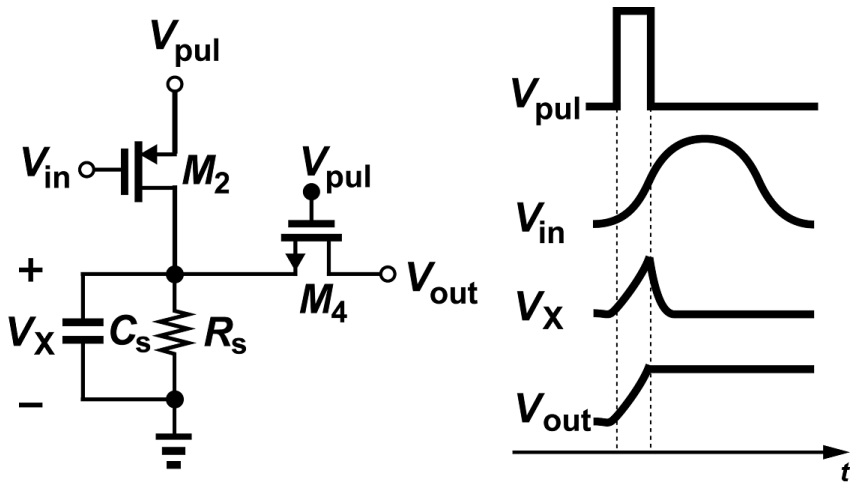


Figure 4.12: A half circuit schematic of the pulse generator and waveforms of interest.

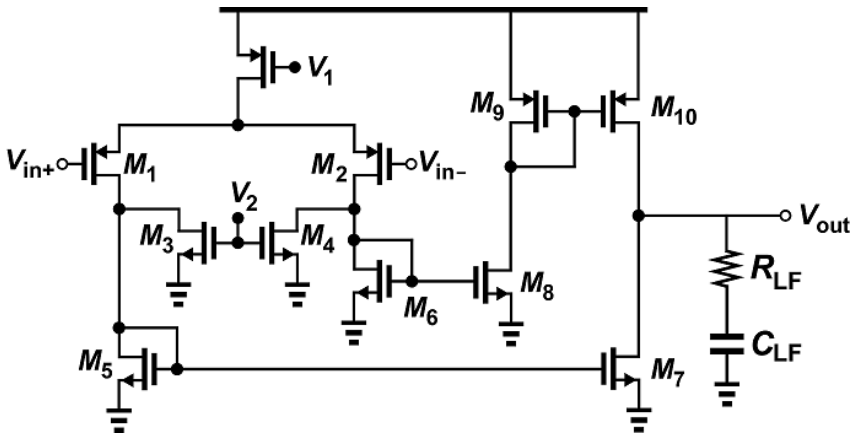


Figure 4.13: A schematic of the transconductance amplifier.

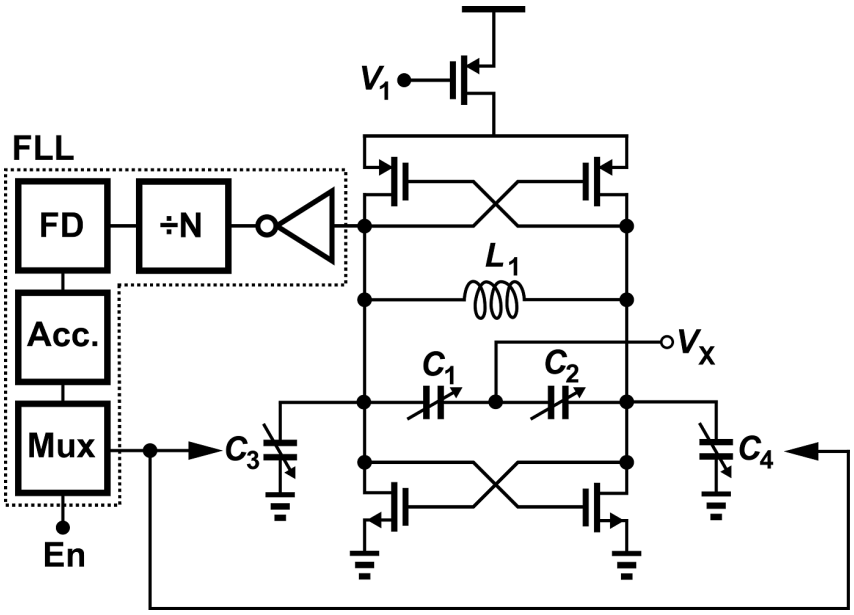


Figure 4.14: A Schematic of the hybrid VCO/DCO.

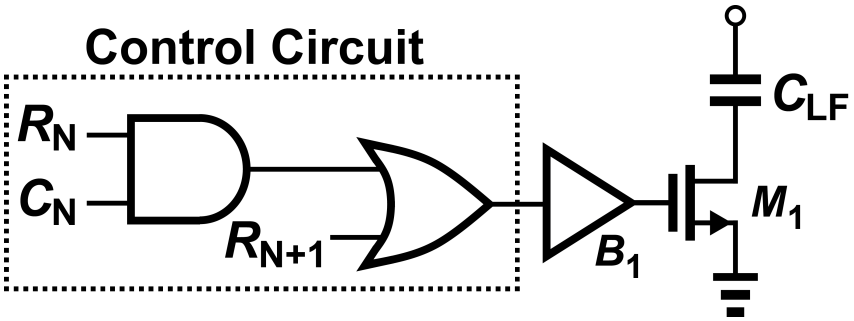


Figure 4.15: Capacitor Bank for DCO.

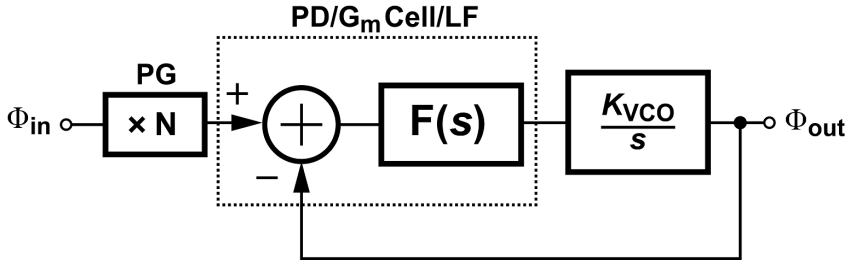


Figure 4.16: Frequency domain model of the AMASS-PLL.

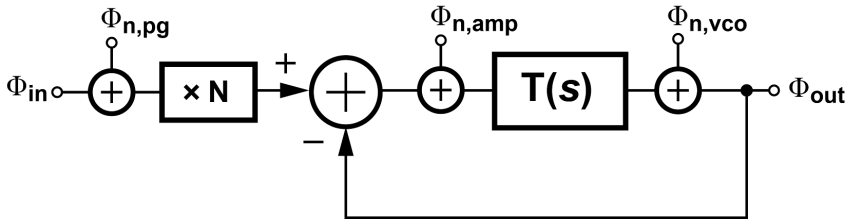


Figure 4.17: Phase domain model of the AMASS PLL with noise sources of interest.

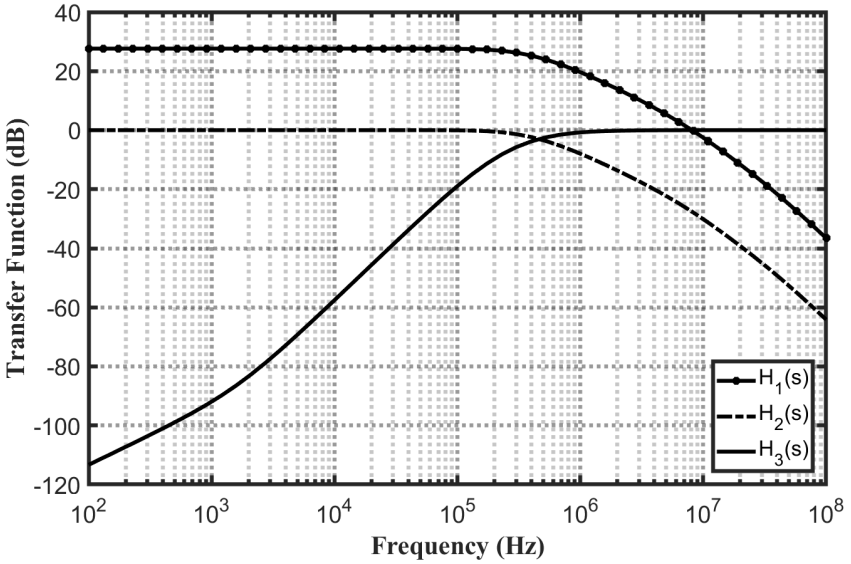


Figure 4.18: The noise transfer functions of the prototype AMASS-PLL.

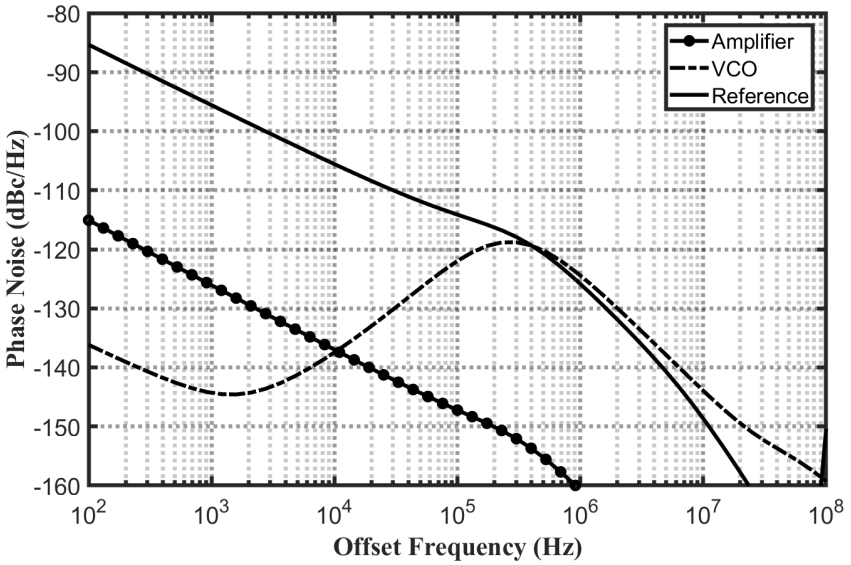


Figure 4.19: The simulated phase noise contribution of each block of the prototype AMASS-PLL.

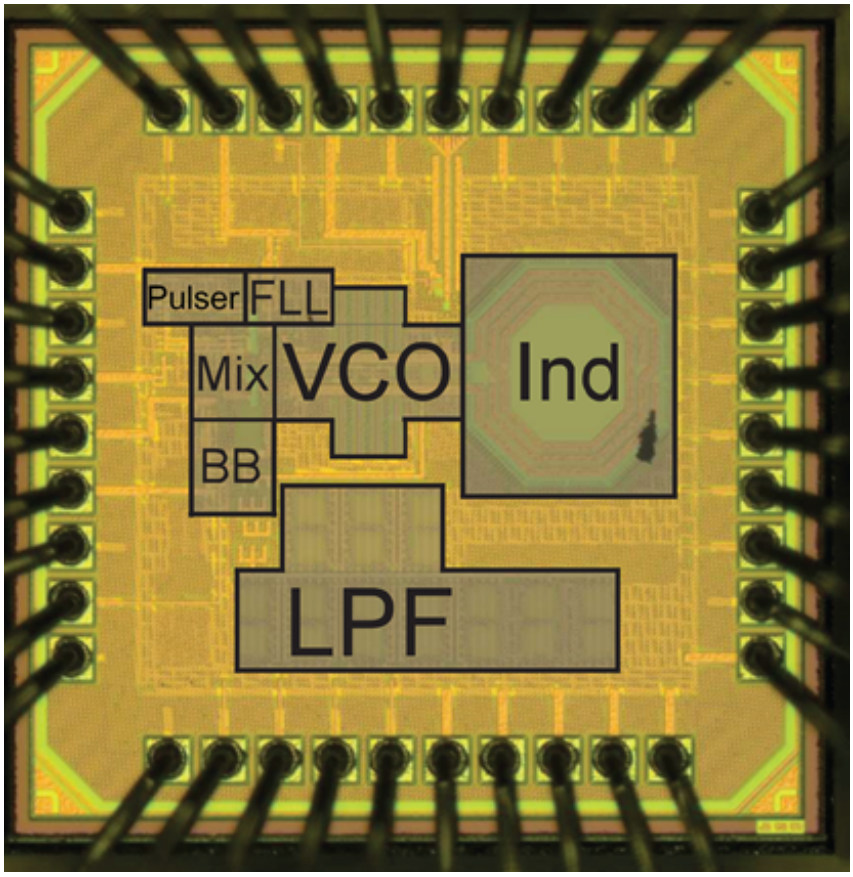


Figure 4.20: A die photo of AMASS-PLL prototype

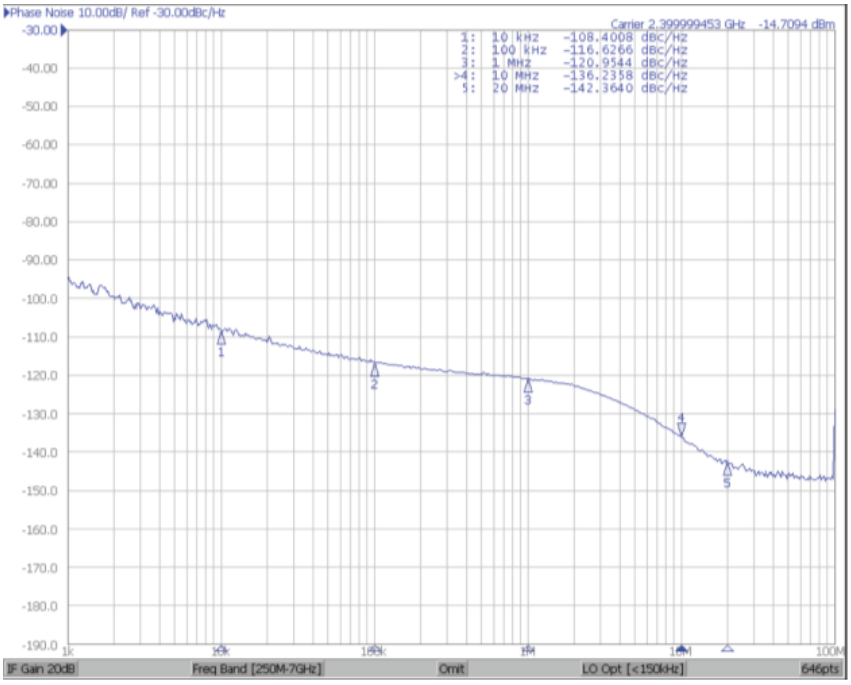


Figure 4.21: The measured phase noise spectrum from Agilent E5052B Signal Source Analyzer

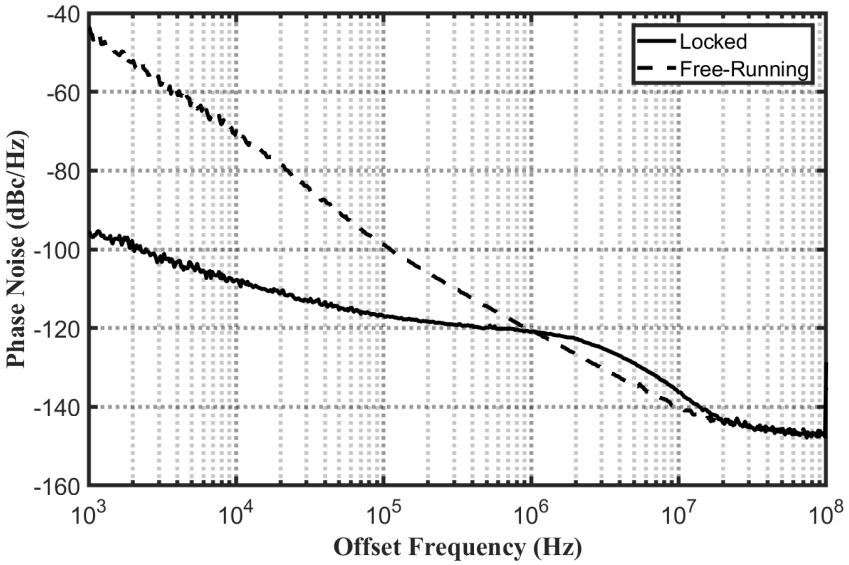


Figure 4.22: The measured output phase noise under locked and free-running conditions.

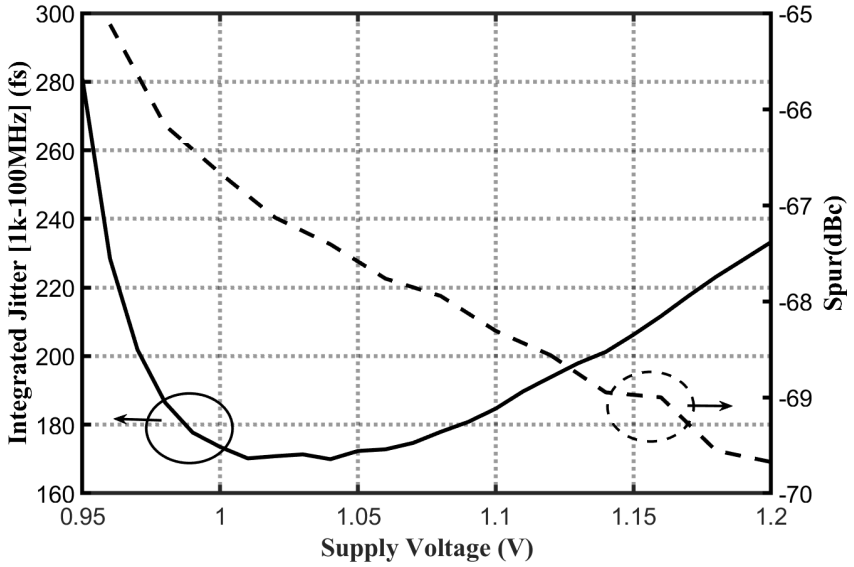


Figure 4.23: The measured reference spur and integrated jitter versus the supply voltage

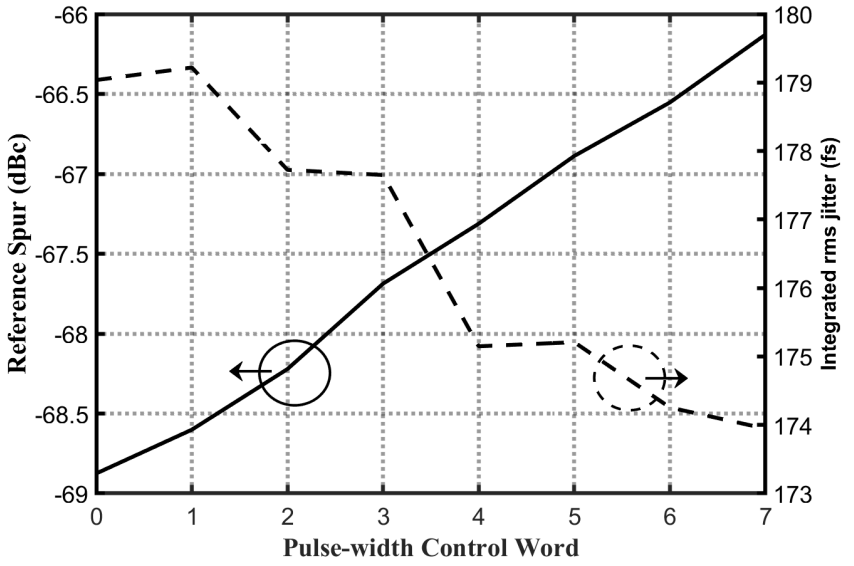


Figure 4.24: The measured reference spur and integrated jitter versus various reference pulsewidths

Chapter 5

Spur Reduction in Sub-Sampling PLLs using Cancellation Varactors

5.1 Introduction

The greatest source of spur in sub-sampling PLLs is the periodic change in the total capacitance of the L-C resonator of the VCO. There have been many publications on reducing the spur in sub-sampling PLLs [4–6, 55] and the general strategy was to improve the isolation between the sampling switch and the resonator.

It should be noted that the spur in sub-sampling PLL is different from the conventional charge-pump based PLLs. Charge-pump based PLLs suffer from spur due to charge-pump current mismatch, and therefore, the feedback path's contribution dominates in spur generation. On the other hand, a simulation of a sub-sampling PLL shows that the spur can be lower than -100 dBc when the VCO is isolated from the phase detector via an ideal voltage controlled voltage source.

This chapter describes a novel way to reduce the reference spur by partially cancelling the modulation of the capacitance due to the sampling mechanism in sub-sampling PLLs.

5.2 Proposed Technique

As mentioned in the previous chapter, the spur reduction of sub-sampling PLL is of interest to many, as the PLL is typically used in applications that require very low

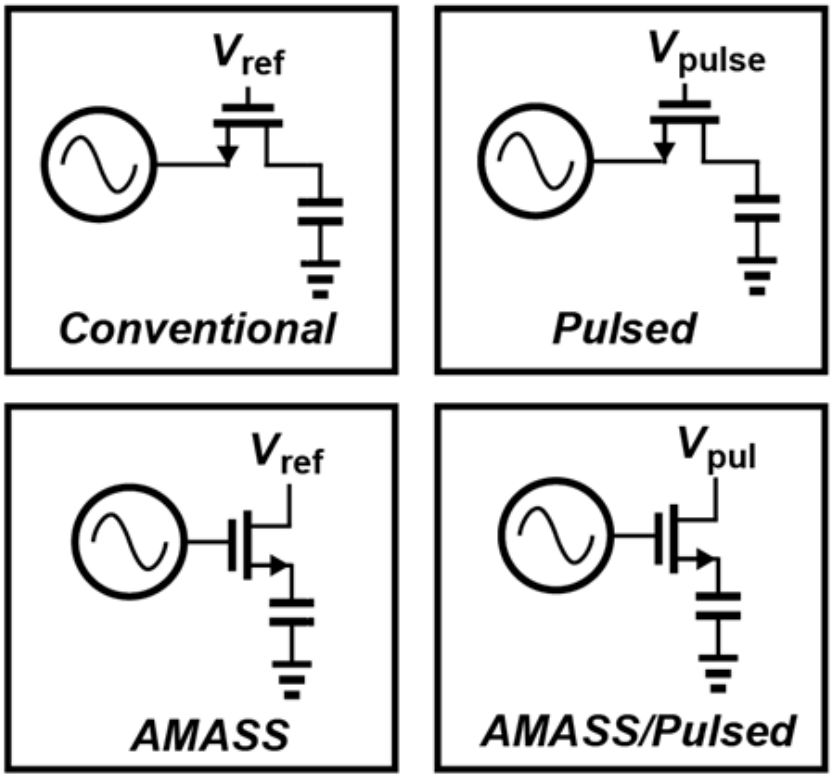


Figure 5.1: Illustration of sources of spur caused by the phase detector.

reference spurious tones. Sampling operation modulates the parasitic capacitance of the phase detector or buffer that is connected to the VCO, and because of the change in capacitance that occurs at every reference period, a large spurious tone is generated at the reference frequency. Figure 5.1 shows some of the prior techniques that were used to mitigate this modulation effect and reduce the spur.

The conventional sub-sampling phase detector caused a reference spur of -46 dBc, and the active-mixer based phase detector with a narrow reference pulse caused a reference spur of -67 dBc. The previous chapter showed how a narrow pulsed operation can further reduce spurious tone of sub-sampling PLL. A typical cellular communication requires a PLL to have a spur as low as -100 dBc. The spur can be significantly reduced with fractional-N operation, but even the fractional-N mode's spur is still correlated with the spur of integer-N mode. Therefore, to further reduce the spur down to as low as -80 dBc, many techniques have been examined. One of the techniques examined

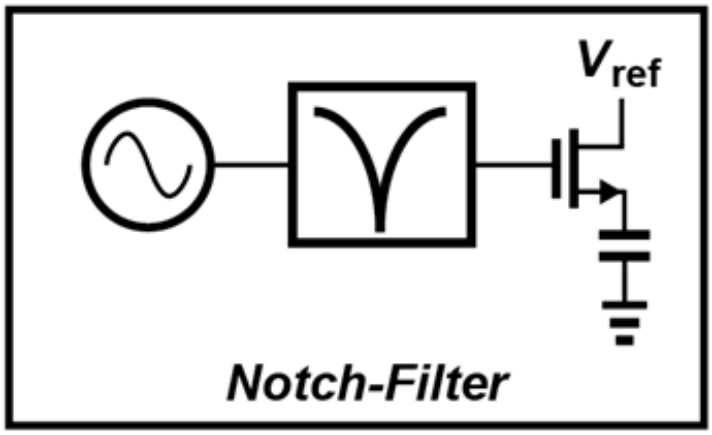


Figure 5.2: Illustration of notch filter for charge injection mitigation.

is using a notch-filter as shown in 5.2 in order to reduce the effect of charge-injection at the reference frequency. Since the notch filter would only filter the reference frequency, its effect on the signal at LO frequency is negligible. If charge-injection had any effect on the spur, it would improve the spurious tone. Therefore, the following values were used to implement a notch filter at 100 MHz: 2500 Ohms resistors and 325 fF capacitors. However, simulation shows that adding a notch filter has a negligible impact on the reference spur. Therefore, a conclusion can be drawn that the dominant source of reference spur in a sub-sampling PLL is the modulation of capacitance.

The next technique examined was adding a source-follower between the VCO and the sampling phase detector. Depending on the size of the source follower's transistor widths, the reference spurious tone could be lowered to as low as -94.72 dBc in simulation. However, reducing the size of the source follower also increases the output phase noise. Increasing the size of the source follower devices increases both power consumption and the reference spur. One way to decouple the trade-off between the power consumption and the size of the source follower device is to duty-cycle the source follower. Aggressively duty-cycling the source follower can lower the power consumption of the source follower to be negligible. However, this approach, in essence, is the same as the AMASS-PLL shown in the previous chapter.

Our implementation of the AMASS-PLL had a higher spurious tone than the

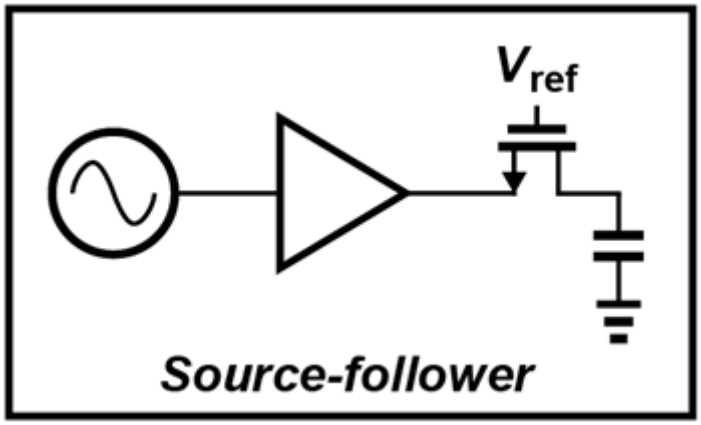


Figure 5.3: Illustration of source follower to improve the isolation between the phase detector and the VCO.

simulation above because the device size was at least 100 times bigger than the values used in the simulation above that yielded -94.72 dBc of spur. The large device size was to ensure that the active mixer's contribution to the phase noise is negligible. In order to decouple the trade-off between the mixer's device size and the spur, another technique, called varactor-cancellation, is proposed.

Shown in Figure 5.5 is the schematic of the proposed varactor-cancellation technique. One side of the phase detector and varactors are shown in the figure. The detailed operation of the pulse-based phase detector is described in the previous chapter. As the V_{pul} is switched on, the gate parasitic capacitance seen by the VCO is modulated. In order to mitigate the effect of this switching, varactors are added, and its one end is driven by the same signal V_{pul} so that the change in capacitance can be precisely cancelled in a synchronized manner. In some ways, this cancellation technique is similar to the dummy path technique from [5]. However, the dummy path technique require both the reference and its inverted signal, whereas this technique only requires a single phase clock and can therefore achieve lower reference spur than the dummy path technique. Figure 5.6 shows the simulation result of the reference spur as the number of fingers in the cancellation varactor is swept from 2 to 10. The reference spur is limited by tunability of the varactor.

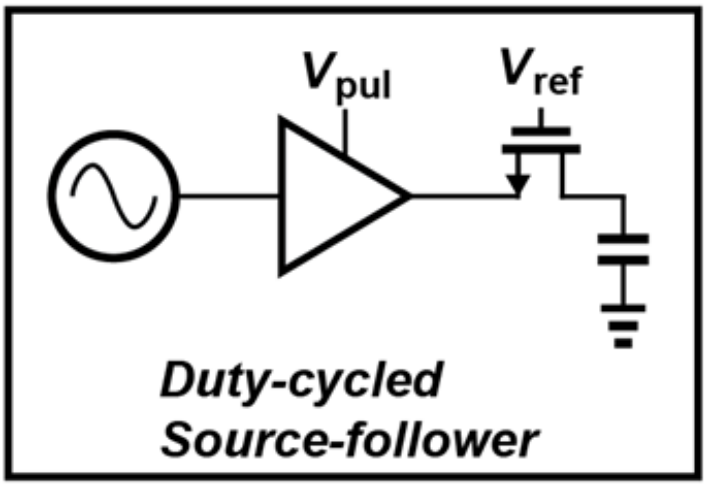


Figure 5.4: Illustration of duty-cycled source-follower to improve the power efficiency of source-follower based isolation.

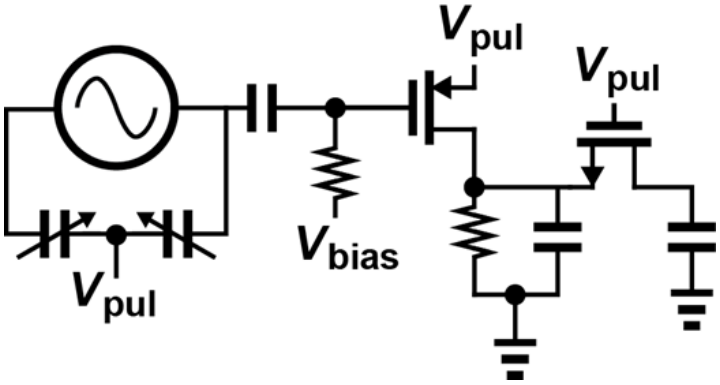


Figure 5.5: Proposed varactor cancellation.

5.3 Simulation Result

All simulations were done in transient analysis of Spectre. In order to mitigate the spectral leakage of discrete Fourier transform, Blackman window was used. Otherwise, the ”noise floor” of DFT will mask the reference spur tones. Figure 5.7 shows the simulated effect of the cancellation varactor. Due to the sampling operation, the frequency of the VCO output is periodically disturbed every reference period (10 microsecond). Once the varactors are added to negate this modulation, it can be seen that the instantaneous frequency fluctuates less than before.

The effect of cancellation varactors on the phase noise was also extensively sim-

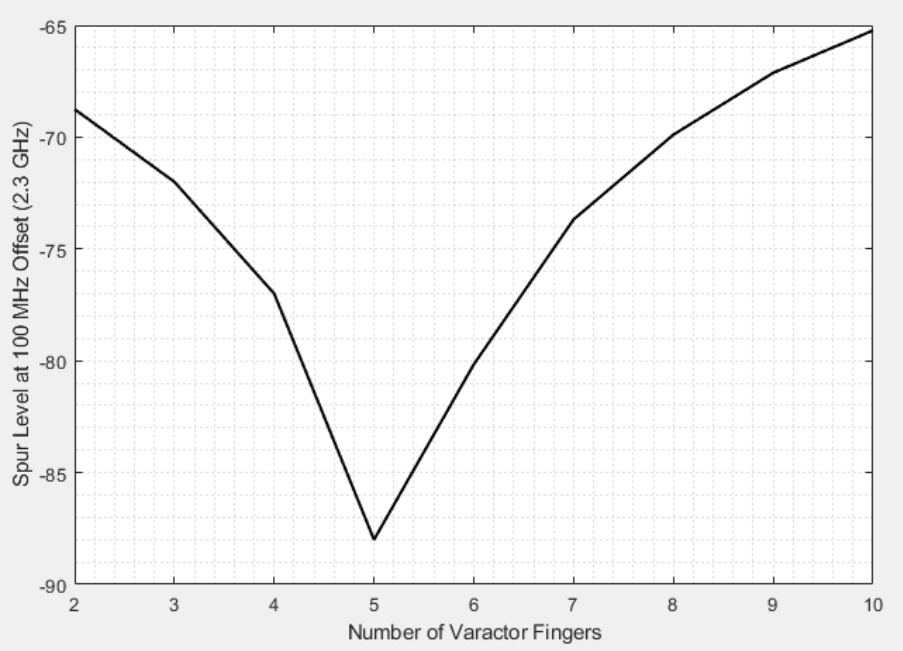


Figure 5.6: Spur (dBc) versus the number of fingers per each varactor.

ulated, and according to the PSS and PNoise simulations in Cadence Spectre, the varactors do not contribute significant amount of phase noise. The spurious tone at the reference frequency offset is about -86 dBc in simulation. Furthermore, the loop bandwidth and phase margin are unaffected as well according to the simulation.

5.4 Design Detail

Figure 5.8 shows the top level layout view of the chip. The chip was taped out in 65-nm CMOS process with 0.8 V supply for every block. At the time of writing this chapter, the design of the chip was submitted for fabrication.

Compared to the previous design of AMASS-PLL, the VCO and the capacitor banks were completely redesigned. This was to save the core area and make it easier to route important signals. A 6-bit MOM cap bank replaced the original 6-bit MIM cap bank for fine-tuning. The resolution of the capacitor bank is 1.8 fF or 750 kHz. The tuning range is 118.45 fF or 50 MHz. The minimum Q-factor of the bank is 166.5.

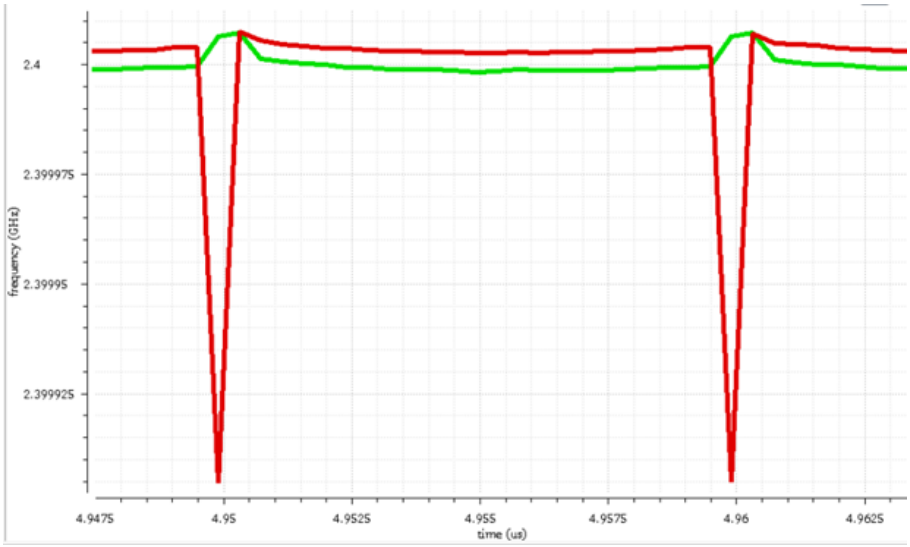


Figure 5.7: VCO Instantaneous Frequency versus Time. Red curve is without the cancellation varactor and green curve is with the cancellation varactor.

Figure 5.9 shows the layout view of the capacitor bank. A 3-bit MIM-cap bank is used for coarse tuning. The tuning range of the coarse bank is 207 MHz or 230.15 fF. The minimum frequency step is 25 MHz which is equivalent to 28.72 fF. The minimum Q-factor of the coarse bank is 210.9. The PLL's architecture is identical to the AMASS-PLL except for the cancellation varactors. The schematic diagram of the PLL is repeated here as Fig. 5.10 for convenience.

The PLL is simulated with an accuracy of 1e-6 reltol in Spectre. PSS and Pnoise analyses were used for phase noise simulation and transient was used for simulating the spur. Figure 5.11 shows the simulated phase noise plot. The total integrated rms jitter is equal to 134 fs. Figure 5.12 shows the simulated reference spur, and is about -81.38 dBc @ 100 MHz offset, which is about 14 dB better than the previous architecture according to the simulation. The total power consumption is expected to be slightly less than 1 mW at 0.8V supply voltage.

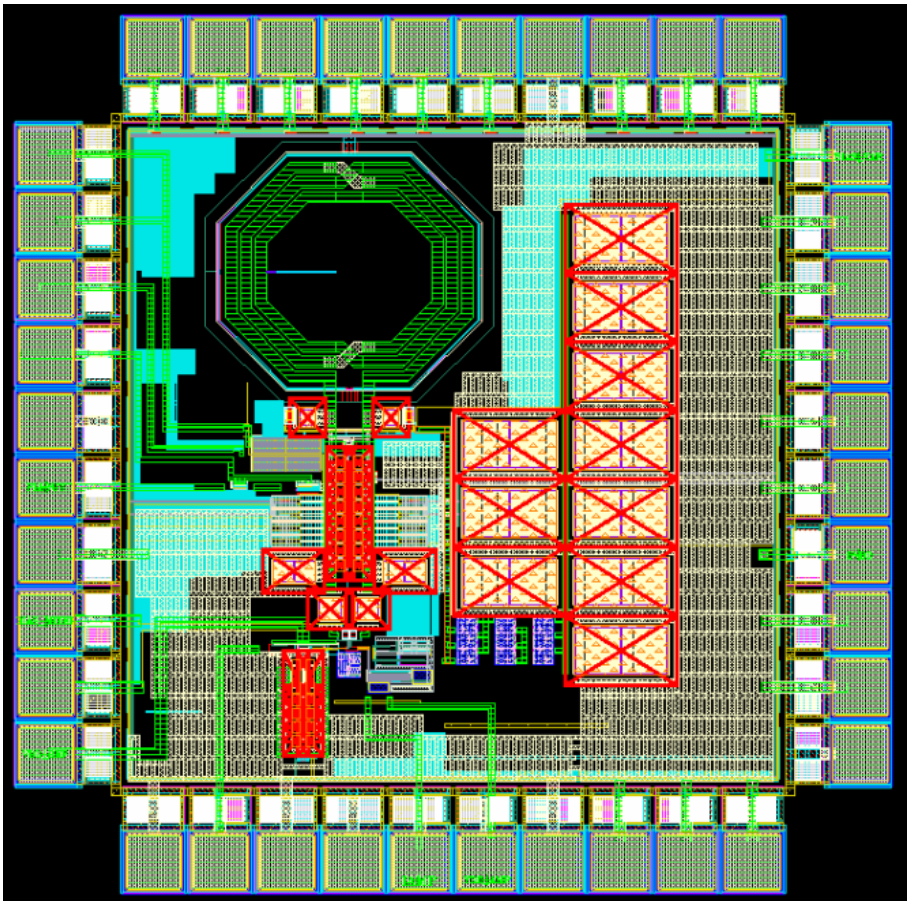


Figure 5.8: Top level Layout View.

5.5 Conclusion

A novel way to reduce the reference spur of a sub-sampling PLL using a varactor is presented in this chapter. The result of prototype simulation is shown to demonstrate the effectiveness of the said design. The technique is better than the prior art as it requires only a single clock and is area-efficient. Furthermore, the technique decouples the trade-off between noise generated by the phase detector and spur caused by the phase detection operation in a SSPLL. The prototype design achieves -81 dBc spur and 134 fs rms jitter at 1 mW power consumption in 65 nm process while operating from 0.8V supply. The silicon implementation will be measured in the future.

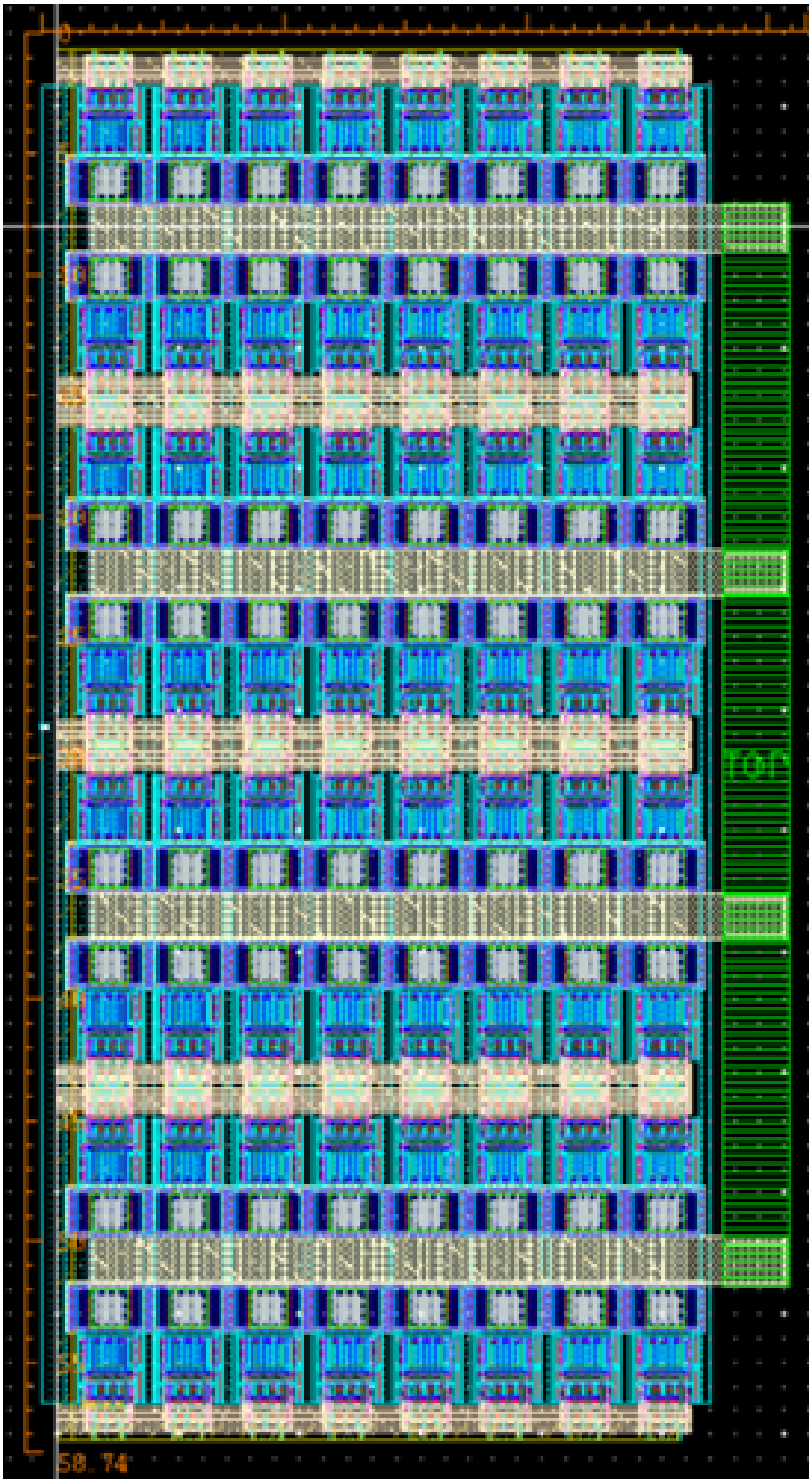


Figure 5.9: Top level capacitor bank layout.

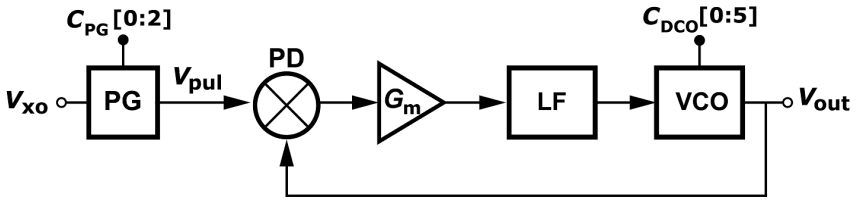


Figure 5.10: A Schematic of the AMASS-PLL

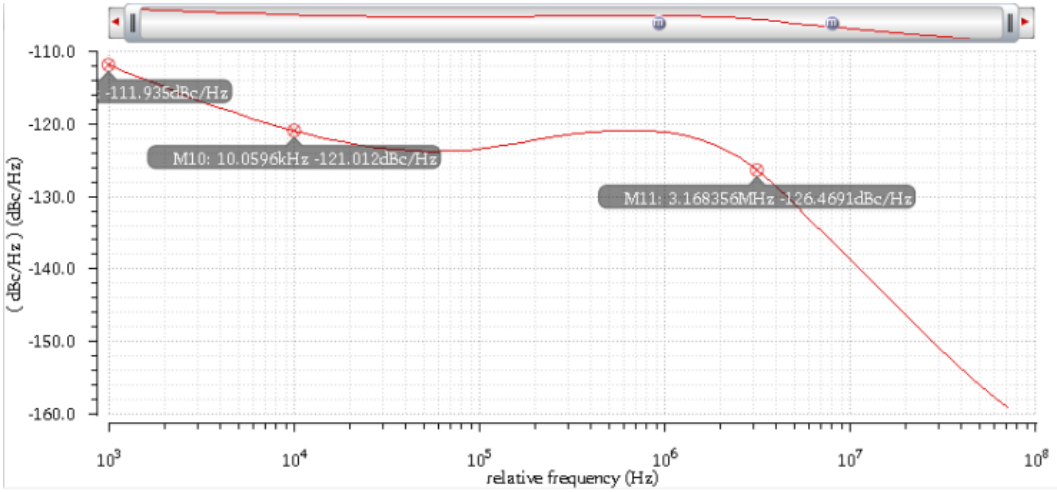


Figure 5.11: The simulated output phase noise is shown.

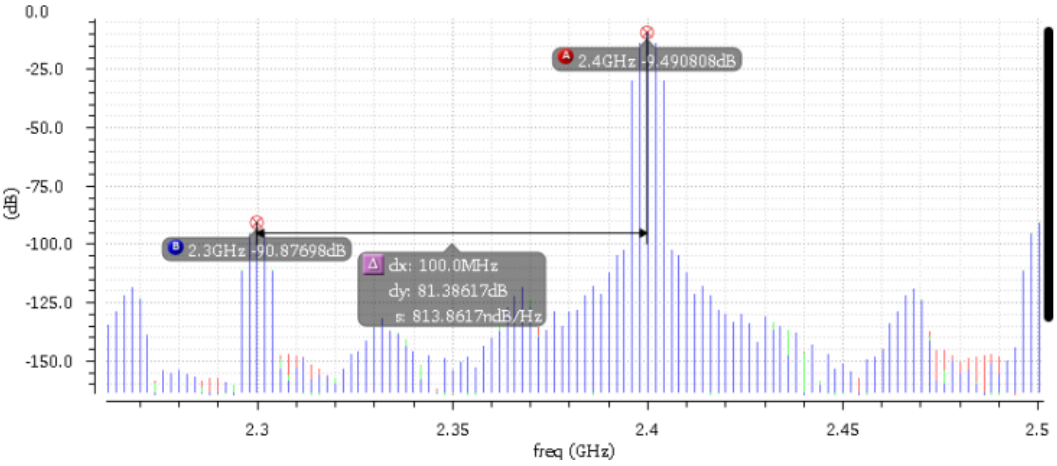


Figure 5.12: DFT of the PLL output shows the simulated spur less than -80 dBc.

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