High-Power Transistor-Based Tunable and Switchable Metasurface Absorber

Aobo Li, *Student Member, IEEE*, Sanghoon Kim, *Student Member, IEEE*, Yong Luo, Yunbo Li, Jiang Long, *Member, IEEE*, and Daniel F. Sievenpiper, *Fellow, IEEE*

***Abstract*— High-power signals traveling along the surface of the shielding of transmitter systems may leak into the system through openings between connecting parts and cause damage to vulnerable electronic devices. This problem could be alleviated by implementing lossy coatings or recently developed passive power-dependent nonlinear surfaces. However, these solutions will either suppress the performance of the electromagnetic devices being shielded or be highly power-dependent. Applying transistors creates an active nonlinear metasurface that can allow the absorption of the surface to be directly controlled by the system, or tuned in response to the local power level using feedback control. This can provide a sharp absorption response with a wide range of controllable power threshold. Different absorption rates at the same power level can also be achieved by applying different biasing to the transistors. In this paper, the first transistor-based, thin, switchable, and tunable high-power surface wave absorber is proposed with full wave and circuit cosimulation analysis as well as waveguide and anechoic chamber measurement.**

***Index Terms*— High-impedance surfaces, high power, microwave absorber, surface wave, transistor.**

I. Introduction

MICROWAVE absorbers are widely studied because of their absorbing abilities that can suppress transmission and reduce reflection or scattering for radar absorber applications [1]–[4]. Another important role that microwave absorbers are playing is to absorb energy of incoming signals to protect sensitive electronic devices from being disrupted or even damaged when input power is high enough, and couples into the system through apertures on the metallic body that support the system.

One approach to mitigating high-power microwaves is to deploy conventional absorbers on the surface of the object to alleviate scattering or energy transmission. However, this coating material is usually expensive, thick, and bulky, and it may have negative effects on the performance of the front end of shielded communication system, like transmit or receive antennas.

Manuscript received November 21, 2016; revised February 7, 2017; accepted February 25, 2017. Date of publication March 28, 2017; date of current version August 4, 2017. This work was supported by the Office of Naval Research under Grant N00014-15-1-2062.

A. Li, S. Kim, Y. Luo, Y. Li, and D. F. Sievenpiper are with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093-0407 USA (e-mail: aol006@eng.ucsd.edu; dsievenpiper@eng.ucsd.edu).

J. Long was with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093-0407 USA. He is now with Skyworks Solutions Inc., San Jose, CA 95134 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2017.2681650

Frequency selective surfaces (FSSs) and metasurfaces working as microwave absorbers have been proposed and applied in many studies [5]–[12], because these subwavelength periodic metallic units have advantages of low loss, low cost, low profile, and unique high performance in various applications, such as conformal antennas [13], wavefront engineering [14], and advanced imaging systems [15]. For metamaterial perfect absorber, related works have been done in both RF and optical frequencies in applications of cloaking as well as energy absorption. The conventional metasurface absorbers are generally passive and have the same response regardless of the incident power and waveform, and thus may be limited in applications when devices to be shielded are working at the same absorbing frequency bands. Therefore, tunable absorbers [16]–[18] are studied and further research has been carried out by loading the metasurface with lumped elements and diodes to introduce nonlinearity [19]–[28]. This nonlinearity could either be power-dependent or waveform-dependent or both, enabling the surface to respond differently to various incoming signals. The active frequency selective absorbers could be tuned to absorb at different frequencies by tuning the biasing of the p-i-n diode to achieve a wideband absorber in the normal direction. However, a large area of active absorber that may require thousands of p-i-n diodes would draw a large amount of current, which may make it impractical. On the other hand, as diodes only turn ON when the voltages across them are greater than the turn-ON thresholds (typically 0.4 V for schottky diodes and 0.7 V for p-i-n diode), conventional diode-based nonlinear absorbers are limited to specific power ranges.

In this paper, we propose the first transistor-based tunable and switchable surface wave absorbing metasurface. It provides surface wave suppression to protect electronic devices from leakage of high-power signals or surface currents through discontinuities in the enclosing structure, as indicated in Fig. 1. Compared with the diode-based absorber, the use of field-effect transistors (FETs) gives an additional degree of freedom, because absorption is controlled through the gate voltage, rather than the diode turn-ON voltage, making this surface switchable and tunable at both low and high microwave power levels. In other words, this transistor-based absorbing surface could be turned ON or OFF at both high power for protection purposes and at low power for scattering or communication purposes. Furthermore, the absorption rate can be easily tuned by adjusting the bias voltage of the transistors, which will be introduced in this paper. Comparing with adopting diodes for switching purpose, FETs can be maintained in

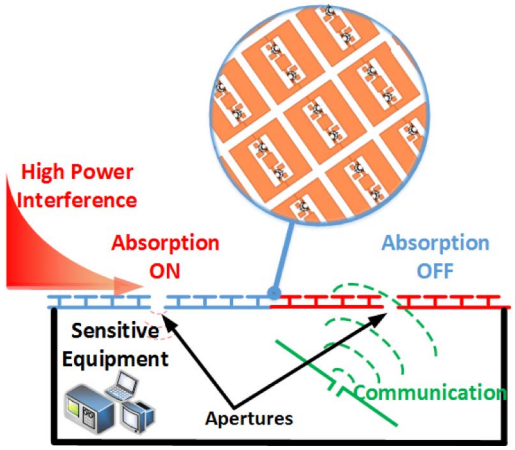


Fig. 1. Conductive body covered with transistor-based absorbing surface, which can protect sensitive equipment from being damaged by high-power interference by turning ON the absorber through transistors, meanwhile, it can sustain communication when the absorbing surface is turned OFF.

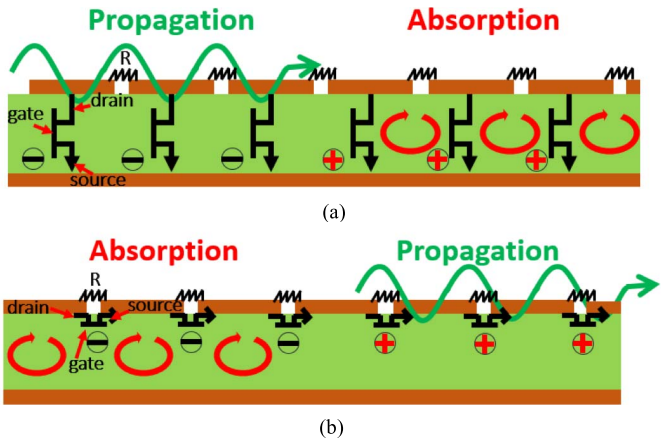


Fig. 2. Transistor-loaded metasurface in the ON- and OFF-states for surface wave absorption. (a) Transistors loaded at the via. (b) Transistors loaded at the gap.

a particular tuning state with no static power draw, since they are voltage controlled. On the other hand, FET's drain–source channel is symmetric, which allow signals conducting in both ways, the active absorbers we are proposing could be tuned without damaging its linearity. We first demonstrate the absorbing response of the transistor loaded metasurface with electromagnetic and circuit cosimulation, and then show the switching and tuning capability of the surface in a waveguide measurement. In order to further verify the surface current suppression performance, we demonstrate a large array of this surface with a slit in the middle representing the discontinuity of the surface. A large difference in attenuation between ON and OFF state leakage through the slit is observed in the chamber measurement, which matches well with the difference of the magnitude of the radiation pattern in the ON- and OFF-states. Compared with conventional nonlinear absorbers, this transistor-based absorbing surface has a sharper response to the amplitude of the input power level. Finally, we demonstrate that we can provide feedback using a power sensor and LabVIEW-based control system to provide an even sharper response, turning ON the absorption at any prescribed leakage power level.

This paper is organized as follows. Section I gives background and an introduction of the application of the metasurface and its unique performance in absorbers when loaded with nonlinear devices, such as transistors. Section II presents the principle and analysis of the high-impedance surface (HIS) loaded with transistors which can switch or tune the absorbing surface. Section III shows the cosimulation and waveguide measurement results of the 6×9 array at different power levels. Section IV describes a large transistor loaded surface wave absorber with a slit in the middle, showing the tuning and switching performance with sharp absorption response. Part V gives a final conclusion.

II. Analysis of the Nonlinear Absorber

The mechanism of this absorbing surface is based on the surface wave suppression property of the HIS. It is composed of periodic subwavelength metallic patches with centered vias connecting the patches to the bottom ground plane. It has a bandgap between the transverse magnetic (TM) and transverse electric (TE) surface wave modes, and it does not support surface waves within the forbidden gap [29]. Near the band edge, incoming fields are enhanced by the resonance of the surface [30], and if losses are included the wave can be highly attenuated. If such a material is deployed on the outer enclosure of an object to be protected, it can effectively suppress surface currents, and thereby minimize leakage through apertures, openings, or discontinuities in the enclosure.

The surface can be modeled as a parallel *RLC* circuit where the resonance frequency is $\omega_0 = (1/(LC)^{1/2})$, in which L is the equivalent inductance determined by the thickness of the surface, and C is the equivalent capacitance of the gap between neighboring patches. The quality factor (Q) of this HIS resonator is related to the gap resistance. A parallel *RLC* circuit's Q is represented as $=(R/\omega_0 L)$, in which R is the resistance at the gap, and $L = \mu h$, where μ is the permeability of the substrate and h is its thickness. When the surface is illuminated with microwaves, the concentration of charge across the gap also leads to current through the resistance, causing absorption. Furthermore, this R can be tuned to adjust the absorption rate and bandwidth, as it affects the quality factor of the resonators that make up the surface.

In order to make this absorbing metasurface tunable and switchable, we introduce active components in the form of transistors at the vias of the metallic patches. This will allow the topology of the surface to be manually transformed, thus having different absorption response to incoming waves shown in Fig. 2(a). We connect the center of the via to the drain of the FET transistor and connect the source of the transistor to the ground plane. The drain to source channel can be turned ON and OFF by applying different dc biases (positive or negative bias, respectively, depending on the threshold voltage of the transistor). For an ideal transistor, the drain to source resistance is zero in the ON-state (positive gate biasing), which connects the via to the ground, creating a high-impedance surface and allowing high absorption of surface waves. On the contrary, in the OFF-state (negative gate biasing), the drain to source channel resistance for an ideal transistor is infinite, and it

appears as an open circuit, which disconnects the via from the ground. This transforms the surface from an HIS into simple array of periodic patches backed with a conducting ground plane, and eliminating the resonance as seen by surface waves. In this state, the structure is essentially a conductor-backed frequency selective surface [31], which has a much higher resonance frequency, and thus lower loss within the band of interest. Hence, it will support surface wave propagation with very low absorption. In addition, when the gates of the transistors are biased with a voltage level between ON- and OFF-states, the drain to source channel will show different equivalent resistances, which changes the quality factor of the surface and adjusts its absorption. In this case, a tunable absorption rate will be observed with different gate biasing voltages.

Besides the topology mentioned above, another transistor-based switchable and tunable surface is represented in Fig. 2(b). Instead of at the vias, transistors are placed at the gaps between the plates, in parallel with the gap resistance. In this structure, the drain to source channel can also be controlled by the bias voltage at the gate. For the transistor's OFF-state (negative gate biasing), the drain to source channels are turned OFF and the surface is highly absorbing. For the transistor's ON-state (positive gate biasing), the drain to source channels are shorting the resistors at the gaps and connecting all the top patches together, which makes surface look highly conductive, and thus reducing absorption. Similar tunable states are expected to be seen as with the former topology. Section III will discuss about the simulation and measurement of these two structures.

III. Cosimulation and Measurement

Two topologies (A and B) of the transistor loaded HISs are designed and cosimulated with HFSS and Ansoft Designer. The elements of topology A and B are implemented, as shown in Fig. 3(a) and (b), respectively. For topology A, to avoid positioning the transistors inside the substrate, we designed a pair of transistors on the surface to connect their drains to the outer ring of each patch and their source to the inner pad which is attached to the via. The gates of the transistors are connected through additional vias from top to the biasing network layer, which provides bias voltage to the gates of all the transistors simultaneously in order to control the whole surface's electromagnetic properties. The 2-kΩ resistors are placed at the gap between neighboring elements, aligned with the E-field direction at the gap, which is perpendicular to the edge of the units along the surface (k-direction in Fig. 4). For topology B, a pair of transistors are placed at the gap in parallel with the resistor, their drains and sources are connected to the neighboring elements. The gates are connected through vias from top to the biasing network layer. The centers of the elements of both A and B are shorted to the ground layer with a through hole plated via with radius 0.5 mm. Rogers RT5880 [32] with thickness of 3.125 mm is used as the substrate for both topologies. For the biasing circuit's layer, we used 0.127-mm-thick FR4 as a substrate. The side view of the stack is shown in Fig. 3(c), which applies to both A and B topologies.

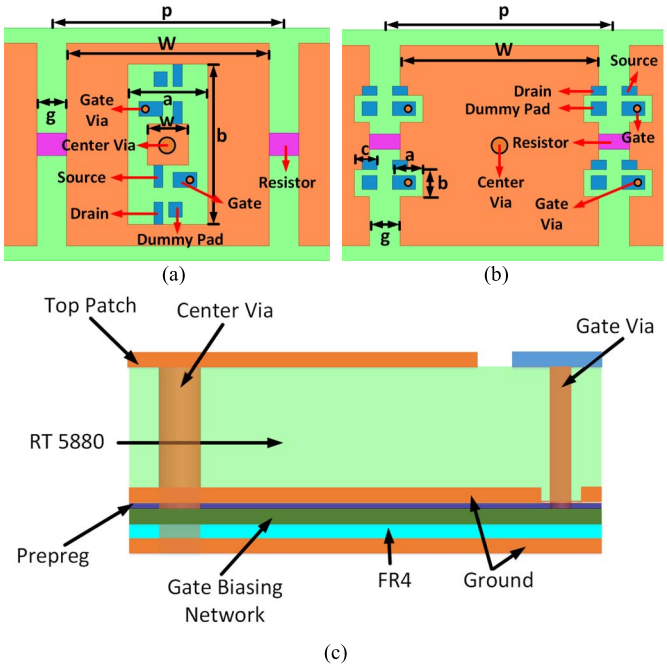


Fig. 3. Element top view of the two topologies in which orange color metal represents the surface patch, while blue metals are pad for transistors (NE3503M04 is used here) and purple rectangular represents the position of the 2-kΩ gap resistors. (a) Topology A with a pair of transistors at the center vias, in which $p = 15.6$, $W = 13.6$, $g = 2$, $a = 5.38$, $b = 10.76$, and $w = 2.76$ (all in mm). Note p is the period of the unit cell. (b) Topology B with a pair of transistors at the gap in which $p = 17.5$, $W = 15.5$, $g = 2$, $a = 2$, $b = 1.75$, and $c = 1.5$ (all in mm). Note p is the period of the unit cell. (c) Side stack view of the structure for both topologies A and B.

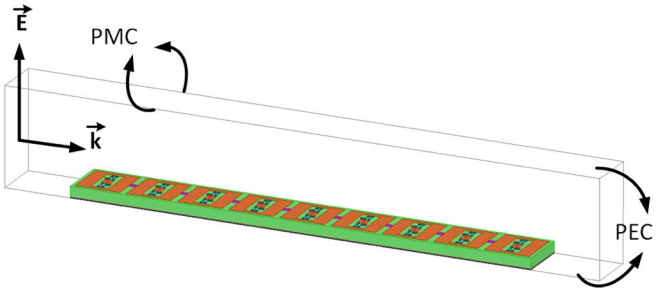


Fig. 4. HFSS simulation model of nine unit cells with top and bottom PEC walls and two side PMC walls as a 2-D array when TM wave excited.

A. EM/Circuit Cosimulation

In order to evaluate the absorption performance of the proposed two topologies, we here implemented HFSS's full wave simulation [19] of an array of nine elements with periodic boundaries for two side walls excited by two wave ports at the left-hand and right-hand sides, and PEC boundary for top and bottom walls when TM excited, shown in Fig. 4. As the target center absorbing frequency is 2.2 GHz which lies in the frequency range of waveguide WR-430, the same height (54.61 mm) of the air box is chosen to be aligned with real waveguide measurements. For TM excitation, the top and bottom of the air box are assigned to be PEC boundary and the two side walls are assigned to be PMC (periodic boundary for TM excitation) thus representing the structure located in an ideal TEM waveguide. Lumped ports are assigned for gap

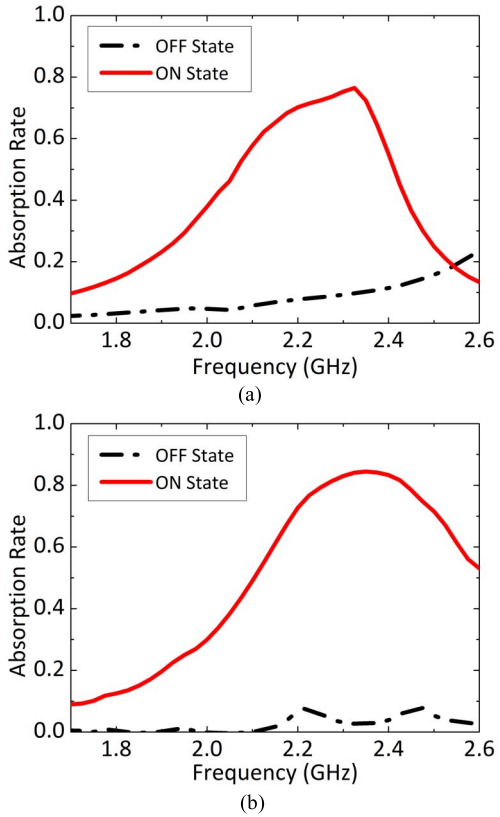


Fig. 5. Co-simulation results of the switchable absorption results of the nonlinear absorbers. (a) Topology A (−3 V for OFF-state, 1 V for ON-state). (b) Topology B (−3 V for ON-state, 1 V for OFF-state).

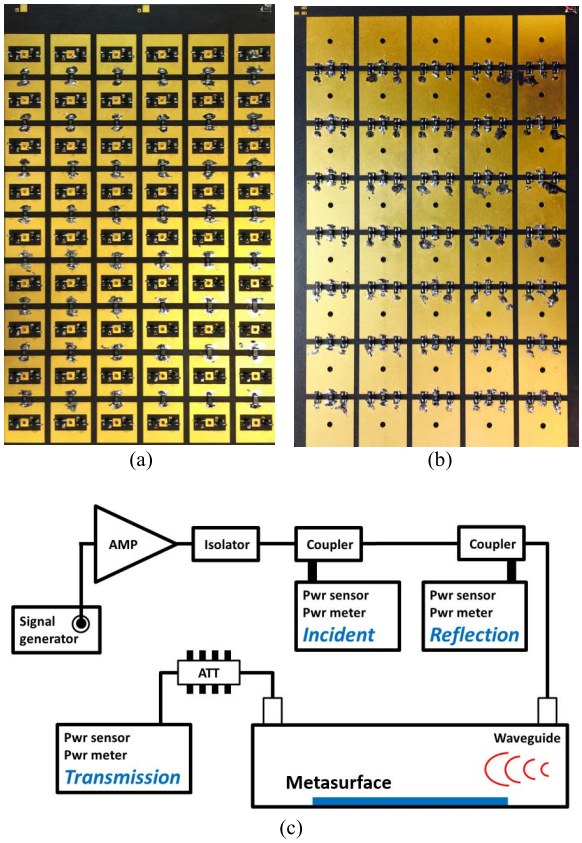


Fig. 6. Small absorbing array fabrication for waveguide measurements. (a) Fabrication of topology A. (b) Fabrication of topology B. (c) Waveguide time-domain measurement setup.

resistors and transistors drain and source channels at their intended locations.

Full wave simulation provides the S-parameter matrix of the passive part of the absorber, from which when imported to circuit simulators (ADS or Ansoft Designer), then connected with transistors and resistors to the corresponding lumped ports [20]. Two wave ports are connected to microwave excitation and receiving port, respectively, with impedance set to be characteristic impedance of the wave port of the model. Absorption performance of the surface can be studied in time domain circuit simulations. We include a full SPICE model of the transistor (NE3503M04), including parasitics and the resistors in the transient simulation. We can easily derive the absorption rate of this surface wave absorber by

$$\mathrm{Abs}(f) = 1 - T(f) - R(f) \tag{1}$$

in which Abs is the absorption rate, T and R are the frequency-dependent transmitted power and reflected power, respectively. In circuit simulations, we bias the gate of the transistors in circuit simulators to turn the transistors ON and OFF by providing positive (0∼1 V) and negative (−3 V) biases, respectively. The switchable absorber's simulated results are shown in Fig. 5(a) and (b). For both topologies, we could see over 80% peak absorption in the ON-state and less than 10% absorption rate in the OFF-state, showing good switching ability.

B. Waveguide Measurement

With the optimized structure, we fabricated a small array indicated in Fig. 6(a) and (b) for both topology A (6 by 9 unit cells) and B (5 by 8 unit cells) with dimensions the same as indicated in Fig. 3(a) and (b), respectively, and measured in the standard WR-430 TE waveguide. Note that TEM waveguide is used in simulation only for simplification of simulations. Power amplifiers (Ophir 5022 and 5193) are used to provide different levels of input power. Several power meters (Agilent N1911A) are used to detect the incident, reflected and transmitted power at the waveguide in real-time, with the measurement controlled by LabVIEW [33]. The measurement setup is shown in Fig. 6(c).

The measured absorption rate curves for the two topologies under different input power levels are plotted in Fig. 7(a) and (b). At low power level (less than 10 mW), we could observe a large absorption difference between ON- and OFF-states of both topologies. Note that at the measured abosrption rate curves of input power less than 10 mW share the same one as 10-mW case. At the frequencies of interest, near 2.2 GHz, the surface has more than 80% absorption rate in the ON-state and lower than 20% absorption rate in the OFF-state. We could observe that for ON-states, the absorption rate begins to drop as power is increased. This is because with higher input power, the drain to source channel current begins to saturate, causing the absorption rate to drop. However, we could still see more than 50% absorption for

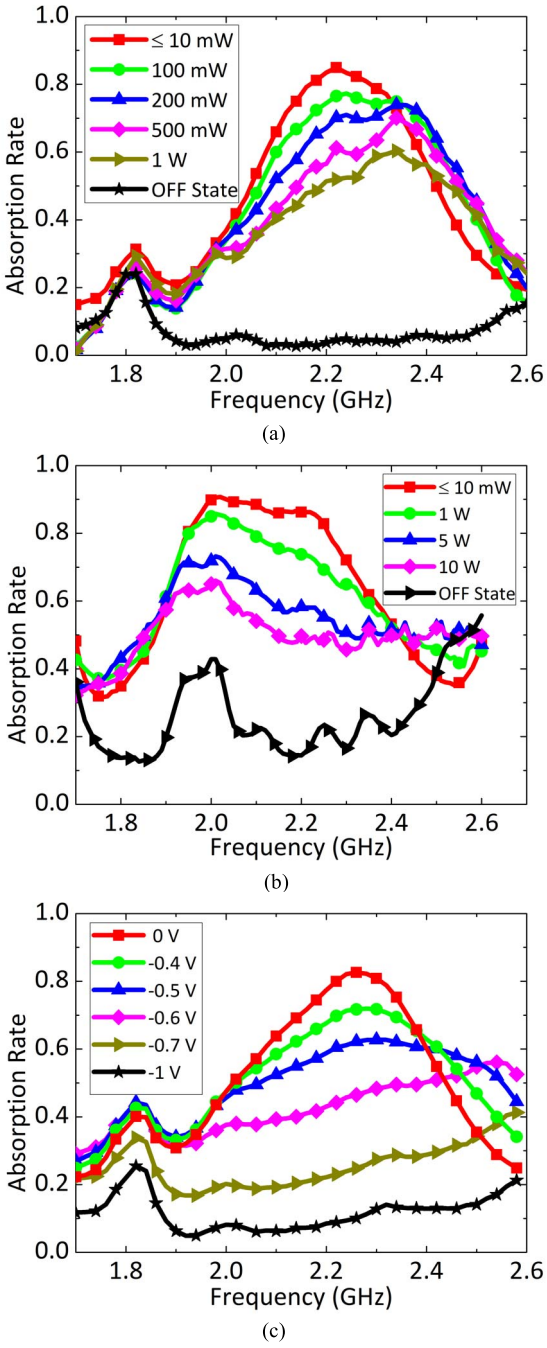


Fig. 7. Waveguide measurement results. (a) Absorption rate at ON- and OFF-states of topology A with different levels of input power. (b) Absorption rate at ON- and OFF-states of topology B with different levels of input power. (c) Measured tunable absorption rate of topology A with different gate biasings.

topology A at 2.2 GHz and a peak abosrption rate over 60% at 2.35 GHz with 1-W input power, which equals 168 W/m^2. This power density is calculated from input power (1 W) divided by the area of the waveguide (0.006 m^2 for WR-430). The measured OFF-states of different input powers share the same curve (black curve in Fig. 7), since the transistor's drain–source channel is OFF all the time with the tested input power range. For Topology B, at 5 W (838 W/m^2) input power, we could still see more than 60% absorption at the frequency of interest between 2 and 2.2 GHz. The power

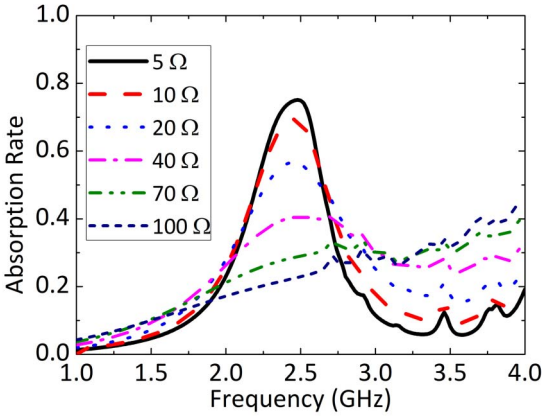


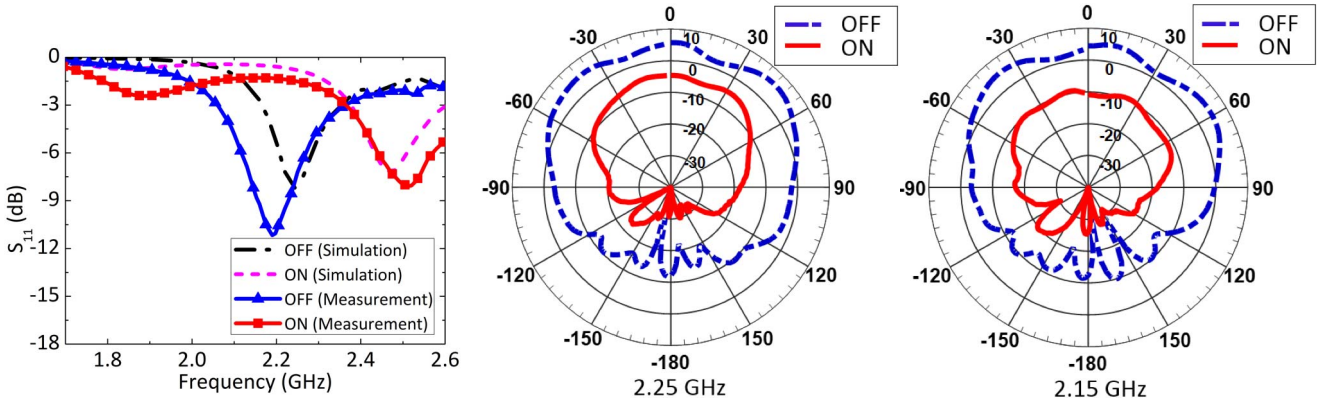
Fig. 8. Absorption rate versus different via resistances.

handling ablity is higher, because this topology's absorbing state is in transistor's OFF-state, where current saturation is not a critical issue. For topology A, to achieve higher power performance, we could change the current transistors with ones having higher saturation drain current. This limitation will be discussed further in Section III-C.

Besides the switching ability of the absorber, the absorption rate can also be tuned to middle states between ON and OFF by applying different bias voltages ($-1\sim0$ V) to the gates. With different bias voltages, the drain to source equivalent impedance is changed accordingly (higher bias voltages gives a lower channel impedance), further affecting the resonance of the surface and changing the absorption rate. This tunable absorption of topology A is measured and shown in Fig. 7(c). Note that for bias voltage greater than 0 V (drain–source channel fully ON) and less than -1 V (drain–source channel fully OFF), the measured absorption rate curves are identical to 0 V bias one and -1 V bias one, respectively.

C. Measurement Result Discussion

For topology A's waveguide measurement, we could see a small peak at 1.8 GHz at both OFF- and ON-states as well as those intermediate states. That is caused by the gate vias of the transistors, which introduces another additional resonance. This could be removed or addressed by adjusting the positions of the vias. Additionally, for the waveguide measurement, as input power increases, there is a drop of absorption rate in the ON-state, seen in Fig. 7(a). The reason for this is because when transistors' gates are positively biased, the drain to source channel is turned ON but this channel's current will saturate at some input power. In other words, at comparatively low power, the transistors are working in the linear region, which yields a small channel resistance, but at high power, they are working in the saturation region, which increases the channel resistance significantly and reduces the quality factor of the surface. We further verified this through simulations by assigning *RLC* boundaries connecting topology A's outer rings to the vias. When the resistance increases, a drop of absorption could be observed as expected, indicated in Fig. 8. This problem could be solved by applying higher power transistors at the via to enable higher power applications. Note that for topology A when using NE3503M04 as the switching transistor, with 1-W (168 W/m^2) input power to



(a) (b) (c)

Fig. 9. (a) Measured versus simulated S_{11} of the slit at both ON- and OFF-states. (b) Radiation pattern (E-plane) at ON- and OFF-states of 2.15 GHz. (c) Radiation pattern (E-plane) at ON- and OFF-states of ¡2.25 GHz.

the WR-430, we could still achieve more than 60% peak absorption at 2.35 GHz and over 50% of absorption at 2.2 GHz.

Topology B is another way to solve the saturation problem, since the absorber is in the ON-state when the transistors are negatively biased. This topology may instead be limited by the breakdown voltage between drain and source, but this would occur at even higher power levels. This could be easily seen from Fig. 7(b), that when input power is 5 W (838 W/m^2), more than 70% peak absorption at 2 GHz and 60% of absorption at 2.2 GHz could still be achieved. However, from topology B's measurement, we observed that compared with the simulated results, the OFF-state's absorption rate is higher than expected. This is because in the OFF-state, when the transistors are positively biased, they are not ideally shorted, instead they will show some drain to source resistance and capacitance. Unlike placing the transistors at the vias, this parasitic capacitance and channel resistance influence the surface more, since the field is mostly concentrated at the gap between neighboring elements where the transistors are placed. This issue could be addressed by implementing smaller transistors at the gap with smaller parasitics.

IV. Large Panel With Slit

A large panel of the absorber of topology A is fabricated in order to test the surface current suppression and absorbing abilities in a realistic scenario in our far-field chamber. The fabricated array consists of 400 unit cells (25 by 16 cells, with length 395 mm and width 254 mm) and a slit in the middle of the board with width 2.54 mm and length 56 mm. The purpose of that slit is to allow for leakage of microwave power and thus to test the absorber's tunable and switchable properties and its ability to suppress leakage. The slit is designed to work as a slot antenna at 2.2 GHz with the absorbing surface, which allows energy to couple through the slit in the OFF-state. We expect to see large attenuation of the leakage power in the absorber's ON-state.

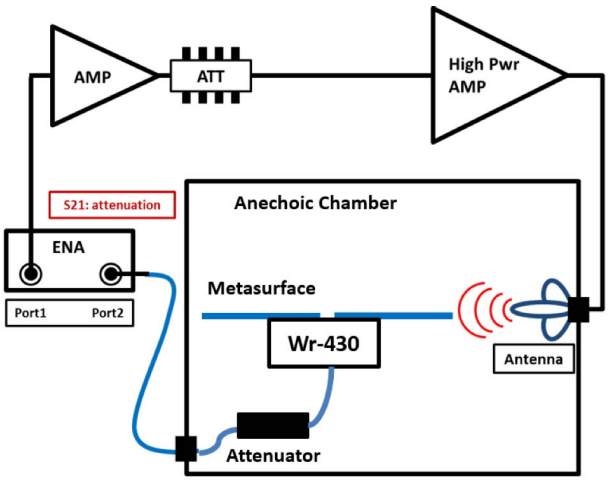
A. Radiation Pattern

We first measured the return loss (S_{11}) of the slit in the absorber's OFF- and ON-states (transistor gates biased negative and positive, respectively) by attaching the standard waveguide WR-430 to the bottom ground plane covering the slit. The slit was basically operating as a slot antenna, but surrounded with the switchable metasurface. The measured return loss results compared with simulated results for a slightly smaller twelve by twelve cell panel is presented in Fig. 9(a). The difference between the measured return loss and the simulated one is mainly due to that the fabricated panel is larger than the simulated one, which is smaller in size to save simulation time. Measured return loss lower than -10 dB is observed at 2.2 GHz in the OFF-state, while in the ON-state -1.3 dB is measured. Because slot antennas radiate through currents on the surrounding ground plane, suppressing those surface currents effectively suppresses radiation, resulting in higher return loss. We further verified this surface current suppression by measuring the radiation pattern in anechoic chamber at the two different states (OFF- and ON-states).

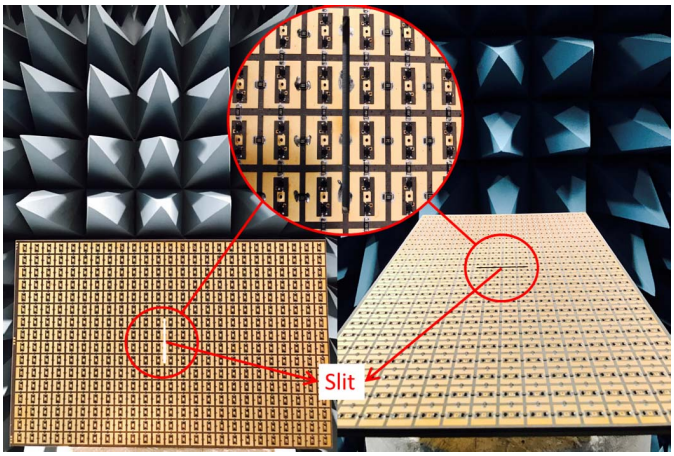
We used a horn antenna (ETS-Lindgren 3164-08) as transmitting antenna. The distance between the transmitting antenna to the absorbing surface is fixed at 2.5 m, which is enough to satisfy the far-field distance. The radiation patterns of the E-plane of the surface at 2.15 and 2.25 GHz are measured and plotted in Fig. 9(b) and (c). An 18 dB difference between OFF- and ON-states in the azimuth plane is observed, showing good surface current absorbing ability.

B. Switchable and Tunable Absorption Measurement

In a more intuitive way, the leakage power through the slit compared with the incident power level was measured in the anechoic chamber. The setup for this measurement is presented in Fig. 10(a). Port 1 of the VNA (Agilent E5071C) provides small transmitting signals, which are amplified by a high-power amplifier, then further transmitted through the horn antenna with proper polarization, directed toward the center of the panel under test. The standard waveguide WR-430 is attached to the bottom of the slit and the received signal returns to the VNA's port 2. The whole setup including VNA was well calibrated with free space path loss, all insertion loss of cables and connectors, and so on. Both normal incidence and grazing incidence are measured with corresponding positions

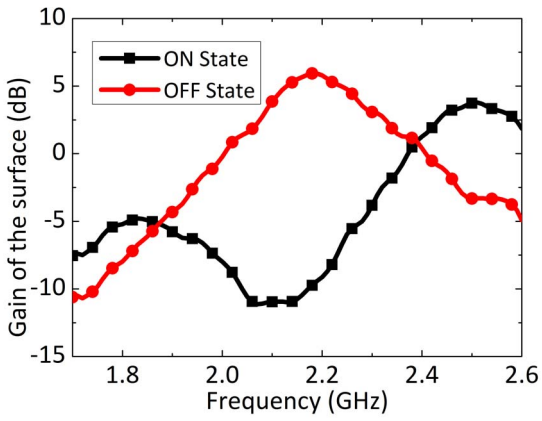


(a)

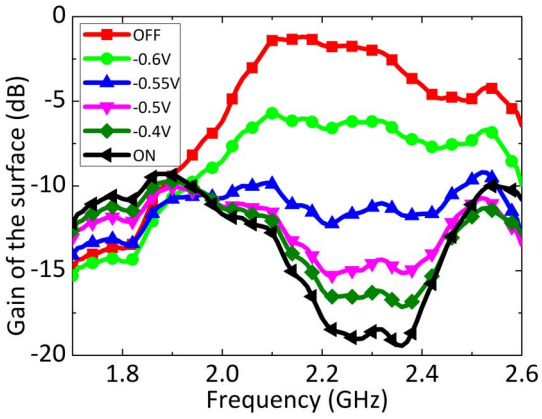


(b)

Fig. 10. (a) Surface wave absorption chamber measurement setup. (b) Normal incidence (left) and grazing incidence (right) modes measurement position of the surface, with zoomed-in view of the surface. This array's element shares the same dimensions with the element described in Fig. 3(a) and the stack is the same as Fig. 3(c), in which the thicknesses of the RT 5880 and FR4 are both 3.125 mm. RT5880 and FR4 are isolated by thin prepreg sheet.



(a)



(b)

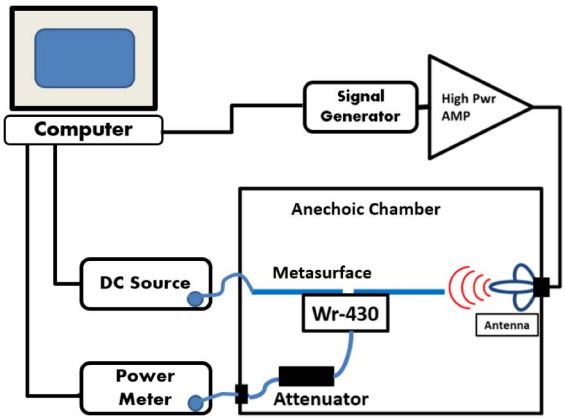
Fig. 11. (a) Relative amplitude comparing with input power leaking through the slit at ON- and OFF-states of normal incidence mode. (b) Tunable absorption rate with different dc biases of grazing incidence.

and angles relative to the polarization of the transmitting horn antenna shown in Fig. 10(b).

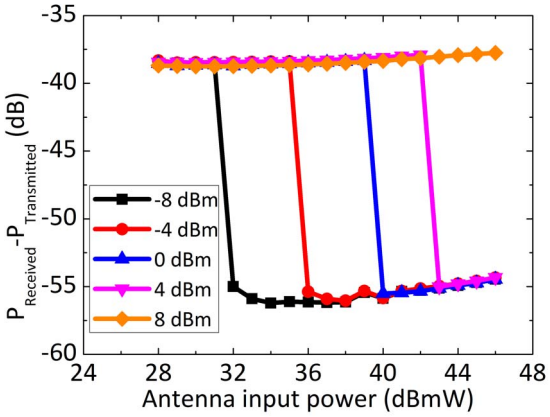
For the normal incidence mode, the ON- and OFF-states' gains are measured and plotted in Fig. 11(a). The gain of the surface is defined as the measured S_{21} value at the normal direction with setup indicated in Fig. 10(a). In the OFF-state, a peak gain of 6 dB is observed around 2.2 GHz, which matches with the gain in the normal direction (0°) of the slit from Fig. 9(b) and (c) in part A, Section IV. In the ON-state, we could see a peak attenuation of 16 dB at the frequency of interest, showing good surface current suppression ability. For the grazing incidence mode, we measured the surface's tunable and switchable absorbing ability by giving different bias to the gates of all the transistors (NE3503M04) and the results are plotted in Fig. 11(b). In the OFF-state, the peak measured gain is around 0 dB, while in the ON-state an attenuation of 18 dB is achieved. All these numbers match well with the azimuth-plane amplitude measured in Section IV-A for both OFF- and ON-states. With the range from −1- to 0-V dc bias on the gates of the switching transistors, different attenuations could be obtained, demonstrating the tunable absorption ability of this surface.

C. Sharp Absorption Response

Another advantage of this absorber is that it can potentially provide a sharp response to different incoming power levels. In other words, it is possible to preset a certain power density level threshold to this surface and control the absorber to be switched on, off or to any other middle state accordingly simply by providing different dc biasing voltages. To show this sharp response ability of the absorber, we used power meter (Agilent N1911A) to detect the received leakage power from the slit through standard waveguide WR-430. We define the threshold as the preset value of maximum power (leakage power) allowed to be received by the waveguide (WR-430). In real-time this power level is compared with the preset threshold value to control the dc supply and adjust the surface absorption. The transmitting signal is generated by a signal generator, (Agilent N5181A) amplified by high-power amplifiers (Ophir 5022 and 5193) and transmitted at a power level ranging from 25 to 50 dBm at the horn antenna located 2 m away from the surface. The measurement setup is shown in Fig. 12(a) and the absorption response is presented in Fig. 12(b) with different leakage power threshold



(a)



(b)

Fig. 12. (a) Experimental setup for sharp response absorbing ability measurement. (b) Sharp response of absorption with different power level thresholds.

values. A sharp response is demonstrated using this surface, and the leakage power attenuation from OFF-state to ON-state is about 17 dB. In other words, the absorber could be real-time controlled switching the surface from OFF-state directly into ON-state representing a sharp response. This has the advantage that at low-power level (less than the preset threshold), the absorber could remain in the OFF-state, which would not affect the performance of communication systems under protection. However, as soon as the threshold is reached, the absorber could be automatically turned on to shield sensitive electronic devices.

V. Conclusion

We introduced the first transistor-based, high-power, switchable and tunable surface wave absorbing metasurface. Two topologies of transistor-based metasurface absorber are studied and discussed. Combining the surface wave suppression ability of HISs with transistors' tunable drain to source channel resistance property, switchable absorbers are designed and measured. In the waveguide high-power measurement, the two topologies showed more than 60% and 70% absorption rate with input power density of 168 and 838 W/m^2, respectively in their ON-states, while in the OFF-states, at the frequency of interest they showed less than 10% and 20% absorption rate accordingly. A large panel with a slit working as a slot antenna is fabricated and measured. The radiation pattern and surface wave absorption are measured in both ON- and OFF-states and they matched each other well. Finally, a threshold preset self-sensing absorbing surface is tested and showed a sharp absorption response versus input power level.

This high-power, switchable, and tunable surface wave metasurface absorber has the advantage of being low profile, and having electronically controllable absorption, which could be used in against a wide range of incident power levels that may cause damage or interference to the communications systems or sensitive microwave components being shielded.

Acknowledgment

The authors would like to thank NRL collaborators J. G. Gil and P. Meyerhofer for their useful discussions and validations of measurements.

References

[1] C. L. Holloway, R. R. DeLyser, R. F. German, P. McKenna, and M. Kanda, "Comparison of electromagnetic absorber used in anechoic and semi-anechoic chambers for emissions and immunity testing of digital devices," *IEEE Trans. Electromagn. Compat.*, vol. 39, no. 1, pp. 33–47, Feb. 1997.

[2] B. K. Chung and H. T. Chuah, "Modeling of RF absorber for application in the design of anechoic chamber," *Progr. Electromagn. Res.*, vol. 43, pp. 273–285, 2003.

[3] Y. Naito and K. Suetake, "Application of Ferrite to electromagnetic wave absorber and its characteristics," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-19, no. 1, pp. 65–72, Jan. 1971.

[4] S. Sugimoto *et al.*, "Barium M-type ferrite as an electromagnetic microwave absorber in the GHz range," *Mater. Trans., JIM*, vol. 39, no. 10, pp. 1080–1083, 1998.

[5] N. I. Landy, S. Sajuyigbe, J. J. Mock, D. R. Smith, and W. J. Padilla, "Perfect metamaterial absorber," *Phys. Rev. Lett.*, vol. 100, no. 20, p. 207402, May 2008.

[6] M. Li, H. Yang, X. Hou, Y. Tian, and D.-Y. Hou, "Perfect metamaterial absorber with dual bands," *Progr. Electromag. Res.*, vol. 108, pp. 37–49, 2010.

[7] M. Li, S. Xiao, Y. Y. Bai, and B. Z. Wang, "An ultrathin and broadband radar absorber using resistive FSS," *IEEE Antennas Wireless Propag. Lett.*, vol. 11, pp. 748–751, 2012.

[8] A. H. Panaretos, D. E. Brocker, and D. H. Werner, "Ultra-Thin absorbers comprised by cascaded High-Impedance and frequency selective surfaces," *IEEE Antennas Wireless Propag. Lett.*, vol. 14, pp. 1089–1092, 2015.

[9] B. Zhu, Z. Wang, C. Huang, Y. Feng, J. Zhao, and T. Jiang, "Polarization insensitive metamaterial absorber with wide incident angle," *Progr. Electromagn. Res.*, vol. 10, no. 1, pp. 231–239, 2010.

[10] J. Lee and S. Lim, "Bandwidth-enhanced and polarisation-insensitive metamaterial absorber using double resonance," *Electron. Lett.*, vol. 47, no. 1, pp. 8–9, Jan. 2010.

[11] G. I. Kiani, K. L. Ford, K. P. Esselle, A. R. Weily, and C. J. Panagamuwa, "Oblique incidence performance of a novel frequency selective surface absorber," *IEEE Trans. Antennas Propag.*, vol. 55, no. 10, pp. 2931–2934, Oct. 2007.

[12] A. Fallahi, A. Yahaghi, H.-R. Benedickter, H. Abiri, M. Shahabadi, and C. Hafner, "Thin wideband radar absorbers," *IEEE Trans. Antennas Propag.*, vol. 58, no. 12, pp. 4051–4058, Dec. 2010.

[13] D. Sievenpiper, H. P. Hsu, J. Schaffner, G. Tangonan, R. Garcia, and S. Ontiveros, "Low-profile, four-sector diversity antenna on high-impedance ground plane," *Electron. Lett.*, vol. 36, no. 16, pp. 1343–1345, Aug. 2000.

[14] J. Lee and D. Sievenpiper, "Patterning technique for generating arbitrary anisotropic impedance surfaces," *IEEE Trans. Antennas Propag.*, vol. 64, no. 11, pp. 4725–4732, Nov. 2016.

[15] J. Hunt *et al.*, "Metamaterial apertures for computational imaging," *Science*, vol. 339, no. 6117, pp. 310–313, 2012.

[16] J. Zhao, Q. Cheng, J. Chen, M. Q. Qi, W. X. Jiang, and T. J. Cui, "A tunable metamaterial absorber using varactor diodes," *New J. Phys.*, vol. 15, no. 4, pp. 43049–43059, Apr. 2013.
[17] D. Shrekenhamer, W.-C. Chen, and W. J. Padilla, "Liquid crystal tunable metamaterial absorber," *Phys. Rev. Lett.*, vol. 110, no. 17, p. 177403, 2013.
[18] Y. Huang, G. Wen, W. Zhu, J. Li, L.-M. Si, and M. Premaratne, "Experimental demonstration of a magnetically tunable ferrite based metamaterial absorber," *Opt. Exp.*, vol. 22, no. 13, pp. 16408–16417, 2014.
[19] H. Wakatsuchi, S. Kim, J. J. Rushton, and D. F. Sievenpiper, "Circuit-based nonlinear metasurface absorbers for high power surface currents," *Appl. Phys. Lett.*, vol. 102, no. 21, pp. 214103-1–214103-4, May 2013.
[20] D. F. Sievenpiper, "Nonlinear grounded metasurfaces for suppression of high-power pulsed RF currents," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1516–1519, Feb. 2012.
[21] H. Wakatsuchi *et al.*, "Experimental demonstration of nonlinear waveform-dependent metasurface absorber with pulsed signals," *Electron. Lett.*, vol. 49, no. 24, pp. 1530–1531, Nov. 2013.
[22] H. Wakatsuchi, S. Kim, J. J. Rushton, and D. F. Sievenpiper, "Waveform-dependent absorbing metasurfaces," *Phys. Rev. Lett.*, vol. 111, no. 24, p. 245501, Dec. 2013.
[23] S. Kim, H. Wakatsuchi, J. J. Rushton, and D. F. Sievenpiper, "Switchable nonlinear metasurfaces for absorbing high power surface waves," *Appl. Phys. Lett.*, vol. 108, no. 4, 2016, Art. no. 041903.
[24] B. Zhu, Y. Feng, J. Zhao, C. Huang, and T. Jiang, "Switchable metamaterial reflector/absorber for different polarized electromagnetic waves," *Appl. Phys. Lett.*, vol. 97, no. 5, p. 051906, 2010.
[25] M. Yoo and S. Lim, "Active metasurface for controlling reflection and absorption properties," *Appl. Phys. Exp.*, vol. 7, no. 11, 2014, Art. no. 112204.
[26] A. Tennant and B. Chambers, "A single-layer tuneable microwave absorber using an active FSS," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 1, pp. 46–47, Jan. 2004.
[27] J. Li *et al.*, "Design of a tunable low-frequency and broadband radar absorber based on active frequency selective surface," *IEEE Antennas Wireless Propag. Lett.*, vol. 15, pp. 774–777, 2016.
[28] P. Kong *et al.*, "A novel tunable frequency selective surface absorber with dual-DOF for broadband applications," *Opt. Exp.*, vol. 22, no. 24, pp. 30217–30224, 2014.
[29] D. Sievenpiper, L. Zhang, R. F. J. Broas, N. G. Alexopolous, and E. Yablonovitch, "High-impedance electromagnetic surfaces with a forbidden frequency band," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 11, pp. 2059–2074, Nov. 1999.
[30] A. Li, E. Forati, and D. Sievenpiper, "Study of the electric field enhancement of high-impedance surfaces," in *Proc. IEEE Int. Symp. Antennas Propag. (APSURSI)*, Jul. 2016, pp. 105–106.
[31] R. Mittra, C. H. Chan, and T. Cwik, "Techniques for analyzing frequency selective surfaces—A review," *Proc. IEEE*, vol. 76, no. 12, pp. 1593–1615, Dec. 1988.
[32] (2016). *Advanced Materials for PCBs, Power Distribution, Impact Protection—Rogers Corp, Rogerscorp.com*. [Online]. Available: http://rogerscorp.com
[33] (2016). *National Instruments: Test, Measurement, and Embedded Systems—National Instruments, Ni.com*. [Online]. Available: https://www.ni.com

Aobo Li (S'16) received the B.S. degree and the M.S. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2010 and 2013, respectively, and the M.S. degree in telecommunications from the Georgia Institute of Technology, Atlanta, GA, USA He is currently pursuing the Ph.D. degree at the University of California at San Diego, La Jolla, CA, USA.

From 2013 to 2014, he was an Application Engineer with National Instruments. His current research interests include active metasurface microwave absorbers, metasurface microwave sources, wireless power transmission, and phased arrays systems.

Sanghoon Kim (S'12) received the B.S. and M.S. degrees in physics from Konkuk University, Seoul, South Korea, in 2005 and 2008, respectively. He is currently pursuing the Ph.D. degree at the University of California at San Diego, La Jolla, CA, USA.

He is currently involved with nonlinear active metamaterial surfaces with nonlinear RF circuit components for high power RF absorbers, reconfigurable impedance surface, and self-tuning metasurfaces. He has authored over ten technical publications.

Yong Luo received the Ph.D. degree from The University of Tokyo, Tokyo, Japan, in 2015.

From 2010 to 2012, he was an Electrical Engineer with Huawei, where he was involved in phased-array antennas for base stations. Since 2016, he has been a Post-Doctoral Fellow with Prof. Daniel F. Sievenpiper's Applied Electromagnetic Group, Jacobs School of Engineering, University of California at San Diego, La Jolla, CA, USA, where he is involved in nonlinear meta-surfaces using diodes. His research interests included active metamaterials for scanning radiation beams by using a micro-machining fabrication process to monolithically integrate antennas with MEMS. His current research interests include active antennas, nonlinear metamaterials, and RF-MEMS.

Yunbo Li received the B.Sc. degree from Xidian University, Xi'an, China, in 2009, the M.Sc. degree from the Graduate School, Second Academy of China Aerospace Science and Industry Corporation, Beijing, China, in 2012, and the Ph.D. degree from Southeast University, Nanjing, China, in 2016.

Since 2016, he has been a Post-Doctoral Fellow with the Applied Electromagnetics Research Group, University of California at San Diego, La Jolla, CA, USA. His current research interests include metasurface-based antenna design, non-Foster and active metasurfaces, and the advanced microwave image system.

Jiang Long (S'11–M'17) received the B.S. and M.S. degrees from Zhejiang University, Hangzhou, China, in 2007 and 2010, respectively, and the Ph. D. degree from the University of California at San Diego, La Jolla, CA, USA, in 2015.

He is currently an RF Engineer with Skyworks Solutions Inc., San Jose, CA, USA. His current research interests include non-Foster circuits in antenna/microwave applications, including non-Foster circuit loaded active fast-wave waveguides, broadband metasurfaces, broadband antennas, and active microwave components.

Dr. Long was a recipient of the IEEE MTT-S Graduate Fellowship in 2015.

Daniel F. Sievenpiper (M'94–SM'04–F'09) received the B.S. and Ph.D. degrees in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, in 1994 and 1999, respectively.

He was the Director of the Applied Electromagnetics Laboratory, HRL Laboratories, Malibu, CA, USA, where he was involved in artificial impedance surfaces, conformal antennas, tunable and wearable antennas, and beam-steering methods. He is currently a Professor with the University of California at San Diego, La Jolla, CA, USA, where he is involved in antennas and electromagnetic structures. He has authored over 120 technical publications and holds over 70 issued patents.

Dr. Sievenpiper was a recipient of the URSI Issac Koga Gold Medal in 2008. Since 2010, he has been an Associate Editor of IEEE ANTENNAS AND WIRELESS PROPAGATION LETTERS.