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Millimeter-wave Wafer-Scale Phased Arrays and Wireless Communication Circuits and Systems in SiGe and CMOS Technology

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Woorim Shin

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor James Buckwalter
Professor Gert Cauwenberghs
Professor William S. Hodgkiss
Professor Lawrence E. Larson

2013

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Chair

University of California, San Diego

2013

DEDICATION

To my parents, Joong-Rin and Myung-Hee,
my wife, Bora, my son, Hajun,
and all of those who shared their lives with me.

EPIGRAPH

Be patient toward all that is unsolved in your heart
and try to love the questions themselves.
—Rainer Maria Rilke

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Chapter 3 is based on and in part a reprint of the following paper:

- W. Shin and G. M. rebeiz, "60 GHz active phase shifter using an optimized quadrature all-pass network in 45nm CMOS," *IEEE Microwave Symposium Digest*, Jun. 2012, pp. 17-22.

Chapter 4 is based on and mostly a reprint of the following paper:

- W. Shin, M. Uzunkol, R. A. Alhalabi, and G. M. Rebeiz, "60 GHz Low Power 1.5 Gb/s ASK Transmitter in 90 nm CMOS with On-board Yagi-Uda Antenna," *IEEE European Microwave Conference*, Sep. 2010, pp. 272-275.

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VITA

2007	B. S. in Electrical Engineering, Seoul National University, Seoul, Rebublic of Korea
2009	M. S. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego
2013	Ph. D. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego

PUBLICATIONS

W. Shin, B.-H. Ku, O. Inac, Y.-C. Ou, and G. M. Rebeiz, "A 108–114 GHz 4×4 wafer-scale phased array transmitter with high-efficiency on-chip antennas," *IEEE Journal of Solid-State Circuits*, accepted for publication, to appear in Sept. 2013.

M. Uzunkol, W. Shin, and G. M. Rebeiz, "Design and analysis of a low-power 3–6-Gb/s 55-GHz OOK receiver with high-temperature performance," *IEEE Trans. Microwave Theory and Tech.*, vol. 60, no. 10, pp. 3263–3271, October 2012.

W. Shin and G. M. Rebeiz, "60 GHz active phase shifter using an optimized quadrature all-pass network in 45nm CMOS," *IEEE Int. Microwave Symp. Dig.*, June 2012, pp. 1–3.

W. Shin, O. Inac, Y.-C. Ou, B. Ku, and G. M. Rebeiz, "A 108–112 GHz 4×4 wafer-scale phased array transmitter with high-efficiency on-chip antennas," *Proc. IEEE Radio Frequency Integrated Circuit Symp.*, June 2012, pp. 199–202.

W. Shin, M. Uzunkol, R. A. Alhalabi, and G. M. Rebeiz, "60 GHz low power 1.5 Gb/s ASK transmitter in 90 nm CMOS with on-board Yagi-Uda antenna," *IEEE European Microwave Conference*, Sept. 2010, pp. 272–275.

G. M. Rebeiz, J. May, M. Uzunkol, W. Shin, O. Inac, and M. Chang, "Towards high-performance > 100 GHz SiGe and CMOS circuits," *IEEE Int. Microwave Symp. Dig.*, June 2010, pp. 1320–1323.

W. Shin, M. Uzunkol, and G. M. Rebeiz, "Ultra low power 60 GHz ASK SiGe receiver with 3–6 Gpbs capabilities," *IEEE Compound Semiconductor Integrated Circuits Symp.*, Oct. 2009, pp. 1–4.

ABSTRACT OF THE DISSERTATION

Millimeter-wave Wafer-Scale Phased Arrays and Wireless Communication Circuits and Systems in SiGe and CMOS Technology

by

Woorim Shin

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2013

Professor Gabriel M. Rebeiz, Chair

This thesis presents a W-band wafer-scale phased array transmitter with high-efficiency on-chip antennas. The 4×4 phased array is based on an RF beamforming architecture with an equiphase distribution network and 2-bit phase shifters placed in every element. The differential on-chip antennas are implemented using a 100 μm thick quartz superstrate and have an efficiency of ~45% at 110 GHz. The use of electromagnetically coupled antenna leads to wafer-scale phased array concept with simple integration method. The phased array transmitter is implemented in 0.18 μm SiGe BiCMOS process, and the measurement shows an array gain of 26.5 dB, pattern directivity of 17.0 dBi, maximum EIRP of 23–25 dBm at 108–114 GHz. The direct pattern measurement from the phased array transmitter shows beam steering capabilities up to ±30°

in two orthogonal directions. This is the first demonstration of wafer-scale phased array in silicon technology.

Millimeter-wave circuit components in 45nm SOI CMOS technology are also presented. Transmission-line based D-band common-source and cascode amplifers are designed with the peak gain of 8.7 dB at 147 GHz and 6.1 dB at 171 GHz, respectively. The experimental characterization of the technology shows that on-chip passive elements has low-quality factor, and it can offset performance advantage of the active devices. A 60 GHz active phased shifter with quadrature all-pass filter shows -4 dB insertion gain with <1.5 dB RMS gain error and <10° RMS phase error. An analysis shows the asymmetric loading to the all-pass filter can induce more phase error, and the use of series resistor is used as a mitigation.

Also, an OOK transmitter in 90nm CMOS technology is presented. The OOK transmitter consists of a 30 GHz VCO, a resistive coupler, a frequency doubler, an OOK modulator based on a cascode amplifier, and a medium power amplifier. A single-ended architecture results in simple low-power implementation of a transmitter, and an output OOK spectrum up to Gbps range is observed, demonstrating OOK modulation scheme is suitable for low-power point-to-point high data-rate communication link in millimeter-wave frequencies.

Chapter 1

Introduction

1.1 Background

The milllimeter-wave frequency band (mm-wave, 30–300 GHz) has interesting characteristics which impose challenges and provide opportunities together for academic research and industrial applications. High propagation loss, additional atmospheric attenuation, and limited device performance are probably major obstacles for implementing practical circuits and systems at mm-wave frequencies. On the other hand, large available bandwidth, smaller antenna size, finer resolution and penetrating capability through thin materials are unique qualities that make mm-wave systems attractive. Possible applications include high data-rate wireless communication systems, active/passive imaging systems, and automotive radars and sensor systems. Previously mm-wave circuits and systems were considered to be mainly implemented using compound semiconductor technologies such as GaAs or InP, but in the past few years silicon technologies have also gained much attention as an alternative for mm-wave circuits and systems, owing to their recent advance in device performance and high level of integration.

Silicon integrated-circuit technologies, i.e. SiGe HBT (silicon-germanium hetrojunction bipolar transistor) and CMOS FET (complementary metal-oxide-semiconductor field effect transistor) technologies, have been continously advanced with aggresive down-scaling, driven by the need for high-performance, low-cost systems with more functionality and high-level of integration. As of 2008, one of the foundry reported

SiGe f_t/f_{max} of 200/380 GHz [1] and another reported CMOS having 150/200 GHz [2], following the projection of ITRS [3]. Performance metrics including transistor speed strongly suggest that silicon technologies are competitive at mm-wave frequencies, and they are expected to be even more competitive with the benefit of digital computation, large-scale integration, and high-yield fabrication. In general, SiGe technology is believed to have superior RF performance to CMOS technology, but the high-frequency performance of CMOS technology is further enhanced by advanced fabrication processes such as SOI (silicon-on-insulator) CMOS technology.

Although the operation frequency of SiGe or CMOS technology has reached mm-wave region, some technical challenges are still to be overcome in order to build mm-wave circuit and systems. Down-scaling of transitors usually results in lower breakdown voltage, thus available power for unit device is smaller than other competing technologies. Also, increased skin effect and substrate loss can lower the quality factors of integrated passive devices which offset the increased performance of active devices. A phased array system is often considered an ingenious solution to this issue due to its ability to combine and focus signal power from multiple elements in one direction. It can also change the direction of the output power, spatially distinguish multiple channels, and increase the link budget of a communication system. Multiple transmitters/receivers with antennas can work in cooperation by the virtue of constructive interference of wave propagation in the space.

A strong demand for low-cost, efficient, and high data-rate wireless communication system is another driving factor for implementing silicon millimeter-wave circuit and systems. Prospective applications including data transfer or video streaming require several gigabit-per-second data rate for user's convenience, and wide available bandwidth in mm-wave bands in conjunction with low-cost silicon technology are considered enabling factors. Especially, unlicensed ISM (industrial, scientific, and medical) bands around 60 GHz (57–64 GHz) and 120 GHz is an attractive field for such systems.

1.2 Motivation

Silicon phased arrays in mm-wave bands have been an active research area in the past few years, but many of the previous works do not integrate antennas on chip, and radiating elements are considered off-chip components. In this case, an interconnect structure from the chip to antenna elements can be highly reactive (inductive) at millimeter-wave frequencies, making it a very challenging task to impedance-match and maximize signal transfer. A typical example of such a structure is a bond-wire which connects on-chip contact pads to external printed circuit boards (PCB). Also, larger tolerance in packaging process sometimes imposes additional constraints in phased array design, resulting in sub-optimal design. This thesis proposes an alternive to design a millimeter-wave phased array in silicon technology by using an electromagnetically coupled (EM-coupled) on-chip antenna structure. This integration method can be applicable to any two-dimensional arrangement of phased array elements, which enables a wafer-scale phased array with large number of elements.

An OOK (on-off keying) modulation scheme results in a simple, low-cost, and low-power implementation for a wireless transceiver. As OOK does not carry information on the phase of the carrier frequency, the OOK transceiver architecture can be implemented without I/Q up-down converters and phase-locked loop which other complex modulation schemes such as BPSK, QPSK, or QAM require. Expected applications of millimeter-wave wireless communication are indoor point-to-point communication link, high-definition video streaming, and wireless multimedia contents transfer from a service station to a mobile device. As these applications suppose a relatively controlled or predictable wireless environment, a low-power OOK transceiver is suitable for these applications in spite of its susceptibility to strong interference. Also, use of a directional antenna of more than 10 dBi or a phased array antennas can improve the overall system performance for an OOK communication link.

1.3 Thesis Overview

This thesis presents millimeter-wave phased array and wireless communication circuits and systems in SiGe and CMOS technology.

Chapter 2 presents a 2-dimensional 4×4 phased array transmitter with wafer-scale integration method, which is operating at 110 GHz and implemented in 0.18 μm SiGe BiCMOS process. The concept of the wafer-scale integration method is described, and a 2-bit phased-array single element with antenna driver amplifier is presented. The 4×4 phased array also contains an equi-phase distribution network which consists of Wilkinson power dividers, on-chip CPW lines, and distribution amplifiers. An internal voltage-controlled oscillator (VCO) and frequency doubler chain is also designed to support stand-alone power generation without an external signal input. The simulated antenna gain and efficiency is 2.7 dBi and 45%, respectively. The phased array successfully demonstrates transmit beam-forming and beam-steering capabilities with ±30° scan angles in two orthogonal directions, showing the first direct pattern measurement from on-chip phased array in silicon technology. The phased array transmitter also results in 26.5 dB array gain, 24.0 dBm maximum EIRP, and 28° 3-dB beamwidth while consuming 1.78 A from 1.9 V supply.

Chapter 3 presents millimeter-wave communication circuits in 45nm SOI CMOS technology, including amplifiers in D-band frequencies and a 60 GHz active phase shifter. First, experimental characterization of SOI CMOS technology at D-band frequency is presented. SOI CMOS transistor shows f_{max} of 230–250 GHz, while on-chip passive elements show degraded quality factors. A common-source (CS) amplifier and a cascode amlifier are designed in D-band with the SOI CMOS process. The CS amplifier shows measured gain of 8.7 dB at 147 GHz and a 3-dB bandwidth of 17 GHz, and the cascode amplifier shows measured gain of 6.1 dB at 171 GHz and a 3-dB bandwidth of 24 GHz. The 60 GHz active phase shifter is also designed and characterized. Design challenges at millimeter-wave active phase shifter are identified and analyzed, and an improved I/Q generation network using series resistors is used in order to mitigate performance degradation. The resulting phase shifter shows -6±2 dB insertion gain with 3-dB bandwidth of 46–64 GHz, <1.5 dB RMS gain error, and ~10° RMS phase error.

Chapter 4 presents a 60 GHz OOK transmitter in 90nm CMOS technology. The OOK transmitter consists of a 30 GHz VCO, a resistive signal coupler, a frequency doubler, an ASK modulator, and a medium power amplifier. A single-ended architecture (except the VCO) results in a low-power solution, which only consumes 31.2 mW from

1.2 V supply. Individual blocks are measured and conforms with simulation results. The 30 GHz VCO results in -11.2 dBm single-ended output power with -99.6 dBc/Hz phase noise at 1 MHz offset frequency. The frequency doubler shows 11–12 dB of conversion loss with -9 to -5 dBm input power, and the OOK modulator shows -1.8 dB of insertion gain with -10 dB input bandwidth of 58–68 GHz. Finally, the medium power amplifier shows 10.7 dB gain at 54.6 GHz with a 3-dB bandwidth of 50–61.4 GHz. Its peak PAE is 12.9 %, and output P1dB of 1.4 dBm. The overall OOK transmitter can support 1.5 Gbps data stream as shown by spectrum measurements.

The thesis concludes with a summary of the work in chapter 5.

Chapter 2

4×4 Wafer-Scale Phased Array Transmitter with High-Efficiency On-Chip Antennas

2.1 Introduction

Millimeter-wave phased-arrays on silicon RFICs have been an important topic of research in the past 5 years with application areas in Gbps communications and automotive radars. After the early demonstrations of single, four and 8-elements arrays on a single-chip [4, 5, 6, 7, 8, 9, 10, 11, 12], the phased-arrays quickly jumped to 16 and 32-elements on a single-chip [13, 14, 15, 16, 17, 18]. For a phased array with N-elements and in the transmit mode, the EIRP (effective isotropic radiated power) is defined as $P_T G_T$ where P_T is the total transmit power and G_T is the transmit antenna gain[19]. P_T is N times the power radiated per element and G_T is proportional to N and the EIRP is proportional to N^2. In the receive mode, the phased array antenna gain is also proportional to N. Therefore, the link budget, which is proportional to $P_T G_T G_R$ has an N^3 dependence, and phased arrays with N=16–32 or even N=64–256 are therefore required for medium to long-range Gbps communication links, automotive radars or active imaging arrays.

The 8, 16, and 32-element phased-array chips did not include any antennas, and

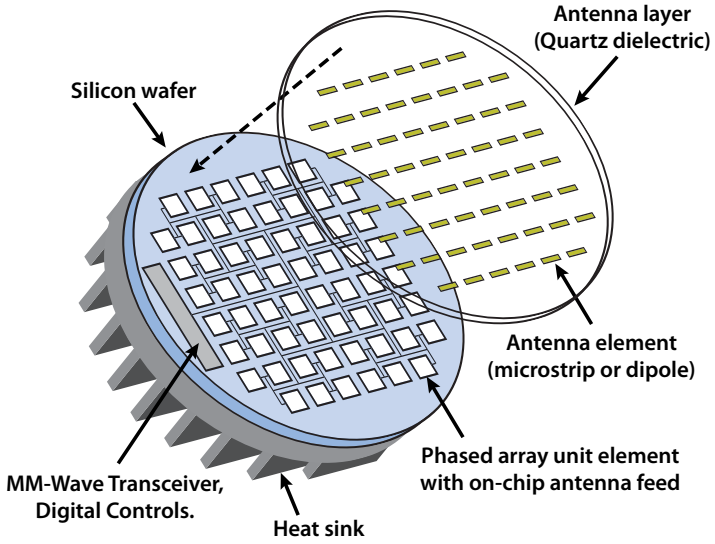


Figure 2.1: Conceptual diagram of a millimeter-wave wafer-scale phased array with on-chip antennas.

therefore, a transmission-line distribution network was used between the N-element silicon chip and the planar antenna array. This required mm-wave transitions between the silicon chip and the distribution network, and was successfully done using flip-chip techniques and multilayer organic, Teflon or LTCC substrates [20, 14, 15, 21, 22, 23, 24, 25, 26, 27, 28, 29], or using polyimide re-distribution layers on-top of the silicon chip to result in a wafer-level package (WLP) or chip-scale package (CSP) [30, 31, 32]. However, the transitions and distribution network adds a substantial amount of loss (2–4 dB at 60–80 GHz for 16 elements) between the silicon chip and the antennas, and requires careful design so as not to introduce electromagnetic coupling between the different antenna elements which can degrade the patterns. Also, it is not scalable beyond 16 (or 32) elements due to the additional loss and distribution complexity. Finally, multi-layer Teflon and LTCC substrates for mm-wave systems are generally as expensive as the silicon chip, which can double the cost of the front-end system.

Wafer-scale phased arrays offer a simple solution to the complex distribution problem (Fig. 2.1). In this case, a wafer-scale antenna layer is placed directly above the silicon substrate and each antenna is fed by a corresponding phased-array cell (phase shifters, VGA, etc.). This approach eliminates the distribution network loss, can be ap-

plied to a 4-element and even a 64-element phased array, and has been proven before at 77 GHz[33], at 90–100 GHz for a 3×3 power amplifier array [34], and at 110 GHz in a 16-element wafer-scale phased array [35]. The concept is also scalable to a very large number of elements (true wafer-scale) but in this case, care should be placed on the power and RF distribution loss for such systems. The antennas must be efficient (~50%) so as to be competitive with the standard technique, and such antennas are currently being demonstrated in many self-contained sensors, radars and short-range communication systems [36, 37, 38, 39, 40, 41]. The wafer-scale approach is also popular at THz frequencies and several groups have demonstrated imaging arrays [42, 43, 44] and transmitters [45] based on high-efficiency on-chip antennas.

It is important to note that the wafer-scale approach does require that the silicon chip be as large as the antenna aperture, which may not be feasible below 60 GHz. For these applications, it is best to build a smaller silicon chip and fan out to the antennas using a multi-layer substrate[21, 25, 15]. However, above 60 GHz, and especially for large systems, the wafer-scale approach may be an excellent solution for phased arrays knowing that the silicon cost continues to drop even for advanced CMOS and SiGe nodes.

2.2 Design

2.2.1 Technology

The 16-element wafer-scale phased array is built using Jazz SBC18H3 process. It is 0.18 μm SiGe BiCMOS process which provides high-speed HBT (0.13 μm emitter width), 6 aluminum metal layers (2.8 μm top metal thickness), and high-density MIM capacitors (5.6 fF/μm^2). The cross-section view of the technology backend is shown in Fig. 2.2. The high-speed HBT has a peak f_t/f_{max} of 240/280 GHz [46].

Grounded co-planar waveguide (G-CPW) transmission lines are heavily used in this phased array for the distribution network and as inductor loads, in order to have high isolation between two adjacent lines or components. The 50 Ω transmission line is implemented using M6 for the signal line and M4 for the ground plane (Fig. 2.2(a)). The electromagnetic (EM) simulations using Sonnet [47] show an attenuation (α) of 1.0

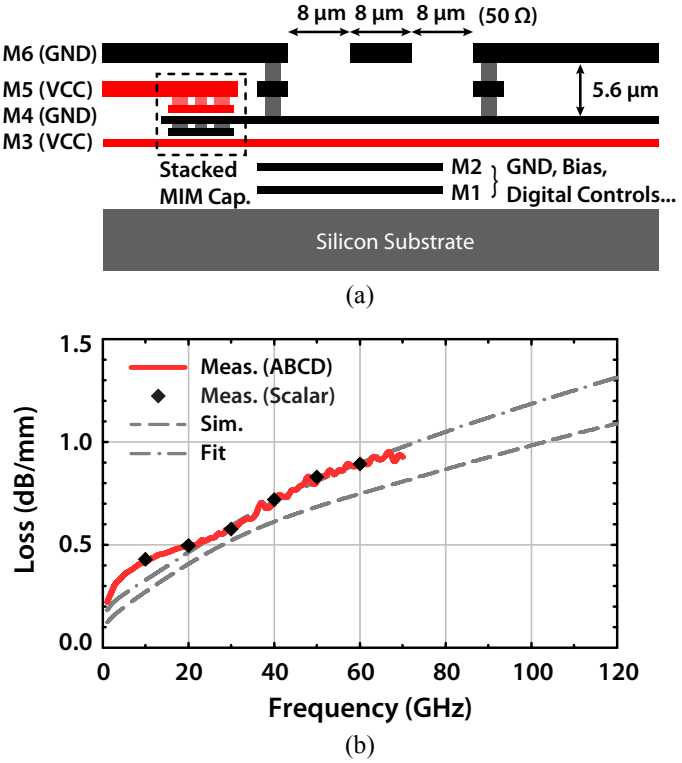


Figure 2.2: (a) Cross-section view of metal layers of the Jazz SBC18H3 technology. An on-chip 50 Ω G-CPW transmission line is shown. (b) Measured and simulated loss of the transmission line.

dB/mm and propagation constant (β) of 4.4 rad/mm at 110 GHz, resulting in transmission line Q ($\beta/2\alpha$) of 18.8. The effective dielectric constant ($\varepsilon_{r,eff}$) is 3.64, resulting in a wavelength of 1.43 mm at 110 GHz.

A 1 mm-long line is measured at DC–67 GHz, and the GSG pad parasitics are de-embedded using an on-chip through standard. Fig. 2.2(b) presents the measured line loss along with simulations. The line loss is calculated in two ways, one using ABCD-parameters [48] and the other using scalar loss subtraction. Both calculations show consistency, and the measured line loss is 0.9 dB/mm at 60 GHz while the simulation predicts 0.75 dB/mm. A modified simulation fitted to the measurement predicts 1.25 dB/mm line loss at 110 GHz, with a t-line Q of 15.0.

Several transistor test structures are also measured in order to examine the effect of metal interconnect parasitics on the transistor performance. A two-step open-short de-embedding in M6 is performed for the test structures, and resulting data include the effect of base/collector contacts and the ground plane (Fig. 2.3(a)). The measured f_t of the transistor along with simulations are presented in Fig. 2.3(b). f_t is extrapolated from H_{21} at 20 GHz assuming -20 dB/dec slope, and the measured peak f_t is 220–230 GHz at a current density of 10–17 mA/μm^2.

2.2.2 Architecture

The block diagram of 4×4 wafer-scale phased array is shown in Fig. 2.4(a). A 54–56 GHz oscillator is used together with a frequency doubler and an amplifier as a 108–112 GHz on-chip source. A rat-race coupler (0°/180° hybrid) is employed and is connected to the VCO and an external RF input. The rat-race coupler provides >20 dB isolation at 95–130 GHz between the two different inputs and allows the use of either the on-chip VCO or the external input as the transmission source (Fig. 2.4(b)). It also provides a 3-dB power division between the top-half and bottom-half of the chip, which is necessary for power distribution. The VCO signal results in a 0°/0° phase difference at the outputs of the rat-race coupler and no phase correction is needed. The signal from the RF input results in a 0°/180° phase difference at the outputs of the rat-race coupler, but this is corrected using the 180° phase shifter in each unit element. The rat-race coupler therefore allows an efficient selection of two different input signals together

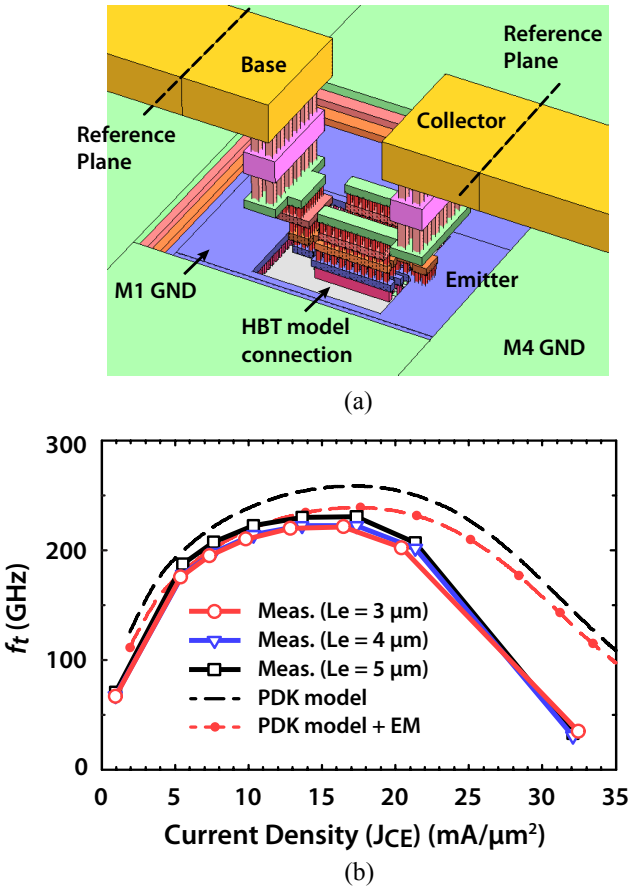


Figure 2.3: (a) 3-D EM modeling of the transistor contact. (b) Simulated and measured f_t of HBT transistors.

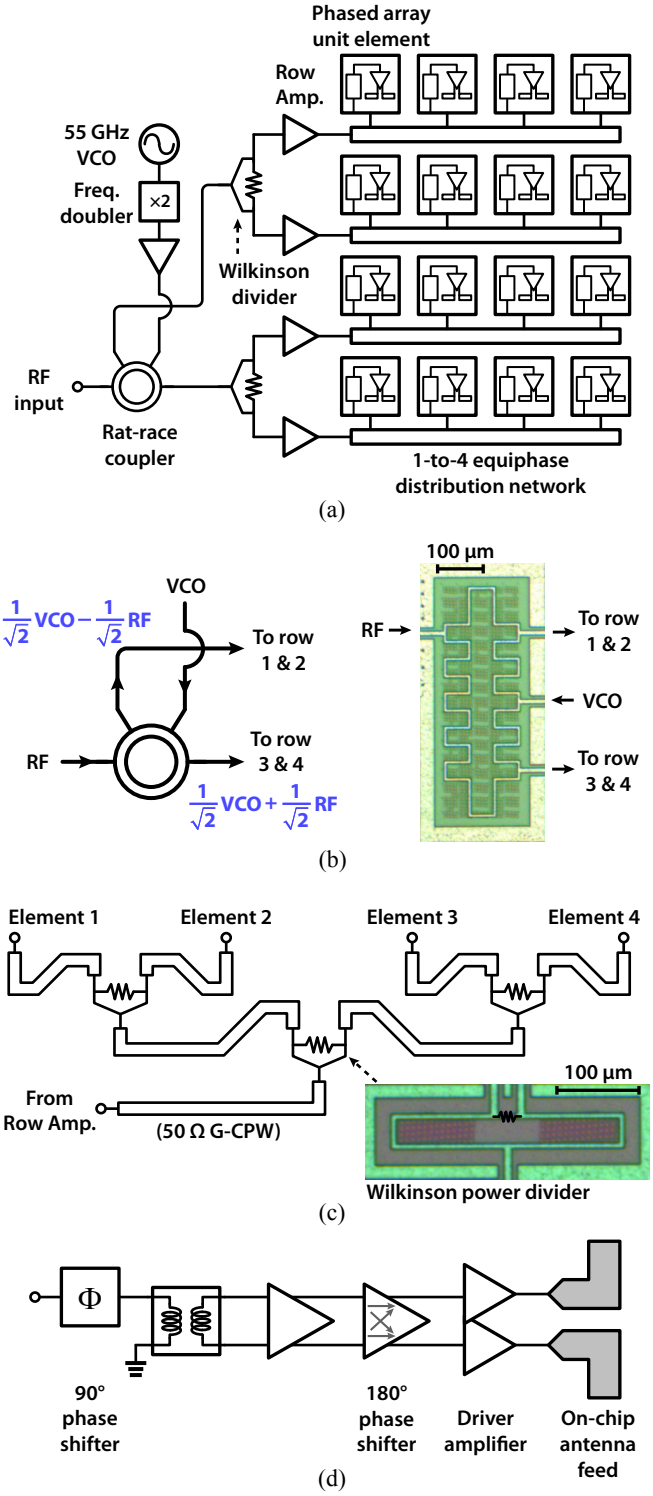


Figure 2.4: Block diagrams of (a) the 4×4 wafer-scale phased array, (b) the rat-race coupler, (c) the 1-to-4 equiphase distribution network, and (d) the phased-array unit-element.

with power division in a 4-port network with minimal loss.

The RF signals are then split using two Wilkinson dividers into 4 row amplifiers, and then split again in an equiphase network consisting of additional Wilkinson dividers and transmission-lines (Fig. 2.4(c)). This ensures that all the 16 signals arriving to each unit element are in phase and no phase correction is needed for the distribution network (other than the 0°/180° from the external RF input due to the rat-race coupler). The unit element consists of a single-ended 90° phase shifter, a passive balun with a buffer amplifier, a differential 180° phase shifter, a pseudodifferential driver amplifier, and a differential high-efficiency wafer-scale dipole antenna. (Fig. 2.4(d)). The design therefore has a 2-bit phase shifter in each unit element capable of generating phase shifts of 0°, −90°, −180°, and −270°.

2.2.3 On-chip VCO and Distribution Network

An 112–114 GHz source is integrated on-chip so as to test the wafer-scale phased array without an external W-band proble. A differential cross-coupled oscillator with a common-collector buffer is used for the VCO (Fig. 2.5(a)). A DC decoupling capacitor (C1) is used for bias control and a common-mode tail resistor (R1) is used for bias stabilization. The shunt capacitor C2 is used to suppress noise from R1 [49]. An accumulation-mode MOS (AMOS) varactor (M1) in series with an MIM capacitor (C3) is used for capacitive tuning. C3 allows a full range (0–V_{CC}) on the control voltage and increases the tuning range. The bias current density is 5.8 mA/μm^2 in order to achieve a balance between output amplitude, power consumption, and phase noise. The VCO and buffer consume 30 mA from 1.5 V supply and result in a simulated 1.0 dBm output power with a phase noise of −85 dBc/Hz at 1 MHz offset. Its tuning range is 56–57.5 GHz with 0–1.5 V control voltage.

The 55-110 GHz balanced doubler is designed using a differential pair (Q1) followed by a cascode stage (Q2) (Fig. 2.5(b)). The Q1 transistors are biased at a low current level (1.6 mA/μm^2) in order to efficiently generate harmonics of the input signal[50, 51]. Due to its balanced operation, only even harmonics are combined constructively at the collector node. Input and output matching provide maximal power transfer at 1st and 2nd harmonics, respectively. The simulated conversion gain is −5.0

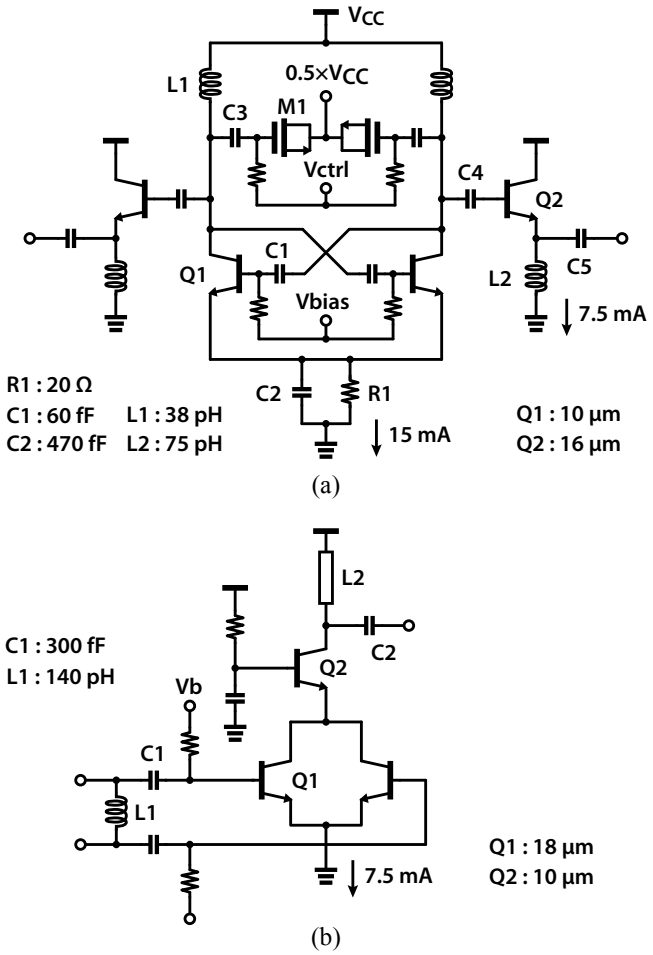


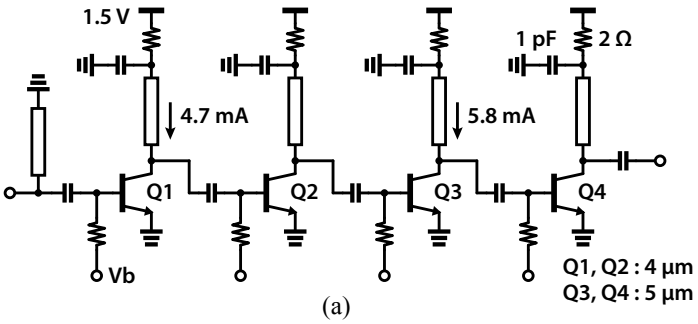
Figure 2.5: Schematic of (a) the 55 GHz VCO and (b) the 110 GHz frequency doubler.

dB at 110 GHz with 1.0 dBm input.

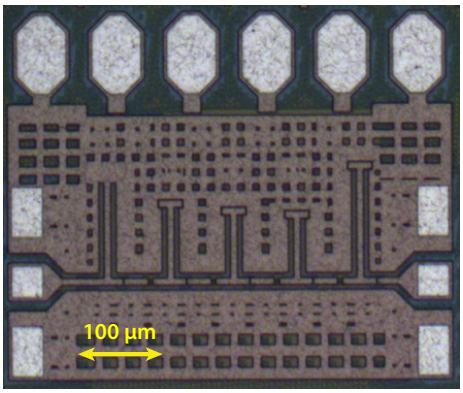
A 4-stage common source (CS) amplifier is used after the doubler (Fig. 2.6), and it is also used in the 1-to-4 distribution network (referred as "row amplifier"). An emitter length of 3–5 μm is found to be optimal as it has a low base resistance and provides a maximum available gain (MAG) of 4.4 dB at 110 GHz. Each transistor is biased at 10–15 mA/μm^2 collector current density for high f_t and f_{max}. G-CPW 50 Ω transmission lines are used as inductive loads and single-stack MIM capacitors are used as matching capacitors. Small resistors (2 Ω) are placed between the power supply and AC ground in order to prevent low frequency oscillation. On-chip bypass networks composed of 3 Ω polysilicon resistors and stacked MIM capacitors are placed around the amplifier in order to prevent coupling through the supply line. Also, the input matching is achieved using a high-pass LC network in order to achieve a wide bandwidth. The simulated gain is 12.5 dB at 110 GHz with a 3-dB bandwidth of 94–121 GHz. The simulated 1-dB output compression point (OP_{1dB}) and saturated output power (P_{sat}) are -1.5 dBm and 2.5 dBm, respectively, at 110 GHz. The current consumption is 21 mA (P_{DC}=31.5 mW).

The single-ended rat-race coupler is implemented using 70 Ω $\lambda/4$- and $3\lambda/4$-long microstrip transmission lines[52]. The meandered microstrip line occupies a smaller area compared to a G-CPW line since it eliminates the side ground walls. A 5 μm width signal line in M6 and ground plane in M4 results in 70 Ω line. The rat-race coupler occupies 510×180 μm^2 area with simulated insertion loss of 4.0±0.2 dB (including the 3 dB power division) at 96–125 GHz and <0.5 dB difference between the two output ports. The Wilkinson coupler is also designed using the 70 Ω $\lambda/4$ microstrip lines, and is employed as a matched power divider in the signal distribution network[52]. It has simulated insertion loss of 3.8 dB (including the 3 dB power division) and an isolation of >18 dB between the two output ports at 110 GHz. Its physical size is 330×90 μm^2.

The 1-to-4 distribution network is based on G-CPW transmission line and two-stage Wilkinson power dividers. The G-CPW meanders between the phased array unit elements so as to provide an equiphase feed to the 4 unit cells. Its simulated insertion loss is 12.7 dB at 110 GHz (including the 6 dB power division), and all unit elements are fed within ±5° phase difference.



(a)



(b)

Figure 2.6: (a) Schematic of the 4-stage common source amplifier (row amplifier). (b) Layout of the row amplifier breakout.

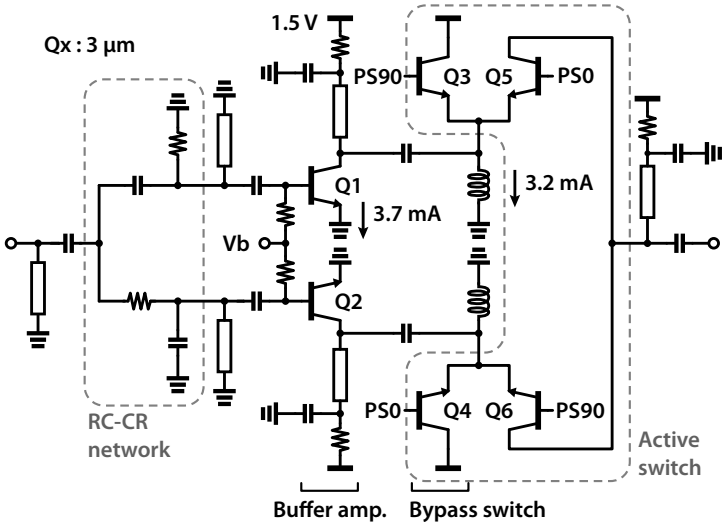
2.2.4 Phased Array Unit Element

The 90° phase shifter is connected to the 1:4 distribution network and has single-ended input and output ports (Fig. 2.7(a)). An RC-CR network is used to generate the $-90°$ phase difference, and the bottom ground plane underneath the RC-CR network is removed in order to reduce the shunt parasitic capacitance to ground. Each of the two outputs from the RC-CR network is followed by a CS buffer (Q1, Q2), which provides gain and isolation from the active-switching stage (Q3–Q6). The switching stage selects one of two signals depending on the phase state. For a phase state of 0° phase shift, Q5 (and Q4) is on and +45° signal is selected to the output. For the $-90°$ phase state, Q6 (and Q3) is on and $-45°$ signal is selected to the output port. The unselected signal in each case is bypassed by Q3 (or Q4) to AC ground (V_{CC}), and prevents leakage of the unselected signal to the output. This improves the gain and phase response of the 90° phase shifter.

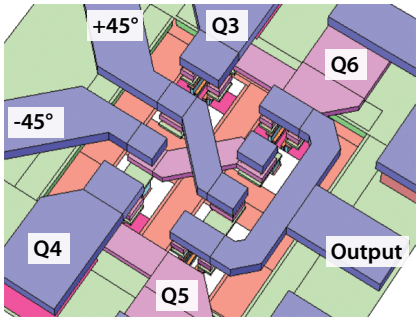
Fig. 2.8 presents a comparison of the gain difference and phase error for the 90° phase shifter as different configurations are used. The gain and phase error are substantially better with the use of bypass switches. The buffer stage has no effect on the gain and phase error when the bypass stages are used, but it provides an additional ~3 dB gain at 110 GHz. After full EM simulation (Fig. 2.7(b)), the 90° phase shifter has a simulated phase error of $10\pm3°$ from 90–118 GHz, an insertion gain of -4.7 dB with <1 dB gain difference from 102–120 GHz, and an OP_{1dB} of -5.5 dBm. The current consumption is 13.8 mA (P_{DC}=20.7 mW).

A passive balun is inserted between the 90° phase shifter and the 180° phase shifter (Fig. 2.9(a)). The primary inductor is done in M6 and the secondary inductor in M5, and they are stacked for vertical magnetic coupling. A custom metal-oxide-metal (in M4–M6) capacitors are used at the input and the output for impedance matching. The simulated insertion loss is 1.6 dB, and the retrun loss is <-10 dB at 90–140 GHz. The gain and phase imbalance is <0.9 dB and $<4°$, respectively, at 90–120 GHz.

A differential buffer amplifier is then placed after the passive balun to improve the gain and phase balance. A 45 Ω resistor is used as common-mode source degeneration and resulting in common-mode gain of -5 dB at 110 GHz. The differential buffer amplifier has a simulated gain of 2.4 dB at 110 GHz with an OP_{1dB} of -2.8 dBm. The



(a)



(b)

Figure 2.7: (a) Schematic of the 90° active phase shifter and (b) EM modeling of the active switch layout.

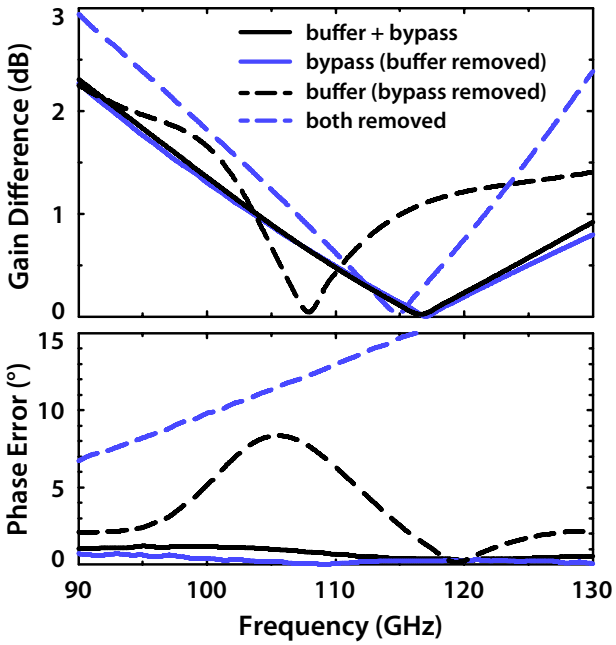


Figure 2.8: Simulated gain difference and phase error for different configurations of the 90° active phase shifter.

gain and phase imbalance after the buffer amplifier is <0.25 dB and <5° at 90–120 GHz.

Fig. 2.10 shows the differential 180° phase shifter based on a separated Gilbert-cell approach. This approach allows a low supply voltage of 1.5 V which is common for all circuit blocks. The first stage (Q1–Q2) uses resistive degeneration in order to further improve the common-mode rejection. The active switching stage (Q3–Q6) crosses the signal at the output, resulting in the 180° phase shift. All interconnections in the circuit are modeled with EM simulations and are accounted in the top level circuit simulation. The 180° phase shifter has a simulated gain of 2.5 dB with 3-dB bandwidth of 96–135 GHz. The gain and phase error between the two states are <0.7 dB and <5° up to 120 GHz, respectively. It consumes 20 mA from 1.5 V and occupies an area of 310×380 μm^2.

In order to drive the differential on-chip antenna feed, the output amplifier is designed as a pseudo-differential amplifier. Fig. 2.11 shows the schematic diagram of its single-ended half circuit which is a 5-stage common-source amplifier. The design approach is similar to the row amplifier, and the simulated gain is 15 dB with a −3 dB

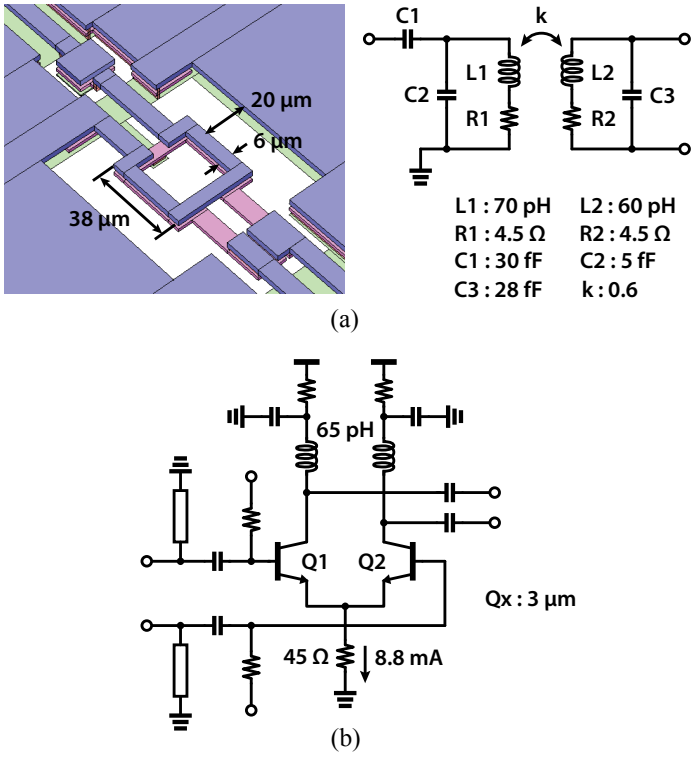


Figure 2.9: (a) EM-modeling of the passive balun and its simple circuit model. (b) Schematic of the differential buffer amplifier following the balun.

bandwidth of 100–123 GHz. The half-circuit OP_{1dB} and P_{sat} are -2 dBm and +2 dBm, respectively, while consuming 22 mA from a 1.5 V supply. The layout is staggered in order to adapt to the wide spacing of the differential antenna feed, and the differential amplifier occupies an area of 760×380 µm^2. Its differential output impedance is $94+j3$ Ω which matches well with the antenna input impedance.

2.2.5 High-Efficiency Differential Dipole Antenna

A dipole antenna with a differential feed is chosen for the following reasons: 1) it occupies less area than a microstrip antenna, and 2) differential signaling allows for a simple implementation of the 180° phase shifter. The smaller area of the differential dipole antenna as compared to a microstrip antenna is critical for this work since it determines the available area for the active circuits in a unit cell ($0.5\lambda_0 \times 0.5\lambda_0$). The electromagnetically (EM)-coupled dipole antenna is patterned using 7000 Å of sputtered

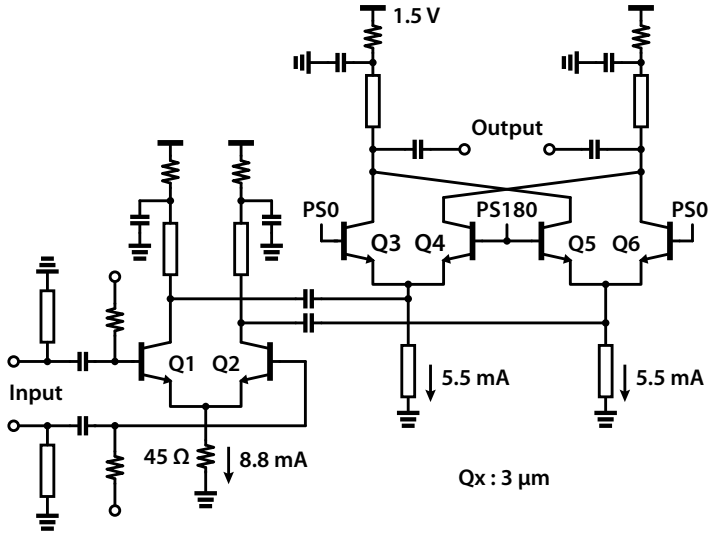


Figure 2.10: Schematic of the 180° active phase shifter.

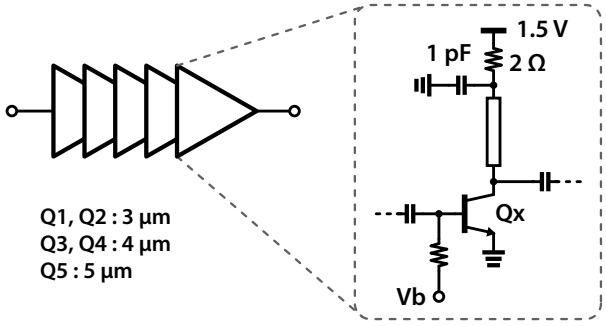


Figure 2.11: Schematic of the 5-stage common source amplifier which drives the on-chip antenna (2 units are used for a differential feed).

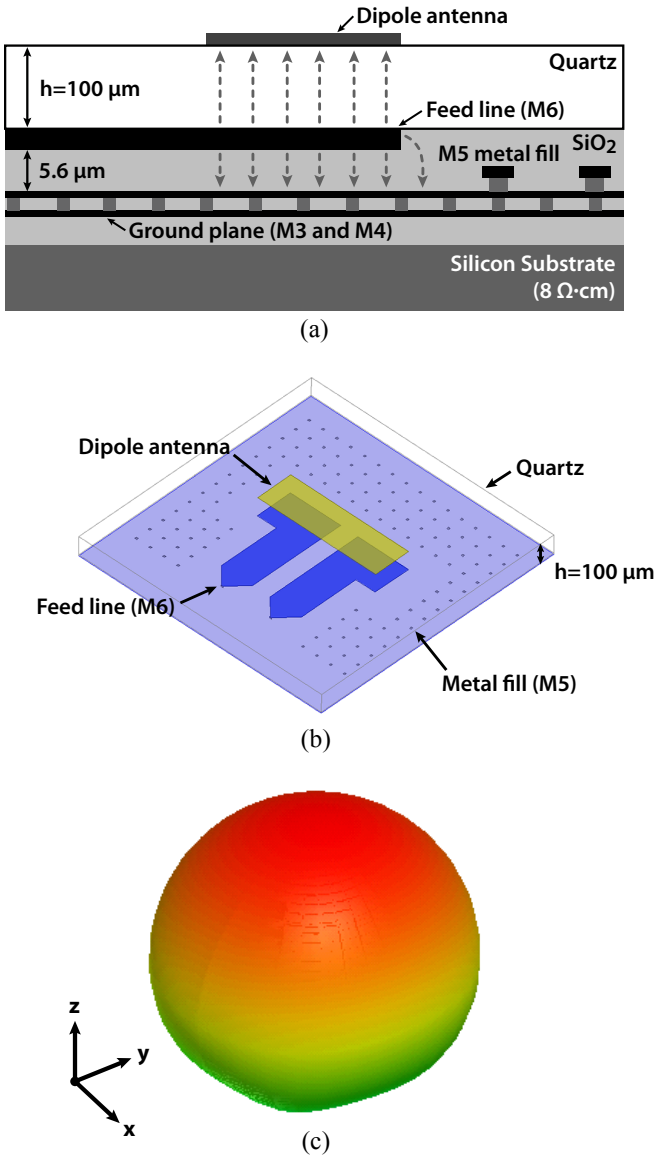


Figure 2.12: Structure of EM-coupled dipole antenna (680 µm×200 µm): (a) cross-section view and (b) 3-D view. An exclusion area of 880×740 µm^2 is placed around the antenna. (c) The simulated 3-D pattern of the dipole antenna on a finite ground plane.

gold on an additional quartz wafer on top of the silicon chip (Fig. 2.12). This novel antenna with a quartz superstrate allows for high efficiency designs at 60–200 GHz and has been presented before for single-ended and differential structures [34, 36, 53, 54, 55]. The dipole feed is placed on the top metal layer (M6), and the ground plane is implemented with combined M3 and M4 layers. The EM-coupling eliminates the use of a direct metal-via feed (and its associated parasitic inductance) from the silicon chip to the radiating structure, and lowers the cost of the entire package.

The thickness of the quartz layer ($\varepsilon_r = 3.8$) is 100 μm, which is found to be optimal at 110 GHz based on HFSS simulations (see [53] and [55] for details on the quartz thickness optimization of such antennas). The M3 and M4 layers also act as a ground plane for the radiating dipole antenna (107.4 μm away), and cover all the area dedicated to the antenna structure in a complementary fashion in order to observe the required density rules for fabrication. This on-chip ground plane isolates the radiated signal from the lossy (8 Ω-cm) silicon substrate, thus resulting in a unidirectional pattern above the silicon and improved antenna efficiency.

In the 4×4 array, the entire M3/M4 on-chip metalization acts as a ground plane for the antenna array, but the results of the single dipole sets a guideline for the dedicated exclusion area around the antenna structure. Also, the metal-fill structures under the feedline degrade the antenna performance, and therefore the M5 metal-fill is placed 50 μm from the M6 feedline. Also, transistors and RF signal lines are not used underneath the antenna in order to avoid any potential coupling. Using HFSS, the antenna area is determined to be 880×740 μm^2 ($0.32\lambda_0 \times 0.27\lambda_0$), which is ~35% of the unit element area. The dipole antenna dimensions are 680×200 μm^2, which is the size of the feed line on M6 (Fig. 2.12(b) and Fig. 2.15).

The simulated differential dipole antenna impedance at the apex feed is $1 - j2.5$ Ω due to the proximity of the M3/M4 ground plane to M6 feed (5.6 μm). Therefore, an impedance transformer consisting of a 180 μm wide and 330 μm long microstrip line ($Z_{odd} = 4.6$ Ω, $\theta_{line} = 103°$ at 110 GHz) is connected to each side of the dipole, and transforms the dipole impedance to a differential $81 - j11$ Ω at the amplifier output port. The efficiency is 45±2% with a directivity of 6.0 dBi and gain of 2.7 dBi at 110 GHz. The differential S_{11} is <-10 dB at 106–114 GHz (referenced to 100 Ω), with a

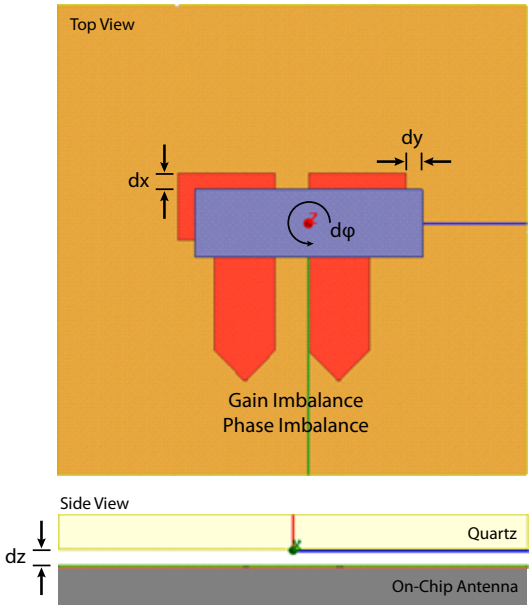


Figure 2.13: Misalignments and imbalances which might affect antenna performance. Possible misalignments include translational (dx, dy), vertical (dz), and rotational (dϕ) displacement. Gain and phase imbalances at the antenna excitation are also considered in simulation.

-3 dB gain bandwidth of 108–114 GHz (Fig. 2.16). The half-power beamwidth is 86°. This antenna results in high efficiency and wide bandwidth when compared to antennas built on a standard RFIC backends (typical efficiency of 5–10%) [56, 57, 58].

The EM-coupled dipole antennas on the quartz superstrate are aligned and attached to the silicon RFIC using a small dot of epoxy at the edge of the 4x4 array chip. Fig. 2.13 shows various possible misalignments between antenna and phased array chip, as well as gain/phase imbalances at the antenna excitation. 3-D EM simulation is used to investigate the effect of misalignments and imbalances on the antenna performance. Due to the fringing fields, the EM-coupled antenna is insensitive to translational (x- and y-directions) misalignments, which results in only additional 0.3 dB gain loss for a $\pm$30 µm misaligment (Fig. 2.14). However, the peak frequency of the antenna changes with the air-gap between phased array IC and quartz superstrate (z-direction), resulting in ~2.0 GHz frequency shift with 2 µm air-gap. The effect of rotational misalignment and gain/phase imbalance at the excitation on the antenna gain is also negligible (not shown).

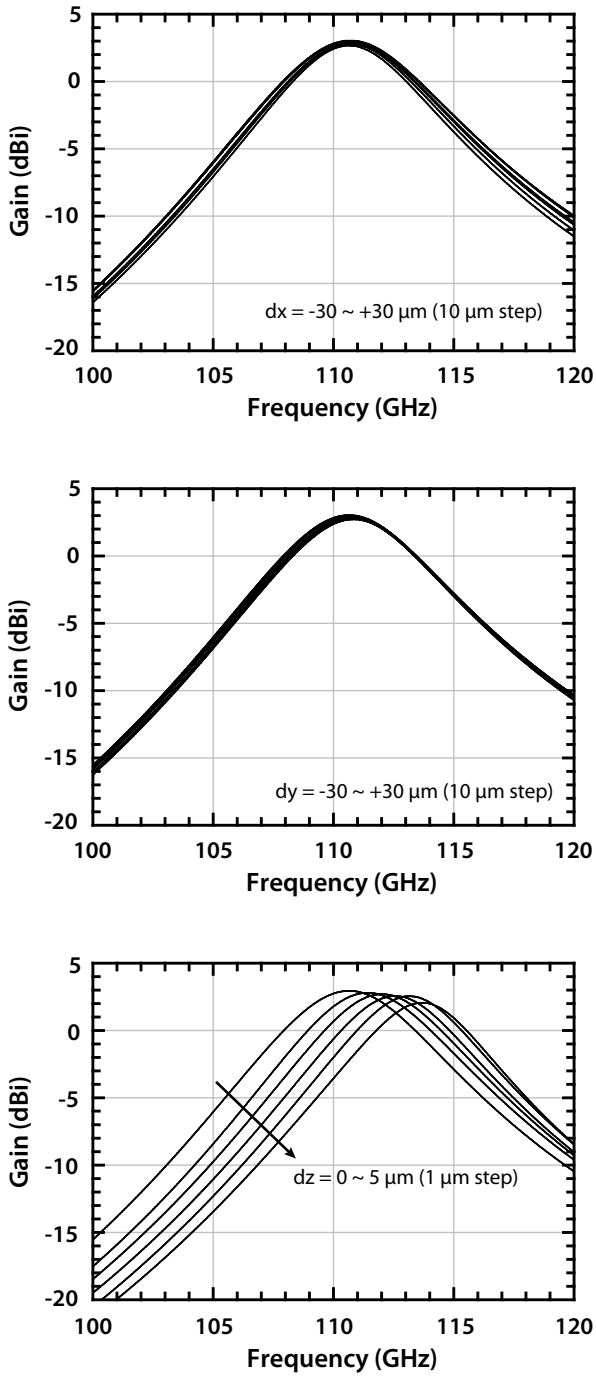


Figure 2.14: Simulated antenna gain under misalignments in x-, y-, and z- directions.

The simulated results show the EM-coupled antennas are suitable for large wafer-scale phased arrays given a careful attachment is achieved to silicon IC.

2.2.6 Digital Control and Chip Integration

Each unit-element has a 2-bit register which stores the phase state. The register is composed of level-triggered D-flip-flops, and the enable clock for the register is controlled by 4-to-16 address decoder. Thus, 7-bit digital interface (4-bit address, 2-bit phase, and 1-bit for control enable) is required to control the entire phased array. The control logic is designed with 0.18-μm CMOS technology, and the delay of a D-flip-flop is ~3 ns. The digital control signal is distributed using M1 and M2 metal layers, and the longest distribution line is about 10 mm which has estimated RC delay of 145 ps. Thus, the delay of the control signal is dominated by the logic gates, and based on the number of logic stages it can support up to 50 MHz of control signals.

A high density MIM capacitor in series with a 3 Ω resistor results in a low-Q DC bypass network and is used in all available area on the chip for improved stability. The total DC decoupling capacitance is ~95 pF in a unit element and ~1.6 nF for the entire chip. Current-mirror biasing is used for most of the circuit blocks, and they are tied in groups and connected to the bias control pin. The M3 and M5 layers are used for V_{CC} as much as possible in order to minimize the DC voltage drop in V_{CC} (IR drop).

Fig. 2.15 presents a detailed microphotograph of the fabricated 4×4 array. Layout arrangement of the circuit components is chosen to achieve efficient use of area with the equi-phase distribution network. An RF GSG pad is located at the west side for the external input, and DC pads including V_{CC} and GND are distributed as evenly as possible at the other three sides. The DC pad pitch is either 100 μm or 200 μm, and pads are allocated to be compatible with available DC probes. A dual-diode ESD protection cells are used for all DC pads, and foundry-provided power clamp circuit is also used between V_{CC} and GND. The fabricated 4×4 array occupies 6.5×6.0 mm^2 area, and simulated power consumption is 1425 mA from 1.5 V supply.

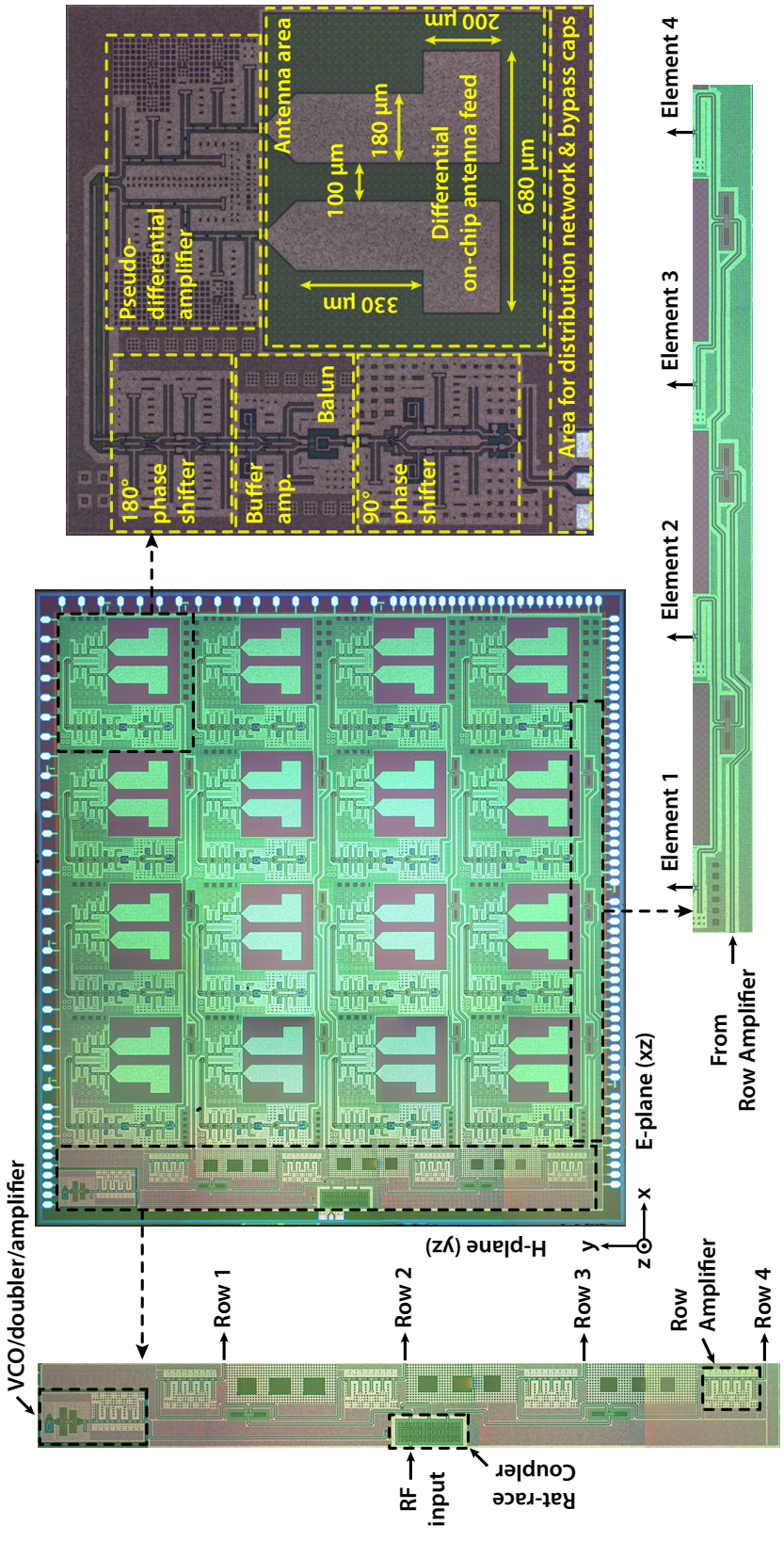


Figure 2.15: Photograph of the 4×4 phased array transmitter (6.5×6.0 mm^2) and its distribution network. A unit element (1.365×1.365 mm^2) is also shown.

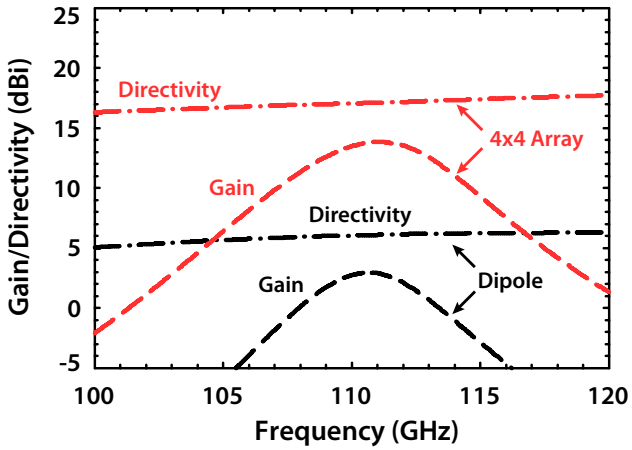


Figure 2.16: Simulated directivity and gain of a single antenna and the 4×4 array antenna.

2.2.7 4×4 Phased-Array Design

The 4×4 array is fabricated with $0.5\lambda_0$ spacing at 110 GHz (1365 µm) in both E-plane and H-plane directions (Fig. 2.15 and Fig. 2.26). The entire antenna array and feedlines are simulated using HFSS (without the front-end electronics), and show a directivity of 17.0 dBi and antenna gain of 13.5 dBi at 110 GHz and 0° scan angle, respectively, demonstrating an antenna efficiency of 45% (Fig. 2.16). The simulated mutual coupling between the antenna elements is <-20 dB in the E- and H-plane planes even for the nearest elements (Fig. 2.17(a)) due to the ground plane (M3/M4) proximity. The effect of the mutual coupling on the input impedance of all 16 elements is negligible as seen in Fig. 2.17(b).

Phased arrays can suffer from grating lobes or scan blindness if placed on a relatively high-ε_r substrate such as quartz dielectric ($\varepsilon_r = 4.0$). Based on a method proposed in [59], the scan blindness angle θ_{sb} can be calculated using:

$$\theta_{sb} = \arcsin\left(\left|\frac{\beta_{sw}}{k_0} - \frac{1}{dx/\lambda_0}\right|\right) \tag{2.1}$$

where β_{sw} is the surface-wave propagation constant for the TM_0 mode in the grounded quartz substrate (h = 107.4 µm), $k_0 = 2\pi/\lambda_0$ is the free-space wavenumber, and dx is element spacing in the x-direction. It is seen that the 4×4 array can scan to ±80° before triggering a dominant substrate mode in the quartz dielectric. Fig. 2.18 presents

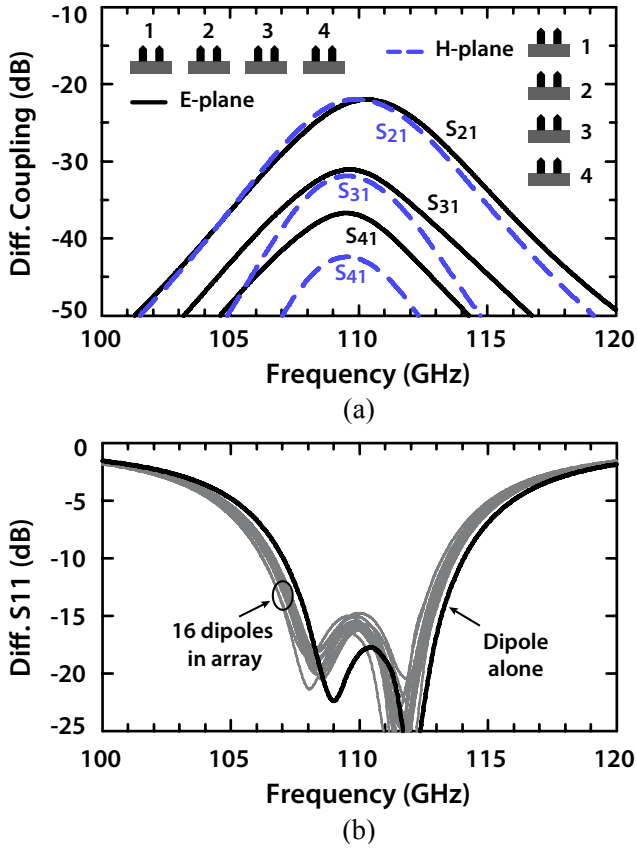


Figure 2.17: (a) Simulated mutual coupling in E-plane direction and H-plane direction in the 4×4 antenna array. (b) Input return loss of each element in the array and an isolated dipole antenna.

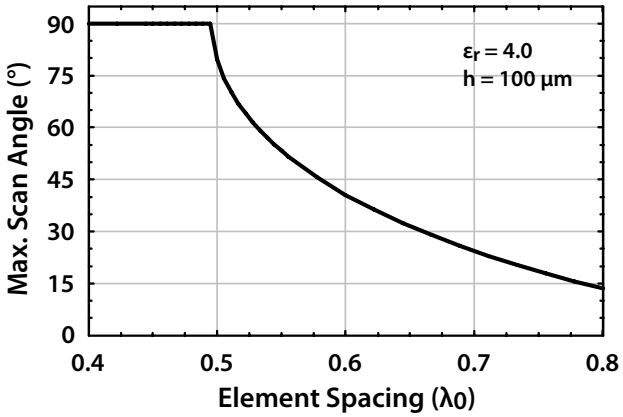


Figure 2.18: Maximum scan angle of a phased array in a dielectric substrate with $\varepsilon_r = 4.0$ and the thickness of 100 µm.

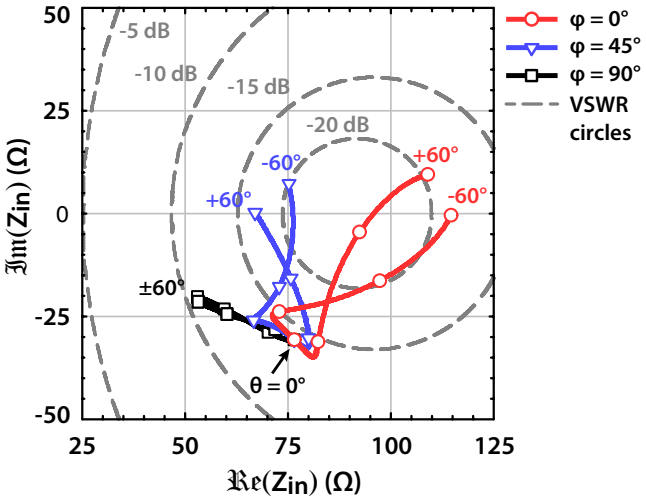


Figure 2.19: Simulated active input impedance of an inner element ($m = n = 2$) for three different principal axes: $\phi = 0°$ (E-plane), $\phi = 45°$, and $\phi = 90°$ (H-plane). Scan angle (θ) varies from $-60°$ to $+60°$, and markers are placed every 20°.

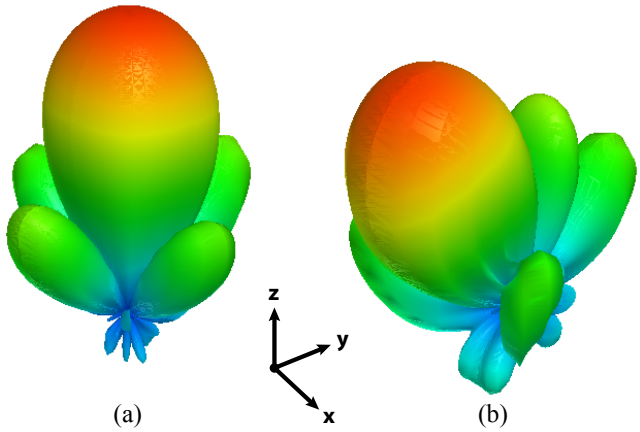


Figure 2.20: Simulated 3-D patterns of the 4×4 antenna array for different H-plane beam-steering positions: (a) θ = 0° with (0°, 0°, 0°, 0°), (b) θ = 30° (0°, −90°, −180°, −270°)

the maximum achievable scan angles for ε_r = 4 and different spacing. The scan angle reduces to ±54° for $dx = 0.55\lambda_0$.

Another important aspect of phased arrays is the input impedance of an antenna element vs. scan angle (typically called active impedance or driving point impedance)[19]. For a 4×4 array in an (m,n) grid with m=1–4 and n=1–4, the input impedance of an antenna at $(m=1,n=1)$ and a scan angle of (θ, ϕ) can be obtained using the Z-parameter matrix as:

$$Z_{in,11} = \frac{V_{11}}{I_{11}} = Z_{11} + Z_{21,11}\frac{I_{21}}{I_{11}} + Z_{31,11}\frac{I_{31}}{I_{11}} + \ldots$$

$$I_{mn} = |I_{mn}|e^{-jk_0(mdx\sin\theta\cos\phi + ndy\sin\theta\sin\phi)}$$

where $Z_{in,11}$ is the active impedance of the driven element, Z_{11} is the self-impedance of the driven element, $Z_{mn,11}$ are the mutual impedance between the driven element and one of the other elements, and I_{mn} is an excitation current at the (m,n) position. In this work, $dx = dy = 0.5\lambda_0$, and $|I_{mn}/I_{11}| = 1$ for a uniformly driven array. Since $Z_{mn,pq}$ varies with antenna spacing, and the excitation current phase varies with scan angle, the active impedance is different for every scan angle. Fig. 2.19 presents the calculated antenna impedance for element $(2,2)$ in the 4×4 array as the array is scanned from −60° to +60° in the E-, H-, and 45° planes. The active impedance does not vary much vs. scan angle because the mutual coupling components, $Z_{mn,pq}$, are quite low. The

active impedance reflection coefficient is <-15 dB (referenced to 90 Ω) over all scan angles.

Fig. 2.20 presents the simulated 3-D pattern of the array under two different scan conditions showing beam-forming and beam-steering capability of the wafer-scale phased array. The first sidelobe level is <-13 dB in the H-plane and <-12 dB in the E-plane, and the far sidelobes are <-25 dB at 0° scanning. Some backside radation is present due to the finite size of the ground plane in the simulation setup.

2.2.8 Electronic System Gain, EIRP, and Array Gain

The 4×4 phased array functional blocks are shown in Fig. 2.21 together with the small-signal gain (or insertion loss) of each block. The simulated system electronic gain, G_s, is defined as the available power at a *single* dipole feed divided by the input power and is 2.3 dB at 110 GHz. This definition of G_s is compatible with a 2-port probe measurement when port 2 is located at the antenna feed. The array gain, G_{array} is defined as the effective isotropic radiated power (EIRP = $P_T G_T$) divided by the input power in the small-signal regime, and is:

$$G_{array} = \frac{\text{EIRP}}{P_{in}} = G_s + 10\log N + G_T \text{ (dB)} \tag{2.2}$$

where N is the number of elements (N=16) and G_T is the 4×4 antenna array gain ($G_T =$ 13.5 dB at $\theta = 0°$). Fig. 2.22 presents the system gain (G_s), the array gain (G_{array}), and the unit element gain ($G_{element}$, see Fig. 2.4(d) to the dipole feed). G_s has almost same frequency response as $G_{element}$ due to the wideband distribution network, but G_{array} has a narrower frequency response due to the dipole antenna bandwidth. The simulated G_{array} is 27.7 dB at 110 GHz with a 3-dB bandwidth of 107–113 GHz.

The absolute EIRP of the 4×4 array can also be calculated using a similar formula:

$$\text{EIRP} = P_{avs} + 10\log N + G_T \text{ (dBm)} \tag{2.3}$$

where P_{avs} is the available output power from the unit-element differential amplifier. For an input power of +5 dBm, $P_{avs} = +1$ dBm per channel, and the simulated EIRP is 26.5 dBm at 110 GHz. This is equivalent to a transmitted power of 13.0 dBm (at the dipole

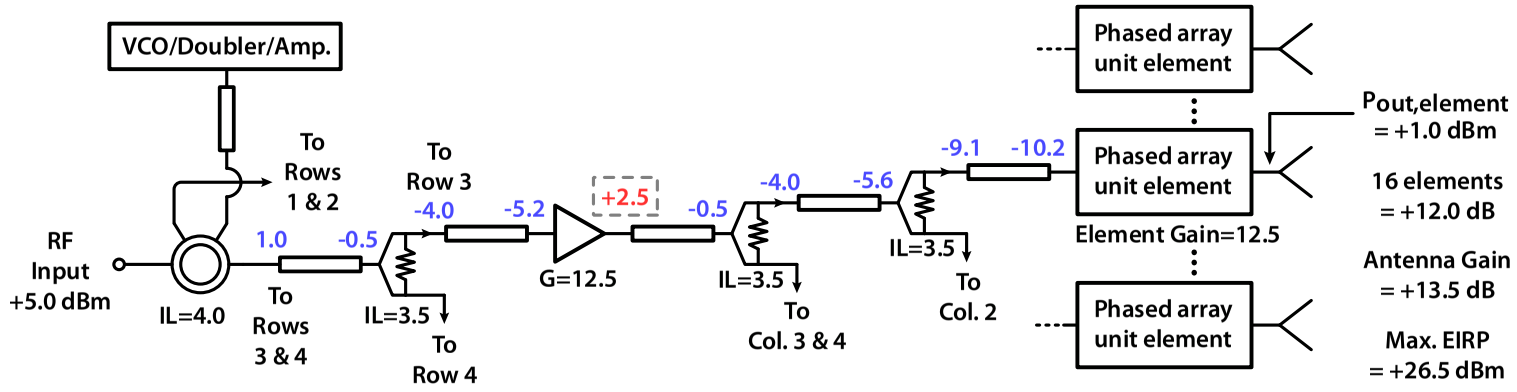


Figure 2.21: Maximum EIRP estimation based on the simulation results. Power level at each point in dBm is denoted with blue number. Maximum EIRP is limited by the row amplifiers (P_{sat}=2.5 dBm shown in dash). Antenna driver amplifier is also in weak compression.

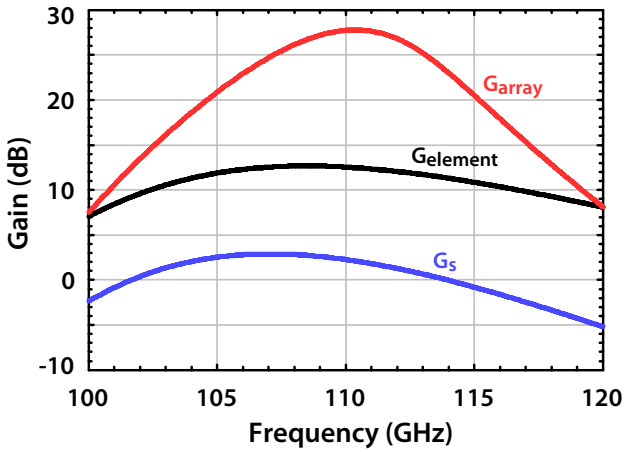


Figure 2.22: Simulated gain of the 4×4 phased array: G_s, $G_{element}$, and G_{array}.

feeds) and a radiated power of 9.5 dBm (in the air).

The EIRP is limited by saturation in the row amplifiers, which results in +1 dBm power at the input of the dipole antenna (and not +4.5 dBm, which is the simulated P_{sat} of the differential antenna amplifiers). Therefore, an EIRP of ~30 dBm at 110 GHz can be expected with a design iteration with improved row amplifiers.

2.3 Measurements

2.3.1 Circuits

The W-band circuit breakouts were tested using two different S-parameter measurement set-ups: one is at 75–110 GHz (WR-10 waveguide band) and the other is at 110–170 GHz (WR-8 waveguide band). The measurement at both frequency bands are taken with an SOLT calibration with a CS-5 calibration substrate [60]. Fig. 2.23 presents the measured S-parameters of back-to-back passive baluns. The back-to-back passive baluns show good agreement with the simulation and have wide input and output matching bandwidth (S_{22} is not shown due to symmetry), and a measured insertion gain of -3.6 dB.

Fig. 2.24(a) presents the measured S-parameters of the row amplifier breakout. The row amplifier has a frequency upshift, but still maintains 13.5 dB gain at 110 GHz with -3 dB bandwidth of 100–133 GHz. The large signal behavior is also characterized

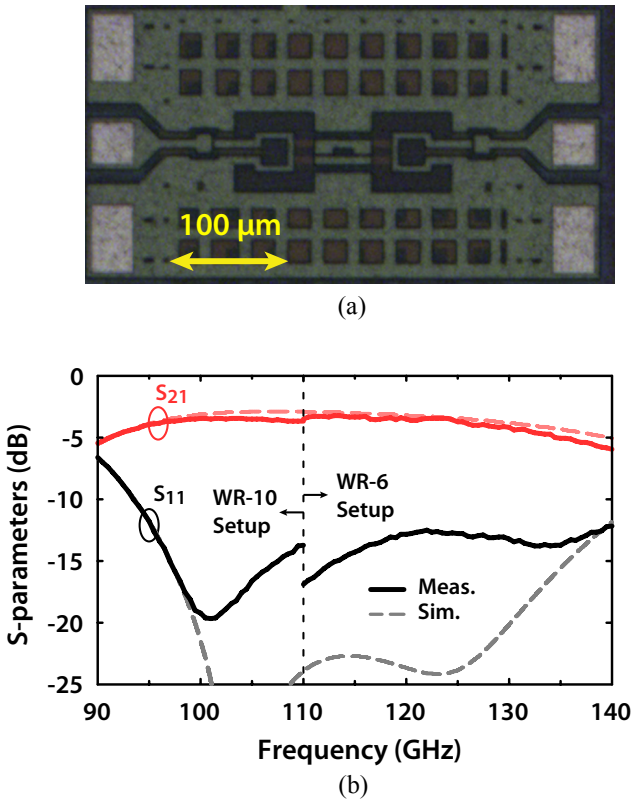


Figure 2.23: (a) Photograph of back-to-back passive baluns and (b) measured S-parameters.

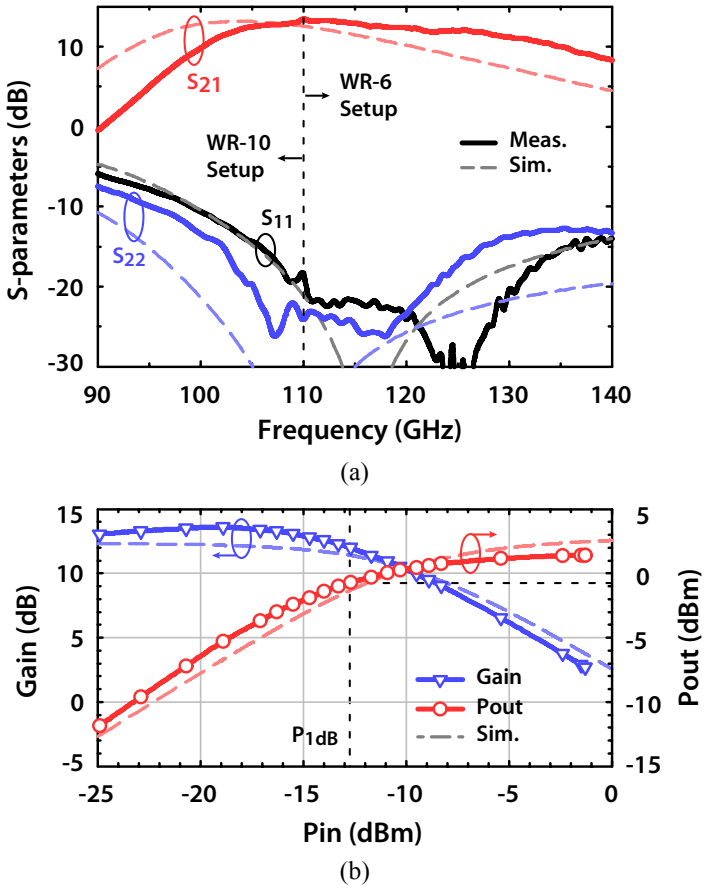


Figure 2.24: Measured and simulated S-parameters of the row amplifier test cell.

at 110 GHz (Fig. 2.24(b)), and its input and output 1-dB compression points are -12.5 dBm and -0.5 dBm, respectively. It has a saturated power (P_{sat}) of 1.5 dBm with -1.5 dBm input. It consumes 28.5 mA from 1.5 V supply.

The measured gain response over frequency of the 90° phase shifter for two different phase states are shown in Fig. 2.25. The insertion gain is -5.2 to -4.5 dB, with a gain difference of <0.5 dB and a phase error of ~5°at 110 GHz. It consumes 18 mA from 1.5V supply. Although a frequency upshift is also observed, measured gain and phase at 110 GHz agree well with the simulation.

The breakouts of VCO and frequency doubler are also measured. The VCO output frequency is 58.4–59.9 GHz with 0–1.5 V control voltage, with an output power of -3 dBm. The measured conversion loss of the frequency doubler is ~8 dB at 110 GHz, and >13 at 120 GHz. The frequency upshift of the VCO turned out to be sub-optimal for the 4×4 array, and the array measurements are therefore obtained using an external signal.

2.3.2 Phased Array

The 4×4 dipole array is fabricated on a 100 μm-thick quartz wafer and is placed on top of the 4×4 phased array IC using small dots of glue at the corners. (Fig. 2.26) The wafer-scale phased array is then placed on a probe station metal chuck and is fed with an external RF signal source using a W-band waveguide GSG probe. The output of the wafer-scale phased array is a plane wave and is received by a rectangular horn antenna which is placed at a far-field distance of R=25 cm ($R_{far-field} > 2D^2/\lambda_0$=22 cm when D = antenna aperture size). RF absorbers are placed around the chip and probe station in order to reduce unwanted reflection and standing waves. The phased array chip is biased with a 31-pin 200 μm-pitch DC probe on the south side and an 11-pin 100 μm-pitch DC probe on the north side. In order to overcome uneven distribution of the DC supply and IR drop across over the chip, the V_{CC} is increased for the pattern and EIRP measurements. The measured power consumption of the 4×4 array is 1.78 A from 1.9 V supply.

Fig. 2.27 presents the measurement set-up. The external RF input is composed of a signal generator, a frequency tripler, and a W-band amplifier so as to maximize

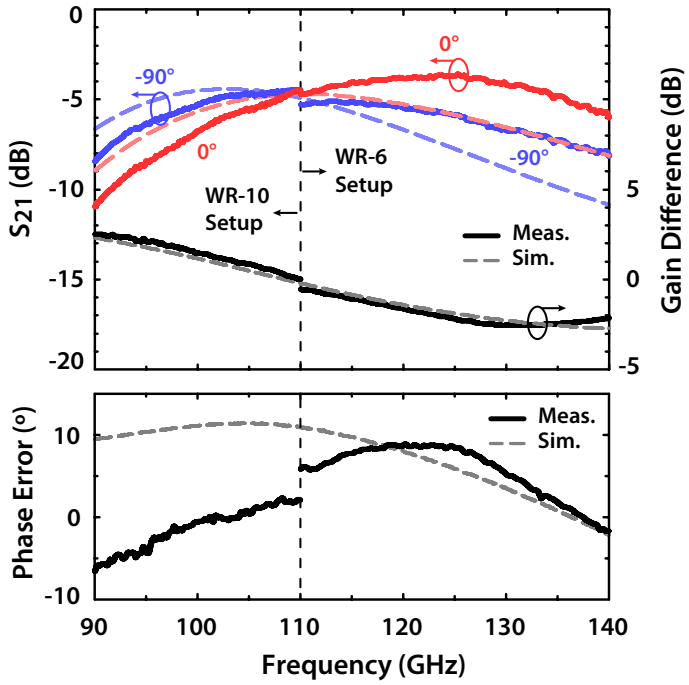


Figure 2.25: Measured and simulated of the 90° phase shifter test cell : (a) S_{21} for both phase states and the associated gain difference and (b) phase error from ideal 90° phase shift.

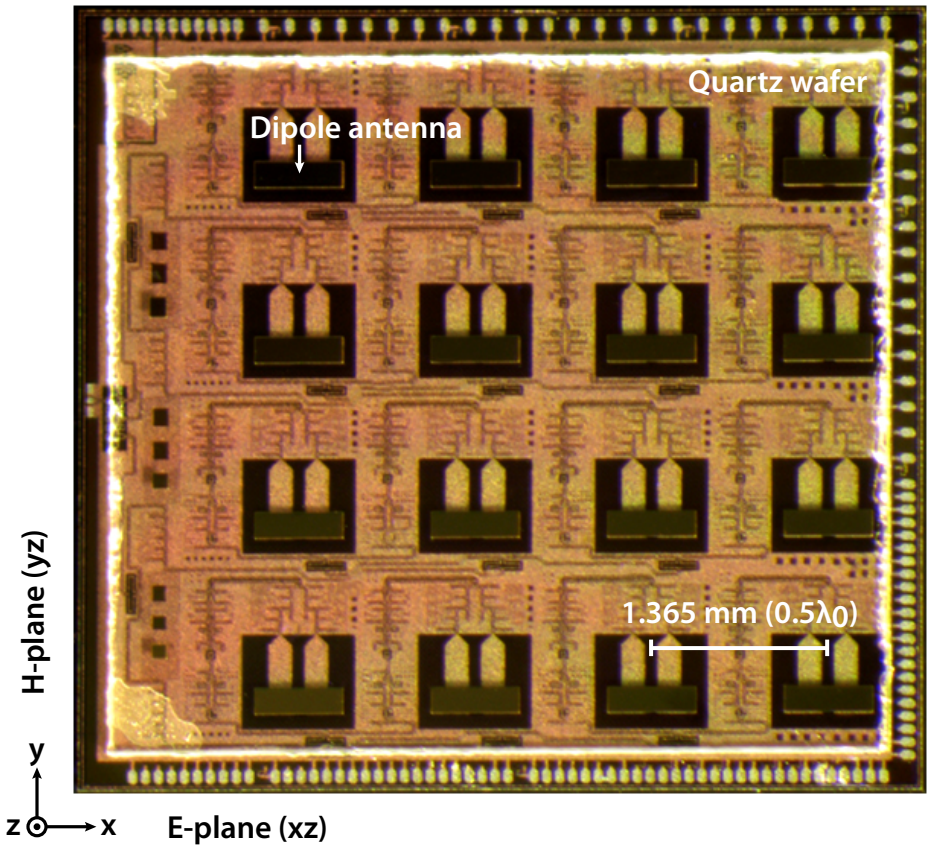


Figure 2.26: Chip photograph of the wafer-scale 4×4 phased array. (6.5×6.0 mm^2)

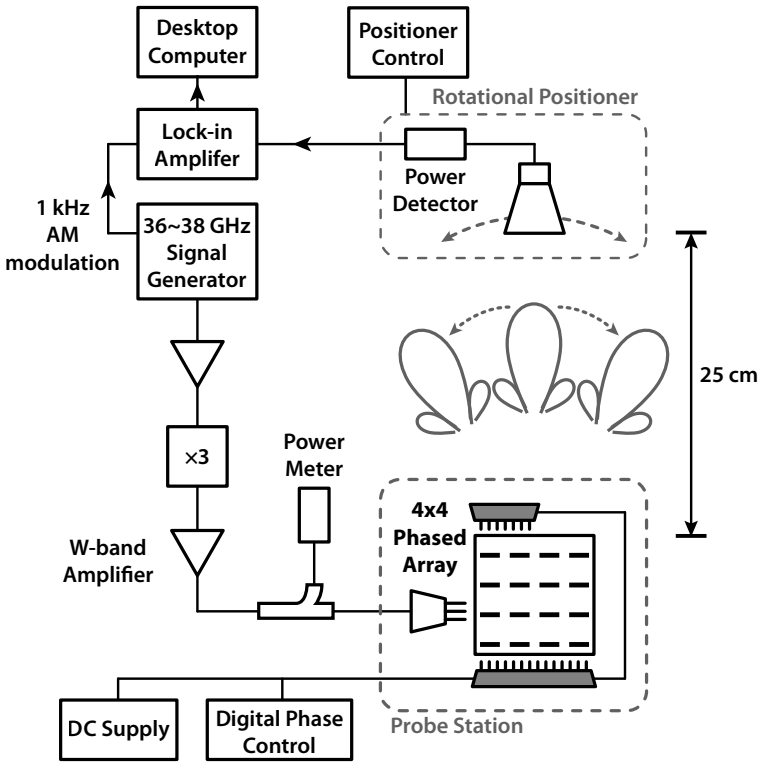


Figure 2.27: Measurement setup of the 4×4 arrays for radiation pattern and EIRP. The power detector is replaced by an absolute power meter for EIRP measurements.

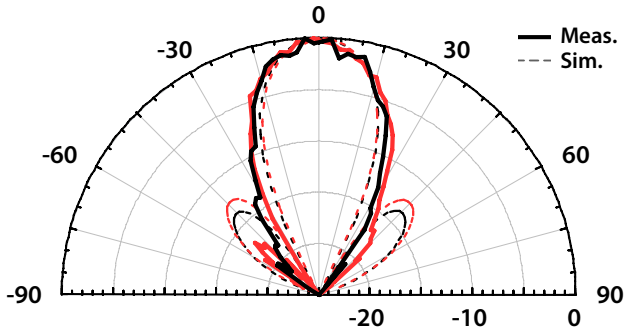


Figure 2.28: Measured and simulated E-plane (black) and H-plane (red) patterns of the 4×4 array.

available power from the source. The RF GSG probe loss (1.5 dB) is taken into account and the input power is referenced to the probe tip. The receiving antenna and power detector are placed on a rotational positioner which scans 0–±60° in the E- and H-planes. The input signal is AM modulated at 1 kHz square-wave with 50% duty cycle, and the power detector detects the envelope of the modulated received signal. The received voltage from the Schottky diode power detector is fed to the SR830 lock-in amplifier[61] and its relative strength is recorded in a desktop computer.

Fig. 2.28 presents the measured patterns in both E- and H-plane at 110 GHz with 0° scan angle. The 3-dB beamwidths of E- and H-plane patterns are 28° and 27°, respectively. The measured pattern and directivity agree well with simulations, and the phased array shows a symmetrical pattern, as designed. The cross polarization for each plane is <-20 dB and is not shown.

The change of row or column phase settings from (0°, 0°, 0°, 0°) to (0°, −90°, −180°, −270°) or (−270°, −180°, −90°, 0°) results in ±30° scan angles in the E- and H-plane, respectively (Fig. 2.29). The measured patterns show clear main beams and deep nulls between sidelobes, and beam-steering capability is demonstrated in both E- and H-planes. The observed distortion in the E-plane patterns is introduced by scattering with the RF GSG probe, and slight a tilt in main beams are also believed to be due to scattering and measurement system misalignment. The patterns are normalized to the maximum level of 0° scan angle, and a gain drop of 2–2.5 dB is seen at ±30° scan angle (0.65 dB due to $\cos(\theta)$, 1.4 dB due to element pattern). No scanning was done in the

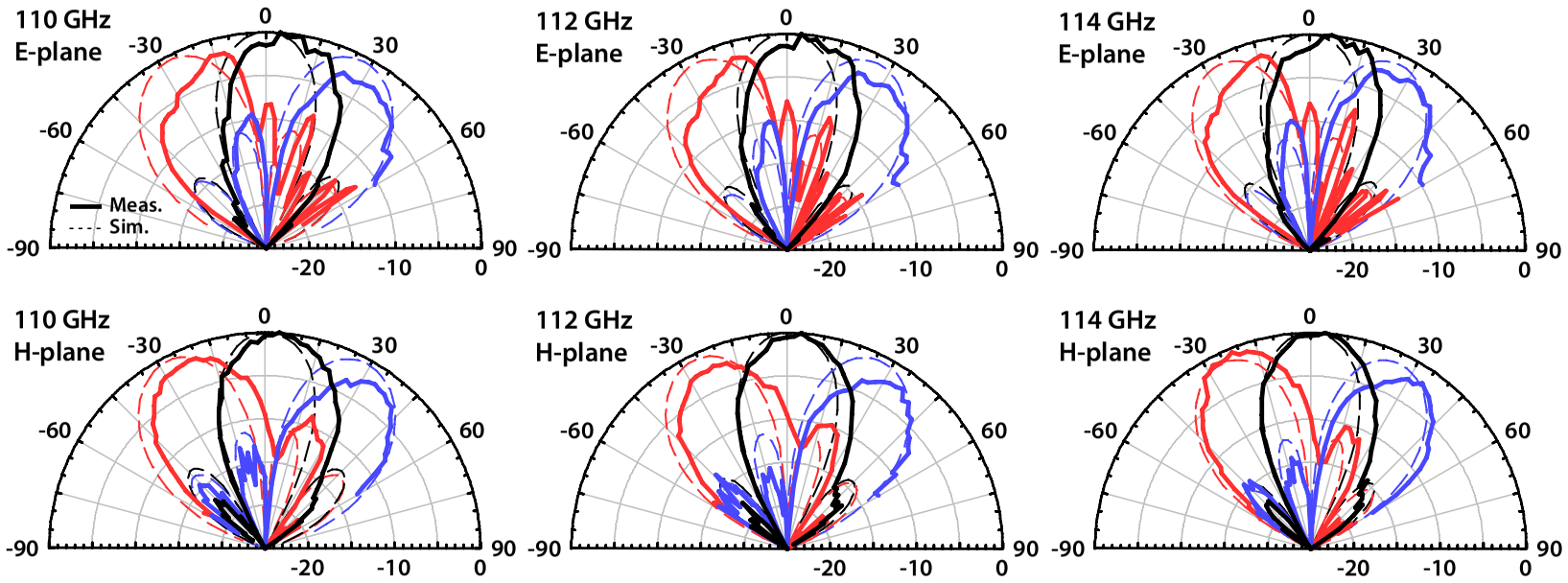


Figure 2.29: Measured (bold) and simulated (dashed) phased array patterns with ±30° beam steering in both E-/H-planes at 110, 112, and 114 GHz. E-plane pattern is distorted due to metal structrue of RF GSG probe.

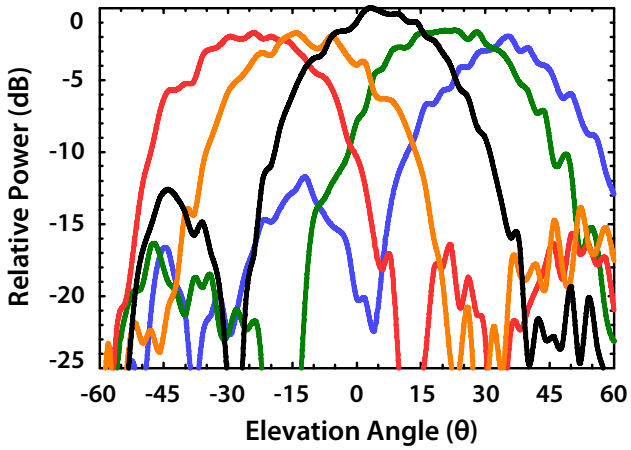


Figure 2.30: Measured radiation patterns with intermediate beam steering for H-plane scanning at 110 GHz.

diagonal plane ($\phi = 45°$) due to the limitation of the available set-up.

The phased array can also be scanned to intermediate angles by setting the row or column phases to (0°, −90°, −90°, −180°; $\theta \simeq 20°$) or (0°, 0°, −90°, −90°; $\theta \simeq 10°$). Fig. 2.30 presents resulting 5 patterns with different scan angles in the H-plane at 110 GHz.

The EIRP is obtained by first measuring the absolute received power from the 4×4 array, and then using the Friis communication link equation:

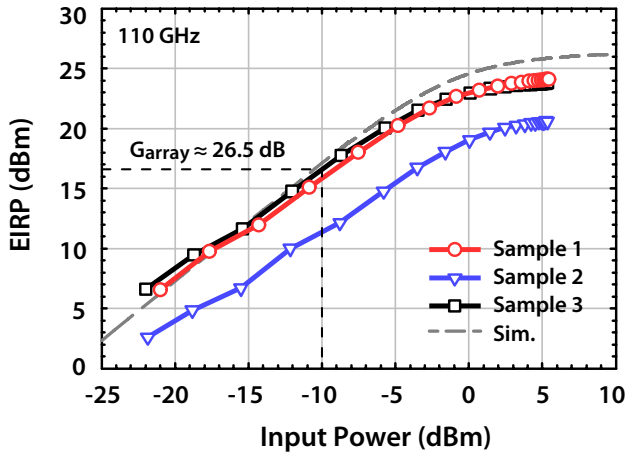
$$P_R = \left(\frac{\lambda_0}{4\pi R}\right)^2 (P_T G_T G_R) \tag{2.4}$$

and

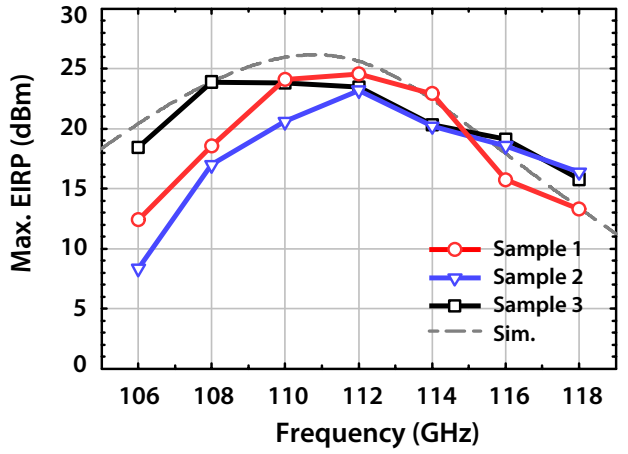
$$\text{EIRP} = P_T G_T = \frac{P_R}{G_R}\left(\frac{4\pi R}{\lambda_0}\right)^2 \tag{2.5}$$

Therefore, due care is taken to independently measure the gain of the receiving horn antenna (G_R=21±0.5 dB at 110 GHz) and calibrated Agilent power sensors (W8486A) are used to measure both input and output power.

Fig. 2.31(a) presents the measured EIRP vs. input power for three different samples at 0° scan angle. The maximum EIRP is 24.0–24.5 dBm at 110–112 GHz for an input power of 5 dBm. The array gain ($G_{array} = \text{EIRP}/P_{in}$) can also be obtained in the small signal regime, which is 26.5±0.5 dB. The maximum EIRP is also measured



(a)



(b)

Figure 2.31: Measured (a) EIRP at 110 GHz for 3 different samples and (b) maximum EIRP at different frequencies.

over frequency at 106–118 GHz (Fig. 2.31(b)), and it shows the repeatability of the measurement. The EIRP at different scan angles can be obtained from the measured patterns, and is 2–2.5 dB lower than the 0° values.

The EIRP can also be expressed as:

$$\text{EIRP} = P_T G_T = \varepsilon P_T D_T = P_{rad} D_T \tag{2.6}$$

where ε is the antenna efficiency and D_T is antenna dirctivity ($G_T = \varepsilon D_T$). The EIRP can therefore be referenced to the radiated power (P_{rad}), with $D_T \simeq 17$ dB. P_T and P_{rad} are calculated from the measured EIRP and are 10.5–11 dBm and 7.0–7.5 dBm, respectively, at 110–112 GHz.

The salient features of the wafer-scale phased array chip are summarized in Table 2.1.

2.4 Conclusion

This paper presented a 16-element wafer-scale phased array with high efficiency on-chip antennas and ±30° scanning capabilities in the E- and H-planes. The wafer-scale array eliminates lossy transitions to external antennas, and can be scaled to 32–64 elements on a single chip with additional row amplifiers. Measurements done on several chips at 108–114 GHz agree well with simulations showing the possibility of this technology for high gain systems. The wafer-scale approach is particularly useful at frequencies above 60 GHz where the chip size is the same as the antenna aperture and high antenna gain can be achieved with 5×5 to 10×10 mm^2 chips, and has the potential to drastically reduce the cost of mm-wave phased arrays. Future work include integrating a complete transceiver instead of the VCO, improving the row amplifiers and increasing the transmit power per element for a higher EIRP. Also, the design can be scaled to 94 GHz for aircraft landing systems, 120 GHz for sensors and communication systems, or 140 GHz for future automotive radars.

2.5 Acknowledgement

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This chapter is mostly a reprint of the material as it appears in:

- W. Shin, B.-H. Ku, O. Inac, Y.-C. Ou and G. M. rebeiz, "A 108–114 GHz 4×4 Wafer-Scale Phased Array Transmitter with High-Efficiency On-Chip Antennas," *IEEE Journal of Solid-State Circuits*, to be appeared in Sept. 2013.

The dissertation author is the primary author of this material.

Table 2.1: Performance Summary

Metric	**Meas.**	**Sim.**
Array Gain (G_{array})	26.5±0.5 dB	27.7 dB
Max. EIRP	24±0.5 dBm	26.5 dBm
Scan Angle	±30° in both E-/H- direction	
3-dB Beamwidth	28±2°	25±1°
Power Consumption	1.78 A @ 1.9 V	1.43 A @ 1.5 V

Chapter 3

D-band Amplifiers and 60 GHz Phase Shifter in 45nm SOI CMOS Technology

3.1 Introduction

A recent success of CMOS technology in RF/microwave frequencies and its applications in the past decade naturally draws strong interest along with high expectation towards its future success in millimeter-wave and terahertz (THz) frequencies. This interest and expectation have been supported by continued advance in CMOS technology, which has reached the minimum feature size in the order of tens of nanometers and the transit frequency (f_t) of hundreds of gigahertz [3]. A silicon-on-insultator (SOI) CMOS technology suggests even more promising performance for the millimeter-wave and terahertz circuits, thanks to its low parasitic capacitance, high isolation, and high speed MOS transistors. Recently, 45nm SOI CMOS technology has been reported to have f_t of 485 GHz [62], providing an excellent opportunity for implementation of millimeter-wave circuits and systems.

Millimeter-wave frequency bands have unique propagation characteristics of high propagation loss and large interaction with various chemical bonds while providing wide absolute bandwidth for the same fraction of the carrier frequency [63, 64]. Em-

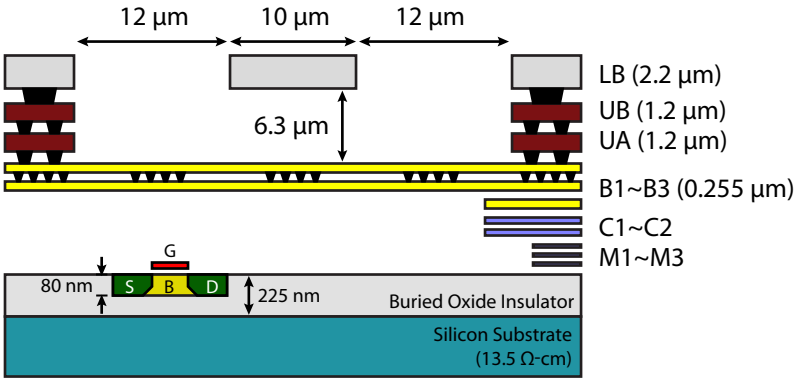


Figure 3.1: Cross-section diagram of IBM 45nm SOI CMOS process (not to scale). Dimensions of on-chip G-CPW transmission line are shown.

bracing these characteristics, possible applications of millimeter-wave systems include short-range point-to-point communication, active or passive imaging, spectroscopy, and short-range radar. 60 GHz frequency band has become an important research topic as unlicensed frequency bands opened up for commercial applications, and D-band (110–170 GHz) frequency range also recently drew much attention as CMOS performance metric became comparable to other semiconductor technologies.

This chapter presents D-band amplifier designs and a 60 GHz phase shifter design in a 45nm SOI CMOS technology, along with some experimental characterization of the technology. The D-band amplifiers with both common-source and cascode topologies are designed, and their performances are evaluated. The quarter-wavelength stubs are used at the drain bias nodes of the common-source amplifier, preventing the effect of unknown impedance at AC ground nodes. The common-source amplifier has 8.7 dB at 147 GHz, and the cascode amplifier results in 6.1 dB at 171 GHz, which is the highest tuned operation frequency to date with a CMOS amplifier. The 60 GHz phase shifter uses a vector modulator with an optimized all-pass I/Q network, resulting in wide-band 4-bit operation with low root-mean-square (RMS) amplitude and phase errors.

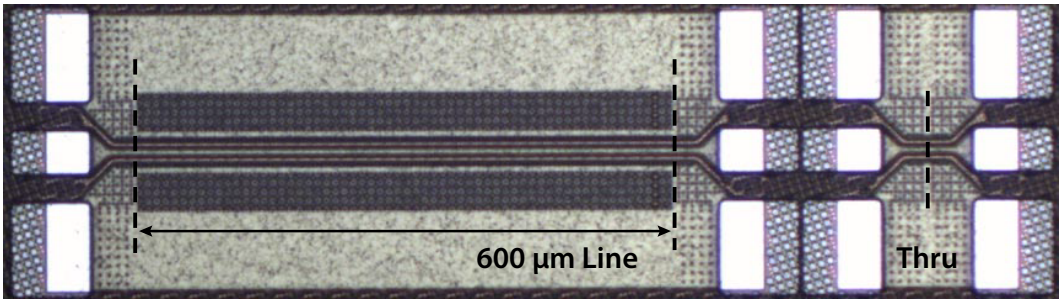
3.2 45nm SOI CMOS Technology Characterization

Process characterization is an important step in millimeter-wave circuit design since circuit performance suffers a lot from parasitic elements and a proven device model is usually not available at high region of millimeter wave frequency bands. In addition to the process characterization from the previous literature [50], a set of test structures including transistors and passive elements are measured directly at G-band frequencies (140–220 GHz) in order to characterize the high-frequency performance of the technology.

Fig. 3.1 presents the cross-section of IBM's 45nm SOI CMOS technology, along with the 50 Ω transmissionline dimension used in the design. Transistor active region is located on the 225 nm-thick buried oxide (BOX) layer which isolates source/drain junction from the silicon substrates. This technology offers 11 metal layers. The top metal layer is an aluminium layer with 2.2 μm thickness (LB), and the other layers are copper. The LB layer serves as a primary signal path and on-chip ground, and it makes on-chip transmission line along with B2/B3 composite layer ground plane. Together with 6.3 μm distance between LB to B3, the width of 10 μm and the gap of 12 μm froms a 50 Ω grounded CPW (G-CPW) transmission line. Transmission line plays an important role in D-band circuit design as interconnects and inductive loads.

A test structure of 600 μm long transmission line is measured with on-chip through standard (Fig. 3.2). S-parameter measurements after SOLT calibration with CS-5 calibration standard for both line and through structures are performed, and a set of matrix operations are performed [48] in order to extract transmission parameters including characeristic impedance (Z_0), effective dielectric constant, attenuation constant (α), and group delay. While Z_0, ε_{eff}, and group delay of the transmission line show small deviation from the simulation, the measured line loss is about twice higher (1.8~2.5 dB/mm at 140~180 GHz) compared to the 3-D EM simulation based on the low frequency electrical properties (1.0~1.1 dB/mm). This high transmission line loss at $>$120 GHz is already reported in the literature [65, 50], but its orgin is not yet clearly identified. The excessive line loss is accounted in the EM simulation with the extra resistivity, and the result is used for the following simulation result.

A foundry-provided interdigitated-finger metal-oxide-metal (MOM) capacitor



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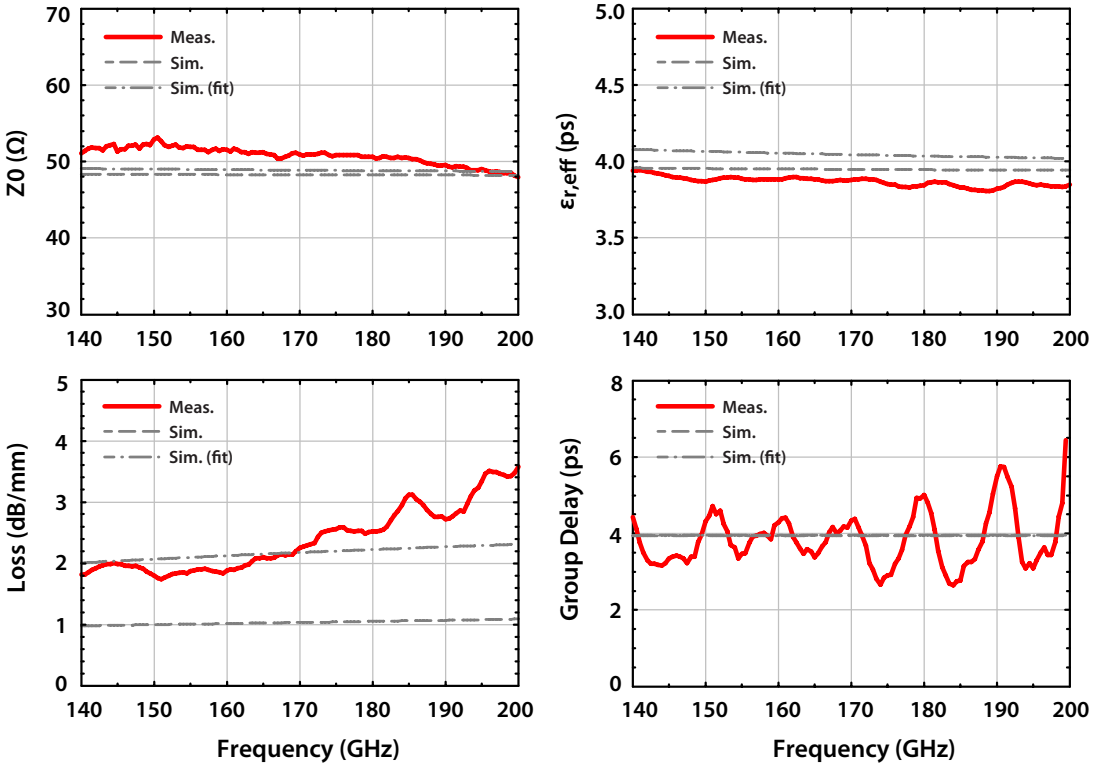
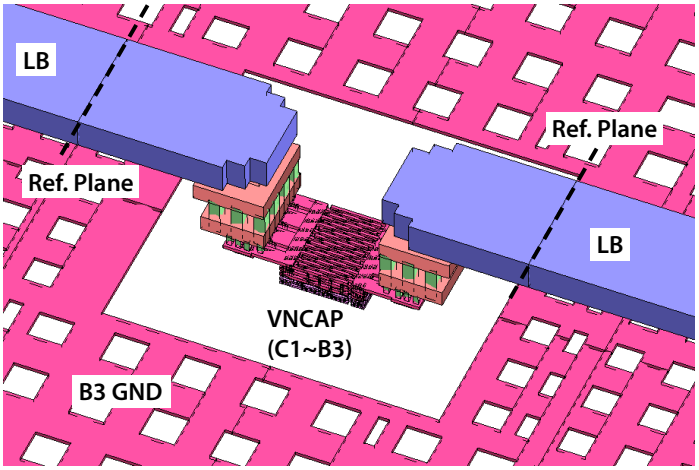


(b)

Figure 3.2: (a) Photograph of measured G-CPW transmission lines (600 µm and through), and (b) extracted t-line parameters from 140–200 GHz along with the simulation results.



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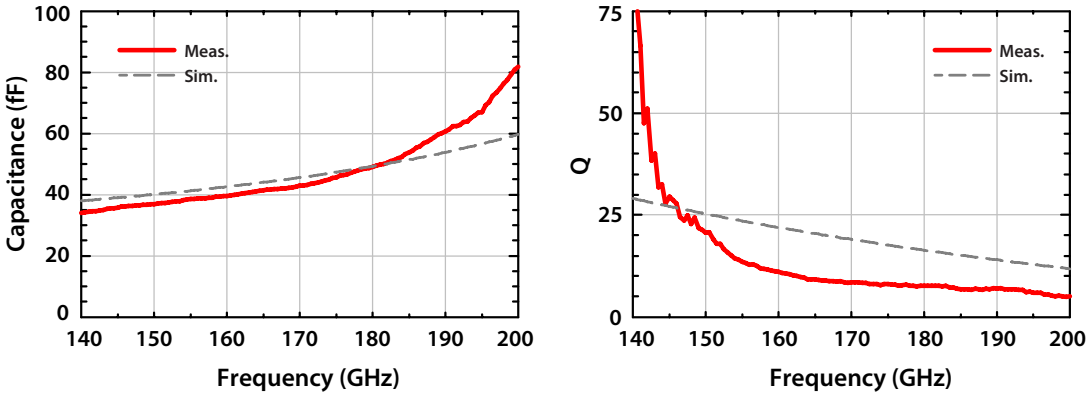
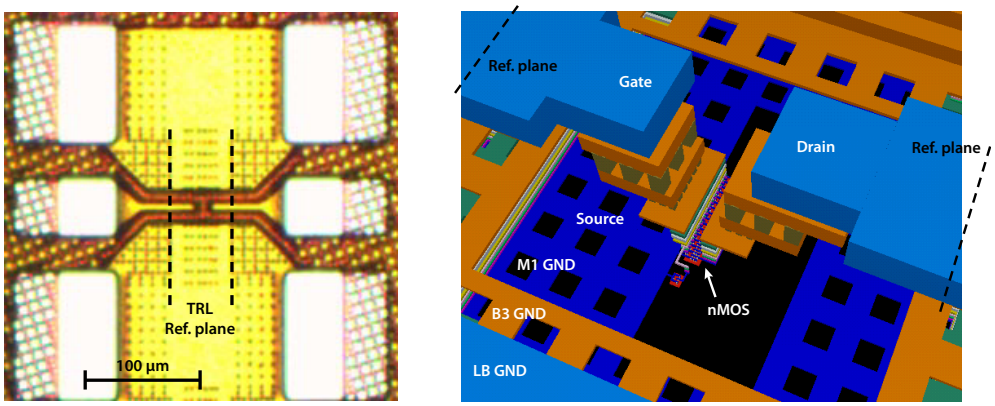


(b)

Figure 3.3: (a) 3-D view of interdigitated finger MOM capacitor test cell and (b) its measured capacitance and quality factor. On-chip TRL calibration brings reference plane to top-level metal layer (LB) and the measure result includes parasitics of metal contact structure.

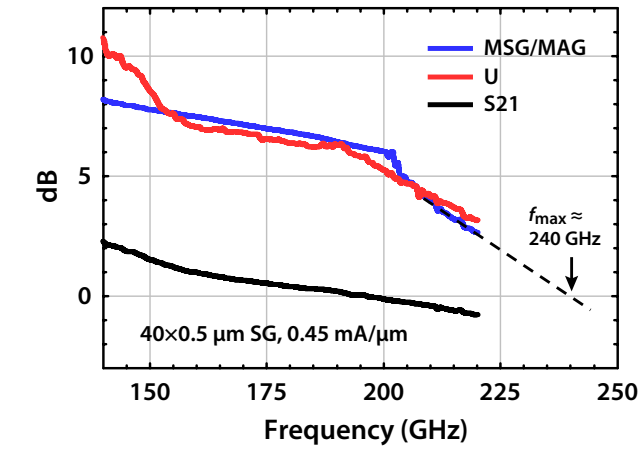


(a) (b)

Figure 3.4: (a) Photograph of MOS test structure, and (b) close-up 3-D view of the MOS test structure.

from C1 to B3 metal layers with the size of 6×6 µm^2 are also directly measured at D-band frequencies (Fig. 3.3). The MOM capacitor test cell is measured with on-chip TRL calibration, and equivalent capacitance and Q-factor is extracted from the measurement. A 3-D view of the MOM capacitor test structure with the TRL reference planes is shown in 3.3 (a). The measurement result inlcludes the via arrays from B3 to LB layer and a certain length of LB connect, since TRL can only bring the reference plane at the level of the line standard. The measurements show acceptable agreement with simulation in terms of capacitance, but the measured Q-factor is roughly 50% of the simulation. The measurement results suggest there exists considerably more loss in the MOM capacitor than what is predicted by simulation with low-frequency model.

A set of nMOS transistors with different configurations are measured with a network analyzer with a millimeter-wave frequency extenders. As in the MOM capacitor structure, the pad parasitics and metal leads in the transistor test structures are de-embedded using the thru-reflect-line (TRL) calibration with customized on-chip standards (Fig. 3.4). Fig. 3.5 (a) presents frequency response of a representative nMOS transistor (a single-gate-contacted (SG) with 20 µm gate width and 0.5 µm width per finger, J_{DS} = 0.45 mA/µm), which shows its S_{21}, maximum stable/available gain (MSG/MAG), and Mason's unilateral gain (U). The nMOS transistor has a positive S_{21} and is conditionally stable up to 200 GHz, and also maintains ~5 dB of Mason's gain at 200 GHz.



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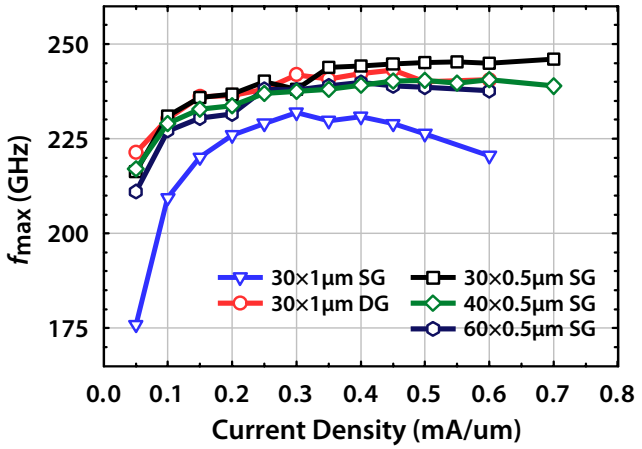


(b)

Figure 3.5: (a) Measured S_{21}, Mason's unilateral gain (U), and maximum stable gain/maximum available gain (MSG/MAG) of a single gate-contacted nMOS transistor. (b) Measured f_{max} of nMOS transistors with different layout configurations.

The maximum oscillation frequency (f_{max}) is extrapolated from the measurement and is 240 GHz in this representative case with some uncertainty. It is proven in the literature that MAG and U are same 0 dB at f_{max}, and U tends to diverge from the ideal low-frequency -20 dB/dec slope at very high frequencies [66], therefore specified f_{max} should be considered as only a rough estimator of the transistor performance.

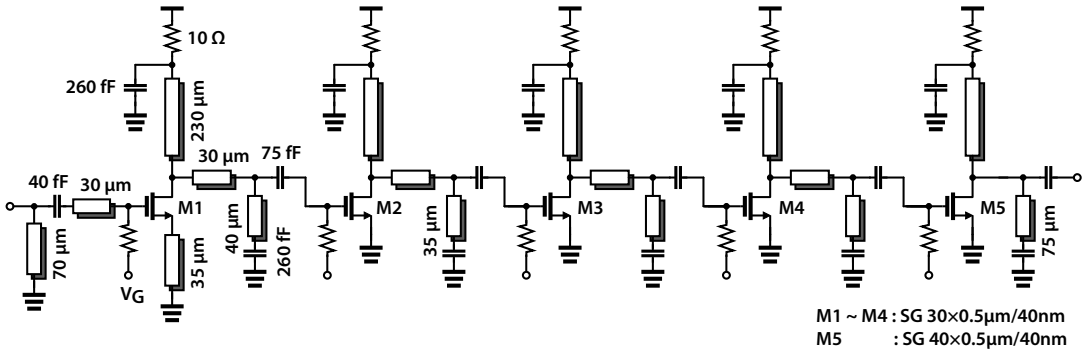
Fig. 3.5 (b) presents the extrapolated f_{max} of different configurations of nMOS transistor including variations of total width, unit finger width, and single or dual gate contacts. As shown in the figure, the single-gate-contacted device with 1 μm unit finger width has significantly low power gain, but other configurations have similar f_{max} of 235–245 GHz with drain current density of 0.2–0.5 mA/μm. The measurement results experimentally verifies that the single gate-contacted device can have comparable performance with the double gate-contated device when the narrow finger width (~0.5 μm) for a device is used.

3.3 D-band amplifiers in 45nm SOI CMOS Technology

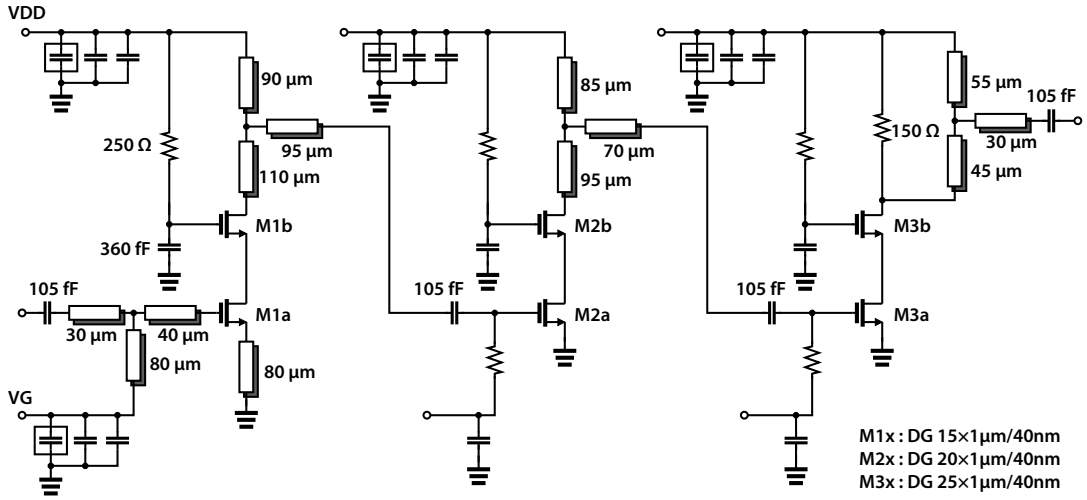
3.3.1 Design

Two D-band amplifiers using different topologies are designed in the IBM 45 nm CMOS SOI process: a 5-stage common-source (CS) amplifier (Fig. 3.6(a)) and a 3-stage cascode amplifier (Fig. 3.6(b)). A floating-body nMOS transistor in the SOI technology provides superior performance to existing bulk CMOS technologies due to its reduced junction capacitances. Both designs utilize floating-body transistors with minimum gate length, and all inductive loads are implemented with 50 Ω G-CPW lines using the top metal layer (12-10-12 μm). Foundry-provided metal-oxide-metal (MOM) interdigitated finger capacitors are extensively used for impedance matching, and accumulated-mode low-Q MOS varactors are used for DC bypass network.

The 5-stage CS amplifier uses 30×0.5 μm transistors, except the last stage at which 40×0.5 μm is used for the increased output power. Transistors with single gate contact (SG) and narrow (0.5 μm) gate width are chosen for the trade-off between gate-to-drain parasitic capacitance and gate resistance per finger. In order to prevent signal coupling through common drain nodes and resulting oscillation, a 10 Ω series resis-



(a)



(b)

Figure 3.6: Schematic diagrams of the D-band (a) 5-stage common source (CS) amplifier and (b) 3-stage cascode amplifier in 45nm SOI CMOS technology.

tor is inserted between V_{DD} node and the transistor drain node. A capacitor bank of ~260 fF forms an in-band AC short, and a $\lambda/4$ transmission line is used to provide high impedance at the drain node. In addition, the quarter-wavelength line makes the amplifier gain less sensitive to unknown variation of impedance at V_{DD} node. Conjugate interstage matching network is designed using transmission line sections and MOM capacitors. The gate of each transistor is biased at 550 mV with 1.4 V drain voltage, resulting in 0.44 mA/μm of drain current density.

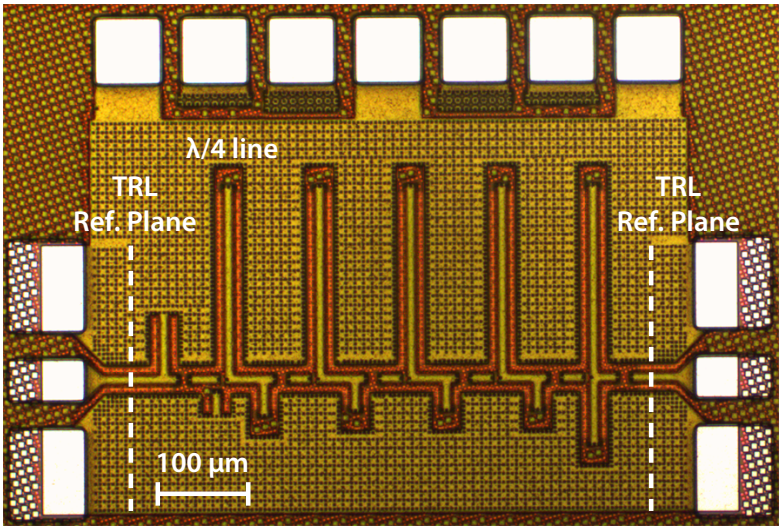
The 3-stage cascode amplifier uses dual gate contact (DG) transistors with 1 μm gate width per finger, and the size at each stage is progressively increased as 15, 20, and 25 μm. Three transmission line sections and a DC block capacitor are used for impedance matching. A 150 Ω de-Q resistor is used at the output matching, and the VDD node at each stage is connected to separate DC probe pads in order to minimize the coupling between VDD nodes. The transistors are also biased with 0.44 mA/μm from 2.0 V supply, which results in the highest performance.

Both designs use inductive source degeneration at the input stage in order to achieve wideband input matching with 15 μm transistors. RC extraction is used to capture the parasitic elements of low metal level structure around transistors, and interconnects and transmission lines in the upper metal levels are simulated using Sonnet 3-D EM simulator in order to correctly account parasitic inductance.

3.3.2 Measurements

The D-band amplifiers are fabricated in IBM's 45-nm SOI CMOS process. (Fig. 3.7) The 5-stage CS amplifier occupies 880×590 μm^2 of area, and the 3-stage cascode amplifier occupies 700×500, both including GSG probe pads.

Small-signal S-parameters of the amplifiers and related test structures are measured using in-house D-/G-band measurement setup, which consists of Agilent E8364B vector network analyzer, N5260A millimeter head controller, and VDI WR5.1 extenders. On-chip TRL calibration as well as SOLT calibration (GGB CS-15) is performed prior to the measurement. The reference plane of the TRL calibration is also shown in Fig. 3.7. Calibration procedure is verified within ±0.2 dB over frequency by measuring the calibration standard again.



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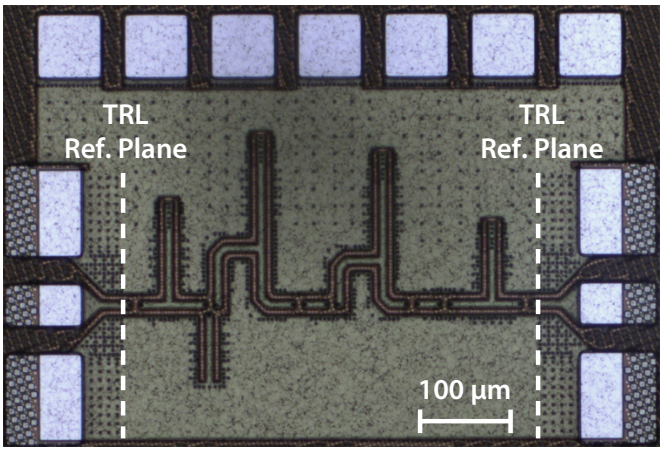
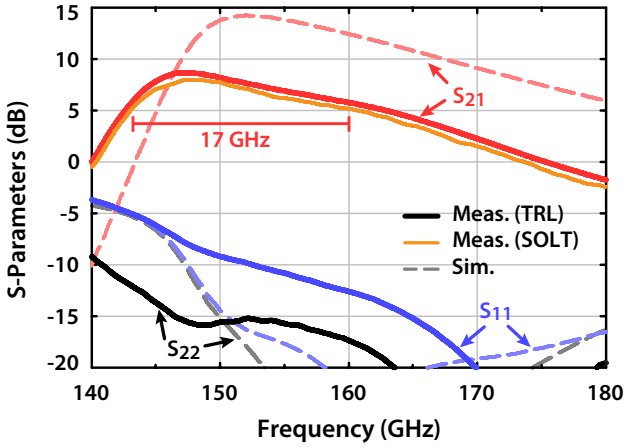


(b)

Figure 3.7: Microphotographs of (a) the 5-stage CS amplifier and (b) the 3-stage cascode amplifier. The TRL reference planes are also shown.



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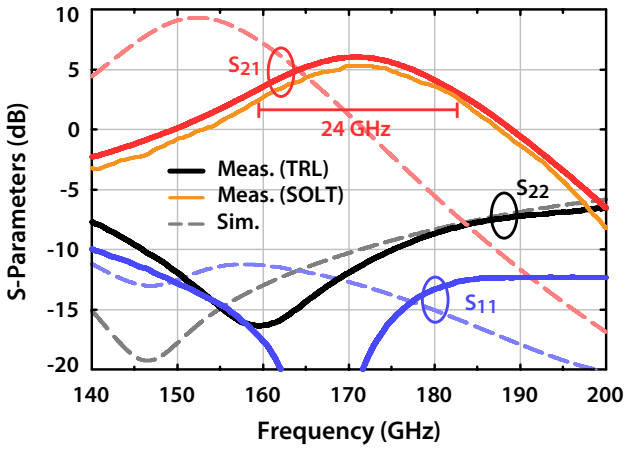


(b)

Figure 3.8: Measured and simulated S-parameters of the D-band (a) the common-source amplifier and (b) the cascode amplifier.

Fig. 3.8 presents the measured and simulated S-parameters of the D-band amplifiers. The 5-stage CS amplifier has a peak gain of 8.7 dB at 147 GHz with 17 GHz 3-dB bandwidth while consuming 49.7 mW from 1.4 V supply. The 3-stage cascode amplifier has a peak gain of 6.1 dB at 171 GHz, a 3-dB bandwidth of 24 GHz, and a DC power consumption of 53.4 mW from 2.0 V supply.

The maximum measured output power from the CS amplifier is -1.6 dBm at 150 GHz, and -4.5 dBm at 170 GHz from the cascode amplifier. Both amplifers do not show gain compression at -8 dBm input, which is limited by available source.

3.3.3 Discussion

Table I summarizes and compares this work with other CMOS D-band amplifiers reported in the literature. The 3-stage cascode amplifier presented in this letter exhibits the highest operating frequency as a D-band CMOS amplifier. The discrepancy between the measurement and simulation is likely due to the excessive loss in the BEOL passive elements, requiring further attention in the CMOS D-band amplifier design.

3.4 V-band Active Phase Shifter in 45nm SOI CMOS Technology

3.4.1 Design

An active phase shifter is a good candidate for a multi-element electronic phased array for wireless communication thanks to its low insertion loss and smaller layout size. Fig. 3.9 presents a block diagram of such an active phase shifter, which relies its operation on vector interpolation techniques. An in-phase and a quadrature-phase outputs (I/Q) of an input signal are generated by an I/Q generator network, such as a quadrature all-pass filter (QAF) or an RC poly-phase filter. The I and Q signals undergo separate gain and sign control with different weighting and summed together to synthesize an output signal with a desired phase rotation. In principle, the separate gain/sign controls for I and Q signals enable the freedom to generate an arbitrary basis vector which can cover all 360° with respect to the input signal. Among parameters which determine the

Table 3.1: CMOS D-band Amplifier Comparison

	[67]	[65]	[68]	This Work	This Work
Technology	65nm Bulk CMOS	65nm Bulk CMOS	65nm Bulk CMOS	45nm SOI CMOS	45nm SOI CMOS
Topology	6-stage CS+CG	3-stage CS	4-stage CS	5-stage CS	3-stage cas-code
Frequency (GHz)	140	150	150	147	171
3-dB BW (GHz)	10	27	>30	17	24
Gain (dB)	8	8.2	16	8.7	6.1
P_{DC} (mW)	63	25.5	115.2	49.7	53.4
Area* (mm^2)	N/A	0.41	0.38	0.52	0.35

*including pads

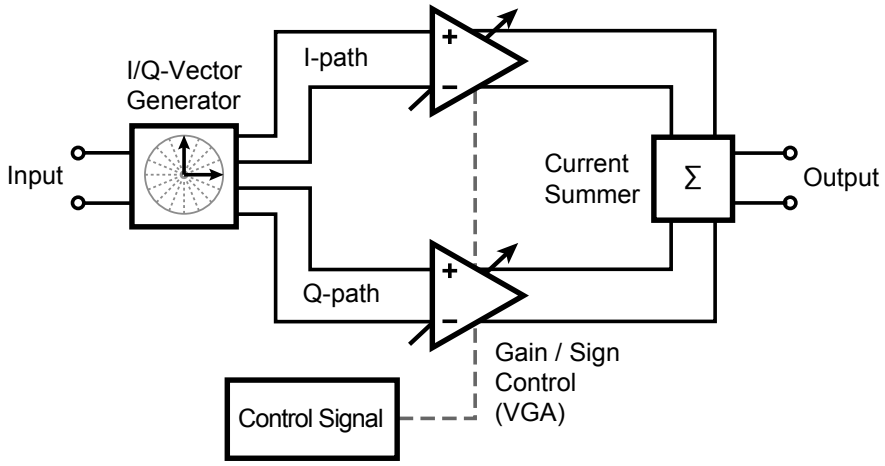


Figure 3.9: Block diagram of an active phase shifter.

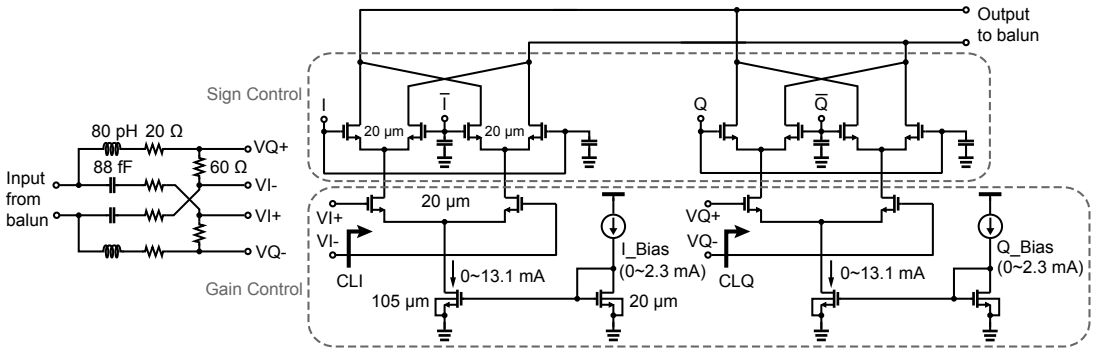
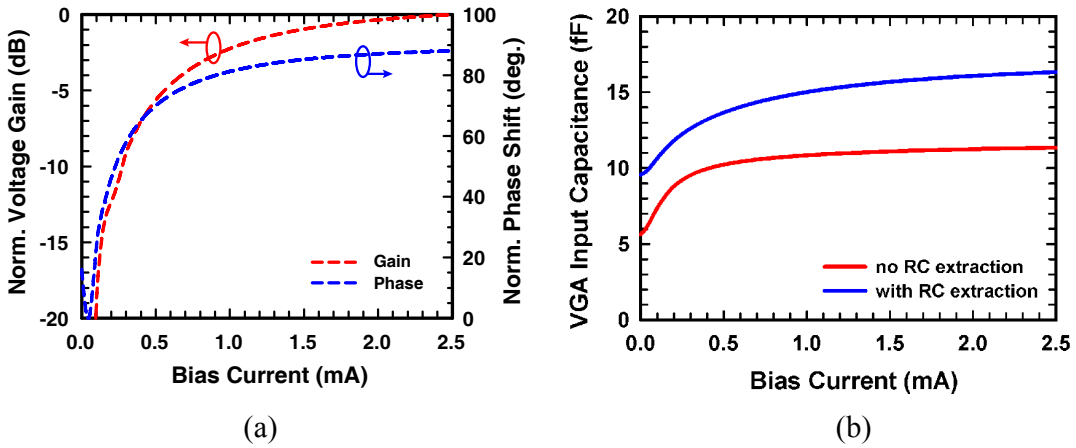


Figure 3.10: Schematic diagram of the active phase shifter.



(a) (b)

Figure 3.11: Simulated (a) normalized gain and phase response and (b) input capacitance of the Gilbert-cell VGA over bias current.

performance of the active phase shifter are amplitude/phase mismatch of the I/Q generator, gain/phase response of the gain/sign control stage over different weighting, number of bits control the weighting factor, and overall insertion loss and bandwith along with power consumption.

Fig. 3.10 presents the schematic diagram for the active phase shifter designed in 45nm SOI CMOS technology. The I/Q generator network is implemented with a quadrature all-pass filter (QAF) network, and the gain/sign control stages are implemented with a pair of Gilbert-cell type differential variable-gain amplifiers (VGA). The gain weighting is controlled by changing the bias current of the Gilbert-cell, and the sign (or polarity) of the signal is controlled by using the switching core. Each I and Q path has one Gilbert-cell amplifier, and the weighted I/Q signals are combined in the current domain at the drain nodes. The selection of QAF is driven by its low insertion loss, wide bandwidth, and resistive input impedance (which in a desirable case can be matched to input). The Gilbert-cell VGA is chosen for its high reverse isolation (S_{21}). The low reverse isolation can be problematic at the millimeter-wave frequencies by increasing the capacitive loading to the QAF through the Miller effect.

The Gilbert-cell type VGA uses dual gate-contacted floating-body NMOS transistors with 20 fingers and 1 μm width per finger, and at the maximum gain state it consumes 13.1 mA for either I or Q VGA, resulting in 0.33 mA/μm current density

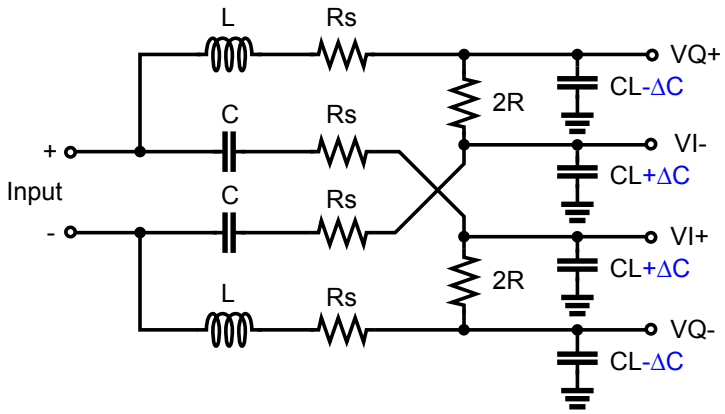


Figure 3.12: General structure of the quadrature all-pass filter including asymmetric capacitve loading between I/Q outputs.

for maximal performance. The required voltage variation range for the VGA can be obtained by using simple trigonometric relationship. For example, in order to obtain a 4-bit phase shifter operation, the minimum phase step is 22.5° and the amplitude of the non-zero minimum basis vector is $\sin(22.5°) = 0.382$ times smaller, which is -8.36 dB lower in the current amplitude than the maximum value. By the same token, the gain variation range of 5-bit phase shifter operation is -14.20 dB. As MOS transistor g_m becomes linear in short-channel devices [69], obtaining the amount of variation range is a challenging task in advanced CMOS technologies such as 45 nm SOI CMOS. Moreover, the phase response of VGA itself and the input capacitance of MOS transistor change over the gain weighting, in extreme cases one of two VGA is completely turned off. Fig. 3.11 show variation of gain response, phase response, and input capacitance of the Gilbert-cell VGA over bias current. It can be observed that phase response of the VGA changes about 30° with 8 dB voltage variation, and the input capacitance ($C_{L,I}$ or $C_{L,Q}$) of the VGA changes from 10 fF to 16 fF over biasing.

The capacitive loading to the QAF degrades amplitude mismatch and phase error of the quadrature all-pass filter [70]. In order to keep C_L/C as low as possible, the values for inductance and capacitance are chosen to be 80 pH and 88 fF, resulting in impedance $Z_0 = \sqrt{L/C} = R = 30\ \Omega$. Still, the loading capacitance of 10–16 fF is not negligible and has a large effect on a 60 GHz vector modulator. C_L/C (capacitive loading to QAF) is

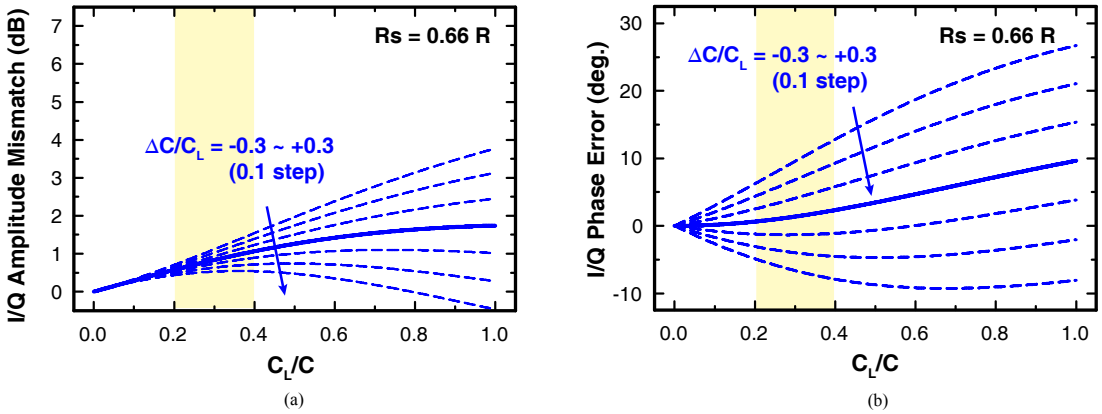


Figure 3.13: Simulated (a) amplitude mismatch and (b) phase error of the QAF general structure under the condition of $R_s = 0.66R$ and $\Delta C/C_L = \pm 0.3$.

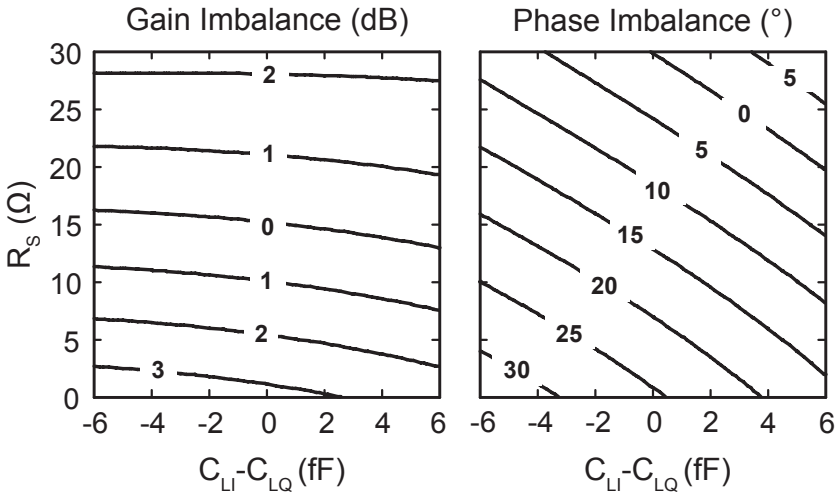


Figure 3.14: Effect of the series resistance, R_S, on amplitude imbalance and phase error under asymmetric loading.

Table 3.2: Simulated performance and phasor diagrams for selected phase states

Phase State	I Bias (mA)	Q Bias (mA)	Gain (dB)	IP1dB (dBm)	Power (mW)
0°	2.5	0	-4.0	1.3	22.2
22.5°	2.2	0.27	-7.3	6.0	22.6
45°	1.8	0.5	-7.7	5.0	21.6
67.5°	1.1	1.15	-6.3	1.4	21.9
90°	0	2.5	-3.7	0.6	22.1

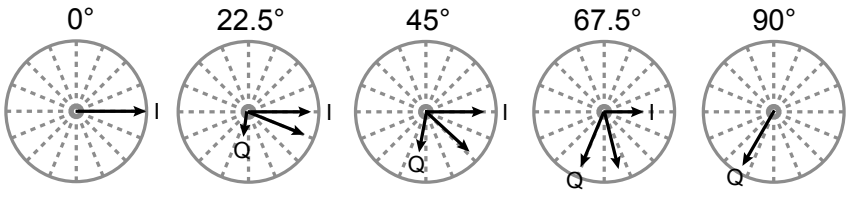


Figure 3.15: Phasor diagram of I- and Q-vectors for different phase states.

0.23–0.34 (C_L is the single-ended loading to QAF and is twice of $C_{L,I}$ or $C_{L,Q}$), and this results in 2–3 dB amplitude mismatch and 3–5° phase error. Putting series resistors in QAF branches improves the amplitude mismatch and phase error at the cost of insertion gain [71]. In this design, $R_s = 20\ \Omega$ is chosen to have improved ampiltude mismatch of ~1 dB.

In addition, in general, different phase states require different weighting at the I/Q VGA, resulting in different bias currents and different input capacitances for I and Q VGAs (Fig. 3.12). This asymmetric capacitive loading in addition to the nominal capacitive loading to QAF stage further degrades phase error, up to $\pm 10°$ with $\pm 30\%$ deviation from nominal capacitive loading (Fig. 3.13). It also means that for every phase setting (and different bias currents), there is a varying amplitude and phase error present at the vector modulator I/Q ports.

The active phase shifter is designed and simulated with foundry-provided design kit model (which does not support valid model at 60 GHz) using Cadence® IC design software. Also, RC extraction using Calibre® tool is performed to capture lower level

metal parasitic effects, and Sonnet® EM simulator is used for upper level metal layers including inductors and long interconnects. The post-layout simulation of QAF output is presented in Fig. 3.14. For $C_{L,I} = C_{L,Q} = 13$ fF, amplitude imbalance and phase error changes over asymmetric loading ($C_{L,I} - C_{L,Q}$). It can be seen that inclusion of R_s improves the overall gain imbalance and phase error, resulting in 0–1 dB gain imbalance and 0–17° phase marging for $C_{L,I} - C_{L,Q} = \pm 6$ fF with $R_s = 20\ \Omega$.

Table 3.2 presents the simulated peformance of the active phase shifter for different phase states along with the current distribution in I/Q VGA, and Fig. 3.15 presents resulting phasor diagrams of I-vector, Q-vector, and synthesized output vector. The I vector, chosen as a reference, is obtained under the bias condition of $I, Q = 2.5, 0$ mA and a $C_{L,I} - C_{L,Q} = +6$ fF. On the other hand, the Q vector is obtained under the bias condition of $I, Q = 0, 2.5$ mA and a $C_{L,I} - C_{L,Q} = -6$ fF. The vector modulator can still be designed under a (near) constant current consumption, but the penalty is a 4 dB variation in the gain and 5.5 dB variation in the P1dB. Simulated noise figure is 13 dB at 60 GHz at 0° phase state.

3.4.2 Measurements

A microphotograph of the 60 GHz phase shifter is shown in Fig. 3.16. The input and output baluns are designed for single-ended measurement. The simulated insertion loss of input and output balun is 1 dB and 2 dB at 60 GHz, respectively. The active phase shifter is measured using GSG probes with Agilent E8361A vector network analyzer. The measured input and output reflection coefficient vs. 16 phase states are presented in Fig. 3.18, and the S_{21} gain and phase response of the active phase shifter is presented in Fig. 3.17. There is a frequency shift down to ~55 GHz, and input -10 dB bandwidth is from 45–63 GHz. There is a 4 dB peak-to-peak gain variation as predicted by simulation, and RMS gain variation is <1.5 dB over all frequencies. Please note the wide bandwidth of the gain response due to the use of relatively high R_s and thus low Q in the QAF network. The phase response shows ~10° of RMS phase variation with 16 phase states, meeting the requirement of 4-bit phase shifter operation. The measured input P1dB at 55 GHz is shown in Fig. 3.19 and agrees with simulations for most phase states.

3.5 Conclusion

The chapter present the first active CMOS phase shifter in 45nm SOI CMOS technology in 60 GHz, to the author's knowledge. The challenges in the design of the millimeter-wave CMOS active phase shifter are identified, and the design is optimized to mitigate severe capacitive loading effect in this frequency range. The phase shifter consumes 23.1 mW from 1.5V supply, and has an average insertion gain of -7 dB, and input P1dB of -1–3 dBm.

3.6 Acknowledgement

This work is supported by Intel corporation, under a UC-Discovery project, and by DARPA LEAP program which provided access to the 45nm SOI CMOS process.

This chapter is in part a reprint of the material as it appears in:

- W. Shin and G. M. rebeiz, "60 GHz active phase shifter using an optimized quadrature all-pass network in 45nm CMOS," *IEEE Microwave Symposium Digest*, Jun. 2012, pp. 17-22.

The dissertation author is the primary author of this material.

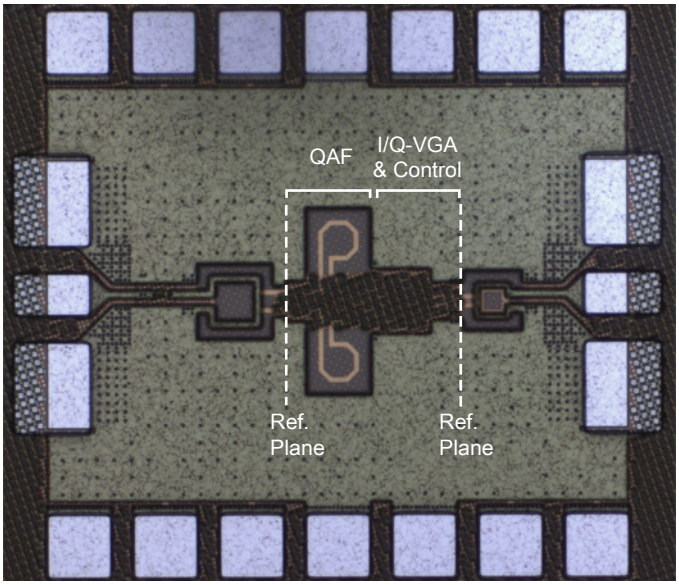
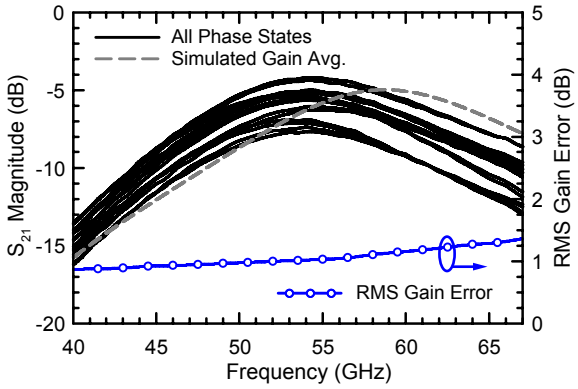
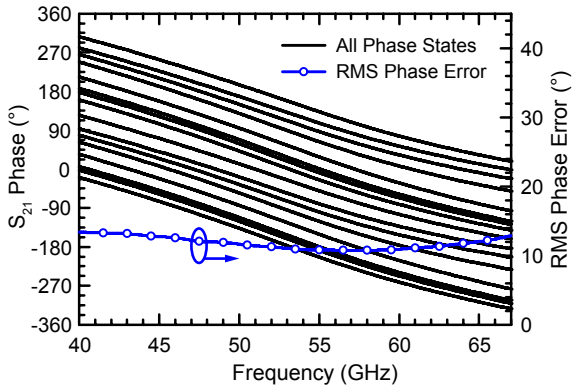


Figure 3.16: Microphotograph of the 60 GHz active phase shifter.



(a)



(b)

Figure 3.17: Measured (a) gain and (b) phase response of the 60 GHz active phase shifter for 16 phase states (4-bit operation)

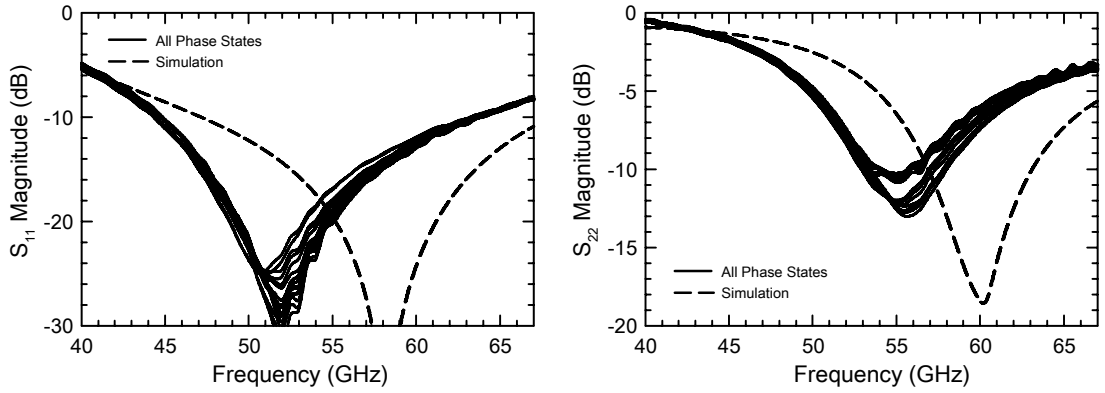


Figure 3.18: Measured (a) input and (b) output return loss of the 60 GHz active phase shifter for 16 phase states (4-bit operation)

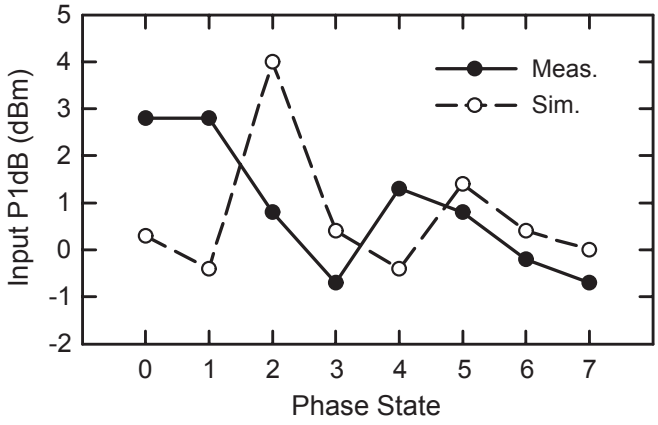


Figure 3.19: Measured (a) gain and (b) phase response of the 60 GHz active phase shifter for 16 phase states (4-bit operation)

Chapter 4

60 GHz Low Power OOK Transmitter in 90nm CMOS Technology

4.1 Introduction

The 60 GHz band has attracted a lot of attention recently due to the availability of unlicensed wide spectrum. This allows Gb/s communication links for media and personal communication networks [72]. Several SiGe and CMOS-based transceivers have been developed in the past two years, mostly based on QPSK or BSPK modulation techniques [72, 73, 74, 75, 76]. The QPSK allows for an OFDM architecture which is essential for multipath mitigation, while the BPSK allows for high sensitivity point-to-point links with relatively low power consumption. Still, for point-to-point communications with short link distances (1–3 ft), the amplitude-shift-keying (ASK, or on-off-keying, OOK) modulation offers an excellent solution with very low power operation. This technique does not require any locking of the local oscillator to a PLL which draws significant current for 60 GHz oscillators. Also, it does not require an I/Q or a synchronous demodulator, resulting in a very simple receiver [77, 78, 79, 36, 80]. However, the ASK is prone to interference from other sources and therefore, must be used with directional antennas and for short distance operation. Also, the receive sensitivity is not high (-36 dBm to -40 dBm for a 3–5 Gbps link [77]) which limits its range. Still, when used with highly directional antennas, it offers significant power saving over the

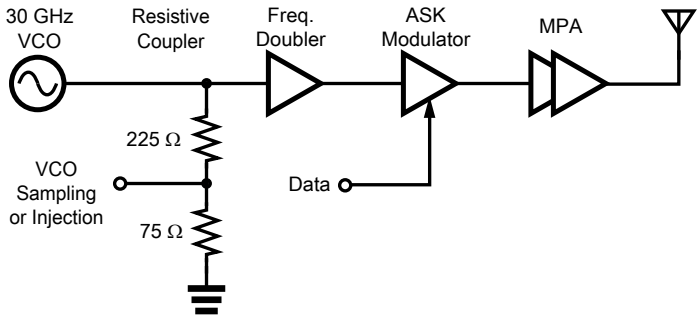


Figure 4.1: Block diagram of the OOK transmitter in 90nm CMOS technology.

QPSK or BPSK architectures, and is a competitive architecture for hand-held 60 GHz units.

Previously, several ASK (or OOK) receivers have been developed using SiGe, CMOS or Schottky diode technologies [77, 78, 79, 36]. This chapter presents a 90 nm ASK transmitter capable of 1–2 Gb/s operation (Fig. 4.1). The chip also contains a port to monitor the LO signal or to inject an external local oscillator. The chip is mounted on a PC board attached to a planar Yagi-Uda antenna with high gain patterns.

4.2 Design

The ASK transmitter is built using the IBM 90nm CMOS process (IBM 9RF). This process uses an NMOS transistor with an ft/fmax of 130/140 GHz, and has 8 metal/dielectric layers above the silicon substrate. The top metal layer is 4.0 μm thick on a 10.3 μm SiO_2 dielectric, and results in a simulated Q of 16 at 60 GHz for CPW transmission lines (GSG = 12/10/12 μm).

The circuit diagram of the ASK transmitter is shown in Fig. 4.2. The 30 GHz oscillator is followed by a resistive sampler/coupler, a doubler, an ASK modulator, and a medium power amplifier. The output is attached to a planar off-chip antenna. The resistive sampler has dual purposes: 1) it allows the local oscillator to be sampled externally using a simple power sensor, and 2) it allows a test signal to be injected into the circuit (while the VCO is turned off) so as to independently test the doubler/ASK modulator. All circuits are single-ended and are based on a transmission-line design except

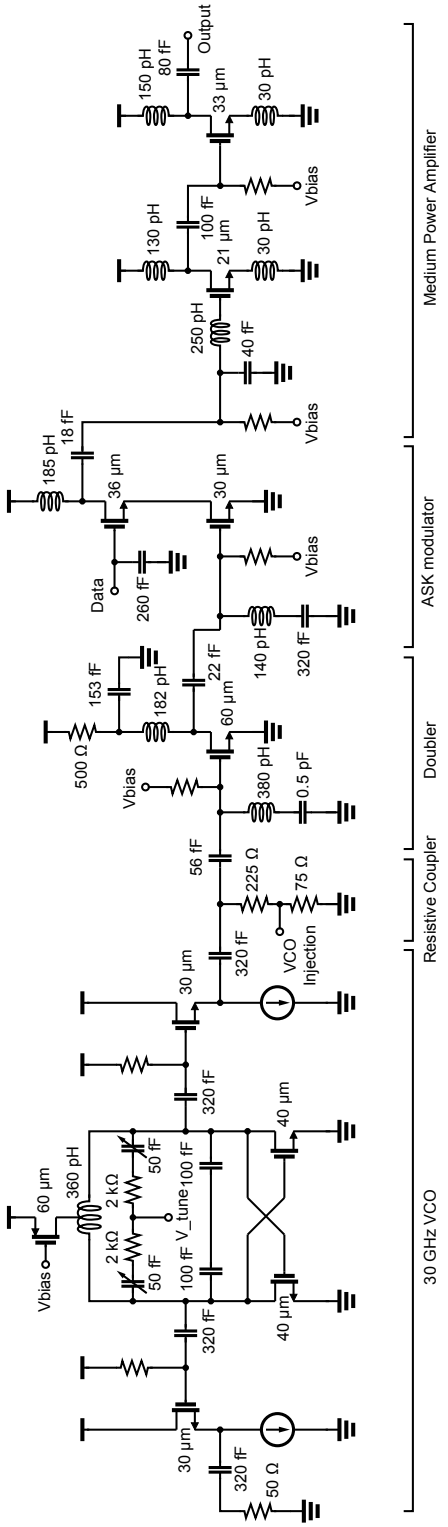


Figure 4.2: Schematic of the OOK transmitter.

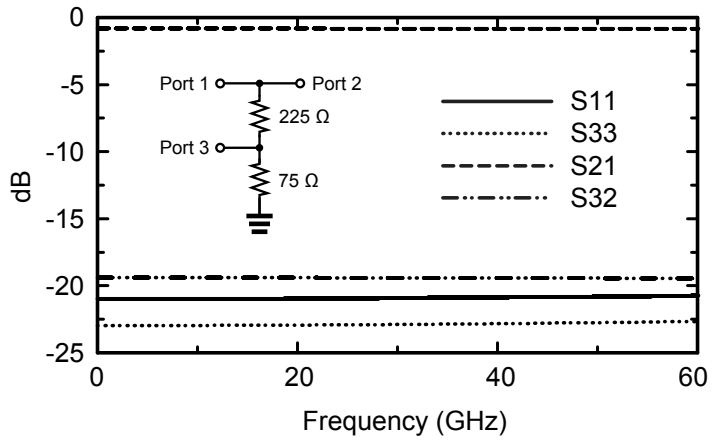


Figure 4.3: S-parameter response of the resistive coupler.

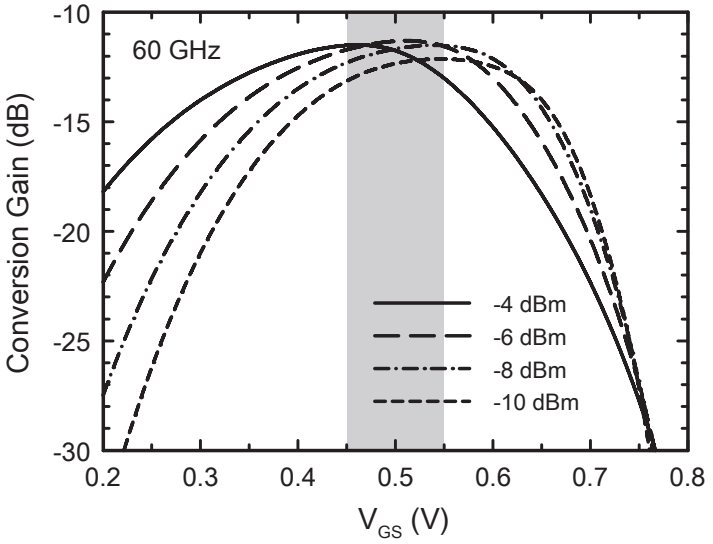


Figure 4.4: Simulated conversion gain of the frequency doubler with different bias voltages.

the VCO which is differential. The VCO design is based on a differential inductor and results in low phase noise and higher performance as compared to a single-ended design. The VCO, doubler, ASK modulator and medium power amplifier are all designed using 50 Ω blocks. No transformers are used between the oscillator and the doubler, and only one node is fed to the doubler to save on chip area.

The simulated S-parameters of the resistive coupler are shown in Fig. 4.3. The use of a $225 + 75\Omega$ shunt load results in an additional insertion loss of < 1 dB, while still maintaining excellent match at the VCO and doubler ports. Also, about -20 dB of the VCO power is sampled to the external port, or an injection efficiency of -20 dB is present for an external source. The resistive coupler is also matched at the injection port (Port 3).

The doubler is based on a single-ended transistor biased in class-B, and its optimum bias point is found to be around $V_{GS} = 500$ mV using the simulation for broad-range of input power (Fig. 4.4). The ASK modulator is implemented using a cascode amplifier with the 1–2 Gb/s data fed to the common-gate stage in order to modulate high-frequency carrier with baseband data. This topology allows up to 2 Gb/s operation before transient ringing distorts the signal. The medium power amplifier is a two-stage common-source design with a simulated gain of 12 dB at 60 GHz with +5 dBm of output saturated power. The power conumption of the ASK transmitter is summarized in Table 4.1.

4.3 Measurements

The OOK transmitter was fabricated in IBM 9RF (Fig. 4.5) together with independent circuits for the oscillator, doubler, OOK modulator and medium power amplifier. The entire transmitter chip, including pads, is < 1.1 mm^2 in area and consumes 31 mW of DC power.

The oscillator was independently tested and results in an output power of -11.2 dBm and a phase noise of -99.6 dBc/Hz at 1 MHz from the carrier and is competitive with other 30 GHz designs [81, 82] (Fig. 4.6a and Fig. 4.6b). The tuning range is 64 MHz, of which main purpose is to set the center frequency for OOK modulation. Its

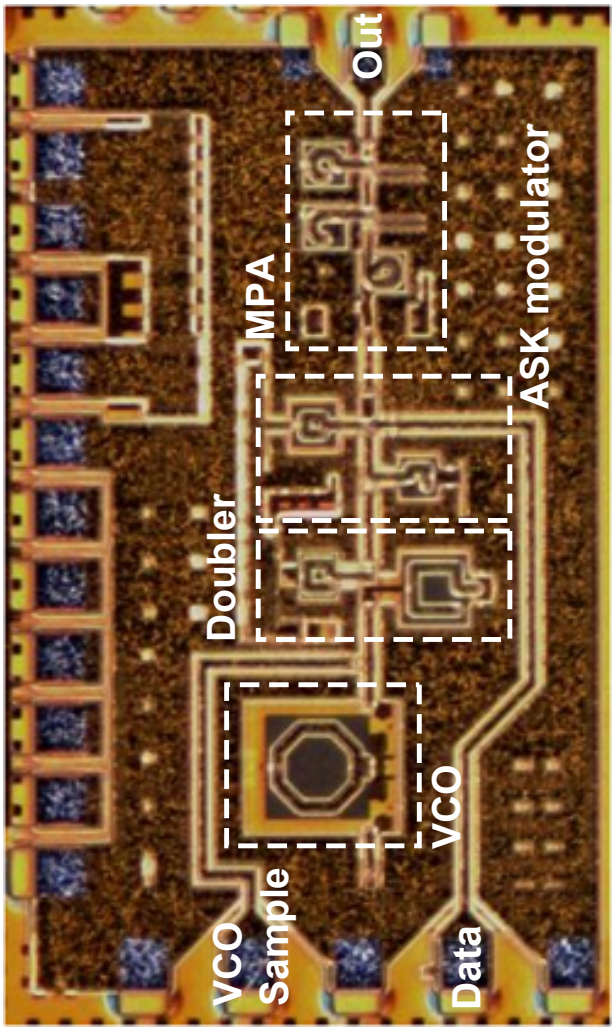
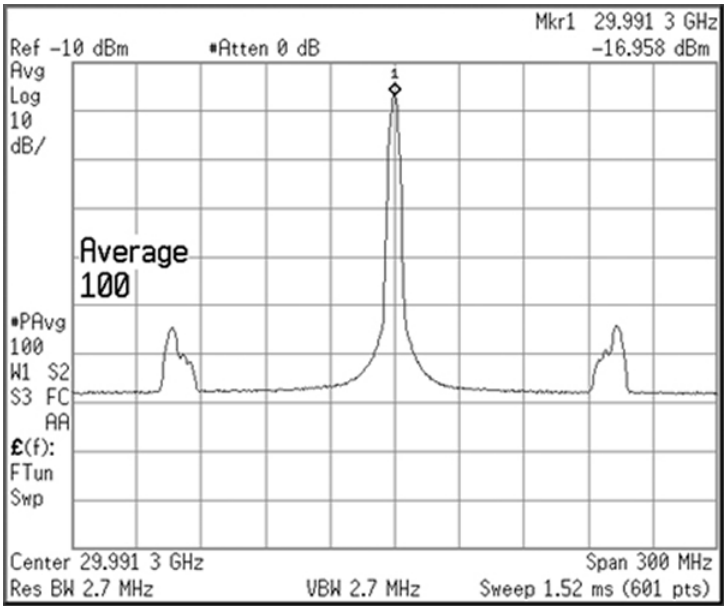
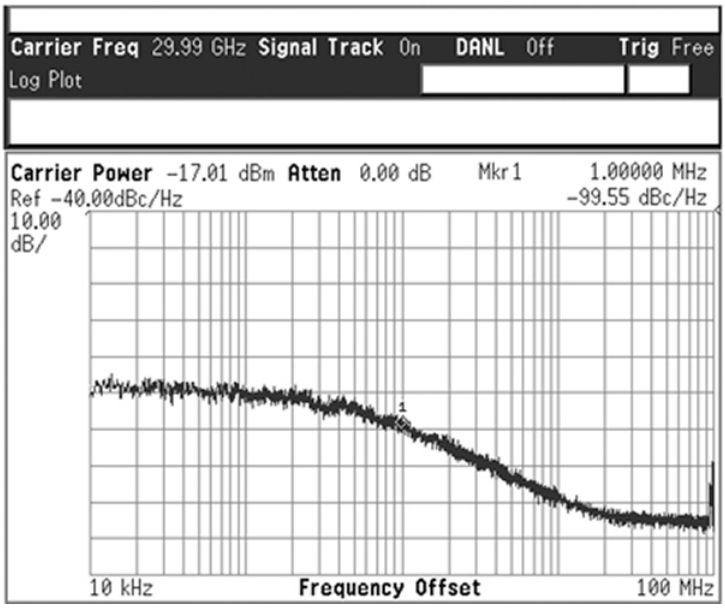


Figure 4.5: Microphotograph of the fabricated OOK transmitter.



(a) VCO output spectrum



(b) VCO phase noise

Figure 4.6: Measured (a) spectrum and (b) phase noise of 30 GHz VCO. Output power includes loss in the measurement apparatus, and up-converted FM interference is also measured. Phase noise at 1.0 MHz offset is -99.6 dBc/Hz.

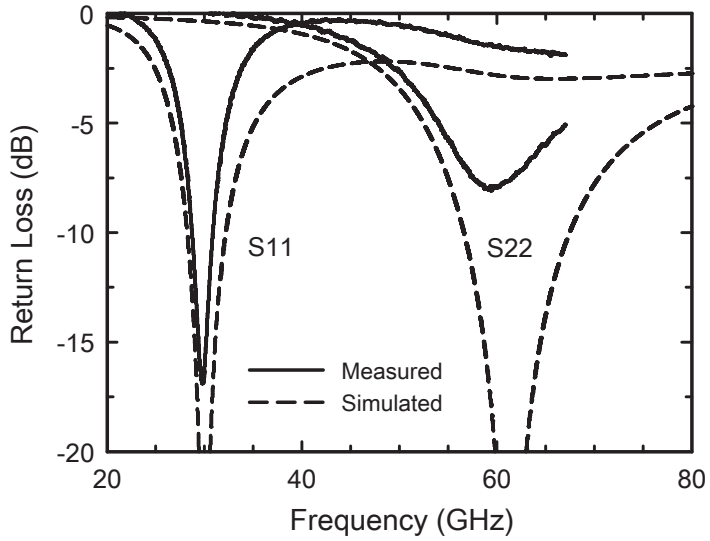
consumes 10.0 mA from 1.2 V supply, and occupies 255 x 290 μm^2 including buffer. A summary of the VCO performance is shown in Table 4.2.

The doubler was characterized using small signal S-parameter technique for its return losses (Fig. 4.7a) and using a large signal techniques at different frequencies for its conversion gain (Fig. 4.7b). The measurements of the frequency doubler agree with simulations, and it input -10 dB bandwidth is 28–32 GHz, and its conversion loss is 11–12 dB with from -9 to -5 dBm input power. It consumes 0.6 mA from 1.2 V supply.

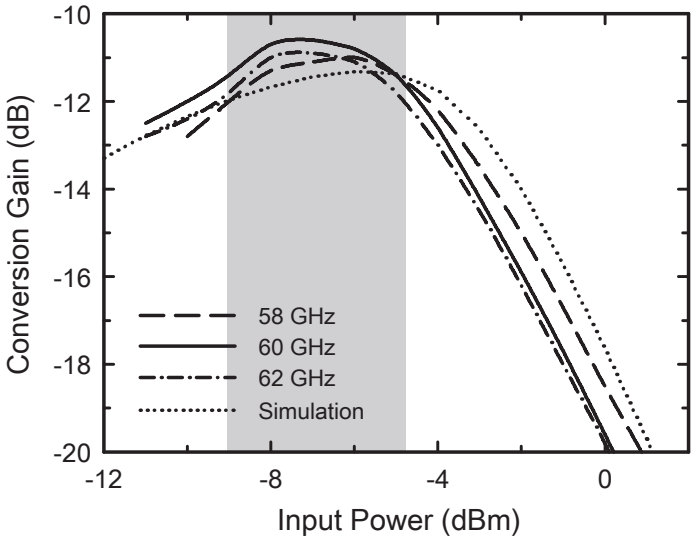
The S-parameters of the OOK modulator are also measured, and its S_{11} and S_{22} are matched at 55–60 GHz for both on (Fig. 4.8a) and off (Fig. 4.8b) states. The modulator gain is -1.8 dB from 55–65 GHz, while its input -10 dB bandwidth is 58–68 GHz. (Fig. 4.9) The output signal has 19.2 dB on/off ratio which is about 9 dB smaller than simulation. This attributes to the modeling inaccuracy of parasitic capacitance of MOS transistor. It consumes 3.0 mA from 1.2 V supply when it is on state.

The medium power amplifier is also characterized by the large-signal behavior in 60 GHz as well as by the S-parameters. It results in a small-signal peak gain of 10.7 dB at 54.6 GHz with a 3-dB bandwidth of 50–61.4 GHz which is 21 % of fractional bandwidth. (Fig. 4.10a) It also shows an output P1dB of 1.4 dBm and saturated output power of > 5 dBm, with peak PAE of 12.9 % (Fig. 4.10b). It can operates up to 100 °C with 2.5 dB reduction in the gain.

The ASK transmitter is tested using a 1–2 Gbps data stream from an Agilent N4903A BER tester. The measured spectrum with the internal VCO and an external frequency source are shown in Fig. 4.11 and Fig. 4.12. The VCO is free running and drifts during spectrum measurements creating a distorted spectrum and the absence of deep nulls, but this has little effect on the ASK performance. Both cases with external source and internal VCO show 1 Gb/s operation, and similar spectrums were obtained at 1.5 Gb/s. However, the spectrum starts to degrade at 2 Gb/s due to the switching bandwidth of the ASK modulator, as predicted by simulations.

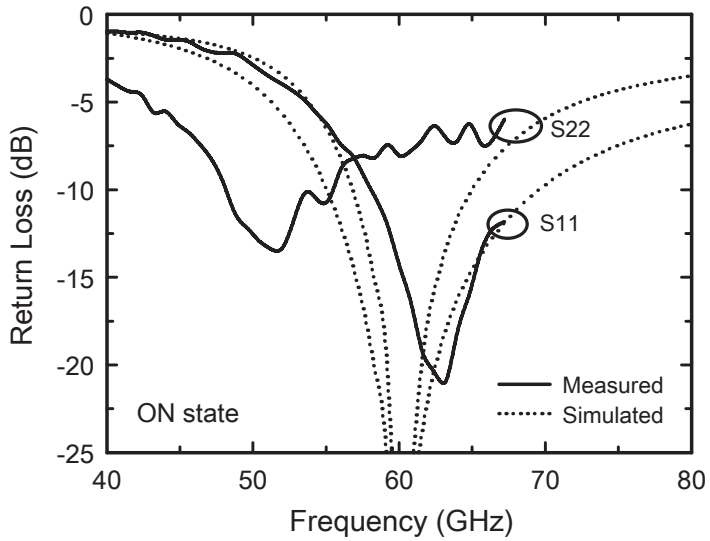


(a)

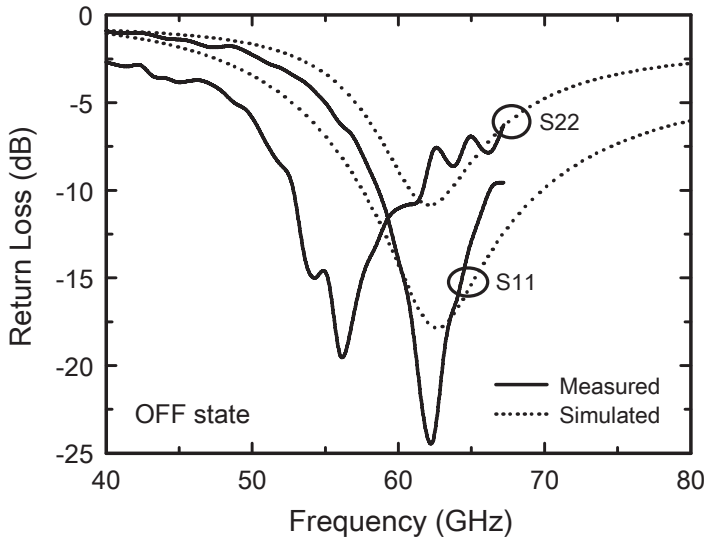


(b)

Figure 4.7: Measured (a) S-parameters and (b) conversion gain of the frequency doubler.



(a)



(b)

Figure 4.8: Measured return loss of the OOK modulator in (a) ON state (Data = 1) and (b) OFF state (Data=0).

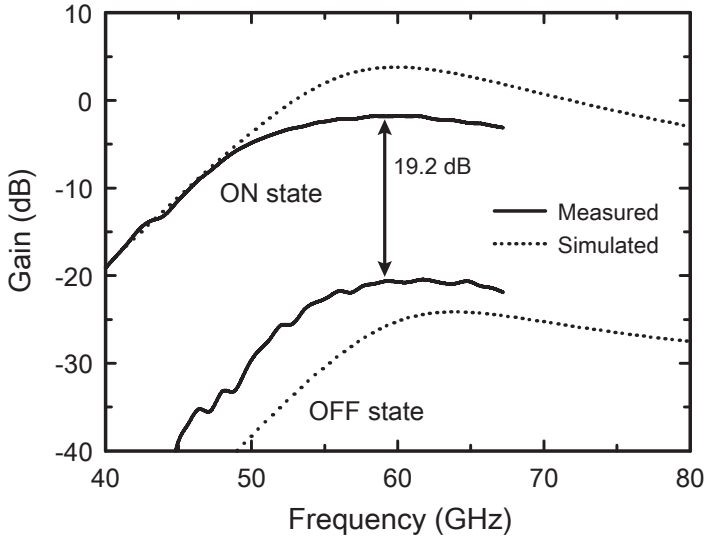


Figure 4.9: Measured gain of the OOK modulator in both ON/OFF states.

4.4 Conclusion

A low power 60 GHz OOK transmitter is developed in 90 nm CMOS technology. The data rate is limited by the single-ended OOK modulator to 1.5 Gb/s. This chip can find its application in short range (0.3–0.5 m) communication link using directional antennas with 11–12 dBi gain.

4.5 Acknowledgement

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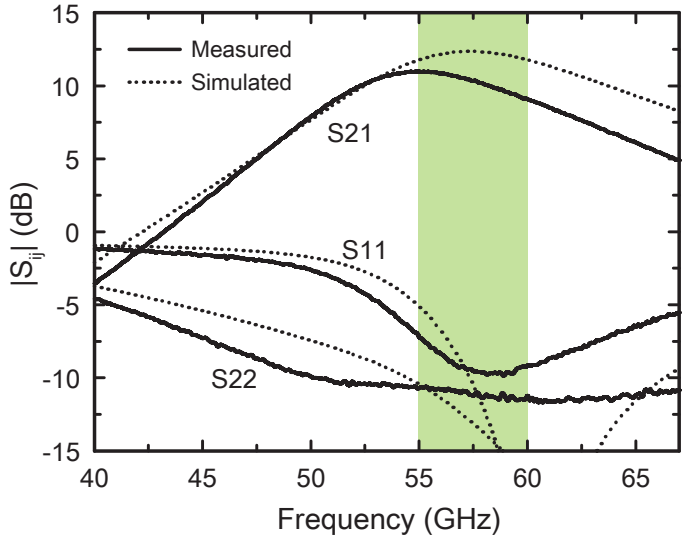
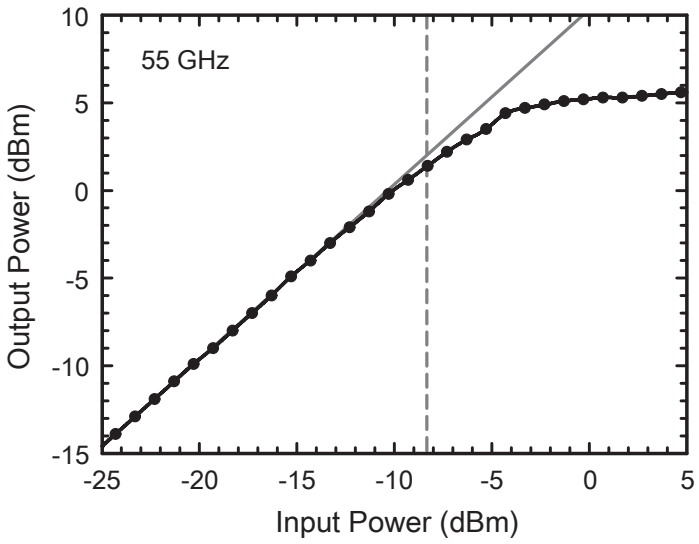
This chapter is mostly a reprint of the material as it appears in:

- W. Shin, M. Uzunkol, R. A. Alhalabi, and G. M. Rebeiz, "60 GHz Low Power 1.5 Gb/s ASK Transmitter in 90 nm CMOS with On-board Yagi-Uda Antenna," *IEEE European Microwave Conference*, Sep. 2010, pp. 272-275.

The dissertation author is the primary author of this material.



(a)



(b)

Figure 4.10: Measured (a) S-parameters and (b) power compression curve of the 60 GHz medium power amplifier.

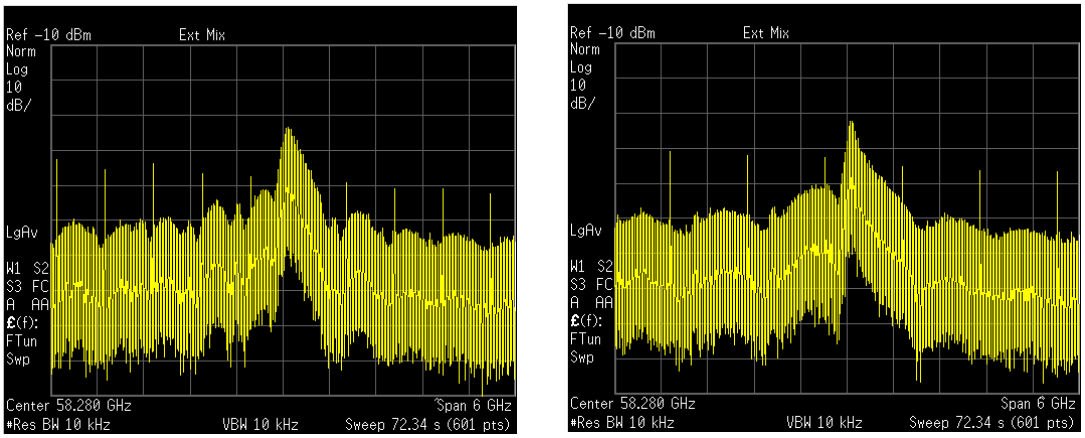


Figure 4.11: Measured output spectrum of the OOK transmitter with internal VCO: (a) 622 Mbps data stream and (b) 1 Gbps data stream

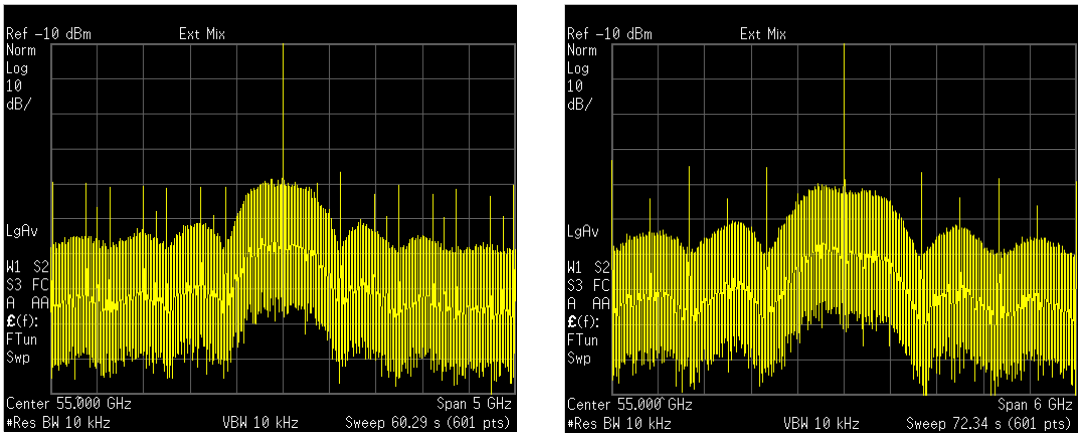


Figure 4.12: Measured output spectrum of the OOK transmitter with external frequency source: (a) 622 Mbps data stream and (b) 1 Gbps data stream

Table 4.1: DC power consumption of the ASK transmitter

Component	Current (mA)	Power (mW)
VCO*	10	12
Resistive Coupler	0	0
Doubler	0.5	0.6
ASK Modulator	3	3.6
Medium Power Amplifier	12.5	15
Total	26	31.2

*including buffer

Table 4.2: VCO Performance

Frequency	29.99 GHz
Tuning Range	64 MHz
Phase Noise	-99.6 dBc/Hz at 1 MHz offset
Output Power (Single-ended)	-11.2 dBm
Power Consumption*	12 mW

*including buffer

Chapter 5

Conclusion

The first wafer-scale silicon phased array with attached on-chip antennas is designed and demonstrated. The phased array operates at 110 GHz and is implemented in a 0.18 μm SiGe BiCMOS technology. The measurements show 26.5 dB array gain, 24.0 dBm maximum EIRP, and 28° 3-dB beamwidth at 110 GHz. It also demonstrates beam-steering capabilities up to ±30°in both principal planes with 2-bit phase shifting operation at each antenna element. Its operation also covers from 108–114 GHz with similar performance. The phased array architecture can be adapted to any arbitrary frequency and can be scaled to large number of elements. Based on the experimental characterization of this work, future improvement can be made in amplifiers in the distribution network, VDD/GND routing grid, and impedance transformer at antenna feed structure. A phased array reciever with the same architecture would constitute a millimeter-wave point-to-point communication link.

The possibility and prospect of millimeter-wave circuits and systems of CMOS technology are demonstrated, in particular with 45nm SOI CMOS technology in D-band and 60 GHz frequency band. A D-band amplifier design result in > 5 dB gain at 170 GHz with 24 GHz 3-dB bandwidth, showing a prospect of high-band mm-wave CMOS systems. However, on-chip passive structure including inductors and interdigitated finger metal-oxide-metal capacitors show severe degradation in Q-factors, still presenting challenges in circuit design. While development of an RF-oriented back-end process would ease burden on the circuit design aspect, a different design appoach such as transformer coupling circuit could improve overall circuit performance without using lossy passive

elements. The experimental result of the 60 GHz active phase shifter in SOI CMOS process also calls for an improved circuit design methodology at millimeter-wave frequencies. As performance of quadrature all-pass I/Q network changes over capacitive loading and its asymmetry, a constant-loading structure in the following stage could prevent the issue. Among possibilities are insertion of a buffer stage, a constant-IP3 I/Q VGA [83], or calibration with fine digital codes. However, different alternatives have different benefits and drawbacks, and system-level considerations would be required for the appropriate choice of the architecture.

A 60 GHz OOK transmitter is designed and its output spectrum with input data stream is obtained. Single-ended design results in simple low-power implementation, with which the OOK transmitter can support 1.5 Gbps data stream while consuming 31.2 mW from 1.2 V supply. A current-sink bypass switch in cascode stage of the OOK modulator can be used to improve on-off ratio and thus overall OOK communication link. Also, an optimized balun can be used at the output of the oscillator to utilize the full scale output swing.

Bibliography

[1] J. Cressler, "Emerging application opportunities for SiGe technology," in *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2008, pp. 57–64.

[2] A. Cathelin, B. Martineau, N. Seller, F. Gianesello, C. Raynaud, and D. Belot, "Deep-submicron digital CMOS potentialities for millimeter-wave applications," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2008, pp. 53–56.

[3] "International Technology Roadmap for Semiconductors." [Online]. Available: http://www.itrs.net

[4] T. Hancock and G. M. Rebeiz, "A 12-GHz SiGe phase shifter with integrated LNA," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 3, pp. 977–983, Mar. 2005.

[5] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, "A four-antenna receiver in 90-nm CMOS for beamforming and spatial diversity," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2515–2524, Dec. 2005.

[6] H. Hashemi, X. Guan, A. Komijani, and A. Hajimiri, "A 24-GHz SiGe phased-array receiver–LO phase-shifting approach," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 2, pp. 614–626, Feb. 2005.

[7] B.-W. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2239–2250, Oct. 2008.

[8] J. Comeau, M. Morton, W.-M. Kuo, T. Thrivikraman, J. Andrews, C. Grens, J. Cressler, J. Papapolymerou, and M. Mitchell, "A silicon-germanium receiver for X-Band transmit/receive radar modules," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 1889–1896, Sep. 2008.

[9] T. Yu and G. M. Rebeiz, "A 22-24 GHz 4-element CMOS phased array with on-chip coupling characterization," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2134–2143, Sep. 2008.

[10] H. Krishnaswamy and H. Hashemi, "A variable-phase ring oscillator and PLL architecture for integrated phased array transceivers," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2446–2463, Nov. 2008.

[11] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A bidirectional TX/RX four-element phased array at 60 GHz with RF-IF conversion block in 90-nm CMOS process," *IEEE Trans. Microwave Theory Tech.*, vol. 58, no. 5, pp. 1438–1446, May 2010.

[12] K.-J. Koh and G. M. Rebeiz, "An X- and Ku-band 8-element phased-array receiver in 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1360–1371, Jun. 2008.

[13] K.-J. Koh, J. May, and G. M. Rebeiz, "A millimeter-wave (40–45 GHz) 16-element phased-array transmitter in 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1498–1509, May 2009.

[14] A. Natarajan, S. Reynolds, M.-D. Tsai, S. Nicolson, J.-H. Zhan, D. G. Kam, D. Liu, Y.-L. Huang, A. Valdes-Garcia, and B. Floyd, "A fully integrated 16-element phased-array receiver in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1059–1075, May 2011.

[15] S. Emami, R. Wiser, E. Ali, M. Forbes, M. Gordon, X. Guan, S. Lo, P. McElwee, J. Parker, J. Tani, J. Gilbert, and C. Doan, "A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 164–166.

[16] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A thirty two element phased-array transceiver at 60GHz with RF-IF conversion block in 90nm flip chip CMOS process," in *IEEE RFIC Symp. Dig.*, May 2010, pp. 457–460.

[17] C.-Y. Kim, D.-W. Kang, and G. M. Rebeiz, "A 44–46-GHz 16-element SiGe BiCMOS high-linearity transmit/receive phased array," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 3, pp. 730–742, Mar. 2012.

[18] S. Y. Kim, O. Inac, C.-Y. Kim, and G. M. Rebeiz, "A 76–84 GHz 16-element phased array receiver with a chip-level built-in-self-test system," in *IEEE RFIC Symp. Dig.*, Jun. 2012, pp. 127–130.

[19] C. A. Balanis, *Antenna Theory: Analysis and Design*, 3rd ed. New Jersey: John Wiley & Sons, 2005.

[20] A. Valdes-Garcia, S. Nicolson, J.-W. Lai, A. Natarajan, P.-Y. Chen, S. Reynolds, J.-H. C. Zhan, D. Kam, D. Liu, and B. Floyd, "A Fully Integrated 16-Element Phased-Array Transmitter in SiGe BiCMOS for 60-GHz Communications," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2757–2773, Dec. 2010.

[21] D. Shin and G. M. Rebeiz, "A high-linearity *X*-band four-element phased-array receiver: CMOS chip and packaging," *IEEE Trans. Microwave Theory Tech.*, vol. 59, no. 8, pp. 2064–2072, Aug. 2011.

[22] A. Siligaris, O. Richard, B. Martineau, C. Mounet, F. Chaix, R. Ferragut, C. Dehos, J. Lanteri, L. Dussopt, S. Yamamoto, R. Pilard, P. Busson, A. Cathelin, D. Belot, and P. Vincent, "A 65-nm CMOS fully integrated transceiver module for 60-GHz wireless HD applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3005–3017, Dec. 2011.

[23] K. Okada, N. Li, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, S. Ito, W. Chaivipas, R. Minami, T. Yamaguchi, Y. Takeuchi, H. Yamagishi, M. Noda, and A. Matsuzawa, "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE802.15.3c," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011.

[24] J.-L. Kuo, Y.-F. Lu, T.-Y. Huang, Y.-L. Chang, Y.-K. Hsieh, P.-J. Peng, I.-C. Chang, T.-C. Tsai, K.-Y. Kao, W.-Y. Hsiung, J. Wang, Y. Hsu, K.-Y. Lin, H.-C. Lu, Y.-C. Lin, L.-H. Lu, T.-W. Huang, R.-B. Wu, and H. Wang, "60-GHz Four-Element Phased-Array Transmit/Receive System-in-Package Using Phase Compensation Techniques in 65-nm Flip-Chip CMOS Process," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 3, pp. 743–756, Mar. 2012.

[25] Y. Atesal, B. Cetinoneri, K.-J. Koh, and G. Rebeiz, "X/Ku-band 8-element phased arrays based on single silicon chips," in *IEEE Int. Microwave Symposium MTT-S*, Anaheim, CA, May 2010, pp. 1258–1261.

[26] J. Lee, Y. Chen, and Y. Huang, "A low-power low-cost fully-integrated 60-GHz transceiver system with OOK modulation and on-board antenna assembly," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 264–275, Feb. 2010.

[27] M. Jahn, R. Feger, C. Wagner, Z. Tong, and A. Stelzer, "A four-channel 94-GHz SiGe-based digital beamforming FMCW radar," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 3, pp. 861–869, Mar. 2012.

[28] S. Hantscher, B. Schlenther, M. Hagelen, S. Lang, H. Essen, A. Tessmann, A. Hulsmann, P. Leuther, and M. Schlechtweg, "Security pre-screening of moving persons using a rotating multichannel W-band radar," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 3, pp. 870–880, Mar. 2012.

[29] A. Amadjikpe, D. Choudhury, C. Patterson, B. Lacroix, G. Ponchak, and J. Papapolymerou, "Integrated 60-GHz antenna on multilayer organic package with broadside and end-fire radiation," *IEEE Trans. Microwave Theory Tech.*, vol. 61, no. 1, pp. 303–315, Jan. 2013.

[30] J. Hacker, C. Hillman, A. Papavasiliou, C. G. Kim, A. Abbaspour-Tamijani, C. Y. Kim, D. W. Kang, and G. Rebeiz, "A 16-element transmit/receive Q-band electronically steerable subarray tile," in *IEEE Int. Microwave Symposium MTT-S*, Montreal, Canada, Jun. 2012, pp. 1–3.

[31] S. Trotta, M. Wintermantel, J. Dixon, U. Moeller, R. Jammers, T. Hauck, A. Samulak, B. Dehlink, K. Shun-Meen, H. Li, A. Ghazinour, Y. Yin, S. Pacheco, R. Reuter, S. Majied, D. Moline, T. Aaron, V. Trivedi, D. Morgan, and J. John, "An RCP packaged transceiver chipset for automotive LRR and SRR systems in SiGe BiCMOS technology," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 3, pp. 778–794, Mar. 2012.

[32] J. Hasch, E. Topak, R. Schnabel, T. Zwick, R. Weigel, and C. Waldschmidt, "Millimeter-wave technology for automotive radar sensors in the 77 GHz frequency band," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 3, pp. 845–860, Mar. 2012.

[33] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: transmitter and local LO-path phase shifting," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807–2819, Dec. 2006.

[34] Y. Atesal, B. Cetinoneri, M. Chang, R. Alhalabi, and G. M. Rebeiz, "Millimeter-wave wafer-scale silicon BiCMOS power amplifiers using free-space power combining," *IEEE Trans. Microwave Theory Tech.*, vol. 59, no. 4, pp. 954–965, April 2011.

[35] W. Shin, O. Inac, Y.-C. Ou, B. Ku, and G. Rebeiz, "A 108–112 GHz 4x4 wafer-scale phased array transmitter with high-efficiency on-chip antennas," in *IEEE RFIC Symp. Dig.*, Jun. 2012, pp. 199–202.

[36] J. May, R. Alhalabi, and G. M. Rebeiz, "A 3 G-bit/s W-band SiGe ASK receiver with a high-efficiency on-chip electromagnetically-coupled antenna," in *IEEE RFIC Symp. Dig.*, May 2010, pp. 87–90.

[37] I. Sarkas, J. Hasch, A. Balteanu, and S. Voinigescu, "A fundamental frequency 120-GHz SiGe BiCMOS distance sensor with integrated antenna," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 3, pp. 795–812, Mar. 2012.

[38] I. Sarkas, E. Laskin, A. Tomkins, A. Balteanu, E. Dacquay, L. Tarnow, S. Voinigescu, J. Hasch, P. Chevalier, and B. Sautreuil, "Silicon-based radar and imaging sensors operating above 120 GHz," in *IEEE MIKON Dig.*, May 2012, pp. 91–96.

[39] J. Hasch, U. Wostradowski, S. Gaier, and T. Hansen, "77 GHz radar transceiver with dual integrated antenna elements," in *Proc. IEEE German Microwave Conf.*, Mar. 2010, pp. 280–283.

[40] Z. Chen, C.-C. Wang, H.-C. Yao, and P. Heydari, "A BiCMOS W-band 2×2 focal-plane array with on-chip antenna," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2355–2371, Oct. 2012.

[41] K. Kang, F. Lin, D.-D. Pham, J. Brinkhoff, C.-H. Heng, Y. X. Guo, and X. Yuan, "A 60-GHz OOK Receiver With an On-Chip Antenna in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1720–1731, Sep. 2010.

[42] R. Han, Y. Zhang, Y. Kim, D. Y. Kim, H. Shichijo, E. Afshari, and O. Kenneth, "280GHz and 860GHz image sensors using Schottky-barrier diodes in 0.13 μm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 254–256.

[43] H. Sherry, J. Grzyb, Y. Zhao, R. Al Hadi, A. Cathelin, A. Kaiser, and U. Pfeiffer, "A 1kpixel CMOS camera chip for 25fps real-time terahertz imaging applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 252–254.

[44] E. Ojefors, U. Pfeiffer, A. Lisauskas, and H. Roskos, "A 0.65 THz focal-plane array in a quarter-micron CMOS process technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1968–1976, Jul. 2009.

[45] K. Sengupta and A. Hajimiri, "A 0.28THz 4×4 power-generation and beam-steering array," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 254–256.

[46] E. Preisler, G. Talor, D. Howard, Z. Yan, R. Booth, J. Zheng, S. Chaudhry, and M. Racanelli, "A millimeter-wave capable sige bicmos process with 270ghz fmax hbts designed for high volume manufacturing," in *IEEE BCTM Proc.*, Oct. 2011, pp. 74–78.

[47] *Sonnet ver. 12.56.3*, Sonnet Software, Inc., Syracuse, NY, 1986-2012.

[48] A. Mangan, S. Voinigescu, M.-T. Yang, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 235–241, Feb. 2006.

[49] S. Nicolson, K. Yau, P. Chevalier, A. Chantre, B. Sautreuil, K. Tang, and S. Voinigescu, "Design and scaling of W-band SiGe BiCMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1821–1833, Sep. 2007.

[50] B. Cetinoneri, Y. Atesal, A. Fung, and G. M. Rebeiz, "W-band amplifiers with 6-dB noise figure and milliwatt-level 170–200-GHz doublers in 45-nm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 692–701, Mar. 2012.

[51] J.-J. Hung, T. Hancock, and G. Rebeiz, "High-power high-efficiency SiGe Ku- and Ka-band balanced frequency doublers," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 2, pp. 754–761, Feb. 2005.

[52] D. M. Pozar, *Microwave Engineering*, 3rd ed. New York: John Wiley & Sons, 2005.

[53] R. Alhalabi and G. M. Rebeiz, "Design of high-efficiency millimeter-wave microstrip antennas for silicon rfic applications," in *IEEE Antennas Propag. Symp.*, Spokane, WA, USA, Jul. 2011, pp. 2055–2058.

[54] Y.-C. Ou and G. Rebeiz, "On-chip slot-ring and high-gain horn antennas for millimeter-wave wafer-scale silicon systems," *IEEE Trans. Microwave Theory Tech.*, vol. 59, no. 8, pp. 1963–1972, Aug. 2011.

[55] Y.-C. Ou and G. M. Rebeiz, "Differential microstrip and slot-ring antennas for millimeter-wave silicon systems," *IEEE Trans. Antenna Propag.*, vol. 60, no. 6, pp. 2611–2619, Jun. 2012.

[56] K.-K. Huang and D. Wentzloff, "60 GHz on-chip patch antenna integrated in a 0.13-µm CMOS technology," in *IEEE Int. Conf. on Ultra-Wideband (ICUWB)*, Sep. 2010, pp. 1–4.

[57] S. Pan and F. Capolino, "Design of a CMOS on-chip slot antenna with extremely flat cavity at 140 GHz," *IEEE Antennas and Wireless Propag. Letters*, vol. 10, pp. 827–830, 2011.

[58] J. M. Edwards and G. M. Rebeiz, "High-efficiency elliptical slot antennas with quartz superstrates for silicon RFICs," *IEEE Trans. Antenna Propag.*, vol. 60, no. 11, pp. 5010–5020, Nov. 2012.

[59] D. Pozar and D. Schaubert, "Analysis of an infinite array of rectangular microstrip patches with idealized probe feeds," *IEEE Trans. Antenna Propag.*, vol. 32, no. 10, pp. 1101–1107, Oct. 1984.

[60] *[Online] http://www.ggb.com/calsel.html*, GGB Industries, Inc., Naples, OR, USA.

[61] *[Online] http://www.thinksrs.com/products/SR810830.htm*, Stanford Research Systems, Inc., Sunnyvale, CA, USA.

[62] S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J.-O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, "Record RF performance of 45-nm SOI CMOS technology," in *IEEE Electron Devices Meeting*, Dec. 2007, pp. 255–258.

[63] ——, "From oxymoron to mainstream: the evolution and future of RF CMOS," in *IEEE Int. Workshop on RF Integ. Tech.*, 2007, pp. 1–6.

[64] O. Andrisano, V. Tralli, and R. Verdone, "Millimeter waves for short-range multimedia communication systems," *Proceedings of the IEEE*, vol. 86, no. 7, pp. 1383–1401, Jul. 1998.

[65] M. Seo, B. Jagannathan, J. Pekarik, and M. Rodwell, "A 150 GHz amplifier with 8 dB gain and +6 dBm P_{sat} in digital 65 nm CMOS using dummy-prefilled microstrip lines," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3410–3421, Dec. 2009.

[66] R. Trew, M. B. Steer, and D. Chamberlain, "Parasitic effects upon the high-frequency performance of three-terminal devices." in *3rd GaAs simulation workshop*, Oct. 1986.

[67] S. Nicolson, A. Tomkins, K. Tang, A. Cathelin, D. Belot, and S. Voinigescu, "A 1.2V, 140GHz receiver with on-die antenna in 65nm CMOS," in *IEEE Radio Freq. Integr. Circuits Symp.*, April 2008, pp. 229–232.

[68] Z.-M. Tsai, H.-C. Liao, Y.-H. Hsiao, H. Wang, J. Y.-C. Liu, M.-C. F. Chang, Y.-M. Teng, and G.-W. Huang, "A 1.2V broadband D-band power amplifier with 13.2-dBm output power in standard RF 65-nm CMOS," in *IEEE Int. Microwave Symposium MTT-S*, June 2012, pp. 1–3.

[69] K. Y. Toh, P.-K. Ko, and R. Meyer, "An engineering model for short-channel MOS devices," *IEEE J. Solid-State Circuits*, vol. 23, no. 4, pp. 950–958, Apr. 1988.

[70] K.-J. Koh and G. M. Rebeiz, "0.13-µm CMOS digital phase shifters for X, Ku- and Ka-band phased arrays," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535–2546, Nov. 2007.

[71] S. Y. Kim, D.-W. Kang, K.-J. Koh, and G. Rebeiz, "An improved wideband all-pass I/Q network for millimeter-wave phase shifters," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 11, pp. 3431–3439, Nov. 2012.

[72] A. Tomkins, R. Aroca, T. Yamamoto, S. Nicolson, Y. Doi, and S. Voinigescu, "A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2085–2099, Oct. 2009.

[73] T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi, and I. Seto, "A 60-GHz CMOS receiver front-end with frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 1030–1037, Apr. 2008.

[74] M. Varonen, M. Kaltiokallio, V. Saari, O. Viitala, M. Karkkainen, S. Lindfors, J. Ryynanen, and K. A. I. Halonen, "A 60-GHz CMOS receiver with an on-chip ADC," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2009, pp. 445–448.

[75] S. Reynolds, B. Floyd, U. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2831, Dec. 2006.

[76] J.-H. Tsai, "A 55–64 GHz fully-integrated sub-harmonic wideband transceiver in 130 nm CMOS process," *IEEE Microwave and Wireless Components Letters (MWCL)*, vol. 19, no. 11, pp. 758–760, Nov. 2009.

[77] W. Shin, M. Uzunkol, and G. Rebeiz, "Ultra low power 60 GHz ASK SiGe receiver with 3–6 Gbps capabilities," in *IEEE Compound Semiconductor Integrated Circuit Symp.*, Oct. 2009, pp. 1–4.

[78] J. Lee, Y. Chen, and Y. Huang, "A low-power low-cost fully-integrated 60-GHz transceiver system with OOK modulation and on-board antenna assembly," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 264–275, Feb. 2010.

[79] Y. Nakasha, M. Sato, T. Tajima, Y. Kawano, T. Suzuki, T. Takahashi, K. Makiyama, T. Ohki, and N. Hara, "W-band transmitter and receiver for 10-Gb/s impulse radio with an optical-fiber interface," *IEEE Trans. Microwave Theory Tech.*, vol. 57, no. 12, pp. 3171–3180, Dec. 2009.

[80] M. Uzunkol, W. Shin, and G. Rebeiz, "Design and analysis of a low-power 3–6-Gb/s 55-GHz OOK receiver with high-temperature performance," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 10, pp. 3263–3271, Oct. 2012.

[81] T. Nakamura, T. Masuda, K. Washio, and H. Kondoh, "A low-phase-noise low-power 27-GHz SiGe-VCO using merged-transformer matching circuit technique," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2007, pp. 413–416.

[82] N. Fong, J. Kim, J.-O. Plouchart, N. Zamdmer, D. Liu, L. Wagner, C. Plett, and G. Tarr, "A low-voltage 40-GHz complementary VCO with 15% frequency tuning range in SOI CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 841–846, May 2004.

[83] B.-W. Min and G. Rebeiz, "Ka-band SiGe HBT low phase imbalance differential 3-bit variable gain LNA," *IEEE Microwave and Wireless Components Letters (MWCL)*, vol. 18, no. 4, pp. 272–274, Apr. 2008.