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HIGH SPEED IMAGING WITH A TAPPED SOLID STATE SENSOR

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ABSTRACT

A high speed camera with a solid state diode array sensor is described. 500 frames/second rates are achieved by dividing the 256×256 pixel array into eight sections. The detected photocharge is tapped in parallel from each section into independent signal processing channels. The circuits for video signal extraction and processing are described and data on measured signal-to-noise ratio, sensitivity and crosstalk are presented. Image artifacts are also discussed and the effectiveness of the sensor fast clear procedure for their elimination shown.

INTRODUCTION

Solid state sensors for optical imaging, which became available in recent years, offer unprecedented distortion-free spatial resolution associated with a wide output range and linearity at excellent signal/noise ratios. These characteristics are especially desirable in telemetry, where many charge coupled devices (CCD), charge injection devices (CID) and diode array sensors are employed. Most of the devices were designed for relatively low image readout rates of 30 frames/second or less. Only few sensors were found capable of running at rates up to 500 frames/second.² High readout rates were achieved by increasing photocharge transfer clock frequencies in these devices to up to 50 MHz. Most of the sensors don't exceed 15 MHz.

Individual photosensitive picture elements (pixels) of an area sensor are organized in rows and columns along a rectangular matrix. The sequence of clock pulses enables a serial readout of individual pixel photocharge through the common output port. The video signal thus appears as a long string of pulses, representing rows and columns of pixels and with the amplitude of each pulse proportional to the photocharge integrated between the two consecutive video frames.

A reduction of video frame readout time results if the photocharge is tapped simultaneously by several parallel output ports. The camera based on such sensor is described in this paper.

The sensor is a 256×256 diode array (RA 2568N, made by EG&G Reticon) divided in 8 sections of 256×32 pixels each. The diodes are square-shaped ($40 \mu\text{m} \times 40 \mu\text{m}$) with a center-to-center spacing of $40 \mu\text{m}$. A p-n junction makes the individual photodiode, to which a MOS capacitor is added to increase the pixel photocharge capacity. Each diode is addressable by two MOS switches, one controlled by a built-in vertical scanner and the other by one of the eight horizontal registers. Each horizontal scanner controls one section of the sensor, accessible through the video signal port. If all eight sections are clocked in parallel by a 5 MHz clock, the full 256×256 pixel image is readout in less than 2 ms, i.e. exceeding the 500 frames/second rate.

Fig. 1 is the sensor block diagram, showing four sections of photodiode arrays (PDA). Each section is organized in a matrix of 64 vertical columns, each containing 256 photodiodes. Even and odd numbered columns are separately controlled by two sets of four horizontal scanners (HS1-HS7 and HS2-HS8). Odd and even scanners are independently advanced through 32 steps by sets of complementary clocks (X_1, X_2 and X_3, X_4), addressing in turn the diodes of the horizontal row. Column gate FET switches connect the addressed photodiodes to the video output ports. The scanners are advanced by four additional steps, creating video lines of 32 active and 4 dummy pixels. The start pulses (ST0 and STE) initiate the scanning of each line.

The vertical scanner, advanced by a pair of complementary clocks (Y_1, Y_2), changes the address of the horizontal diode row before the horizontal scanner starts a new line. Also, the photocharge of the addressed row of diodes is transferred at

this time to the column gates for readout by the alternating pair of pulses A (even lines) and B (odd lines). Thus the vertical scanner needs 128 steps to address all 256 diode lines of the sensor. In addition to 256 active lines, the scanner generates additional 4 dummy lines, one before, and three after the beginning of each video frame. A signal (EOF) is generated by the vertical scanner at the end of each video frame, and can be used for the readout synchronization. A scan cycle can be interrupted and the scanner reset at any time by holding both Y clock inputs at the low level.

The total sensor photocharge can be dumped quickly at any time by the reset clock pulses (LR, FR and FRD). All photodiodes are discharged simultaneously to the external reference voltage (LRD). A more detailed diagram of two sensor sections containing 256 rows of 64 diode columns (32 even and 32 odd) is shown in Fig. 2. It shows in detail how the individual photodiodes are accessed. Each vertical scanner step controls the access gates of two diode rows. The pulse A turns on the row of odd MOS switches through the gate GA connecting briefly the photodiodes to the adjacent collecting line running vertically along the column. These lines serve as a temporary charge storage capacitors, which are in turn connected one by one to the video output line by the horizontal scanners. The scanner clock inputs are independent, allowing the readout of even and odd photodiode columns either simultaneously or in quadrature. The clocking scheme depends on the method of video signal processing and the rate of horizontal scanning.

The timing sequence of clock pulses driving the sensor is shown in Fig. 3. The sensor is readout continually until the external reset pulse (line A) stops the vertical clocks (line F, G), holding them low for the duration of the reset extension time (line B). During this period the whole sensor is cleared of all photocharge by a sequence of three reset clock pulses (lines C, D and E). Also, the vertical scanner is initialized and stays in this state until the end of the reset extension time. This is also the time for the image integration in the photodiodes of the sensor. For the imaging of pulsed light sources or fast decaying phosphors, the readout should not start until the photon emission has subsided to a negligible level.

The video frame readout starts with four inactive (dummy) lines followed by 128 steps of the vertical scanner (lines F, G). During each step two video lines are addressed, as described earlier. The even line is strobed by the clock A, and the odd

line by the clock B (lines H, I). After each strobe, which transfers the line photocharge into the column storage, the horizontal scanners are initialized (X_{st}) and then clocked by 36 pairs of X pulses per video line (lines J, K, L). Therefore each video line has 32 active pixels and 4 dummy ones (line M). Both even and odd columns are read out in phase if all horizontal scanners are advanced by the same set of X clock. Another set of X clocks, delayed by one half of period, is required to drive the even and odd horizontal scanner in quadrature.

500 FRAMES/S CAMERA DESCRIPTION

In order to read out each sensor section of 256×32 pixels in 2 ms, reasonably low frequency of 5 MHz is required to advance horizontal scanners. However, relatively large charge readout time constant and substantial crosstalk noise from clock transitions superimposed on the photocharge are limiting factors even though the scanners could run at a higher frequency. Fast ECL logic circuits were used for generating proper clock sequences of the camera. Such circuits allow the change in readout time over a large range merely by changing the frequency of externally provided variable reference source. Also, the phase difference between the clock pulse edges can be precisely adjusted for minimum crosstalk and does not change much afterwards with the change in reference frequency.

The basic camera blocks and supporting instrumentation used in the prototype evaluation is shown in Fig. 4. Internal 5 MHz reference clock drives the camera logic for frame readout time of 2 ms. It can be replaced by an external source if variable frame rate readout is needed for the camera testing. The logic circuits control specially designed fast clock drivers producing 13 volt pulses required by the sensor. Also the appropriate bias voltages are supplied to the sensor. Four each even and odd video signals are processed by two quad gated video amplifiers.

The video signal is first inverted in a preamplifier (gain of eight) and then amplified ten times in the main amplifier. The amplifiers are gated externally by the horizontal clock frequency triggered pulse generator. The strobe pulses to the odd amplifier section are delayed by one half of the clock period so that the amplifier outputs are in quadrature. The outputs of each even-odd amplifier pair are combined into a single video output and available through a 50-ohm line driver. The video signal line is thus shaped into a sequence

of 64 even-odd pulses with amplitude proportional to the recovered photocharge. The pixel readout rate is thus doubled to 10 MHz.

In order to test the camera prototype with the strobed light, the frame readout rate is reduced. A pulse generator is then triggered by such low rate pulses in synchronism with the camera. The pulse generator delayed output can trigger the calibrated xenon flash at any time within the video frame. The efficiency of photocharge readout and the magnitude of crosstalk between the sensor sections can be studied, both spatially and temporally, by projecting a test pattern or a pinhole on the sensor surface.

PHOTOCHARGE READOUT CONSIDERATIONS

The image pixel size is defined by the photodiode size of $40 \times 40 \mu\text{m}$. During the integration time the photocharge is accumulated in a MOS capacitor attached to each photodiode to increase pixel saturation capacity. Each pixel photocharge can be accessed through two MOS switches, S_v and S_h , controlled by the vertical and the horizontal scanners of the sensor (Fig. 5). The switch S_v is open during the integration time. The voltage across the pixel storage capacitor C_d containing the accumulated photocharge, q at the end of the integration period is $V_d = q/C_d$. When the pixel's row is addressed by the vertical scanner, S_v is turned on for a short time by the pulse A (or B), transferring the charge from the storage capacitor through the switch serial resistance R_c into the storage capacitance C_c of the connecting vertical video line. The switch S_v should be on sufficiently long to let settle the voltage across C_c :

$$V_c = q(1 - e^{-t/A}) / (C_d + C_c); A = R_c C_c C_d / (C_c + C_d)$$

If the strobe pulse A width exceeds the charging time constant A more than five times, the voltage will be approximately $V_c = q / (C_c + C_d)$. The photocharge remaining in C_c after the switch is turned off will be less than q : $q_c = q C_c / (C_d + C_c)$. The charge in C_c waits its turn to be switched by the horizontal scanner controlled switch S_h to the video readout line. To the line capacitance C_1 the capacitance C_i of the preamplifier and stray capacitance of the connecting wires is added. The shunt resistor R_1 defines the discharge time constant and is for the moment considered large in comparison with the serial switch resistance R_1 . Upon the closing of the switch, the output voltage increases as

$$v_1 = q_c(1 - e^{-t/B}) / (C_c + C_1 + C_i);$$

$$B = R_c C_c (C_c + C_1) / (C_c + C_c + C_1)$$

where B is the line charging time constant. The stationary pixel output voltage is then $V_1 = q C_c / (C_c + C_1 + C_i)(C_c + C_d)$. The switch S_h is closed for the duration of the pixel clock time when the video line must be discharged through R_1 . The discharge voltage v_d decreases approximately as

$$v_d = V_1(1 - e^{-t/D}); D = R_1(C_c + C_1 + C_i)$$

The voltage waveform of one illuminated pixel at the amplifier output is shown in Fig. 6. The leading edge time constant B and the trailing edge time constant D read 30 ns and 160 ns, respectively. With the external discharge resistor $R_1 = 3.3 \text{ k ohms}$, the calculated total value of video line capacitance $C_c + C_1 + C_i$ is approximately 50 pF.

TESTS WITH STROBED AND CONTINUOUS LIGHT

A 1 mm diameter pinhole was focused onto the sensor surface and strobed by a xenon flash source. One video line (with 32 active and 4 dummy pixels is shown in Fig. 7a. The noninverting amplifier with a gain of 10 (Fig. 5) and pixel discharge time constant of 160 ns (Fig. 6) produced signal amplitude of 160 mV across the 100-ohm load. Sharp clock pulse transition crosstalk signal is clearly visible. It subsides well before the pixel signal peak is reached. Since the peak height occurring 50 ns later is proportional to the recovered photocharge, the crosstalk can be separated from the signal.

The signal amplitude is about 12% below saturation level. The light intensity, increased by a factor of 13, saturated the signal at 180 mV level (Fig. 7b), did not cause excessive blooming. Fig. 7c shows the signal when the light was attenuated 10 times from the level used in Fig. 7a.

A substantial amount of unwanted photocharge is generated in the vertical read out lines running along each column. Fortunately, this charge can be quickly dumped by applying a line reset pulse prior to the start of the pixel charge readout. If not eliminated, the line generated "ghost" image appears in the first video line immediately after the flash.

The "ghost" image of the pinhole image, Fig. 7, is shown in Fig. 8a. Individual video lines are clearly separated by crosstalk transients coinciding with the four dummy pixels of each line. The flash occurred at the beginning of the second video line. The circular 1 mm diameter pinhole image covers vertically 26 video

lines, spaced by $40\text{ }\mu\text{m}$. Only 13 pixels per line are seen in Fig. 7 since only even-numbered pixels are shown. Consequently, the whole ghost image is collapsed into a single line. In the case of circular pinhole image as shown, the envelope of the ghost line signal is sinusoidal.

The ghost charge may be too large to be cleared out during the readout of only one line. It took 6 lines to clear the ghost image in Fig. 8a, because the pixel readout time is not long enough, i.e. the horizontal scanner switches on the next pixel before the full discharge of the preceding one. The total ghost magnitude of the highest center pixel is 1.2 V and the amplitude of the same image pixel (Fig. 7a) is 120 mV. Since there are 26 pixels illuminated in this column, their combined amplitude would be 3.12 V. Hence, the image-to-ghost photocharge ratio is 2.6.

The Fig. 8a flash intensity was 90 percent off the pixel saturation level. In Fig. 8b the intensity was increased 4 times, driving the amplifier to saturation at 4.5 V amplitude of the first ghost line. The discharge of the whole ghost image took more than six video lines. Since there is no charge limiting provision implemented in the sensor itself, very large signals can be recovered. For instance, the device may be used as a linear sensor with a greatly expanded dynamic range. Also, when imaging at very high frame rates, the readout of the ghost image can quickly determine if there is an image stored worth reading. If not, the frame can be immediately reset and the new frame readout attempted. Much higher image processing rates may result along with the saving in the storage and processing hardware.

The sensitivity of the camera was tested with a xenon light source calibrated to $2.462\text{ }\mu\text{J}/\text{cm}^2$ per flash through a 570 nm bandpass filter. A video signal of 160 mV (Fig. 7a) was obtained by attenuating the light 50 times with a neutral density filter. The signal saturation, found at the 180 mV level is then reached at an exposure of $0.14\text{ }\mu\text{J}/\text{cm}^2$.

In order to demonstrate the sensor operation, a fast oscilloscope was used as a high frame rate video monitor. The horizontal time base was synchronized with the frame start and the vertical input driven by a ramp voltage derived from the video line pulses. The beam intensity was

modulated with the video signal. A test pattern slide was projected on the sensor. Fig. 9 shows one full frame and the beginning of the next one, indicating a rate of 530 frames/s. Only one quarter of the sensor is shown, with even and odd pixels combined (64 vertically and 256 horizontally).

CONCLUSION

Very high frame rate solid state video camera using the RA2568N diode sensor array divided into eight individually tapped sections was built and tested. Considered are the best ways of clocking the charge transfer switches to minimize the interference in recovering the photocharge and find limits in pixel readout rates. Methods in processing the video signal were studied in order to optimize the signal to noise range and fixed noise pattern. The results show that current 530 frames per second rate can be exceeded with some increase in complexity of signal processing hardware. The "ghost" image, normally an unwanted artifact, can be found useful in turning the device into a very high dynamic range linear sensor, or for image "preview" for video frames worth saving.

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Fig. 7 a) Even video line with a strobed pinhole image, 12% below saturation; b) same line saturated with 2.5 higher light intensity; c) video line attenuated with ND1 filter.

8 a

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Fig. 9 Live display of a bar test slide with continuous light at 530 frames/s on oscilloscope modified as fast video monitor.

8 b

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Fig. 8 a) "Ghost" of pinhole image in Fig. 7, generated in vertical charge transport lines of the sensor. The discharge takes several video lines, depending on the exposure intensity; b) light intensity increased 4 times drove the amplifier to saturation at 4.5 V.

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