UNIVERSITY OF CALIFORNIA SAN DIEGO

High-sensitivity Current Sensing Front-End for Biomedical Applications

A Dissertation submitted in partial satisfaction of the requirements
for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Da Ying

Committee in charge:

Professor Drew A. Hall, Chair
Professor Gert Cauwenberghs
Professor Tzu-Chien Hsueh
Professor Yu-Hwa Lo
Professor Patrick Mercier

2022

The Dissertation of Da Ying is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2022

DEDICATION

This thesis is dedicated to my parents, Lixia Li and Yiming Ying.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

With full disclosure, I first started my Ph.D. at UCSD with a major in nanodevice. But then I discovered my interest in integrated circuits from Prof. Hall's lectures, so I decided to change my path in my first year. Countless times had my mind wandered back to the moment I anxiously stepped into Prof. Hall's office, hoping he would sign my transfer petition. "Sure, I will sign. But this does NOT mean you are with the group yet. You need to prove yourself." At the time, I was put under a lot of pressure by that last statement. Only later did I realize that was actually a professor's way of supporting and motivating students to perform with a sense of purpose. To use a stale analogy - if the research group (BioEE) is a rocket ship, Prof. Hall is the captain who pilots it to maximum momentum with his academic rigor and good-humored personality!

There is something about the people in BioEE that glues everyone as a whole, both academically and socially. Things such as self-organized journal club, and frisbee on Pacific Beach, are just not something you find a typical research group would spend the time on. I thank each one of them – Xiahan, Haowei, Iric, Corentin, Michael, Josh, Somok, Aditi, Omid, Tyler, Saeromi, Naveen, Mathew, Edwin, and Alex – for the rigorous technical discussion as well as the off-work good times we shared throughout the years. Thank you for making our lab such an enjoyable place, a truly admirable thing to achieve, especially when there was not a single window.

I will be dishonest if I say there was no hardship over the six years because there have been ups and downs that fundamentally affected me. Naturally, I'm not a sociable person but it was during the hard times when I thankfully realized the few I do have are the ones to keep for

life. Such brief acknowledgment is merely a minor token of my immense gratitude – Chenxi, Eddy, Tony, and Kidd – to say the least, my life becomes more meaningful with your presence in it.

I have always believed the strongest feeling needs not to be spoiled by words. Since I was a child, I have not been the one who knows how to express terms of endearment to his most loved ones. This is particularly true when it comes to my interaction with my parents. There had been a phase of me when I thought thanking parents in any public forum was cliché and cringy. My younger self would have been proud of the idea to remark something funny in the dedicated section, just trying to act aloof and different. But when the time actually came, I could not think of a second-best thing to say. Because I am certain this is the only one-liner that can stand the test of time no matter what.

In the following, I will acknowledge several of my collaborators for their tremendous contributions to several of my published work.

Chapter 1, in part, is based on the material from Da Ying and Drew A. Hall, "Current Sensing Front-Ends: A Review and Design Guidance," *IEEE Sensors*, vol. 21, no. 20, Oct. 2021. The dissertation author was the primary investigator and author of this paper.

Chapter 2, in part, is based on the material from Da Ying, Chi-Yang Tseng, Ping-Wei Chen, Yu-Hwa Lo, and Drew A. Hall, "A 30.3 fA/√Hz Biosensing Current Front-End with 139 dB Cross-Scale Dynamic Range, *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, vol. 15, no. 6, Dec 2021. The dissertation author was the primary investigator and author of this paper.

Chapter 3, in part, is based on the material from Da Ying, Joshua Rosenberg, Naveen K. Singh, and Drew A. Hall, "A 26.5 pArms Neurotransmitter Front-End with Class-AB Background Subtraction," *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, In Press. The dissertation author was the primary investigator and author of this paper.

Da Ying

Santa Clara, California

July 2022

VITA

2015 Bachelor of Engineering in Electrical Engineering, Vanderbilt University

2022 Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego

PUBLICATIONS

Da Ying, Joshua Rosenberg, Naveen K. Singh, and Drew A. Hall, "A 26.5 pArms Neurotransmitter Front-End with Class-AB Background Subtraction," *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, In Press.

Da Ying, Chi-Yang Tseng, Ping-Wei Chen, Yu-Hwa Lo, and Drew A. Hall, "A 30.3 fA/√Hz Biosensing Current Front-End with 139 dB Cross-Scale Dynamic Range," *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, vol. 15, no. 6, Dec 2021.

Da Ying and Drew A. Hall, "Current Sensing Front-Ends: A Review and Design Guidance," *IEEE Sensors*, vol. 21, no. 20, Oct. 2021.

Da Ying, Ping-Wei Chen, Chi Tseng, Yu-Hwa Lo, and Drew A. Hall, "A Sub-pA Current Sensing Front-End for Transient Induced Molecular Spectroscopy," *IEEE Symp. on VLSI Circuits*, Kyoto, Japan, Jun. 11-13, 2019.

Chih-Cheng Huang, Xiahan Zhou, **Da Ying**, and Drew A. Hall, "A GMR-Based Magnetic Flow Cytometer Using Matched Filtering," *Proceedings of IEEE Sensors*, Glasgow, Scotland, Oct. 30 – Nov. 1, 2017.

ABSTRACT OF THE DISSERTATION

High-sensitivity Current Sensing Front-End for Biomedical Applications

by

Da Ying

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2022

Professor Drew A. Hall, Chair

Sensors link the physical and electronic worlds, making them useful in environmental, automotive, industrial, communication, and medical applications, among many more. In the first chapter of this dissertation, current sensors and current-sensing front-ends are reviewed, aiming to provide readers with all-around design guidance from both sensor and circuit

perspectives. Starting from the transduction method, capacitive, resistive, diode/FET-based, and MEMS sensors are individually reviewed with a focus on applications, circuit models, and nonidealities that must be considered for front-end design. This is followed by a discussion of current-sensing front-ends, specifically transimpedance amplifiers (TIAs), current conveyors (CC), and current-mode delta-sigma (I-ΔΣ) modulators. Each front-end is analyzed in terms of gain, bandwidth, stability, noise, and general design considerations are presented. In this chapter, state-of-the-art works for each front-end are also summarized, and tradeoffs between different architectures are discussed. The following chapters describe two application-specific current front-ends.

In Chapter 2, a novel label- and immobilization-free biosensing technique, transient induced molecular electronic spectroscopy (TIMES), was introduced. An 8-channel array of low-noise (30.3 fA/√Hz) current sensing front-ends with on-chip microelectrode electrochemical sensors was proposed to observe real-time protein-ligand interactions. The analog front-end (AFE) consists of a 1st-order continuous-time delta-sigma (CT-ΔΣ) modulator that achieves 123 fA sensitivity over a 10 Hz bandwidth and 139 dB cross-scale dynamic range with a 2-bit programmable current reference. A digital predictor and tri-level pulse width modulated (PWM) current-steering DAC realize the equivalent performance of a multi-bit ΔΣ in an area- and power-efficient manner. The AFE consumes 50.3 μW and 0.11 mm^2 per readout channel.

In Chapter 3, an AFE for fast-scan cyclic voltammetry (FSCV) with analog background subtraction using a pseudo-differential sensing scheme to cancel the large non-faradaic current before seeing the front-end. As a result, the AFE can be compact and low-power compared to conventional FSCV AFEs with dedicated digital back-ends to digitize and subtract the

background from subsequent recordings. The proposed AFE, fabricated in a 0.18-µm CMOS process, consists of a class-AB common-mode rejection circuit, a low-input-impedance current conveyor, and a 1st-order I-ΔΣ modulator with an infinite impulse response quantizer. This AFE achieves an effective dynamic range of 83 dB with a state-of-the-art 39.2 pA_{rms} input-referred noise loaded with a 1 nF input capacitance (26.5 pA_{rms} open-circuit) across a 5 kHz bandwidth while consuming only 3.7 µW. This design was tested with carbon-fiber microelectrodes scanned at 300 V/s using flow-injection of dopamine, a key neurotransmitter.

Chapter 1. CURRENT SENSING FRONT-ENDS

1.1 Introduction

Sensors are ubiquitous in nearly all aspects of our daily life ranging from environmental and industrial to medical applications. They serve as the gateway for humans and machines to gain awareness and understand the environment from a macroscopic down to a microscopic level. In addition to the sensor that captures the signal of interest, one also needs a front-end to record and process it. A well-engineered acquisition system can be challenging to realize as it requires designers to have a deep understanding of both the sensor and circuit – two very different skill sets. This paper aims to bridge this gap by reviewing different types of sensors and circuit design considerations for front-ends and providing readers with practical knowledge on how to design a front-end for their sensor.

The fundamental principle of a sensor is the ability to transduce an external stimulus into an electrical signal. Among which, current-output sensors refer to the subset of sensors whose output signal is a current. In this paper, current-output sensors are referred to as "current sensors" for simplicity. However, readers should note that current sensors might refer to the sensors that measure a current outside the scope of this paper. Based on the underlying transduction method, current sensors are categorized into four main types, *i.e.,* capacitive [1]–[11], resistive [12]–[23], diode/FET-based [24]–[31], and microelectromechanical system (MEMS) sensors [32]–[38], as shown in Fig. 1.1. For both capacitive and resistive sensors, they are typically biased at a constant voltage such that a current signal is generated from a change in sensor impedance due to stimuli (*e.g.*, temperature [13], humidity [4], or biomolecular interaction [10]). On the other hand, diode- and FET-based sensors work by lowering a semiconductor barrier in response to stimuli. Classic

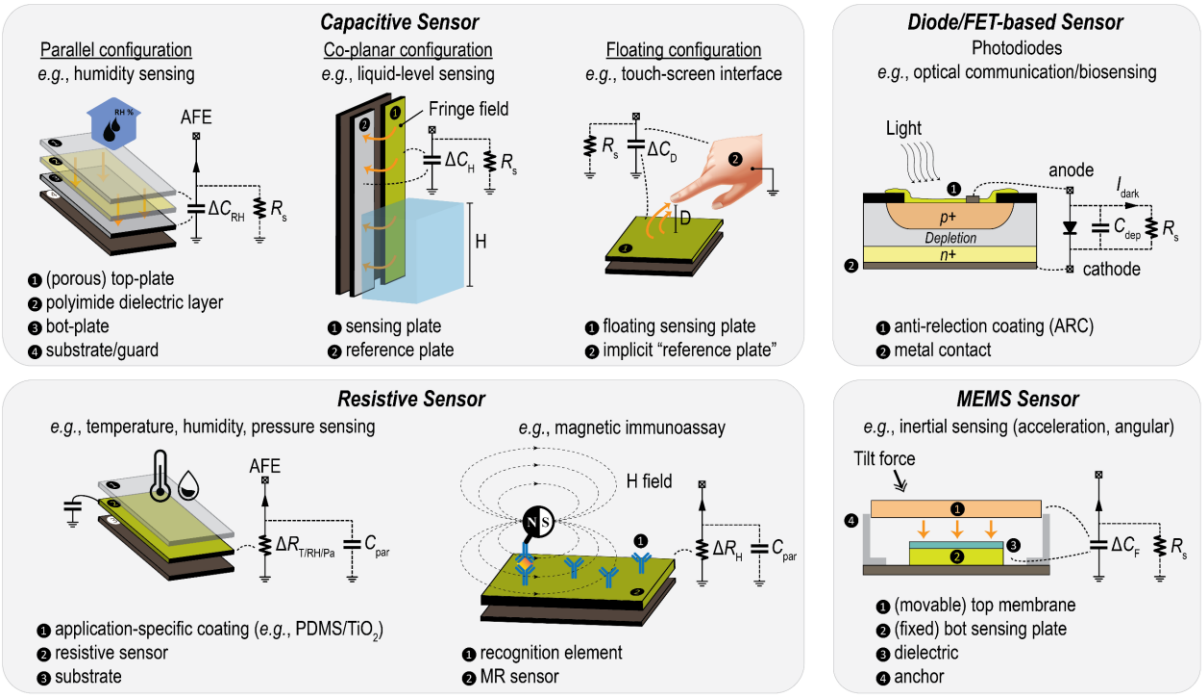


Figure 1.1 Examples of current sensors and their applications.

examples of this type of sensors are photodiodes [27], [39] and ion-sensitive field-effect transistors (ISFETs) [26]. Finally, MEMS sensors, while often capacitive, require much different design considerations than conventional capacitive sensors and therefore deserve their own discussion.

To interface with the sensor, an analog front-end (AFE) typically consists of an amplifier, some filtering, and an analog-to-digital converter (ADC). In a current-sensing AFE, the sensor output is converted to a voltage by a transimpedance amplifier (TIA), time by a current-to-frequency converter (*I*-to-*F*), or interfaced with current-mode circuits to avoid the need for an explicit transimpedance element. Typical current-mode circuits include current conveyors (CC) and current-mode delta-sigma (I-ΔΣ) modulators. Each of these front-ends has a constellation of performance tradeoffs, including bandwidth, noise, power, and input impedance, among others. Choosing and designing the appropriate readout circuit is critical to achieving high performance from any sensor. Even though there are many other semiconductor technologies, such as bipolar junction transistors (BJT) or bipolar CMOS (BiCMOS), they are far less commonly used and prone

to issues such as large input bias current. Therefore, this chapter discusses front-end designs of integrated and discrete CMOS implementations.

1.2 Sensors Overview

1.2.1 Capacitive Sensors

Capacitive sensors are used in a wide range of applications, including liquid level sensing [1], [2], environmental sensing (gas [3], humidity [4], etc.), touch interfaces [5], [6], material analysis [7], and life science applications [8]–[10]. Capacitive sensors are formed by two conductive electrodes separated by a dielectric where the stimuli modulate the material properties, as shown in Fig. 1.1. For example, polyimide is an insulating material with a dielectric constant dependent on humidity, thus can modulate the capacitance at different humidity levels. The high electric field between the parallel plates allows capacitive sensors to have very high sensitivity. Several other capacitive sensor geometries, such as co-planar and floating structures, exploit the principle of fringe capacitance – a consequence of the fringing electric field at the edge of a conductor. In a co-planar configuration, the two electrodes are arranged side-by-side (or interdigitated) in the same plane. In this way, the electric field lines are more dominant near the edges between the electrodes such that this type of sensor has high sensitivity along the z-axis, enabling applications ranging from liquid level sensing [1] to molecular sensing (e.g., bacteria growth monitoring [8], neurotransmitter detection [9], cell culture monitoring, and drug testing [10]). The electrode placement remains the same in a floating configuration; however, the second electrode is instead implicitly defined by a grounded medium that can be, for example, the culture solution for living cell monitoring [11], as shown in Fig. 1.2(a), or a fingertip for touch display applications [5], [6]. Unlike the parallel-plate capacitance, the fringe capacitance is non-linearly

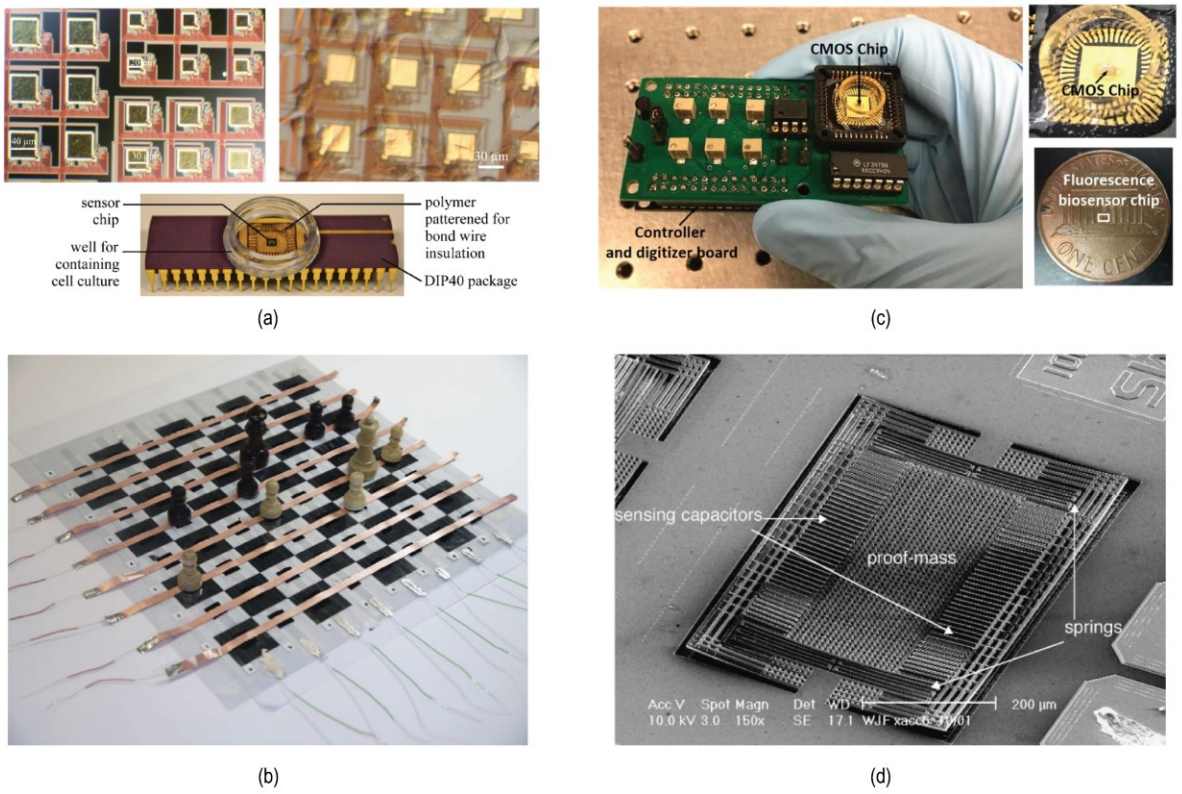


Figure 1.2 Examples of current sensing systems based on sensor types: (a) a capacitive sensing platform used to monitor the *in-vivo* proliferation of breast cancer cells [11], (b) a prototype chess board with an ultra-sensitive resistive pressure sensor based on a microstructured conducting polymer thin film [15], (c) the first single-chip fluorescence-based biosensor with integrated nanoplasmonic filters [39], and (d) scanning electron microscope (SEM) image of an ultra-sensitive capacitive MEMS accelerometer [32].

related to the sensor area, often necessitating finite element modeling (FEM) and geometric optimization.

In electrochemistry, an electrode submerged in an electrolyte has an electrode-electrolyte interface modeled as a double layer capacitance, C_{dl}, which is a series combination of the Stern layer and diffuse layer capacitors [40]. The capacitance per unit area is very high (~1 pF/µm^2), with sensor areas that are often several square millimeters resulting in large capacitances. This capacitance is in parallel with a charge transfer resistance, R_{ct}, that is all in series with the solution resistance, R_s, as shown in the abstract figure. The signal from C_{dl} can be non-faradaic, faradaic, or a combination of both, as in the case of fast-scan cyclic voltammetry (FSCV), a technique with high temporal resolution used to study neurotransmitters [41]. In a non-faradaic process, the

current is a direct result of charging or discharging the capacitor, *i.e.* $i = C\,dV/dt$, whereas in a faradaic process, ions transfer electrons during a reduction-oxidization (redox) process at the electrode-electrolyte interface resulting a current proportional to the analyte concentration.

The sensitivity and dynamic range (DR) are important parameters to define when designing a capacitive sensor AFE. Since the change in capacitance (ΔC) may be orders of magnitude smaller than the nominal capacitance (C_0), this often requires a capacitive AFE to have a DR of more than 40 dB and, in some cases, upwards of 100 dB. In addition, any form of a capacitance-to-current front-end must be concerned with the stray capacitance at the input node because it can significantly affect the bandwidth, stability, and noise performance of the system. This stray capacitance can come from packaging, connections between the sensor and front-end on the PCB, and/or the sensor itself.

1.2.2 Resistive Sensors

Resistive sensors have been reported for environmental monitoring applications including temperature [12]–[14], pressure [15], [16], [23], and gas sensing [17], [18], as well as biosensors for proteomics [19] and lab-on-chip platforms [20]–[22]. Among them, resistor-based temperature sensors, or thermistors, are made with metal oxides with large temperature coefficients. Resistive pressure and gas sensors are based on piezo-resistive and chemo-resistive effects, respectively. For pressure sensors, a polydimethylsiloxane (PDMS) elastomer doped with conductive composites such as graphene and carbon-nanotubes has been recently reported to increase the sensitivity [16], [23]. Fig. 1.2(b) shows an example of a resistive pressure sensor array that achieves 1 Pa sensitivity using a modified polymer thin film. The key challenge for pressure sensors has been achieving high sensitivity across a large pressure range. Similarly, in sensing gas, highly conductive metal electrodes (*e.g.*, Pt) are generally modified by acceptor coating materials (*e.g.*, TiO_2 for sensing

H_2) for high selectivity. Compared to their capacitive counterpart, resistive gas sensors are less sensitive to parasitic capacitance but suffer from temperature and humidity drift [42].

Examples of magnetic sensors used for current sensing are Hall-effect and magnetoresistive (MR) sensors [43]. Sensing using a magnetic field has enabled Hall-effect sensors to be widely employed in non-contact current monitoring, position sensors, and automotive applications. For MR sensors, the sensor resistance is a function of the applied magnetic field. They have been used as the read head in rotating hard disk drives and recently biosensors to detect biomolecules labeled with magnetic nanoparticles (MNPs) [44], [45]. Since biological samples are intrinsically non-magnetic, MR biosensors achieve very high sensitivity. However, the need for an external magnetic field (*e.g.*, magnet, electromagnet, etc.) generally makes such platforms bulky.

Although resistive sensors can be easily arranged in a differential configuration (*i.e.,* Wheatstone bridge), they often have a sizeable sensor-to-sensor mismatch and still require front-ends to have large DR (>40 dB) to compensate. Worse yet, in applications such as MR biosensing, the presence of an external field leads to a large baseline-to-signal ratio ($R_0/\Delta R$) and requires an even larger DR (>80 dB). In cases where a signal pattern is predicable, signal processing techniques such as matched filtering can increase detection efficiency [46]. On the other hand, noise peaking concerns for resistive sensor front-ends are less significant due to lower input capacitance.

1.2.3 Diode/FET-based Sensors

Diode- and FET-based sensors are semiconductor devices that modulate their conductance in response to stimuli, often non-linearly. Among which, photodiodes (PD) generate currents due to the presence of light and are often used for communication [47]–[49], automotive [50], [51], and biosensing (*e.g.*, SPR [28], ELISA [29], [31]). Optical sensing is typically complicated and

bulky as it requires a multitude of external optical elements such as lasers, lenses, filters, or photo-multiplier tube (PMT) detectors. However, Hong *et al.* demonstrated an optical biosensing system (Fig. 1.2(c)) with integrated waveguide-based filters in a standard CMOS technology [39], opening a promising landscape for compact optical sensing systems. Among FET-based sensors, ISFETs are an electrochemical biosensor that modulate the channel conductance based on charged species present at the gate electrode. ISFETs have been reported for the detection of DNA hybridization [24] and immunoassays [25], but they are mostly used as pH sensors [26].

Unfortunately, both PD and ISFET experience large sensor mismatch and temperature dependency, making a pseudo-differential architecture less effective at canceling the common-mode variation. Worse yet, the sensitivity and DR of a PD are typically limited by the dark current. In image sensors, signal-processing techniques such as spike-based encoding are used to recover the DR [52]. The parasitic capacitance of a PD heavily depends on the process and how the *pn* junction is implemented [53]. Although it can be small (0.2 to 0.5 pF [54]), the PD capacitance can seriously complicate the front-end design for high-speed applications.

1.2.4 MEMS Sensors

MEMS sensors are often treated as a subset of capacitive sensors. However, the design considerations for MEMS are very different from the ones for general capacitive sensors described earlier since MEMS sensors target an entirely different set of applications, such as accelerometers [32]–[35] and gyroscopes [37], [38]. In MEMS sensors, as illustrated in Fig. 1.1, one side of the capacitor plate is movable under an exerted force to change the sensor's inertial state. The plate's movement alters the electric potential between plates; therefore, it can be measured as a change in capacitance.

Negative feedback (*e.g.*, TIA, I-ΔΣ) improves linearity and lowers sensitivity to process, voltage, and temperature (PVT) variation; however, it is particularly challenging to introduce another feedback in a MEMS system due to the existing feedback in a typical accelerometer or gyroscope which is used to control the proof mass position of the sensing element [34]. The system dynamics require careful attention to not cause instability. MEMS sensors are mostly fabricated through specialized micromachining processes (*e.g.*, surface micromachining in Fig. 1.2(d)) and connected to front-ends through wire bonding or flip-chip techniques, which can cause large parasitic capacitance on the order of a few pF. As will be discussed later, large input capacitance for a current front-end can cause more noise and even stability issues.

1.3 Transimpedance Amplifier

1.3.1 Overview

TIAs have been widely investigated and employed for optical receivers [55]–[59], biosensing [60]–[63], and many other applications due to their simplicity and a reasonable trade-off between design parameters such as noise, bandwidth, and power [39]. A TIA converts the current into a voltage signal with a transimpedance element, either a resistor or capacitor, known as a resistive-TIA (R-TIA) capacitive-TIA (C-TIA), as shown in Fig. 1.3. The reason behind such

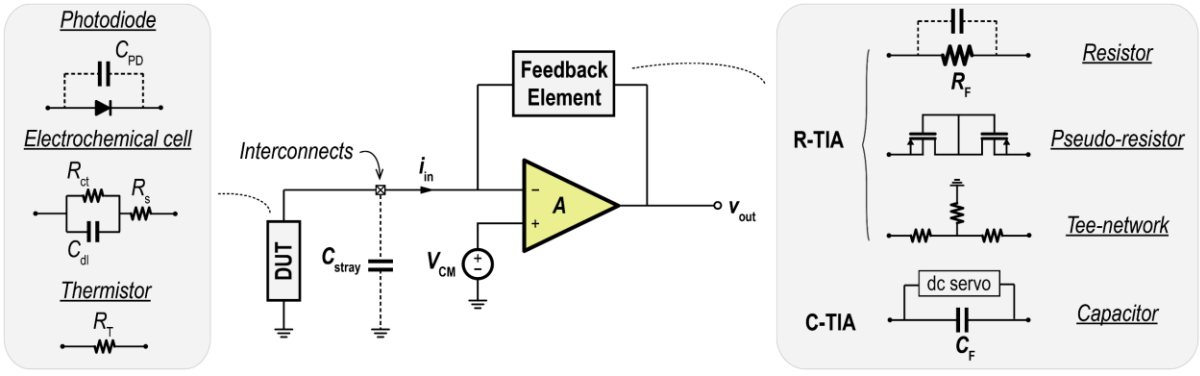


Figure 1.3 Transimpedance amplifier with different feedback configurations and input sensor models.

I-to-*V* conversion is that signal processing (*e.g.*, filtering, digitization, etc.) is traditionally done in the voltage domain.

In a traditional R-TIA, a resistor, R_F, is connected in feedback between the inverting and output nodes of an amplifier while the non-inverting terminal is driven to a potential, V_{CM}, that also biases the sensor, as shown in Fig. 1.3. There is usually also a feedback capacitor (explicit or parasitic) connected in parallel with R_F that determines the TIA's stability and band limits the signal. The amplifier's non-inverting input is also connected to the sensor, known as the device under test (DUT). This node is often referred to as a "*virtual ground*" since the negative feedback ensures minimal voltage perturbation. The current signal from the DUT, i_{in}, flows through R_F, whose value, when the amplifier's open-loop gain is much greater than unity, determines the total transimpedance gain. The output voltage, v_{out}, is simply related to the input current as: $v_{out} = V_{CM} \pm i_{in}R_F$, with the sign depending on whether the DUT is sinking (+) or sourcing (-) current. Having a virtual ground at the input node means one has full control over the sensor voltage, which can be helpful in, for example, electrochemical impedance spectroscopy (EIS), where the DUT is excited with a sinusoidal voltage and the impedance calculated by reading the resulting in- and quadrature-phase current. Many advantages of the R-TIA stem from the fact that it is a closed-loop system. Negative feedback around the amplifier ensures a constant transimpedance gain and makes it insensitive to the amplifier's open-loop gain variation. It can also be easily shown that the negative feedback reduces the input impedance, which is desirable for a current front-end, while simultaneously lowering the output impedance, which is desirable for a voltage output.

1.3.2 Gain, Bandwidth, and Stability

While a TIA structure is relatively straightforward, contradicting design requirements such as high gain, large bandwidth, and low noise make designing a TIA a non-trivial task. Since increasing the gain usually has the opposite effect on the bandwidth and stability, the three parameters must be considered together during the design process. As shown in Fig. 1.3, the total input capacitance, C_{IN}, is the parallel combination of the sensor capacitance (photodiode, C_{dl}, etc.) and the total stray/parasitic capacitance, C_{stray}, from the amplifier input and routing interconnects. The amplifier has a single-pole response $A(s) = A_0/(1 + s\tau_A)$ where A_0 is the dc gain and τ_A is the *RC* time constant for the internal pole at frequency, f_A, *i.e.* $\tau_A = 1/(2\pi f_A)$. The closed-loop transimpedance frequency response, $Z_T(s)$, can be derived as [64]

$$Z_T(s) = -R_T \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{1.1}$$

$$R_T = R_F \frac{A_0}{A_0 + 1} \tag{1.2}$$

$$\omega_0 = \sqrt{\frac{A_0 + 1}{R_F C_{IN} \tau_A}} \tag{1.3}$$

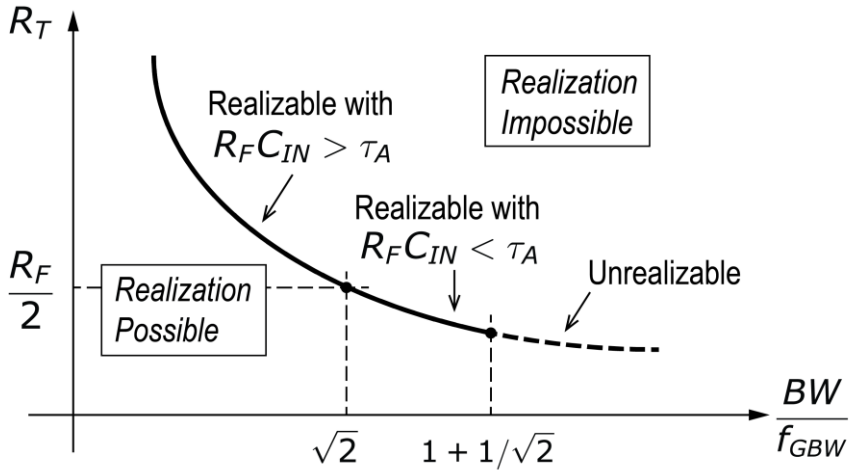


Figure 1.4 Tradeoff between BW and R_T for an R-TIA [64].

$$Q = \frac{\sqrt{(A_0 + 1)R_F C_{IN} \tau_A}}{R_F C_{IN} + \tau_A} \quad 1.4$$

where R_T is the dc gain accounting for the finite loop gain, ω_0 is the natural frequency, and Q is the quality factor describing the damping behavior of the filter response. For a typical peaking-free Butterworth low-pass characteristic, $Q \leq 1/\sqrt{2}$ and therefore, the maximum bound on transimpedance gain is

$$R_T \leq \frac{f_{GBW}}{2\pi C_{IN} BW^2} \quad 1.5$$

where BW is the TIA's -3dB bandwidth and $f_{\mathrm{GBW}} = A_0 f_{\mathrm{A}}$ is the amplifier's gain-bandwidth product (GBW). This bound is known as the *transimpedance limit* [65] and was generalized for other TIA topologies by Säckinger [64]. The transimpedance limit describes a TIA's maximum transimpedance gain for a given bandwidth. The tradeoff between transimpedance and bandwidth of an R-TIA for a given amplifier GBW can be represented graphically in Fig. 1.4, which can be helpful for TIA designers to make an educated estimate of the amplifier requirements for a particular design. For applications (*e.g.*, biomedical) which need considerable gain (> 100 MΩ) for high sensitivity, large R_F can be implemented as a discrete chip resistor, on-chip as a pseudo-resistor [66], or in a tee network configuration [67].

The TIA stability is another important design consideration due to C_{IN}, especially for sensor applications where C_{IN} can be quite large or the TIA is near the transimpedance limit. For example, the C_{dl} introduced by electrochemical sensors can easily be a few nF [41]. As a result, $C_{IN}R_F$ may introduce a pole within the loop bandwidth and cause instability. The feedback capacitor, C_F, introduces a zero in the feedback path to compensate for the phase shift from the input time constant. C_F may be either an explicit or parasitic capacitance. The ~1 pF capacitance from the PCB and package is often sufficient for high-gain discrete designs. Extra care must be taken with

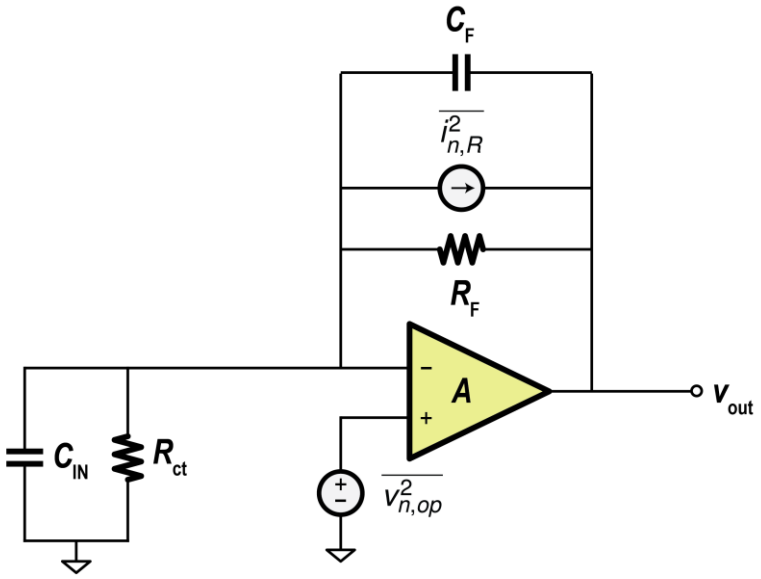


Figure 1.5 Noise sources in an R-TIA with input sensor replaced by an equivalent circuit model.

the tee network due to the parasitic capacitance at the intermediate node. To find a good starting point for sizing C_F, it is mathematically convenient to calculate C_F for a phase margin of 45° where

$$C_F = \frac{1}{4\pi R_F f_{GBW}}\left(1 + \sqrt{1 + 8\pi R_F C_{IN} f_{GBW}}\right) \quad 1.6$$

However, designers are encouraged to overcompensate the TIA to ~65° phase margin considering the tolerance in C_F and the fact that PVT variation may shift the amplifier bandwidth.

1.3.3 Noise

The noise model of a typical R-TIA is shown in Fig. 1.5. Having a resistor in the feedback path unavoidably adds to the total input-referred noise of the system. The input-referred current noise power spectral density (PSD) is

$$\overline{i_n^2} = \frac{4k_B T}{R_F} + \overline{v_{n,op}^2}\left[\frac{1}{R_F^2} + (2\pi f)^2 (C_F + C_{IN})^2\right] \quad 1.7$$

where $\overline{v_{n,\mathrm{op}}^2}$ is the input-referred voltage noise of the amplifier, k_B is Boltzmann's constant, and T is the temperature. The resistor and the amplifier's noise are the two main contributors to the noise. Decreasing the amplifier's noise typically comes at the expense of higher power consumption, whereas R_F can be maximized considering the amplifier output swing. However, as shown in Equation 1.5, larger R_F reduces the closed-loop bandwidth making it undesirable for high-speed applications. There has been research on noise-canceling (NC) techniques to reduce the TIA noise by 15% while maintaining a large bandwidth [57]. In the proposed NC-TIA, the noise voltage at the input and output of the TIA are added destructively through an auxiliary path while the signal is unaffected. However, such cancellation is very sensitive to PVT variation and ineffective at canceling the thermal noise from R_F; therefore, R_F still needs to be maximized, and the tradeoff remains.

Another implication of Equation 1.7 is in its second term where the amplifier noise is scaled by the total input capacitance and asymptotically increases at 20 dB/dec, typically dominating the noise performance at high frequency, as shown in Fig. 1.6. Unfortunately, this noise-peaking

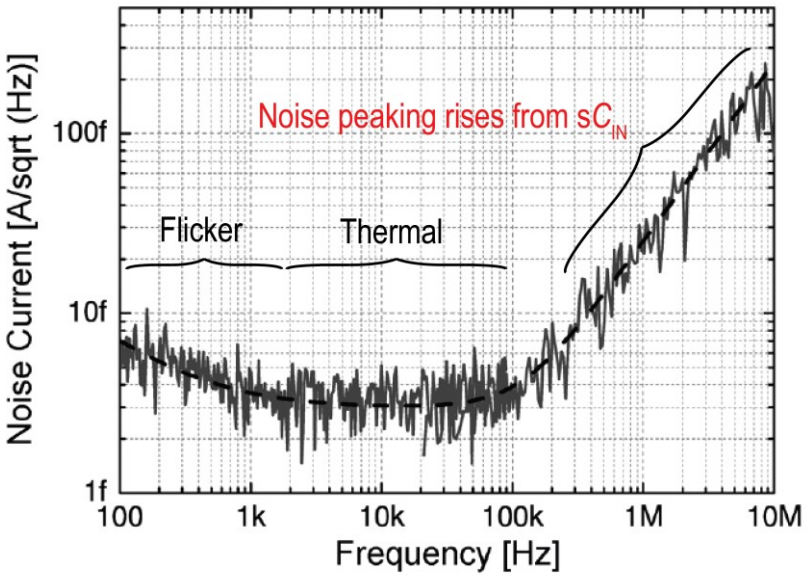


Figure 1.6 Typical contribution to the total input-referred current noise PSD in a TIA [60].

behavior is shared among all current front-end topologies, making low-power, low-noise, and high-bandwidth TIA design a very challenging topic. Therefore, most TIAs are designed to be application-specific. For example, TIAs for biosensing applications are usually heavily bandlimited to achieve low noise and power since most biological signals are slow (<100 Hz) while having large gain (>10 MΩ). On the other hand, broadband (> GHz) TIAs for optical applications are typically very power-hungry and have considerably lower gain (<100 kΩ).

1.3.4 Capacitive TIA

Besides its effect on the bandwidth, large R_F (up to GΩ) also poses a practical limitation due to the area required in CMOS implementations and tolerance in discrete applications. C-TIAs are one way of eliminating such limitations by replacing R_F with a noiseless capacitor. In CMOS technologies, capacitors are usually preferred since operational transconductance amplifiers (OTAs) have high output impedance. As shown in Fig. 1.7(a), a C-TIA is essentially an integrator whose output voltage is a function of the integrated input current. However, like all integrators, a C-TIA is prone to saturation when given a dc input signal or leakage. Therefore, a simple reset switch across C_F is used to reset its charge periodically and provide a dc feedback path. In the presence of a signal with a large dc component, as in many bio-applications (*i.e.,* dark current from photodiodes or ionic current in nanopores), the reset time can set an unreasonably short measurement period. Continuous-reset schemes using a pseudo-resistor [68], [69] or current reducer [60] (Fig. 1.7(b)) have been proposed to maintain large bandwidth at the expense of linearity and additional power overhead. A second stage differentiating amplifier is usually required to recover a linear relationship between the input current and output voltage. The resulting topology is referred to as the *integrator-differentiator* architecture. The differentiator's noise is

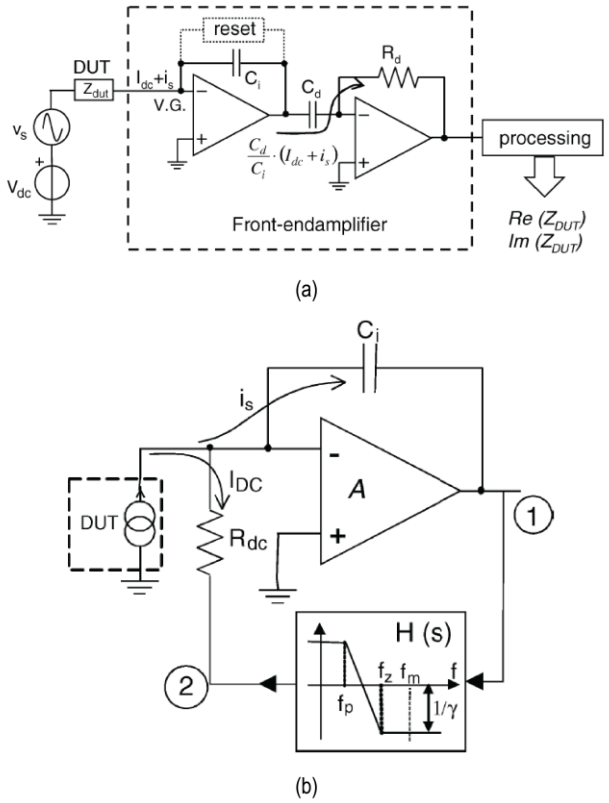


Figure 1.7 (a) Example of an impedance spectroscopy setup using the integrator-differentiator architecture with a reset network to prevent saturation of the integrator induced by the dc input current, (b) schematic of a C-TIA with active feedback as a continuous reset [60].

inconsequential as it is heavily attenuated by the first stage when input-referred. As a result, a C-TIA offers unique advantages of high sensitivity and very low noise across a wide bandwidth. The total transimpedance gain for a typical integrator-differentiator architecture is R_dC_d/C_I, where C_I is the integrator feedback capacitance and R_d and C_d are the RC components in the differentiator, as shown in Fig. 1.7(a). The closed-loop bandwidth is

$$f_{-3\mathrm{dB}} = f_{\mathrm{GBW}} \frac{C_\mathrm{I}}{C_\mathrm{I} + C_\mathrm{IN}} \tag{1.8}$$

where C_{IN} is the total input capacitance and f_{GBW} is the gain bandwidth product of the opamp. It is beyond this paper's scope to derive the exact expression for frequency response and input-referred current noise for a C-TIA as it depends on how the dc servo loop is implemented. In general, designers need to consider the thermal noise introduced by the active path in a continuous-time

feedback implementation. In a discrete-time reset scheme, the system is limited by the k_BT/C and folded-back high-frequency noise due to sampling. However, it has been shown that correlated double sampling (CDS) is very effective at eliminating correlated noise such as k_BT/C and flicker noise in a discrete-time system [70]. However, designers must also be aware that CDS increases the overall white noise due to noise-folding.

1.3.5 Common-Gate TIA

As mentioned above, traditional shunt-feedback TIAs have reduced bandwidth and instability when presented with a large input capacitance. The common-gate TIA (CG-TIA) has been proposed as an alternative TIA topology where the open-loop nature eliminates stability concerns. As a result, CG-TIAs are widely used in high-speed optical receivers with large photodiode parasitics [71]–[73]. In a typical CG-TIA shown in Fig. 1.8(a), the input current is sensed by a CG stage which provides an input impedance of roughly $1/g_m$, where g_m is the transconductance of the input transistor M_1. The drain terminal of M_1 is connected to a resistor, R_T, which defines the total transimpedance gain. In this way, the input impedance (input pole) and the transimpedance (output pole) are conveniently decoupled and can therefore be optimized separately, a notable advantage over its shunt-feedback counterparts. To further reduce the input impedance of a CG-TIA, techniques such as regulated-cascode [71], [72] and negative impedance by cross-coupling CGs [73] have been proposed.

The main challenges in designing CG-TIAs are noise and limited headroom. Fig. 1.8(b) shows noise sources in a typical CG-TIA. Since the input transistor M_1 forms a casocde stage when the input is open (to calculate current noise), it contributes negligibly to the total input-referred current noise at low frequency. However, the noise current produced by the load R_T and current source M_2 are directly referred to input as

$$\overline{i_n^2} = \frac{4k_B T}{R_T} + 4k_B T\gamma g_{m2} + \frac{K_f g_{m2}^2}{C_{ox} WLf} \tag{1.9}$$

where g_{m2} is the transconductance of M_2, γ and K_f are both process-dependent coefficients ($\gamma = 2/3$ for long channel devices and >2 for deep sub-micron processes), C_{ox} is the unit oxide capacitance, and W and L are the width and length of the transistor, respectively. A CG-TIA typically has higher noise due to the first term in Equation 1.9 since the size of R_T is limited by the headroom. In low voltage designs, R_T is usually maximized for transimpedance gain and lower noise; hence the IR drop across R_T severely limits the headroom available for the rest of the circuit.

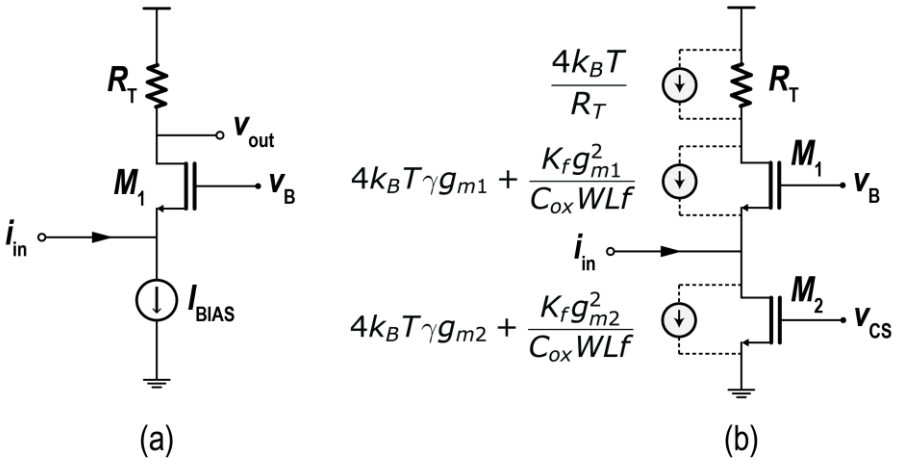


Figure 1.8 (a) Basic common-gate TIA implementation; (b) Noise sources in CG-TIA including current source noise.

Table 1-1 State-of-the-art Transimpedance Amplifiers

	Reference	Arch.	Gain (Ω)	Input Range [a]	BW (Hz)	IRN (fA/ √ Hz)	C_{IN} [b] (pF)	I_{BIAS} (fA)	Power (mW) @ Supply (V)	Application
Bench-top	Femto™ DDPCA-300	R-TIA	10 k – 10 T	1 mA	1 – 400	0.2 – 45,000	5	30	1050 @ 15	General
	Axopatch ™ 200B	R-TIA	0.5 – 500 G	200 nA	70 k	11 – 30	-	1000	-	Patch-clamp
	SRS™ 470	R-TIA	1 k – 1 T	5 mA	10 – 1 M	5 – 150,000	-	-	6000 @ 24	General
	Keithley™ 480	R-TIA	1 k – 100 G	10 mA	1 – 10 k	1.2 – 900	-	-	-	General
Discrete	LTC6563	R-TIA	22.2 k	90 µA	500 M	4,500	1.5	-	200 @ 3.3	Lidar
	ADN2820	SiGe R-TIA	5 k	1.4 mA	9 G	10,000	-	-	200 @ 3.3	Ethernet
	OPA857	R-TIA	5 k, 20 k	240 µA	105 M, 125 M	125,000	2	-	77 @ 3.3	Optical
Integrated	Ferrari [60]	C-TIA	60 M	10 nA	4 M	4	-	-	45 @ 3	General
	Mulberry [63]	C-TIA	0.86 – 7 G	1 nA	4.4 k	6.25	-	-	12.5 @ 3.3	Nanopore
	Kang [62]	C-TIA	10 M – 10 G	100 µA	5 M	1,700 – 30,000	-	-	5.2 @ 1.8	Ultra-sound
	Rosenstein [61]	R-TIA	100 M	1.5 nA	1 M	41	1	-	5 @ 1.5	Nanopore
	Djekic [66]	R-TIA	1 M – 1 G	20 nA	8 k – 2 M	5.5 – 140	-	-	9.2 @ 1.8	General
	Ray [72]	CG-TIA	50 k	30 µA	6.3 G	27,000	1	-	108 @ 1.2	Optical

[a]Maximum input I_{peak}
[b]input stray capacitance, not the input capacitance used for noise characterization
BW: bandwidth, IRN: input-referred noise, I_{BIAS}: input bias current

Table 1-1 provides a non-exhaustive summary of state-of-the-art TIAs in different form factors. This table aims to provide readers with general guidance on picking or designing the TIA for their sensor of choice. Benchtop TIAs provide excellent performance and flexibility due to additional features such as active cooling or capacitance neutralization, which come at the cost of power and size. Integrated solutions typically employ the C-TIA topology and open a new frontier for large-scale parallel sensing, especially in arrayed applications, such as biosensors and touch

displays. Discrete solutions provide a middle ground between compactness and versatility and are used in low channel count applications and for prototyping.

1.4 Current Conveyor

1.4.1 Overview

A current conveyor (CC) is the most integral building block of any current-mode circuit due to its versatility and ability to handle a large input range with high efficiency. It is worthwhile to introduce the concept of a current-mode circuit first to help further the discussion. Current-mode circuits are characterized as circuits whose signals of interest are handled in the current domain without needing a transimpedance element, such as in a TIA. For example, the current signal from the sensor can be directly processed by current-mode circuits (*e.g.*, CC or current-input ADC), eliminating the need for an extra step to convert the signal into the voltage domain followed by a voltage-mode ADC. The advantages of current-mode circuits should become evident at this point,

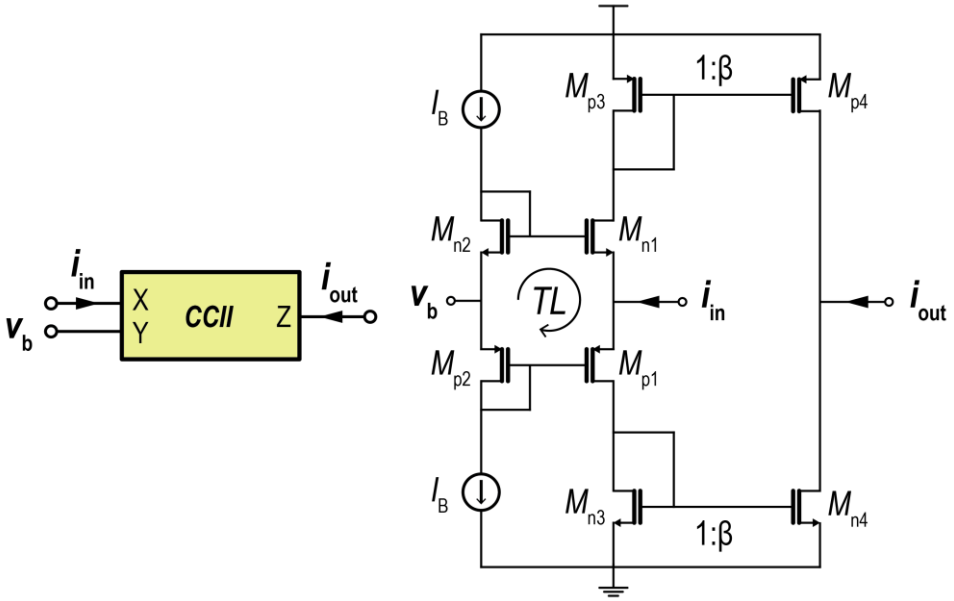


Figure 1.9 Block representation and simplified CMOS implementation of second-generation current conveyor (CCII).

as they: 1) do not require a high-performance closed-loop amplifier for large voltage gain; 2) are easily scaled into advanced CMOS process nodes since the limited supply voltage does not constrain their DR, and they do not need high precision passive components; and 3) show high performance in terms of speed, bandwidth, and accuracy.

Sedra and Smith [74] first introduced the concept of a CC, and it has since been shown using the *Theory of Adjoint Networks* [74], [75], that all active devices can be made of a suitable connection of one or two CCs (specifically the second generation CC, or CCII), making the CC a versatile component in analog systems. As shown in Fig. 1.9, a CCII is a three-port system that can be represented by a transfer matrix that captures the current or voltage expression at each port. The CCII has a transfer matrix of

$$\begin{bmatrix} i_{\mathrm{Y}} \\ v_{\mathrm{X}} \\ i_{\mathrm{Z}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_{\mathrm{Y}} \\ i_{\mathrm{X}} \\ v_{\mathrm{Z}} \end{bmatrix} \tag{1.10}$$

where i_{k} and v_{k} are the current and voltage at port *X, Y,* and *Z*, respectively. Therefore, the voltage at the input node *X*, v_{X}, follows the voltage applied to node *Y*, which has an infinite input impedance as it sees no current (the difference between CCI and CCII is whether $i_{\mathrm{Y}} = i_{\mathrm{X}}$ or $i_{\mathrm{Y}} = 0$, respectively). The output node, *Z*, which has ideally infinite output impedance, carries the same (or opposite) current as i_{X}. The following intrinsic properties of a CC make it a promising front-end choice for sensor applications: 1) low input impedance for negligible signal attenuation and thus is less sensitive to stray capacitance at the sensor interface; 2) high output impedance as needed to drive subsequent current-mode circuits; and 3) voltage following between nodes *X* and *Y* ensures a well-defined bias of the sensor voltage, which is required in most sensor applications [76]–[80].

The CMOS implementation of the CCII shown in Fig. 1.9 was derived from the CCI based on a translinear loop (TL) formed by the four input transistors [81]. The translinear principle

exploits the exponential *I-V* characteristic of bipolar transistors [82], [83] and was later generalized for CMOS transistors operating in subthreshold (which also have an exponential *I-V* relationship) and eventually operating above threshold [84]. The TL ensures accurate voltage following from node *Y* to *X* while defining a PVT-insensitive quiescent current flowing through transistor M_{n1} and M_{p1}, which solves the major limitation in early generation CCs [85], [86]. Another issue with conventional CCs is that they could not achieve simultaneous low quiescent power consumption and large input range since they have maximum input and output current limited by the dc bias current. With the TL architecture, the CC has class-AB (push-pull) operation by conveying a current larger than its quiescent current, significantly increasing the current efficiency over its class-A counterpart. However, the additional transistors required to construct the TL loop unavoidably increase the minimum headroom margin by two overdrive voltages. To address this issue, class-AB CCs based on quasi-floating gate techniques were developed without the supply voltage penalty but at the cost of an additional amplifier and passive components used for ac coupling [87], [88].

1.4.2 Gain, Bandwidth, and Stability

The dc transfer function of the CCII in Fig. 1.9 can be derived by the size ratio, β, between the output current mirrors, M_{n4}/M_{n3} and M_{p4}/M_{p3}. To evaluate the ac response of a current-output circuit, the output port of the CC is shorted to ground in small-signal analysis, hence

$$\frac{i_{\text{out}}}{i_{\text{in}}}(s) = \frac{\beta}{1 + sR_{\text{IN}}C_{\text{IN}}} \tag{1.11}$$

where C_{IN} is the total input capacitance and R_{IN} is the finite input impedance of the CC, namely

$$R_{\text{IN}} \approx \frac{1}{g_{\text{m,n}} + g_{\text{m,p}}} \tag{1.12}$$

One issue with a TL-based CC is that its input impedance is solely determined by the transconductance of the input transistors, which is highly dependent on the process and the quiescent current, I_Q, of the input branch. In low-power applications, when the CC is biased with a small I_Q, the transistors have small g_m, therefore, resulting in a relatively large input impedance (*e.g.*, ~2.5 MΩ at $I_Q = 10$nA with typical $g_m/I_D = 20$, which places the input pole at ~60 Hz for $C_{IN} = 1$ nF), significantly limiting the frequency and noise performance.

To reduce the input impedance of a TL-based CC while maintaining the class-AB operation, I_Q can be increased for larger g_m. However, this increases the thermal noise and power consumption of the CC. Another approach is to use an amplifier feedback topology (Fig. 1.10),

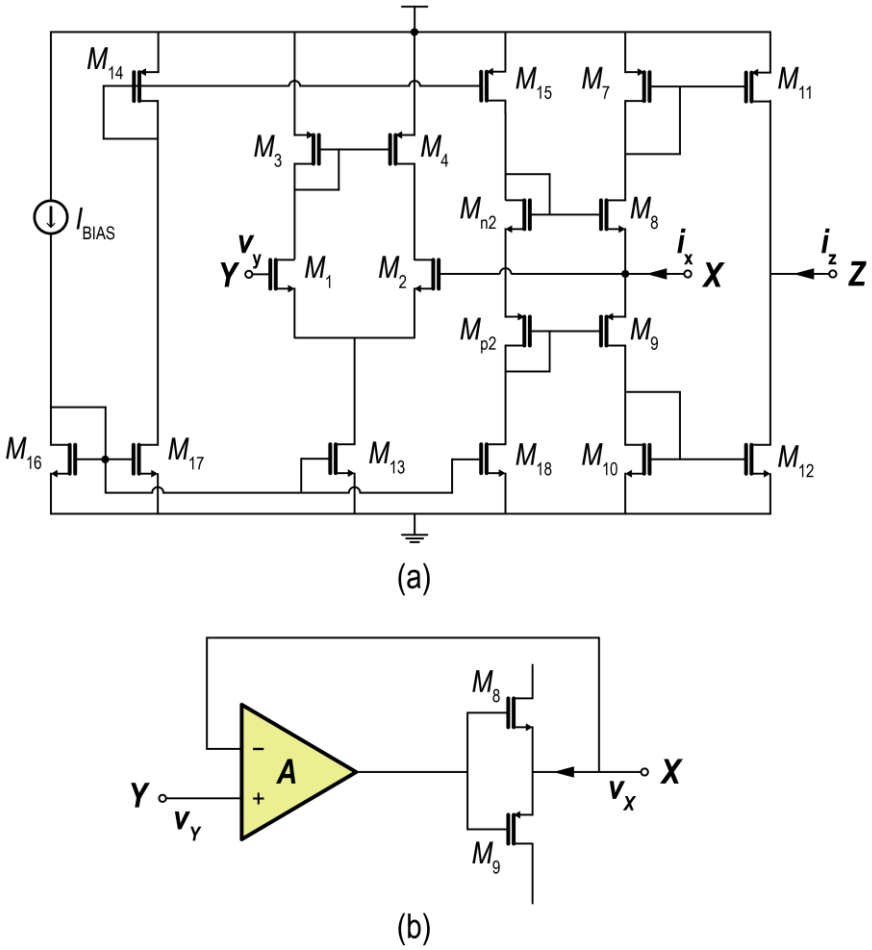


Figure 1.10 (a) Schematic of an early class-AB CCII with opamp feedback to reduce the input impedance; (b) Conceptual model for the input stage proposed in [90] and later employed in [91].

which was proposed in [89] and recently used in a current front-end for amperometry [90]. The resulting closed-loop system resembles a regulated common-gate structure, and the amplifier's open-loop gain reduces the CC input impedance. However, adding a feedback amplifier may introduce stability concerns since there are two poles in the new CC structure – one pole remains at the CC's input, and the other is the dominant pole of the added amplifier. It can be shown that stability can be maintained if the unity-gain frequency of the amplifier is less than the input pole of the original CC [91].

1.4.3 Noise

Typical noise sources in a CC are shown in Fig. 1.11. For simplicity, assume the transconductance for PMOS and NMOS transistors are the same, *i.e.* $g_{\mathrm{m,n}} = g_{\mathrm{m,p}} = g_{\mathrm{m}}$, and the output current mirrors have a gain of β. The input-referred current noise PSD of a TL-based CC can be calculated as

$$\overline{i_n^2} = \left(4 + \frac{2}{\beta}\right)\left(4k_{\mathrm{B}}T\gamma g_{\mathrm{m}} + \frac{K_{\mathrm{f}}g_{\mathrm{m}}^2}{C_{\mathrm{ox}}WLf}\right)\left(1 + s\frac{C_{\mathrm{IN}}}{2g_{\mathrm{m}}}\right)^2 \qquad 1.13$$

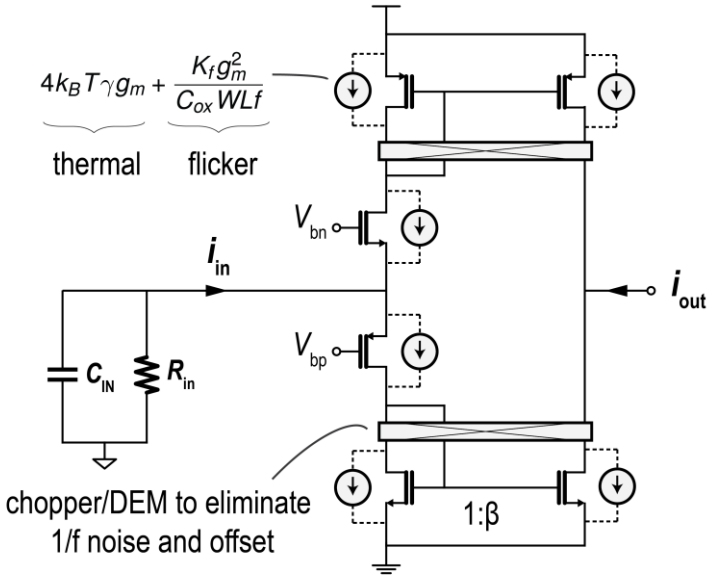


Figure 1.11 Noise sources in a CCII with the input sensor replaced by an equivalent circuit model.

The first and second noise terms in (13) refer to the thermal noise (or shot noise, $2qI$, depending on the region of operation) and flicker noise of each transistor, respectively. The in-band flicker noise (and offset) of the current mirrors can be significantly suppressed by using chopping or dynamic element matching (DEM) at the expense of additional power from the clock and pseudo-random sequence generation [92]. The third term in (13) is why the input impedance of CC needs to be minimized such that the noise zero gets pushed away from the signal bandwidth. In the case of the feedback variant of the CC shown in Fig. 1.10, even though the input impedance is reduced, the amplifier introduces another noise source such that the input noise PSD becomes

$$\overline{i_n^2} = \overline{i_{n,\mathrm{CC}}^2}\left(1 + s\frac{C_{\mathrm{IN}}}{A_0 2g_{\mathrm{m}}}\right)^2 + \overline{v_{n,\mathrm{op}}^2}\left(\frac{1 + sR_{\mathrm{s}}C_{\mathrm{IN}}}{R_{\mathrm{s}}}\right)^2 \qquad 1.14$$

where A_0 is the dc gain of the added opamp, and R_{s} is the sensor shunt resistance, which is typically very large (>100 MΩ). Like the TIA, the voltage noise of the amplifier in a CC also scales with C_{IN} and needs to be minimized at the cost of more power consumption.

1.5 Current-Mode Delta-Sigma Modulator

1.5.1 Overview

Current-mode delta-sigma (I-ΔΣ) modulators have been gaining interest as sensor interfaces for direct current-to-digital conversion. Although most state-of-the-art continuous-time (CT) ΔΣ modulators are used for digitizing voltage signals, they can be adapted into a I-ΔΣ modulator by removing the input resistors such that the loop filter directly integrates the sensor current. Therefore, as will be shown later, many of the system-level considerations for CT-ΔΣ modulators also directly apply to I-ΔΣ modulators.

A I-ΔΣ modulator, in its most simplified form, consists of a loop filter (integrator), a quantizer (comparator), and a feedback network (resistor), as shown in Fig. 1.12(a). The resulting architecture is an error-feedback system that utilizes two key concepts: oversampling and noise shaping. In contrast to a Nyquist-rate ADC, a ΔΣ modulator is sampled at a frequency much higher than the signal bandwidth such that the output signal is recovered from the *averaged* bitstream sequence rather than an instantaneous quantization result. In a stable modulator, the negative feedback ensures that the *average* capacitor current is zero; otherwise, the voltage across the

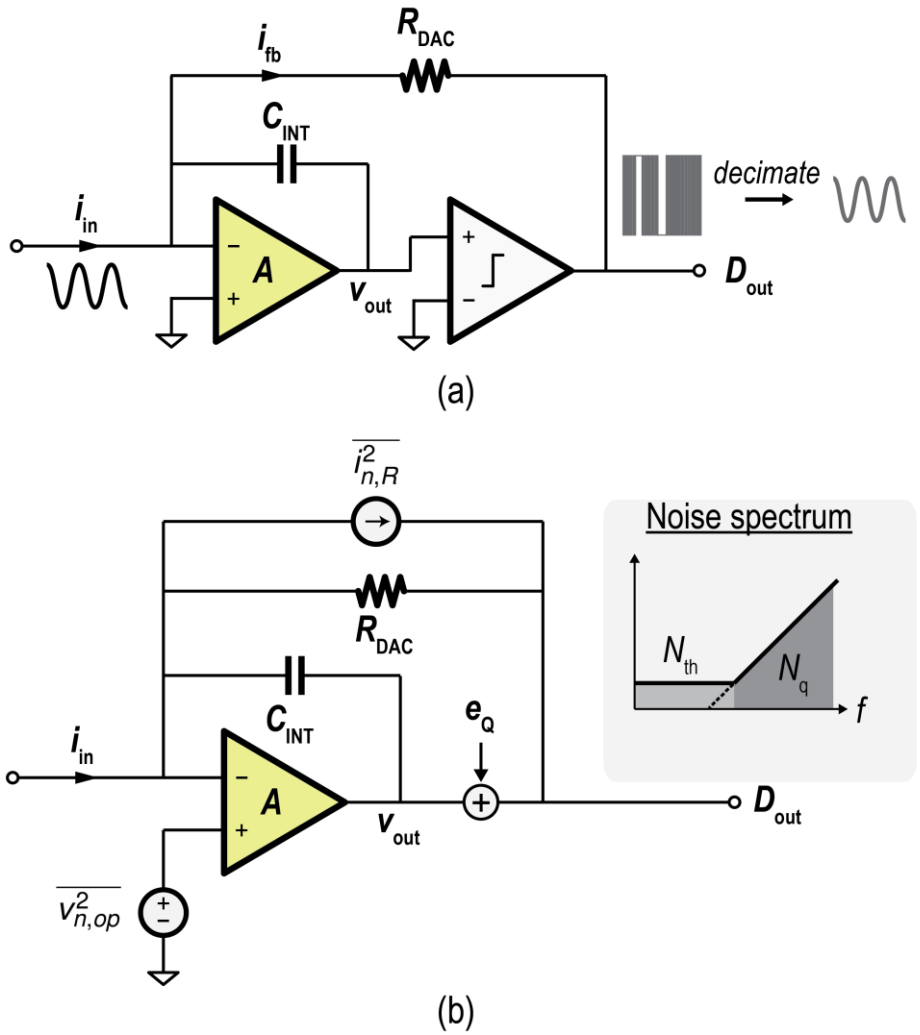


Figure 1.12 Single-ended schematic of a 1st-order I-ΔΣ (a) with resistive feedback and (b) noise model with quantizer modeled as additive noise source.

capacitor would be unbounded. Therefore, on average, $\overline{i_{\text{in}}} = \overline{i_{\text{fb}}}$, which results in a signal transfer function (STF) of

$$STF = \frac{\overline{v_{\text{out}}}}{\overline{i_{\text{in}}}} = -R_{\text{DAC}} \tag{1.15}$$

It can also be shown that the STF in the frequency domain is a $sinc$ function, which means that the modulator filters signals at integer multiples of f_s. This inherent anti-aliasing property is another advantage of a I-ΔΣ modulator such that it does not require extra filters to band-limit the noise. Compared to the aforementioned TIAs and CC, a I-ΔΣ modulator includes a highly nonlinear block – the quantizer, which directly adds a quantization error, e_Q, to the output, as shown in Fig. 1.12(b). To analyze the noise transfer function (NTF) from e_Q to the output, a CT ΔΣ can be rearranged into separate CT and discrete-time (DT) domains for simplicity [93]. In this way, the NTF is

$$NTF = 1 - \frac{A_0}{1 + A_0} z^{-1} \tag{1.16}$$

where A_0 is the dc gain of the integrator. Therefore, an ideal integrator results in a high-pass NTF that shapes most of e_Q away from the signal band. Such noise shaping behavior allows a ΔΣ modulator to achieve high resolution using only a coarse quantizer, which can even be a single-bit comparator, significantly relaxing the system's design complexity and area/power requirements.

A I-ΔΣ modulator can be directly connected to the sensor [94]–[98] or used after a current AFE such as CC [76], [79]. For applications where the sensor is held at a constant dc bias voltage, direct quantization is superior in terms of noise performance, thanks to the inherent anti-aliasing of a CT ΔΣ. On the other hand, the latter scheme is generally employed in applications where voltage modulation is necessary (*e.g.*, cyclic voltammetry) such that the AFE shields the sensor voltage variation from changing the virtual ground of the modulator to achieve better linearity. Even though DEM can be used to eliminate the flicker noise of the current mirrors in a CC, having

an additional stage unavoidably increases the total input-referred noise such that the shot noise of the CC usually limits the overall system.

The dynamic range of a I-ΔΣ modulator is determined by its loop filter order, quantizer resolution, and oversampling ratio ($OSR = f_s/(2f_b)$, where f_b is the signal bandwidth) while the feedback limits its input range. There has been work with higher-order modulators [41], but most low-bandwidth, moderate resolution sensor interfaces can get by with a 1st- or 2nd-order, single-bit design. To avoid having a prohibitively large OSR or current references spanning orders of magnitude, I-ΔΣ modulators with a duty-cycled DAC [96] or input [76] have been proposed where the reference (or input) is pulse-width modulated to achieve higher sensitivity and larger dynamic range with little power overhead or hardware complexity. However, this technique is only applicable to dc input signals and sensitive to charge injection from the sampling switch. Introducing a digital filter in a 1st-order loop has also been proposed to achieve multi-bit quantization and feedback with negligible power overhead [95], [97], [99].

Discussion on ΔΣ modulators can be found at both ends of the spectrum – too mathematical or too hand-wavy, neither of which provides helpful insight to new designers. In the following, general considerations for a I-ΔΣ modulator will be addressed in conjunction with a design strategy based on rules of thumb, aiming to equip the readers with practical tools to tackle the design of a I-ΔΣ modulator for their sensor.

1.5.2 Gain, Bandwidth, and Stability

Since a ΔΣ modulator is a data converter with a digital output, the concept of gain and bandwidth is different from the previous discussion of TIAs and CCs. In this section, the same analysis will be carried out for the integrator instead. Nevertheless, as will be shown later, the

integrator's gain and bandwidth in a ΔΣ are tightly related to the specifications such as the OSR and f_s of the modulator.

The integrator is by far the most important block of a ΔΣ modulator as it is crucial to the overall linearity, in-band noise (IBN), and energy efficiency of the system. The most popular realization of an integrator in a ΔΣ modulator is to connect an OTA in feedback with a capacitor. An OTA with infinite gain and bandwidth means the integrator is linear. However, with finite dc gain, the integrator is referred to as a "lossy" integrator, as not all charge integrated on the capacitor corresponds to a voltage change at the output. A lossy integrator and the quantizer's nonlinear nature can lead to dead-zones, where inputs smaller than a specific level do not affect the digital output. In the frequency domain, a lossy integrator pushes the zero of the NTF in Equation 1.16 away from dc, increasing the quantization noise in the signal band. A general rule of thumb is that the amplifier's open-loop dc gain in a single-loop modulator should be roughly equal to its OSR [100], *i.e.* $A_0 \approx OSR$, such that the additional quantization noise is less than 1.2 dB. The OSR of a ΔΣ can be chosen based on the target signal-to-quantization noise ratio (SQNR), as

$$SQNR_{\text{peak}} = \frac{3(2L+1)M^2 OSR^{2L+1}}{2\pi^{2L}} \tag{1.17}$$

where L is the order and M is the number of levels in the quantizer. The OTA bandwidth is another important design consideration as it can cause integrator gain errors and increase the total IBN. Through simulation, it is suggested that for a single-loop modulator, there is no significant IBN degradation if the GBW of the amplifier is roughly equal to f_s [100].

The stability of a 1st-order ΔΣ can be guaranteed if the input signal does not exceed the reference range. However, stability becomes much less intuitive as the number of integrators increases in higher-order systems. Designers must rely on simulations or tools such as the *Delta-*

Sigma Toolbox by Schreier to decide the scaling coefficients for each integrator and feedback path to maintain stable operation [101].

1.5.3 Noise

Assuming the flicker noise of the integrator and feedback DAC are eliminated with chopping or DEM, the modulator's IBN comprises both the thermal noise, N_{th}, and the quantization noise, N_q, that is shaped by the loop filter. It can be shown that decreasing N_q (by increasing the OSR or NTF order) has less than a linear power tradeoff, while decreasing N_{th} by 2× increases the power consumption by the same factor in a constant g_m/I_D design. As a result, a larger N_{th} can be tolerated with less power for the same total IBN. Therefore, in a typical ΔΣ design, the total IBN is strategically partitioned such that N_{th} accounts for most of the IBN budget for good power efficiency. A good rule of thumb is to keep N_q ~12 dB lower than N_{th} [93].

Neglecting the noise contribution from N_q and the latter stages in a higher-order design, the total input-referred (thermal) noise of a I-ΔΣ modulator can be expressed as

$$\overline{i_n^2} = \overline{i_{n,DAC}^2} + \overline{v_{n,op}^2}\left(\frac{1}{Z_s \parallel Z_{fb}}\right)^2 \tag{1.18}$$

where $\overline{i_{n,DAC}^2}$ is the thermal noise from the feedback DAC, and the second term in Equation 1.18 is the integrator's input-referred voltage noise reflected into a current by the impedance seen at the input node (*i.e.* the parallel combination of the sensor, Z_s, and feedback, Z_{fb}, impedances). The feedback DAC can be realized as resistive (R-DAC), capacitive (C-DAC), or current-steering (I-DAC). It can be shown that R-DACs typically have better noise performance (>3 dB), but I-DACs are much smaller and easier to implement with a large dynamic range using techniques such as current-splitting [102]. C-DACs are less sensitive to clock jitter but necessitate an OTA with sufficiently high linearity due to the sharp transient current. Worse yet, C-DACs compromise the

inherent anti-aliasing property of CT-ΔΣ by sampling the virtual ground, which is a less popular choice [93]. There are other "noise-like" behaviors in a I-ΔΣ modulator, such as inter-symbol interference (ISI) and clock jitter. However, it is beyond this paper's scope to discuss all the nonidealities in a ΔΣ modulator.

1.6 Current-to-Frequency Converter

1.6.1 Overview

I-to-*F* converters are another type of current-mode AFE that converts the sensor current into a time-domain pulse train whose frequency is directly proportional to the current magnitude [103]. Therefore, *I*-to-*F* converters achieve direct current quantization without an explicit ADC, significantly saving area, power, and complexity, and thus are often found in applications where the area is the most critical factor, such as implantable healthcare devices [104]–[106]. Another motivation for using an *I*-to-*F* converter is that the frequency/duty cycle modulated output waveform is intrinsically compatible with backscatter communication (load shift keying) – a

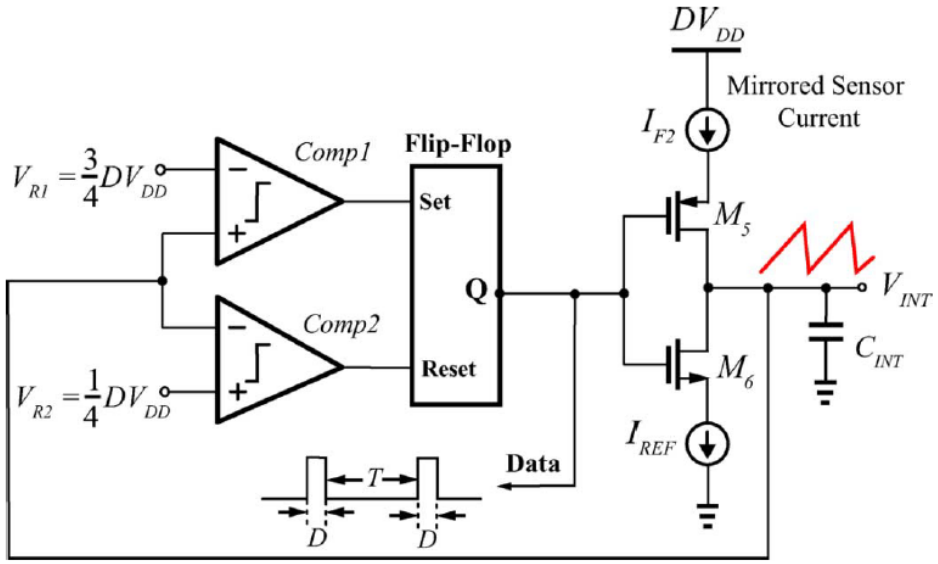


Figure 1.13 Implementation of a current-to-frequency converter [107].

wireless transmission technique often found in implantable/RFID system-on-chip (SoC) to greatly reduce the total power consumption by pushing the digitization and transmission burden to the host side.

1.6.2 Gain, Bandwidth, and Stability

I-to-*F* converters can be implemented by a current-starved ring oscillator whose oscillation frequency is proportional to the input current [104] or a pulse position modulator [105], [106]. An example of the latter is shown in Fig. 1.13, and the basic operation principle is as follows: the input current is mirrored to isolate the sensor from kickback. The mirrored current, I_{F2}, charges a capacitor, C_{INT}, until V_{INT} exceeds a pre-defined threshold voltage (*e.g.*, $3/4 \cdot DV_{DD}$) of the comparator, *Comp1*, which flips the SR-latch output. Then, a reference current, I_{REF}, discharges C_{INT} until V_{INT} drops below the lower threshold voltage (*e.g.*, $1/4 \cdot DV_{DD}$) of *Comp2*. Therefore, the duty cycle, *D*, and period, *T*, of the *I*-to-*F* converter output can be expressed as

$$T = \frac{DV_{DD}C_{INT}}{2I_{F2}} \tag{1.19}$$

$$D = \frac{DV_{DD}C_{INT}}{2I_{REF}} \tag{1.20}$$

As such, the sensor current can be derived from the D/T ratio with respect to I_{REF} without precisely needing to know the values of C_{INT} or DV_{DD}. In the context of a wireless implantable system, where the *I*-to-*F* converter is connected to a backscatter switch for data transmission, the D/T ratio should be chosen to be less than unity (or <20% in [105]) such that the switch is open for most of the transmission period. This means I_{REF} should be a fraction [105] or larger [106] than the sensor current, depending on the orientation of the current sources. However, the absolute value of I_{REF} can be subject to PVT variation; therefore, a calibration step might be necessary to measure I_{F2} at the expense of added complexity and power overhead.

In Fig. 1.13, the windowed comparator (*Comp1* and *Comp2*) continuously compare V_{INT} to 3/4 and 1/4 of the reference voltage (DV_{DD}), respectively. Therefore, *Comp1* and *Comp2* should be implemented as NMOS and PMOS inputs, respectively, to ensure enough headroom for all transistors. Unfortunately, gain mismatch between the comparators results in an error in the output waveform. This behavior will be further discussed in the following section. The comparator bandwidth should be large enough (*e.g.*, to a first-order, 5× larger for 99% accuracy) to minimize error from the propagation delay for the narrowest pulse width, T_{min}, for the given signal range and C_{INT}. Specifically,

$$\frac{g_{\mathrm{m}}}{2\pi C_{\mathrm{L}}} > \frac{1}{5 \times T_{\mathrm{min}}} \tag{1.21}$$

where g_{m} and C_{L} are the input pair transconductance and load capacitance of the comparators, respectively.

1.6.3 Noise

The noise contributors and noise-like nonidealities in an *I*-to-*F* converter consist of the thermal noise from the current sources, comparators, and reference voltages, as well as the nonidealities introduced by the comparators, *e.g.* offset and propagation delay. It can be shown that comparator offset only leads to a dc error in the final *D*/*T* ratio since the offset is constant for both the charge and discharge phase, therefore not affecting the overall linearity of the converter. However, the comparator propagation delay is signal-dependent as it takes more time to resolve to the correct state when V_{INT} is approaching the thresholds *slowly*, as in the case for a small input current. Thus, comparator delay introduces a signal-dependent variation in *T* and a dc offset in *D*, increasing the system's nonlinearity.

1.7 Low-Leakage PCB Design Guidelines

In high-precision current-sensing applications, low leakage is required to measure current signals in the sub-pA range. Sometimes, the best effort in designing an ultra-sensitive AFE is ruined if a designer does not take care to reduce potential sources of leakage between the AFE and off-chip sensors or test equipment. For a standard FR4 PCB shown in Fig. 1.14(a), where the chip is wire-bonded to the PCB (chip-on-board packaging) to reduce packaging parasitics, several things can cause leakage on the order of tens of pAs if preemptive measures are not taken, specifically: 1) surface contaminants (flux residue), 2) surface charge (solder mask), and 3) substrate leakage [107]. Worse yet, PCB leakage is PVT-dependent which makes it difficult to calibrate. The following describes PCB design and preparation practices such as guarding and

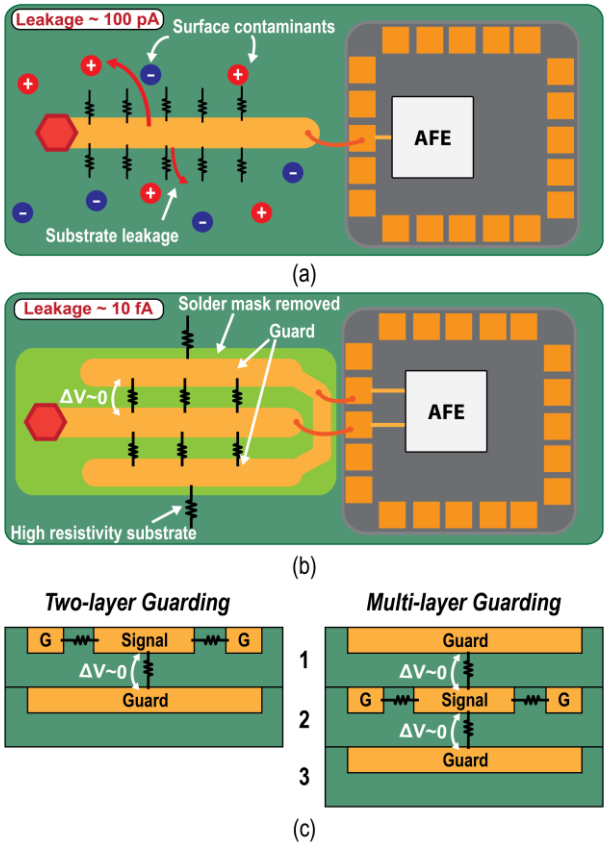


Figure 1.14 Overview of leakage sources from PCB (a) with standard FR4, (b) proper PCB design for low leakage [108], and (c) cross-sectional view of two- and multi-layer guarding.

cleaning (Fig. 1.14(b)). These techniques have been shown to reduce PCB leakage to the low-fA level.

Guarding is a technique to protect the sensitive trace by surrounding it with another trace driven by a low impedance source. As such, guarding minimizes the potential difference between the signal trace and the guard traces, thereby significantly reducing the signal trace leakage [108]. Guarding is especially important if the PCB resistivity is low relative to the sensor impedance. For example, the typical resistance of a standard FR4 PCB is on the order of 10 GΩ. Under a 1-V difference between the signal and substrate, there will be a leakage current on the order of 10 pA if guarding is not implemented, which is unacceptable for fA – pA range sensing applications. However, conductive guard traces close to the signal trace can be another source of parasitic input capacitance, which designers should account for given the noise implications. In a lab setting, the guard is usually provided by the measurement equipment (*e.g.*, Keithley SourceMeter). However, in a practical deployment, designers need to provide the guard voltage by generating a replica of the signal voltage. In a TIA, this is usually the same voltage used to bias the sensor, V_{CM}. As shown in Fig. 1.14(c), guard traces should also be placed below and on the sides (on the same plane) of the signal trace. In multi-layer PCBs, the signal trace can also be sandwiched between two layers of guard traces.

Removing the solder mask is another useful PCB technique for leakage mitigation. Solder masks are generally used to reduce moisture infiltration into the PCB material and ease soldering. However, solder mask tends to accumulate surface charge that can cause leakage. Therefore, the solder mask should be removed around the guard and sensitive traces when designing a low-current measurement system.

The PCB substrate is a subtle but important consideration. Among them, FR4 glass epoxy is the most common insulating substrate on the market. However, when performance is the uttermost concern, PCBs with ceramic hybrid substrates, such as Rogers 4003C, typically have 1,000× higher resistivity than standard FR4. They have been shown to have ~5 fA of leakage, ~20,000× lower than standard FR4 [107]. Rogers substrates are often used in microwave and high-speed circuits but also perform well in low-current applications by significantly reducing substrate leakage. Some designers forego the PCB connection entirely and "air solder" the input as air is an excellent dielectric.

Lastly, an assembled PCB should be adequately cleaned to remove surface contaminants such as dust or flux residue, contributing to leakage. In a typical cleaning protocol [109], the PCB is soaked in acetone for roughly ten minutes, followed by aggressively scrubbing with isopropanol. Then the PCB is rinsed with deionized water for a few minutes, blow-dried with nitrogen gas, and baked for 2 hours at 85 ºC before use. Cleaning has been shown to reduce PCB leakage by more than 20× compared to an unwashed PCB.

1.8 Discussion

The development of ultra-sensitive sensors has spurred the need for higher-performance AFEs. Among these, CMOS designs have achieved state-of-the-art performance with ever-increasing sensitivity, dynamic range, and power efficiency. Such constant improvements over prior works are often made possible by innovative circuit design. Therefore, although this paper's scope is beyond just CMOS AFEs, Table 1-2 shows recent trends in CMOS current-sensing AFEs over the last decade. In the following, the four architectures described previously, *i.e.,* TIA, CC, I-

Table 1-2 State-of-the-Art CMOS Current Sensing Front-Ends

Ref	Topo-logy	Node (nm)	Gain	Input Range	BW (Hz)	IRN (fA/√Hz)	C_{noise} [a] (pF)	DR [b] (dB)	Power (mW) @ Supply (V)	Area [c] (mm^2)	Application
[60]	C-TIA	350	60 MΩ	10 nA [d]	4 M	4	1	60	45 @ ±1.5	0.34	General
[62]	C-TIA	180	10 M – 10 GΩ	100 µA	7.1 – 5.7 M	1,700 – 30,000	15	46	5.2 @ ±0.9	0.12	Ultrasound
[63]	C-TIA	350	0.86 – 7 GΩ	1 nA	4.4 k	6.25	-	68	12.5 @ 3.3	0.02	Nanopore
[61]	R-TIA	130	100 MΩ	1.5 nA	1M	41	1	31	5 @ 1.5	0.2	Nanopore
[55]	R-TIA	180	2.6 k	15 µA	8.5 G	11,600	0.2	24	81 @ 1.8	0.25 [e]	Optical Receiver
[56]	R-TIA	65	20 k	20 µA	10 G	7,000	0.1	29	23 @ 1.2	0.12	Optical Receiver
[58]	R-TIA	65	500 Ω	100 mA	40 G	19,800	-	88	55.2 @ 1.2	0.6	Optical Receiver
[59]	R-TIA	130	30 – 4,500 Ω	5 mA	27 G	20,000	-	64	313 @ 3.3	1.12	Optical Receiver
[66]	R-TIA	180	1 M – 1 GΩ	20 nA	8 k – 2 M	5.5 – 140	5	66	9.2 @ 1.8	0.07	General
[72]	CG-TIA	130	50 k	30 µA	6.3 G	27,000	1	23	108 @ 1.2	0.08	Optical
[88]	CC	500	1 – 15 A/A	50 µA	1 – 3 M	5,700	-	74	0.28 @ 3.3	0.127	General
[77]	CC + I-ΔΣ	500	1 – 32 A/A	16 µA	0.5	141	-	54	0.241 @ 5	0.157	Electro-chemical
[80]	CC + I-ΔΣ	130	1 – 1/1000 A/A	1 mA	100	9,100	-	60	0.029 @ 3	0.16	Electro-chemical
[96]	I-ΔΣ	350	-	2.8 µA	10	6,957	-	77	0.017 @ 1.5	0.5	pH
[98]	I-ΔΣ	180	-	1.1 µA	10	30	-	78	0.05 @ 1.8	0.11	Biosensing
[99]	I-ΔΣ	180	-	10 µA	1.8	74.5	-	160	0.295 @ 1.8	0.2	Biosensing
[100]	I-ΔΣ	55	-	200 µA	4 k	31,600	-	140	1.011 @ 1.2	0.585	General
[104]	*I*-to-*F*	180	-	11.6 µA	10 k	11.6	-	140	5.22 @ 1.8	0.091	Biosensing

[a]Input capacitance used for noise characterization
[b]$20\log(I_{MAX}/I_{MIN})$ calculated at a fixed-gain setting
[c]Active area (per channel)
[d]Frequency-dependent input range
[e]Estimated
BW: bandwidth, IRN: input-referred noise

ΔΣ, and *I*-to-*F* converters, are compared on a system level, aiming to provide readers with strategic

design consideration to select the front-end topology best suited for their application.

R-TIAs provide a reasonable balance between key design parameters such as the gain-bandwidth product (GBW), power, and noise among the various front-end topologies. Therefore, R-TIAs are very versatile and can be found in many applications with a wide range of specifications. However, as described in Section III, the transimpedance limit exhibits a quadratic power increase for large bandwidths making an R-TIA design for high-speed applications (*e.g.*, optical communications) typically consume tens of mW. Thermal noise from the feedback resistor also relegates R-TIAs to the worst in noise performance. On the other hand, C-TIAs have been shown to achieve the lowest input-referred noise (<10 fA/√Hz) by taking advantage of a noiseless feedback element. Despite the need for a second differentiator stage, its noise contribution is negligible due to the large gain from the integrator stage. As a result, C-TIAs are usually favored in low-noise applications. However, they are prone to saturation and require either periodic resetting [90] or a continuous feedback path to discharge the signal's dc component. Such reset techniques require clock generation and/or alter the C-TIA frequency response (*e.g.*, bandpass in [60]); therefore, they are generally not employed in wideband applications. The additional differentiator stage typically makes the overall C-TIA consume more power than its R-TIA counterpart. The effect of charge injection due to the reset switch was characterized for electrochemical sensors in [90]. The average current integrated onto the working electrode was more than 4× compared to a CC designed with the same power consumption and sampling frequency. Thus, one should consider the impact of having the sensor directly connected to a front-end that is chopped. Unlike R-TIAs or C-TIAs, CG-TIAs operate in open-loop such that a large input capacitance will not de-stabilize the amplifier. CG-TIAs are generally used in high-speed optical links where the PD parasitic capacitance is large

given the bandwidth, and noise is not the most critical concern. CG-TIAs suffer from limited headroom.

The primary purpose of having a CC in a current-sensing AFE is to provide a low input impedance and voltage bias to the sensor while having moderate gain (<10 A/A) to relax the noise requirement of the following stages. A CC's gain is defined by a current mirror ratio, which is often chopped or rotated with DEM for high resolution at the cost of additional power. For a low-bandwidth design, the transistors that cannot be chopped in a CC must be sized large enough to mitigate flicker noise. CCs have been shown to have better current efficiency due to the class-AB operation and are particularly helpful in cases where a large voltage excursion needs to be applied at the sensor side (*e.g.*, scanning the working electrode in cyclic voltammetry) due to their ability to maintain linear current conveying across a wide input common-mode voltage range, which is typically unwanted for an amplifier, as in the cases for a TIA and I-ΔΣ modulator.

In cases where the sensor is biased at a constant dc voltage, a I-ΔΣ modulator can be used to directly quantize the signal for the best power efficiency. Due to oversampling, I-ΔΣ modulators typically target low bandwidth signals (<10 kHz). Unlike TIAs, I-ΔΣ modulators can theoretically achieve an extremely large dynamic range (>80 dB) by properly choosing the order, OSR, and quantizer resolution. An even larger cross-scale dynamic range (>120 dB) was reported using a current-steering DAC with a programmable range setting. For example, in [98], the input polarity was asynchronously flipped whenever the integrator output was close to saturation, as detected by a windowed comparator. This technique eliminates the need to reset the C-TIA and allows continuous integration to achieve a state-of-the-art dynamic range of 160 dB with high linearity (7 ppm integrated nonlinearity). In [97], a sub-pA resolution was achieved by incorporating a digital prediction filter in a single-bit I-ΔΣ modulator to realize the equivalent of multi-bit quantization

with negligible power overhead. However, the input impedance of a I-ΔΣ is quite high, and noise peaking needs to be considered for capacitive sensing.

Last but not least, *I*-to-*F* converters achieve direct quantization with very little hardware by converting the input current level to a frequency/duty cycle modulated waveform suitable for backscatter communication systems, such as often encountered in IoT devices. The current sources should be sized large or chopped if the resolution is limited by flicker noise. The input pairs of the comparators should also be sized large to increase the g_m/I_D ratio for low offset and input-referred noise. The passive capacitor can be replaced by an active integrator, providing a virtual ground for the current sources. However, the additional amplifier's area and power overhead conflict with the incentive of using an *I*-to-*F* converter in the first place; therefore, this design is not generally used.

1.9 Conclusion

Current sensors transduce current signals in response to stimuli from everyday life, spanning macroscopic signals such as temperature, pressure, and light to the microscopic regime such as biomolecular binding events. Their versatility has led to broad deployment in environmental, automotive, industrial, and medical applications. This chapter first reviewed examples of such sensors to gain an understanding of the application-specific requirements and nonidealities. While understanding the sensor is crucial, a complete sensing system requires engineers to know front-end design as well. This article then discussed the primary design considerations for three common current-sensing architectures, namely the transimpedance amplifiers (R-TIA, C-TIA, and CG-TIA), current conveyor (CC), current-mode delta-sigma modulator (I-ΔΣ), and current-to-frequency (*I*-to-*F*) converters. R-TIAs provide a reasonable balance between key parameters such as gain-bandwidth product, power, and noise; therefore are

the most commonly used. However, they are unsuitable for high-speed or ultra-low-noise applications due to noisy shunt feedback and tightly coupled design parameters, such as the input impedance, transimpedance gain, stability, and bandwidth. C-TIAs are a low-noise variation for R-TIAs by utilizing a noiseless feedback element but require an auxiliary path (*e.g.*, dc servo loop or reset switch) to avoid saturation. CG-TIAs are the open-loop version of R-TIAs that do not suffer from instability with a large input capacitance but tend to be noisy and have limited transimpedance gain when resistively loaded. The transimpedance gain can be increased by using a CC. CCs have current gain and are usually paired with a current-mode ADC such as I-ΔΣ when there is a need to decouple the sensor from the ADC (*e.g.,* to provide low input impedance or voltage excitation). I-ΔΣ modulators have been gaining popularity as front-ends for resistive sensors and are best suited for applications where a large dynamic range is required (*e.g.,* biosensors where a small signal is superimposed on a significantly larger background signal). Despite not being as popular as the other AFEs, *I*-to-*F* converters are used in applications where size and power are of the most critical concerns, such as wireless systems. Last, this paper provided low-leakage PCB design guidelines that should be followed for high-sensitivity current front-end designs.

Chapter 1, in part, is based on the material from Da Ying and Drew A. Hall, "Current Sensing Front-Ends: A Review and Design Guidance," *IEEE Sensors*, vol. 21, no. 20, Oct. 2021. The dissertation author was the primary investigator and author of this paper.

Chapter 2. CURRENT FRONT-END FOR PROTEIN-LIGAND STUDY

2.1 Introduction

With the rapid advances in exploration and screening techniques, the pharmaceutical industry identifies almost ten thousand new drug compounds annually [110]–[112]. However, the success rate from drug discovery to a clinical trial is a meager 0.05% due to the involvement of extraordinarily high-cost and time-consuming multi-phase human trials [113]. Many of these failures could have been predicted and avoided in the pre-clinical stage if scientists had tools to allow them better understand and screen drug-drug interactions. There is currently an unmet need

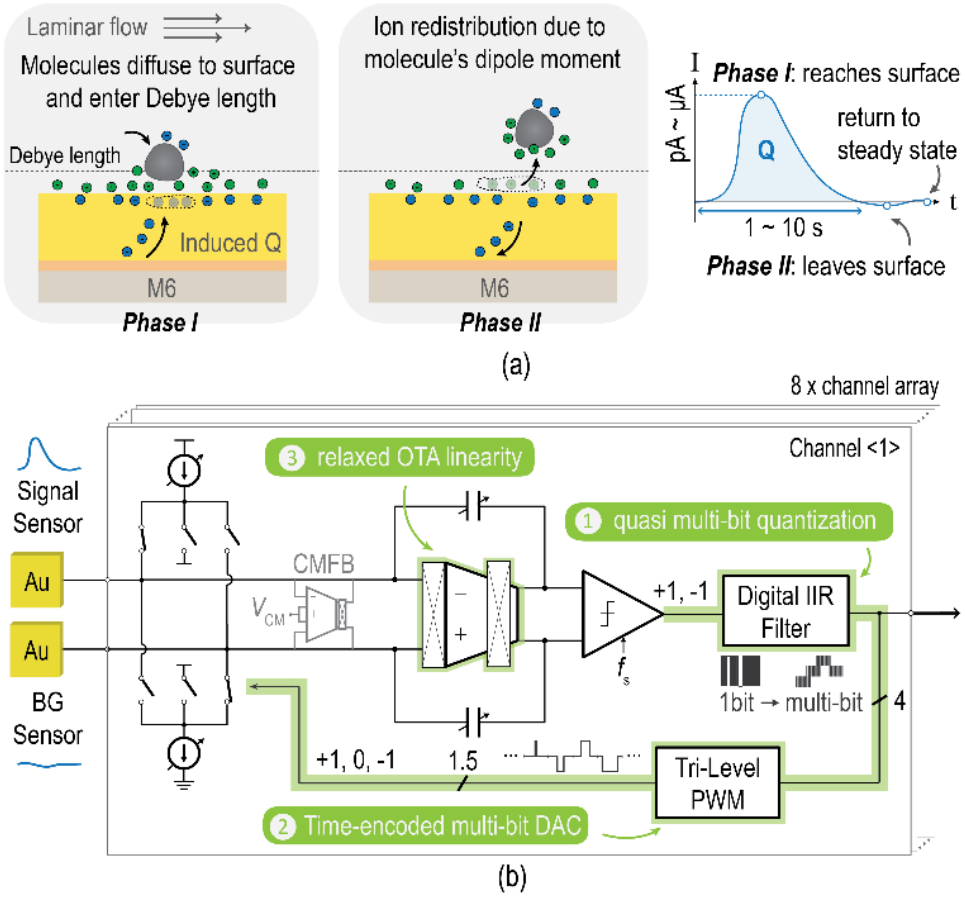


Figure 2.1 (a) TIMES sensing principle and signal model and (b) system architecture of the proposed AFE.

for *in-vitro* testing of protein-ligand interactions to assess the binding properties qualitatively and quantitatively analyze the binding kinetics in physiological conditions [114]–[116].

Proteins have complex interactions with other biomolecules (*i.e.,* ligands). There has been significant effort in developing quantitative molecular-level tests for protein screening, but the performance is heavily dependent on how the molecules are prepared. For example, surface plasmon resonance (SPR) [117]–[119] and Forster resonance energy transfer (FRET) [120]–[122] require immobilization and/or labeling of the ligand, which can interfere with binding. As such, existing methods introduce disruptions (sometimes significant) in the binding kinetics and lead to results that do not resemble those *in vivo*.

Transient-induced molecular electronic spectroscopy (TIMES) is a recently reported biosensing technique for characterizing protein-ligand interactions without imposing any physical alteration to the biomolecules, such as labeling or immobilization [123]–[125]. In TIMES, the transient signal is generated as the surface charge distribution on the electrodes is reoriented by the dipole moment of a protein-ligand complex passing by under laminar flow, as shown in Fig. 2.1(a). As a result, TIMES is closer to physiological conditions and reveals molecular properties unattainable with existing methods. It is important to note that this is not a general-purpose biosensing technique as it intrinsically lacks specificity. TIMES's detection principle and validity have been studied using discrete sensors and an off-the-shelf transimpedance amplifier instrument (SRS 570). This work presents a monolithic integration of the sensors and a multi-channel current front-end, achieving a miniaturized sensing platform—μTIMES, as shown in Fig. 2.1(b).

Integrating a sensor with the readout circuit eliminates parasitics due to long cables from the sensor to the front-end, exhibits better environment interference resilience, and generally leads to lower noise, higher fidelity measurements. Table 2-1 lists the design specifications for μTIMES

based on prior benchtop studies. To implement eight parallel channels on a 3×3 mm^2 CMOS chip, a 3×5 sensor array (8 channels with shared references and test structures) was designed, each with a maximum sensor area of 300 μm × 300 μm, which limits the active circuit area and scales the signal range down to 100 fA – 1 μA for the target protein concentration range of 0.1 μM – 10 mM. The 140 dB dynamic range (DR) was portioned across 4 on-chip references in this work, relaxing the DR for each reference to 80 dB. The laminar flow rate (5 cm/s) is the determinant factor in determining the bandwidth, but the physical dimension of the channel is also relevant as smaller molecules like ligands theoretically move faster. Therefore the transient response of ligands was used to determine the 10 Hz upper bound on the signal bandwidth. In contrast, chemical parameters such as the molecule's surface charge affect signal magnitude more than bandwidth.

In electrochemical techniques such as cyclic voltammetry or chronoamperometry, where sensing electrodes need to be electrically modulated, intermediate stages such as transimpedance amplifiers [126], [127] or current conveyors [78], [128] are commonly used to decouple the readout front-ends from the large voltage variation. However, during a TIMES study, both working and reference electrodes (WE and RE) are biased at a dc potential and thus can be interfaced with a current-input analog-to-digital converter (I-ADC) for direct quantization. While there are many I-ADCs, such as voltage-controlled oscillators (VCOs) [129] and current-to-frequency (*I*-to-*F*) converters [130], delta-sigma modulator (ΔΣ)-based ADCs are by far the most embraced due to

Table 2-1 Target Specification of The Current Sensing AFE

	Application Requirement	**AFE target**
Sensitivity*	0.1 μM detection limit	100 fA
Dynamic range	0.1 μM – 10 mM	100 fA – 1 μA
Bandwidth	5 cm/s laminar flow rate	10 Hz
Active area	8 on-chip electrodes	0.1 mm^2/ch

*Lysozyme protein on a 300×300μm^2 sensor

their excellent resolution-to-energy tradeoff for low bandwidth signals [131], [76], [95], [132], [98], [133], [99], [97]. However, few works can achieve the 100-fA resolution target with such a wide cross-scale DR.

In [76], a pulse width modulated (PWM) switch was added at the input of a 1st-order incremental ΔΣ. This scales down the input signal and lets the ΔΣ operate with a lower reference current for better energy efficiency. A large DR was achieved by partitioning the signal range across five references from 50 pA to 500 nA. However, the input modulation makes this architecture sensitive to noise folding and aliasing since a discrete-time (DT) ΔΣ does not have inherent anti-aliasing. Furthermore, charge injection from the input switch can perturb the sensor, such as with the capacitive sensor in μTIMES. In [98], asynchronous input flipping was proposed in an hourglass-ΔΣ to avoid saturating the integrator, resulting in a state-of-the-art DR of 160 dB while using a single reference. However, this work requires two continuous-time comparators, a 5th-order polynomial calibration loop, and dynamic element matching (DEM) – making it both area- and power-hungry and thus less attractive for multi-channel applications.

Fig. 2.1(b) shows the proposed architecture for each readout channel, where a 1st-order continuous-time current-mode ΔΣ modulator was implemented for its compact area and good energy efficiency. To increase resolution while consuming low area and power, we propose to add a digital infinite impulse response (IIR) filter after the single-bit quantizer in a ΔΣ to achieve multi-bit quantization. The added IIR filter effectively achieves a 4-bit feedback system by predicting the next output from previous 1-bit quantizer outputs. This improves the modulator resolution with finer feedback levels. The output is then fed back using a tri-level (return-to-open) PWM current-steering DAC (I-DAC). The proposed architecture is equivalent to a multi-bit modulator that can be clocked at a lower sampling rate than a single-bit modulator for the same resolution, thus

relaxing the bandwidth requirement and improving the anti-aliasing. A cross-scale dynamic range of 140 dB was achieved by partitioning the reference current. This work expands on the work originally reported in [97].

2.2 Sensing Principle

In this label- and immobilization-free detection scheme, an electronic signal is generated through a non-faradic process when a molecule or complex (*i.e.,* a protein-ligand) diffuses towards the electrode. The protein, ligand, and buffer are introduced in two separate microfluidic channels to create a flux of molecules towards the electrode, with the buffer-only channel serving as a reference. Background currents and interferences (*e.g.*, 60 Hz, temperature drift, etc.) common to both channels are canceled by differential sensing. In the protein-ligand channel, the protein is the *only* macromolecule with a dipole moment. The formation of a protein-ligand complex alters the 3D configuration, changing the dipole moment and charge distribution [134]. Fig. 2.1(a) illustrates this process where ions on the sensor surface redistribute by the protein-ligand dipole moment to maintain local charge neutrality, introducing a charge flux due to the image charge effect. The transient change in the surface charge results in a current signal that the AFE records. In contrast to FET-based sensing, where the source-drain current is modulated by the change in surface change when immobilized probes capture or release the targets, TIMES is a label-free and immobilization-free measurement so different kinds of biomolecules can be measured with the same device.

The reference electrode (RE) used in TIMES is a pseudo-reference electrode biased at mid-scale, 0.9 V. Due to the TIMES sensing principle, where the charge perturbation on the electrodes is measured, the potential between the solution and the electrodes does not need to be as well defined as in many other electrochemical sensing approaches. Therefore, there is no need for a dedicated potentiostat to drive the RE. This sensing technique can be generalized to all molecular

interactions, including protein-ligand, protein-protein, and protein-nucleic acid interactions. By measuring the transient signals induced by the ligand, protein, and mixtures of ligand and protein molecules in different ratios, one can calculate the dissociation coefficient, K_d, of the protein-ligand interaction. As in Table 2-1, the dynamic range for K_d measurements can vary between mM (weak/nearly no binding) to nM (strong binding). Furthermore, this technique can also capture a "*molecular fingerprint*" of the target biomolecule's (or complex) interaction with the sensor surface.

2.3 System Architecture

The transient signal induced by the protein-ligand complex in μTIMES is intrinsically band-limited to only a few hertz. Oversampled data converters are well-suited for capturing such signals. Specifically, a 1st-order ΔΣ modulator with a moderate to a high oversampling ratio (OSR) can provide sufficient signal-to-noise ratio (SNR) to meet the 13-bit resolution target while being area- and power-efficient; two factors that are important in multi-channel/arrayed applications.

Historically, single-bit quantization in ΔΣ, as shown in Fig. 2.2(a), has been widely adopted because of its ease of implementation and inherent linearity, avoiding the need for DEM [131], [76], [95]. However, several nonideal aspects of single-bit quantization can significantly degrade the performance. First and foremost, for a 1st-order loop filter, doubling the sampling frequency, f_s, only improves the signal-to-quantization noise ratio (SQNR) by 1.5 bits; thus, one must resort to a high OSR causing higher power consumption. Another problem is that the quantization noise is strongly deterministic, resulting in in-band harmonic distortion and limit cycles. Consequently, 1st-order single-bit ΔΣ modulators are challenging to model and analyze with a linear model, highlighting the third issue—arbitrary quantizer gain. Since a single-bit quantizer only has two

levels, its gain can take a wide range of values, potentially shifting the poles and altering the loop dynamics. As a result, designing a 1st-order, single-bit ΔΣ usually relies on exhaustive simulation [93].

This work proposes a 4-bit IIR quantizer to avoid the aforementioned issues with single-bit quantization. As shown in Fig. 2.2(b), the IIR quantizer consists of a single-bit quantizer (*i.e.* a comparator) and a 4-bit digital IIR filter that increases the effective quantization resolution by linearly predicting its quantization level based on two previous comparator decisions, *q*. The proposed IIR quantizer balances the tradeoff between low implementation complexity and higher resolution from using a multi-bit quantizer. Finally, a tri-level PWM DAC encodes the 4-bit output, *d*, into a symmetrical pulse sequence whose width is proportional to the digital code and is subtracted from the input, *u*, to close the feedback loop.

Interestingly, a similar principle was first introduced in [135] and [136] where an integrated neural recording SoC was presented with a state-of-the-art power efficiency. In this ADC-direct front-end, the radix-2 quantizer's output is fed into a digital prediction loop implemented using a

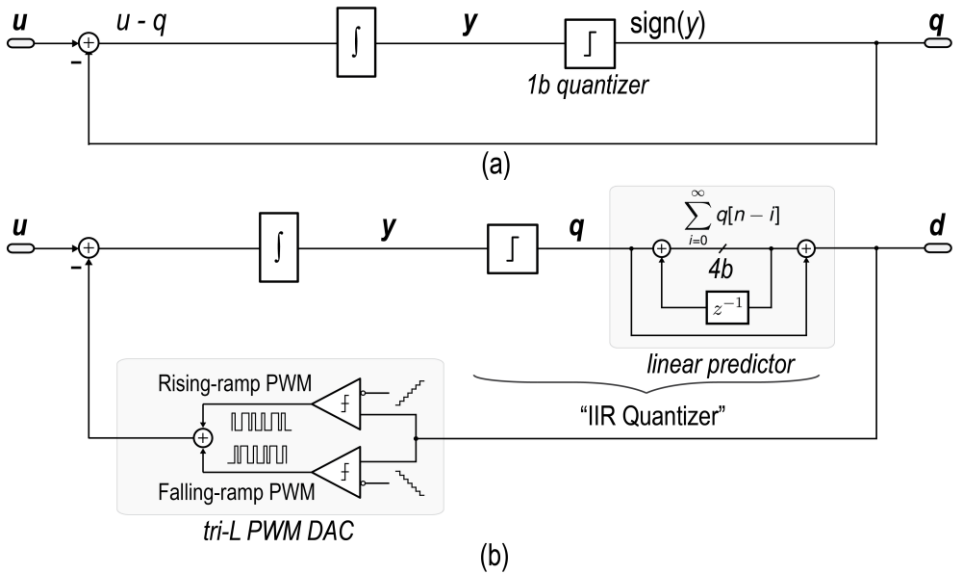


Figure 2.2 Block diagram of (a) conventional 1st-order 1-bit ΔΣ and (b) the proposed ΔΣ modulator with IIR quantizer and tri-level PWM DAC.

digital accumulator. Deriving the transfer function of this digital predictor results the same IIR expression in this work. In [135] and [136], the ADC output was taken at the predictor input, resulting a first-order differentiation signal transfer function which necessitates an extra integration step in the back-end to recover the signal. In this work, the predictor accumulates the 1-bit comparator's output in a linear fashion. The following sections will try to describe the loop dynamics in a logical and intuitive manner.

2.3.1 Linear Prediction in a 1st-order Single-order loop

Unlike a Nyquist-rate ADC (*e.g.*, flash, SAR, etc.), where the result is instantaneously available, a ΔΣ modulator outputs a time-encoded sequence, of which each sample is dependent on the previous values. This "memory" effect and oversampling form the fundamental basis for using linear prediction to increase the quantizer resolution. For a reasonably large OSR, any input signal can be estimated by linearly extrapolating from its previous samples [137]. For example, with a slow-varying discrete-time sequence x, $x[\mathrm{n}+1]$ can be approximated by taking the first two terms in the Taylor expansion around $x[\mathrm{n}]$. It can then be shown that each sample in x is a linear combination of its previous two samples, *i.e.*

$$x[\mathrm{n}+1] \approx x[\mathrm{n}] + \frac{\partial x}{\partial t} T = 2x[\mathrm{n}] - x[\mathrm{n}-1] \tag{2.1}$$

where T is the sampling period.

Before applying the concept of linear prediction to a single-bit ΔΣ, we first look at how each output relates to the instantaneous input magnitude. Starting with a standard single-bit CT ΔΣ, the comparator output is directly subtracted from the input. The quantizer input, y, is equal to the previous sample plus the instantaneous residue between the input and feedback, as shown in if Fig. 2.2(a), where

$$y[\mathrm{n}] = y[\mathrm{n}-1] + u[\mathrm{n}] - q[\mathrm{n}]. \qquad 2.2$$

On average, q is fed back such that the residue seen by the integrator, $u - q$, is minimized, so it is reasonable to expect a statistical relation between u and q. For example, for a u close to the positive full-scale range, the local density of +1's in q is also large because the modulator tries to feedback a large *mean* value.

2.3.2 IIR Quantizer

To realize Equation 2.1 with only single-bit quantization, Fig. 2.2(b) shows the comparator output is passed through a filter whose transfer function can be derived from the difference equation

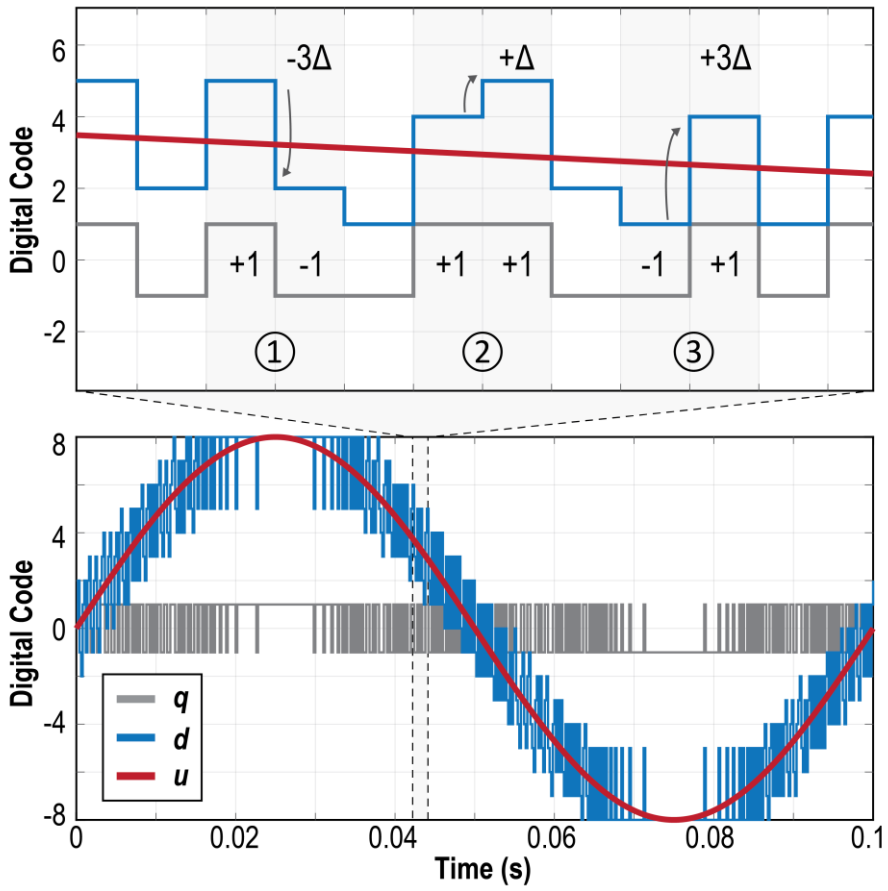


Figure 2.3 Transient waveforms of the linear prediction in a IIR-ΔΣ with input, u, comparator output, q, and modulator output bitstream, d.

$$d[\mathrm{n}] = d[\mathrm{n}-1] + 2q[\mathrm{n}] - q[\mathrm{n}-1]. \quad (2.3)$$

The addition of $d[\mathrm{n}-1]$ compared to Equation 2.1 is because q only contains the polarity of $y[\mathrm{n}-1]$. Here the state variable, $d[\mathrm{n}]$, is a multi-bit quantity that stores the cumulative sum of the 1-bit comparator decision, $q[\mathrm{n}]$. Since the output code of a ΔΣ is a time-encoded sequence where each sample is decoded from all prior samples, a state variable is needed to capture such "memory" effect of ΔΣ modulation. The z-transform of Equation 2.3 is

$$\frac{d[z]}{q[z]} = \frac{2 - z^{-1}}{1 - z^{-1}} \quad (2.4)$$

which has the characteristic response of a direct-form I IIR filter. In Fig. 2.2(b), the IIR filter is visually represented as a delay-free DT integrator $(1 - z^{-1})^{-1}$ and a unity-gain feedforward path from q to d. If $q[0] = d[0] = 0$, then $d[\mathrm{n}]$ is the cumulative sum of all q and $q[\mathrm{n}]$, *i.e.,* $d[\mathrm{n}] = q[\mathrm{n}] + \sum_{i=1}^{n} q[i]$, showing that one way of implementing the IIR filter is with an accumulator and adder. In this work, a 4-bit adder (with an extra overflow bit) was used; therefore, d has a 4-bit resolution.

A transient waveform of the proposed 1st-order ΔΣ with an IIR quantizer is shown in Fig. 2.3. The inclusion of the IIR filter results in the output bitstream, d, tracking u, as in a multi-bit modulator. Importantly, the IIR filter updates d synchronously with q, introducing no excess loop delay (ELD) and thus no stability concerns. As shown in Fig. 2.3, the IIR quantizer step size can be either ±D or ±3D, where D is the minimum step size. Consequently, the 4-bit IIR quantizer has higher quantization noise than a 4-bit Nyquist quantizer, whose quantization step is strictly D. A conservative quantization noise analysis reveals that the IIR quantization error, e_{q}, has a uniform probability density function (PDF) bounded between ±3D/2, thus resulting in a total integrated

quantization noise power of $9D^2/12$. Theoretically, the proposed IIR-ΔΣ has 14.6 dB lower quantization noise power than a single-bit ΔΣ while still being 9.5 dB higher than a true 4-bit ΔΣ. This is in close agreement with the simulated results shown in Fig. 2.4 of a 1st-order ΔΣ with an ideal 1-bit, 4-bit IIR, and 4-bit flash quantizer achieving 67.9, 81.3, and 90.7 dB SQNR, respectively, at an OSR of 250. Thermal noise was not included to ensure the modulator is quantization noise limited. For optimal prediction efficacy, the IIR step, 3Δ, should be larger than the maximum signal change in one sampling period. It can be shown that an OSR > 8 is needed

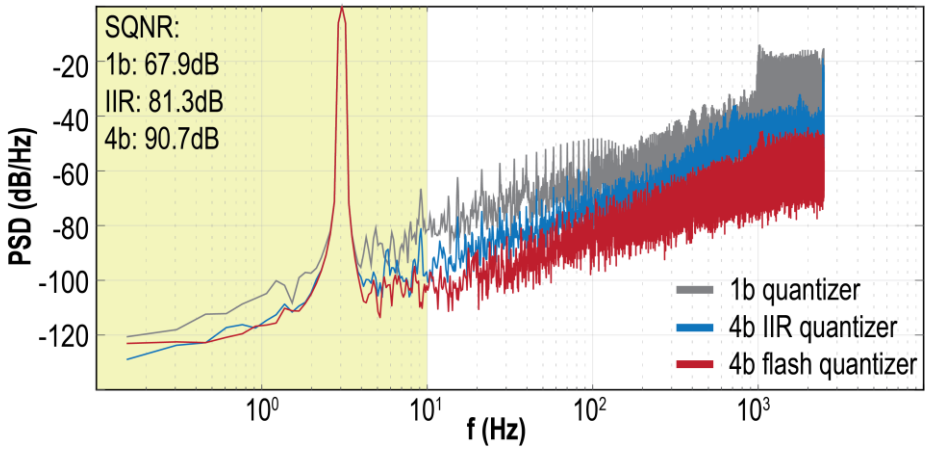


Figure 2.4 Simulated SQNR of a 1st-order ΔΣ with a 1-bit, 4-bit IIR, and 4-bit flash quantizer.

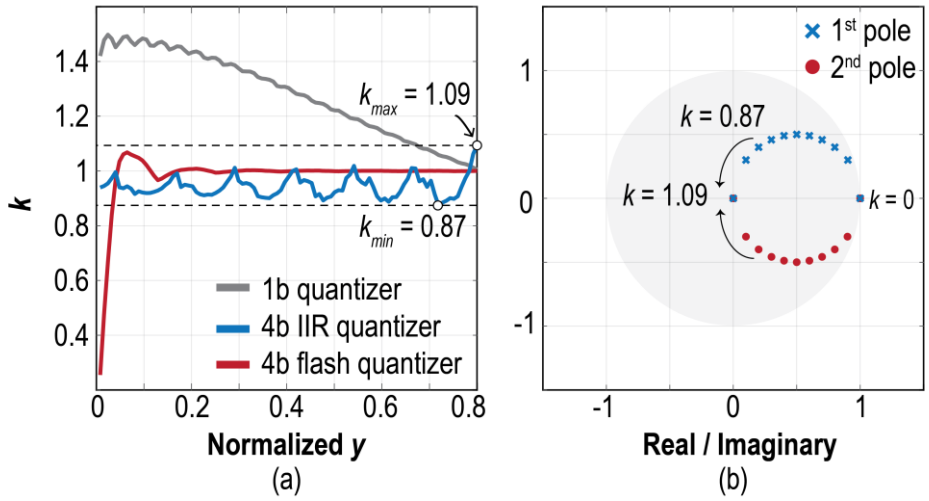


Figure 2.5 (a) Simulated quantizer gain, *k*, within the non-overloading range for 1-bit, 4-bit IIR, and mid-tread 4-bit flash quantizers; (b) root locus.

for a 4-bit IIR resolution, which sets a conservative lower bound for the OSR. However, as will be discussed later, an OSR > 64 ensures the STF and NTF of the proposed IIR-ΔΣ are identical to its 1-bit counterpart.

The quantizer gain, k, of a single-bit quantizer is determined by the statistical correlation between the input and output, specifically the slope of a straight line that minimizes the error between y and d for a given range of y [93], namely

$$k = \frac{\langle d, y \rangle}{\langle y, y \rangle} \tag{2.5}$$

where $\langle d, y \rangle$ is the cross-correlation between d and y and $\langle y, y \rangle$ is the autocorrelation of y. The simulated k values for a 1-bit, 4-bit IIR, and 4-bit flash quantizer are shown in Fig. 2.5(a). For illustration purposes, the quantizer input, y, was swept from 0 to 80% of the full-scale range (FSR), at which point $k_{1\mathrm{b}} = 1$, whereas in transient simulation, y was kept within 20% FSR for all u. As expected, k_{flash} has near unity gain and $k_{1\mathrm{b}}$ monotonically increases as y decreases resulting in an input-dependent gain. Importantly, k_{IIR} closely tracks k_{flash} with a minimum and maximum of 0.87 and 1.09, respectively. The variation of k_{IIR} exhibits input-dependence and the effect of varying k on the modulator's noise transfer function (NTF) is

$$NTF_{\mathrm{k}}(z) = \frac{\frac{2 - z^{-1}}{1 - z^{-1}}}{1 + L(z)k} \tag{2.6}$$

where $NTF_{\mathrm{k}}(z)$ is the NTF with a quantizer gain of k and $L(z)$ is the loop filter gain with $k = 1$. Fig. 2.5(b) shows a root locus with k varying from 0.87 to 1.09. The IIR quantizer introduces a pair of conjugate poles residing within the unit circle and therefore has a negligible impact on the modulator's stability.

The addition of the IIR filter changes the modulator's signal transfer function (STF) and NTF. Fig. 2.6(a) shows the equivalent analytical model for the proposed IIR-ΔΣ, where $p(t)$ is a

generalized pulse function representing the tri-level PWM DAC. In the case of a CT ΔΣ, the block diagram can be redrawn such that the CT integrator and sampler are rearranged to better visualize the STF and NTF. The STF in the CT domain is found by multiplying the CT integrator by the NTF evaluated at $e^{j2\pi f}$, *i.e.*

$$NTF(z) = (2 - z^{-1})(1 - z^{-1}) \tag{2.7}$$

$$STF(f) = \frac{1}{j2\pi f}\left(2 - e^{-j2\pi f}\right)\left(1 - e^{-j2\pi f}\right). \tag{2.8}$$

Fig. 2.6 shows the effect of the extra scaling factor $(2 - z^{-1})$ in the STF and NTF compared to a standard 1-bit CT ΔΣ. Although this extra term contributes to slightly higher out-of-band gain (OBG), its in-band effect is negligible, as can be seen when $f \to 0$, the $(2 - z^{-1})$

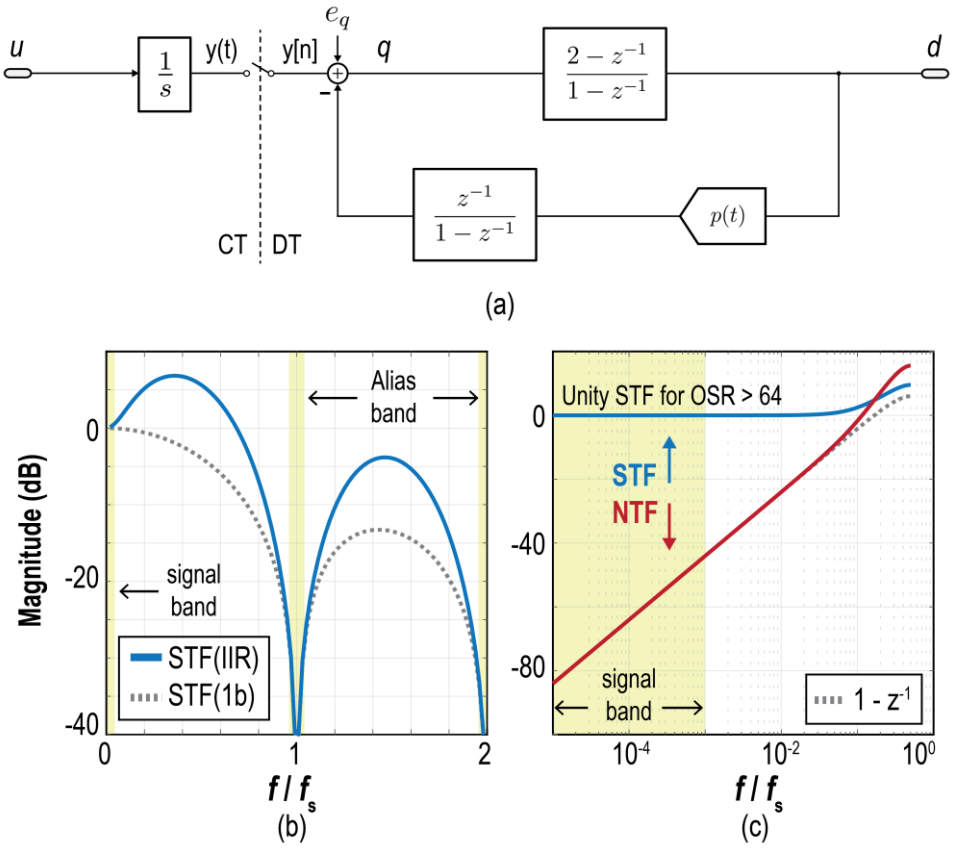


Figure 2.6 (a) Mathematical model of the IIR-ΔΣ separated into the continuous- and discrete-time domains; (b) STF of IIR-ΔΣ and 1-bit ΔΣ showing the inherent anti-aliasing and (c) STF and NTF of the IIR-ΔΣ.

term evaluates to unity. Fig. 2.6(b) shows that the modified STF preserves the inherent anti-aliasing property by having notches at integer multiple of f_s. For an OSR > 64, the IIR-ΔΣ has a nearly identical STF and NTF to its 1-bit counterpart, as shown in Fig. 2.6(c). The NTF's OBG is increased by ~9 dB, which results in a slight 2 dB loss in the maximum stable amplitude (MSA). The effect of increased OBG on MSA is more prominent in higher-order modulators [138]. It is also worth noting that in higher-order modulators, the *Bode sensitivity integral* suggests that higher OBG helps attenuate in-band noise (IBN) [93]; however, in an IIR-ΔΣ this has no effect due to the extra scaling factor.

2.3.3 Tri-level PWM DAC

The addition of an IIR filter necessitates a multi-bit DAC to close the loop. Since any nonlinearity introduced by the feedback DAC is directly added to input, the DAC must be as linear as the overall modulator. A conventional multi-bit DAC implementation uses unit or weighted cells with DEM or data-weighted averaging (DWA) to randomize/shape the mismatch [139], [140]. However, this typically results in a large area for an I-DAC as each current source transistor still needs to be sized relatively large to minimize the residue 1/*f* noise after DEM or DWA. It also has a power penalty from the circuitry used to generate the pseudo-random bit sequence [98]. As a result, an area- and power-efficient implementation is needed for multi-channel applications like μTIMES.

Critically, in a 1st-order CT ΔΣ, it can be shown that the modulator is insensitive to the shape of the feedback waveform as long as the total charge delivered in each cycle is proportional to the digital code, *i.e.*

$$\int_0^{T_s} p(t)\,dt = d[\mathrm{n}] \qquad 2.9$$

where $p(t)$ is the feedback pulse, $d[n]$ is the normalized output code, and T_s is the sampling period. In other words, feeding back a fraction of the reference for T_s is equivalent to feeding back the full-scale reference for the same fraction of T_s. The only difference is that for the latter, just a single unit DAC is needed, so nonidealities such as asymmetric rise/fall time introduce a constant offset common to all codes. To evenly partition T_s, a faster, synchronized clock can be used at the cost of increased jitter sensitivity. For example, in a 4-bit IIR implementation, a clock at $16/T_s$ can clock a 4-bit counter and generate a two-level PWM waveform, as shown in Fig. 2.7(a). The modulator output code, d, is held during each T_s and compared to the counter. The two-level PWM waveform is generated by combinatorial logic that determines if d is greater or equal to the counter.

Although a two-level PWM waveform is inherently linear, this work implements a tri-level PWM for better noise performance, as shown in Fig. 2.7(b). A dedicated "0" (shunt) state

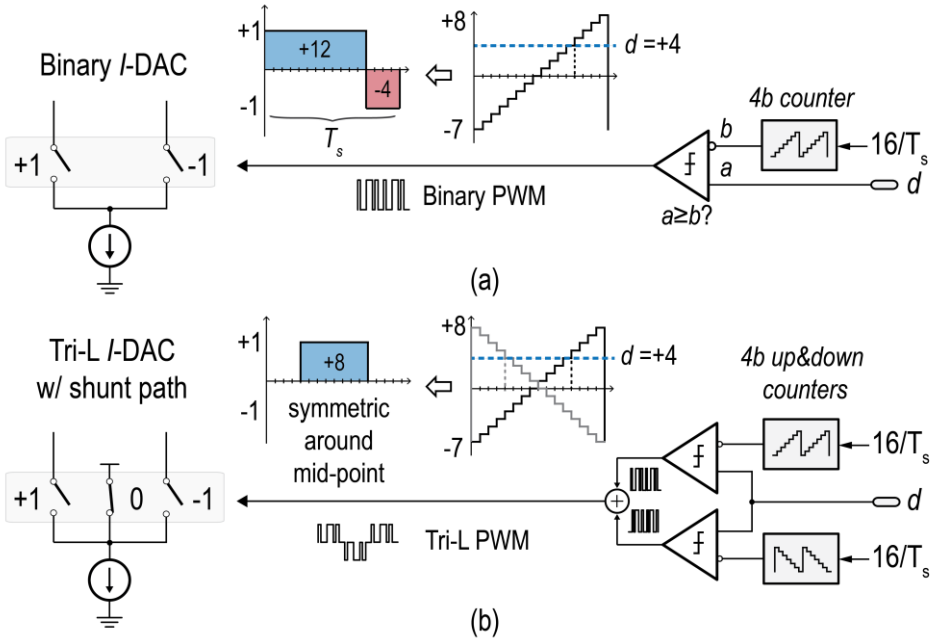


Figure 2.7 Visualization of (a) two-level PWM with current-steering DAC and (b) tri-level PWM with current-steering DAC with additional shunt path.

means linearity is no longer maintained with current source mismatch. The "0" state introduced by the tri-level PWM disconnects the feedback from the loop, effectively bypassing the current source's thermal noise, resulting in lower input-referred noise for small inputs. Combining two-level PWM signals, the tri-level PWM is essentially a half-scale return-to-zero (RZ) pulse train free of even-order distortion [141]. Reducing the feedback amplitude by half also relaxes the linearity requirement for the loop filter since the amplifier only needs to sink or source a fraction of the current. For the same reason, the tri-level PWM has a 6 dB lower jitter sensitivity than the two-level PWM. For all codes except ±1, the feedback pulse in a tri-level implementation is a fraction of the sampling period and symmetric around the midpoint. Thus, the tri-level PWM DAC is also robust against intersymbol interference (ISI).

The tri-level PWM is used to modulate an I-DAC. An I-DAC was chosen over its resistive counterpart (R-DAC) for two reasons. First, to partition a large DR over multiple references, the DAC should have scalability over a large range. For current sources, current-splitting can generate reference current over several decades while maintaining a relatively compact area. Second,

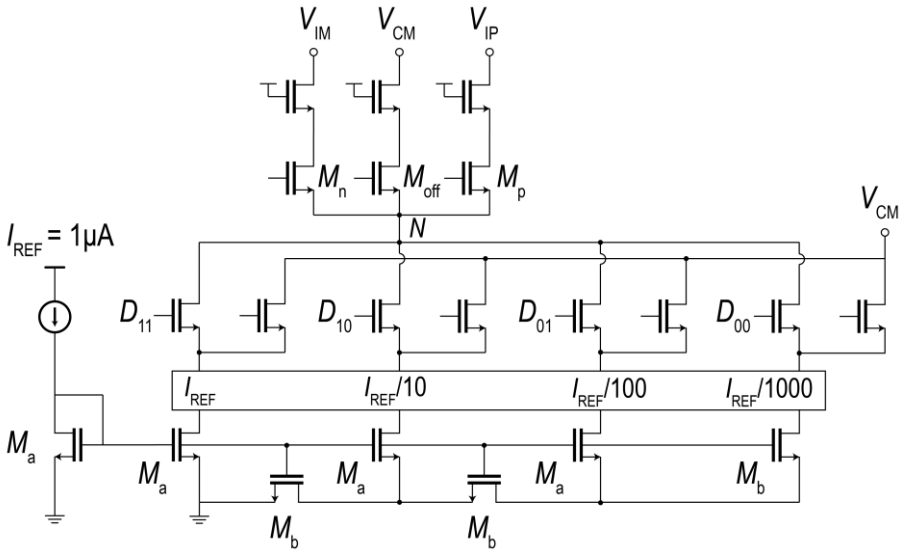


Figure 2.8 Circuit implementation of the large dynamic range current reference using current-splitting.

resistive loading from an R-DAC at the virtual ground reduces the loop gain around the loop filter. The situation is exacerbated when the resistors are large and have large parasitic capacitance. The reduced feedback factor increases the input-referred noise and degrades the integrator's linearity. In contrast, cascoded current sources ensure that the I-DAC has a large output impedance across the entire reference range.

2.4 Circuit Implementation

2.4.1 Current-splitting DAC

The reference for each channel is generated from a programmable 2-bit current-splitting DAC [102] that progressively divides a 1 mA reference current, I_{REF}, by a factor of 10× down to 1 nA, as shown in Fig. 2.8. Current-splitting is inherently linear, regardless of the transistor's region of operation. Transistors M_a and M_b form a ratiometric current-splitting chain, like an R-2R ladder. The current through each branch is proportional to the transistor's W/L where the unit transistor, M_b, is 10 mm/10 mm for low 1/f noise and good matching such that the relative error at I_{REF} = 1 nA is within 10%. Transistors M_a are proportionally sized 90 mm/10 mm for splitting by a factor of 10×. All transistors are biased in subthreshold, and M_a and M_b are implemented using

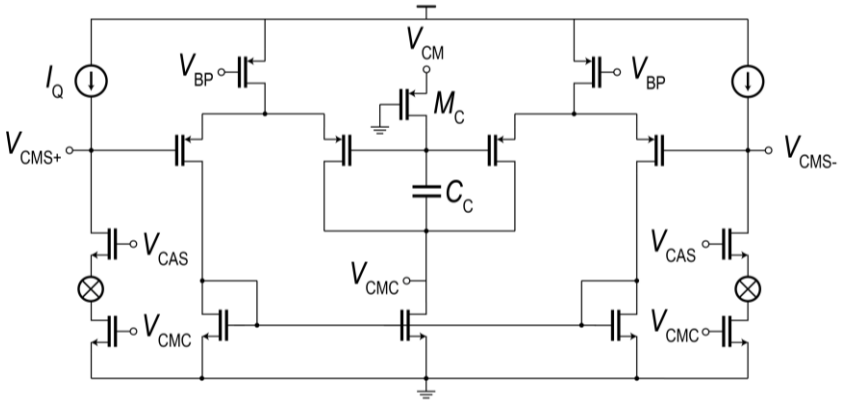


Figure 2.9 Circuit implementation of the CMFB amplifier (biasing not shown).

thick-oxide, deep n-well (DNW) devices to minimize leakage. Cascode transistors boost the output impedance by 160× to ensure negligible impact on overall input impedance seen by the sensor and precise current mirroring down to 1 nA. High output impedance in the I-DAC is also critical to ensure the virtual ground voltage does not modulate the current. When one of the four references is selected, the other three branches are shunted to V_{CM} at 0.9 V. The tri-level functionality is realized with switches M_p, M_n, and M_{off}, whose source voltages are always maintained at the virtual ground voltage, thus reducing the transition delay and distortion from signal-dependent perturbation at the tail node, N. Cascode transistors isolate the integrator inputs from the switching transistors to minimize distortion from clock feedthrough.

2.4.2 Input Common-Mode

Since the inputs are directly connected to high impedance on-chip electrodes, a system-level continuous-time common-mode feedback (CMFB) [142] is needed to set the input common-

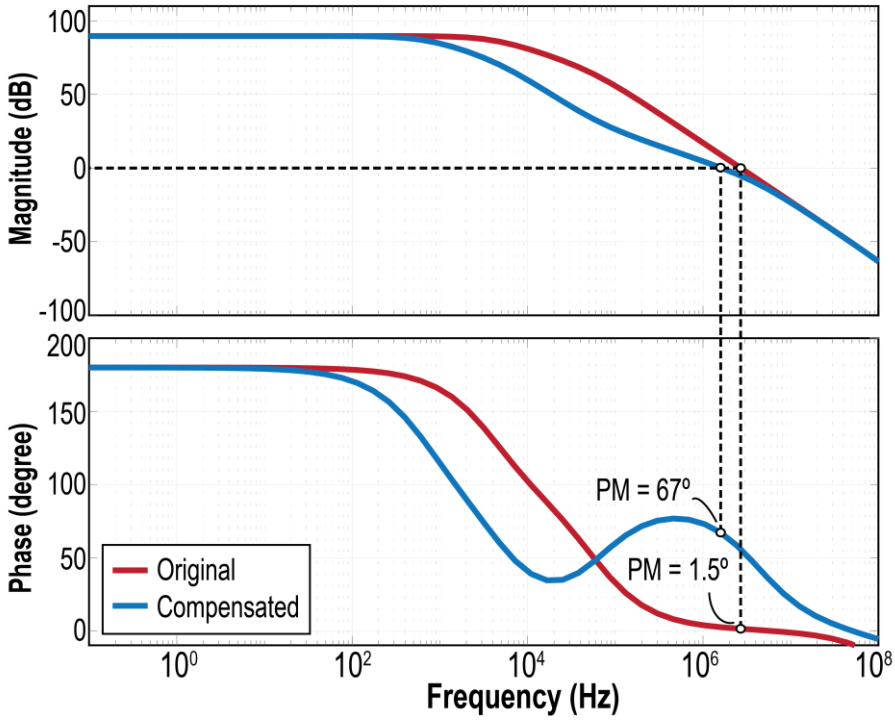


Figure 2.10 Simulated loop gain of CMFB with LHP zero compensation.

mode voltage while providing a high output impedance at the current summing nodes. The CMFB does not affect the normal operation of the modulator since the CMFB only responds to common-mode variation, whereas the I-DAC operates in differential-mode. As shown in Fig. 2.9, the CMFB consists of a two-stage differential difference amplifier (DDA) to ensure a high dc loop gain (> 90 dB) and minimize input common-mode offset while still allowing for large input swing. In the DDA, the four input transistors average and compare the differential input voltage, V_{CMS}, to the desired reference voltage, V_{CM}. The difference is then amplified and converted into a common-mode output current to adjust V_{CMS} until it matches V_{CM}. Similar to the I-DAC, the CMFB has a cascoded output stage (I_Q = 500 nA) for high output impedance such that the output current is independent of the virtual ground voltage. In this two-stage amplifier, the second stage contributes a pole at ~3 kHz, and the first stage has a second pole at ~30 kHz. As such, the two low-frequency poles result in less than 1.5° phase margin without compensation. A left-half-plane zero was added by connecting V_{CM} to a 10 pF capacitance, C_C, and a long-channel triode PMOS (220 nm/1 µm), M_C, with a ~250 kΩ impedance. These place zero near the unity-gain frequency, increasing the phase margin to 67°. Fig. 2.10 shows the simulated loop gain of the amplifier with and without the compensation. The conductance of M_C, and therefore the phase margin of the CMFB, will deviate due to process variation. A 100-point Monte Carlo simulation showed an average phase margin of 66° with a standard deviation of 5°, ensuring CMFB stability. At start-up, the input common-mode voltage is near ground. Therefore, only a PMOS-input CMFB is necessary to stabilize the input common-mode voltage to $V_{DD}/2$ and remains within the input-common range after that.

2.4.3 Chopper-stabilized OTA

A conservative rule of thumb is that the OTA dc gain should be approximately equal to the OSR such that the increase in quantization noise due to NTF zero shift is negligible [100].

However, finite integrator gain and the nonlinear nature of the quantizer can lead to dead-zones where the modulator is unresponsive to small input signals. Therefore, the dc gain requirement of the OTA in a 1st-order ΔΣ is particularly stringent. In this work, the OTA dc gain was chosen to be at least 80 dB. Because the feedback DAC is modulated at 16× of the sampling frequency, the OTA's unity-gain frequency (UGF) should be at least $16\times f_s$ = 80 kHz to avoid increasing the in-band noise (IBN) and nonlinearity.

A fully-differential folded-cascode amplifier was implemented for good energy efficiency and large output swing, as shown in Fig. 2.11. Large PMOS input transistors (40 mm/1 mm) were used to reduce 1/*f* noise while maximizing the g_m for low input-referred noise and offset. The other transistors are sized to have g_m/I_D > 18 S/A with a 1 mA bias current. Chopper stabilization was used at the inputs and low-impedance nodes of the cascode stage to further reduce 1/*f* noise and offset. A chopping frequency of $f_s/2$ was chosen to avoid noise folding. The CMFB is a DDA-based amplifier load compensated with a 10-pF capacitor to achieve a phase margin of 86°. A 1:5 current ratio was used to partition the CMFB and bias currents for robustness.

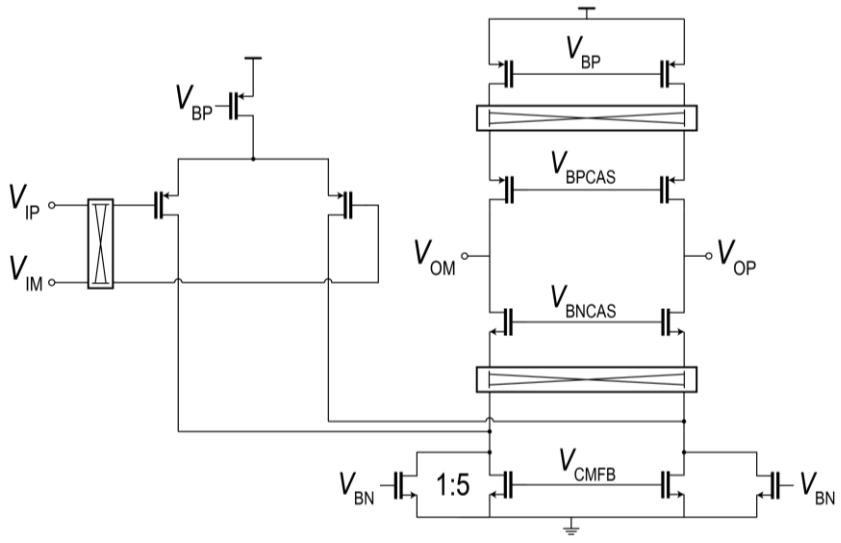


Figure 2.11 Circuit implementation of the chopper-stabilized folded-cascode OTA (biasing and CMFB not shown).

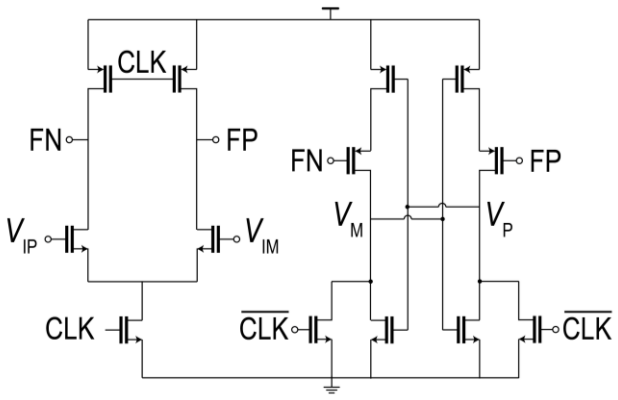


Figure 2.12 Circuit implementation of the dynamic comparator (SR-latch not shown).

From simulation of the extracted amplifier, the OTA has an 84 dB dc gain, 8 MHz unity-gain bandwidth, and an ~80 kHz 1/*f* corner. A 100-point Monte Carlo simulation shows a mean offset of 78 μV after chopping, with a standard deviation of 8 μV. Notably, the OTA offset voltage does not impact the modulator linearity but results in an offset current from the input impedance. The input-referred noise was reduced from 620 to 26 nV/ √ Hz with chopping at 100 kHz, which results in a negligible current noise of 4 fA_{rms} for the 20 MΩ input impedance of the modulator. The input-referred current noise is dominated by the shot noise and residual flicker noise of the CMFB (95%), while only a small fraction is contributed by the OTA (0.1%) and I-DAC (5%).

In current front-ends, the input impedance, R_{in}, is a critical parameter because an R_{in} too large will result in in-band noise peaking when combined with a large input capacitance, C_{in}, which considerably impacts the total noise performance [143]. The simulated input-impedance of the proposed front-end with the CMFB is ~110 kΩ at 10 Hz, which is sufficiently low to push the noise zero out of band with the load from the capacitance interface.

2.4.4 Comparator

The comparator is implemented by a preamplifier followed by a regenerative latch, as shown in Fig. 2.12. The preamplifier has a moderate gain of ~5 V/V to attenuate the noise from

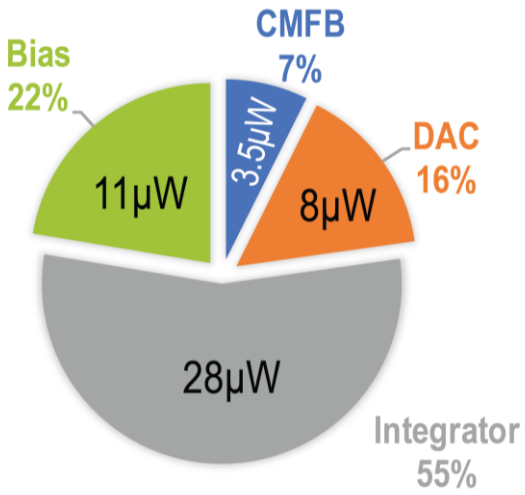


Figure 2.13 Measured power breakdown for each readout channel.

the latch. The propagation delay is less than 10 ns to minimize dead-zones and ELD. The output nodes of the latch, V_M and V_P, connect to an SR latch with high skew inverters to prevent false triggering and minimize dynamic errors. The input-referred noise of the comparator was simulated with transient noise (noisefmax = 10 MHz) and fitting the averaged comparator decisions to an error function for a given range of input offset [144]. The 6.2 mV_{rms} comparator noise is not a concern because the NTF significantly attenuates it.

2.5 Measurement Results

This design was fabricated in a 180 nm CMOS process and occupies 3×3 mm^2. As shown in Fig. 2.13, there are eight recording channels with four shared reference electrodes. The majority of the chip area is dedicated to on-chip sensors implemented on the top metal layer. The active area per readout channel is 0.11 mm^2, including the bias circuits. Electrical and *in-vitro* measurements were performed with the circuit enclosed in a dark faradic cage to suppress 60 Hz interference.

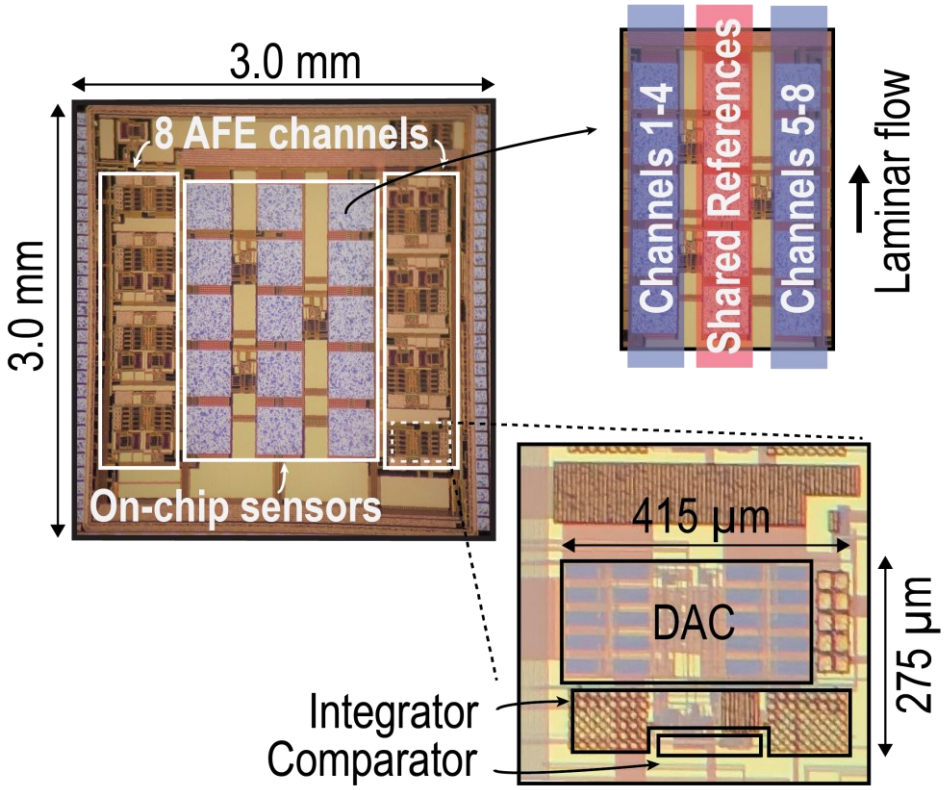


Figure 2.15 Die micrograph annotated with microfluidic channels.

2.5.1 Electrical Characterization

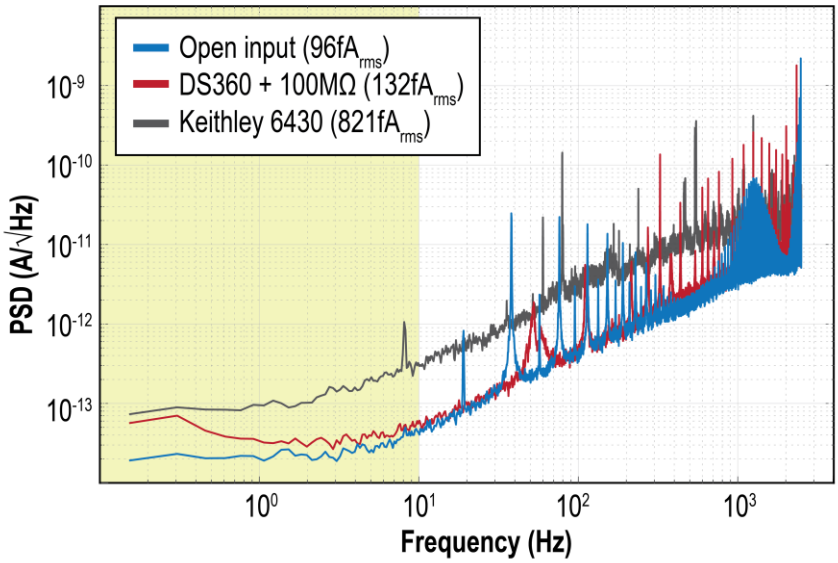


Figure 2.14 Measured input-referred current noise PSD with open input and different instruments.

With a 1.8 V supply and I_{REF} = 1 µA, the power consumption per channel is 50.3 µW, and the power breakdown is shown in Fig. 2.14. The digital IIR filter and tri-level PWM logic were implemented off-chip in an FPGA (Opal Kelly XEM6310). These circuits would consume 50 nW based on simulations using synthesized logic if implemented on-chip. Unless stated otherwise, all measurements were made with f_s = 5 kHz at an OSR of 250.

The total integrated input-referred noise (IRN) measured with the input floating (open input) was 96.2 fA_{rms} over a 10 Hz bandwidth, as shown in Fig. 2.15. For sensitive current sensing

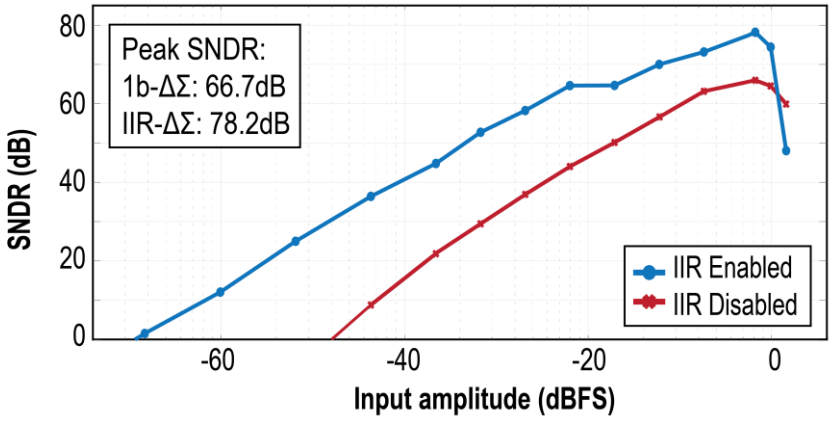


Figure 2.16 Measured SNDR vs. input amplitude of single-bit and IIR-ΔΣ.

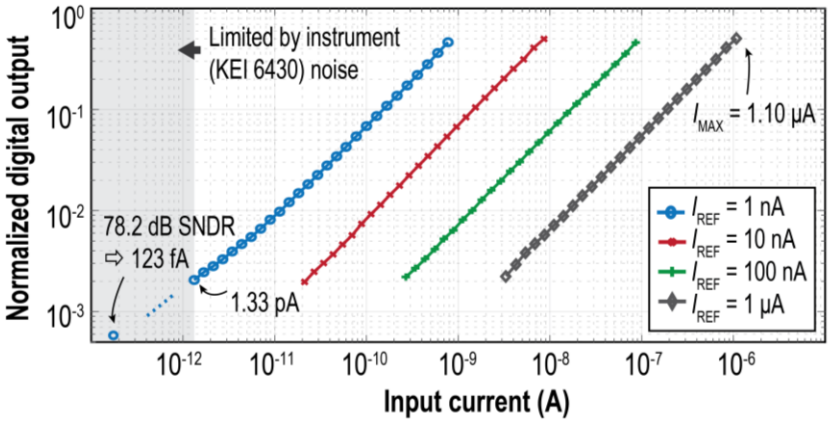


Figure 2.17 Measured cross-scale dynamic range of IIR-ΔΣ.

AFEs, capacitive loading at the input introduces a noise zero that directly amplifies the current noise and limits the resolution. Due to the added capacitive loading, using a sub-fA SourceMeter

(Keithley 6430), the measured IRN was 821 fArms. Isolating the instrument's capacitive loading through a 100 MΩ resistor reduced the noise to 132 fA_{rms}. The electrode's estimated electrical double-layer (EDL) capacitance in 1× HEPES is ~90 nF (~1 pF/μm^2). This large capacitive load increases input-referred current noise to ~1.2 pA_{rms} (890 fA_{rms} in simulation) in a 10 Hz bandwidth.

For ac measurements, a sinusoidal input current was generated by connecting a low-distortion function generator (SRS DS360) in series with a large resistor for *V*-to-*I* conversion. The resistor introduces a negligible current noise while significantly attenuating the voltage noise of the instrument. The series resistance and the input capacitance of the AFE also low-pass filter the instrument noise. Resistances of 1, 10, 100, and 5000 MΩ were used for input ranges of 1000, 100, 10, and 1 nA, respectively. With a 100 MΩ input resistance, it is shown in Fig. 2.15 that the *V*-to-*I* configuration leads to comparable IRN as the open-input configuration.

Fig. 2.16 shows the measured spectra of single-bit and IIR-ΔΣ with a –2 dBFS sinusoidal input at 3.052 Hz. The peak SNDR of the IIR-ΔΣ was 78.2 dB – an 11.5 dB improvement over its single-bit counterpart. This is slightly lower than the simulated 14.6 dB improvement shown in

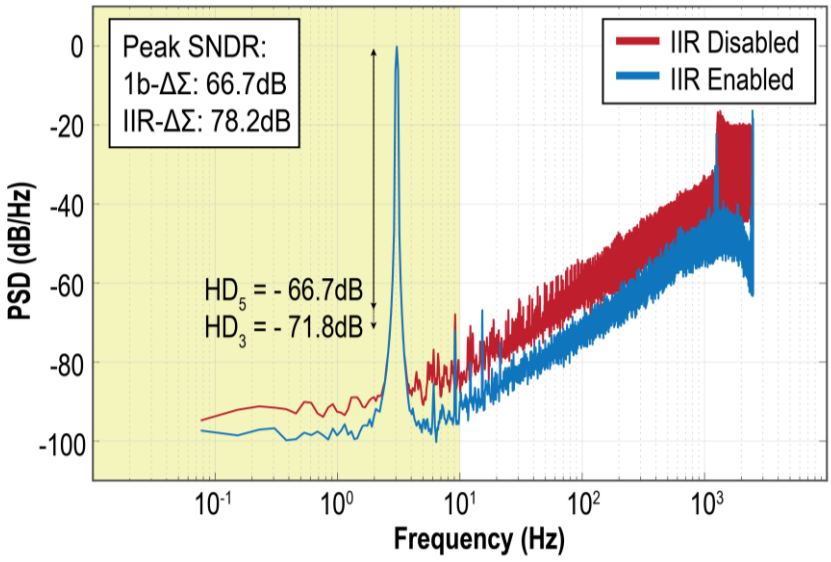


Figure 2.18 Measured peak SNDR for a single-bit and IIR-ΔΣ at -2 dBFS input

Fig. 2.4 due to increased harmonic distortion (HD), specifically HD_3 and HD_5 at -66.7 dB and -71.8 dB, respectively. The increased HD is due to mismatch in the tri-level PWM DAC. The measured relative error (from a stand-alone DAC test structure) increases as I_{REF} scales down from 0.12% at 1 μA to 9.9% at 1 nA.

Fig. 2.17 shows the SNDR plotted against the input amplitude. The measured DR demonstrates that the modulator has performance commiserate with a multi-bit quantizer by exhibiting a 21.5 dB improvement in the DR for low input amplitudes, where a significant amount of the current source

noise is shunted from the input by the "0" state of the tri-level PWM DAC. The SNDR of the IIR-ΔΣ rolls off much more sharply than its 1-bit counterpart for inputs larger than full-scale. To plot the entire working range of the reported AFE, a sub-fA SourceMeter was used to sweep the dc current from 100 fA to 1.1 μA. As shown in Fig. 2.18, the minimum was limited by the instrument and measured to be 1.33 pA, which is consistent with the integrated input-referred noise measured for the instrument shown previously. The sensitivity of 123 fA was defined by the peak SNDR measured at 1 nA reference. This AFE achieves a 78.2 dB DR and a 139 dB cross-scale DR.

2.5.2 *in-vitro* Measurements

The top metal of most CMOS processes is aluminum, which is prone to oxidation in ionic solutions. Therefore, before microfluidic assembly, the μTIMES chip was treated with an electroless nickel immersion gold (ENIG) to coat the sensor surface with gold. Fig. 2.19(a) shows the ENIG post-processed device. The microfluidics used in this work consists of two layers of polydimethylsiloxane (PDMS) to deliver reagents to the sensing area, as shown in Fig. 2.19(b). The microfluidic mold was fabricated by patterning a positive photoresist (SU8-2050) on a four-inch silicon wafer. The silicon wafer was cleaned with acetone, methanol, and isopropanol

sequentially with sonication. The surface was then treated with O_2 plasma (Technics PEIIB Planar Etcher). SU8 was spin-coated and patterned. Two 30-µm thick molds were formed on the wafer. The microfluidic flow cell was fabricated by pouring PDMS on the mold and curing it at 65 °C overnight. To bond the PDMS and µTIMES chips, ultraviolet/ozone treatment was used to activate the surface. Finally, the microfluidic blocks were aligned and bonded using an acrylic plate to apply pressure for sealing.

In the following proof-of-principle *in-vitro* experiment, Lysozyme, an enzyme that hydrolyzes polysaccharide chains, and its specific ligand, N,N,N"-triacetylchitotriose (NAG_3), were prepared in 1× HEPES buffer at 7.16 pH. A standard dialysis procedure was performed for the HEPES buffer to maintain buffer consistency throughout the experiment. A washing buffer

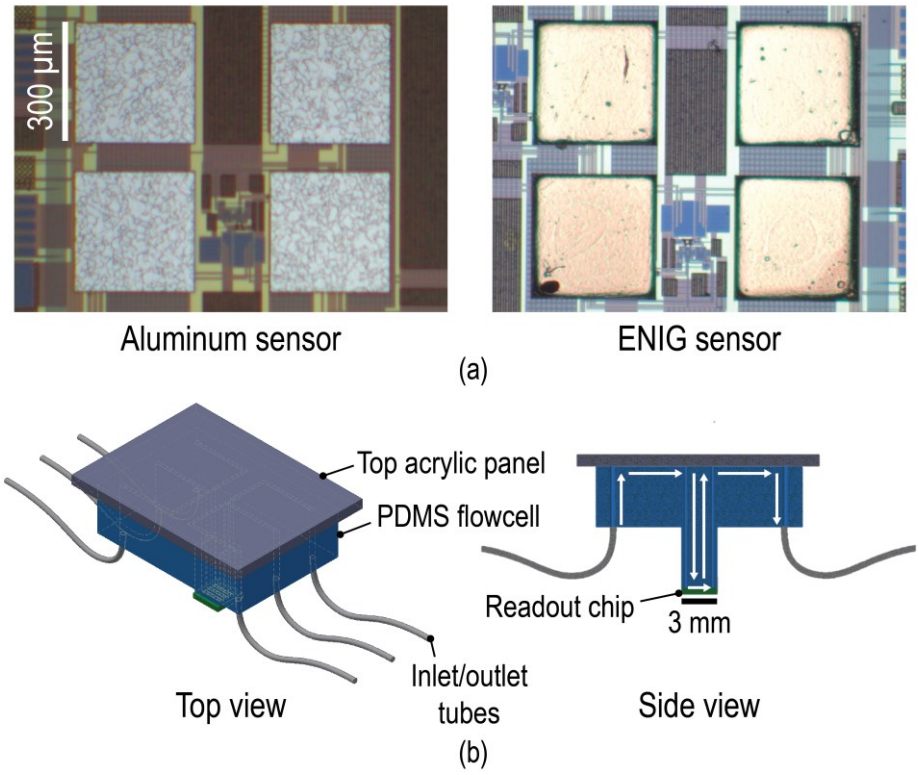


Figure 2.19 (a) Optical images of aluminum sensor surface post-treated with ENIG and (b) top and side view of PDMS microfluidic flow cell.

containing 25 mM tris, 150 mM NaCl, and 1% CHAPS was used to remove biomolecule residues and preserve ENIG integrity between experiments. All *in-vitro* experiments were performed at a pump rate of 10 μL/min to avoid channel leakage. Signals were decimated to a 10 Hz bandwidth without additional post-processing, such as offset removal and filtering. Each experiment was performed multiple times to verify the reproducibility. More TIMES experimental data can be found in [123]–[125].

At the start of an *in-vitro* flow experiment, the microfluidic channel with the reference sensor was filled with 1× HEPES buffer, and the channel with the working electrode was soaked in 1× HEPES buffer containing Lysozyme at different concentrations ($100 - 400$ μM). At $t = 20$ s when the syringe pump was turned on to displace the solution over the working electrode with buffer, the output current rose and settled at a new level dependent upon the Lysozyme concentration (Fig. 2.20). Between each Lysozyme run, the channel was rinsed with washing buffer to preserve sensor integrity and remove sensing artifacts due to the experiment sequence. This can be verified that the initial baseline for each run settled to a consistent value of 30 nA in Fig. 2.20.

The baseline signal (*i.e.,* response from 1× HEPES without Lysozyme) between running buffer over the working electrode and the still buffer over the background electrode is from the electro-osmosis effect where the pressure-driven flow caused a net ionic current near the electrode. In electro-osmotic flow, the velocity profile is constant along the cross-section of the channel, as opposed to a parabolic profile for a laminar flow. Assuming the system has a negative zeta potential, cations accumulate at the electrolyte/electrode interface, and the cations flow produces a net current immediately above the electrode. This ionic flow creates a voltage drop, thus changing the oxidation rate of the Au electrode. By adding Lysozyme to the buffer, the Lysozyme

adsorbed to the electrode and increased the effective spacing between the ions and the electrode, reducing the electro-osmosis-induced oxidation current. When the buffer solution is introduced to the channel, the absorbed Lysozyme are desorbed from the electrode surface, generating the signal corresponding to this dynamic process in Fig. 2.20. We demonstrate that the coupling of the microfluidic device and the electronic circuit allows us to characterize molecular coating on a surface, a key parameter for electrochemical biosensors where capture probes need to be deposited on metal surfaces with an optimal surface coverage.

Fig. 2.21 shows measured transient signatures for different protein-ligand configurations. The *in-vitro* data was sampled (50 kHz) and decimated (100 Hz) at a 10× faster rate to show clearer

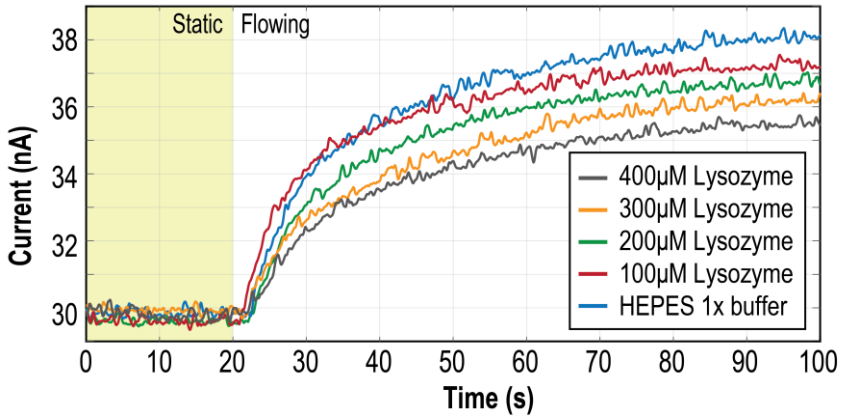


Figure 2.20 *in-vitro* measurement results of Lysozyme at various concentrations.

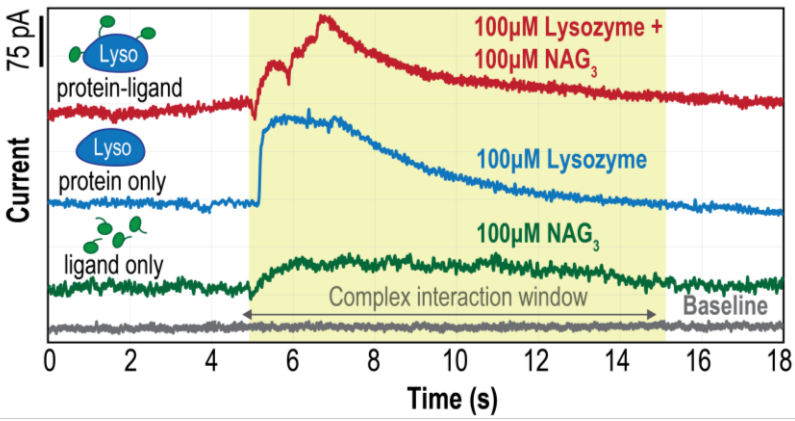


Figure 2.21 *in-vitro* measurement results of Lysozyme, NAG_3, and 1:1 mixture of Lysozyme and NAG_3.

Table 2-2 Comparison To Prior current sensing AFEs

	[97] Stanacevic TBCAS'07	[77] Li TBCAS'16	[96] Son TBCAS'17	[133] Ghoreishizadeh TBCAS'17	[99] Hsu ISSCC'18	[100] Wu ISSCC'21	[131] Lu TBCAS'21	**This work**
Toplogy	Inc. ΔΣ	Inc. ΔΣ	ΔΣ	TIA + SAR	Hourglass ΔΣ	ΔΣ	CC + *I*-to-*F*	IIR-ΔΣ
Process (nm)	500	500	350	350	180	55	180	180
On-chip Sensors?	×	×	×	Yes	×	×	×	Yes
# of Channels	16	50	1	1	1	1	1	8
Area/ch. (mm^2)	0.25**	0.157	0.5	0.6	0.2	0.585	3.17	0.11
Power/ch. (μW)	3.4	241	16.8	9,300	295	1011	25	50.3
Max Input (μA)	1	16	2.8	20	10	200	10	1.1
IRN* (fA) @ BW (Hz)	100 @ 0.1	100 @ 1	22,000 @ 10	470 @ 10	100 @ 1.8	2,000,000** @ 4k	87,000 @ 0.15	96 @ 10
DR (dB)	40**	54**	77.5	65.9**	160	140	58	78.2
Cross-scale DR (dB)	140	164	-	156	-	-	-	139
IRN Density (fA/√Hz)	316	100	6,960	149	74.5	31,600	225,000	30.3
FoM*** (pA^2μJ)	0.34	2.4	810	210	1.0	1,000,000	1,300,000	0.046

*Measured with open input
**Not explicitly given
***FoM=resolution^2×energy/conversion
Cross-scale DR = I_{MAX}/I_{MIN}
IRN: input-referred noise
Inc. ΔΣ: incremental ΔΣ
CC: current conveyor

temporal details. This experiment investigates the biochemical reaction produced by Lysozyme (protein), NAG_3 (ligand), and a 1:1 mixture of Lysozyme and NAG_3, which produces Lysozyme-NAG_3 complex having its concentration determined by the dissociation coefficient (*i.e.,* the inverse of the reaction constant) of the two molecules. In parallel experiments, sample solutions (Lysozyme, NAG_3, and Lysozyme-NAG_3 complex) were injected into the working channel to displace the buffer solution pre-filled at the start of each recording. The difference in the signal can be attributed to the dipole moment difference of each biomolecule compound as they approach the electrode. For the same concentration of Lysozyme and NAG_3, the resulting current of NAG_3 is noticeably lower than Lysozyme due to a much smaller dipole moment. On the other hand, even though the size, molecular weight, and dipole moment of NAG_3 are much smaller than those of Lysozyme, NAG_3 still significantly alters the structure stability and the dipole moment direction

of Lysozyme, giving rise to differently induced electrical responses. The signal produced by the mixture of NAG_3 and Lysozyme in a 1:1 ratio is not a superposition of signals from the individual molecules, suggesting that the two molecules react to form a protein-ligand complex. A detailed analysis of the waveforms allows one to obtain the dissociation coefficient of the reaction.

Table 2-2 compares this work to other state-of-the-art current sensing front-ends. This work achieves the best input-referred current noise density of 30.3 fA/√Hz by utilizing linear prediction and a return-to-open I-DAC in the feedback loop. The added digital logic contributed little power (and area) overhead. The resolution-to-power tradeoff was captured by the resolution-FoM, which is widely used to characterize the power efficiency of sensor front-ends [4], [14], [145]. This work achieves the best FoM of 0.046 $pA^2\mu J$, which is 7.4× better than other current sensing front-ends. While it is tempting to scale down the reference current, I_{REF}, to attempt a better resolution-FoM, the overall signal-to-noise ratio (SNR) is compromised with a smaller input range. Therefore, it is not a good design strategy to shrink I_{REF} only for noise purposes. The merit of this work is that it achieves the best resolution-FoM while having a comparable dynamic range to other work listed in Table 2-2. It is also worth noting that the high resolution achieved by this work is not from having a small I-DAC reference. Instead, it is from the advantage of using a tri-level PWM I-DAC where most I-DAC noise is shunted away from input.

Chapter 2, in part, is based on the material from Da Ying, Chi-Yang Tseng, Ping-Wei Chen, Yu-Hwa Lo, and Drew A. Hall, "A 30.3 fA/√Hz Biosensing Current Front-End with 139 dB Cross-Scale Dynamic Range, *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, vol. 15, no. 6, Dec 2021. The dissertation author was the primary investigator and author of this paper.

Chapter 3. NEUROTRANSMITTER CURRENT FRONT-END

3.1 Introduction

The nervous system controls nearly all bodily functions by directing communication between the various organs. This coordination occurs through electrical (*i.e.*, action potentials propagating along axons) and chemical (*i.e.*, release and uptake of neurotransmitters across synaptic junctions) signaling [146]–[149]. Accurate action potential monitoring has been achieved with large-array extra-/intra-cellular voltage recording front-ends [150]–[153]. Quantitatively studying neurotransmitters is also important in neurological research as disturbances in these chemical messengers influence numerous health conditions, including addiction, anxiety, cognition, and movement disorders [154]–[157]. Dopamine is a neurotransmitter closely linked to

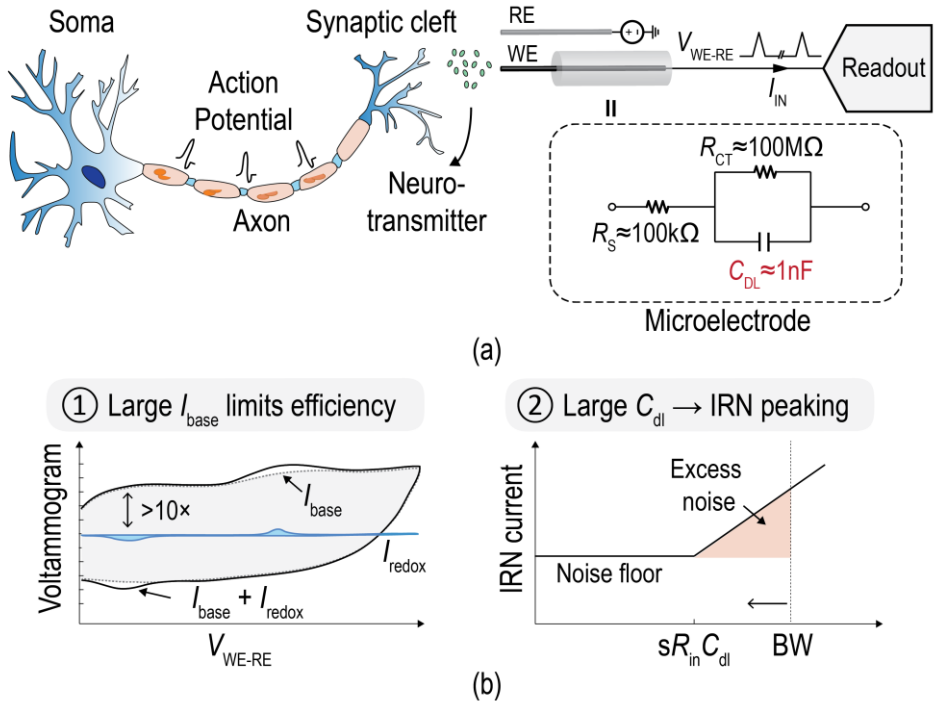


Figure 3.1 (a) Overview of a neurotransmitter model and typical FSCV readout system; (b) practical challenges in FSCV front-end designs.

reward-motivated behavior, and its dysfunction is often involved in many psychiatric disorders like schizophrenia and Parkinson's disease [158].

Several techniques have been proposed for neurotransmitter detection and real-time monitoring to diagnose and analyze neurological diseases. For example, nuclear medicine tomographic imaging (single-photon [159] and two-photon [160]) detects photon emission from a radioactive tracer injected intravenously to map neuronal activity in three dimensions. Optical techniques such as Raman spectroscopy [161] or Forster resonance energy transfer (FRET) [162] can also observe neurotransmitters with high sensitivity. Since most neurotransmitters are electroactive, electrochemical techniques such as amperometry [163] and fast-scan cyclic voltammetry (FSCV) [164]–[166] have gained popularity as a non-optical alternative. Fig. 3.1(a) illustrates a typical FSCV system in which microelectrodes rapidly sweep the potential to oxidize and reduce analytes of interest. The redox current is measured and plotted as a function of the applied potential. The resulting voltammogram provides a "fingerprint" for analyte identification and quantification [167]. As such, FSCV can achieve excellent spatial and temporal resolution.

Like most current-sensing circuits, an FSCV analog front-end's (AFE) performance is heavily affected by capacitive loading from the sensor. With electrochemical sensors, the input capacitance is dominated by the double-layer capacitance, C_{dl}, due to the electrode-electrolyte interface, which is typically a few nanofarads [40], [168]. This large C_{dl} is particularly problematic in FSCV since the working electrode (WE) is swept at 300-400 V/s for high temporal resolution, which unavoidably introduces a large (300-400 nA) non-faradaic current, I_{BG}, superimposed on the much smaller faradaic signal current, I_{redox} (< 10 nA), as shown in Fig. 3.1(b).

There has been increasing effort in integrating FSCV AFEs with wireless telemetry to enable real-time monitoring of dopamine release in freely moving small animals necessitating low-

power designs [169], [41], [170]–[173], [78], [174], [175], [130]. These designs have two main issues: the non-faradaic background current and the input impedance since it is tied to the noise performance. The large I_{BG} has typically been dealt with by recording a reference scan at the start of the experiment to capture a neurotransmitter-free background signal that is subtracted from subsequent scans in software. However, resolving the quasi-repetitive large background current requires an AFE with a high dynamic range (DR), increasing the power consumption. Therefore, several techniques have been reported to cancel I_{BG} such that the AFE output is primarily I_{redox} from the neurotransmitter of interest. In [41], a digital signal processor (DSP) performed background subtraction on-chip, but with a significant area and power cost. In [170] and [176], a two-step approach stored and subtracted I_{BG} after the transimpedance stage; however, this still requires the ADC and DAC to have high DR. The lowest power design, described in [177], cancels I_{BG} prior to it seeing the front-end with a coarse subtraction, but the nonlinear nature of an FSCV signal requires sophisticated calibration to be effective. The second challenge described in Fig. 3.1(b) is the need for a low input impedance, R_{in}. A small R_{in} is crucial so that the noise zero introduced by $sR_{in}C_{dl}$ is beyond the signal bandwidth.

In this work, we overcome the aforementioned challenges using a pseudo-differential sensing scheme and a common-mode rejection (CMR) circuit that cancels I_{BG} before seeing the front-end. When the electrode properties (*e.g.*, electrolyte, material, size) are nominally the same, C_{dl} (and therefore I_{BG}) track and can be turned into a common-mode (CM) signal that is canceled by a CMR circuit in the front-end. In Fig. 3.2, the proposed *in-vivo* system is shown, where the main WE is placed in the dorsal striatum, and a replica WE is placed in a less active region. The two WEs are surrounded by cerebrospinal fluid (CSF), a common body fluid found in vertebrates' brains, and thus present similar C_{dl} at the front-end input. The resulting differential current is only

the faradaic and residual background current copied to a current-mode ADC by a class-AB regulated current conveyor (RCC) for low input impedance. The ADC is implemented as a 1st-order delta-sigma (ΔΣ) modulator with an assisted-operational transconductance amplifier (OTA) and an infinite impulse response (IIR) quantizer for high energy efficiency [97], [178]. The proposed architecture can tolerate I_{BG} up to 290 nA without a differential linearity penalty, achieving an effective DR of 83 dB. Furthermore, it has the lowest input-referred noise (39.2 pA_{rms}) over a 5 kHz bandwidth when loaded with a 1 nF input capacitance (26.5 pA_{rms} with open input) while consuming only 3.7 µW since the AFE power was optimized to only resolve the small redox current.

3.2 System Architecture

The key concept in this work is the combination of a pseudo-differential sensing scheme and a CM rejection circuit at the AFE input such that a significant portion of I_{BG} is eliminated. As a result, the front-end's DR can be reduced, thus decreasing the system power. Fig. 3.2 shows the proposed FSCV architecture, which measures the current from two carbon-fiber microelectrodes

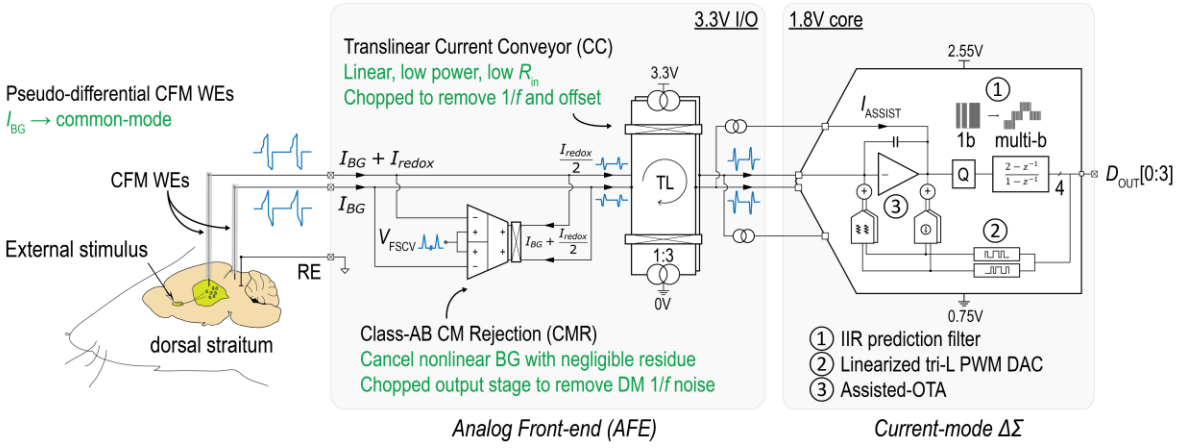


Figure 3.2 System architecture of the proposed pseudo-differential FSCV front-end with background current cancellation.

(CFM) and a shared Ag/AgCl reference electrode (RE). The double-layer capacitance, C_{dl}, given by the Helmholtz model, is

$$C_{\mathrm{dl}} = \frac{\epsilon_0 \epsilon_{\mathrm{r}} A}{t} \tag{3.1}$$

where ϵ_0 and ϵ_{r} are the free space permittivity and the electrolyte's relative permittivity, respectively, A is the electrode's surface area, and t is the Helmholtz double-layer thickness in CSF [40], [168]. According to Equation 3.1, CFMs with similar physical properties (*e.g.*, material, dimension) in the same electrolyte have similar capacitances. For a CFM with a μm diameter, C_{dl} is ~1 nF, which is much larger than the capacitance from electrode interconnects (<10 pF) and AFE input (~ pF). The large capacitance at the AFE input makes designing an FSCV front-end challenging, specifically the DR, frequency response, and noise performance.

From an architectural perspective, existing FSCV AFEs can be categorized by their domain of operation. In voltage-mode AFEs [170], [175], the input current is converted into a voltage followed by a voltage-mode quantizer. The transimpedance elements are sized proportionally to the DR, often in a large array when the input signal spans many orders of magnitude. Whereas in current-mode AFEs, for example, a current-mode ΔΣ (I-ΔΣ), directly quantize current signals without area and power consumed by an extra transimpedance stage [41], [171], [176]. However, the DR often necessitates a higher-order modulator and cannot be directly connected to the electrode since the 1.4 V_{pp} FSCV waveform introduces a large voltage excursion on the DAC, compromising the linearity of the modulator. This work uses a current-mode architecture for a compact design and high current efficiency while isolating the ADC from the FSCV waveform to prevent linearity degradation seen in prior work [41], [169].

In an FSCV measurement, the WE is swept across a voltage range to observe the two-electron redox reaction between dopamine and its oxidized form, dopamine-ortho-quinone. The

oxidization and reduction potentials for dopamine are 0.7 and –0.1 V, respectively [146]. Due to CSF's high conductivity and the small currents in FSCV, a two-electrode setup with no counter electrode (CE) was chosen over a potentiostat [165]. The WEs are swept from –0.4 to 1.0 V relative to the RE at 300 V/s with a 10 Hz interval, resulting in a 9.3 ms scan time. To ensure sufficient headroom, a 3.3 V supply was used for the AFE, while a 1.8 V supply was used for the ADC for better energy efficiency. The Ag/AgCl RE is biased at the AFE CM voltage (V_{CM}), 1.65 V. To center the V_{CM} of the AFE and ADC, the ADC ground is biased at 0.75 V requiring that all NMOS transistors in the ADC are in a deep N-well such that they are isolated from the substrate. Using a 1.8-V supply for the ADC more than doubles the energy efficiency; however, such a dual-supply scheme complicates the supply generation, possibly reducing the benefit of doing so when fully integrated.

As shown in Fig. 3.2, the large I_{BG} resulting from charging and discharging C_{dl} is a CM input to the front-end and absorbed by a class-AB CMR circuit. The push-pull nature helps handle large bidirectional CM signals with a quiescent current that is a small fraction of the peak current. This allows the proposed AFE to have low average power. The FSCV voltage waveform modulates the positive terminal of the CMR circuit, which drives both WEs at the negative terminals to the desired scan voltages through negative feedback.

The CMR circuit absorbs half of the signal due to the pseudo-differential configuration. The I_{redox} and residue I_{BG} from mismatch enter the RCC serving as a current buffer before the ADC. Dynamic element matching (DEM) was implemented to remove flicker (1/*f*) noise and mismatch from the current mirrors. A current gain of 3× was chosen to balance the noise and ADC DR. Unlike other CC variants [179], the RCC is fully-differential with the quiescent current, I_Q, well-defined by a translinear input stage, which also operates in class-AB and has a well-defined

R_{in}. An I_Q of 50 nA was budgeted to be 2.5× more than the current needed to support a maximum dopamine concentrations of 1 μM. This allows the AFE to tolerate a ~10% mismatch in C_{dl} when swept at 300 V/s. For a typical nF value of C_{dl}, R_{in} needs to be less than 30 kΩ for the noise concern described above, which is difficult to achieve with an open-loop CC structure whose R_{in} is ~$1/g_m$ and on the order of a few hundred kΩ. Therefore, amplifiers were used to cascode-regulate the CC to further reduce its input impedance for low input-referred noise in the presence of large C_{dl}.

The physiological range of dopamine means I_{redox} can span up to 60 dB. To not have the ADC limit the DR, a 12-bit 1st-order I-ΔΣ digitizes the RCC output current at a moderate oversampling ratio (OSR) of 128. Compared to a conventional 1-bit modulator, this work utilizes an IIR filter after the comparator to realize an equivalent multi-bit quantization for improved resolution at a low power and area overhead. A single-bit R-DAC is used for low noise and inherently linear tri-level feedback. In addition, the OTA output is assisted with a replica of both the input (simply with an extra mirror branch in CC) and feedback signals such that it can be low power while achieving >70 dB linearity.

3.3 Circuit Implementation

3.3.1 Class-AB Common-Mode Rejection (CMR) Circuit

The CMR circuit shown in Fig. 3.3 is implemented by a two-stage differential-difference amplifier (DDA) with two input pairs and a class-AB output stage. The structure is connected in unity-gain feedback such that it acts similar to current-mode common-mode feedback (CMFB) with bipolar current driving capability [180]. The operation of the CMR circuit can be described as follows. During a measurement, the 1.4 V_{pp} FSCV waveform, V_{FSCV}, directly modulates the positive terminals of the DDA, which drive the WEs to the same voltage through negative

feedback. When both V_{I1} and V_{I2} are equal to V_{FSCV}, the DDA is in equilibrium and drives zero current from output V_{O1} and V_{O2}. Now suppose both V_{I1} and V_{I2} are momentarily larger than V_{FSCV} with the drains of M_1/M_4 and M_2/M_3 shorted, the DDA input pairs inject more current to the drain of M_{10} than M_9, raising V_N, therefore, causing M_{13} to sink more current (than M_{14} sources) and pulls down V_{I1} and V_{I2} until they match V_{FSCV}. When the DDA is in equilibrium, M_{13} and M_{14} each carry a 50-nA quiescent current, I_Q. If V_{I1} and V_{I2} are significantly larger than V_{FSCV}, V_N increases and turns off M_8 (more). This causes M_{12} to source less current and V_P to go up, turning off M_{14}

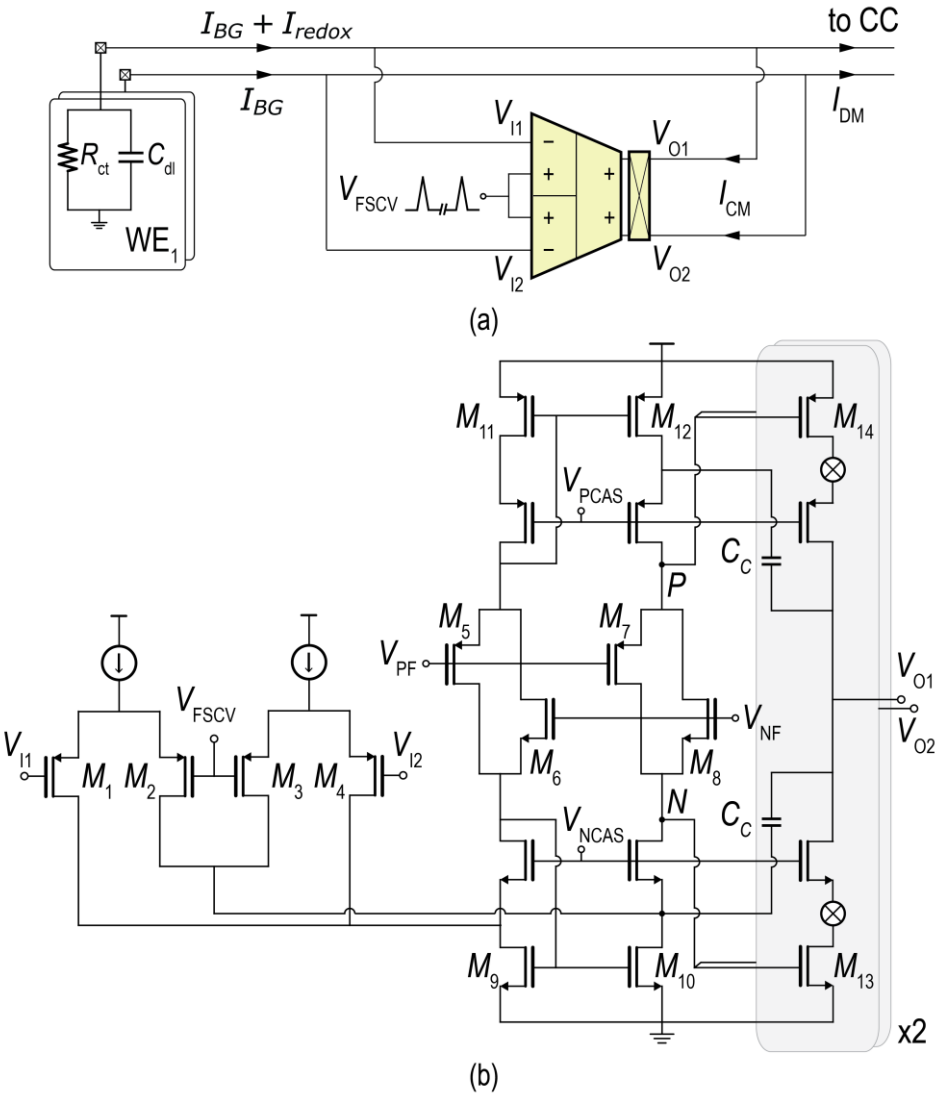


Figure 3.3 (a) Block diagram of the class-AB CMR circuit and (b) schematic.

further while M_{13} is sinking more current. This push-pull operation allows the bi-directional current driving capability of more than $6\times I_Q$.

All transistors in the CMR circuit are I/O devices operating in subthreshold with $V_{DSAT} \approx$ 100 mV and remain in strong inversion even with large CM voltage variation. The DDA input pairs, $M_1 - M_4$, were sized to have a large aspect ratio with a g_m/I_D of 22 S/A. Two floating current sources, M_5/M_6 and M_7/M_8, each carry 250 nA such that a total of 300 nA flows through M_9 and M_{10}. Simulation showed that a large current in the cascode stage is necessary for fast settling during an FSCV scan cycle. The floating current sources bias the cascode stage precisely and allow V_N and V_P to swing near the supplies. As a result, the class-AB output stage can sink or source the amount of current necessary to maintain the correct voltages on both terminals. The simulated dc loop gain was 105 dB with a unity-gain frequency of 8.2 kHz, which is accurate and fast enough to settle a 1.4 V_{pp} FSCV triangular waveform.

Since the CMR circuit is connected in unity-gain feedback, its current noise is directly referred to the input. With the folded DDA stage shared between the two output stages, $M_1 - M_{12}$ contribute only CM noise. Chopping (f_{chop} = 100 kHz) removes the amplifier's $1/f$ noise and offset. After chopping, the CMR input-referred current noise was reduced from 86 to 17.36 pA_{rms} in simulation. In practice, input imbalance (electrode impedance, transistor mismatch, etc.) will lead to imperfect CM noise cancellation from the CMR amplifier. With a 10% electrode and CMR amplifier mismatch, the input-referred noise increased by 15% in Monte-Carlo simulations.

Stability is another design concern, especially when interfaced with a large reactive load. Cascode compensation was chosen over Miller compensation because the former offers a faster transient response (from having a smaller C_C) and does not introduce a right-half-plane zero [181].

As shown in Fig. 3.3, a 4.5 pF capacitor is connected from V_{O1} to the drain of M_{10} (and another to M_{13}), an internal low impedance node, resulting in an 80° phase margin at C_{dl} = 1 nF.

3.3.2 Fully-Differential Regulated Current Conveyor (RCC)

The RCC isolates the ADC from the electrodes preventing the large CM excursion from deteriorating the ADC linearity while also providing a low input impedance for noise purposes. Fig. 3.4 shows the implementation of the RCC, which stems from a classic second-generation current conveyor (CCII) biased by a translinear (TL) stage for class-AB operation [81]. The TL principle ensures accurate voltage tracking from node X to Y while defining a PVT-insensitive 50 nA I_Q flowing through transistors $M_{N1,2}$ and $M_{P1,2}$. With a 3.3-V supply, all transistors are in strong inversion, tolerating up to a 2 V_{pp} input with a negligible impact on the linearity.

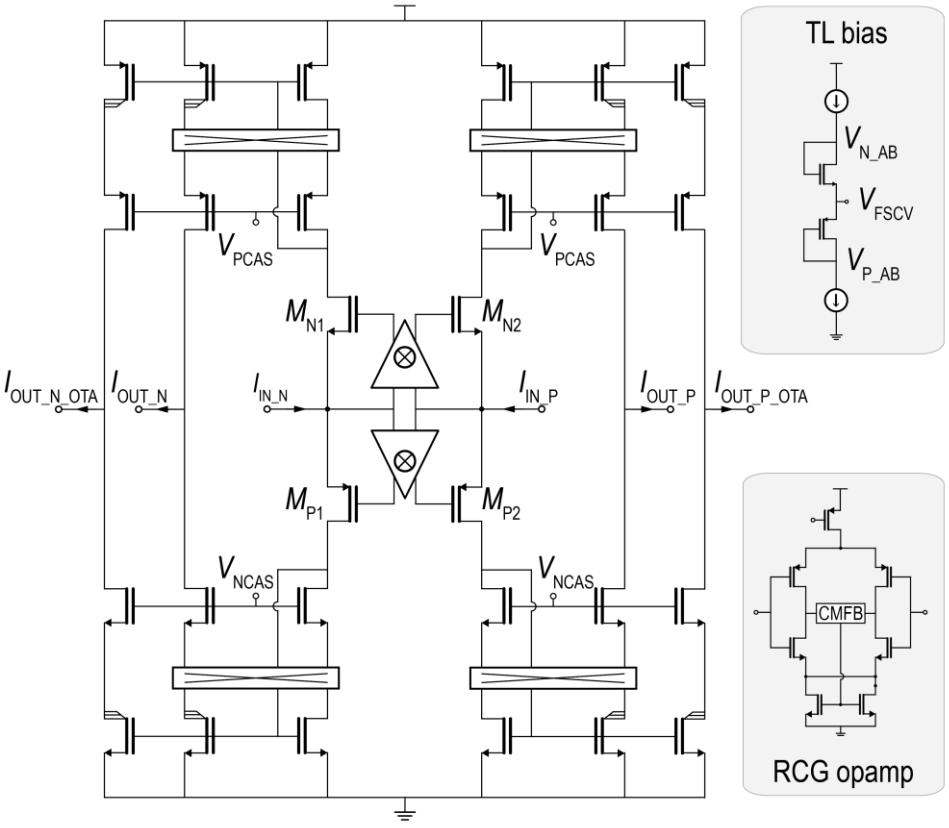


Figure 3.4 Circuit implementation of the class-AB RCC.

One issue with the original TL-based CC is that its input impedance is solely determined by the transconductance, g_m, of the input transistors, which is highly dependent on process and I_Q. The transistors have a small g_m for a low power design, resulting in a large input impedance. For example, $R_{in} \approx 500$ kΩ at $I_Q = 50$ nA, placing the noise zero from s$R_{in}C_{dl}$ at 320 Hz, well below the targeted 5 kHz bandwidth, thus significantly increasing the input-referred noise. To address this, a regulated common-gate (RCG) structure was integrated within the TL loop with a high-gain opamp actively driving the gates of the input transistors, $M_{N1,2}$ and $M_{P1,2}$, reducing R_{in} by the opamp's open-loop gain, A_{reg}. The opamp was designed with a complementary, current-reuse structure for high current efficiency. The opamp has a 41-dB dc gain and 13-MHz unity-gain frequency in simulation. The regulated TL operation can be intuitively understood as follows: when an influx of current tries to raise the input voltage, the opamps steer the gates of $M_{N1,2}$ and $M_{P1,2}$ in the opposite direction. This simultaneously reduces and increases the current through $M_{N1,2}$ and $M_{P1,2}$, respectively, counterbalancing the input voltage while maintaining the class-AB operation of the TL loop. The loop was simulated and had more than 70° phase margin across the 1.4 V_{pp} input range.

Fig. 3.5 shows the simulated bandwidth improvement from RCC, with an R_{in} of ~4.5 kΩ. The dc operating point of $M_{N1,2}$ and $M_{P1,2}$ is maintained by setting the opamp output CM voltage to $V_{N\text{-}AB}$ and $V_{P\text{-}AB}$, the original bias voltage defined by the TL stage. Fig. 3.6 shows the simulated noise contribution from the combined CMR and RCC blocks. If the PMOS and NMOS input transistors have equal g_m, then the total input-referred current noise, including the CMR stage, can be written as

$$\overline{i_{n,rms}^2} = 2q(I_{CMR} + I_{CC})\left(1 + s\frac{1}{2A_{reg}g_m}C_{dl}\right)^2 + \overline{v_{n,op}^2}\left(\frac{1 + sR_{ct}C_{dl}}{R_{ct}}\right)^2 \qquad 3.2$$

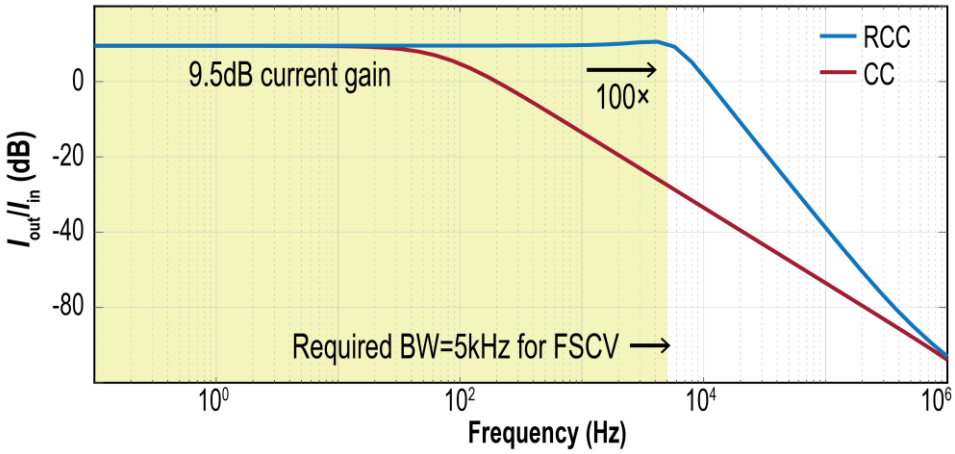


Figure 3.5 Simulated bandwidth improvement from the RCC.

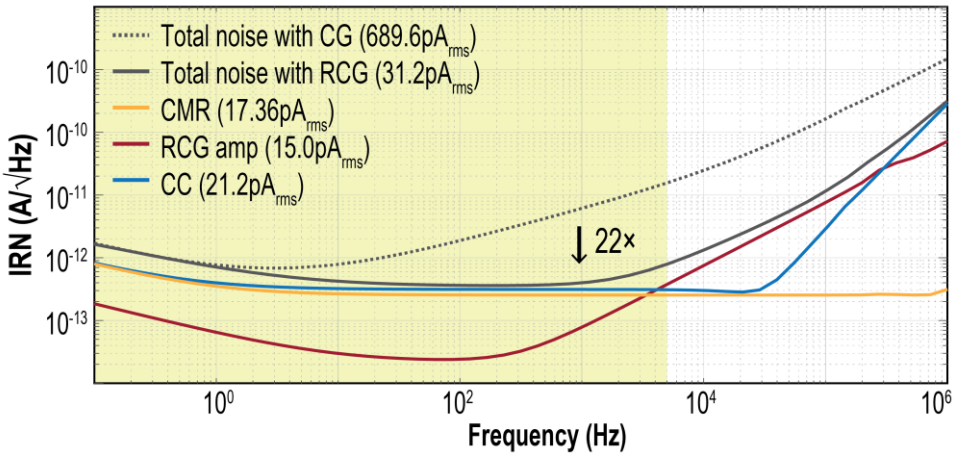


Figure 3.6 Simulated input-referred noise of the CMR and RCC.

where q is the electron charge, I_{CMR} and I_{CC} are the bias currents of the CMR and CC, respectively, $\overline{v_{n,op}^2}$ is the input-referred noise voltage of the opamp, and R_{ct} is the electrode's charge transfer resistance, which is >100 MΩ for CFMs. The first term in Equation 3.2 is the shot noise of the CMR and CC, whereas the second term is the opamp noise reflected into a current by the input impedance (*i.e.,* $R_{ct}||1/sC_{dl}$). For the opamp to contribute negligibly to the overall noise, it was designed to have a 40-nV/√Hz noise floor for a noise efficiency factor (NEF) of 2.4. DEM reduces the 1/f noise and mismatch from the 1:3 current mirror. The total input-referred noise current with

C_{dl} = 1 nF was reduced from 689.6 to 31.2 pA_{rms} with DEM in simulation. The dominant inband noise is the shot noise from the CMR circuit, while the opamp dominates the high-frequency noise.

3.3.3 Energy-Efficient IIR-ΔΣ

It was shown in [97] that modifying a 1st-order 1-bit ΔΣ with an IIR predictor and tri-level pulse width modulated (PWM) DAC can realize the equivalent performance of a multi-bit ΔΣ in an area- and power-efficient manner. As shown in Fig. 3.7, the IIR filter can be implemented as a delay-free, discrete-time integrator and a unity-gain feedforward path from the 1-bit quantizer output, q, to the modulator output, d. It was also shown that d[n] could be derived from the cumulative sum of all q[n], *i.e.,* $d[\mathrm{n}] = q[\mathrm{n}] + \sum_{i=1}^{n} q[i]$. Therefore, the IIR predictor can be simply realized with a digital accumulator and adder [97]. The same digital implementation was used in this work, and d has a 4-bit resolution.

A multi-bit DAC is needed to close the loop, and it must be as linear as the modulator. Taking advantage of a 1st-order continuous-time ΔΣ being insensitive to the shape of the feedback waveform, d is encoded in time by modulating the duty cycle of a single DAC unit. In [178], where the noise was critical, the tri-level feedback DAC was modulated by a tri-level control sequence

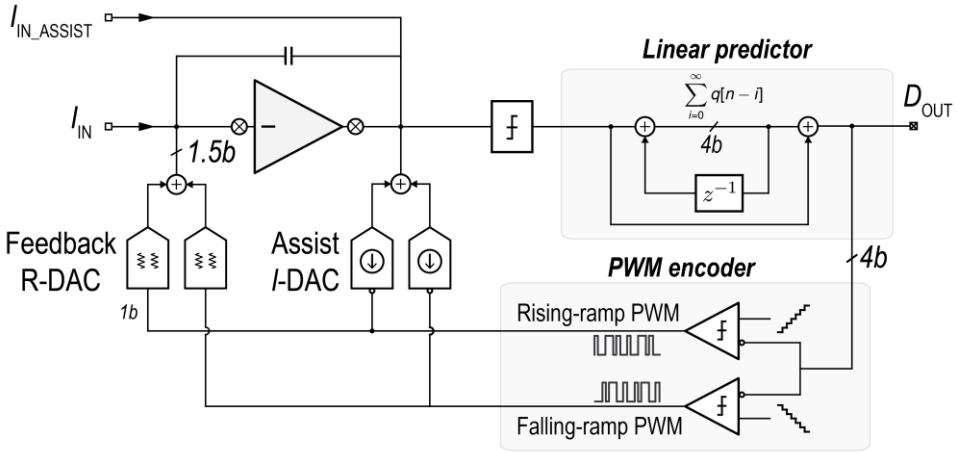


Figure 3.7 Block diagram of the current-mode IIR-ΔΣ.

(0 and ±1) such that the "0" state shunts away DAC noise for smaller inputs. But without mismatch shaping, the intrinsic DAC linearity was not preserved across codes, as shown in Fig. 3.8(a). This work solves this problem by splitting the tri-level DAC into two 1-bit DACs and summing the currents at the modulator's virtual ground to improve linearity without using a multi-bit current source. As shown in Fig. 3.8(b), each split DAC is controlled by a 1-bit PWM signal with complementary phases such that the sum of the two pulses is a return-to-zero (RZ) waveform symmetric around the mid-point in each sample period. By not having a discrete "0" feedback level, the resulting tri-level DAC is linear by averaging the mismatch across codes, similar to a tri-level DAC with rotational DEM [182].

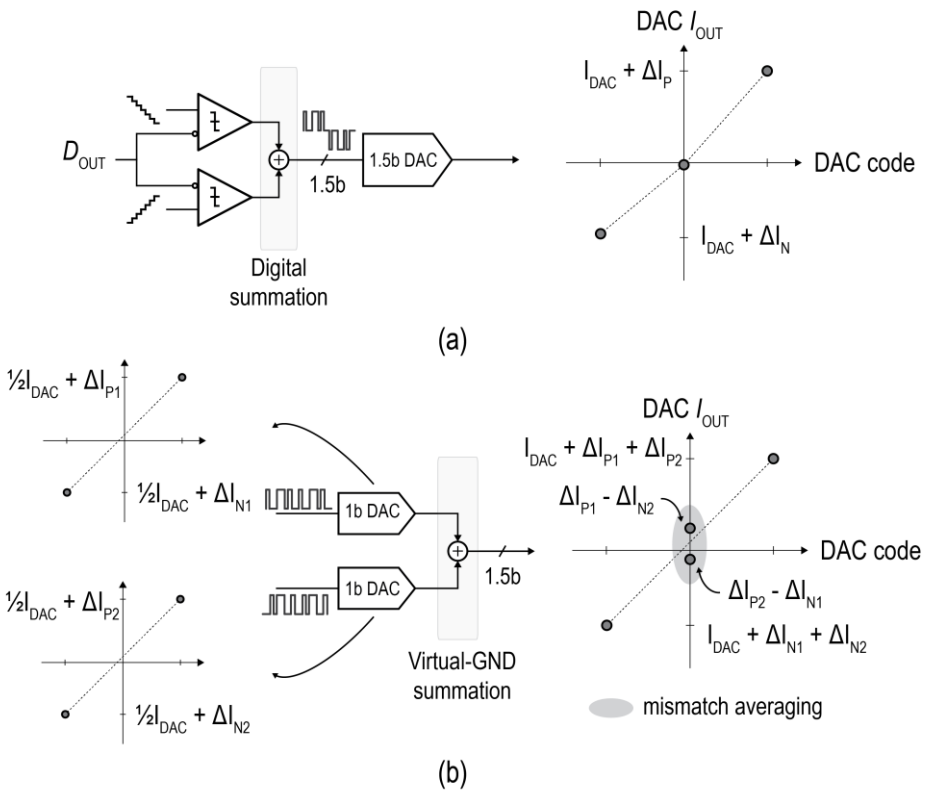


Figure 3.8 Block diagram and linearity of (a) non-linear tri-level feedback DAC and (b) proposed linearized tri-level feedback DAC.

A resistive DAC (R-DAC) was used for lower thermal noise than a current-steering DAC. The impact of reduced loop-gain due to the DAC impedance was negligible with OTA assistance, where a DAC current replica, *I-DAC*$_a$, is injected directly at the OTA output, effectively bypassing

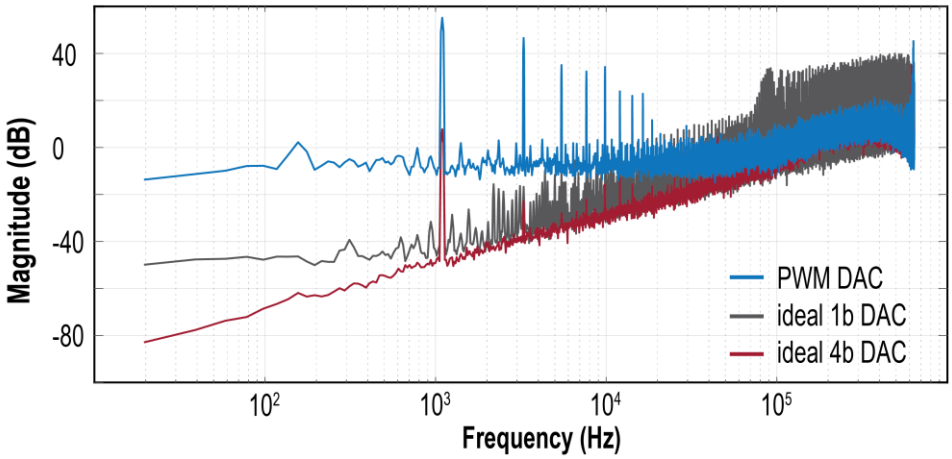


Figure 3.9 Comparison of the harmonic content from PWM DAC and an ideal 1b/4b DAC at the virtual ground of the IIR-ΔΣ.

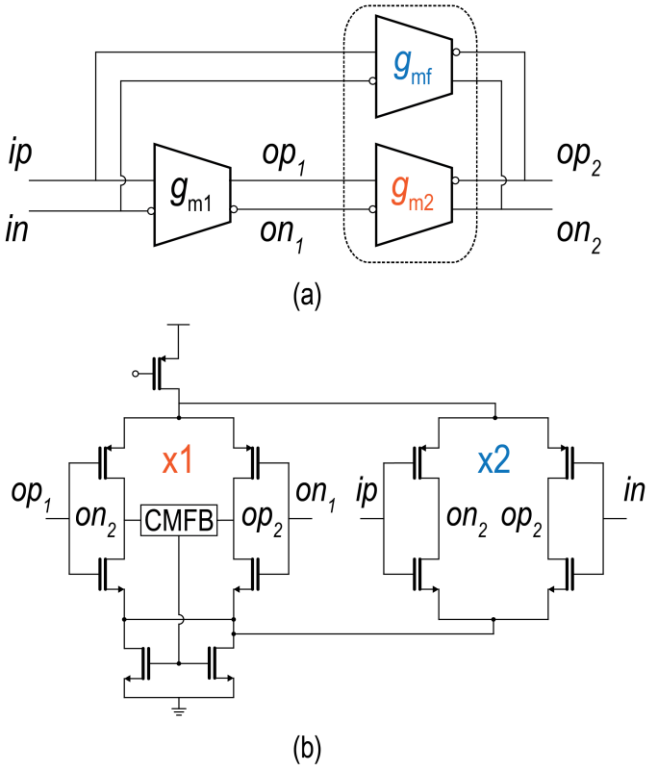


Figure 3.10 (a) Block diagram and (b) circuit implementation of feed-forward inverter-based OTA.

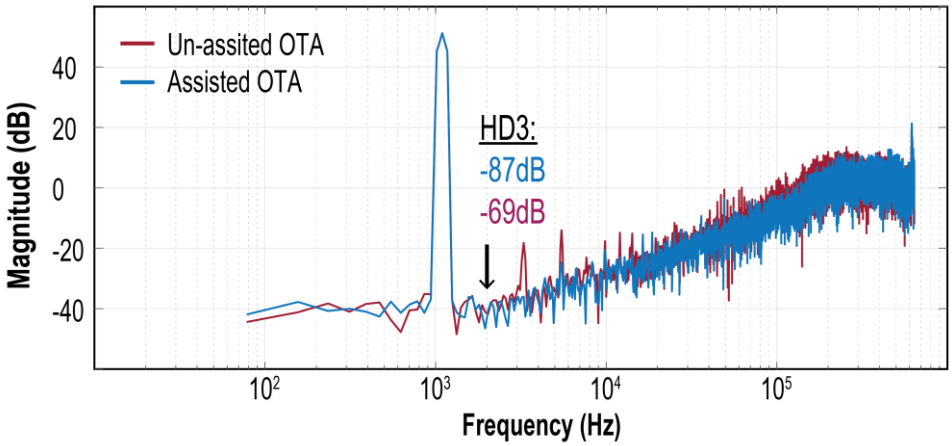


Figure 3.11 Simulated spectrua of IIR-ΔΣ with OTA-assistance at -2 dBFS.

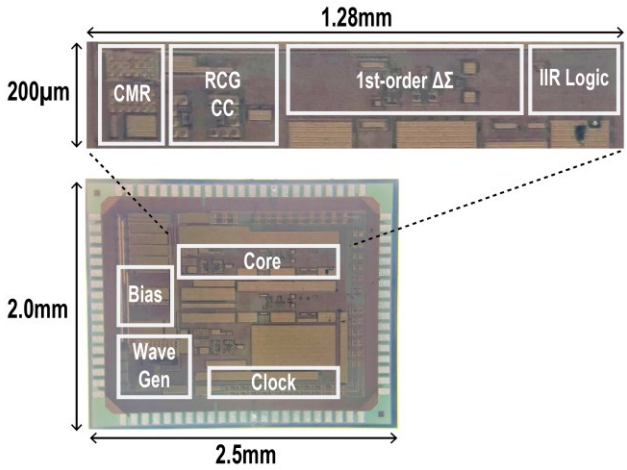


Figure 3.12 Die micrograph of proposed FSCV AFE.

the OTA from processing the DAC signals, therefore improving the linearity [183], as shown in Fig. 3.7. Since the nonlinearity, noise, and mismatch (to the R-DAC) of the assistance DAC are suppressed when input-referred, an *I*-DAC was used to provide minimum loading at the OTA output. Shunting also improves the OTA tolerance to an increased harmonic content at the virtual ground due to the PWM DAC compared to its single-bit and multi-bit counterparts, as shown in Fig. 3.9.

The OTA was implemented with high energy efficiency (NEF = 1.7) by a two-stage current-reuse amplifier, as shown in Fig. 3.10. The first-stage amplifier was designed with a low quiescent current of 200 nA and long-channel (L = 1 μm) input devices with a 40 dB gain and a dominant pole at ~20 kHz. The second stage provides an additional 20 dB of gain. The feedforward transconductance stage, g_{m3}, adds a left-half-plane (LHP) zero controlled by the ratio of g_{m2} and g_{mf} (1:2) and cancels the non-dominant pole contributed by the 2nd stage. Feedforward compensation was chosen to avoid energy consumed by charging/discharging the compensation capacitor, C_C, and the extra assistant branch needed for Miller compensation [183]. In extracted simulations, the two-stage OTA has a 64 dB dc gain and a 54 MHz unity-gain bandwidth (UGBW). The OTA stability was verified with a 200-point Monte Carlo simulation and showed a mean phase margin of 72° (σ = 1.4°). As shown in Fig. 3.11, transient noise simulation shows that the ADC's peak SNDR with the assisted-OTA is 72.1 dB, which is >5 dB better than the unassisted case and >11 dB more than the IIR-disabled case.

3.4 Measurement Results

The proposed FSCV front-end was fabricated in a 180 nm CMOS process with the digital IIR filter and tri-level PWM logic synthesized on-chip. As shown in Fig. 3.12, the AFE and ADC have an active area of 1.28 × 0.2 mm^2. The AFE was implemented with thick-oxide (3.3 V) devices to tolerate a 1.4 V_{pp} FSCV waveform, whereas the ADC and digital back-end used 1.8 V core devices. The ADC and synthesized logic were placed inside a deep n-well with an elevated ground voltage of 0.75 V to center the AFE output and ADC input CM voltage at 1.65 V. With a deep n-well, substrate coupling between the digital and analog circuits is minimized. Electrical and *in-*

vitro measurements were performed with the device enclosed in a dark faradic cage to suppress 60 Hz interference and photodiode leakage currents.

3.4.1 Electrical Characterization

The measured static power consumption of the proposed FSCV front-end is 35.25 µW, among which the AFE and ADC consume 24.8 µW and 10.44 µW, respectively. When averaged over a 10-Hz FSCV cycle (9.3 ms active), the average active power consumption is 3.74 µW. The power breakdown is shown in Fig. 3.13. Unless stated otherwise, all measurements were taken with f_s = 1.28 MHz for an OSR of 128, which is sufficiently large for the IIR filter not to affect the modulator's STF and NTF [178]. The integrated input-referred noise (IRN) current measured with open inputs was 26.5 pA_{rms} in a 5 kHz bandwidth, as shown in Fig. 3.14, demonstrating that

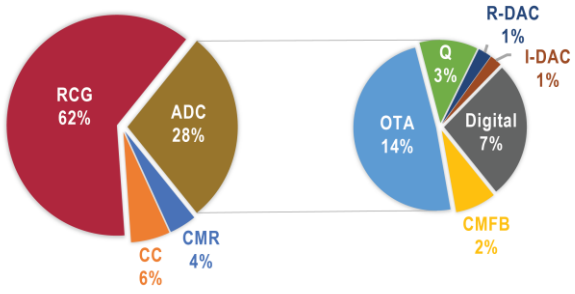


Figure 3.13 Measured power breakdown of proposed FSCV AFE.

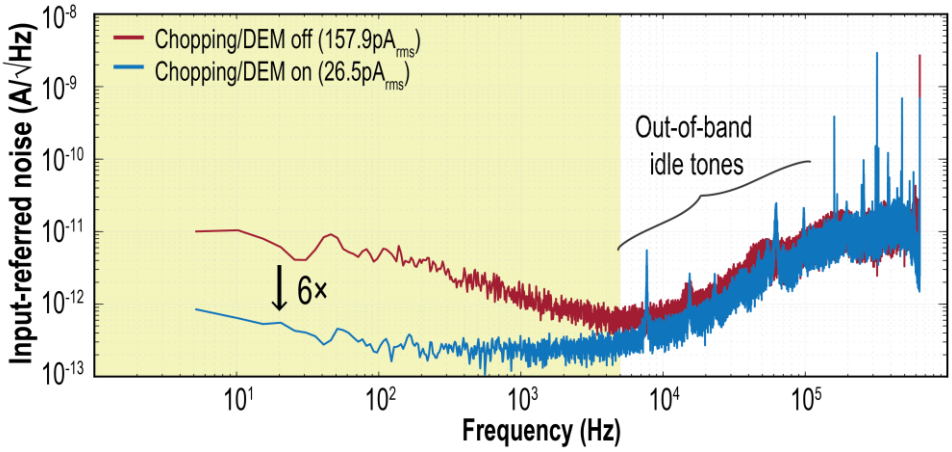


Figure 3.14 Measured input-referred current noise PSD (open input).

chopping reduces the IRN by more than 6×. For sensitive current sensing, capacitive loading at the AFE input introduces a noise zero, amplifying the current noise and limiting resolution. The CFM electrode's double-layer capacitance in 1× HEPES is ~1 nF. Due to the relatively low input impedance, this capacitive loading increases the input-referred current noise from 26.5 to 39.2 pA_{rms} in a 5 kHz bandwidth. Fig. 3.15 shows the measured IRN at four discrete input loading conditions (100, 250, 500, and 1000 pF).

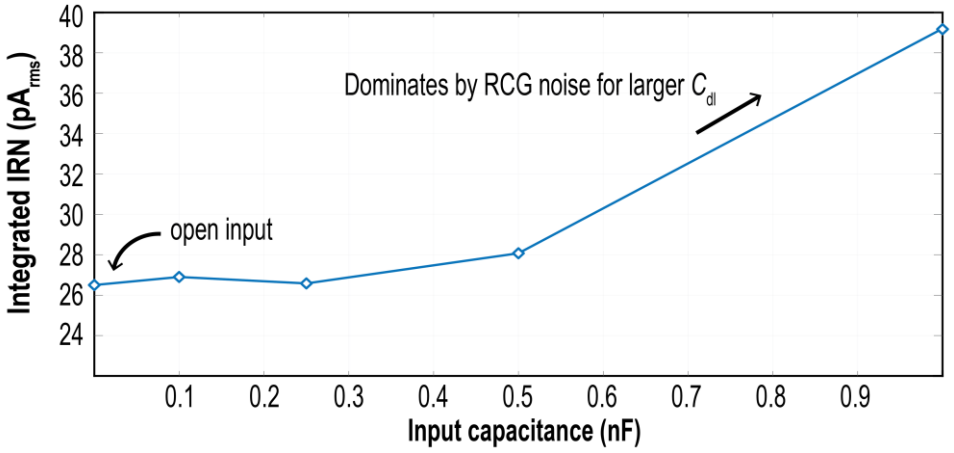


Figure 3.15 Measured input-referred current noise vs. input capacitance.

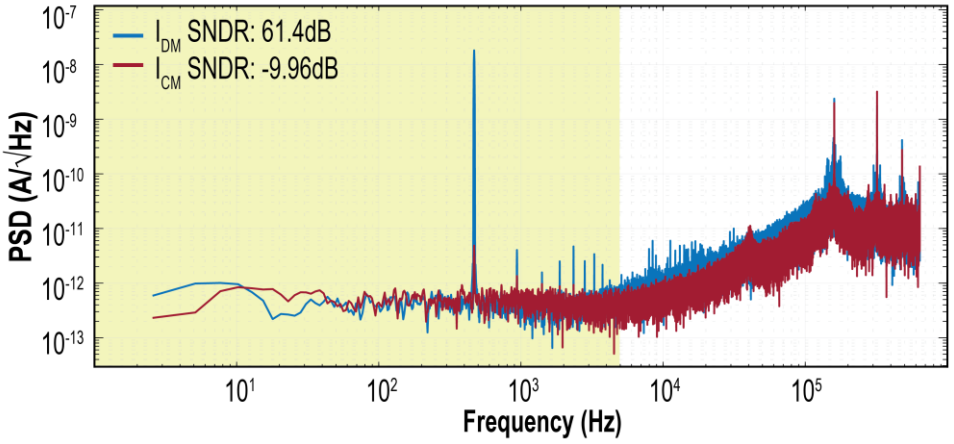


Figure 3.16 Measured spectra with a -2 dBFS differential-mode (DM) and common-mode (CM) input.

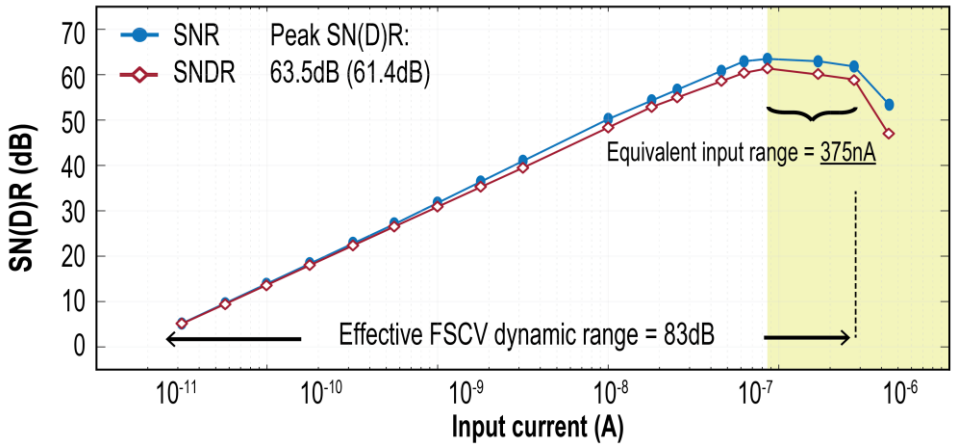
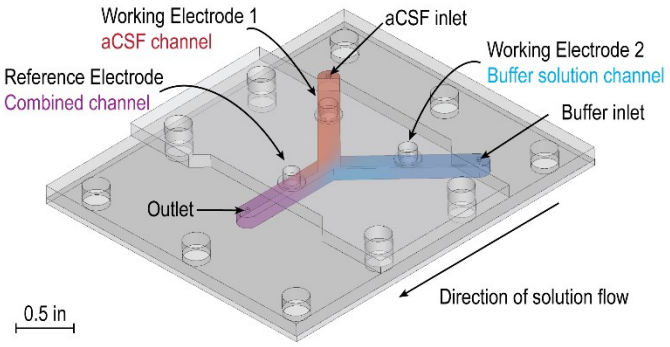


Figure 3.17 Measured dynamic range vs. input current.

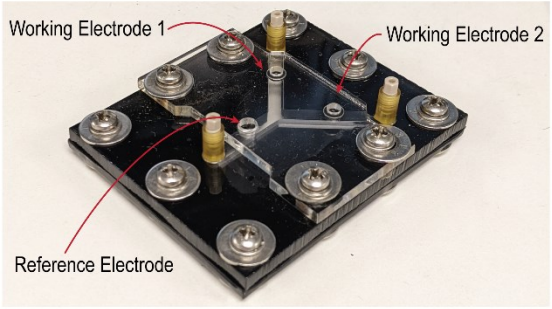
For ac measurements, a sinusoidal input current was generated by connecting a low-distortion function generator (SRS DS360) in series with a large resistor for *V*-to-*I* conversion. The resistor introduces a negligible current noise while significantly attenuating the instrument's voltage noise. The series resistance and the AFE's input capacitance also low-pass filter the instrument noise. With a 100 MΩ input resistance, the IRN is comparable to the floating input configuration. Fig. 3.16 shows measured spectra of the proposed front-end with a –2 dBFS sinusoidal differential-mode (DM) and CM input at 469 Hz. The peak SNDR measured in DM and CM are 61.4 and -9.98 dB, respectively, thus achieving a common-mode rejection ratio (CMRR) of 71.4 dB. The measured spurious-free dynamic range (SFDR) is 71.8 dB. Fig. 3.17 shows the measured SNDR versus the input amplitude where a 300 Hz CM signal was superimposed on the maximum DM signal, and no SNDR degradation was observed up to 290 nA_{pp}, effectively extending the DR from 70 to 83 dB.

3.4.2 *in-vitro* Measurements

Electrochemical measurements were performed with CFMs (BASi, MF-2007) in a custom fabricated Y-channel flow cell, as shown in Fig. 3.18. The flow cell is composed of two milled acrylic plates bolted together. A rubber gasket between the plates creates a seal and prevents leaks. The channels are 4 mm wide to accommodate the CFM and Ag/AgCl electrodes. Rubber o-rings were placed around the electrodes to create a seal. The Y-channel design was specifically chosen to isolate the two working electrodes from each other while still being electrically referenced to the same reference electrode. An Ag/AgCl reference electrode was used in an artificial CSF solution composed of 140 mM NaCl, 5 mM KCl, 2.5 mM $CaCl_2$, 1 mM $MgCl_2$, and 10 mM HEPES (pH 7.4) [170]. A dopamine and buffer mixture was pumped through one inlet, while buffer solution was pumped through the other so that each WE was submerged in either background



(a)



(b)

Figure 3.18 Flow cell (a) rendering and (b) photograph.

solution or analyte. The two solutions were combined at the output to flow past the RE, linking the two WEs to the same reference while keeping each working electrode separate. The solution was pumped in at 2 mL/min using LabSmith valves and a syringe pump. The tubing lengths were matched so that both solutions would reach the flow cell and thus each WE simultaneously. LabSmith valves were used to switch analyte or buffer into the analyte side of the flow cell. Continuously moving the solutions through the flow cell allowed for the exposure of both WEs to their corresponding solutions. Due to the laminar flow, there is little to no mixing once the flows are combined and no backflow.

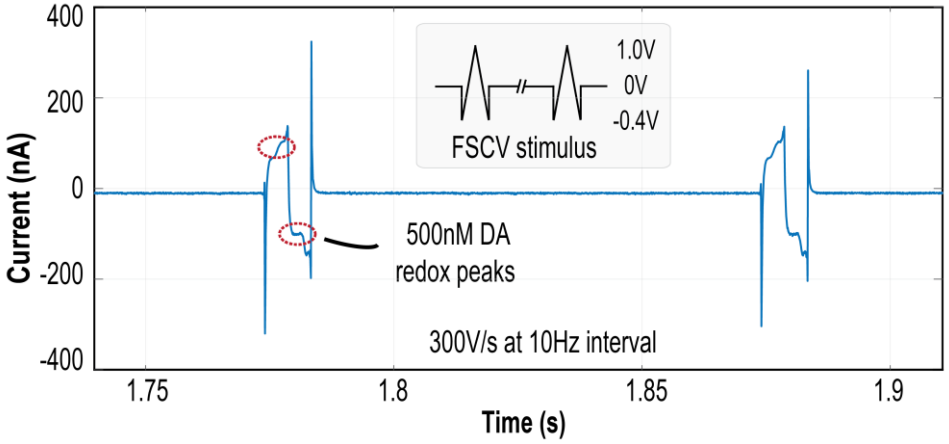


Figure 3.19 *in-vitro* FSCV measurement results with 500 nM dopamine.

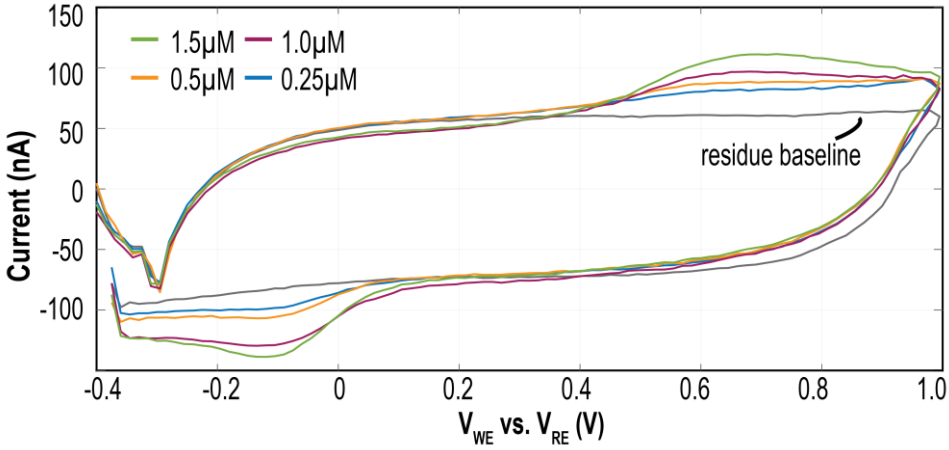


Figure 3.20 Reconstructed FSCV waveforms at various dopamine concentrations without background subtraction.

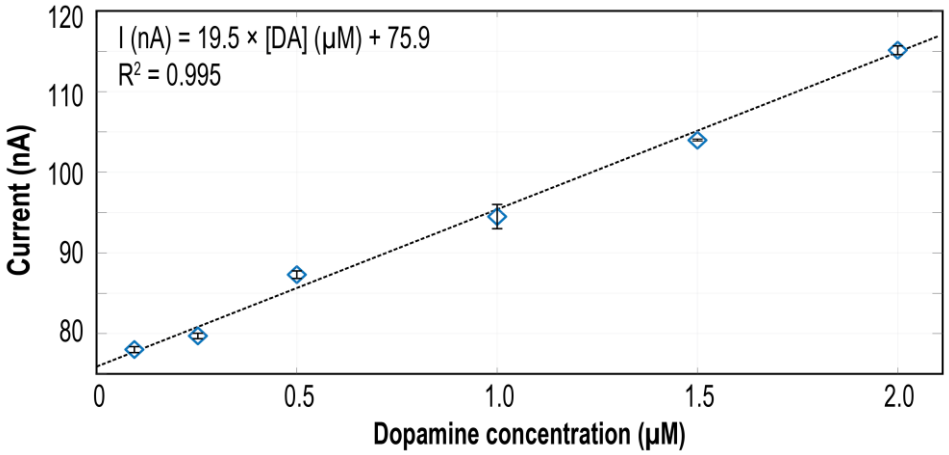


Figure 3.21 Measured dopamine sensitivity curve.

A 300 V/s triangular waveform was generated using a Keysight Trueform 33622A waveform generator. The waveform spanned from –0.4 to 1 V and was pulsed at 10 Hz. Dopamine and buffer solutions were pumped through the flow cell for 30 seconds, over which CV measurements were recorded. Fig. 3.19 shows a real-time recording of 500 nM dopamine without post-processing. Redox peaks were visible even in the raw recording due to the low-noise front-end with CM rejection. Dopamine measurements were taken at 100, 250, 500, 750, and 1000 nM to characterize the response. Post-processing averaged 20 scans and reconstructed the voltammograms, as shown in Fig. 3.20. The peak current versus concentration is shown in the calibration curve in Fig. 3.21, where the error bars were calculated from 20 consecutive scans. The measured sensitivity was 19.5 nA/μM.

Table 3-1 compares this work to the state-of-the-art FSCV front-ends. This work achieves the lowest input-referred current noise (26.5 pA_{rms}) with an open input due to the low input impedance input structure. Even with 1 nF of input capacitance, this work achieves excellent noise performance at 39.2 pA_{rms}. The resolution-to-power tradeoff is captured by the resolution-FoM, which is widely used to characterize the power efficiency of sensor front-ends [4], [14], [145]. This work achieves an FoM of 0.52 $pA^2\mu J$, which is 17.4× better than the state-of-the-art.

Table 3-1 Comparison To Prior FSCV AFEs

	[177] Nasri TBCAS'17	[175] Zamani MWCAS'20	[131] Lu TBCAS'21	[170] Dorta TBCAS'16	[41] Bozorgzadeh TBCAS'16	[169] Bozorgzadeh JSSC'14	**This work**
Process (nm)	65	180	180	65	350	350	180
Topology	Dual slope	1st-ord. ΔΣ	I-to-F + TDC	TIA + SAR	3rd-ord. ΔΣ	3rd-ord. ΔΣ	CC + 1st-ord. IIR-ΔΣ
Scan rate (V/s)	400	400	0.008 - 400	300	400	400	300
Sample freq. (Hz)	5k	1.6M	50k	10k	625k	625k	1.28M
Bandwidth (Hz)	2.5k	5k	25k	2k	4.88k	5k	5k
Background cancellation	Constant offset subtraction	Two-step cyclic	-	Two-step cyclic	On-chip DSP	-	Class AB CMR
Input range (nA)	165	1000	10000	430	900	950	375
CMRR (dB)	-	-	-	-	-	-	71.4
Sensitivity (nA/μM)	10	35.9	-	8.6	23.3	52.2	19.5
Avg. power* (μW)	3.1	14.1	1.77	14.4	9.5	9.3	3.7
Resolution (pA_{rms})	125.2†	710†	25000	92†	68.2†	55†	26.5 (open) 39.2 (1 nF)
FoM** ($pA^2\mu J$)	19.4	1422	425000	60.9	9.05	5.6	0.52

*Average power during 10 Hz scan **FoM=resolution^2×energy/conversion
†Input loading not explicitly stated

Chapter 3, in part, is based on the material from Da Ying, Joshua Rosenberg, Naveen K. Singh, and Drew A. Hall, "A 26.5 pArms Neurotransmitter Front-End with Class-AB Background Subtraction," *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, In Press. The dissertation author was the primary investigator and author of this paper.

Chapter 4. SUMMARY

4.1 Dissertation Summary

This dissertation presented a comprehensive review of current-sensing analog front-ends and described techniques to achieve high-accuracy current readout circuits tailored to particular biosensing applications. In this section, some key results are summarized.

Chapter 1 aims to provide the reader with a background of current-sensing front-ends by reviewing a selection of state-of-the-art current readout circuits. Current sensors can be categorized by their transduction method into capacitive, resistive, diode/FET-based, and MEMS sensors. Each type was individually reviewed, focusing on applications, circuit models, and nonidealities. A more in-depth discussion of current-sensing front-ends, specifically TIAs, CC, and current-mode delta-sigma (I-ΔΣ) modulators, was carried out later in the chapter to focus on analyzing in terms of gain, bandwidth, stability, noise, and general design considerations. Last, general guidelines for designing low-leakage PCBs were also provided.

In Chapter 2, a novel label- and immobilization-free biosensing technique, transient induced molecular electronic spectroscopy, was introduced. And an 8-channel array of low-noise current sensing front-ends with on-chip microelectrode electrochemical sensors was proposed to observe real-time protein-ligand interactions. The analog front-end consists of a 1st-order continuous-time delta-sigma modulator with a novel digital predictor design for high power efficiency.

In Chapter 3, an AFE for fast-scan cyclic voltammetry with analog background subtraction using a pseudo-differential sensing scheme to cancel the large non-faradaic current before seeing the front-end. As a result, the AFE can be compact and low-power compared to conventional

FSCV AFEs with dedicated digital back-ends to digitize and subtract the background from subsequent recordings. The proposed AFE, fabricated in a 0.18-µm CMOS process, consists of a class-AB common-mode rejection circuit, a low-input-impedance current conveyor, and a 1st-order I-ΔΣ modulator with an improved IIR-ΔΣ from the previous work. This readout front-end was tested with carbon-fiber microelectrodes scanned at 300 V/s using flow-injection of dopamine.

4.2 Future Work

The two current-sensing front-ends presented in this dissertation can be expanded in several ways. In µTIMES, the input impedance of the current-mode ΔΣ needs to be studied further. As addressed in Chapter 3, typical ΔΣ could present a large resistive load to the current sensors, which in some applications might result in signal attenuation or alter the underlying physiological current transduction and lead to untruthful data interpretation. In addition, the tri-level DAC logic resulted in an increased level of linearity degradation due to DAC mismatch. This issue was alleviated in the neurotransmitter front-end at an area tradeoff from using the resistive DAC. In both works, a 1st-order ΔΣ, however, the area and power penalty beyond the first stage in a ΔΣ can actually be marginal if properly designed. So even increasing the order of the *I*-ΔΣ by one can substantially improve dynamic range with higher immunity to limit cycle, which could result in in-band tones for quasi-dc biological signals and degrade linearity. However, the PWM DAC current implementation is built upon the insensitive nature of 1st-order CT-ΔΣ to DAC pulse shape. Further study must ensure the stability of PWM DAC in higher-order ΔΣ and could be an interesting research topic.

REFERENCES

[1] F. N. Toth, G. C. M. Meijer, and M. van der Lee, "A planar capacitive precision gauge for liquid-level and leakage detection," *IEEE Trans. Instrum. Meas.*, vol. 46, no. 2, pp. 644–646, Apr. 1997, doi: 10.1109/19.572052.

[2] H. Canbolat, "A Novel Level Measurement Technique Using Three Capacitive Sensors for Liquids," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 10, pp. 3762–3768, Oct. 2009, doi: 10.1109/TIM.2009.2019715.

[3] D. Barrettino, M. Graf, S. Hafizovic, S. Taschini, C. Hagleitner, A. Hierlemann, and H. Baltes, "A single-chip CMOS micro-hotplate array for hazardous-gas detection and material characterization," in *2004 IEEE International Solid-State Circuits Conference (IEEE Cat. No.04CH37519)*, Feb. 2004, pp. 312-313 Vol.1. doi: 10.1109/ISSCC.2004.1332719.

[4] H. Jiang, C. Huang, M. R. Chan, and D. A. Hall, "A 2-in-1 Temperature and Humidity Sensor with a Single FLL Wheatstone-Bridge Front-End," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2174–2185, Aug. 2020, doi: 10.1109/JSSC.2020.2989585.

[5] J. Park, D. Lim, and D. Jeong, "A Reconfigurable 40-to-67 dB SNR, 50-to-6400 Hz Frame-Rate, Column-Parallel Readout IC for Capacitive Touch-Screen Panels," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2305–2318, Oct. 2014, doi: 10.1109/JSSC.2014.2336800.

[6] M. Miyamoto, M. Hamaguchi, and A. Nagao, "A 143×81 Mutual-Capacitance Touch-Sensing Analog Front-End With Parallel Drive and Differential Sensing Architecture," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 335–343, Jan. 2015, doi: 10.1109/JSSC.2014.2364092.

[7] N. Kirchner, D. Hordern, D. Liu, and G. Dissanayake, "Capacitive sensor for object ranging and material type identification," *Sens. Actuators Phys.*, vol. 148, no. 1, pp. 96–104, Nov. 2008, doi: 10.1016/j.sna.2008.07.027.

[8] E. Ghafar-Zadeh, M. Sawan, V. P. Chodavarapu, and T. Hosseini-Nia, "Bacteria Growth Monitoring Through a Differential CMOS Capacitive Sensor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 4, pp. 232–238, Aug. 2010, doi: 10.1109/TBCAS.2010.2048430.

[9] M. S.-C. Lu, Y.-C. Chen, and P.-C. Huang, "5×5 CMOS capacitive sensor array for detection of the neurotransmitter dopamine," *Biosens. Bioelectron.*, vol. 26, no. 3, pp. 1093–1097, Nov. 2010, doi: 10.1016/j.bios.2010.08.065.

[10] G. Nabovati, E. Ghafar-Zadeh, A. Letourneau, and M. Sawan, "Smart Cell Culture Monitoring and Drug Test Platform Using CMOS Capacitive Sensor Array," *IEEE Trans. Biomed. Eng.*, vol. 66, no. 4, pp. 1094–1104, Apr. 2019, doi: 10.1109/TBME.2018.2866830.

[11] S. B. Prakash and P. Abshire, "Tracking cancer cell proliferation on a CMOS capacitance sensor chip," *Biosens. Bioelectron.*, vol. 23, no. 10, pp. 1449–1457, May 2008, doi: 10.1016/j.bios.2007.12.015.

[12] S. Pan and K. A. A. Makinwa, "A 0.25 mm2-Resistor-Based Temperature Sensor With an Inaccuracy of 0.12 °C (3σ) From −55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3347–3355, Dec. 2018, doi: 10.1109/JSSC.2018.2869595.

[13] P. Park, D. Ruffieux, and K. A. A. Makinwa, "A Thermistor-Based Temperature Sensor for a Real-Time Clock With 2 ppm Frequency Stability," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1571–1580, Jul. 2015, doi: 10.1109/JSSC.2015.2417806.

[14] S. Pan, Y. Luo, S. H. Shalmany, and K. A. A. Makinwa, "A Resistor-Based Temperature Sensor With a 0.13 pJ·K2 Resolution FoM," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 164–173, Jan. 2018, doi: 10.1109/JSSC.2017.2746671.

[15] L. Pan, A. Chortos, G. Yu, Y. Wang, S. Isaacson, R. Allen, Y. Shi, R. Dauskardt, and Z. Bao, "An ultra-sensitive resistive pressure sensor based on hollow-sphere microstructure induced elasticity in conducting polymer film," *Nat. Commun.*, vol. 5, no. 1, Art. no. 1, Jan. 2014, doi: 10.1038/ncomms4002.

[16] H. Tian, Y. Shu, X.-F. Wang, M. A. Mohammad, Z. Bie, Q.-Y. Xie, C. Li, W.-T. Mi, Y. Yang, and T.-L. Ren, "A Graphene-Based Resistive Pressure Sensor with Record-High Sensitivity in a Wide Pressure Range," *Sci. Rep.*, vol. 5, no. 1, Art. no. 1, Feb. 2015, doi: 10.1038/srep08603.

[17] M. Tonezzer, D. T. T. Le, S. Iannotta, and N. Van Hieu, "Selective discrimination of hazardous gases using one single metal oxide resistive sensor," *Sens. Actuators B Chem.*, vol. 277, pp. 121–128, Dec. 2018, doi: 10.1016/j.snb.2018.08.103.

[18] S. Pandey, G. K. Goswami, and K. K. Nanda, "Nanocomposite based flexible ultrasensitive resistive gas sensor for chemical reactions studies," *Sci. Rep.*, vol. 3, no. 1, Art. no. 1, Jun. 2013, doi: 10.1038/srep02082.

[19] J.-R. Lee, D. M. Magee, R. S. Gaster, J. LaBaer, and S. X. Wang, "Emerging protein array technologies for proteomics," *Expert Rev. Proteomics*, vol. 10, no. 1, pp. 65–75, Feb. 2013, doi: 10.1586/epr.12.67.

[20] A. C. Fernandes, C. M. Duarte, F. A. Cardoso, R. Bexiga, S. Cardoso, and P. P. Freitas, "Lab-on-Chip Cytometry Based on Magnetoresistive Sensors for Bacteria Detection in Milk," *Sensors*, vol. 14, no. 8, Art. no. 8, Aug. 2014, doi: 10.3390/s140815496.

[21] R. S. Gaster, D. A. Hall, and S. X. Wang, "nanoLAB: an ultraportable, handheld diagnostic laboratory for global health," *Lab. Chip*, vol. 11, no. 5, pp. 950–956, Mar. 2011, doi: 10.1039/c0lc00534g.

[22] X. Zhou, M. Sveiven, and D. A. Hall, "A CMOS Magnetoresistive Sensor Front-End With Mismatch-Tolerance and Sub-ppm Sensitivity for Magnetic Immunoassays," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1254–1263, Dec. 2019, doi: 10.1109/TBCAS.2019.2949725.

[23] J. Pan, S. Liu, Y. Yang, and J. Lu, "A Highly Sensitive Resistive Pressure Sensor Based on a Carbon Nanotube-Liquid Crystal-PDMS Composite," *Nanomaterials*, vol. 8, no. 6, Art. no. 6, Jun. 2018, doi: 10.3390/nano8060413.

[24] L. Bandiera, G. Cellere, S. Cagnin, A. De Toni, E. Zanoni, G. Lanfranchi, and L. Lorenzelli, "A fully electronic sensor for the measurement of cDNA hybridization kinetics," *Biosens. Bioelectron.*, vol. 22, no. 9–10, pp. 2108–2114, Apr. 2007, doi: 10.1016/j.bios.2006.09.025.

[25] Z. E. Selvanayagam, P. Neuzil, P. Gopalakrishnakone, U. Sridhar, M. Singh, and L. C. Ho, "An ISFET-based immunosensor for the detection of β-Bungarotoxin," *Biosens. Bioelectron.*, vol. 17, no. 9, pp. 821–826, Sep. 2002, doi: 10.1016/S0956-5663(02)00075-1.

[26] P. A. Hammond, D. Ali, and D. R. S. Cumming, "A system-on-chip digital pH meter for use in a wireless diagnostic capsule," *IEEE Trans. Biomed. Eng.*, vol. 52, no. 4, pp. 687–694, Apr. 2005, doi: 10.1109/TBME.2005.844041.

[27] P. Damborský, J. Švitel, and J. Katrlík, "Optical biosensors," *Essays Biochem.*, vol. 60, no. 1, pp. 91–100, Jun. 2016, doi: 10.1042/EBC20150010.

[28] K. Pimková, M. Bocková, K. Hegnerová, J. Suttnar, J. Cermák, J. Homola, and J. E. Dyr, "Surface plasmon resonance biosensor for the detection of VEGFR-1--a protein marker of myelodysplastic syndromes," *Anal. Bioanal. Chem.*, vol. 402, no. 1, pp. 381–387, Jan. 2012, doi: 10.1007/s00216-011-5395-3.

[29] E. Engvall and P. Perlmann, "Enzyme-linked immunosorbent assay (ELISA). Quantitative assay of immunoglobulin G," *Immunochemistry*, vol. 8, no. 9, pp. 871–874, Sep. 1971, doi: 10.1016/0019-2791(71)90454-x.

[30] S. J. Dwight, B. S. Gaylord, J. W. Hong, and G. C. Bazan, "Perturbation of Fluorescence by Nonspecific Interactions between Anionic Poly(phenylenevinylene)s and Proteins: Implications for Biosensors," *J. Am. Chem. Soc.*, vol. 126, no. 51, pp. 16850–16859, Dec. 2004, doi: 10.1021/ja0469737.

[31] Q.-Y. Zhang, H. Chen, Z. Lin, and J.-M. Lin, "Comparison of chemiluminescence enzyme immunoassay based on magnetic microparticles with traditional colorimetric ELISA for the detection of serum α-fetoprotein," *J. Pharm. Anal.*, vol. 2, no. 2, pp. 130–135, Apr. 2012, doi: 10.1016/j.jpha.2011.10.001.

[32] Jiangfeng Wu, G. K. Fedder, and L. R. Carley, "A low-noise low-offset capacitive sensing amplifier for a 50-μg/√Hz monolithic CMOS MEMS accelerometer," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 722–730, May 2004, doi: 10.1109/JSSC.2004.826329.
[33] B. V. Amini, R. Abdolvand, and F. Ayazi, "A 4.5-mW Closed-Loop Delta-Sigma Micro-Gravity CMOS SOI Accelerometer," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2983–2991, Dec. 2006, doi: 10.1109/JSSC.2006.884864.
[34] F. Chen, X. Li, and M. Kraft, "Electromechanical Sigma–Delta Modulators (ΣΔM) Force Feedback Interfaces for Capacitive MEMS Inertial Sensors: A Review," *IEEE Sens. J.*, vol. 16, no. 17, pp. 6476–6495, Sep. 2016, doi: 10.1109/JSEN.2016.2582198.
[35] A. Sabato, C. Niezrecki, and G. Fortino, "Wireless MEMS-Based Accelerometer Sensor Boards for Structural Vibration Monitoring: A Review," *IEEE Sens. J.*, vol. 17, no. 2, pp. 226–235, Jan. 2017, doi: 10.1109/JSEN.2016.2630008.
[36] Y. Deimerly, P. Rey, P. Robert, T. Bourouina, and G. Jourdan, "Electromechanical damping in MEMS accelerometers: A way towards single chip gyrometer accelerometer co-integration," in *2014 IEEE 27th International Conference on Micro Electro Mechanical Systems (MEMS)*, Jan. 2014, pp. 725–728. doi: 10.1109/MEMSYS.2014.6765743.
[37] C. He, Q. Zhao, Q. Huang, D. Liu, Z. Yang, D. Zhang, and G. Yan, "A MEMS Vibratory Gyroscope With Real-Time Mode-Matching and Robust Control for the Sense Mode," *IEEE Sens. J.*, vol. 15, no. 4, pp. 2069–2077, Apr. 2015, doi: 10.1109/JSEN.2014.2371456.
[38] J. Raman, E. Cretu, P. Rombouts, and L. Weyten, "A Closed-Loop Digitally Controlled MEMS Gyroscope With Unconstrained Sigma-Delta Force-Feedback," *IEEE Sens. J.*, vol. 9, no. 3, pp. 297–305, Mar. 2009, doi: 10.1109/JSEN.2008.2012237.
[39] L. Hong, H. Li, H. Yang, and K. Sengupta, "Fully Integrated Fluorescence Biosensors On-Chip Employing Multi-Functional Nanoplasmonic Optical Structures in CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2388–2406, Sep. 2017, doi: 10.1109/JSSC.2017.2712612.
[40] H. Wang and L. Pilon, "Accurate Simulations of Electric Double Layer Capacitance of Ultramicroelectrodes," *J. Phys. Chem. C*, vol. 115, no. 33, pp. 16711–16719, Aug. 2011, doi: 10.1021/jp204498e.
[41] B. Bozorgzadeh, D. R. Schuweiler, M. J. Bobak, P. A. Garris, and P. Mohseni, "Neurochemostat: A Neural Interface SoC With Integrated Chemometrics for Closed-Loop Regulation of Brain Dopamine," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 3, pp. 654–667, Jun. 2016, doi: 10.1109/TBCAS.2015.2453791.
[42] N. Gilda and V. R. Rao, "Comparison of capacitive versus resistive mode of sensing for vapor phase explosive detection," Jun. 2015, pp. 778–781. doi: 10.1109/EDSSC.2015.7285233.
[43] J. Lenz and S. Edelstein, "Magnetic sensors and their applications," *IEEE Sens. J.*, vol. 6, no. 3, pp. 631–649, Jun. 2006, doi: 10.1109/JSEN.2006.874493.
[44] R. S. Gaster, D. A. Hall, C. H. Nielsen, S. J. Osterfeld, H. Yu, K. E. Mach, R. J. Wilson, B. Murmann, J. C. Liao, S. S. Gambhir, and S. X. Wang, "Matrix-insensitive protein assays push the limits of biosensors in medicine," *Nat. Med.*, vol. 15, no. 11, Art. no. 11, Nov. 2009, doi: 10.1038/nm.2032.
[45] D. A. Hall, R. S. Gaster, K. Makinwa, S. X. Wang, and B. Murmann, "A 256 pixel magnetoresistive biosensor microarray in 0.18μm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1290–1301, May 2013, doi: 10.1109/JSSC.2013.2245058.
[46] C. Huang, X. Zhou, D. Ying, and D. A. Hall, "A GMR-based magnetic flow cytometer using matched filtering," in *2017 IEEE SENSORS*, Oct. 2017, pp. 1–3. doi: 10.1109/ICSENS.2017.8233892.
[47] H. Kaushal and G. Kaddoum, "Optical Communication in Space: Challenges and Mitigation Techniques," *IEEE Commun. Surv. Tutor.*, vol. 19, no. 1, pp. 57–96, Firstquarter 2017, doi: 10.1109/COMST.2016.2603518.
[48] R. X. G. Ferreira, E. Xie, J. J. D. McKendry, S. Rajbhandari, H. Chun, G. Faulkner, S. Watson, A. E. Kelly, E. Gu, R. V. Penty, I. H. White, D. C. O'Brien, and M. D. Dawson, "High Bandwidth

GaN-Based Micro-LEDs for Multi-Gb/s Visible Light Communications," *IEEE Photonics Technol. Lett.*, vol. 28, no. 19, pp. 2023–2026, Oct. 2016, doi: 10.1109/LPT.2016.2581318.

[49] Z. Zeng, S. Fu, H. Zhang, Y. Dong, and J. Cheng, "A Survey of Underwater Optical Wireless Communications," *IEEE Commun. Surv. Tutor.*, vol. 19, no. 1, pp. 204–238, Firstquarter 2017, doi: 10.1109/COMST.2016.2618841.

[50] T. Fersch, R. Weigel, and A. Koelpin, "A CDMA Modulation Technique for Automotive Time-of-Flight LiDAR Systems," *IEEE Sens. J.*, vol. 17, no. 11, pp. 3507–3516, Jun. 2017, doi: 10.1109/JSEN.2017.2688126.

[51] S. Oh and H. Kang, "Fast Occupancy Grid Filtering Using Grid Cell Clusters From LIDAR and Stereo Vision Sensor Data," *IEEE Sens. J.*, vol. 16, no. 19, pp. 7258–7266, Oct. 2016, doi: 10.1109/JSEN.2016.2598600.

[52] A. Harrison, R. Özgün, J. Lin, A. Andreou, and R. Etienne-Cummings, "A spike based 3D imager chip using a mixed mode encoding readout," in *2010 Biomedical Circuits and Systems Conference (BioCAS)*, Nov. 2010, pp. 190–193. doi: 10.1109/BIOCAS.2010.5709603.

[53] K. Murari, R. Etienne-Cummings, N. Thakor, and G. Cauwenberghs, "Which Photodiode to Use: A Comparison of CMOS-Compatible Structures," *IEEE Sens. J.*, vol. 9, no. 7, pp. 752–760, Jul. 2009, doi: 10.1109/JSEN.2009.2021805.

[54] B. Razavi, *Design of Integrated Circuits for Optical Communications*, 1st edition. Boston: McGraw-Hill Science/Engineering/Math, 2002.

[55] D. Li, M. Liu, S. Gao, Y. Shi, Y. Zhang, Z. Li, P. Y. Chiang, F. Maloberti, and L. Geng, "Low-Noise Broadband CMOS TIA Based on Multi-Stage Stagger-Tuned Amplifier for High-Speed High-Sensitivity Optical Communication," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 66, no. 10, pp. 3676–3689, Oct. 2019, doi: 10.1109/TCSI.2019.2916150.

[56] M. G. Ahmed, M. Talegaonkar, A. Elkholy, G. Shu, A. Elmallah, A. Rylyakov, and P. K. Hanumolu, "A 12-Gb/s -16.8-dBm OMA Sensitivity 23-mW Optical Receiver in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 445–457, Feb. 2018, doi: 10.1109/JSSC.2017.2757008.

[57] M. Atef and H. Zimmermann, "Optical Receiver Using Noise Cancelling With an Integrated Photodiode in 40 nm CMOS Technology," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 60, no. 7, pp. 1929–1936, Jul. 2013, doi: 10.1109/TCSI.2012.2230495.

[58] S. G. Kim, C. Hong, Y. S. Eo, J. Kim, and S. M. Park, "A 40-GHz Mirrored-Cascode Differential Transimpedance Amplifier in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1468–1474, May 2019, doi: 10.1109/JSSC.2018.2886323.

[59] M. G. Ahmed, T. N. Huynh, C. Williams, Y. Wang, P. K. Hanumolu, and A. Rylyakov, "34-GBd Linear Transimpedance Amplifier for 200-Gb/s DP-16-QAM Optical Coherent Receivers," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 834–844, Mar. 2019, doi: 10.1109/JSSC.2018.2882265.

[60] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro, "Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1609–1616, May 2009, doi: 10.1109/JSSC.2009.2016998.

[61] J. K. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard, "Integrated nanopore sensing platform with sub-microsecond temporal resolution," *Nat. Methods*, vol. 9, no. 5, Art. no. 5, May 2012, doi: 10.1038/nmeth.1932.

[62] E. Kang, M. Tan, J.-S. An, Z.-Y. Chang, P. Vince, N. Sénégond, T. Mateo, C. Meynier, and M. A. P. Pertijs, "A Variable-Gain Low-Noise Transimpedance Amplifier for Miniature Ultrasound Probes," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3157–3168, Dec. 2020, doi: 10.1109/JSSC.2020.3023618.

[63] G. Mulberry, K. A. White, and B. N. Kim, "Analysis of Simple Half-Shared Transimpedance Amplifier for Picoampere Biosensor Measurements," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 2, pp. 387–395, Apr. 2019, doi: 10.1109/TBCAS.2019.2897287.

[64] E. Säckinger, "The Transimpedance Limit," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 57, no. 8, pp. 1848–1856, Aug. 2010, doi: 10.1109/TCSI.2009.2037847.

[65] S. S. Mohan, M. D. M. Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, Mar. 2000, doi: 10.1109/4.826816.

[66] D. Djekic, G. Fantner, K. Lips, M. Ortmanns, and J. Anders, "A 0.1% THD, 1-M to 1-G Tunable, Temperature-Compensated Transimpedance Amplifier Using a Multi-Element Pseudo-Resistor," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1913–1923, Jul. 2018, doi: 10.1109/JSSC.2018.2820701.

[67] R. Yang, S.-W. Zhen, Y.-R. Zhang, Y.-Q. Zhao, X. Yang, and B. Zhang, "A wideband transimpedance amplifier with tee network topology," in *2020 IEEE 15th International Conference on Solid-State Integrated Circuit Technology (ICSICT)*, Nov. 2020, pp. 1–3. doi: 10.1109/ICSICT49897.2020.9278244.

[68] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003, doi: 10.1109/JSSC.2003.811979.

[69] S.-Y. Peng, M. S. Qureshi, P. E. Hasler, A. Basu, and F. L. Degertekin, "A Charge-Based Low-Power High-SNR Capacitive Sensing Interface Circuit," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 55, no. 7, pp. 1863–1872, Aug. 2008, doi: 10.1109/TCSI.2008.918006.

[70] M. Crescentini, M. Bennati, M. Carminati, and M. Tartagni, "Noise limits of CMOS current interfaces for biosensors: a review," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 2, pp. 278–292, Apr. 2014, doi: 10.1109/TBCAS.2013.2262998.

[71] F. Aflatouni and H. Hashemi, "A 1.8mW Wideband 57dBΩ transimpedance amplifier in 0.13µm CMOS," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2009, pp. 57–60. doi: 10.1109/RFIC.2009.5135489.

[72] S. Ray and M. M. Hella, "A 53 dB $Ømega 7$ -GHz Inductorless Transimpedance Amplifier and a 1-THz+ GBP Limiting Amplifier in 0.13- µ m CMOS," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 65, no. 8, pp. 2365–2377, Aug. 2018, doi: 10.1109/TCSI.2017.2788799.

[73] M. H. Taghavi, L. Belostotski, J. W. Haslett, and P. Ahmadi, "10-Gb/s 0.13-µm CMOS Inductorless Modified-RGC Transimpedance Amplifier," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 62, no. 8, pp. 1971–1980, Aug. 2015, doi: 10.1109/TCSI.2015.2440732.

[74] G. W. Roberts and A. S. Sedra, "All current-mode frequency selective circuits," *Electron. Lett.*, vol. 25, no. 12, pp. 759–761, Jun. 1989, doi: 10.1049/el:19890513.

[75] G. W. Roberts and A. S. Sedra, "Adjoint networks revisited," in *IEEE International Symposium on Circuits and Systems*, May 1990, pp. 540–544 vol.1. doi: 10.1109/ISCAS.1990.112110.

[76] H. Li, C. S. Boling, and A. J. Mason, "CMOS Amperometric ADC With High Sensitivity, Dynamic Range and Power Efficiency for Air Quality Monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 4, pp. 817–827, Aug. 2016, doi: 10.1109/TBCAS.2016.2571306.

[77] H. Li, S. Parsnejad, E. Ashoori, C. Thompson, E. K. Purcell, and A. J. Mason, "Ultracompact Microwatt CMOS Current Readout With Picoampere Noise and Kilohertz Bandwidth for Biosensor Arrays," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 1, pp. 35–46, Feb. 2018, doi: 10.1109/TBCAS.2017.2752742.

[78] M. H. Nazari, H. Mazhab-Jafari, L. Leng, A. Guenther, and R. Genov, "CMOS Neurotransmitter Microarray: 96-Channel Integrated Potentiostat With On-Die Microsensors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 338–348, Jun. 2013, doi: 10.1109/TBCAS.2012.2203597.

[79] M. Haberler, I. Siegl, C. Steffan, and M. Auer, "A Bidirectional Current-Mirror-Based Potentiostat Using a Slice-Based Class-AB Amplifier," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 298–301, 2020, doi: 10.1109/LSSC.2020.3013667.

[80] J. Guo, W. Ng, J. Yuan, and M. Chan, "A 51fA/Hz0.5 low power heterodyne impedance analyzer for electrochemical impedance spectroscopy," in *2013 Symposium on VLSI Circuits*, Jun. 2013, pp. C56–C57.

[81] S. Kawahito and Y. Tadokoro, “CMOS class-AB current mirrors for precision current-mode analog-signal-processing elements,” *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 43, no. 12, pp. 843–845, Dec. 1996, doi: 10.1109/82.553403.
[82] B. Gilbert, “Translinear circuits: a proposed classification,” *Electron. Lett.*, vol. 11, no. 1, pp. 14–16, Jan. 1975, doi: 10.1049/el:19750011.
[83] A. Fabre, O. Saaid, F. Wiest, and C. Boucheron, “High frequency applications based on a new current controlled conveyor,” *IEEE Trans. Circuits Syst. Fundam. Theory Appl.*, vol. 43, no. 2, pp. 82–91, Feb. 1996, doi: 10.1109/81.486430.
[84] E. Seevinck and R. J. Wiegerink, “Generalized translinear circuit principle,” *IEEE J. Solid-State Circuits*, vol. 26, no. 8, pp. 1098–1102, Aug. 1991, doi: 10.1109/4.90062.
[85] E. Bruun, “Class AB CMOS first-generation current conveyor,” *Electron. Lett.*, vol. 31, no. 6, pp. 422–423, Mar. 1995, doi: 10.1049/el:19950337.
[86] Z. Wang, “Wideband class AB (push-pull) current amplifier in CMOS technology,” *Electron. Lett.*, vol. 26, pp. 543–545, Apr. 1990, doi: 10.1049/el:19900353.
[87] F. Esparza-Alfaro, S. Pennisi, G. Palumbo, and A. J. Lopez-Martin, “Low-Power Class-AB CMOS Voltage Feedback Current Operational Amplifier With Tunable Gain and Bandwidth,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 61, no. 8, pp. 574–578, Aug. 2014, doi: 10.1109/TCSII.2014.2327390.
[88] A. Lopez-Martin, J. Ramirez-Angulo, R. G. Carvajal, and J. M. Algueta, “Compact class AB CMOS current mirror,” *Electron. Lett.*, vol. 44, pp. 1335–1336, Dec. 2008, doi: 10.1049/el:20082419.
[89] T. Kurashina, S. Ogawa, and K. Watanabe, “A high performance class AB current conveyor,” in *1998 IEEE International Conference on Electronics, Circuits and Systems. Surfing the Waves of Science and Technology (Cat. No.98EX196)*, Sep. 1998, vol. 3, pp. 143–146 vol.3. doi: 10.1109/ICECS.1998.813954.
[90] H. M. Jafari and R. Genov, “Chopper-Stabilized Bidirectional Current Acquisition Circuits for Electrochemical Amperometric Biosensors,” *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 60, no. 5, pp. 1149–1157, May 2013, doi: 10.1109/TCSI.2013.2248771.
[91] K. Bult and G. J. G. M. Geelen, “A fast-settling CMOS op amp for SC circuits with 90-dB DC gain,” *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1384, Dec. 1990, doi: 10.1109/4.62165.
[92] G. Wegmann and E. A. Vittoz, “Analysis and improvements of accurate dynamic current mirrors,” *IEEE J. Solid-State Circuits*, vol. 25, no. 3, pp. 699–706, Jun. 1990, doi: 10.1109/4.102663.
[93] R. Schreier, S. Pavan, and G. C. Temes, *Understanding Delta-Sigma Data Converters*, 2nd ed. Wiley-IEEE Press, 2017.
[94] A. Gore, S. Chakrabartty, S. Pal, and E. C. Alocilja, “A Multichannel Femtoampere-Sensitivity Potentiostat Array for Biosensing Applications,” *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 53, no. 11, pp. 2357–2363, Nov. 2006, doi: 10.1109/TCSI.2006.884432.
[95] H. Son, H. Cho, J. Koo, Y. Ji, B. Kim, H. Park, and J. Sim, “A Low-Power Wide Dynamic-Range Current Readout Circuit for Ion-Sensitive FET Sensors,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 3, pp. 523–533, Jun. 2017, doi: 10.1109/TBCAS.2016.2643784.
[96] M. Stanacevic, K. Murari, A. Rege, G. Cauwenberghs, and N. V. Thakor, “VLSI Potentiostat Array With Oversampling Gain Modulation for Wide-Range Neurotransmitter Sensing,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 1, pp. 63–72, Mar. 2007, doi: 10.1109/TBCAS.2007.893176.
[97] D. Ying, P.-W. Chen, C. Tseng, Y.-H. Lo, and D. A. Hall, “A Sub-pA Current Sensing Front-End for Transient Induced Molecular Spectroscopy,” in *2019 Symposium on VLSI Circuits*, Jun. 2019, pp. C316–C317. doi: 10.23919/VLSIC.2019.8777980.
[98] C. Hsu and D. A. Hall, “A current-measurement front-end with 160dB dynamic range and 7ppm INL,” in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, Feb. 2018, pp. 326–328. doi: 10.1109/ISSCC.2018.8310316.
[99] S.-H. Wu, Y.-S. Shu, A. Y.-C. Chiou, W.-H. Huang, Z.-X. Chen, and H.-Y. Hsieh, “A Current-Sensing Front-End Realized by A Continuous-Time Incremental ADC with 12b SAR Quantizer and Reset-Then-Open Resistive DAC Achieving 140dB DR and 8ppm INL at 4kS/s,” in *2020 IEEE*

International Solid- State Circuits Conference - (ISSCC), Feb. 2020, pp. 154–156. doi: 10.1109/ISSCC19947.2020.9062990.
[100] F. Gerfers and M. Ortmanns, *Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations*. Berlin Heidelberg: Springer-Verlag, 2006. doi: 10.1007/3-540-28473-7.
[101] R. Schreier, "Delta Sigma Toolbox." https://www.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox
[102] B. Linares-Barranco and T. Serrano-Gotarredona, "On the design and characterization of femtoampere current-mode circuits," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1353–1363, Aug. 2003, doi: 10.1109/JSSC.2003.814415.
[103] S. Dai, R. T. Perera, Z. Yang, and J. K. Rosenstein, "A 155-dB Dynamic Range Current Measurement Front End for Electrochemical Biosensing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 5, pp. 935–944, Oct. 2016, doi: 10.1109/TBCAS.2016.2612581.
[104] Y. Liao, H. Yao, A. Lingley, B. Parviz, and B. P. Otis, "A 3-μW CMOS Glucose Sensor for Wireless Contact-Lens Tear Glucose Monitoring," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 335–344, Jan. 2012, doi: 10.1109/JSSC.2011.2170633.
[105] H. Jiang, X. Zhou, S. Kulkarni, M. Uranian, R. Seenivasan, and D. A. Hall, "A Sub-1 μW multiparameter injectable BioMote for continuous alcohol monitoring," in *2018 IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2018, pp. 1–4. doi: 10.1109/CICC.2018.8357045.
[106] M. M. Ahmadi and G. A. Jullien, "A Wireless-Implantable Microsystem for Continuous Blood Glucose Monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 3, pp. 169–180, Jun. 2009, doi: 10.1109/TBCAS.2009.2016844.
[107] C. Pochet, H. Jiang, and H. Drew, "Ultra-Low Leakage ESD Protection Achieving 10.5 fA Leakage."
[108] Y. M. Chi, C. Maier, and G. Cauwenberghs, "Ultra-High Input Impedance, Low Noise Integrated Amplifier for Noncontact Biopotential Sensing," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 1, no. 4, pp. 526–535, Dec. 2011, doi: 10.1109/JETCAS.2011.2179419.
[109] ACDi, "Printed Circuit Board Cleaning: An Important Step in the Electronic Manufacturing Assembly Process," *ACDI*, Feb. 07, 2020. https://www.acdi.com/printed-circuit-board-cleaning-an-important-step-in-the-electronic-manufacturing-assembly-process/
[110] J. Drews, "Drug discovery: a historical perspective," *Science*, vol. 287, no. 5460, pp. 1960–1964, Mar. 2000.
[111] G. MacBeath and S. L. Schreiber, "Printing Proteins as Microarrays for High-Throughput Function Determination," *Science*, vol. 289, no. 5485, pp. 1760–1763, Sep. 2000, doi: 10.1126/science.289.5485.1760.
[112] A. J. Hughes and A. E. Herr, "Microfluidic Western blotting," *Proc. Natl. Acad. Sci.*, vol. 109, no. 52, pp. 21450–21455, Dec. 2012.
[113] J. A. DiMasi, H. G. Grabowski, and R. W. Hansen, "Innovation in the pharmaceutical industry: New estimates of R&D costs," *J. Health Econ.*, vol. 47, pp. 20–33, May 2016, doi: 10.1016/j.jhealeco.2016.01.012.
[114] L. M. Hellman and M. G. Fried, "Electrophoretic mobility shift assay (EMSA) for detecting protein-nucleic acid interactions," *Nat. Protoc.*, vol. 2, no. 8, pp. 1849–1861, 2007, doi: 10.1038/nprot.2007.249.
[115] J. D. Durrant and J. A. McCammon, "Molecular dynamics simulations and drug discovery," *BMC Biol.*, vol. 9, no. 1, p. 71, Oct. 2011, doi: 10.1186/1741-7007-9-71.
[116] P. Neužil, S. Giselbrecht, K. Länge, T. J. Huang, and A. Manz, "Revisiting lab-on-a-chip technology for drug discovery," *Nat. Rev. Drug Discov.*, vol. 11, no. 8, pp. 620–632, Aug. 2012, doi: 10.1038/nrd3799.
[117] X. Shan, X. Huang, K. J. Foley, P. Zhang, K. Chen, S. Wang, and N. Tao, "Measuring Surface Charge Density and Particle Height Using Surface Plasmon Resonance Technique," *Anal. Chem.*, vol. 82, no. 1, pp. 234–240, Jan. 2010, doi: 10.1021/ac901816z.

[118] X. Shan, S. Wang, and N. Tao, “Study of single particle charge and Brownian motions with surface plasmon resonance,” *Appl. Phys. Lett.*, vol. 97, no. 22, p. 223703, Nov. 2010, doi: 10.1063/1.3519364.
[119] K. M. Mayer and J. H. Hafner, “Localized Surface Plasmon Resonance Sensors,” *Chem. Rev.*, vol. 111, no. 6, pp. 3828–3857, Jun. 2011, doi: 10.1021/cr100313v.
[120] C. Fan, K. W. Plaxco, and A. J. Heeger, “Biosensors based on binding-modulated donor-acceptor distances,” *Trends Biotechnol.*, vol. 23, no. 4, pp. 186–192, Apr. 2005, doi: 10.1016/j.tibtech.2005.02.005.
[121] K. M. Kedziora and K. Jalink, “Fluorescence resonance energy transfer microscopy (FRET),” *Methods Mol. Biol. Clifton NJ*, vol. 1251, pp. 67–82, 2015, doi: 10.1007/978-1-4939-2080-8_5.
[122] M. M. Lee and B. R. Peterson, “Quantification of Small Molecule–Protein Interactions using FRET between Tryptophan and the Pacific Blue Fluorophore,” *ACS Omega*, vol. 1, no. 6, pp. 1266–1276, Dec. 2016, doi: 10.1021/acsomega.6b00356.
[123] T. Zhang, T. Wei, Y. Han, H. Ma, M. Samieegohar, P.-W. Chen, I. Lian, and Y.-H. Lo, “Protein–Ligand Interaction Detection with a Novel Method of Transient Induced Molecular Electronic Spectroscopy (TIMES): Experimental and Theoretical Studies,” *ACS Cent. Sci.*, vol. 2, no. 11, pp. 834–842, Nov. 2016, doi: 10.1021/acscentsci.6b00217.
[124] P.-W. Chen, C.-Y. Tseng, F. Shi, B. Bi, and Y.-H. Lo, “Measuring Electric Charge and Molecular Coverage on Electrode Surface from Transient Induced Molecular Electronic Signal (TIMES),” *Sci. Rep.*, vol. 9, no. 1, p. 16279, Nov. 2019, doi: 10.1038/s41598-019-52588-6.
[125] P.-W. Chen, C.-Y. Tseng, F. Shi, B. Bi, and Y.-H. Lo, “Detecting Protein-Ligand Interaction from Integrated Transient Induced Molecular Electronic Signal (i-TIMES),” *Anal. Chem.*, vol. 92, no. 5, pp. 3852–3859, Mar. 2020, doi: 10.1021/acs.analchem.9b05310.
[126] A. Manickam, R. Singh, N. Wood, B. Li, A. Ellington, and A. Hassibi, “A fully-electronic charge-based DNA sequencing CMOS biochip,” in *2012 Symposium on VLSI Circuits (VLSIC)*, Jun. 2012, pp. 126–127. doi: 10.1109/VLSIC.2012.6243822.
[127] S. Fischer, D. Muratore, S. Weinreich, A. Peña-Perez, R. M. Walker, C. Gupta, R. T. Howe, and B. Murmann, “Low-Noise Integrated Potentiostat for Affinity-Free Protein Detection With 12 nV/rt-Hz at 30 Hz and 1.8 pArms Resolution,” *IEEE Solid-State Circuits Lett.*, vol. 2, no. 6, pp. 41–44, Jun. 2019, doi: 10.1109/LSSC.2019.2926644.
[128] H. Li, S. Parsnejad, E. Ashoori, C. Thompson, E. K. Purcell, and A. J. Mason, “Ultracompact Microwatt CMOS Current Readout With Picoampere Noise and Kilohertz Bandwidth for Biosensor Arrays,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 1, pp. 35–46, Feb. 2018, doi: 10.1109/TBCAS.2017.2752742.
[129] P. Prabha, S. J. Kim, K. Reddy, S. Rao, N. Griesert, A. Rao, G. Winter, and P. K. Hanumolu, “A Highly Digital VCO-Based ADC Architecture for Current Sensing Applications,” *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1785–1795, Aug. 2015, doi: 10.1109/JSSC.2015.2414428.
[130] S.-Y. Lu and Y.-T. Liao, “A 19 μW, 50 kS/s, 0.008-400 V/s Cyclic Voltammetry Readout Interface With a Current Feedback Loop and On-Chip Pattern Generation,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 2, pp. 190–198, Apr. 2021, doi: 10.1109/TBCAS.2021.3062377.
[131] M. Stanacevic, K. Murari, A. Rege, G. Cauwenberghs, and N. V. Thakor, “VLSI Potentiostat Array With Oversampling Gain Modulation for Wide-Range Neurotransmitter Sensing,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 1, pp. 63–72, Mar. 2007, doi: 10.1109/TBCAS.2007.893176.
[132] S. S. Ghoreishizadeh, I. Taurino, G. De Micheli, S. Carrara, and P. Georgiou, “A Differential Electrochemical Readout ASIC With Heterogeneous Integration of Bio-Nano Sensors for Amperometric Sensing,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 5, pp. 1148–1159, Oct. 2017, doi: 10.1109/TBCAS.2017.2733624.
[133] A. Manickam, K.-D. You, N. Wood, L. Pei, Y. Liu, R. Singh, N. Gamini, M. W. McDermott, D. Shahrjerdi, R. G. Kuimelis, and A. Hassibi, “A CMOS Electrochemical Biochip With 32×32 Three-Electrode Voltammetry Pixels,” *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 2980–2990, Nov. 2019, doi: 10.1109/JSSC.2019.2941020.

[134] T. Zhang, T.-H. Ku, Y. Han, R. Subramanian, I. A. Niaz, H. Luo, D. Chang, J.-J. Huang, and Y.-H. Lo, "Transient Induced Molecular Electronic Spectroscopy (TIMES) for study of protein-ligand interactions," *Sci. Rep.*, vol. 6, p. 35570, Oct. 2016, doi: 10.1038/srep35570.
[135] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "A 92dB dynamic range sub-μVrms-noise 0.8μW/ch neural-recording ADC array with predictive digital autoranging," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, Feb. 2018, pp. 470–472. doi: 10.1109/ISSCC.2018.8310388.
[136] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "Sub-μVrms-Noise Sub-μW/Channel ADC-Direct Neural Recording With 200-mV/ms Transient Recovery Through Predictive Digital Autoranging," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3101–3110, Nov. 2018, doi: 10.1109/JSSC.2018.2870555.
[137] N. Wood and N. Sun, "Predicting ADC: A new approach for low power ADC design," in *2014 IEEE Dallas Circuits and Systems Conference (DCAS)*, Oct. 2014, pp. 1–4. doi: 10.1109/DCAS.2014.6965323.
[138] P. Shettigar and S. Pavan, "Design Techniques for Wideband Single-Bit Continuous-Time ΔΣ Modulators With FIR Feedback DACs," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2865–2879, Dec. 2012, doi: 10.1109/JSSC.2012.2217871.
[139] K. L. Chan, N. Rakuljic, and I. Galton, "Segmented Dynamic Element Matching for High-Resolution Digital-to-Analog Conversion," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 55, no. 11, pp. 3383–3392, Dec. 2008, doi: 10.1109/TCSI.2008.2001757.
[140] H. Chandrakumar and D. Marković, "A 15.2-ENOB 5-kHz BW 4.5-μW Chopped CT ΔΣ-ADC for Artifact-Tolerant Neural Recording Front Ends," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3470–3483, Dec. 2018, doi: 10.1109/JSSC.2018.2876468.
[141] F. Colodro and A. Torralba, "New Continuous-Time Multibit Sigma–Delta Modulators With Low Sensitivity to Clock Jitter," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 56, no. 1, pp. 74–83, Jan. 2009, doi: 10.1109/TCSI.2008.922178.
[142] L. Lah, J. Choma, and J. Draper, "A continuous-time common-mode feedback circuit (CMFB) for high-impedance current-mode applications," *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 47, no. 4, pp. 363–369, Apr. 2000, doi: 10.1109/82.839673.
[143] D. Ying and D. A. Hall, "Current Sensing Front-Ends: A Review and Design Guidance," *IEEE Sens. J.*, pp. 1–1, 2021, doi: 10.1109/JSEN.2021.3094830.
[144] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *2008 IEEE Asian Solid-State Circuits Conference*, Nov. 2008, pp. 269–272. doi: 10.1109/ASSCC.2008.4708780.
[145] W. Choi, Y. Lee, S. Kim, S. Lee, J. Jang, J. Chun, K. A. A. Makinwa, and Y. Chae, "A Compact Resistor-Based CMOS Temperature Sensor With an Inaccuracy of 0.12 °C (3 σ) and a Resolution FoM of 0.43 pJ·K2 in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3356–3367, Dec. 2018, doi: 10.1109/JSSC.2018.2871622.
[146] P. W. Glimcher, "Understanding dopamine and reinforcement learning: the dopamine reward prediction error hypothesis," *Proc. Natl. Acad. Sci. U. S. A.*, vol. 108 Suppl 3, pp. 15647–15654, Sep. 2011, doi: 10.1073/pnas.1014269108.
[147] S. B. Floresco, "The nucleus accumbens: an interface between cognition, emotion, and action," *Annu. Rev. Psychol.*, vol. 66, pp. 25–52, Jan. 2015, doi: 10.1146/annurev-psych-010213-115159.
[148] C. E. Larson and E. Meng, "A review for the peripheral nerve interface designer," *J. Neurosci. Methods*, vol. 332, p. 108523, Feb. 2020, doi: 10.1016/j.jneumeth.2019.108523.
[149] E. Kandel, J. D. Koester, S. H. Mack, and S. Siegelbaum, *Principles of Neural Science, Sixth Edition*, 6th edition. New York: McGraw-Hill Education / Medical, 2021.
[150] T. Chi, J. S. Park, J. C. Butts, T. A. Hookway, A. Su, C. Zhu, M. P. Styczynski, T. C. McDevitt, and H. Wang, "A Multi-Modality CMOS Sensor Array for Cell-Based Assay and Drug Screening," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 6, pp. 801–814, Dec. 2015, doi: 10.1109/TBCAS.2015.2504984.

[151] J. Dragas, V. Viswam, A. Shadmani, Y. Chen, R. Bounik, A. Stettler, M. Radivojevic, S. Geissler, M. E. J. Obien, J. Müller, and A. Hierlemann, "In Vitro Multi-Functional Microelectrode Array Featuring 59 760 Electrodes, 2048 Electrophysiology Channels, Stimulation, Impedance Measurement, and Neurotransmitter Detection Channels," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1576–1590, Jun. 2017, doi: 10.1109/JSSC.2017.2686580.

[152] C. M. Lopez, H. S. Chun, S. Wang, L. Berti, J. Putzeys, C. Van Den Bulcke, J.-W. Weijers, A. Firrincieli, V. Reumers, D. Braeken, and N. Van Helleputte, "A Multimodal CMOS MEA for High-Throughput Intracellular Action Potential Measurements and Impedance Spectroscopy in Drug-Screening Applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3076–3086, Nov. 2018, doi: 10.1109/JSSC.2018.2863952.

[153] S.-Y. Park, J. Cho, K. Na, and E. Yoon, "Modular 128-Channel Δ-ΔΣ Analog Front-End Architecture Using Spectrum Equalization Scheme for 1024-Channel 3-D Neural Recording Microsystems," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 501–514, Feb. 2018, doi: 10.1109/JSSC.2017.2764053.

[154] G. Winterer and D. R. Weinberger, "Genes, dopamine and cortical signal-to-noise ratio in schizophrenia," *Trends Neurosci.*, vol. 27, no. 11, pp. 683–690, Nov. 2004, doi: 10.1016/j.tins.2004.08.002.

[155] D. B. Miller and J. P. O'Callaghan, "Biomarkers of Parkinson's disease: present and future," *Metabolism.*, vol. 64, no. 3 Suppl 1, pp. S40-46, Mar. 2015, doi: 10.1016/j.metabol.2014.10.030.

[156] R. Z. Goldstein and N. D. Volkow, "Dysfunction of the prefrontal cortex in addiction: neuroimaging findings and clinical implications," *Nat. Rev. Neurosci.*, vol. 12, no. 11, pp. 652–669, Nov. 2011, doi: 10.1038/nrn3119.

[157] L. Squire, D. Berg, F. E. Bloom, S. du Lac, A. Ghosh, and N. C. Spitzer, Eds., *Fundamental Neuroscience*, 4th edition. Amsterdam ; Boston: Academic Press, 2012.

[158] S. D. Niyonambaza, P. Kumar, P. Xing, J. Mathault, P. De Koninck, E. Boisselier, M. Boukadoum, and A. Miled, "A Review of Neurotransmitters Sensing Methods for Neuro-Engineering Research," *Appl. Sci.*, vol. 9, no. 21, Art. no. 21, Jan. 2019, doi: 10.3390/app9214719.

[159] M. Laruelle, A. Abi-Dargham, C. H. van Dyck, W. Rosenblatt, Y. Zea-Ponce, S. S. Zoghbi, R. M. Baldwin, D. S. Charney, P. B. Hoffer, and H. F. Kung, "SPECT imaging of striatal dopamine release after amphetamine challenge," *J. Nucl. Med. Off. Publ. Soc. Nucl. Med.*, vol. 36, no. 7, pp. 1182–1190, Jul. 1995.

[160] W. C. Drevets, J. C. Price, D. J. Kupfer, P. E. Kinahan, B. Lopresti, D. Holt, and C. Mathis, "PET measures of amphetamine-induced dopamine release in ventral versus dorsal striatum," *Neuropsychopharmacol. Off. Publ. Am. Coll. Neuropsychopharmacol.*, vol. 21, no. 6, pp. 694–709, Dec. 1999, doi: 10.1016/S0893-133X(99)00079-2.

[161] L. Tang, S. Li, F. Han, L. Liu, L. Xu, W. Ma, H. Kuang, A. Li, L. Wang, and C. Xu, "SERS-active Au@Ag nanorod dimers for ultrasensitive dopamine detection," *Biosens. Bioelectron.*, vol. 71, pp. 7–12, Sep. 2015, doi: 10.1016/j.bios.2015.04.013.

[162] S. Zadran, S. Standley, K. Wong, E. Otiniano, A. Amighi, and M. Baudry, "Fluorescence resonance energy transfer (FRET)-based biosensors: visualizing cellular dynamics and bioenergetics," *Appl. Microbiol. Biotechnol.*, vol. 96, no. 4, pp. 895–902, Nov. 2012, doi: 10.1007/s00253-012-4449-6.

[163] R. H. S. Westerink, "Exocytosis: Using Amperometry to Study Presynaptic Mechanisms of Neurotoxicity," *NeuroToxicology*, vol. 25, no. 3, pp. 461–470, Mar. 2004, doi: 10.1016/j.neuro.2003.10.006.

[164] M. L. A. V. Heien, M. A. Johnson, and R. M. Wightman, "Resolving Neurotransmitters Detected by Fast-Scan Cyclic Voltammetry," *Anal. Chem.*, vol. 76, no. 19, pp. 5697–5704, Oct. 2004, doi: 10.1021/ac0491509.

[165] P. Takmakov, C. J. McKinney, R. M. Carelli, and R. M. Wightman, "Instrumentation for fast-scan cyclic voltammetry combined with electrophysiology for behavioral experiments in freely moving animals," *Rev. Sci. Instrum.*, vol. 82, no. 7, p. 074302, Jul. 2011, doi: 10.1063/1.3610651.

[166] R. B. Keithley, P. Takmakov, E. S. Bucher, A. M. Belle, C. A. Owesson-White, J. Park, and R. M. Wightman, "Higher Sensitivity Dopamine Measurements with Faster-Scan Cyclic Voltammetry," *Anal. Chem.*, vol. 83, no. 9, pp. 3563–3571, May 2011, doi: 10.1021/ac200143v.
[167] N. T. Rodeberg, S. G. Sandberg, J. A. Johnson, P. E. M. Phillips, and R. M. Wightman, "Hitchhiker's Guide to Voltammetry: Acute and Chronic Electrodes for in Vivo Fast-Scan Cyclic Voltammetry," *ACS Chem. Neurosci.*, vol. 8, no. 2, pp. 221–234, Feb. 2017, doi: 10.1021/acschemneuro.6b00393.
[168] H. Wang and L. Pilon, "Physical interpretation of cyclic voltammetry for measuring electric double layer capacitances," *Electrochimica Acta*, vol. 64, pp. 130–139, Mar. 2012, doi: 10.1016/j.electacta.2011.12.118.
[169] B. Bozorgzadeh, D. P. Covey, C. D. Howard, P. A. Garris, and P. Mohseni, "A Neurochemical Pattern Generator SoC With Switched-Electrode Management for Single-Chip Electrical Stimulation and 9.3 μW, 78 pA rms , 400 V/s FSCV Sensing," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 881–895, Apr. 2014, doi: 10.1109/JSSC.2014.2299434.
[170] C. I. Dorta-Quiñones, X. Y. Wang, R. K. Dokania, A. Gailey, M. Lindau, and A. B. Apsel, "A Wireless FSCV Monitoring IC With Analog Background Subtraction and UWB Telemetry," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 289–299, Apr. 2016, doi: 10.1109/TBCAS.2015.2421513.
[171] M. Roham, D. P. Covey, D. P. Daberkow, E. S. Ramsson, C. D. Howard, B. A. Heidenreich, P. A. Garris, and P. Mohseni, "A Wireless IC for Time-Share Chemical and Electrical Neural Recording," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3645–3658, Dec. 2009, doi: 10.1109/JSSC.2009.2035549.
[172] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Wireless Micropower Instrumentation for Multimodal Acquisition of Electrical and Chemical Neural Activity," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 6, pp. 388–397, Dec. 2009, doi: 10.1109/TBCAS.2009.2031877.
[173] B. N. Kim, A. D. Herbst, S. J. Kim, B. A. Minch, and M. Lindau, "Parallel Recording of Neurotransmitters Release from Chromaffin Cells Using a 10 × 10 CMOS IC Potentiostat Array with On-Chip Working Electrodes," *Biosens. Bioelectron.*, vol. 41, pp. 736–744, Mar. 2013, doi: 10.1016/j.bios.2012.09.058.
[174] H. M. Jafari, K. Abdelhalim, L. Soleymani, E. H. Sargent, S. O. Kelley, and R. Genov, "Nanostructured CMOS Wireless Ultra-Wideband Label-Free PCR-Free DNA Analysis SoC," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1223–1241, May 2014, doi: 10.1109/JSSC.2014.2312571.
[175] J. Guo, W. Ng, J. Yuan, S. Li, and M. Chan, "A 200-Channel Area-Power-Efficient Chemical and Electrical Dual-Mode Acquisition IC for the Study of Neurodegenerative Diseases," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 3, pp. 567–578, Jun. 2016, doi: 10.1109/TBCAS.2015.2468052.
[176] H. Zamani, S.-A. Chan, C. Smith, and P. Mohseni, "A Neurochemical Recording Microsystem with Analog Background Current Subtraction and 400V/s FSCV Sensing Using a 1st-Order ΔΣM," Aug. 2020, pp. 517–520. doi: 10.1109/MWSCAS48704.2020.9184687.
[177] B. Nasri, T. Wu, A. Alharbi, K.-D. You, M. Gupta, S. P. Sebastian, R. Kiani, and D. Shahrjerdi, "Hybrid CMOS-Graphene Sensor Array for Subsecond Dopamine Detection," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 6, pp. 1192–1203, Dec. 2017, doi: 10.1109/TBCAS.2017.2778048.
[178] D. Ying, C.-Y. Tseng, P.-W. Chen, Y.-H. Lo, and D. Hall, "A 30.3 fA/Hz Biosensing Current Front-End with 139 dB Cross-Scale Dynamic Range," *IEEE Trans. Biomed. Circuits Syst.*, pp. 1–1, 2021, doi: 10.1109/TBCAS.2021.3124197.
[179] H. M. Jafari and R. Genov, "Chopper-Stabilized Bidirectional Current Acquisition Circuits for Electrochemical Amperometric Biosensors," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 60, no. 5, pp. 1149–1157, May 2013, doi: 10.1109/TCSI.2013.2248771.
[180] K.-D. Kim, S. Kang, Y.-K. Choi, K.-H. Lee, C.-H. Lee, J. Lee, M. Choi, K. Ko, J. Jung, N. Park, H. Park, and G.-C. Hwang, "A fully-differential capacitive touch controller with input common-mode

feedback for symmetric display noise cancellation," in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, Jun. 2014, pp. 1–2. doi: 10.1109/VLSIC.2014.6858444.

[181] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation, 3rd Edition*, 3rd edition. Piscataway, NJ : Hoboken, NJ: Wiley-IEEE Press, 2010.

[182] M. G. Kim, G.-C. Ahn, P. K. Hanumolu, S.-H. Lee, S.-H. Kim, S.-B. You, J.-W. Kim, G. C. Temes, and U.-K. Moon, "A 0.9 V 92 dB Double-Sampled Switched-RC Delta-Sigma Audio ADC," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1195–1206, May 2008, doi: 10.1109/JSSC.2008.920329.

[183] S. Pavan and P. Sankar, "Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1365–1379, Jul. 2010, doi: 10.1109/JSSC.2010.2048082.