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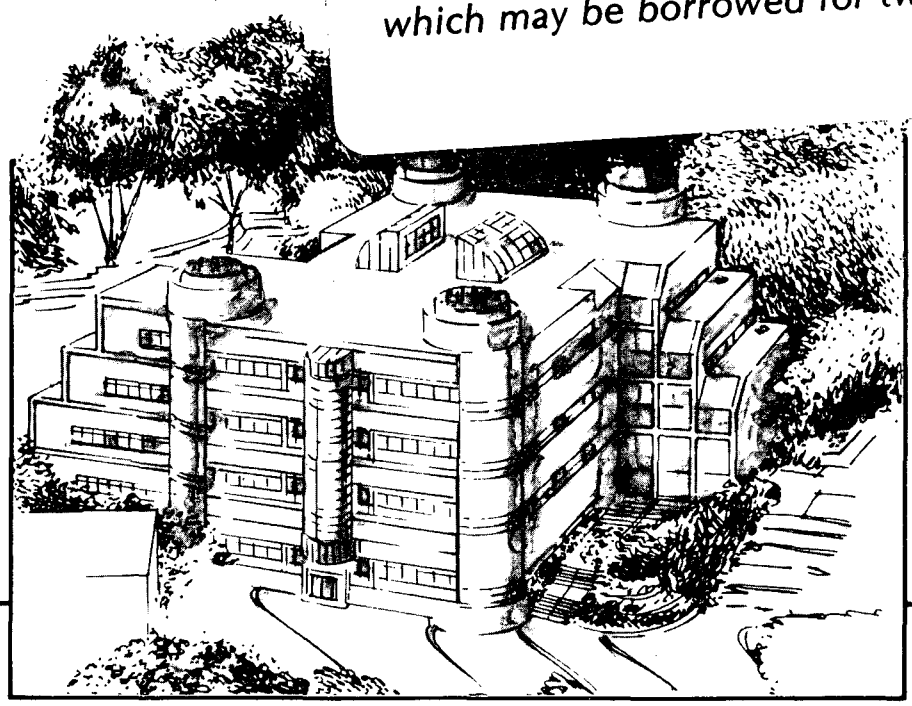

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METHODS TO DECREASE DEFECT DENSITY IN GaAs/Si HETEROEPITAXY

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ABSTRACT

In this paper, the fundamental mechanisms of procedures improving the structural quality of GaAs grown on Si are discussed. Patterned growth, strained layer superlattices and proper thermal cycling are promising approaches to achieve a high quality of GaAs layers grown on Si substrates.

INTRODUCTION

Recent developments in the field of GaAs/Si heteroepitaxy have been spurred [1] by the possibility of combining high-speed GaAs material with well-established Si technology, thus gaining better thermal conductivity, higher fracture toughness, smaller weight and larger diameters wafers offering the possibility for integration of optoelectronic and digital devices. Unfortunately, many problems are encountered in growth of GaAs on Si, such as growth of polar crystal on nonpolar substrate, lattice mismatch of 4.1%, and a considerable difference in thermal expansion coefficient between epilayer and substrate. As a consequence of these problems, the quality of GaAs epilayers on Si substrates is very poor. This is evidenced clearly by the width of the X-ray rocking curve, which is typically more than an order of magnitude broader than in GaAs/GaAs homoepitaxy [2]. The dominant defects in the GaAs epilayer are misfit dislocations formed at the interface with Si, stacking faults, microtwins and threading dislocations which propagate through the epilayer.

ORIGIN OF DEFECTS IN THE EPILAYER

Interfacial Contamination

In addition to the problems caused by lattice and thermal mismatch, one of the most important origins of defect formation in the epilayer are irregularities and residual contamination at the interface (Figs. 1 a, b). Protrusions such as shown in this figure clearly originate at oxide or carbide contaminants at the substrate. Many of them can be avoided by proper cleaning. The most commonly used method for preparation of the Si substrate is the Ishizaka method [3]. However, after such cleaning islands of impurities can still be observed [4]. Cross sectional transmission electron microscopy (TEM) shows typically a white band at the interface between the GaAs and Si, which has frequently been attributed to artifacts of the TEM sample preparation. Our own investigation of metal/GaAs heterostructures deposited in-situ in ultra high vacuum did not reveal such a white band. Only air-exposed surfaces showed such a white band at the interface[5,6]. In GaAs/Si heteroepitaxy formation of this white contrast does not occur after application of a Ga reduction process as suggested by Kroemer [7,8], confirming that in most cases this white contrast is indicative of contamination at the hetero-interface.

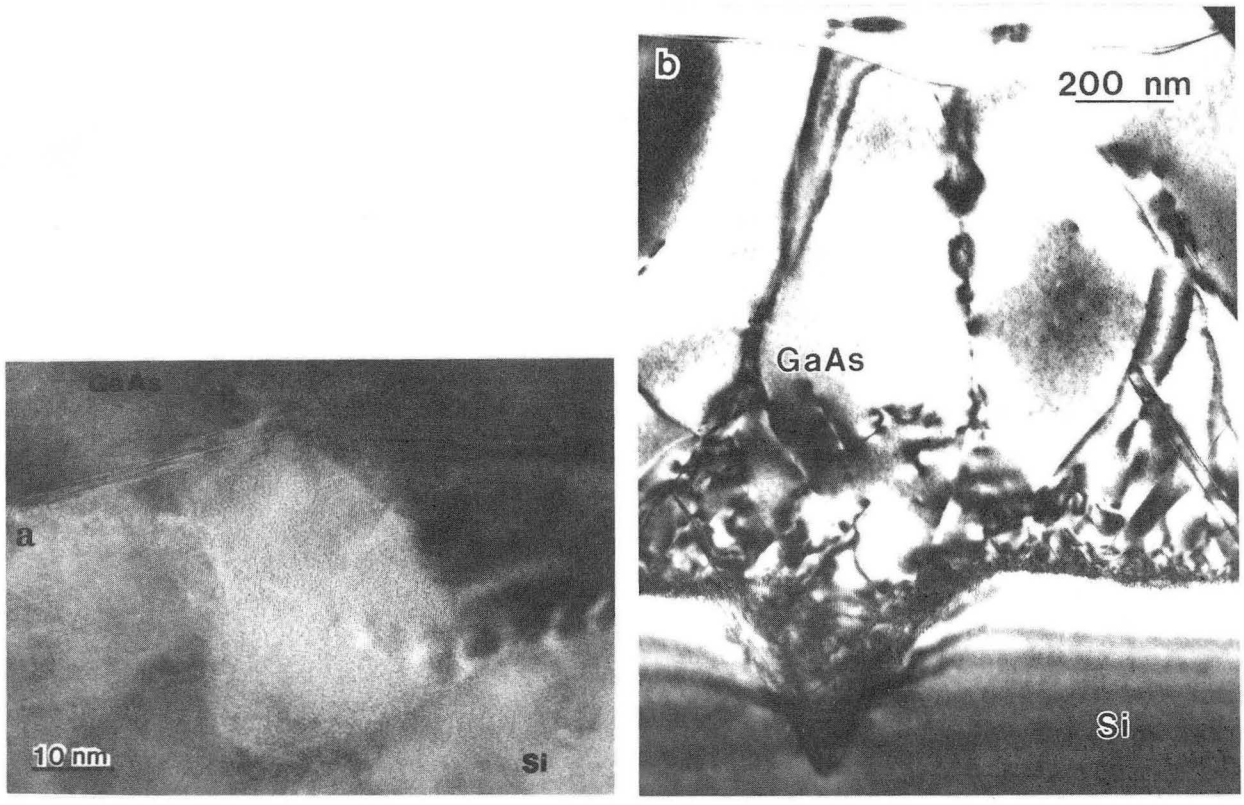

Fig. 1: TEM micrographs of GaAs grown on: a) (211) Si surface, b) (100) Si surface. Protrusions with oxygen and carbon contamination were found on both surfaces. Such contamination are additional sources for dislocations and stacking faults formation as indicated on these micrographs.

Island Nucleation

Initial growth of GaAs on Si is often observed to start from islands [9-11]. Coalescence of the islands can result in the formation of additional defects. Islands with small lateral dimensions are strained and free of dislocations. The thickness of such islands can easily exceed the critical thickness as e.g. calculated by Matthews and Blakeslee [12]. Upon increasing lateral dimensions of the islands, misfit dislocations become visible at the interface. One possible mechanism for misfit dislocation formation for large islands is the glide of half loops from the island surface to the interface. Such half loops generate misfit dislocations at the interface which relieve interfacial strain. The "arms" of such half loops form threading dislocations in the epilayer. Two types of misfit dislocations were detected at GaAs/Si (100) heterointerfaces: 90° dislocations with Burgers vector parallel to the interface which are sessile (Lomer type), and glissile 60° dislocations with Burgers vector inclined to the interface. These dislocations relieve a smaller amount of stress compared to Lomer-type dislocations [13]. Therefore a higher density of these dislocations is required to relieve the same stress. Moreover, the 60° dislocations can glide back into the epilayer, which makes them less desirable.

Polar on non-polar growth

Polar on non-polar growth is connected with the appearance of antiphase domains (APDs). Their appearance is most probably due to the presence of single steps at the Si surface and the preferred bonding of As with Si. The presence of single steps was observed by using many surface sensitive techniques [14] and it was confirmed by cross-sectional TEM using the Atomic

Resolution Microscope in Berkeley with a point-to-point resolution of 1.7 Å [15]. APDs can be detected by chemical etching of the surface [16] or by TEM using the convergent beam technique [17, 18] or dark field imaging for 200 and -200 reflection [19]. The dark field imaging technique allows to detect *differences* in polarity, but the convergent beam technique can be used to determine directly the polarity of even a single domain on a microscale [17].

Such APDs are three-dimensional islands and the boundaries (APBs) between these islands can be formed on low index as well as on high index planes. Our own observations show that very often such boundaries macroscopically appear to be formed on various planes (Fig. 2), such as for example on {111} planes, although microscopically they consist of terraces of {110} APBs [18]. Formation of APBs on {110} planes would confirm Petroff's prediction that {110} and {112} APBs with alternating As-As and Ga-Ga bonds have the lowest energy of formation [20].

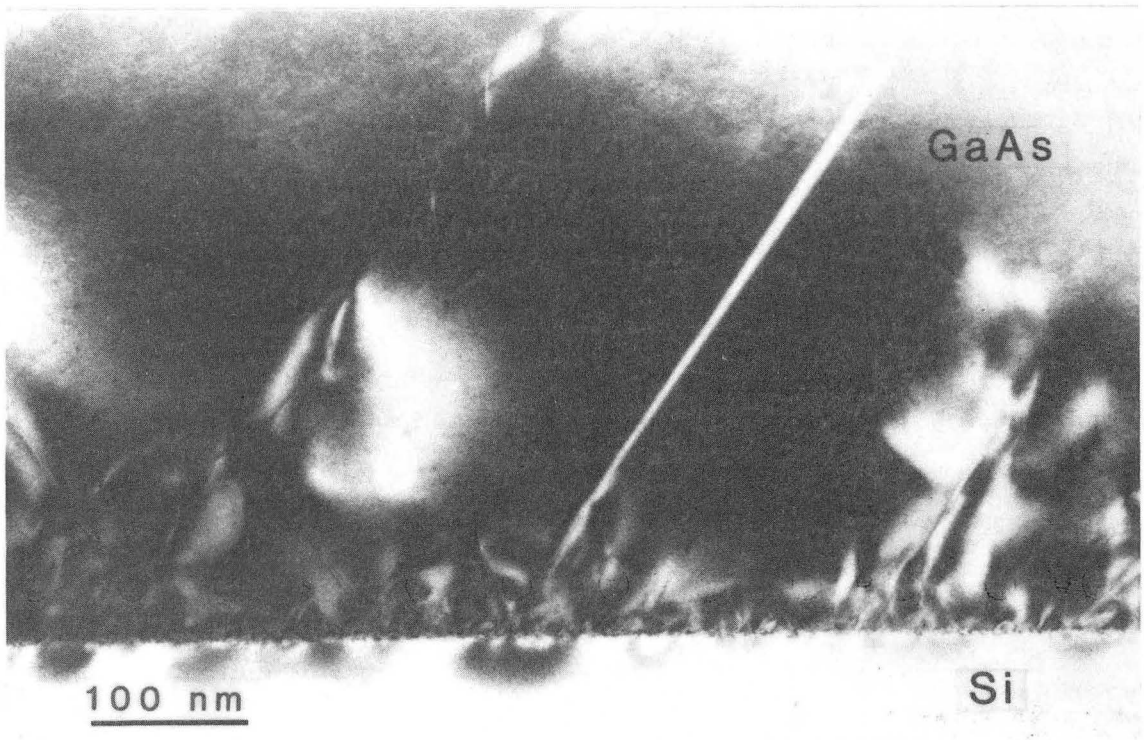

Fig. 2: TEM micrograph of GaAs grown on (100) Si showing an antiphase boundary, as confirmed by CBED analysis [18]. The antiphase boundary is composed of small facets along {110} planes (edge-on or inclined) which, when viewed as a whole, appears to be parallel to the {111} microtwin planes shown on this micrograph.

It has been reported that misorientation from the nominal (100) orientation by rotation of 2°-4° about the [011] direction leads to the disappearance of antiphase boundaries [21-23]. Our own observations show that even for such misoriented substrates antiphase domains can be found if the growth conditions are not optimized, preferentially in the areas close to the interface [24]. Many of these domains terminate inside the epilayer so that only a small number of APBs extend to the surface. Drastic changes of the APD density are observed upon changing the growth parameters. After post-growth annealing APD free layers even on nominal (100) substrates were found [16]. The growth of APD free GaAs is an essential achievement in GaAs heteroepitaxy, reached within the last two years.

Different Thermal Expansion Coefficients

Photoluminescence studies have shown that tensile strain is present in GaAs grown on Si, rather than compressive strain as expected from the lattice mismatch between GaAs (5.653 Å) and Si (5.431 Å). We found that the number of misfit dislocations is related to the stress relief at the growth temperature and this number is too high for room temperature [25]. The difference in thermal expansion coefficient (a_{GaAs} = 6.8 x 10^{-6}/°C, a_{Si} = 2.6 x 10^{-6}/°C) produces new strain during cooling from the growth temperature opposing the lattice mismatch strain [26]. The tensile strain observed experimentally is considerably lower than the expected value 2.4 x 10^{-3}, indicating strain relief by plastic flow. Cooling from 600°C to only 400°C is sufficient to generate a biaxial tensile stress far above the experimentally determined critical resolved shear stress of 15 MPa at 400°C [27], which will result in the glide of additional threading dislocations of various types from the interface into the epilayer. In addition, misfit dislocations at the interface can be forced to dissociate on a {111} plane inclined to the interface, leaving one partial dislocation at the interface and forming an extended stacking fault. The formation of extended stacking faults by glide processes was first found in plastically deformed semiconductors cooled under high stress [28,29]. An alternative explanation of formation of such planar defects can be their nucleation at the initial stage of growth for strain relief [30].

HOW TO DECREASE DEFECT DENSITY?

Conventional two-step growth

A very successful method for the growth of GaAs on Si is two-step growth in which an initial buffer layer ~100-300Å thick is grown at low temperature (~400°C), and then at ~650°C to continue growth. The dislocation density decreases with layer thickness due to the interaction and annihilation of dislocations. Pearton et al. [31] showed directly by X-ray rocking curve analysis the increase of cristalline quality with GaAs layer thickness. However, with increasing layer thickness new problems occur with cracking, wafer bowing and decreased energy dissipation through a thick GaAs layer during device operation, which limits the thickness of useful GaAs/Si to 2-3μm.

Two-dimensional Initial Growth

GaAs generally starts to grow on Si in the form of islands [9]. Several reasons might lead to such three-dimensional growth. Island formation may be connected with strain due to lattice mismatch, surface tension of the epilayer, preferred growth at surface steps or growth only in areas free of impurities. Coalescence of such islands is very often connected with formation of additional defects such as dislocations and antiphase boundaries. It was shown that even in the case of GaP grown on Si where mismatch is much smaller than between GaAs and Si three-dimensional growth occurs [32,33].

One promising method is to start with a lattice-mismatched system such as AlGaP which provides very good wetting of the substrate. Umeno's group reported first the role of Al during growth of GaP on Si [32, 33]. The addition of small amounts of Al causes perfect two-dimensional growth (Fig. 3). This might be due to the high affinity of Al for oxide formation, allowing to grow Al compounds on clean and contaminated surfaces [32].

Another very promising method is migration-enhanced epitaxy in which the Ga and As flux is alternating [34] or modulation enhanced epitaxy with continous As flux and intermittend Ga flux [35]. It was demonstrated that this kind of growth ensures two dimensional growth and results in very narrow PL lines.

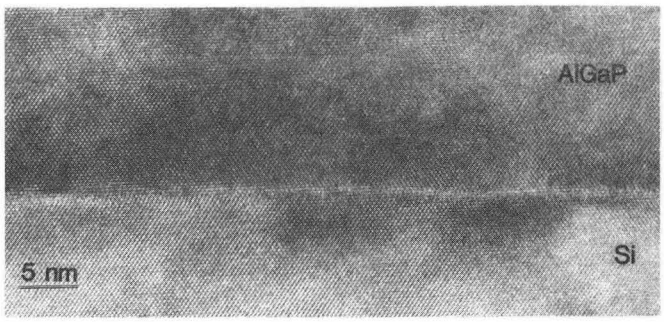

Fig. 3: High resolution image of the AlGaP/Si interface showing perfect two dimensional growth by adding of Al to GaP (in contrast to three dimensional growth of GaP on Si).

Post-Annealing

a) Furnace Annealing

If the heteroepitaxial layer is grown strain-free with the correct density of misfit dislocations at the interface, any change of temperature will induce strain, the sign and magnitude of which depends on the difference between growth temperature and annealing. Thus it is possible to move dislocations by thermal cycling during or after the growth. It was reported that annealing at 850°C under arsenic overpressure results in dislocation rearrangement at the interface forming a majority of Lomer type dislocations and decreasing the number of stacking faults [36, 37]. Our own observations do not confirm these results fully. Furnace annealing at 800°C for 10 min changed only slightly the defect rearrangement [Fig. 4]. The dislocation density remains in the same range as for "as-grown samples" but they are more tangled. A slight decrease in stacking fault density was observed. This discrepancy can indicate a strong dependence on the detailed annealing conditions, requiring careful optimization.

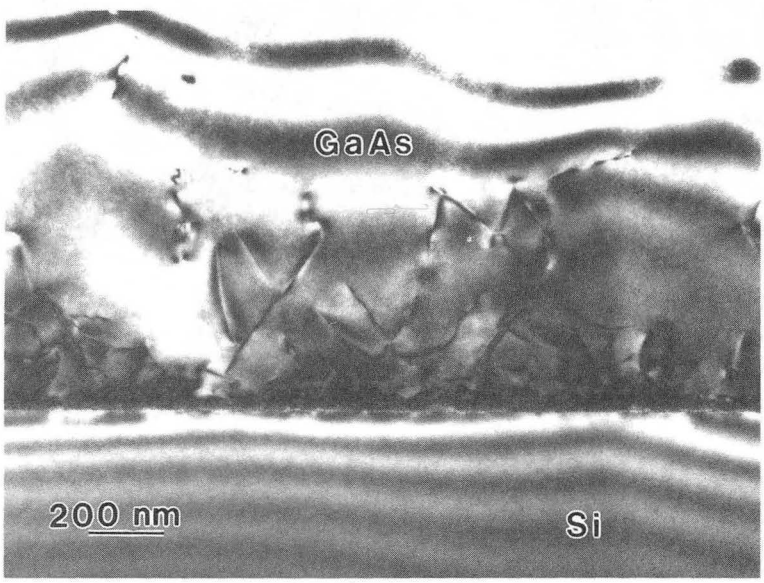

Fig. 4:. TEM micrograph of GaAs/Si (100) after furnace annealing.

b) Rapid Thermal Annealing

Noticeable improvements in the quality of GaAs/Si epilayers grown by MBE were observed after rapid thermal annealing (RTA) at 800°C for 10 sec by the capless close-proximity method in a commercial heatpulse furnace. The density of stacking faults after this treatment was very low [Fig. 5], possibly because of the different cooling rate compared to furnace annealing. Partial dislocations which were mobilized during annealing and could glide back to the interface to recombine with the second partial. During rapid cooling they were "frozen" in this state and did not dissociate again into partials. This mechanism is beneficial for the removal of stacking faults, but

prohibitss stress relief during cooling down, and this is evidenced by cracking of the GaAs epilayers which experienced RTA. Cracking was even more severe than in as-grown samples. The heterointerface is observed to be more undulated after RTA, compared to as-deposited samples. Independent electrical measurements of devices after RTA [38] showed noticable improvement for forward and reverse bias characteristics. Leakage currents were reduced by more than two orders of magnitude after this treatment.

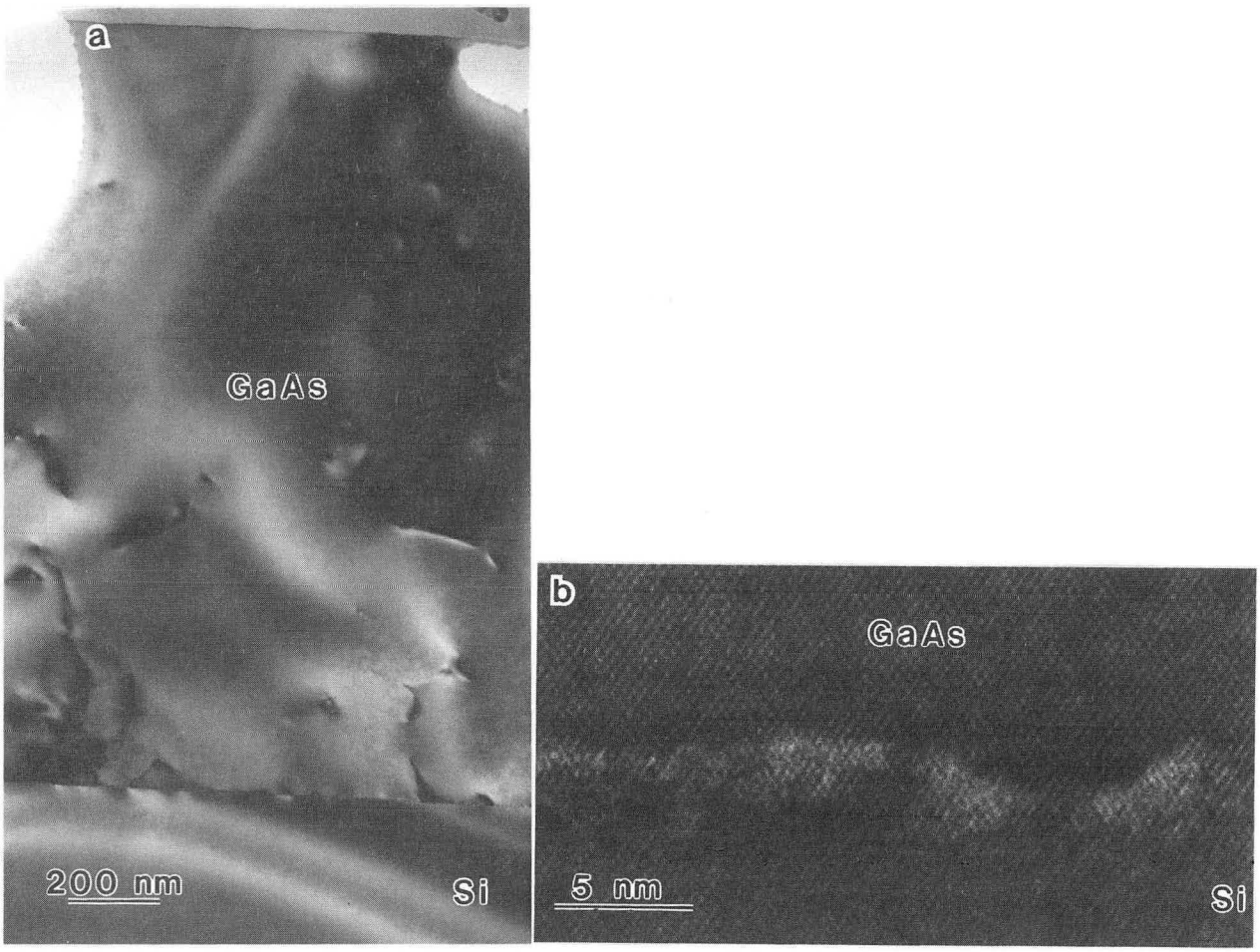

Fig. 5: a) TEM micrograph of the GaAs/Si (100) interface after RTA annealing.
b) High resolution image of the GaAs/Si interface showing ondulation of the interface after RTA and complete ellimination of the stacking faults.

c) In-situ Annealing

It was reported that in-situ annealing at 800°C for 5 min. during growth is more efficient in defect reduction than ex-situ annealing [39]. This causes visible dislocation bending, providing a better chance for threading dislocations to interact and, ideally, to move to the periphery of the wafer. After this treatment the density of dislocations was reduced to $2 \times 10^{-7}/cm^2$ [39].

Yamaguchi et al. [40, 41] carried out an even more successful thermal treatment during MOCVD growth. It involved thermal cycling during growth in which annihilation and coalescence of dislocations were caused by dislocation movement under the alternating thermal stress. The growth of the GaAs was interrupted several times, and the substrate temperature was lowered to room temperature, followed by a temperature increase up to 900°C and subsequent annealing for up to 15 min at this temperature in an arsine atmosphere. After this treatment, the substrate temperature was again lowered to 700°C and a new layer of GaAs was grown in the same fashion. This process was repeated several times. The reported dislocation density for GaAs grown on Si

with such thermal cycling was estimated from the etch pit density to be as low as 1-2 x $10^6/cm^2$. Such thermal cycling during growth appears to be a very promising approach for decreasing the defect density in the heterolayer.

Patterned Growth

The goal to grow a lattice mismatched heteroepilayer with a network of misfit dislocations confined to the interface and no threading dislocations in the epilayer is difficult to achieve for a homogeneous 3" wafer. It would require glide of the threading "arms" of misfit dislocations across the whole wafer without being blocked by other threading dislocations. However, it appears to be much easier to achieve this goal if the growth area is confined to a small part of the substrate, e.g. by pattering lines or mesas on the substrate.

One example of such patterned growth is the growth of GaAs on Si through openings in an oxide or nitride [42-44]. Our own results [45] show that GaAs grown above the SiN mask was polycrystalline, but in the open areas where the nitride was removed monocrystalline GaAs was detected with much lower dislocation density than in typical two step growth [Fig. 6]. The stacking fault density was much lower in the entire pattern, increasing only at the border with nitride. This decrease in defect density is probably connected with the stress release at the periphery of patterns in polycrystalline areas. Post-growth annealing at 850°C in arsenic overpressure results in significant grain growth in the remaining polycrystalline GaAs overgrown on the amorphous areas such as oxides or nitrides, and elimination of the defects at the transition region from polycrystalline to single crystal growth. An increase of Hall mobility of 30% was observed in these annealed samples. Fitzgerald et al. proposed patterned growth by growing a lattice mismatched $In_{0.05}Ga_{0.95}As$ layer on free standing mesa structures of GaAs (2μm high with 60nm diameters and larger). Only misfit dislocations were observed in these structures. The epi-layer was dislocation free, no threading dislocations were detected by cathodoluminescence in these structures. This method may also be useful in the growth of GaAs on Si substrates, however particular design patterns should be tested in order to determine if the result is compatible with device applications.

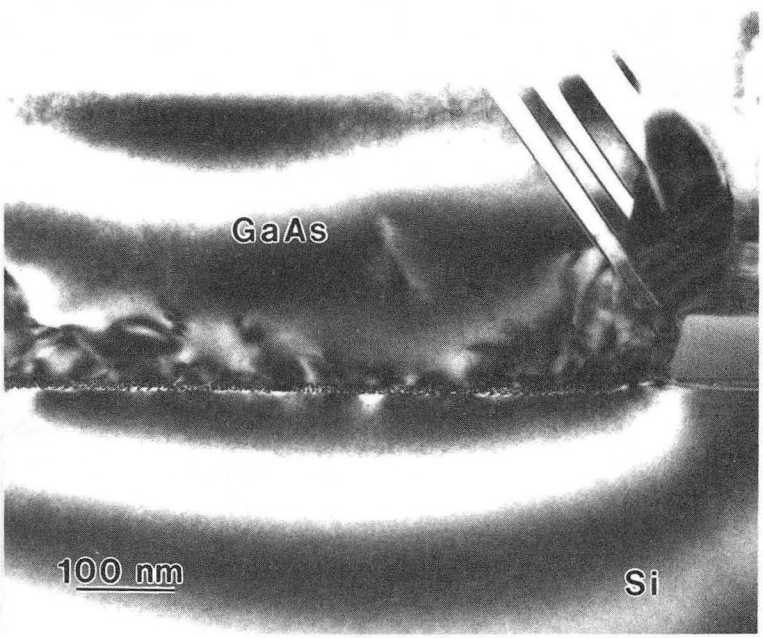

Fig. 6: Cross-section TEM micrograph near the patterned boundary. Note stacking faults present at the boundary with polycrystalline material grown over SiN and very low density of defects within the stripe of 100nm width GaAs.

Strained Layer Superlattices

As mentioned before, in order to obtain device quality epitaxial GaAs material, a reliable method for suppressing defect propagation in the epilayer is necessary. One promising method is to use strained layer superlattices (SLSLs), which cause dislocations to bend into the strained interface, thus promoting dislocation interactions. It was reported [8] that by application of SLSLs of InGaAs/GaAs with 10 nm thick periods grown on Si (211) blocking of dislocation propagation did not occur at all interfaces inside the SLSLs, but occured almost entirely at the uppermost interface between the strained layers and the final GaAs layer [Fig.7]. It was concluded that reduction of dislocation density was only weakly dependent on the number periods of the strained-layer superlattices. InGaAs/GaAs strained-layer superlattices proved to be more efficient in dislocation bending than InGaAs/InGaP SLSLs. Because it was recognized that the number of periods did not influence the reduction of dislocation propagation and that the upper interface of SLSLs is most efficient in dislocation bending, packages consisting of 5 periods of SLSLs (InGaAs/GaAs) were applied. Indeed, each set of SLSLs caused additional dislocation bending, but in some areas additional dislocations were formed at the lower interface between the buffer layer and the SLSL (Fig. 8). Therefore, in some areas the dislocation density was slightly higher. However, on the average, the dislocation density in this sample was in the ~2 x $10^7/cm^2$ range, which is very low taking into account that all misfit dislocations in the GaAs grown on Si(211) are 60° dislocations with Burgers vector inclined to the interface.

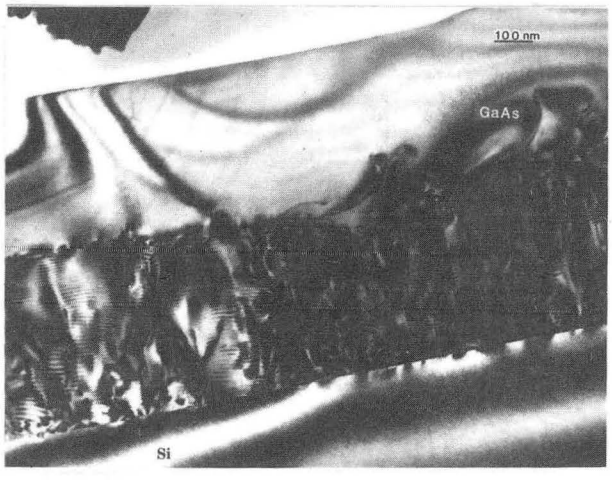

Fig. 7: TEM cross-section micrograph of the GaAs/Si interface with 50 periods of InGaAs(25%In)/GaAs SLSL grown directly at the interface with Si. Note the large number of stacking faults formed at the interface, propagating through the SLSL and stoping at the last interface with epilayer of GaAs. Bending of dislocations was most effective at this interface as well.

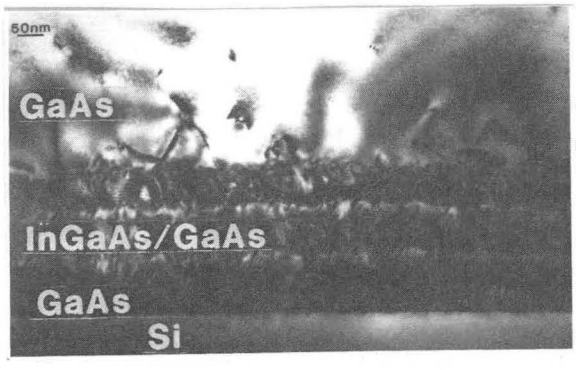

Fig. 8: TEM micrograph of the GaAs/Si interface with the application of three packages of ten periods each of the InGaAs/GaAs SLSL. Note dislocation bending at each package interface (occasionaly, the formation of new dislocation was observed). Application of packages of SLSL was most succesful to decrease dislocation density in the epilayer.

This kind of SLSL was applied to growth of GaAs on Si(100) and results obtained were very similar [47] to the ones obtained on Si (211) surfaces. Yamaguchi et al. [48] reported that strain is related to the composition of SLSLs and their thickness. Two kinds of critical thickness are important to achieve successful application of SLSLs: a critical thickness h_{c1} must be exceeded to introduce enough strain necessary for dislocation bending and the layers should not exceed a critical thickness h_{c2} which causes the generation of new dislocations.

CONCLUSIONS

This report on the mechanisms to reduce the density of structural defects in heteroepitaxial growth of GaAs on Si leads to the promising conclusion that such growth is possible and higher quality of the epilayer appears to be possible. The first step, the controlled growth of antiphase domain free GaAs/Si has been achieved. The cleaning of the Si substrate has been improved, but is not yet satisfactory. Of special interest should be approaches avoiding the high temperature substrate annealing steps currently used. Such high annealing temperatures result in roughening of the Si surface and are generally incompatible with patterned epitaxy. A promising approach is the use of Ga reduction and/or the growth of ternary, Al-containing buffer layers as pioneered by Umeno's group [32, 33].

Further defect reduction strategies such as thermal cycling during the growth, post-growth annealing and the use of strained layer superlattices have to be optimized. Combined use of some of these methods together with the possibilities of patterned epitaxy appear to make high-quality growth of lattice mismatched heterostructures such as GaAs/Si achievable. Only such optimized low-defect material will allow to make practical use of the numerous devices possible with this technology, including minority carrier devices, the feasibility of which already have been demonstrated in GaAs/Si heteroepitaxy.

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