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TOWARD A SELF-POWERED MM-SCALE MEMS SENSOR PLATFORM THROUGH HETEROGENEOUS INTEGRATION OF SCUM AND HV SOI CMOS

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ABSTRACT

This work presents a novel, ultra-thin, multipurpose micro-electromechanical system (MEMS) sensor platform that integrates on-chip power, control, actuation, and sensing. Two silicon-on-insulator (SOI) wafers undergo thermocompression bonding (TCB) and substrate release to form an 80 μm thick device with no substrate consisting of two silicon device layers. MEMS devices on both the upper and lower SOI layers provide sensing and actuation for the platform, and solar cells formed with in-situ doping harvest power for the sensor platform. Optionally, integrated circuits can be attached to the platform through TCB to provide analog, digital, and other RF functionality. In this work, we describe the platform's fabrication process and characterize the performance of solar cells and SOI MEMS devices, such as mechanical joints and electrostatic motors. We then present an example of a fully integrated sensor system using the proposed platform.

KEYWORDS

Thermocompression bonding (TCB), MEMS CMOS Integration, Silicon on Insulator MEMS (SOI - MEMS)

INTRODUCTION

Recent advances in ultra-thin chiplet system integration such as high-bandwidth memory (HBM) stacks and system-in-package (SiP) technologies have demonstrated the potential of miniaturized, high-performance systems composed of multiple specialized chiplets interconnected via silicon interposers [1]. These architectures enable scalable solutions for applications such as high-speed computation processing.

However, existing approaches focus primarily on electronic integration and lack support for the co-integration of electromechanical (MEMS) devices, energy-harvesting elements, and wireless communication modules within the same platform [2]. Such integration is particularly relevant for compact systems like wearable electronics, implantable biomedical devices, and autonomous microrobots. These applications require millimeter-scale integrated system platforms that can perform sensing, computation, actuation, and communication while generating and managing their own power. Such sensor platforms are typically built on printed circuit boards (PCBs) populated with multiple discrete components, often leading to centimeter-scale footprints unsuitable for the tighter size constraints of next-generation devices [3].

Building on our previous work on silicon-on-insulator-based PCB (SOI-PCB) concepts, we present advances in our microfabrication methods to enable the co-integration of MEMS devices, solar cells, inductors, and multilayer wiring within a single, ultra-thin substrate [4].

The resulting platform supports the heterogeneous integration through TCB of CMOS integrated circuits, forming a monolithic sensor system at millimeter scale.

To illustrate these capabilities, we propose a representative mm-scale sensor platform shown in Fig. 1 containing: 1) SC μ M-V, a heterogeneously integrated system-on-chip (SoC) featuring a radio, a microcontroller, clock generation, and NFC-based bootloading, [5] 2) fully released MEMS devices, including accelerometers for sensing and gap-closing actuators (GCAs) for electrostatic actuation, 3) high-voltage solar cell array integrated into the substrate for on-package power generation, and 4) an inductor supporting wireless power or communication functionalities.

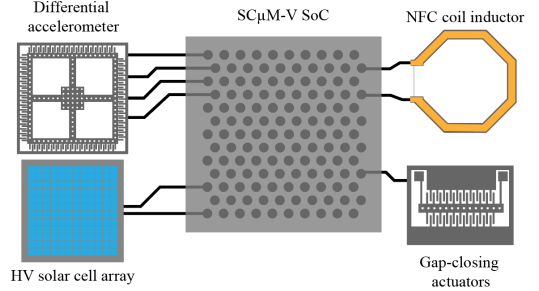


Figure 1: Proposed mm-scale MEMS sensor platform combining a wireless SoC with in situ MEMS sensors and actuators, solar cells, and RF passives.

This work details the fabrication process, design, and characterization of the MEMS, solar cell, and inductor devices in an ultra-thin form factor platform suitable for advanced sensing and actuation in miniature systems.

FABRICATION

The presented sensor platform shown in Fig. 2 is composed of two patterned single-crystal silicon (SCS) device layers fabricated on separate silicon-on-insulator (SOI) wafers and subsequently bonded and released from their substrates. Both the upper and lower halves of the device are fabricated using conventional planar microfabrication processes on 40-2-550 μm SOI substrates. Each half integrates electrical interconnects, doped regions, and MEMS structures. A silicon nitride layer electrically isolates two conductive layers while gold is employed as both an interconnect via and a thermocompression bond (TCB) interface.

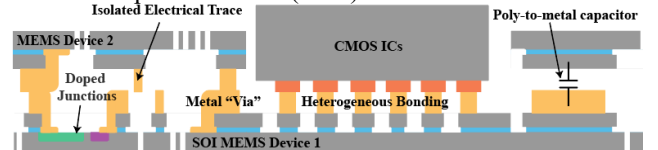


Figure 2: Cross section of the final proposed system and release. The final platform consists of two 40 μm device layers fabricated in identical planar processing and later bonded through gold-gold TCB and substrate release.

Planar Device Fabrication

Beginning with two standard 40-2-550 μm SOI wafers, we deposit a 150 nm thick silicon nitride layer to serve as an insulating barrier between the conductive layers. Next, a 550 nm thick N-type doped polysilicon layer is deposited and patterned to form the second electrical layer and to act as a hard mask for the subsequent wet nitride etch.

The exposed SCS regions are then selectively doped with either N-type or P-type dopants using thermal diffusion. An alumina (Al_2O_3) passivation layer is deposited and patterned to protect exposed nitride sidewalls. A 1.8 μm thick gold layer is electroplated onto a Ni-Au seed stack and serves three purposes: 1) forming vias between insulated conductive layers, 2) defining TCB bond sites, and 3) acting as the main body of the second electrical layer. MEMS features are then etched into the SCS device layer using deep reactive ion etching (DRIE), followed by a second DRIE step to define through-wafer etch holes and dicing lanes. The final planar device prior to bonding is shown in Fig. 3.

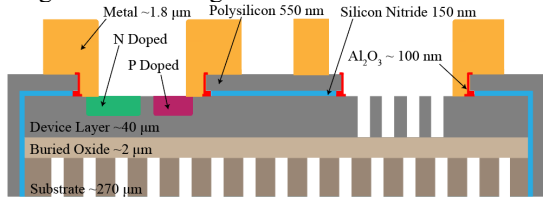


Figure 3: Detailed cross section of the SOI wafers after planar device fabrication steps. Gold pillars resting on top of the polysilicon serve as the bond sites for the TCB.

Thermocompression Bonding and Release

Gold-to-gold thermocompression bonding is performed at the chip level using a Finetech Lambda flip-chip bonder at 325°C. The top and bottom chiplets are aligned such that the gold bond pads on each wafer interface directly, establishing both mechanical and electrical contact. Approximately 7.5% of the total die area is allocated for gold bond pads to ensure sufficient mechanical rigidity during handling.

Following bonding, bonded chiplets undergo a 180-minute vapor-phase hydrofluoric acid (VHF) release in KLA's Primaxx etcher. Buried oxide (BOX) layers are selectively removed and silicon substrate then fully detaching from the bonded device stack.

Thermal stability and chemical resistance of adhesion materials for the gold film were studied to improve bond strength. While titanium (Ti) and chromium (Cr) are commonly used, both are unsuitable in this process. Cr undergoes thermal diffusion during bonding, forming a Cr-Au alloy that migrates toward the surface, degrading adhesion and compromising mechanical integrity [6]. Titanium, while thermally stable, exhibits poor etch resistance against vapor HF, resulting in complete removal of the Ti layer during full substrate release.

A comparative summary of failure modes across different adhesion materials is provided in Table 1. Based on these evaluations, both nickel (Ni) and titanium-tungsten (TiW) were identified as viable candidates. Ni was selected due to its good thermal stability and solder wettability, facilitating post-bonding integration with tin-based solders for future packaging steps.

Table 1: Summary of Failure Occurred in Adhesion Layer Metal Tested During TCB and VHF Release.

Adhesion Layer	Failure Mode	Description
Cr	Thermal	Bond sites prone to delamination due to Cr diffusion through Au for TCB above 200°C
Ti	Chemical	Poor etch resistance in VHF
Ni	None	Small amount of nickel fluoride formation in vapor HF
TiW	None	Self-terminating etching in VHF

SELF-POWERED SENSOR PLATFORM

Key building blocks of a self-powered sensor platform include solar cell arrays, MEMS sensors and actuators, mechanical linkages, and multilayer wiring. Each component fabricated in the proposed process is described in detail in the following subsections.

HV Solar Cell Array

A functional solar cell requires both a PN junction and a conductive wiring layer, as illustrated in Fig. 4. In the presented platform, the PN junctions are formed during thermal dopant diffusion while adjacent cells are electrically isolated by front-side DRIE. The conductive trace layer consists of electroplated gold, insulated by a silicon nitride layer and patterned on the second SCS device layer. Electrical connections to both N- and P-doped regions are made using gold-to-gold TCB, eliminating the need for wire bonding. The cells are back-illuminated during the operation.

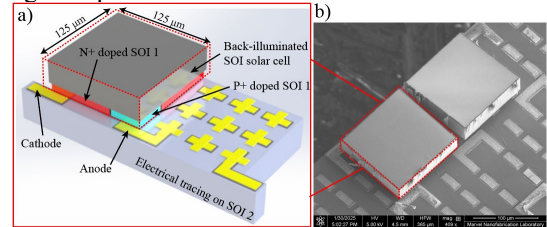


Figure 4: a) Illustration of a single solar cell fabricated in upper SOI and bonded to traces on the lower SOI. b) SEM images of the fabricated single solar cells.

The gold trace layer supports flexible configuration of solar cells in either series or parallel to accommodate different voltage and current requirements. We demonstrate a high-voltage (HV) solar cell array configured in series to drive GCAs, as shown in Fig. 5. A ring light with an intensity of 1.7 mW/mm^2 is used to illuminate the array from the backside. Under these conditions, 80 connected cells achieve a total output power of 0.972 mW with an open-circuit voltage of 53.2 V and a short-circuit current of 18.4 μA .

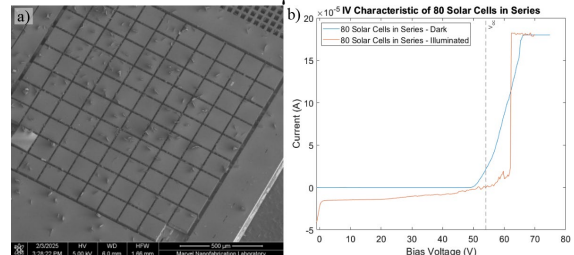


Figure 5: a) SEM image of a HV solar cell array. b) I-V characteristics of the array with ring lights on and off.

Anchor-Free MEMS Devices

Unlike conventional MEMS devices fabricated on unreleased SOI substrates, the MEMS devices presented here are fully released from their substrate and operate without anchors. Gold bond sites serve as mechanical and

electrical connection within the same die, as illustrated in Fig. 6. This anchor-free design enables seamless integration of previously demonstrated MEMS architectures, such as GCAs and inchworm actuators [7].

GCAs are patterned into the SCS device layer using DRIE and are connected to the trace layer through gold bond pads. A measured pull-in voltage of 91 V is observed, accompanied by a leakage current of 18 mA, which is suspected to originate from shorting between fingers due to organic contamination introduced during fabrication.

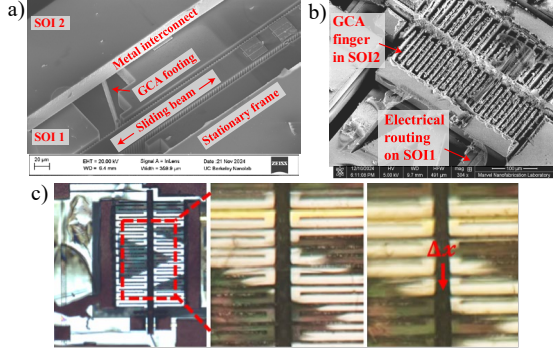


Figure 6: a) Close-up SEM image of the released bilayer SOI slider mechanism. The sliding beam is a prismatic joint confined by the frame with one degree of freedom. b) SEM image of a GCA bonded to a wiring layer on the second SOI. c) The GCA is driven with external power supply applied on metal contact pads.

The anchor-free design also enables complex, fully released mechanical features previously constrained by compliant flexures or soft springs in traditional SOI MEMS designs. For example, rotary joints fabricated using this platform no longer require elastic elements to maintain connectivity. Instead, features are constrained through interlocking structures formed across the bonded layers. A ring-shaped stator in the lower device layer bonded to a bar in the upper layer enables full 3D confinement of a rotor, eliminating the need for spring elements and reducing mechanical energy loss during actuation. Both spring-free rotary and prismatic joints in motion are shown in Fig. 7.

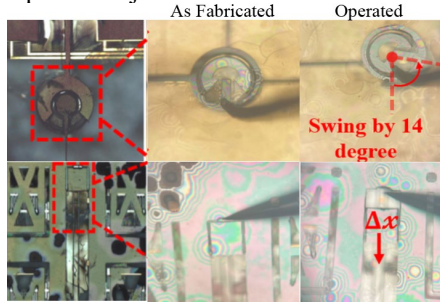


Figure 7: Microscopic view of two types of mechanical linkages in bilayer SOI devices, rotational (top) and prismatic (bottom). The fully released rotor is confined within a stator frame with a single degree of freedom of movement. A probe tip is used to move the rotor and to demonstrate the full range of motion.

Multiple Interlayer Connection

The presented platform supports four electrically insulated layers, N+ poly and SOI on each side, enabling multilayer wiring and compact interconnect architectures. Interlayer connectivity is achieved through gold vias that optionally short N+ poly to the underlying SOI layer, and gold TCBs that connect N+ poly on opposite SOI layers.

In a typical single-layer planar MEMS process, routing signals from differential capacitor fingers across multiple unit cells often results in layout conflicts due to intersecting

traces. As a result, compact differential capacitors are difficult to implement. In contrast, the multilayer architecture in this platform allows front and rear capacitor fingers to be routed on separate silicon layers—front fingers are shorted together via gold interconnects to the second SCS layer while rear fingers are routed on the first SCS layer as illustrated in Fig. 8. Additionally, both sets of fingers are electrically insulated from the moving proof mass via silicon nitride layers.

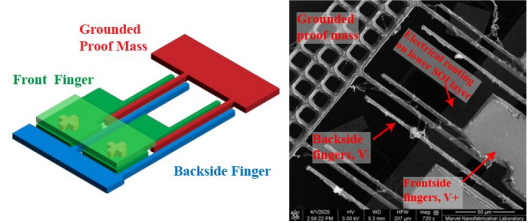


Figure 8: Illustration of the differential capacitor (left) and SEM image (right) with components colored by the nets of the electrical signals. The front finger is connected via the second SOI layer to reduce wiring complexity.

This same interlayer wiring strategy is applied to implement a pull-in relay for GCA feedback control. In this configuration, a control voltage of 1.8 V is applied to the gap-stop electrode of a Pensky-style GCA [8]. As the stator voltage increases, the grounded rotor is electrostatically attracted toward the gap stop. Upon contact, a measurable voltage drop occurs, providing a signal that can be monitored by a microcontroller to detect pull-in events. This mechanism enables closed-loop feedback for efficient GCA operation, particularly under variable loads.

Routing control signals to multiple gap-stop relays in an actuator array poses significant challenges in conventional SOI MEMS due to limited wiring flexibility. The multilayer interconnect approach in this platform resolves this issue by distributing the pull-in relay supply voltage through the second silicon layer, with gold vias connecting down to each gap stop. The final integrated relay-enabled GCA array is shown in Fig. 9.

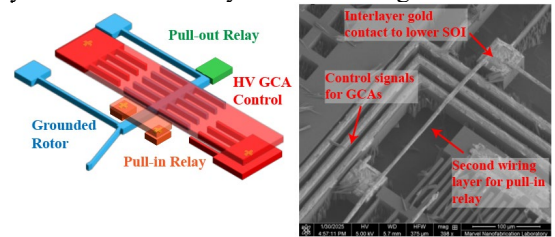


Figure 9: Illustration of the four I/O connected to a GCA (left) and SEM image (right) with HV GCA control and pull-in relay signal wired through the second SOI layer.

Wireless Capabilities

The SCμM-V SoC integrates a 2.4 GHz Bluetooth Low Energy (BLE) and IEEE 802.15.4 radio, and future generations are expected to incorporate near-field communication (NFC) tag functionality for power harvesting and over-the-air boot-loading [5]. However, while the NFC coil required at 13.56 MHz (typically 1-3 μH) is too large for the 2 × 2 mm SCμM-V SoC, it would be well-suited to construction within our substrate.

Our microfabricated sensor platform provides a gold-on-poly insulated electrical layer that can be used to fabricate planar spiral inductors appropriate for NFC coils, sub-GHz antennas, and RF filters. The direct integration of these RF features within the substrate reduces form factors

and simplifies system-level integration.

Toward this goal, general-purpose planar spiral inductor test structures were designed and fabricated to evaluate the experimental relative permeability of inductors integrated directly into the platform. Single-turn, rectangular planar inductors with widths of 180, 280, 380, and 480 μm were measured with inductance of 0.38, 0.65, 0.89, and 1.1 nH. The measured inductance is lower than the theoretical value by 18%, but we attribute the difference to thickness variations in the insulating nitride.

FULL SYSTEM INTEGRATION

Differential Accelerometer

A two-axis differential capacitive accelerometer was fabricated to demonstrate the multilayer wiring capabilities of the presented platform as shown in Fig. 10. The device features a 52- μg proof mass suspended by crab-leg springs, allowing a displacement range of $\pm 1 \mu\text{m}$ along both the x- and y-axes. The system is designed to achieve a displacement resolution of 60 pm when interfaced with a 10 μV analog-to-digital converter (ADC). Preliminary capacitance measurements were performed by displacing the proof mass using a micromanipulator. The intrinsic capacitance between the proof mass and the front electrodes was measured to be 0.852 pF, increasing to 1.71 pF when the proof mass contacted the gap stop along one axis. The measured capacitance values were lower than the expected design targets, likely due to residual footing artifacts from front-side DRIE and fluorocarbon residues introduced during the backside release process.

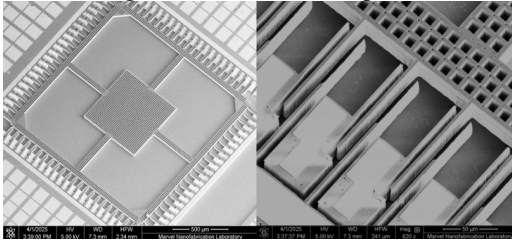


Figure 10: SEM image of the differential capacitive sensor (left) and close-up image of the capacitive fingers (right).

System Integration

As a proof-of-concept of the proposed fabrication method, a $14 \times 6 \text{ mm}$ ultra-thin sensor platform was fabricated as shown on Fig. 11. The integrated system incorporates multiple heterogeneous components on a single substrate, including bond sites for interfacing with the SC μ M-V, six HV solar cell arrays, GCA arrays, and a two-axis differential capacitive accelerometer. These components are co-fabricated within the same multilayer structure, assembled with TCB, and connected in the substrate's multiple routing layers.

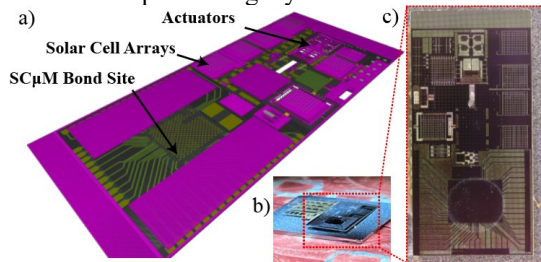


Figure 11: a) Illustration of the fully integrated self-powered sensor platform with on-board sensing and actuation. b) Macroscopic view of the fully released system as yet not function.

c) System headshot of the fabricated platform.

CONCLUSION

This work presents an ultra-thin, self-powered MEMS sensor platform enabled by multilayer SOI microfabrication. An 80 μm thick device stack that integrates multiple functional layers for sensing, actuation, power harvesting, and signal routing within a single compact footprint is achieved. A gold adhesion layer compatible with thermocompression bonding and vapor HF release is explored for the process. Key components demonstrated on the platform include high-voltage solar cell arrays, anchor-free gap-closing actuators (GCAs), multiple interlayers connect, and substrate-integrated inductors for wireless applications.

The co-integration of passive and active components highlights the feasibility of building monolithic microsystems without the need for PCB-level packaging. The demonstrated platform represents a significant step toward miniaturized, autonomous sensor systems for applications such as micro robotics, biomedical devices, and next-generation IoT nodes. Future work will focus on perfecting device release process, expanding device list to 3D MEMS features and communication elements, and packaging and testing the full system in application environments.

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