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Progress in hybrid-silicon photonic integrated circuit technology

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Adding III-V materials to the silicon-on-insulator platform enables increasingly complex devices, making it well-positioned to address energy-efficient, compact, and low-cost photonic applications.

Photonic integration is the technology that allows the combination of different optical components, such as lasers, modulators, and photodetectors, on a single photonic chip. Such devices are known as photonic integrated circuits (PICs). The prospect of medium- and large-scale integration, with tens to hundreds of components on a single chip, is a major driver for research on silicon photonics in the silicon-on-insulator (SOI) platform. The SOI fabrication infrastructure is compatible with the mature and high-quality CMOS technology, which is robust and reproducible and has high yield. It is possible to make PICs in the SOI platform on large 200mm-diameter wafers, and this allows for low cost and high volumes. Since these PICs can operate at wavelengths of 1.3 and 1.55μm, prime application candidates are telecommunication and interconnects.[1]

The SOI platform offers an almost complete suite of photonic components, including filters, (de)multiplexers, splitters, modulators, and photodetectors. However, electrically pumped efficient sources on silicon remain a challenge due to this substance's indirect bandgap.

The integration of III-V materials, such as indium phosphide (InP), gives the SOI platform access to the complete suite of high-speed and efficient III-V-based photonic components. The hybrid-silicon complex heterogeneously incorporates III-V functionality on the SOI platform by means of molecular wafer bonding.[2] Hybrid-silicon III-V waveguides have the properties of the III-V material, such as gain, high-speed modulation, and photodetection, but are still located on an SOI circuit (see Figure 1). We can use tapered-mode converters to change a hybrid mode into a mode that resides fully in the silicon waveguide. We can also fabricate the active III-V components with lithographic precision and alignment accuracy, thereby enabling large-scale integration. This is done in a back-end process after the SOI fabrication, which means we avoid contamination of a CMOS foundry and that the III-V manufacturing is in principle fully compatible with the SOI-CMOS fabrication procedure. The hybrid-silicon platform combines the maturity and scale of CMOS processing and SOI photonics with essential III-V functionality and, as such, is unique and well-positioned for medium-scale photonic integration.

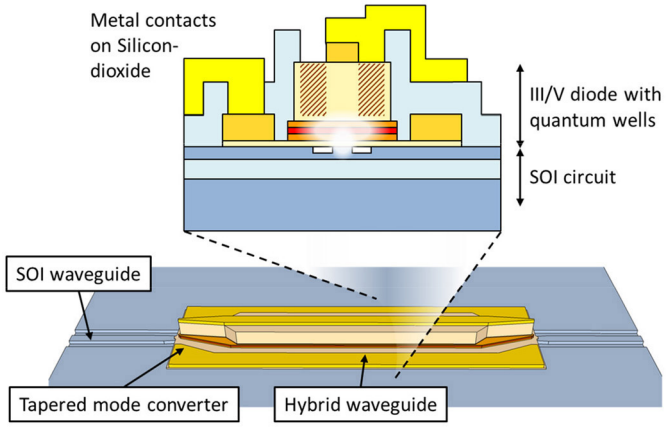

Figure 1. *Diagram showing a hybrid-silicon III-V optical amplifier integrated with a silicon waveguide (bottom) and the hybrid waveguide cross section (top). Tapered-mode converters form the interface between the silicon and hybrid waveguide. The optical mode (white) overlaps with both the silicon waveguide and the III-V quantum wells (red). The top p-contact and the lateral n-contacts (yellow) provide electrical current. The device achieves current confinement by ion implanting the p-mesa (dashed). SOI: Silicon on insulator.*

The timeline of Figure 2 shows the success of the hybrid-silicon technology, which we developed in collaboration with

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Intel, since its conception in 2006. In this graphic, we plot the PIC complexity as a function of time and show both the progress of InP-based and hybrid-silicon PICs. It is clear that InP-based monolithic integration has increased its complexity exponentially over the last two decades. Hybrid-silicon PICs are catching up fast though, with highly integrated transmitters,[5] switches,[6] and optical phased arrays.[7] There seem to be three major factors for this. First, hybrid-silicon photonics can make use of the mature CMOS fabrication infrastructure for at least part of the process flow. Second, the hybrid-silicon platform builds on the already existing knowledge of III-V-based photonics and rapidly incorporates that into the platform. And, finally, there is an early adoption by industry, with companies like Intel, HP, and Aurrion being active in this field and developing the technology.

However, the close integration of multiple components puts upper limits on power dissipation per component to avoid thermal crosstalk and prohibitively large total power dissipation. This is especially important for future energy-efficient interconnect applications.[8] Our current efforts focus on optimizing the performance of tapered-mode converters and of hybrid waveguide geometry for laser and optical amplifier applications. We improved threshold current and slope efficiency of hybrid-silicon lasers by about 30% compared with our previous work. Advances in the fabrication process resulted in a reduction in series resistance by almost a factor of three. We realized low-loss and low-reflectivity mode converters, with losses of 0.3dB per transition and reflections better than −41dB, which is essential for high-performance PICs.

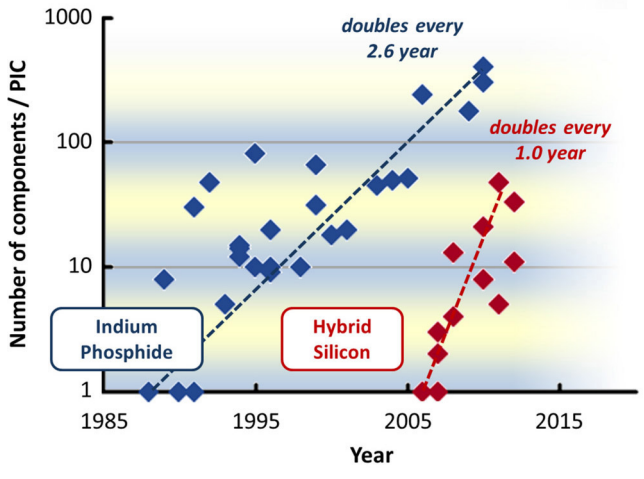

Figure 2. *Development of chip complexity measured as the number of components per chip. We show data for indium-phosphide-based photonic integrated circuits (PICs, blue)[3] and for hybrid-silicon PICs (red),[4] which fit to exponential growth curves (dashed).*

The progress shown in Figure 2 emphasizes that the hybrid-silicon platform has the potential to become the platform of choice for complex PICs. Future terabit-per-second datacom and interconnect applications will require fully integrated solutions, with volumes running into the 100ks to 1Ms per year. Compared with InP-based circuits, hybrid-silicon PICs offer the advantage of economies of scale, with their 200mm silicon substrates and CMOS-compatible fabrication technology. Besides being an economic driver, these applications are also a technology driver, with clear targets for energy-efficient operation. Our current work represents a step in this direction, with the goal of bringing the hybrid-silicon performance on par with the monolithic InP-based technology and meeting future demands on operation efficiency. We anticipate further improvement in PICs by optimizing the III-V material design. We are working on using this technology for, among others, ultra-low-noise microwave generation, free-space beam-steering chips, and high-speed transmitters for interconnects.

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