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A Chip-Level CDM ESD Protection Circuit Modeling and Simulation Method and Experimental Verification

A Thesis submitted in partial satisfaction
of the requirements for the degree of

Master of Science

in

Electrical Engineering

by

Han Wang

December 2018

Thesis Committee:
Dr. Albert Wang, Chairperson
Dr. Ming Liu
Dr. Shaolei Ren

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Han Wang
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The Thesis of Han Wang is approved:

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Committee Chairperson

University of California, Riverside

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To my family for all the support.

ABSTRACT OF THE THESIS

A Chip-Level CDM ESD Protection Circuit Modeling and Simulation Method and Experimental Verification

by

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University of California, Riverside, December 2018
Dr. Albert Wang, Chairperson

Electrostatic discharge (ESD) failure is one of the most challenging reliability problems to integrated circuits (ICs) and other electronic systems. Industrial statistics suggests that more than 30% of IC failures are caused by ESD or electro overstress (EOS) events [1], resulting in billions of dollars in losses annually to the industry. Therefore, ESD protection is required for all ICs and other electronic products. There are many different ESD characterization models and standards, such as, human body model (HBM) and charged device model (CDM), which are adapted by the industry. Among these ESD models, CDM ESD failure and protection design is extremely challenging due to the ultrafast nature of CDM ESD pulses.

As the semiconductor process technologies advance to sub-32nm nodes, CMOS gate oxide becomes thinner and the junction becomes shallower, making ICs more susceptible to ESD failure, especially the ultrafast CDM ESD surges [1]-[5]. On the other hand, costs for IC designs and fabrication at advanced IC technology nodes has become extremely high, which demands for first-Silicon design success of advanced IC chips.

Therefore, full-chip level ESD protection circuit simulation becomes desirable for on-chip ESD protection design, which has been a major challenge in IC designs due to the complexity of ESD protection at full chip level.

Substantial efforts have been devoted to developing full-chip circuit-level ESD protection design simulation techniques in recent years. For example, a chip-level ESD protection circuit simulation method for HBM ESD protection using SPICE was reported in [7]-[8], which allows accurate circuit-level ESD protection simulation. However, for the emerging CDM ESD protection designs, little success has been reported. This is largely due to the fact that CDM ESD events are extremely fast, down to 100ps for the rise time of an CDM ESD pulse, and the distribution of electrostatic charges inside an IC chip in CDM ESD mode is very difficult to model. The state-of-the-art in CDM ESD protection simulation utilizes an over-simplified lumped electrostatic charge distribution model, which does not reflect the real-world problem [43]-[52].

This thesis describes a novel distributed electrostatic charge distribution model and a new circuit-level simulation method to enable accurate full-chip CDM ESD protection circuit simulation, aiming to achieve CDM ESD protection design prediction and hence, first-Silicon design success in developing CDM ESD protection solutions for advanced ICs. The new CDM ESD model and simulation techniques developed was verified in ICs implemented in a commercial 28nm CMOS technology.

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Chapter 1 Introduction

1.1 What is ESD?

The earliest discovery of electrostatic phenomena traces back to Thales, a natural philosopher of ancient Greece. He found the attraction between rubbed amber and the straw rap in approximately 600 B.C.E [58]. From that on, scientists discovered the truth about ESD (electrostatic discharge) with constant exploration. ESD is an instantaneous charge flow between two charged objects. To be specific, when two charged objects with different electrostatic potentials are in direct contact, or the medium between these two objects is broken down by the electrostatic field when they are close to each other, a process of electrostatic charge transfer forms, which means ESD. For example, people will see the electric spark when they touch some metal in the dry winter. Thunder and lightning in nature are also ESD phenomena.

There are many ways to generate the static charge, for example, triboelectric charging, conducting charging, and inducing charging. Among them, triboelectric charging is the most common charging method. When two objects of different materials are in contact with each other and then separated, electrons will be transferred from one object to another, and the two objects carry the same amount of different charge.

ESD can seriously harm the quality of devices in microelectronics. For the integrated circuit industry, each IC (integrated circuit) is accompanied by static electricity among the lifetime including fabrication, packaging, testing, transportation, and even mounting onto the printed circuit board (PCB). Although there are numerous ways to reduce the static electricity source in the IC production, such as ground machines and increase humidity, static electricity cannot be completely eliminated. Therefore, it is necessary to add robust ESD protection circuits in the chip to enhance the ESD tolerance.

1.2 ESD Stress Models

ESD may occur in various situations. In order to evaluate the impact of ESD stress in different situations, some associations have published ESD stress models. Human body model (HBM), machine model (MM) and charged device model (CDM) are three elementary models that have been used in the industry to measure the ESD protection level of ICs.

1.2.1 Human Body Model

Human body model is the earliest defined and the most commonly used test model which refers to the ESD phenomenon that occurs when an electrostatically charged human body contacts a chip and forms a discharge path. The equivalent circuit is shown in Figure 1-1. At the beginning of the test, the switch is on the left (A), and the high voltage power source charges the human body equivalent capacitance C_{ESD} (100pF), indicating the static charge carried by the human body. Then the switch is turned to the right (B), and C_{ESD} discharges to the device under test (DUT) through the human body equivalent resistance

R_{ESD} (1.5kΩ). According to the JEDEC standards, HBM has a current rise time of approximately 2.0-10.0ns, a decay of 130-170ns, and a peak current of about 0.6-3.0A [53]. The test method of HBM is described as follows: first, select one pin as the input terminal of ESD stress generated by zapping guns, and then perform the zapping test with all other pins as the ground terminal in turn. The HBM test between every two pins consists of a positive pulse zapping and a negative pulse zapping.

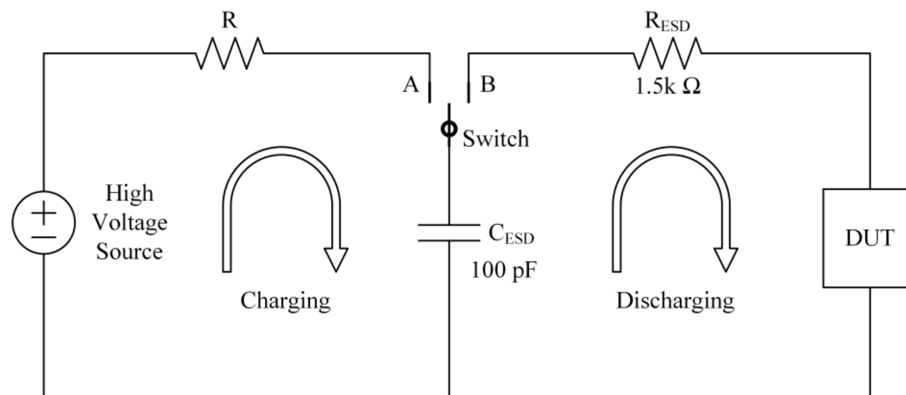

Figure 1-1 An equivalent circuit of HBM.

1.2.2 Machine Model

Machine model emulates that the machine or tool with static charge contacts the chip and forms a discharge path to the ground, resulting in ESD phenomenon. MM is equivalent to replacing the human body in HBM with a metal mechanical arm or tool in the production line. The equivalent circuit of MM is shown in Figure 1-2. C_{ESD} (200pF) represents the capacitance of machines. Because of the low-resistance discharge path (the metal mechanical arm or tool), there is no resistors in the right-hand side loop. The MM test method is the same with HBM. It is worth noting that according to the latest documents

of MM from JEDEC, MM has been discontinued across the industry and associations because it is superfluous to HBM [55].

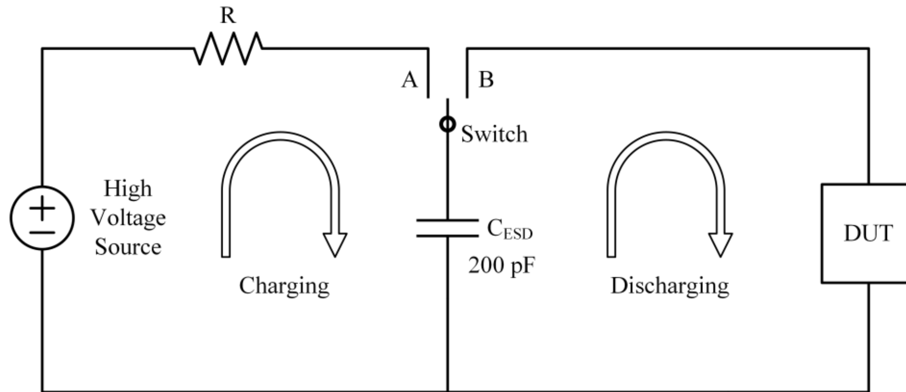

Figure 1-2 An equivalent circuit of MM.

1.2.3 Charged Device Model

Besides HBM and MM, there is another type of ESD model that is far more harmful than HBM and MM due to its self-discharge procedure, named charged device model. CDM defines a scenario where the IC is charged during fabrication, production or transportation, and the charge transfer takes place between the inside and the outside of the IC after the IC comes into contact with any conductors or grounded, as shown in Figure 1-3.

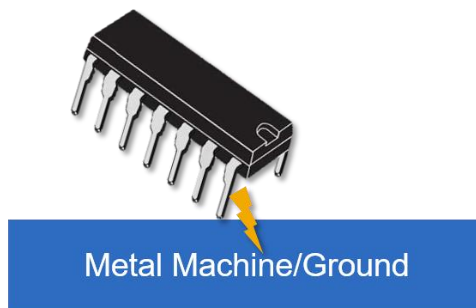

Figure 1-3 CDM Events.

The static charge inside the chip accumulates slowly, so it will not lead to any damage to the chip. However, due to the little parasitic impedance of the discharge path (including the resistance and inductance), the rise time and the duration is extremely short compared with HBM, and the discharge may generate CDM current up to tens of amperes. The equivalent circuit is shown in Figure 1-4. When the switch is closed at A, the high voltage power supply charges the equivalent capacitance C_{ESD} of the DUT to indicate that the chip carries static charge during production or transportation; when the switch is closed at B, the discharge circuit is turned on, indicating that the chip pin contacts ground or the conductors and the internal charge flows out. A CDM tester electrical schematic is shown in Figure 1-5. The parameters of DUT (R_{DUT}, C_{DUT}, and L_{DUT}) are related to the layout, die size, technology process, and package of the chip.

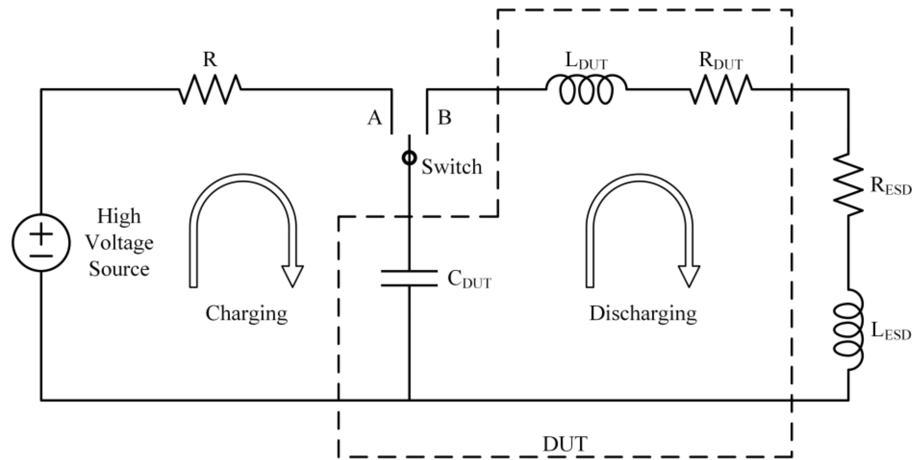

Figure 1-4 An equivalent circuit of CDM.

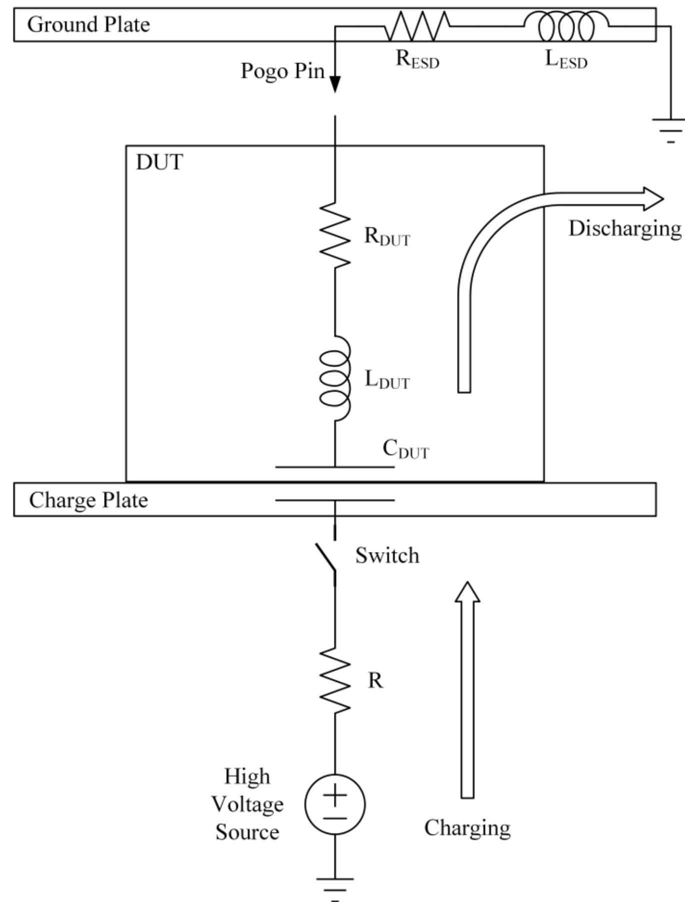

Figure 1-5 A simplified CDM tester electrical schematic.

1.3 ESD Protection Design Method

1.3.1 ESD Design Window

As for the principle of ESD protection design, firstly, the protection circuit should conduct ESD pulse quickly on the premise of keeping itself in good condition. Secondly, the protection circuit should remain off under normal circumstances. Thirdly, the designer should consider the discharge efficiency and the parasitic effect of the ESD protection structures.

Designers can determine the design window of ESD protection circuit (see Figure 1-6) according to the above ESD design principles and ESD protection levels [4]-[6]. There are 6 key parameters on the snapback curve: turn-on voltage V_{t1}, turn-on current I_{t1}, holding voltage V_h, holding current I_h, second breakdown voltage V_{t2} and second breakdown current I_{t2}. In the I-V graph shown in Figure 1-6, V_{t1} must be lower than the breakdown voltage of protected circuit and keep a safe margin. Similarly, V_h must be higher than the supply voltage and also keep a safe margin. I_h must be higher than the normal working current to prevent any latch-up effects. These key points in the I-V graph defines a fine area for ESD design window. The ESD design window shrinks as the integration process scales down to sub-32nm domains [7]-[8]. Therefore, the ESD simulation of CDM, especially the schematic-level simulation, becomes more crucial in the IC design.

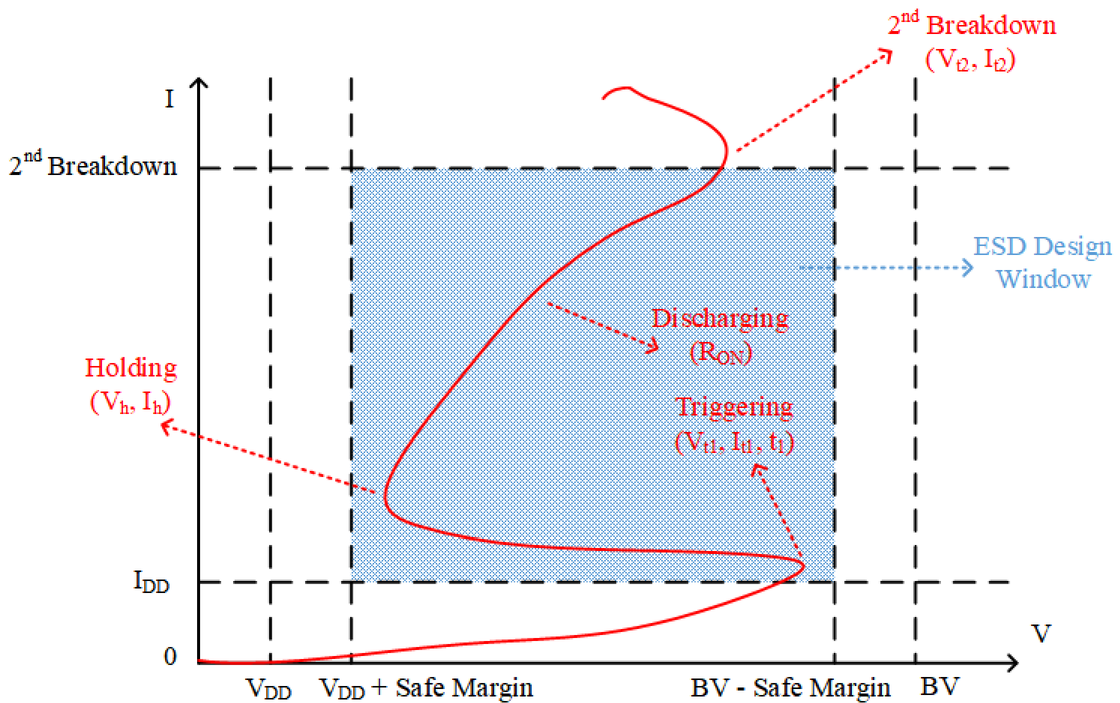

Figure 1-6 ESD design window and the snapback curve.

1.3.2 Full-Chip ESD Protection

A typical ESD protection schematic is shown in Figure 1-7 (a) [2]. At each I/O (input/output) pad, ESD protection structures in two directions (positive and negative) span between three nodes (VDD, I/O and VSS), guiding the ESD pulse from I/O pad to VDD or VSS node. ESD protection structures across V_{DD} node and V_{SS} node (aka power clamp) are to provide discharge paths between V_{DD} node and V_{SS} node directly. Multi-directional ESD protection structures can be used to save silicon area [2], as shown in Figure 1-7 (b).

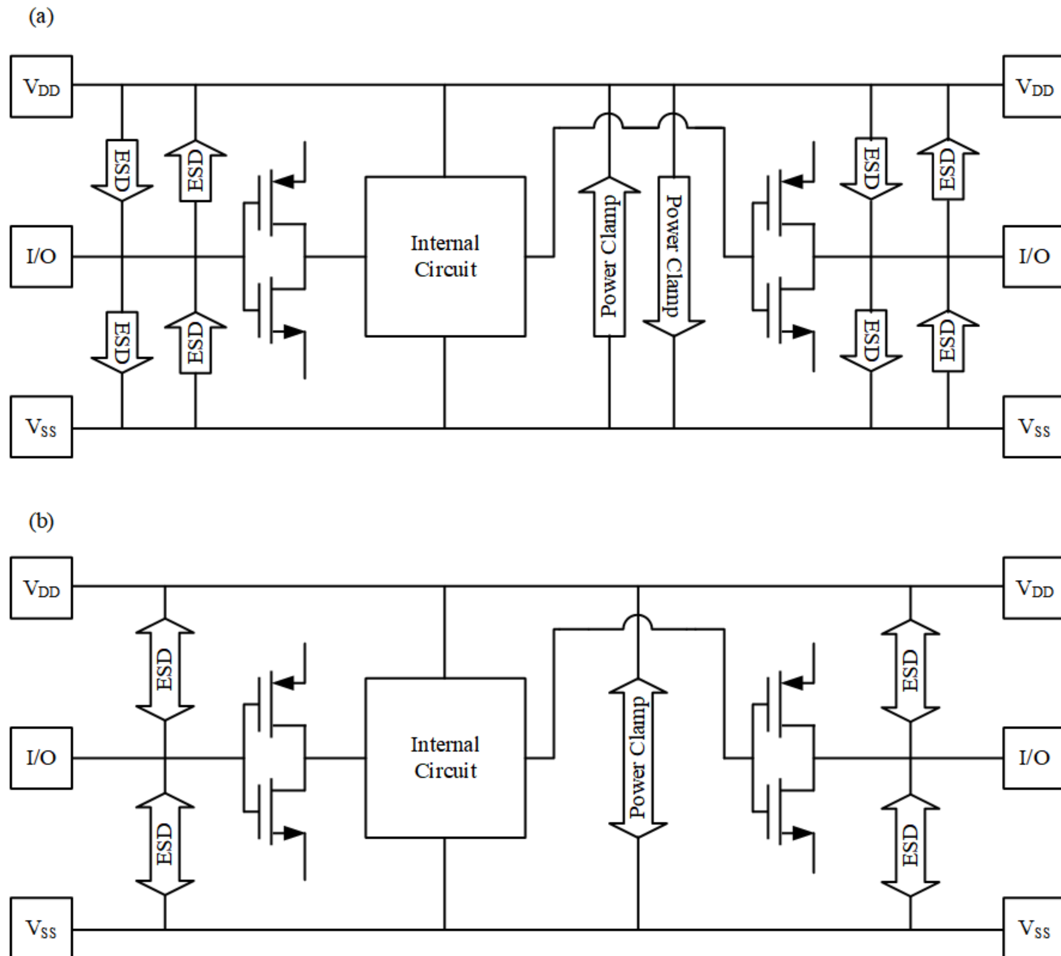

Figure 1-7 Typical ESD protection schematics with two I/O pads. (a) One-directional ESD protection structures (b) Multi-directional ESD protection structures

1.4 ESD Protection Structures

The key to ESD protection of ICs is ESD protection devices, including diodes, bipolar junction transistors (BJT), metal-oxide-semiconductor field effect transistors (MOSFET) and silicon-controlled rectifiers (SCR). Most of the protection modules are made up of one or two of these devices.

1.4.1 Diode

As the simplest ESD protection structure, junction diodes are widely used in various designs. A typical cross-section of diode is shown in Figure 1-8. Both the forward and reverse direction of the diode can be used to conduct ESD currents. As shown in Figure 1-9, a reverse diode (typically, Zener diode) and a forward diode string are used as protection structures. The reverse breakdown voltage of the diode is generally higher than the forward voltage-drop (typically, 0.7V), which means a higher turn-on voltage in reverse mode. Therefore, it is necessary to string multiple forward diodes together to ensure a proper turn-on voltage.

Every coin has two sides. Although the diode has advantages in the structure, its conduction capability of ESD pulse per unit area is not as much as other ESD protection structures. Moreover, the diode has a large leakage current compared to other ESD protection structures when the chip works normally, which results in the high-power consumption of the chip.

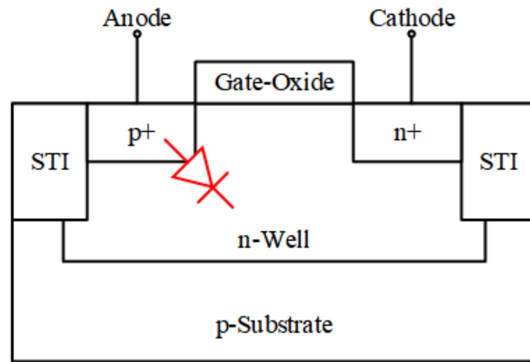

Figure 1-8 A typical cross-section of diode.

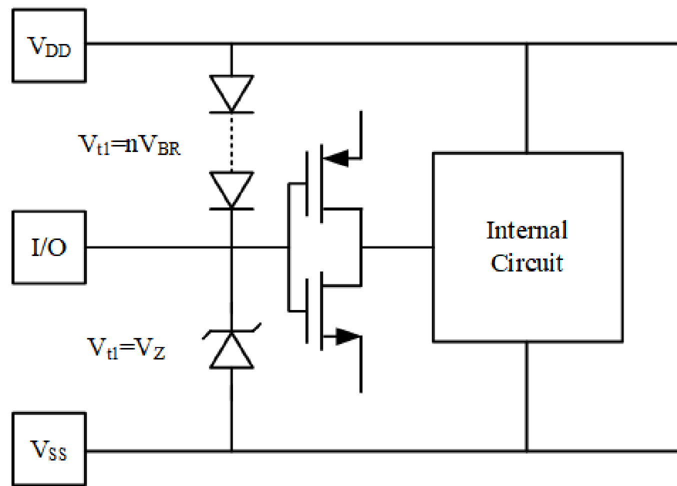

Figure 1-9 Diodes as ESD protection circuits.

1.4.2 BJT

Unlike diodes, BJT works in a snapback mode. As shown in Figure 1-10 and Figure 1-11, the base of BJT is connected to the emitter by a resistor. As for NPN BJTs, with the occurrence of ESD events, huge voltage causes avalanche breakdown to the collector-base (CB) junction of BJT. With the avalanche multiplication effect, a large number of electron-hole pairs generated at the CB junction. The electrons are pushed into the collector by the electric field of CB junction, and the holes are pulled into the base. Because of the

resistance at the base region, V_{BE} increases and the base-emitter (BE) junction is forward turned on. Then V_{CE} starts decrease rapidly, i.e. the snapback phenomenon.

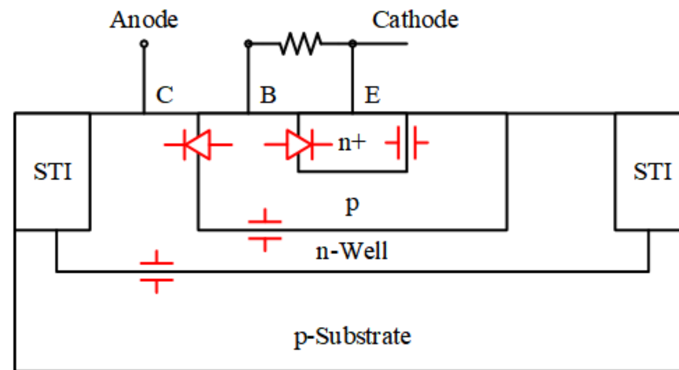

Figure 1-10 A typical cross-section of BJT.

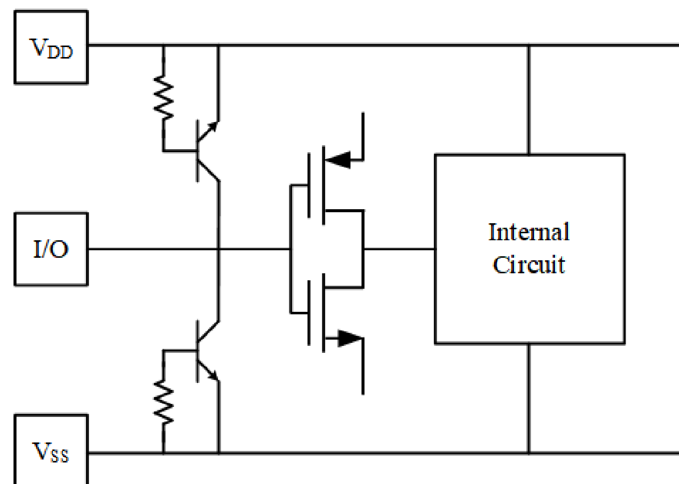

Figure 1-11 BJTs as ESD protection circuits.

1.4.3 MOSFET

The two most important devices in IC technology, PMOS and NMOS, are also useful in the ESD protection design, which means they are compatible with CMOS (complementary metal oxide semiconductor) technology. Grounded-gate NMOS (ggNMOS) and grounded-gate PMOS (ggPMOS) are both simple ESD protection structures. The drain is connected to the I/O pad and the gate and source are connected

together to the ground, as shown in Figure 1-12. The protection principle of ggMOS is pretty the same with BJT, because a parasitic BJT exists in every ggMOS. As mentioned earlier, the CB junction is reverse breakdown when ESD pulse appears at the I/O pad. Owing to the parasitic resistance in the substrate, V_{BE} of the parasitic BJT increases and then the BE junction turns on. Finally, V_{CE} (V_{DS}) drops quickly and protects the circuit.

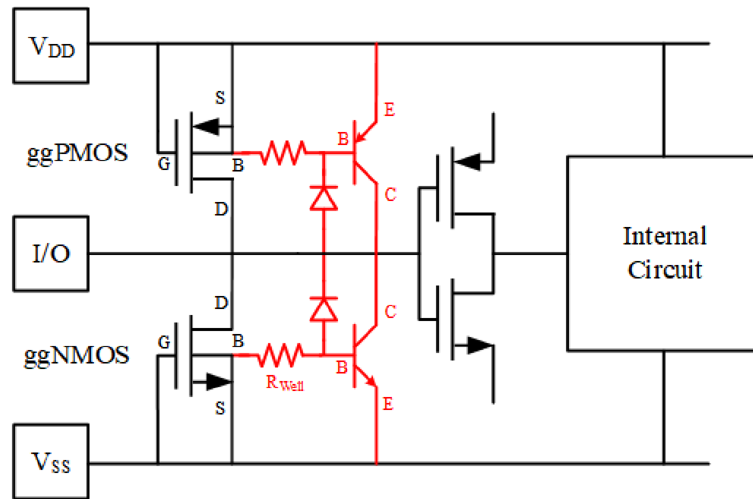

Figure 1-12 A typical ggMOS ESD protection circuit (black) and its equivalent circuit (red).

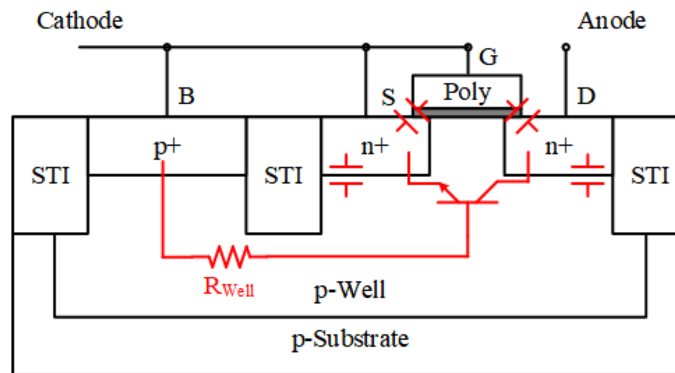

Figure 1-13 A typical cross-section of ggMOS.

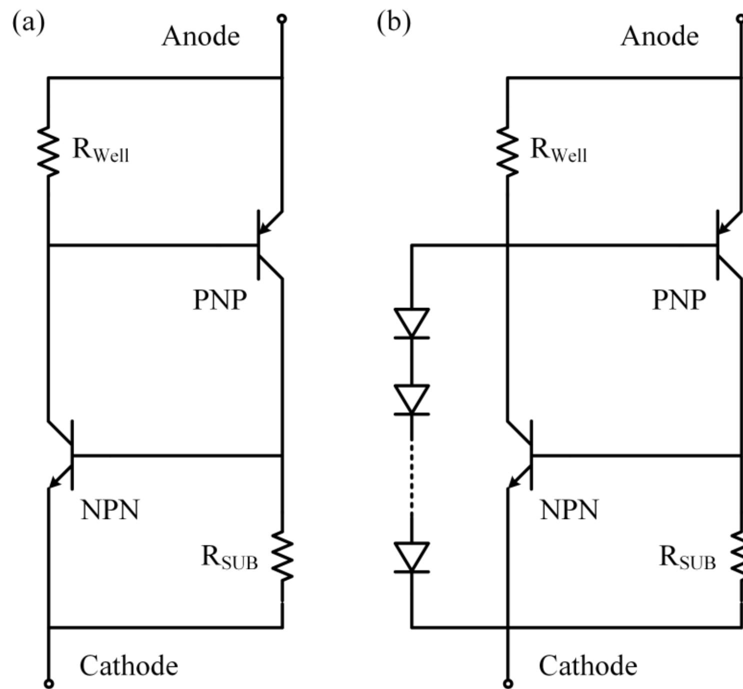

Figure 1-14 Schematic diagrams of (a) SCR structure and (b) DTSCR structure.

1.4.4 SCR

SCR is one of the ESD protection structures with the highest area utilization. It is a two-terminal device with a PNPN structure, as shown in Figure 1-14 (a) and Figure 1-15. SCR contains a lateral parasitic NPN BJT, a vertical parasitic PNP BJT and two parasitic resistors. As the ESD pulse appears at the anode of SCR, the CB junction of NPN is broken down, generating lots of electron-hole pairs. The collector current of NPN sets up the bias at the base of PNP by the parasitic resistor R_{Well} and turns the PNP on. Mutually, the NPN is turned on by the collector current of PNP.

Although SCR has its advantage in area utilization and conduction efficiency, the trigger voltage (V_{t1}) is relatively high. Diode-triggered SCR (DTSCR) can significantly

minimize V_{t1} by choosing the proper number of diodes in the string. A typical schematic diagram of DTSCR is shown in Figure 1-14 (b) [62].

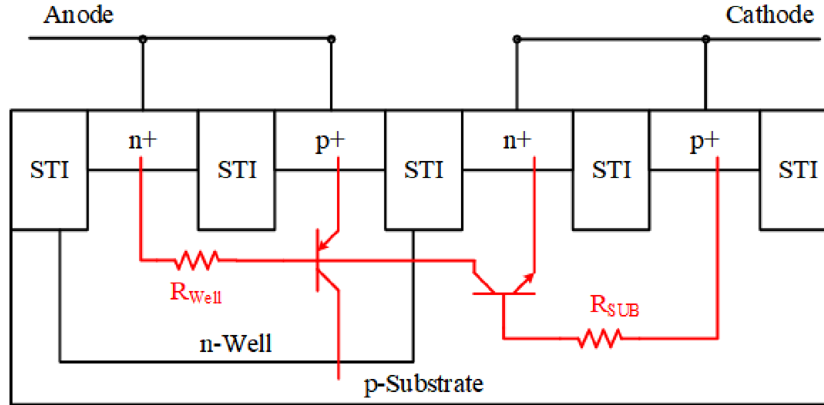

Figure 1-15 A typical cross-section of SCR.

1.5 CDM ESD Protection Design Challenges

In recent years, with the extensive use of automated machinery and equipment, CDM, as a potentially destructive discharge mechanism, has gradually become important. One of the most important characteristics of CDM is the low impedance discharge path, which leads to an extremely rapid charge transfer. During the CDM discharge, the rise time is very short (typically, 0.25-0.75ns) [56]-[57], which requires short trigger time of CDM ESD protection structures. Moreover, with the improvement of chip integration technology and the development of new packaging techniques, the equivalent parasitic capacitance of the chip increases, resulting in an increase in the amount of charge carried by the chip, and this requires an increase in the protection capability of CDM ESD protection structures. Therefore, it is necessary to pay increasingly attention to the CDM ESD protection.

1.6 ESD Simulation Methods

ESD simulation methods can be divided into two categories, TCAD (technology computer aided design) based simulation and SPICE (simulation program with integrated circuit emphasis) based simulation. TCAD calculates and predicts the electrical characteristics of devices with specific structure by solving the semiconductor physical equations such as Poisson's equation and continuity equation numerically. It is widely used in the simulation of ESD protection structures. SPICE calculates the input and output characteristics of the circuit using device behavior models and Kirchhoff's law.

Vast efforts have been made in ESD device models and ESD protection simulation methods [7]-[13]. A TCAD based mixed-mode ESD protection simulation-design methodology was developed, which allows IC designers to predict the ESD protection circuit performance at circuit-level [9]-[10]. However, this mixed-mode ESD protection circuit simulation is only suitable for ESD protection structures and small I/O blocks due to the limitation of TCAD tools. Several technology-independent CAD tools and algorithms were developed to perform whole-chip ESD protection design prediction and verification at layout level [11]-[13]. Recently, a novel chip-level ESD protection circuit simulation method for HBM using SPICE simulator and ESD behavior models was developed, which allows IC designers to conduct fast, accurate and transient schematic-level ESD protection simulation without being limited by the availability and accuracy of IC technology information, layout data and physics-based ESD device compact models [7]-[8].

As for the CDM ESD simulation, many studies were aimed at the simulation of ESD devices themselves (i.e. device-level) or small I/O blocks, while few focused on CDM ESD simulation at the chip-level. A compact electro-thermal device model used for simulating the operation of NMOS devices in the snapback regime is presented in [68]. An enhanced compact modeling of CMOS I/O circuit is presented in [69], which allows the simulation of complete CMOS I/O circuit response. More literature on circuit-level CDM ESD simulation will be discussed in the first section of Chapter 2.

1.7 Thesis Organization

This thesis is organized as follows. First of all, the basic concepts of ESD event and ESD protection are introduced in Chapter 1. In Chapter 2, the design motivation and the CDM discharge model including the CDM charge storage model and the CDM discharge path model at schematic-level are described. In Chapter 3, the simulation technique of the CDM ESD model using Cadence Virtuoso is described in this chapter. Moreover, the CDM modeling method and ESD simulation technique are applied to a pseudorandom binary sequence generator circuit. The conclusion and future work are discussed in Chapter 4.

Chapter 2   Circuit-Level CDM Simulation Modeling

2.1 Backgrounds, Problems and Motivation

With the popularization of automated equipment in the chip industry chain, more machines are used in chip manufacturing, packaging, testing, storage and transportation. According to statistics, more than 30% of chip failures are caused by ESD/EOS [1], and the proportion of chip failures caused by CDM is gradually increasing over the years. As mentioned earlier, as the semiconductor process shrinks to sub-32nm regions, the CMOS gate oxide becomes thinner and the junction becomes shallower, making ICs more susceptible to CDM ESD failures [1]-[5]. Meanwhile, the higher speed and the lower operating voltage of ICs also make the ESD design window narrower.

On the other hand, people do not have a thorough understanding of the mechanism of CDM failures, and experience is still important for ESD protection design. In the non-ESD protection circuit design, designers can rely on simulators such as SPICE for pre-layout and pre-silicon (post-layout) verification. However, as for the ESD protection design for ICs, few pre-layout or pre-silicon verification methods can be adopted.

At present, the mainstream ESD protection design method is that the foundry provides various ESD protection structures in the PDK (process design kit) for IC designers. These ESD protection structures are taped out, characterized and verified by the foundry. However, these ESD protection structures in the PDK do not always meet the IC designers'

expectations. If the ESD device cannot provide enough protection, the ESD failures may occur. On the contrary, if the ESD device provides over protection, it is a waste of the die area. These problems can only be discovered after taping out, which causes a great waste. Therefore, pre-layout simulation and pre-silicon simulations are very important for ESD protection designs. Some efforts that have been done on circuit-level CDM ESD simulations are summarized below.

A CDM behavior simulation methodology with CDM macromodel at chip-level is presented in [43]-[44]. The workflow for CDM analysis is as follows: physical layout database, RC extraction, CDM macromodel, hierarchical chip-level modeling and netlist generation. After finishing the chip layout, a distributed network analyzer and a layout extractor are used for RC extraction. The R is distributed on all the conduction parts of the chip, and the C which act as CDM source consists of the package capacitance between V_{DD} and V_{SS} conductive planes and the off-chip ground, the junction capacitance, the oxide capacitance, the metal-metal capacitance and the substrate decoupling capacitance. The CDM macromodels are divided by the chip floorplan, functionality and power bus architecture. Then a hierarchical analyzing method is performed in each CDM subsystem. Finally, the netlist is generated and the CDM behavior of the chip is simulated. This simulation methodology assumes that the charge that contributes to CDM events is mainly stored in the capacitance between V_{DD} planes and the off-chip ground, and the capacitance between V_{SS} planes and the ground, which is not consistent to the today's cognition (on-die CDM charge is stored in the substrate). In addition, only the active devices at I/O buffer of the subsystems are considered in this simulation methodology, while many active

devices in the core-circuit which are also vulnerable to CDM events are not taken into account. Besides, this is a post-layout CDM behavior simulation methodology as it requires the layout data.

A 3-D circuit model used for evaluating CDM performance of ICs is presented in [45]-[48]. The circuit model is divided into three parts: IC package, substrate resistance and capacitance, protection devices and circuit elements. The capacitance, inductance and resistance of the package are derived from measured S-parameters. Assuming the CDM charge is stored at the bottom of the substrate, the die substrate is divided into smaller unit volumes with 3-D resistive networks. A distributed small capacitor is connected to the bottom of each small unit volume. ESD protection devices are modeled by their compact circuit models. Furthermore, the active devices such as MOSFESTs and BJTs are replaced by PN junctions and capacitors with the assumption that the IC is not powered up during CDM events. Power lines as circuit elements are also considered in this model. The assumption that CDM charge is distributed at the bottom of the die substrate is not quite consistent with the real world cases since Coulomb repulsion can spread the charge. In addition, some active devices may be powered up by the CDM ESD pulse though the entire IC is powered off, therefore, the active devices should not be replaced by PN junctions and capacitors directly. Similar to the method described in the last paragraph, this is also a post-layout simulation.

The effect of package, substrate resistivity, decoupling capacitance and location of ESD protection circuits to the CDM events are studied in [49]-[50], meanwhile, an internal I/O model which can be used for CDM simulation is presented. This CDM model consists

of a package capacitance and inductance model, a substrate resistance model and a cross-domain I/O model. The parasitic parameters of the package can be calculated or estimated according to the data sheets. The substrate model is a 3-D resistance grid mesh with CDM charge storage capacitance at the bottom of the substrate, which is the same as the 3-D resistive network in [45]-[48]. The cross-domain I/O model focuses on the I/O buffers, ESD power clamps, and the power bus resistance and capacitance extracted from the layout. Thus, this model do not consider the internal circuits (i.e. the core circuit inside the power domain) that may affect the CDM behavior of the chip.

Recently, a methodology to construct equivalent circuit models for packaged IC on CDM testers is presented in [51]-[52]. This full-component model consists of a CDM tester model, a package interconnect model, a pad-ring model, a core power distribution network model, a die substrate model, an on-die decoupling capacitance model and a tester-die coupling model. This CDM simulation methodology takes all necessary parasitic components into account and is useful to identify the vulnerable location of ICs after finishing the layout.

These state-of-the-art methodologies are all for post-layout CDM simulations, however, the need for pre-layout simulation does exist. For example, circuit designers may optimize the circuit topology to enhance the CDM protection level of the circuit itself when they know the vulnerable parts by doing pre-layout CDM ESD simulations. Moreover, ESD engineers and layout engineers can pay more attention to the vulnerable parts of the circuit if they know where the vulnerable circuit is. Pre-layout CDM ESD simulations can greatly improve the ESD design efficiency of ICs, just like the SPICE simulation for the

circuit design. In a word, this work aims to improve the design efficiency and reliability of CDM ESD protection by realizing the pre-layout circuit-level CDM ESD simulation.

2.2 Circuit-Level CDM Simulation Modeling

The CDM discharging model describes the entire process of CDM events. In order to illustrate this model, in principle, we can clearly divide the model into two phases: charging (static charge generation and storage) and discharging (when an IC is grounded). In the following sections, this new CDM ESD charge storage model (Section 2.3) and the discharging model (Section 2.4-2.7) for pre-layout circuit-level CDM ESD protection simulation will be stated in detail.

2.3 CDM Charge Storage Model – Substrate Capacitance

2.3.1 CDM Tester Discharge Procedure

Before describing the CDM charge storage model, it is necessary to review the field-induced CDM tester discharge procedure in the CDM standard. The diagrammatic drawing of this discharge procedure is shown in Figure 2-1. In this example, DUT is a bare die, i.e. silicon substrate. The charge distribution in the charged extrinsic semiconductors is briefly described as below. As we know, although the band structure of a semiconductor is similar to that of an insulator (conduction band, valence band and band gap), its band gap is much narrower than that of an insulator. Electrons and holes can move freely in the semiconductor due to doping and their average drift velocity in the electric field are

$$v_{hole} = \mu_p \mathbf{E} = \frac{q\bar{\tau}}{m_p^*} \mathbf{E} \tag{2.1}$$

$$v_{electron} = -\mu_n \mathbf{E} = -\frac{q\bar{\tau}}{m_n^*}\mathbf{E} \tag{2.2}$$

where μ is the average drift mobility of electrons/holes, m^* is the effective mass of electrons/holes, $\bar{\tau}$ is the average scattering time, q is the elementary charge, and $\mathbf{E}$ is the electric field.

To be more specific, the electron or hole can be transferred to a new energy state by the electric field when there is an empty energy level near the level of this electron or hole, which is called conduction. The distribution of charge (electrons and holes) in electrostatic equilibrium is shown in Figure 2-1. Similar to a charged metal conductor, the net charge of a charged semiconductor distributes on the surface.

Conductors near the IC may affect the net charge distribution within the IC. When a charged device (A) approaches to a grounded conductor (B), the side of B near A will induce charge which is opposite to the net charge on A by the electric field of A. The charge induced on B generates a new electric field, which will affect the charge distribution of A at the same time. Then the charge on A redistributes and affects the charge on B again. Finally, the charge on A and B reaches an electrostatic equilibrium state. Therefore, considering that when a CDM event occur, the IC may be grounded at any angle, and its internal net charge distribution will be affected. COMSOL Multiphysics simulation results show three different cases of positions of the DUT and the grounded conductors, which reflect three different charge distributions on the DUT.

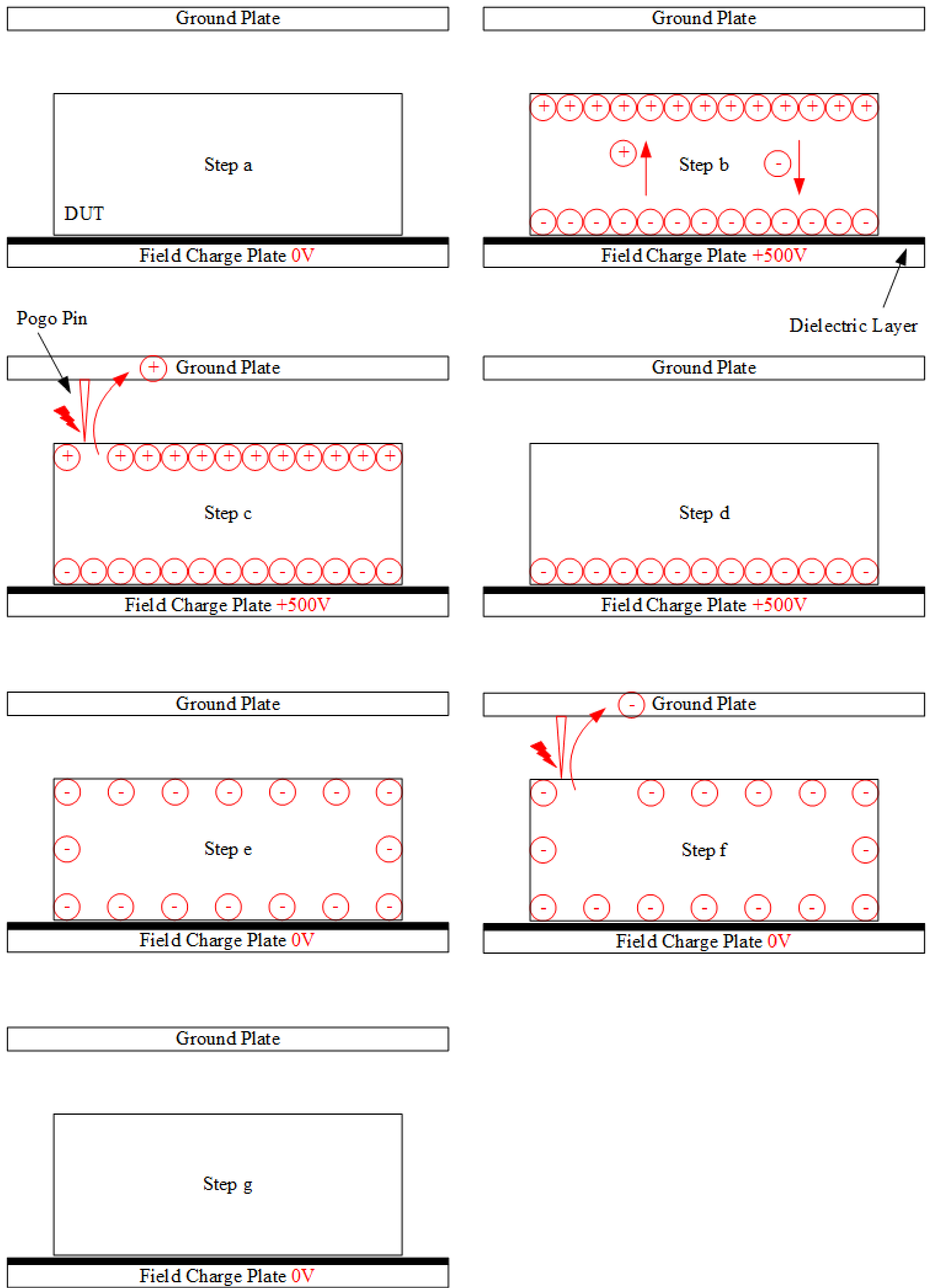

Figure 2-1 Dual Discharge Procedure.

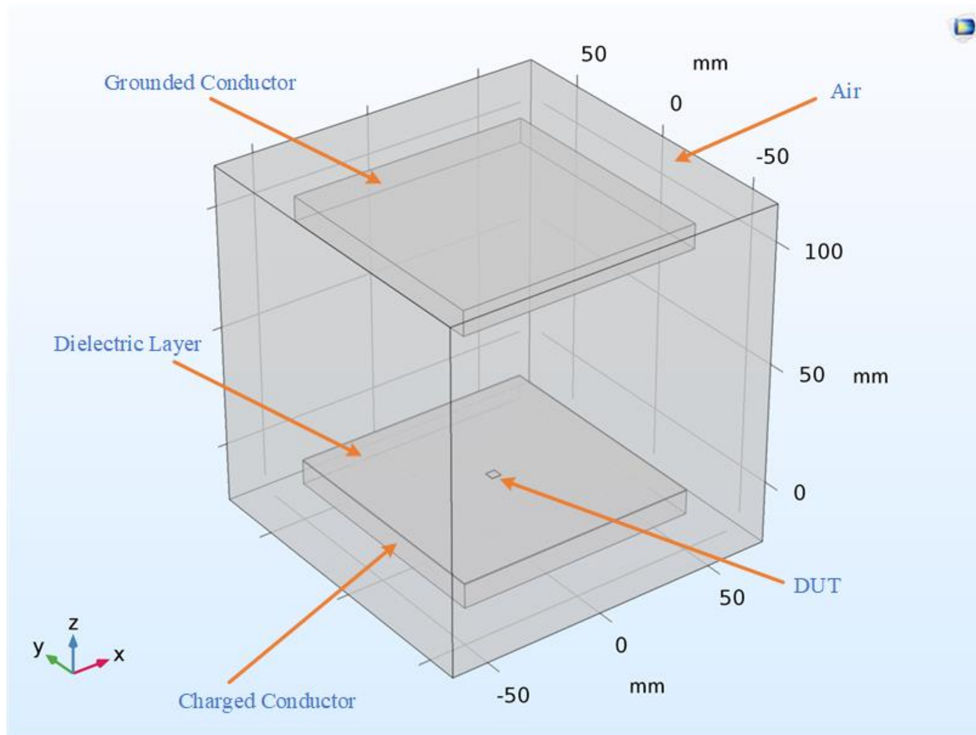

Figure 2-2 Case 1: DUT between two plate conductors.

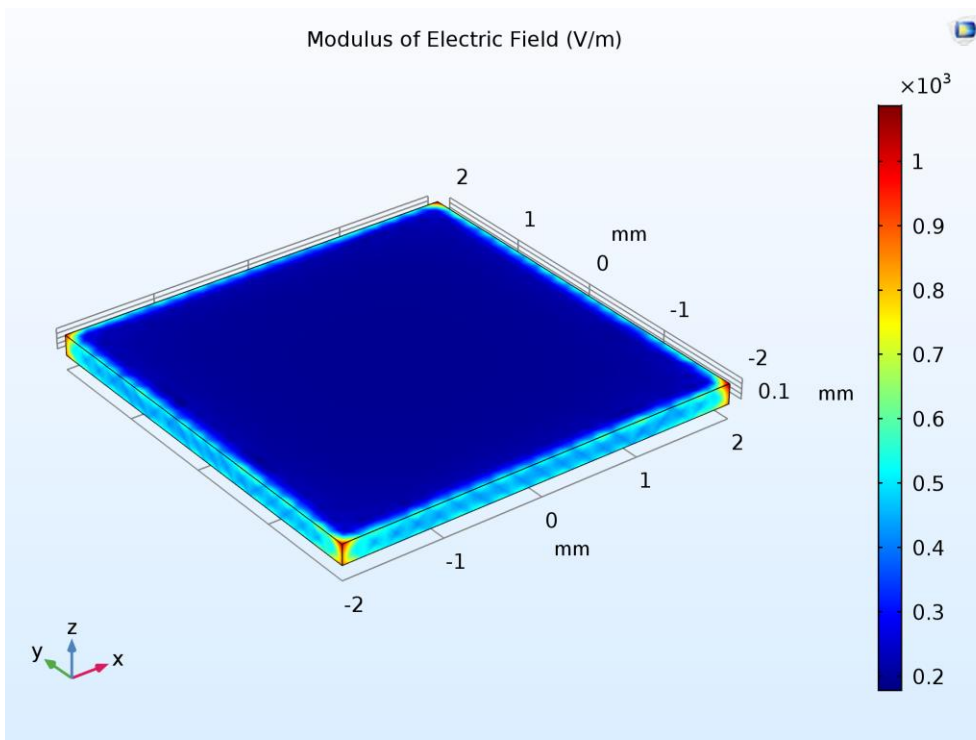

Figure 2-3 Charge distribution of DUT in Case 1.

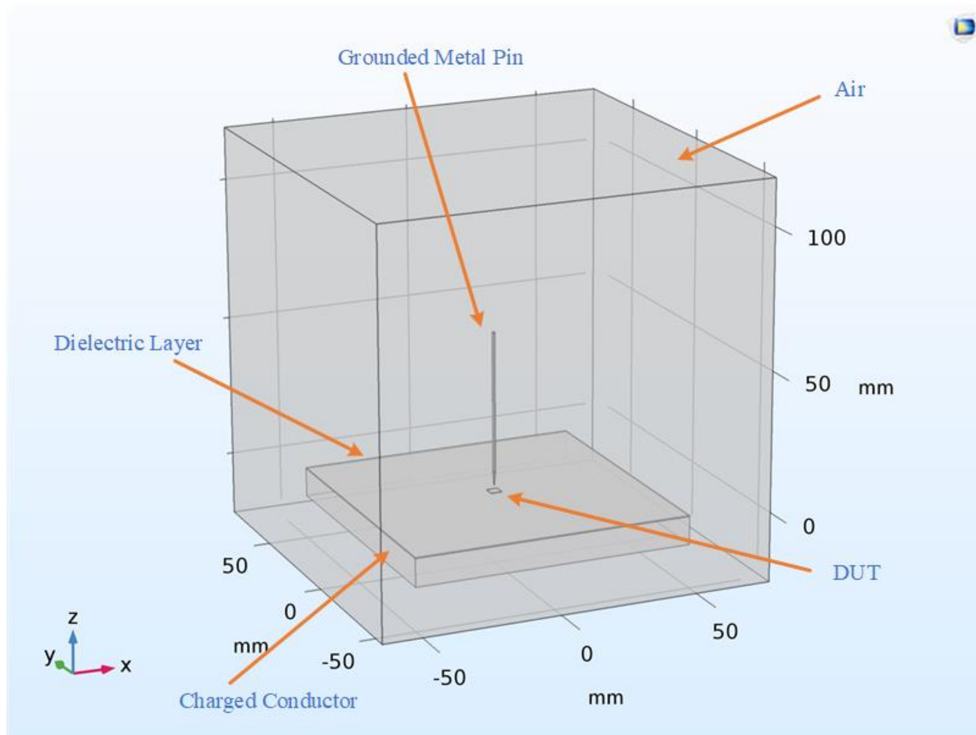

Figure 2-4 Case 2: DUT under a vertical grounded pin.

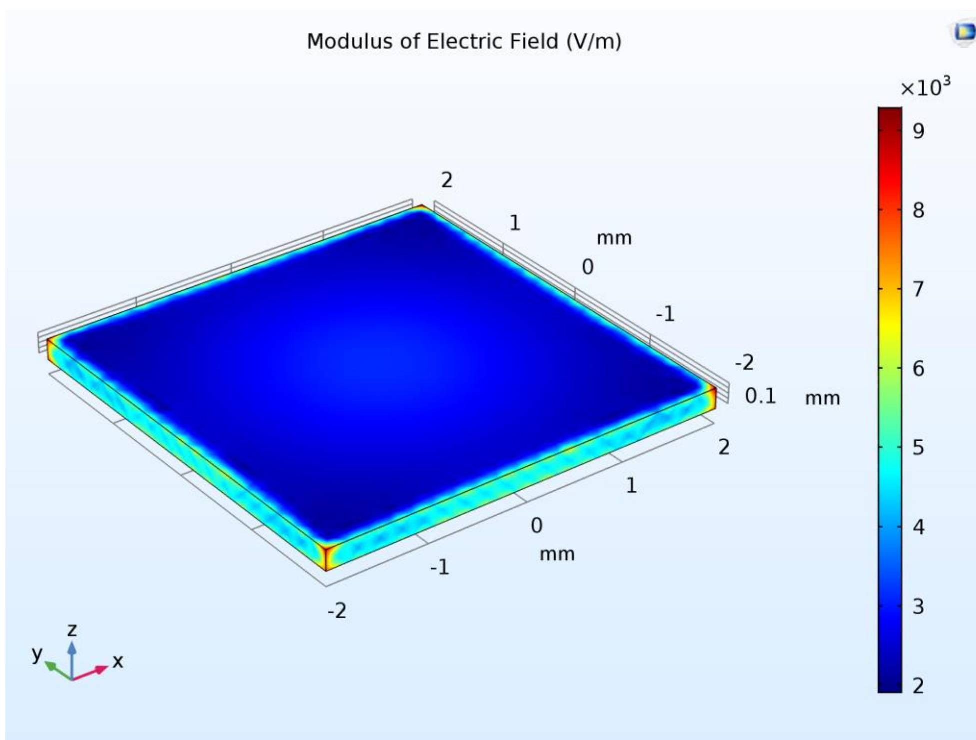

Figure 2-5 Charge distribution of DUT in Case 2.

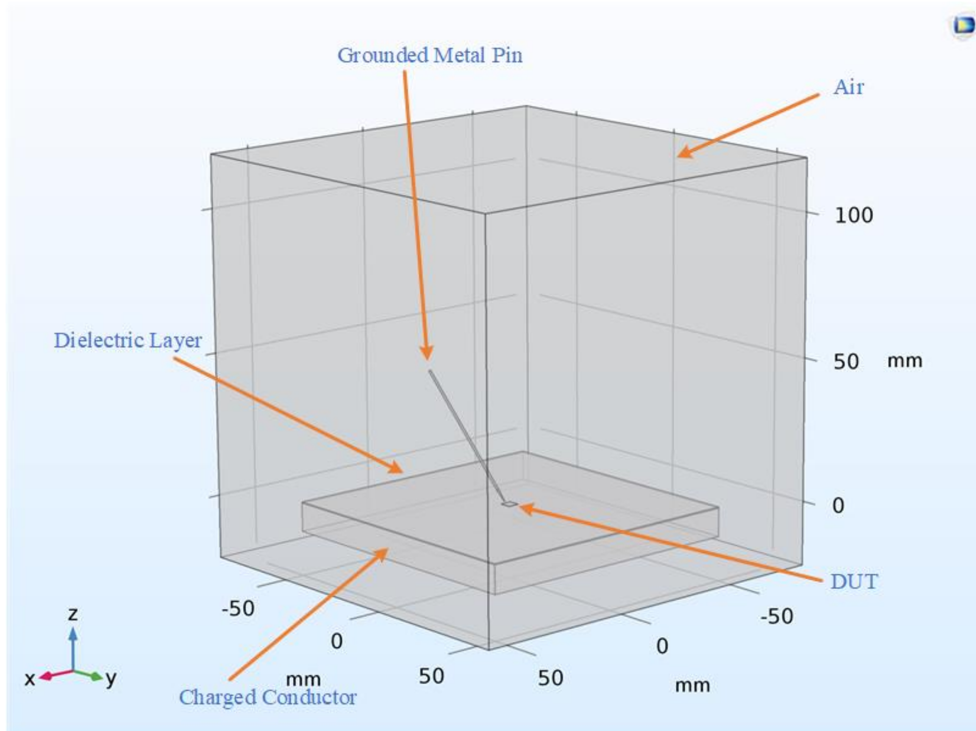

Figure 2-6 Case 3: DUT under a diagonal grounded pin.

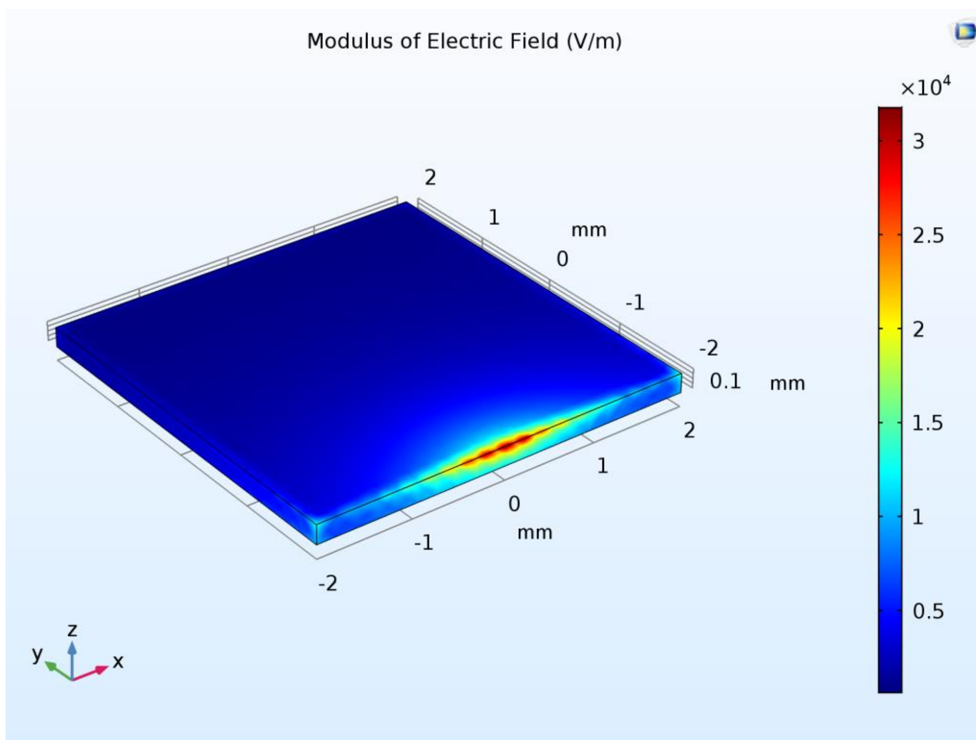

Figure 2-7 Charge distribution of DUT in Case 3.

The relationship between the charge density and the electric field is

$$\mathrm{div}\,\mathbf{E} = \frac{\sigma}{\varepsilon_0 \varepsilon_r} \tag{2.3}$$

where div **E** is the divergence of the electric field, σ is the volume charge density, and $\varepsilon_0 \varepsilon_r$ is the permittivity. The charge distribution varies with the external conductors (i.e. external electric field), as shown from Figure 2-2 to Figure 2-7. In addition to the external electric field, metal in the package may also change the charge distribution inside the IC, for example, heat sink, lead frame and bond wire.

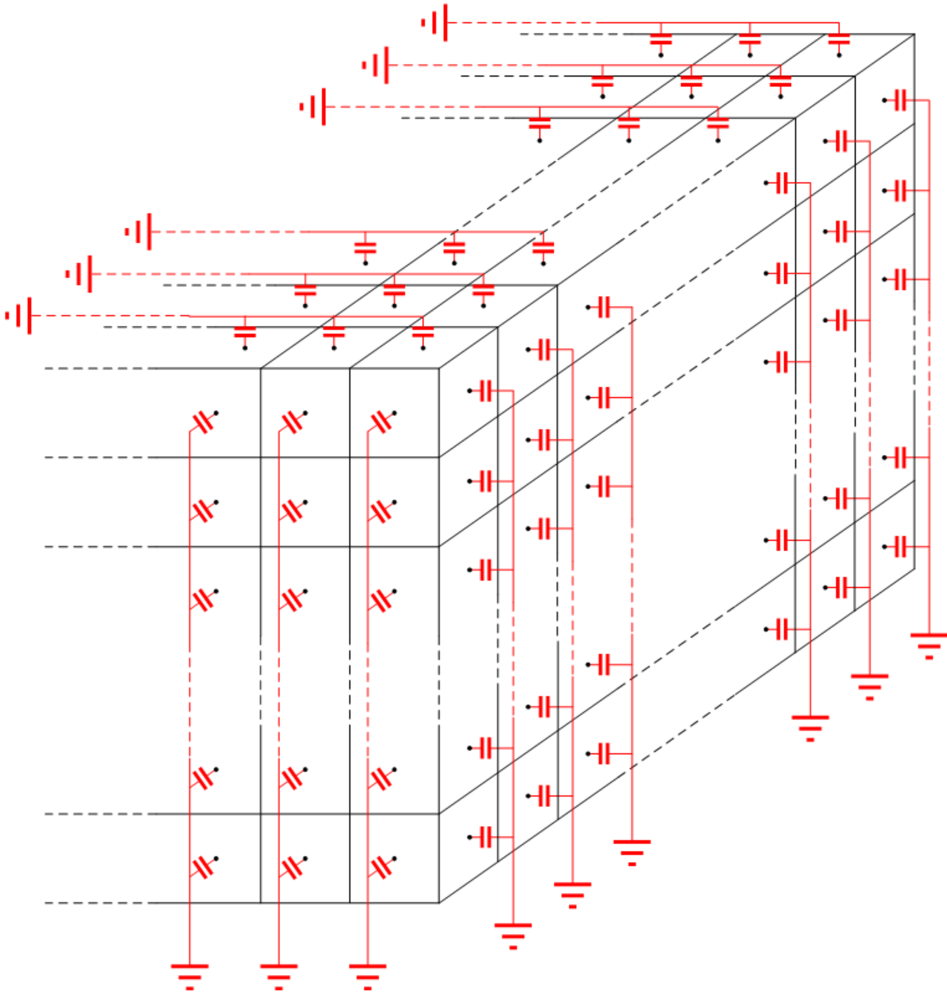

Figure 2-8 CDM charge storage model.

2.3.2 Substrate Capacitance Model

In order to propose a general model which is applicable to any scenarios to help circuit designers to explore vulnerable circuit topologies before doing layout and selecting package, this CDM charge storage model ignores the external electric field of the bare die. In this CDM charge storage model, charge is stored in the capacitors on the surface of the IC die. In order to simplify the model and simulation, the capacitance is evenly distributed on the surface, ignoring the tip effect (charge collects at the tip) on the apex of the silicon substrate, as illustrated in Figure 2-8.

Considering that the active Si layer containing IC devices is much thinner than the Si substrate (e.g., ~2μm *vs.* ~250μm) and to make the charge storage model simple, we can ignore the effect of the active layer on the static charge distribution. As for the value of these capacitors, we apply a capacitance formula based on first-order correction for the fringing to calculate the total capacitance [64].

$$C_{total} \approx \varepsilon \frac{(W+2d)(L+2d)}{d} \approx \varepsilon \left[\frac{WL}{d} + 2(W+L)\right] \tag{2.4}$$

where W and L are the width and length of the IC die, respectively, d is the distance between the IC and the field charge plate, and ε is the permittivity. The dielectric layer is made with FR4 ($\varepsilon_r \approx 4.5$) or similar epoxy-glass material, and its thickness is 0.381mm.

Table 2-1 on the next page shows the comparison between theoretical calculation and simulation of the total capacitance, and their relative errors. The total capacitance formula can meet the requirements of theoretical calculation with a small relative error in common dimensions. The value of each capacitor is given by

$$C_{sub} = \frac{C_{total}}{N} \quad (2.5)$$

where N is the number of capacitors on the surface.

In brief, the CDM charge storage model is represented by a great many of capacitors distributed on the surface of the silicon substrate. The total capacitance formed by metal-insulator-semiconductor is calculated using Equation (2.4) and Equation (2.5).

Table 2-1 Theoretical calculation, simulation, and relative errors of the total capacitance.

IC Die Dimensions (mm)			Capacitance (pF)		Relative Errors (%)
Width	Length	Thickness	Calculation	Simulation	
40	40	0.2	173.6984886	173.29	0.235725412
20	20	0.2	45.01837814	44.668	0.78440526
10	10	0.2	12.05147254	11.915	1.145384267
5	5	0.2	3.411307134	3.294	3.561236608
2	2	0.2	0.737059861	0.6988	5.47508034
1	1	0.2	0.263952765	0.28332	6.835816266
0.5	0.5	0.2	0.105832091	0.09824	7.728106004
0.2	0.2	0.2	0.036058207	0.040221	10.34980082
0.1	0.1	0.2	0.016983332	0.019672	13.66748854
0.05	0.05	0.2	0.008230223	0.010644	22.67734955
40	40	0.24	173.6984886	173.4	0.172138735
20	20	0.24	45.01837814	44.711	0.687477672
10	10	0.24	12.05147254	11.918	1.119923942
5	5	0.24	3.411307134	3.2948	3.53609123
2	2	0.24	0.737059861	0.70666	4.301907766
1	1	0.24	0.263952765	0.24963	5.737597786
0.5	0.5	0.24	0.105832091	0.10084	4.950507079
0.2	0.2	0.24	0.036058207	0.038663	6.737173488
0.1	0.1	0.24	0.016983332	0.028824	8.897702538
0.05	0.05	0.24	0.008230223	0.020031	15.21475886
1	1	0.5	0.263952765	0.26785	1.455006401
1	1	0.4	0.263952765	0.25952	1.708063099
1	1	0.3	0.263952765	0.25359	4.086425078
1	1	0.25	0.263952765	0.24963	5.737597786
1	1	0.2	0.263952765	0.23732	11.22230126
1	1	0.1	0.263952765	0.22792	15.80939161

2.4 CDM Discharge Model – Substrate Resistance

After the charge is released from the surface capacitance of the substrate, it enters the resistance mesh grid inside the substrate. A general 3-D grid mesh is shown in Figure 2-8. Each substrate grid cuboid is connected to 6 resistors of its neighboring cuboids as shown in Figure 2-9. For the size of each cuboid, we adopt an optimization method based on root-mean-square (RMS) to balance the variation (accuracy) and the computational cost (efficiency) of the simulation, which is proposed in [51]. The variation of one node in a K-layer ($k = 2, 3, \dots, K$) substrate is given by

$$V(K) = \frac{\sqrt{\frac{1}{N}\sum_{t_n}[V_K(t_n) - V_{K-1}(t_n)]^2}}{\sqrt{\frac{1}{N}\sum_{t_n}[V_{K-1}(t_n)]^2}} \tag{2.6}$$

where t_n is the simulation time ($n = 0, 1, 2, \dots, N-1$), and $V(K)$ is calculated for all nodes in the substrate, then the variation of the K-layer substrate is Max[$V(K)$]. As the number of layers increases, the variation gradually decreases. The computational cost is given by

$$C(K) = \frac{simulation\ time\ of\ K\ layers}{simulation\ time\ of\ 2\ layers} \tag{2.7}$$

Unlike the model in [51], all of the non-linear devices in the schematic are retained in this CDM discharging model, so the number of layers in the X, Y, and Z directions need to be optimized by calculating the variation and the computational cost. For the x-axis and y-axis that $i = 2, 3, \dots, I$ and $j = 2, 3, \dots, J$, we have

$$V(I) = \frac{\sqrt{\frac{1}{N}\sum_{t_n}[V_I(t_n) - V_{I-1}(t_n)]^2}}{\sqrt{\frac{1}{N}\sum_{t_n}[V_{I-1}(t_n)]^2}} \tag{2.8}$$

$$V(J) = \frac{\sqrt{\frac{1}{N}\sum_{t_n}[V_J(t_n) - V_{J-1}(t_n)]^2}}{\sqrt{\frac{1}{N}\sum_{t_n}\left[V_{Y_{J-1}}(t_n)\right]^2}} \tag{2.9}$$

$$C(I) = \frac{simulation\ time\ of\ I\ layers}{simulation\ time\ of\ 2\ layers} \tag{2.10}$$

$$C(J) = \frac{simulation\ time\ of\ J\ layers}{simulation\ time\ of\ 2\ layers} \tag{2.11}$$

To minimize the variation and the cost, a judging method is defined as Equation (2.12) to show the best tradeoff of both the variation and the computational cost.

$$W = \frac{1}{\text{Max}[V] \cdot C} \tag{2.12}$$

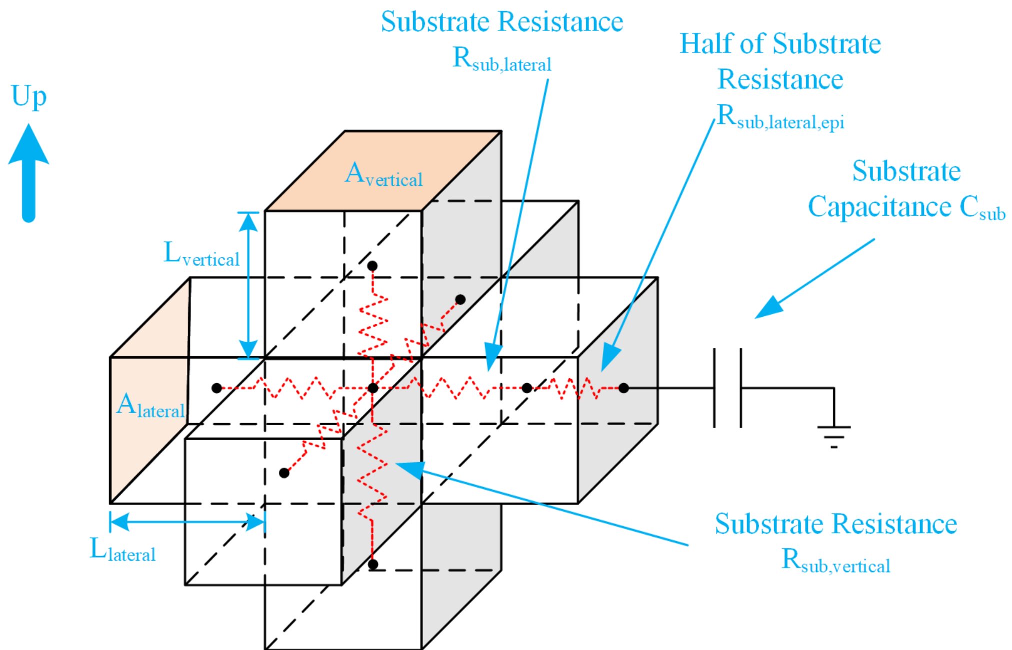

Figure 2-9 Substrate grid cuboid with 6 resistors connected to its adjacent cuboids.

The doping concentration and mobility can be found in the PDK provided by the foundry. Using these parameters, we can calculate the conductivity by

$$\sigma = \frac{1}{\rho} = q\left(n \cdot \mu_n + p \cdot \mu_p\right) \tag{2.13}$$

where ρ is the resistivity, q is the elementary charge, n and p are the concentrations of electrons and holes, respectively, and μ is the mobility of carriers. The resistance R_{sub} is

$$R_{sub} = \frac{\rho \cdot L}{A} \tag{2.14}$$

where L is the thickness, A is the cross-section area.

2.5 CDM Discharge Model – Core Circuit

2.5.1 ESD Parasitic Components

In essence, PN junctions are the elements of ICs. As mentioned earlier, when CDM discharging occurs, the electric charge gushes out from the substrate and leave the die via pads. In order to combine the ESD events with SPICE simulation to simulate the reaction of each functional component in the core circuit when ESD event occurs, the functional components in the core circuit are presented with their ESD parasitic components. Diodes and series resistors are added to the MOSFETs as the CDM discharging paths in the schematic, as shown in Figure 2-10. Similarly, diodes and resistors connected with the substrate resistance mesh grid are added to diodes, BJTs, resistors, and capacitors in the core circuit, and examples are shown from Figure 2-11 to Figure 2-14. It is worth noting that the ESD parasitic model of the diode does not contain the intrinsic diode that has already exist in the schematic.

The added ESD parasitic diodes are BSIM models from the PDK, which contain the parameters corresponding to the technology and will behave appropriately as PN junctions in the functional components when an ESD event occurs. For example, the PN junction capacitance is included in the diode BSIM models. The reason which functional components in the core circuit are not directly replaced with the parasitic components is that functional components may affect the ESD discharge. For example, MOSFETs in the output buffer with self-protection effect affect the ESD discharging behavior. If these MOEFESTs are replaced with ESD parasitic components, the self-protection effect will not be reflected in the ESD simulation.

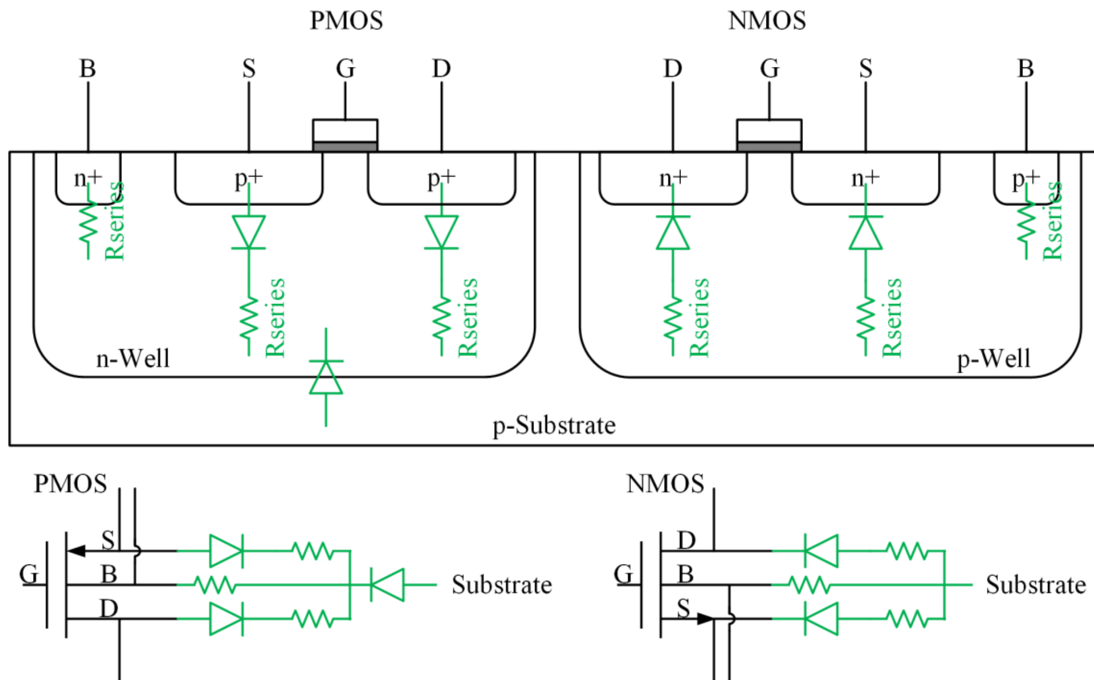

Figure 2-10 ESD parasitic components of MOSFETs in the cross section and the schematic.

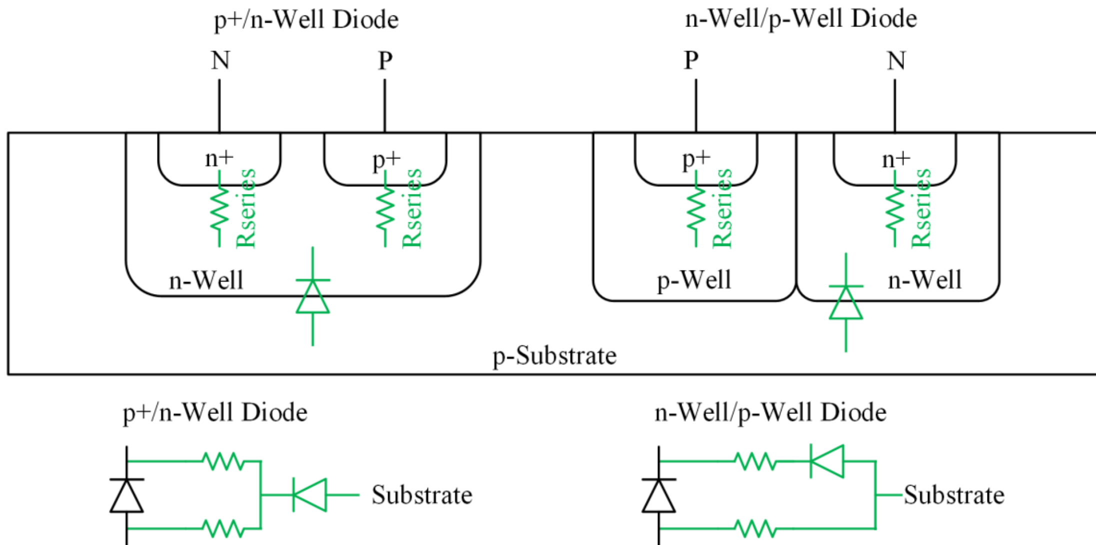

Figure 2-11 ESD parasitic components of Diodes in the cross section and the schematic.

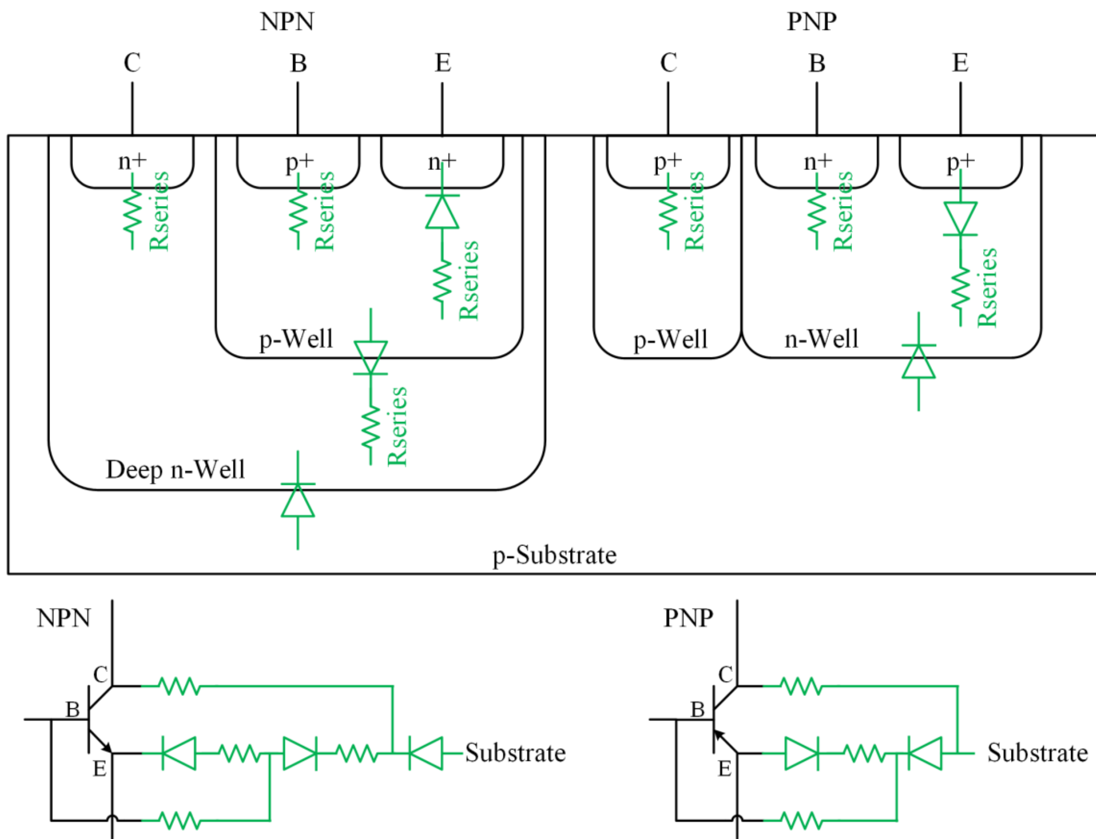

Figure 2-12 ESD parasitic components of BJTs in the cross section and the schematic.

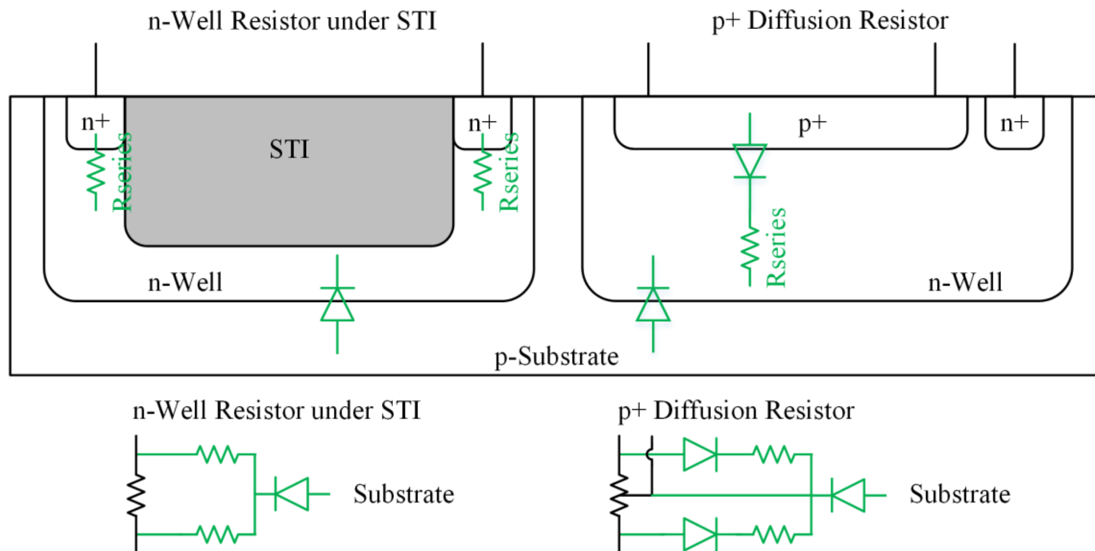

Figure 2-13 ESD parasitic components of resistors in the cross section and the schematic.

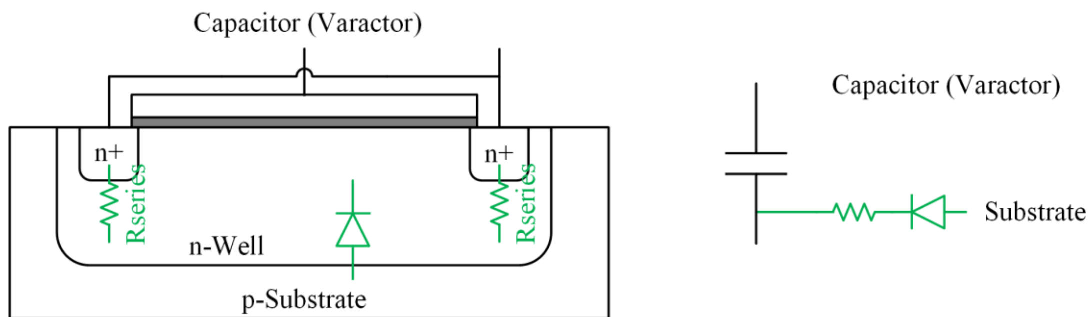

Figure 2-14 ESD parasitic components of capacitors in the cross section and the schematic.

2.5.2 Calculation of ESD Parasitic Components

The calculation method of ESD parasitic diode area is briefly described as follows. Taking the MOSFET as an example, the gate length and width of the MOSFET are clearly defined in the schematic, and the gate width is exactly the width of the source or drain, i.e. ESD parasitic diode. As for the length of the diode, for example, MOSFETs are automatically generated in batches by Electronic Design Automation (EDA) software following the design rules in the layout. Thus, the length of the diode can be obtained by analyzing the design rules. However, the device sizes may vary in analog circuits, so circuit

designers need to manually adjust the area of ESD parasitic diodes according to the area of the source or drain.

To concretely show the method for determining the parameters of ESD parasitic components, an example of calculating the ESD parasitic diode area of MOSFETs in a 28nm CMOS technology is given as follows. For MOSFETs with odd fingers,

$$A_{diode,source} = A_{diode,drain} = x_1 \times W_{finger} + x_2 \times \frac{N-1}{2} \times W_{finger} \quad (2.15)$$

For MOSFETs with even fingers,

$$A_{diode,source} = x_1 \times W_{finger} \times 2 + x_2 \times \left(\frac{N}{2} - 1\right) \times W_{finger} \quad (2.16)$$

$$A_{diode,drain} = x_2 \times \frac{N}{2} \times W_{finger} \quad (2.17)$$

where the definitions of N, x_1 and x_2 are shown in Figure 2-15.

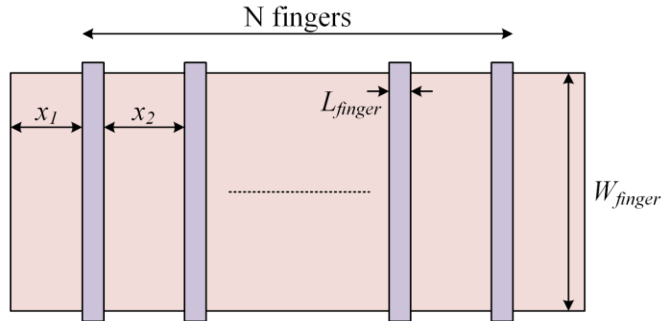

Figure 2-15 Example: layout of MOSFETs in digital circuits.

Similarly, the dimensions of ESD Parasitic resistances can be determined in the same way, and the resistance can be calculated by Equation (2.13) and Equation (2.14). What needs to be pointed out is that the intention of this simulation method is to preliminarily evaluate and verify the CDM ESD protection capability of the circuit in the schematic design, and this method will not excessively pursue the accuracy of the CDM

simulation. Therefore, estimating the parameters of ESD parasitic components with design rules is reasonable and practical.

2.6 CDM Discharge Model – Power Network

The core circuits are connected to the power network, which is made of metal. A power network with parasitic resistance and inductance is illustrated in Figure 2-16, which includes the power mesh of core circuit and the power bus of pad ring. Circuit designers need to estimate the size of the power network and the approximated floorplan including the location of pads, according to the core circuit they designed. To simplify the model and simulation, a power network with the same grid size as the substrate grid is recommended though the grid size can be customized. Typically, the power networks (V_{DD}, V_{SS} and GND) are on the top metal layers. Lower and thinner metal layers are ignored in this model because of their relatively high resistance. The sheet resistance ($R_{\square}$) of these metals can be found in the PDK, and the thickness (t) of the metal layer is derived from the sheet resistance. The resistance between two adjacent nodes is

$$R = \frac{\rho \cdot l}{w \cdot t} = R_{\square} \frac{l}{w} \tag{2.18}$$

where ρ is the resistivity of the metal, l and w are the length and width of the conductor that between the two adjacent nodes, respectively. Thus, the thickness is

$$t = \frac{\rho}{R_{\square}} \tag{2.19}$$

The parasitic inductance of the power network can be simulated using COMSOL Multiphysics with Magnetic and Electric Field model. Taking $l = 5\mu m, w = 2\mu m, t =$

$1\mu m$ and $l = 20\mu m, w = 5\mu m, t = 2\mu m$ as two examples, the simulated values (inductance *vs.* frequency) are shown in Table 2-2. We can see that the frequency change has little impact on the inductance, so it is reasonable to fix the inductance that corresponding to 1.0GHz to simplify the simulation.

Table 2-2 Simulated inductance of the power network model.

Frequency (GHz)	Inductance (pH) of 5μm×2μm×1μm	Inductance (pH) of 20μm×5μm×2μm
0.3	0.17959	0.62612
0.4	0.17959	0.62601
0.5	0.17958	0.62588
0.6	0.17958	0.62571
0.7	0.17958	0.62552
0.8	0.17958	0.62529
0.9	0.17957	0.62504
1.0	0.17957	0.62475
1.1	0.17956	0.62444
1.2	0.17956	0.6241
1.3	0.17955	0.62373
1.4	0.17954	0.62333
1.5	0.17953	0.6229

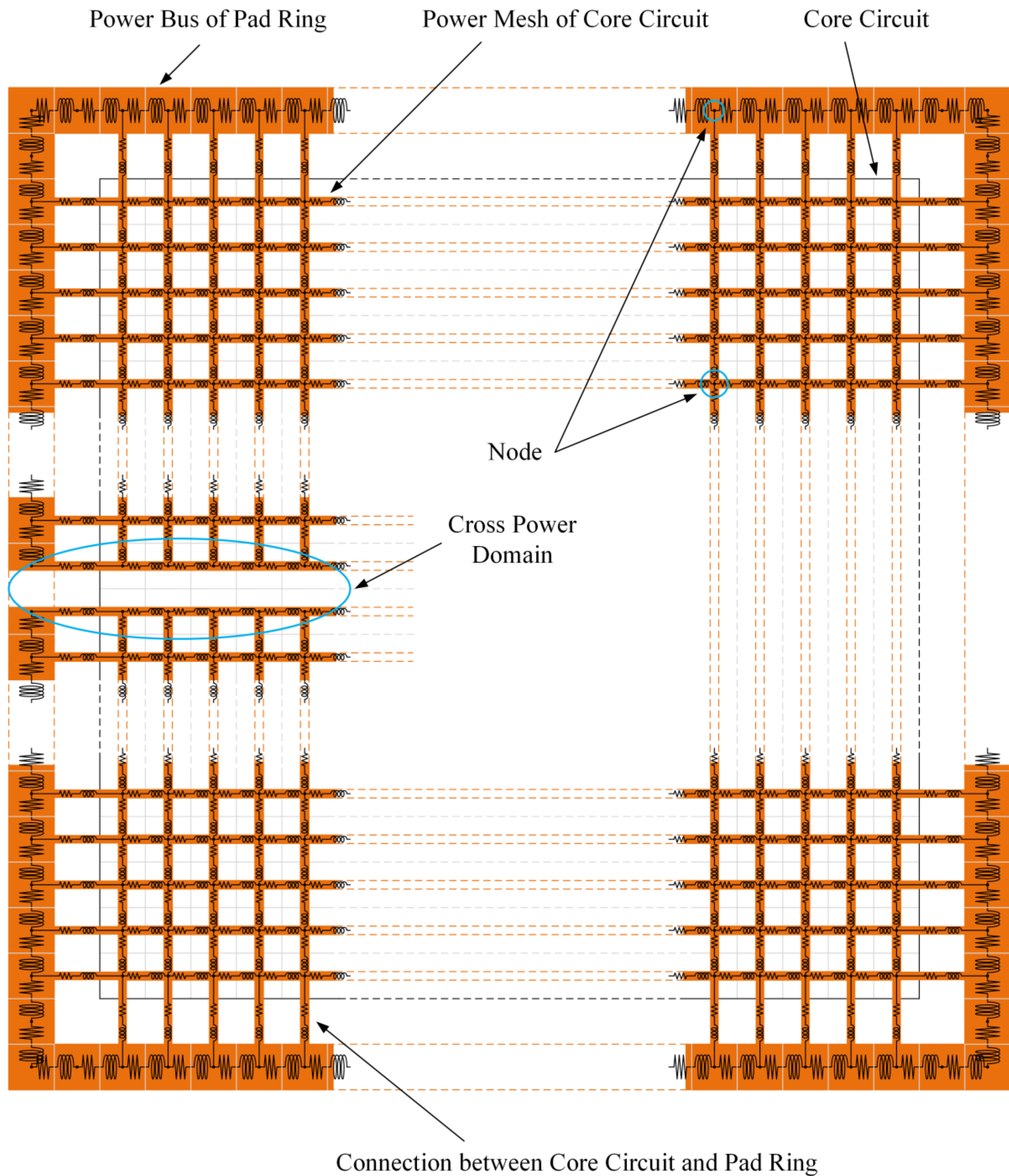

Figure 2-16 Power network model with parasitic resistance and inductance.

The parasitic capacitance is formed between the power networks, i.e. V_{DD} and V_{SS}. The area capacitance (C_{area}) and the edge capacitance (C_{edge}) of each metal layer are listed

in the PDK. Figure 2-17 shows the calculation method of parasitic capacitance between V_{DD} and V_{SS} power mesh. In Figure 2-17,

$$C_{bus} = 25\ (\mu m^2) \times C_{area}\ (pF/\mu m^2) + 10\ (\mu m) \times C_{edge}\ (pF/\mu m) \qquad (2.20)$$

$$C_{mesh} = 9\ (\mu m^2) \times C_{area}\ (pF/\mu m^2) + 16\ (\mu m) \times C_{edge}\ (pF/\mu m) \qquad (2.21)$$

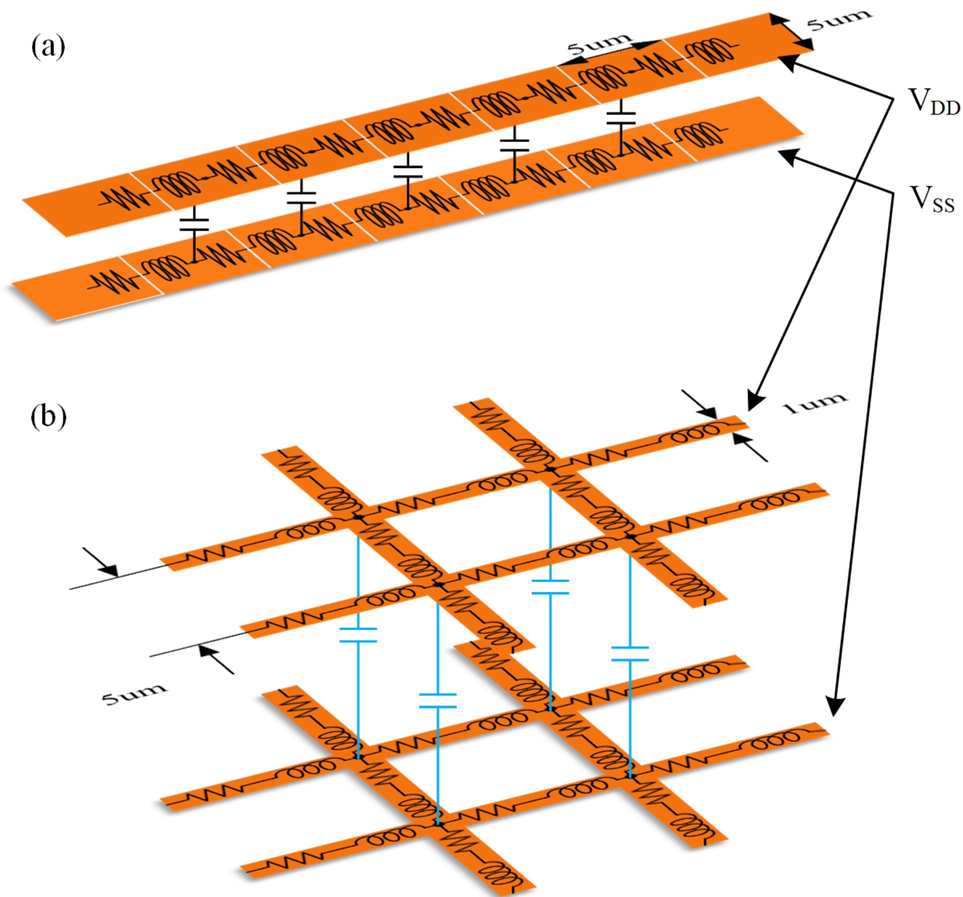

Figure 2-17 Parasitic Capacitance between V_{DD} and V_{SS} in the (a) power bus model (b) power mesh model.

2.7 Behavior Model of ESD Protection Structure

Behavior models of ESD protection structures [7]-[8] are adopted in this SPICE simulation. The procedure of building behavior models is summarized as follows. Firstly,

ESD protection structures are designed and fabricated with selected process. Secondly, the I-V curves of ESD protection structures are measured with Transmission-Line Pulse (TLP) or Very Fast Transmission-Line Pulse (VFTLP) testers. Lastly, behavior models are designed with Verilog-A using the characteristics (V_{t1}, I_{t1}, V_h, I_h, V_{t2}, I_{t2} and R_{ON}) extracted from I-V curves.

Chapter 3 Circuit-Level CDM Simulation

3.1 PRBS Generator Circuit

In engineering, pseudorandom signals are widely used in mobile communication, navigation, radar and secure communication, as well as measurement of communication system performance. The spectrum of pseudorandom binary sequence (PRBS) is very close to the white noise. A 7-bit PRBS generator circuit shown in Figure 3-1 is adopted as the first example to verify this schematic-level CDM ESD simulation method.

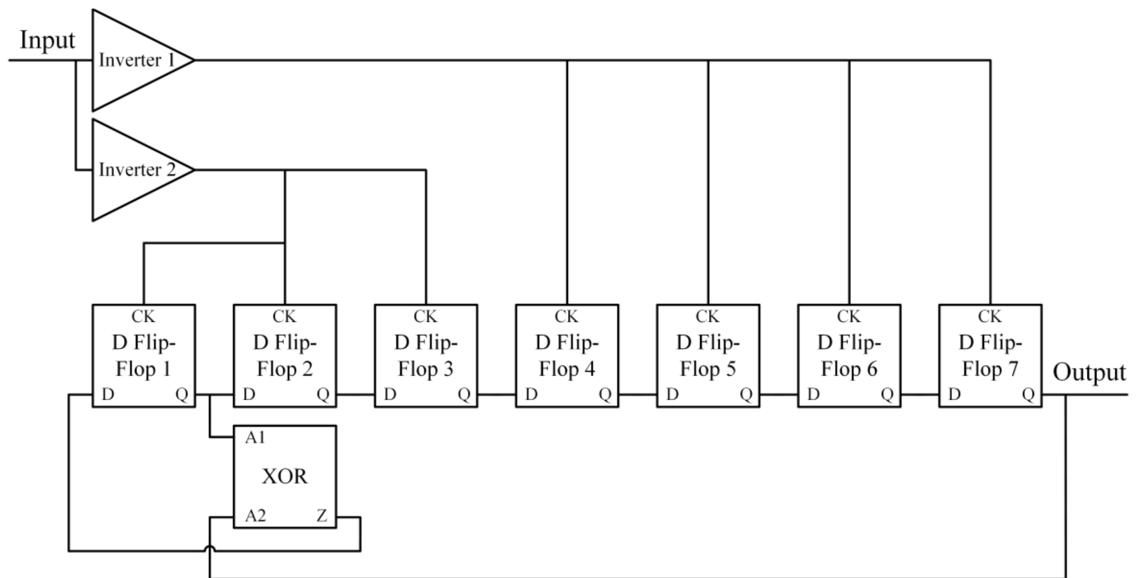

Figure 3-1 7-bit PRBS generator circuit.

3.2 Circuit-Level CDM ESD Simulation Method

Figure 3-2 shows the PRBS generator circuit designed with full ESD protection in a foundry 28nm technology. Two DTSCR of V_{t1}~3.19V are used as used as power clamps,

and eight ESD diodes of V_{t1}~1.03V are placed at the I/O pads [7]. The estimated die size is 150µm by 150µm, as shown in Figure 3-3, and the estimated dimensions of each block is listed in Table 3-1.

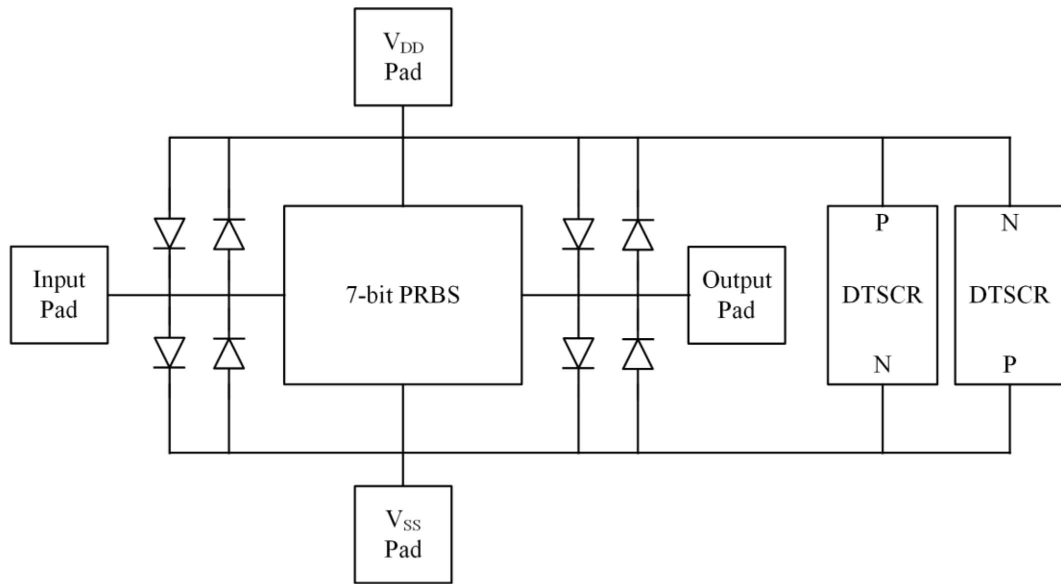

Figure 3-2 A 7-bit PRBS generator circuit with full ESD protection in 28nm CMOS technology.

Table 3-1 Estimated dimensions of each block in the PRBS generator circuit (Units: µm).

Inverter	6.25×5	XOR Gate	5×5	D Flip-Flop	5×5
PRBS	20×15	ESD Diode	20×15	ESD DTSCR	45×20
Pad	50×50				

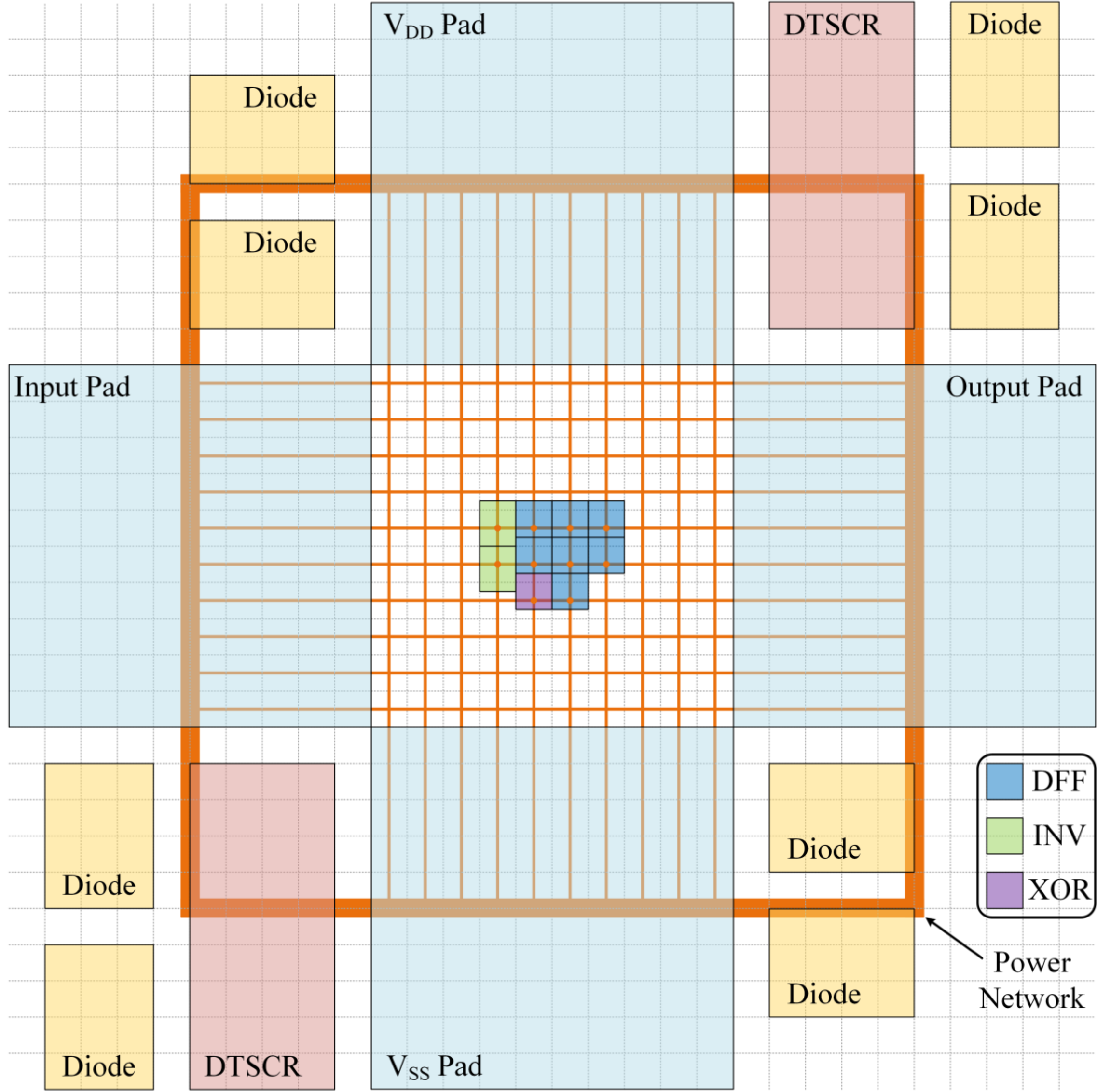

Figure 3-3 Estimated floorplan of the PRBS generator circuit.

Key parameters are calculated as follows. The charge storage capacitance is

$$C_{total} = 30.08\ (fF),\ \ C_{sub} = 4.642 \times 10^{-3}(fF) \tag{3.1}$$

After optimization, the substrate is divided into 6 layers in the z-direction and 30 in x- and y-directions. The resistance for each grid in the substrate mesh is

$$\begin{aligned} R_{lateral} = 288\ (\Omega),\ \ R_{lateral,epi} = 144\ (\Omega), \\ R_{vertical} = 18.4\ (K\Omega),\ \ R_{vertical,epi} = 9.2\ (K\Omega) \end{aligned} \tag{3.2}$$

In this PRBS generator circuit, the number of PMOS is as much as the number of NMOS, so it is reasonable to assume that the n-Well occupies half area of the block. The series resistance of the inverter is

$$R_{\text{series,n-Well}} = 5.67\ (\Omega),\ \ R_{\text{series,p-Substrate}} = 1.47\ (K\Omega) \tag{3.3}$$

The series resistance of the XOR and the D flip-flop is

$$R_{\text{series,n-Well}} = 7.01\ (\Omega),\ \ R_{\text{series,p-Substrate}} = 1.84\ (K\Omega) \tag{3.4}$$

The width of the metal in power mesh is 1μm and it is 3μm in power bus.

$$\begin{gathered} R_{mesh} = 80.00\ (m\Omega),\ \ L_{mesh} = 0.220\ (pH),\ \ C_{mesh} = 371.8\ (fF), \\ R_{bus} = 26.67\ (m\Omega),\ \ L_{bus} = 0.145\ (pH),\ \ C_{bus} = 403.0\ (fF) \end{gathered} \tag{3.5}$$

The test bench consists of two parts (see Figure 3-4), one is the capacitance charging module that charges the substrate capacitance at the beginning of the simulation, and the other is a pogo pin which provides the grounded path for discharge. The pogo pin is modeled by a series-connected inductor and a resistor, with one end of the probe being connected to the pad and the other end being grounded. Two application cases of this CDM ESD simulation model are described as follows.

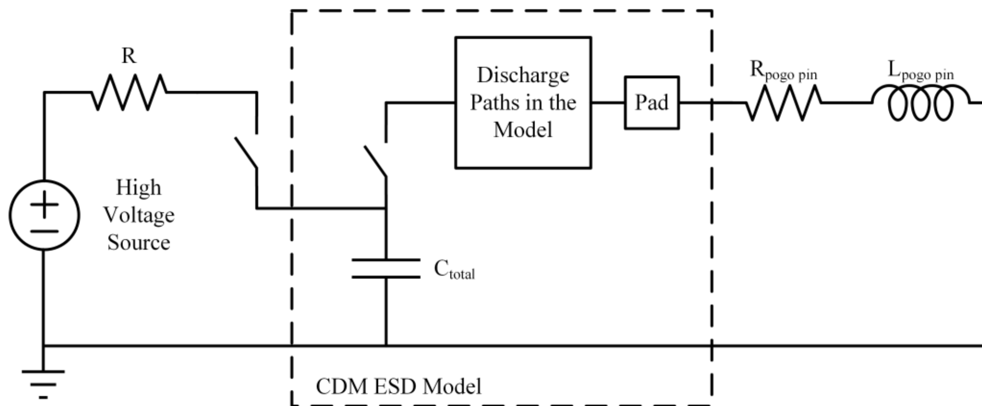

Figure 3-4 Test bench of CDM ESD simulation.

3.2.1 Application Case 1

The first case is CDM ESD discharging when the input pad is grounded. Without ESD protection structures, the PRBS generator circuit cannot pass a positive 100V CDM test which applies positive pulse to the input pad. Figure 3-5 lists the devices having ESD failures reported in logfile during a 2ns transient simulation. Gate-drain junction (J_{GD}) and gate-source junction (J_{GS}) of PM1 and NM1 in two inverters are failed in the simulation. J_{GD} of MM8 in seven D flip-flops are broken down. Waveforms of nodal voltage are shown in Figure 3-6. It is well understood that there is no discharge path existing when ESD protection structures are absent.

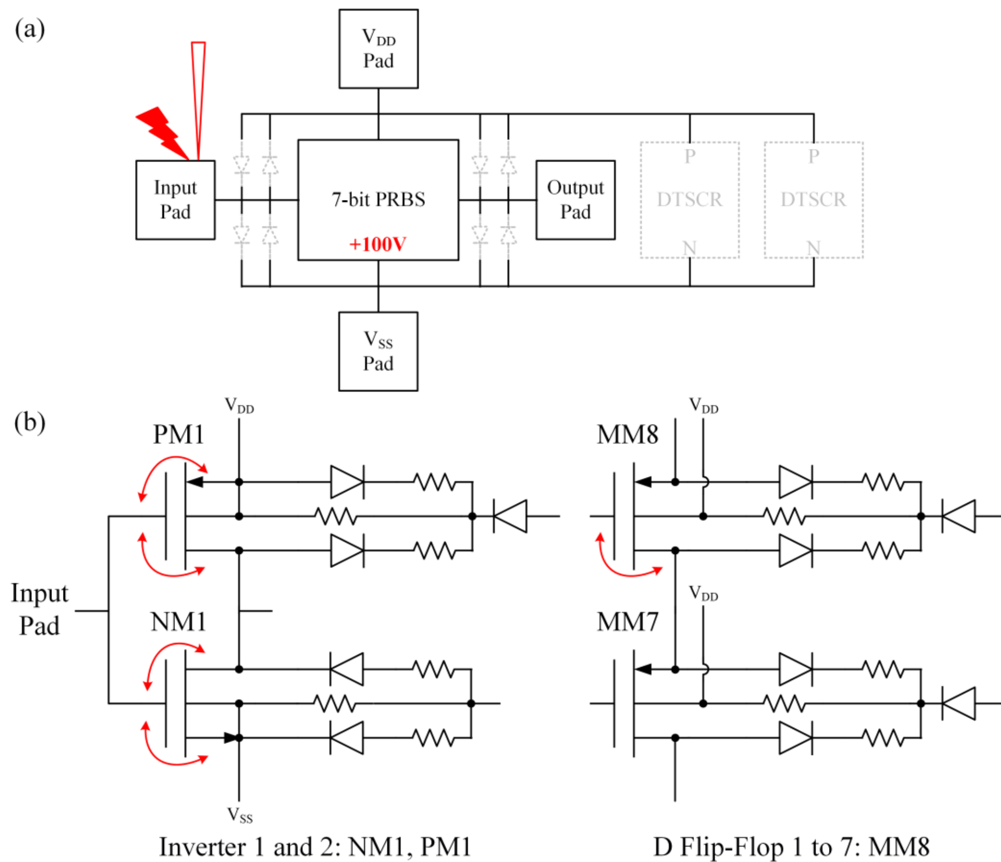

Figure 3-5 (a) Schematic and (b) devices with ESD failures at positive 100V in PRBS generator circuit without ESD protection structures (breakdown junctions are marked in red).

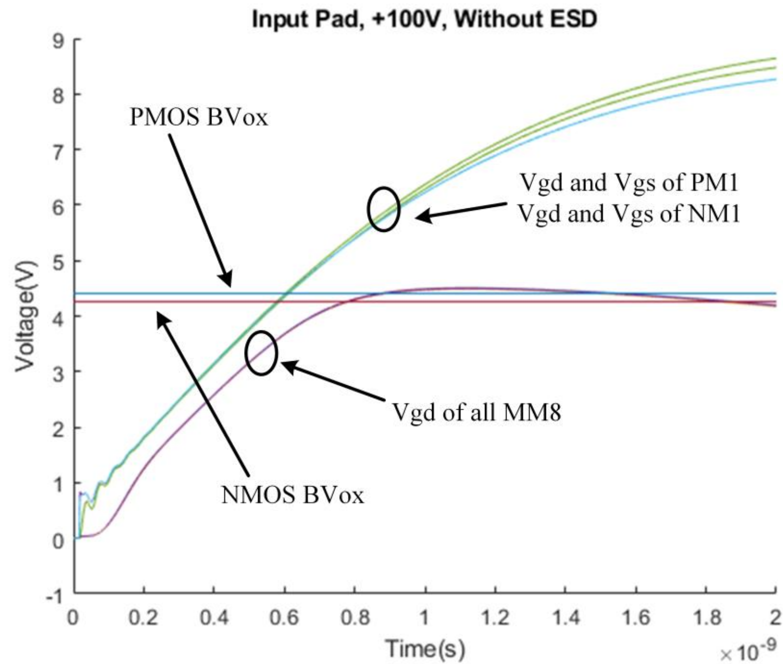

Figure 3-6 Nodal voltage waveforms of NM1, PM1 and MM8 (input pad, +100V, without ESD).

Adding ESD protection structures to the schematic, the PRBS generator circuit passes a positive 250V CDM test. The nodal voltage waveform is shown in Figure 3-7, and the current flow are shown in Figure 3-8 and Figure 3-9. ESD protection structures provide discharge paths for ESD pulse and protect the circuit at 250V. However, an NMOS in the XOR block (see Figure 3-10) is broken down under 300V CDM test, which means that these ESD protection structures provide well protection of 250V in the CDM ESD test. By adding another ESD diode to constitute a primary-secondary ESD protection structure (see Figure 3-12), the ESD protection design reaches the CDM level of 300V, as shown in Figure 3-13.

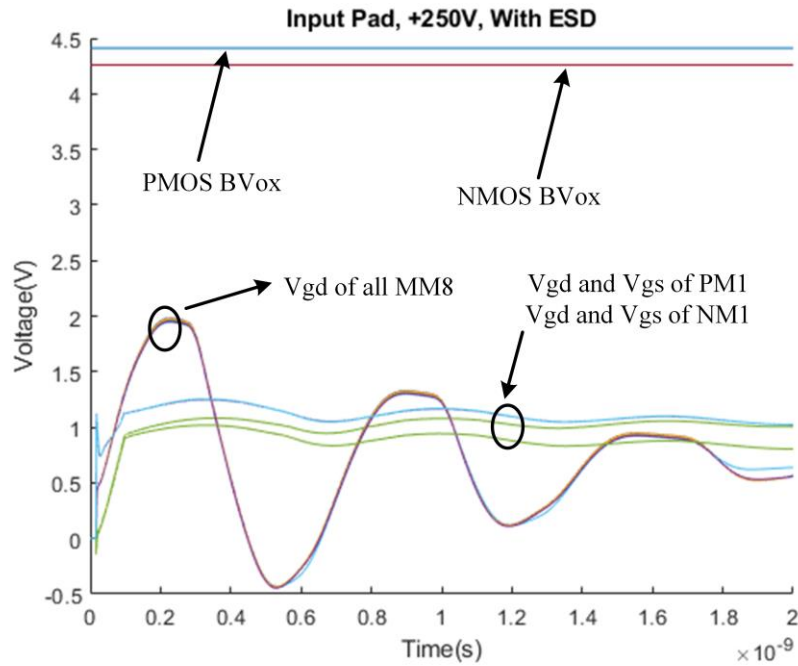

Figure 3-7 Nodal voltage waveforms of NM1, PM1 and MM8 (input pad, +250V, with ESD).

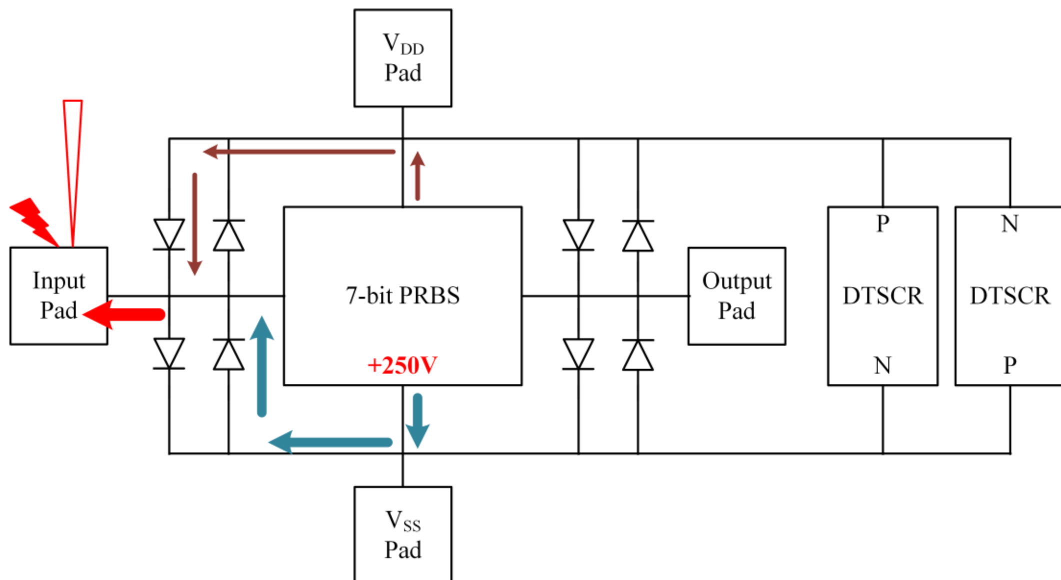

Figure 3-8 Current flow of the PRBS generator circuit and ESD protection structures during a positive 250V CDM test.

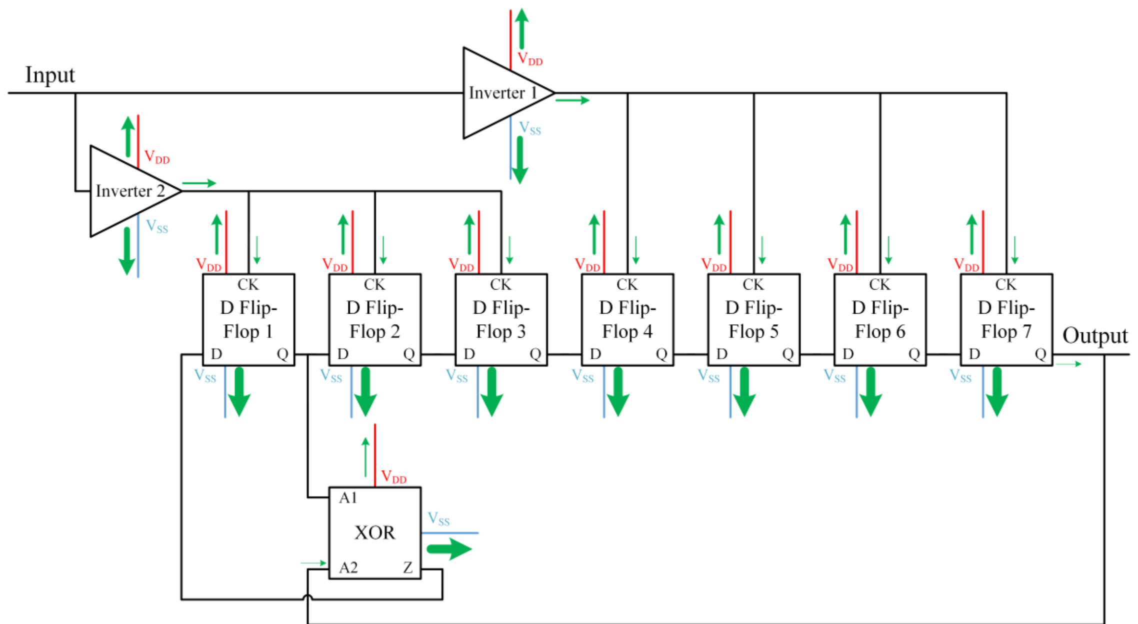

Figure 3-9 Current flow (green arrows) in the PRBS generator circuit during a positive 250V CDM test.

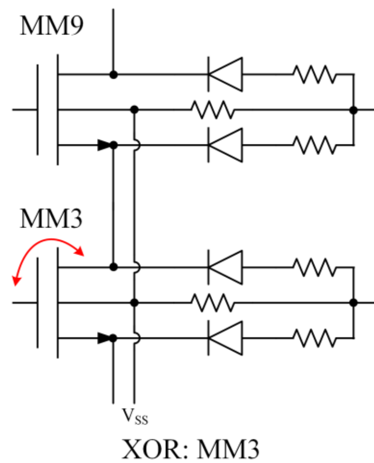

Figure 3-10 Devices with ESD failures at positive 300V in PRBS generator circuit with ESD protection structures (breakdown junction is marked in red).

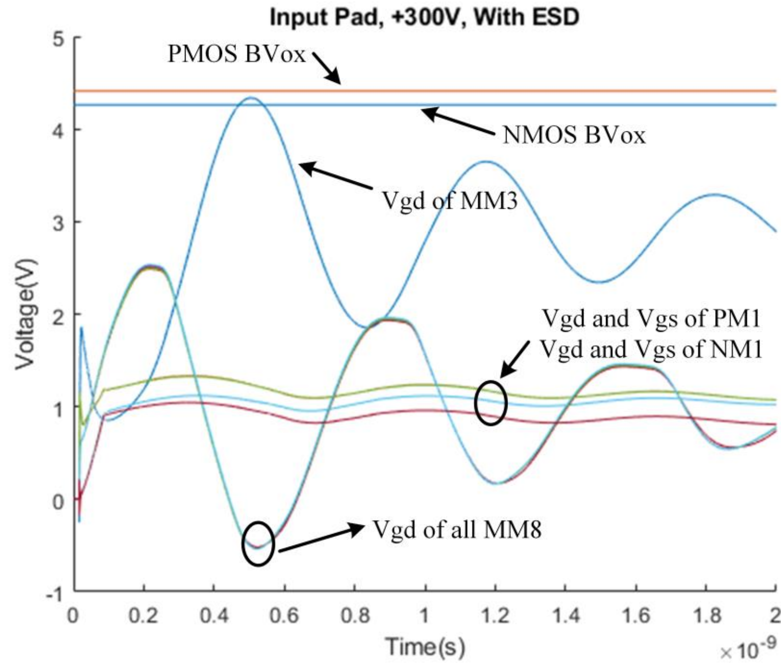

Figure 3-11 Nodal voltage waveforms of NM1, PM1, MM8 and MM3 (input pad, +300V, with ESD).

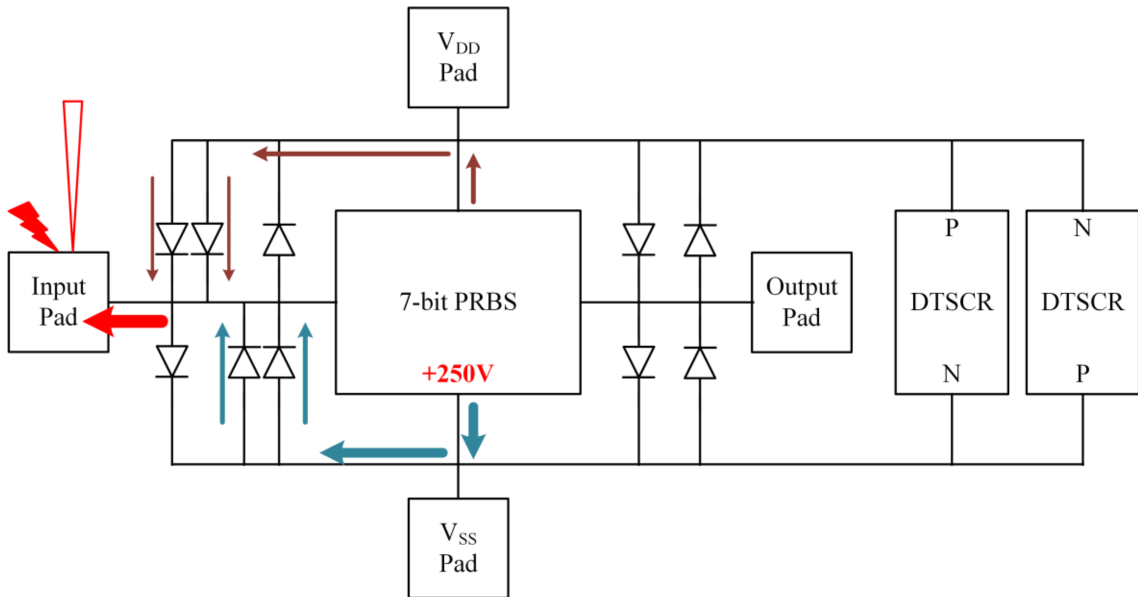

Figure 3-12 Current flow of the PRBS generator circuit and primary-secondary ESD protection structures during a positive 300V CDM test.

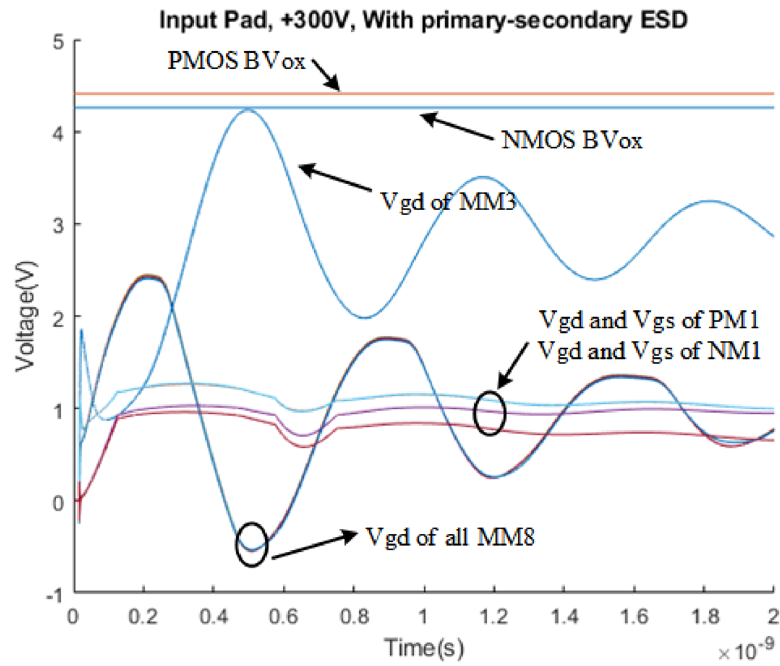

Figure 3-13 Nodal voltage waveforms of NM1, PM1, MM8 and MM3 (input pad, +300V, with primary-secondary ESD).

3.2.2 Application Case 2

In the second case, a negative charged die (PRBS generator circuit) is grounded via the output pad. Without ESD protection structures, the body-drain junction (J_{BD}) of MM23 in the last D flip-flop (DFF7) is broken down at -300V, as shown in Figure 3-14. The body terminal of MM23 is connected to the output pad which discharges easily, thus, the voltage across body (n-type) and drain (p-type) is probably higher than the forward breakdown voltage of the PN junction. The J_{BD} breakdown voltage of NMOS (~8.4V) is higher than it of PMOS (~1.86V). Nodal voltage waveform of MM23 is shown in Figure 3-15.

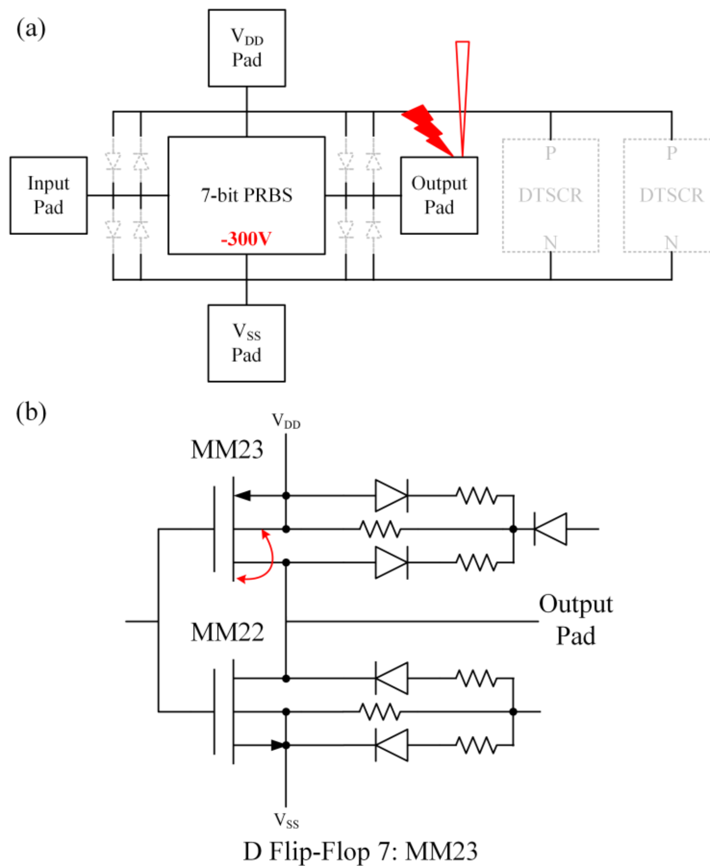

Figure 3-14 (a) Schematic and (b) devices with ESD failures at negative 300V in PRBS generator circuit without ESD protection structures (breakdown junctions are marked in red).

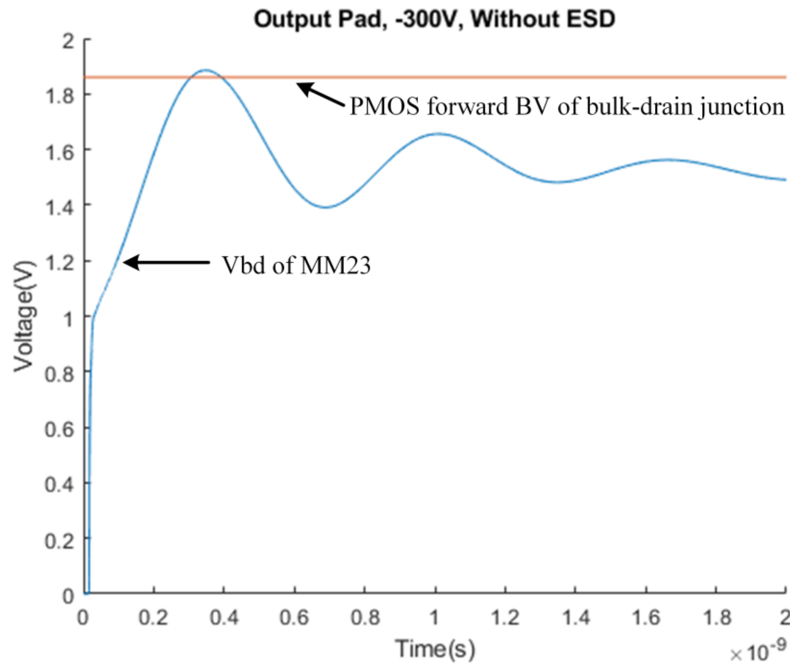

Figure 3-15 Nodal voltage waveforms of MM23 (output pad, -300V, without ESD).

The PRBS generator circuit passes a negative 400V CDM test after ESD protection structures are added on. The nodal voltage waveform is shown in Figure 3-16 and the current flow are shown in Figure 3-17 and Figure 3-18. ESD protection structures provide a discharge path for the body of MM23. As the testing voltage drops to -450V, J_{GD} of a PMOS in XOR is broken down (part of the schematic is shown in Figure 3-19). Waveforms of nodal voltage are shown in Figure 3-20. As in the first case, if the primary-secondary ESD protection structures are applied to the circuit, the circuit will reach a CDM protection level of XXXV, as shown in Figure 3-21 and Figure 3-22.

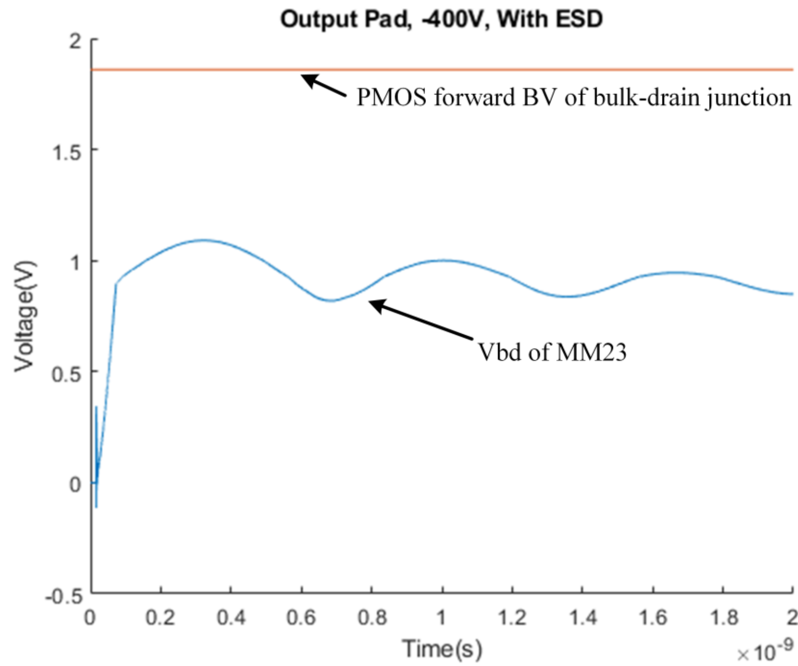

Figure 3-16 Nodal voltage waveforms of MM23 (output pad, -400V, with ESD).

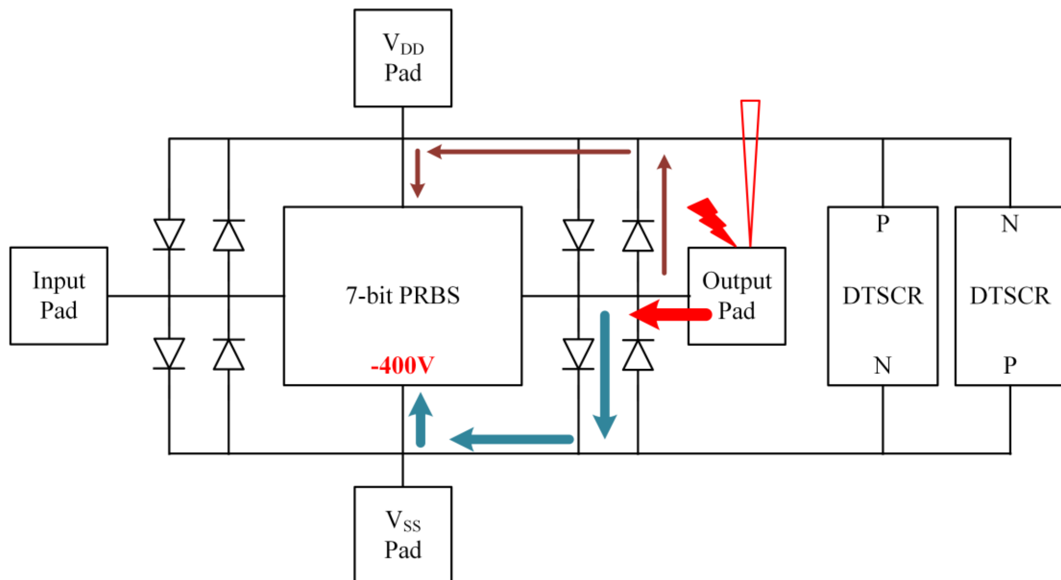

Figure 3-17 Current flow of the PRBS generator circuit and ESD protection structures during a negative 400V CDM test.

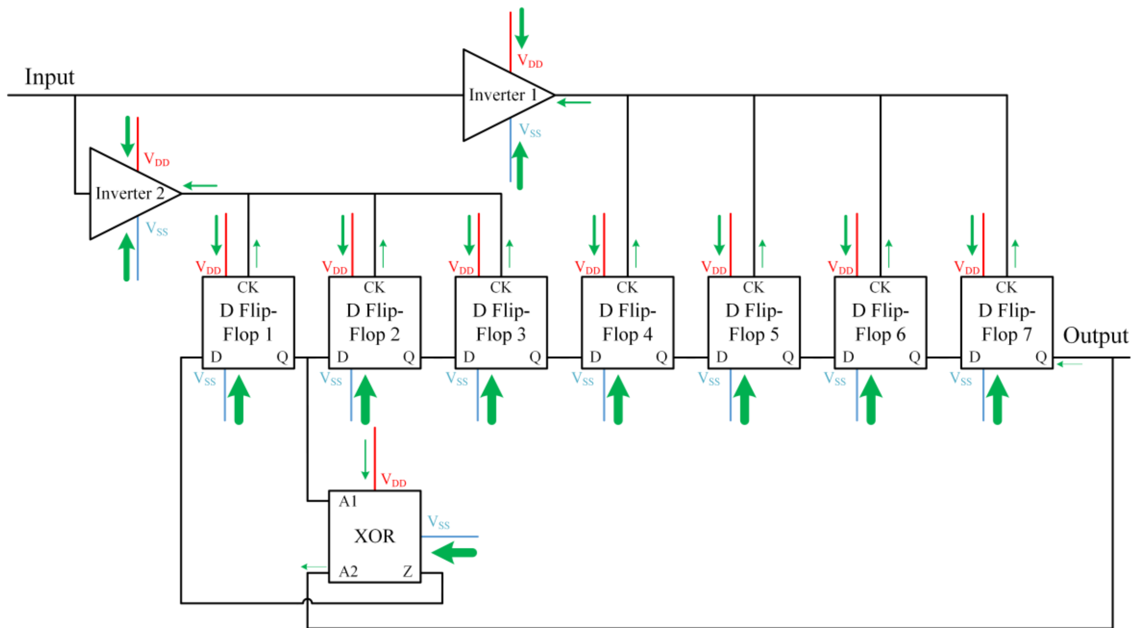

Figure 3-18 Current flow (green arrows) in the PRBS generator circuit during a negative 400V CDM test.

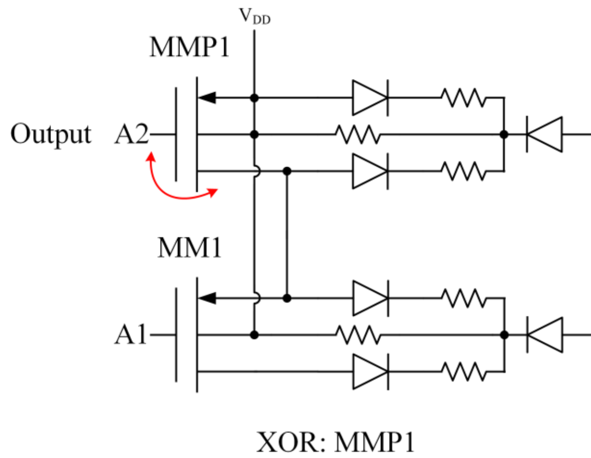

Figure 3-19 Devices with ESD failures at negative 450V in PRBS generator circuit with ESD protection structures (breakdown junction is marked in red).

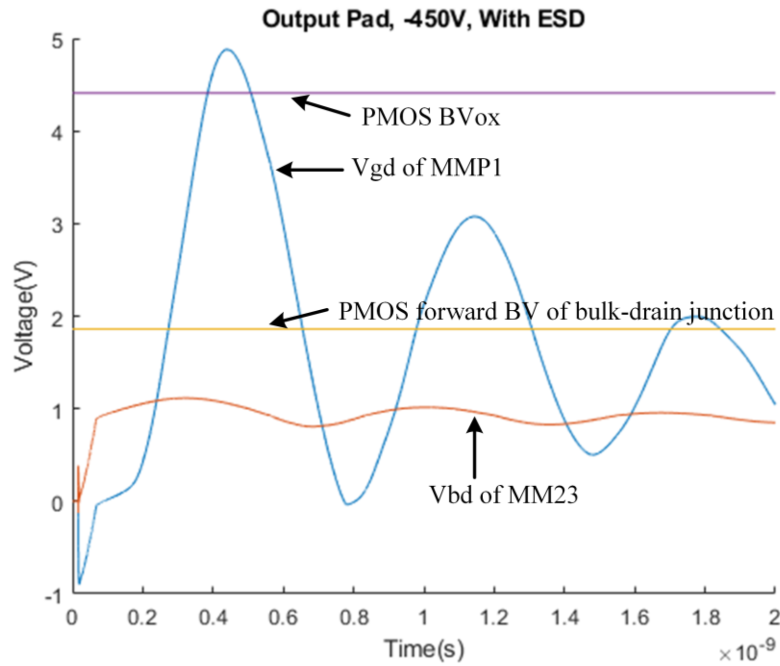

Figure 3-20 Nodal voltage waveforms of MM23 and MMP1 (output pad, -450V, with ESD).

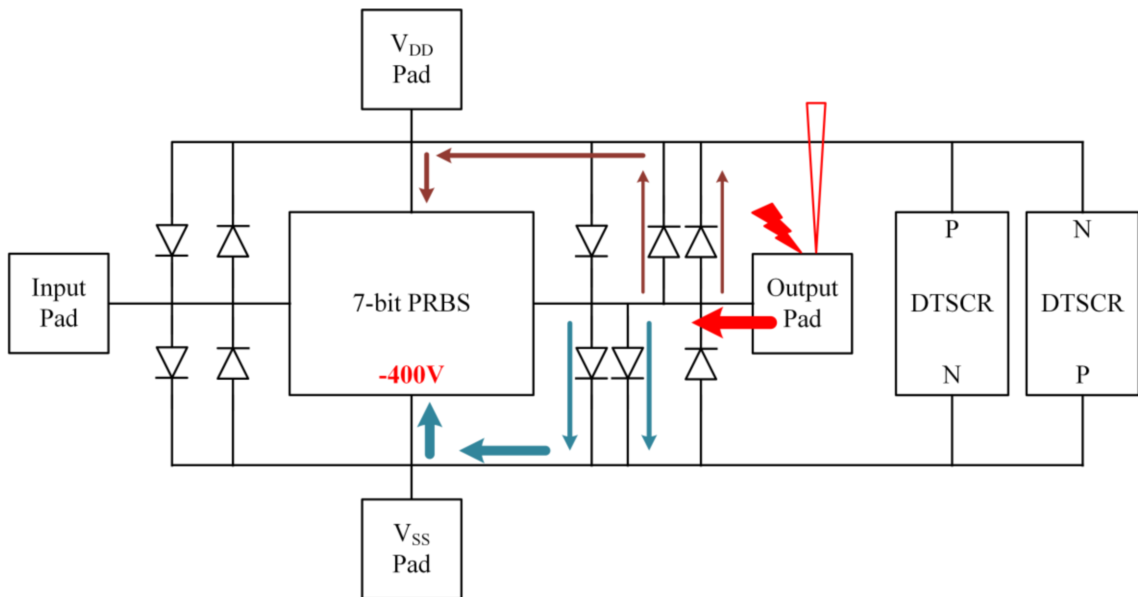

Figure 3-21 Current flow of the PRBS generator circuit and primary-secondary ESD protection structures during a negative 450V CDM test.

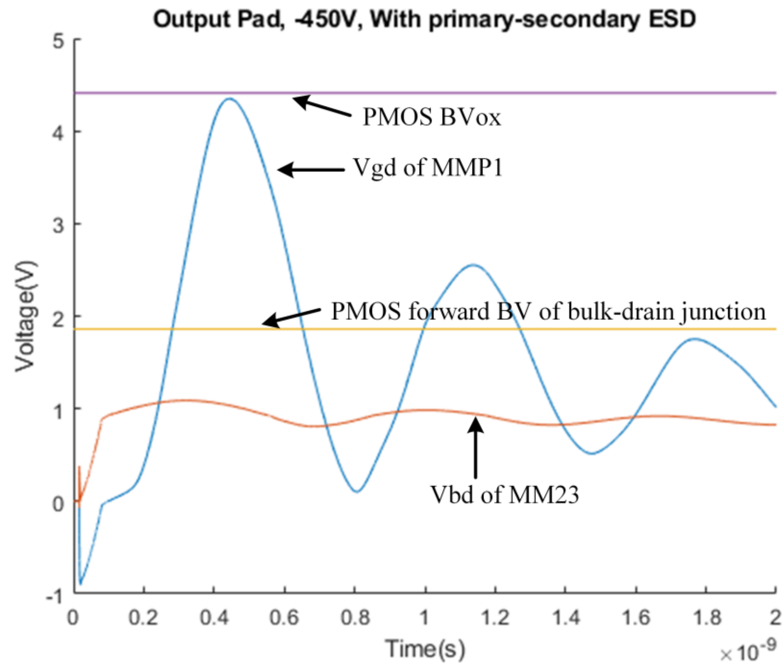

Figure 3-22 Nodal voltage waveforms of MM23 and MMP1 (output pad, -450V, with primary-secondary ESD).

Two application cases described above show the way to use this pre-layout circuit-level CDM ESD simulation methodology to check and verify the ESD protection design in detail. In the next section, a typical circuit and vulnerable circuit topology discovered in the simulation will be discussed.

3.3 A Vulnerable Circuit Topology

Analyzing the failure cases, we can find that the cascode topology (see Figure 3-23) is vulnerable. The electric charge comes out from the substrate to the MOSGFETs through ESD parasitic diodes and resistors when an ESD event occurs. G1/G2 (or G3/G4) are connected to many other devices in the circuit while D1/S2 (or S3/D4) are not connected to other devices except to each other. According to the transient simulation, the potential

of G1 or G2 (G3 or G4) rises or drops slower than the potential of D1 or S2 (S3 or D4). Therefore, once V_{gd1} or V_{gs2} (V_{gs3} or V_{gd4}) is higher than the breakdown voltage of the oxide layer (BV_{OX}), the ESD failure will occur. This topology is very common in digital circuits, so designers should pay much attention to it. To prevent CDM ESD failures in this PRBS generator circuit, the designer may consider ESD protection structures with lower trigger voltage V_{t1}, lower conducting resistance R_{ON} and higher discharging efficiency.

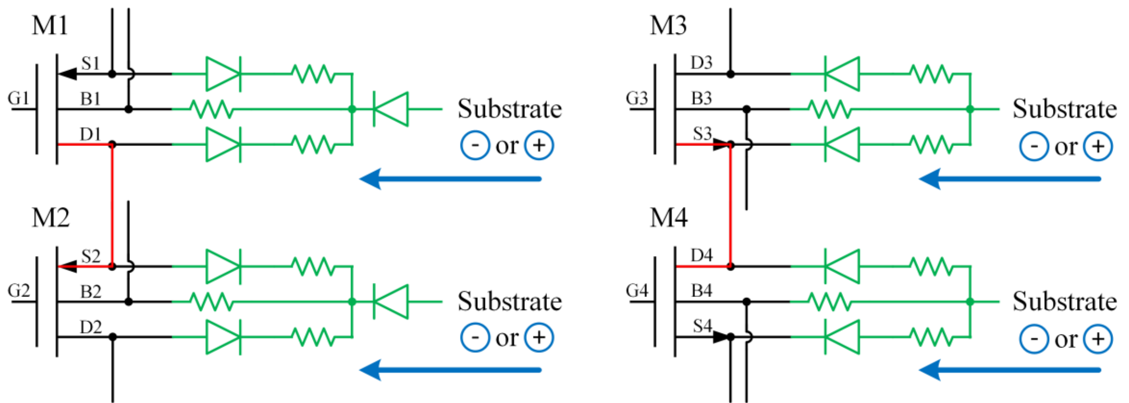

Figure 3-23 Two vulnerable circuit topologies marked in red for PMOS (left) and NMOS (right).

Chapter 4 Conclusion

CDM ESD stress is a major IC reliability issue and its circuit-level simulation is extremely challenging. The previous circuit-level CDM ESD simulation based on the extraction of layout data is complicated and not applicable for circuit engineers to quickly verify the ESD protection design before layout.

To improve the design efficiency and reliability of CDM ESD protection, a CDM ESD model in SPICE and a method of circuit-level CDM ESD protection circuit simulation that enables the full-circuit CDM ESD protection design optimization, verification, and prediction are presented in this thesis. The critical technical problem of pre-layout circuit-level CDM ESD simulation is that the estimation method of each component must be relatively accurate.

This circuit-level CDM ESD simulation model includes a substrate capacitance model, a substrate resistance model, a core circuit model, a power network model and ESD protection structure behavior models. The circuit-level CDM ESD protection simulation methodology is validated using a PRBS generator circuit which designed in a foundry 28nm CMOS technology. A vulnerable circuit topology is discovered in the circuit-level CDM ESD protection simulation.

As for future improvement of this circuit-level CDM ESD protection simulation methodology, the charge distribution may be considered to be more refined, the ESD

parasitic components of ESD protection structures and the impact of packages may be taken into account to get a more realistic chip-level CDM ESD model.

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