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LAWRENCE RADIATION LABORATORY
UNIVERSITY of CALIFORNIA BERKELEY

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ABSTRACT

A storage unit for analog pulses is described which is used to decrease counting losses in high-rate, high-resolution, pulse-height analysis experiments. Three pulse stretchers connected in series store up to three pulses until they can be processed by an external analog-to-digital converter.

An effective dead time of 6 μs is achieved when analyzing randomly occurring pulses at rates up to 20,000 cps. No degradation in pulse height resolution due to the insertion of this instrument has been detected.

I. INTRODUCTION

An important objective of instrumentation for pulse height analysis of the randomly occurring pulses in nuclear spectroscopy is to acquire data at the highest possible rate. To attain this end, pulse-height encoders have been designed for shorter and shorter dead times,1) while analog pulse-processing circuits have been designed to allow good resolution at the high counting rates which the new pulse-height analyzers can handle2).

Currently, pulse-height encoder dead times range from 10 to 200 μs for 12-bit encoding, and good pulse-height resolution can be obtained at input rates much higher than 20 KHz. However, input pulses for nuclear spectroscopy arrive randomly in time and often arrive when the encoder is processing a previous pulse. Thus, the number of pulses measured is much lower than the number arriving at the pulse-height analyzer. This wastes good (and expensive) experimental data; and, in some experiments, requires count rate corrections whose accuracy may be questionable.

For example, consider a typical case of 1.99×10^4 pulses per second, randomly spaced in time, arriving at an analyzer having a fixed dead time of 50 μs. This will result in approximately 10^4 counts per second being analyzed, with the analyzer being busy and rejecting pulses for about 50% of the time. Any count rate correction must be quite accurate since the correction forms a large fraction of the total.

If the pulses arrived at a regular rate to the analyzer, the number of pulses accepted and processed would be twice as large and no count rate correction would be necessary!

The effects of derandomizing incoming data before digitizing have been discussed by Chase[3)] who also describes the operation of an early vacuum tube prestretcher[4)] used for its derandomizing effect. The effects of derandomizing _after_ digitizing has been examined by Alexander et al, who showed that for a three-stage digital derandomizer, counting losses of randomly occurring signals would be reduced to less than 1% at rates approaching 40% of the rate that would saturate the equipment. These calculations agreed well with experimental results.

A relatively simple three-stage analog-pulse derandomizer has been developed, using a modified version of a pulse stretcher designed by Goulding[1)]. The input dead time of the circuit is 4.5 μs. This was chosen to be shorter than the minimum dead time of the pulse processing circuits of the input amplifier system, which are needed for good resolution at high rates[2)]. The pile-up-rejection circuits now used cause a dead time of not less than 6 μs per pulse.

In a typical experimental setup, at the LRL HILAC, dead time per pulse of a 4096 channel analyzer is 35 μs, and counting rates during the 4 ms beam pulse are 15 KHz per second. Under these conditions, the use of the derandomizer reduces counting losses from about 35% to 7%. In order to achieve equivalent results without a derandomizer, it would be necessary to use a pulse-hieght analyzer having a dead time of 6 μs. At the rates quoted, the degradation in resolution when the derandomizer was inserted between the amplifier and analyzer is less than 0.1 channels for a peak near channel 3000.

The design of the derandomizer is shown schematically in fig. 1. Three gated stretcher cards are connected in series; each pulse passes through all stretchers with time delay of about 0.1 μs, and is finally transmitted to the analyzer. If the analyzer is busy, the pulse is held in the third stretcher until the analyzer is free. If that stretcher is full, the next pulse is stored in the second stretcher and if that one is full, the first stretcher stores the pulse. Any pulse that arrives when all stretchers are full will be rejected. When the analyzer becomes free, the output level of the third stretcher is transmitted as a pulse to the analyzer, the stretcher is cleared and reloaded from the level (if any) in stretcher 2. Stretcher 2 in turn is reloaded from stretcher 1. The derandomizing series of 3 stretchers was chosen as a compromise between minimum counting losses and minimum amount of circuitry. For many applications one or two stretchers would be just as satisfactory. A schematic of stretcher 1 is shown in fig. 2, and of stretcher 2, 3 in fig. 3.

In order to understand the details of circuit operation, it is useful to trace the train of events that occurs when a pulse reaches the input. We suppose that this happens when the external ADC is busy processing a previous pulse.

The input gates to all stretchers being open, the input pulse will pass quickly through the first and second stretchers into the third one, triggering all discriminators. After a delay of 2 μs, or at the end of the input pulse, whichever occurs first, the input gate to the first stretcher will close, and trigger a circuit which produces a 130 mV pedestal, needed to ensure linear operation. At the end of 3 μs the gate to the second stretcher will close, and at the same time the first stretcher receives a reset pulse. An additional pedestal is now formed in stretcher 2. (see fig. 4 for idealized waveforms of the second stretcher).

At the end of 4.5 μs, the gate to the third stretcher closes, and the second stretcher is reset. A third pedestal is generated in the third stretcher.

The signal in the third stretcher is held until the ADC BUSY signal falls. At that point, an output pulse is generated whose amplitude is equal to the voltage level held in stretcher 3, and stretcher 3 is reset. (A second signal waiting in stretcher 2 would immediately trigger the discriminator of stretcher 3, and after 4.5 μs, stretcher 3 gate would close again and stretcher 2 would be reset.

To avoid rate effects the stretchers are entirely dc coupled after a s-ngle input capacitor. Thus, dc drift due to temperature changes could easily cause a drift in effective pulse amplitude when the output level of the third stretcher is converted to a pulse for transmission to the ADC. Drift is minimized by careful circuit design in the stretcher; but an additional feedback circuit was found necessary to reduce it adequately. This circuit samples the output level of the third stretcher whenever no signals are present and provides a long-term baseline reference signal. At very high rates, when there may never be a time without signals present, a special "busy" signal is produced periodically which inhibits the source of pulses for the few microseconds necessary to sample the output baseline and generate the correction signal. The circuit card used to give output pulses and control the baseline is shown in fig. 5.

In fig. 5, the lower part at the circuit feeds a constant current to the base of Q1. This current is automatically adjusted by the amplifier Q10 - Q16, so as to hold the base of Q10, and hence the emitter at Q2 at a constant voltage, in the absence of input signals. When input signals are present, the feedback circuit is cut at Q13, the constant current reference being maintained due to the voltage level held by C11. Capacitor C11 discharges very slowly while signals are present and is restored very rapidly when input signals are not present. The quiescent voltage level on the emitter of Q2 is initially adjusted by R19 to exactly compensate the pedestal voltages produced by the 3 stretchers.

The output pulse to the ADC has an amplitude equal to the voltage at the emitter of Q2, and a width equal to that of the "Strobe" pulse. Transistor Q3 supplies a constant current of about 5.5 mA, all of which normally flows in R5, leaving CR1 and CR3 reverse biased. Currents in

CR7 and CR6 are equal, and the base of Q7 is held very close to 0 volts. During the strobe pulse, Q4 conducts, CR2 is reverse biased, and the constant current from Q3 is shared equally by CR1 and CR3, raising the base of Q7 and thus the output signal on the emitter of Q9 to the voltage level on the emitter of Q2, giving an output pulse suitable for the input to an ADC.

ACKNOWLEDGEMENTS

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FOOTNOTE AND REFERENCES

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5. T. K. Alexander, H. G. Reddering and J. M. Kennedy, A Transistor Magnetic Core Buffer Store used as a Derandomizer, AECL 926 November 1959.

FIGURE CAPTIONS

Fig. 1. Logic diagram of analog pulse storage circuitry. Input signals from a pulse amplifier are stored and then transmitted to an ADC.

Fig. 2. Input stretcher circuit. Input signals are capacitively coupled, and the circuit Q5, Q6 and Q7 prevents the input gate from opening while an input signal is present.

Fig. 3. Circuit for second and third stretchers.

Fig. 4. Waveforms appearing on the second stretcher. For an input pulse occurring when all stretchers are unloaded.

Fig. 5. Output baseline stabilizing and pulse forming networks.

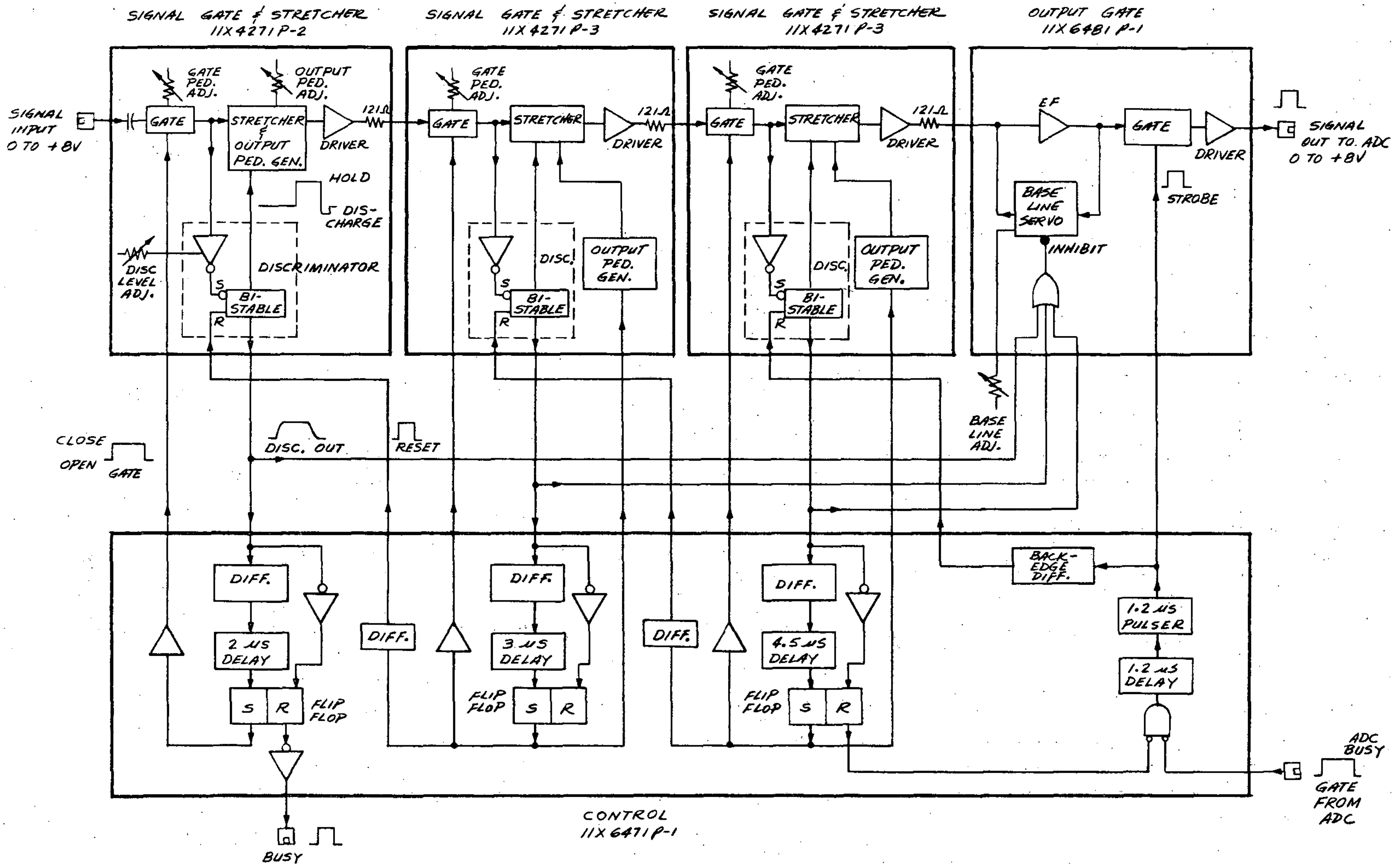

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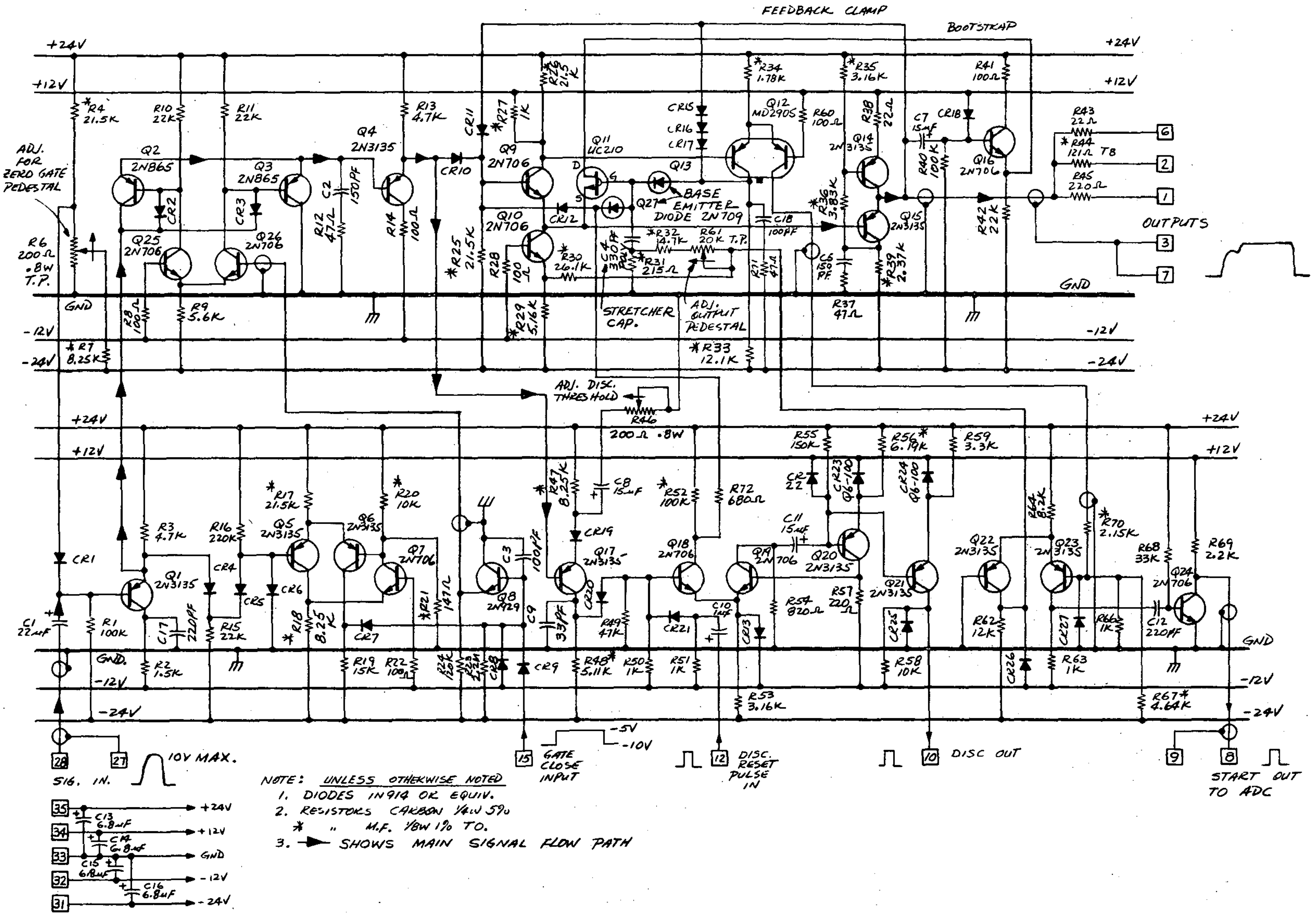
Fig. 1. Logic diagram of analog pulse storage circuitry.



NOTE: UNLESS OTHERWISE NOTED

1. DIODES 1N914 OR EQUIV.
2. RESISTORS CARBON 1/4W 5%
   * " M.F. 1/8W 1% TO.
3. → SHOWS MAIN SIGNAL FLOW PATH

Fig. 2. Input stretcher circuit.

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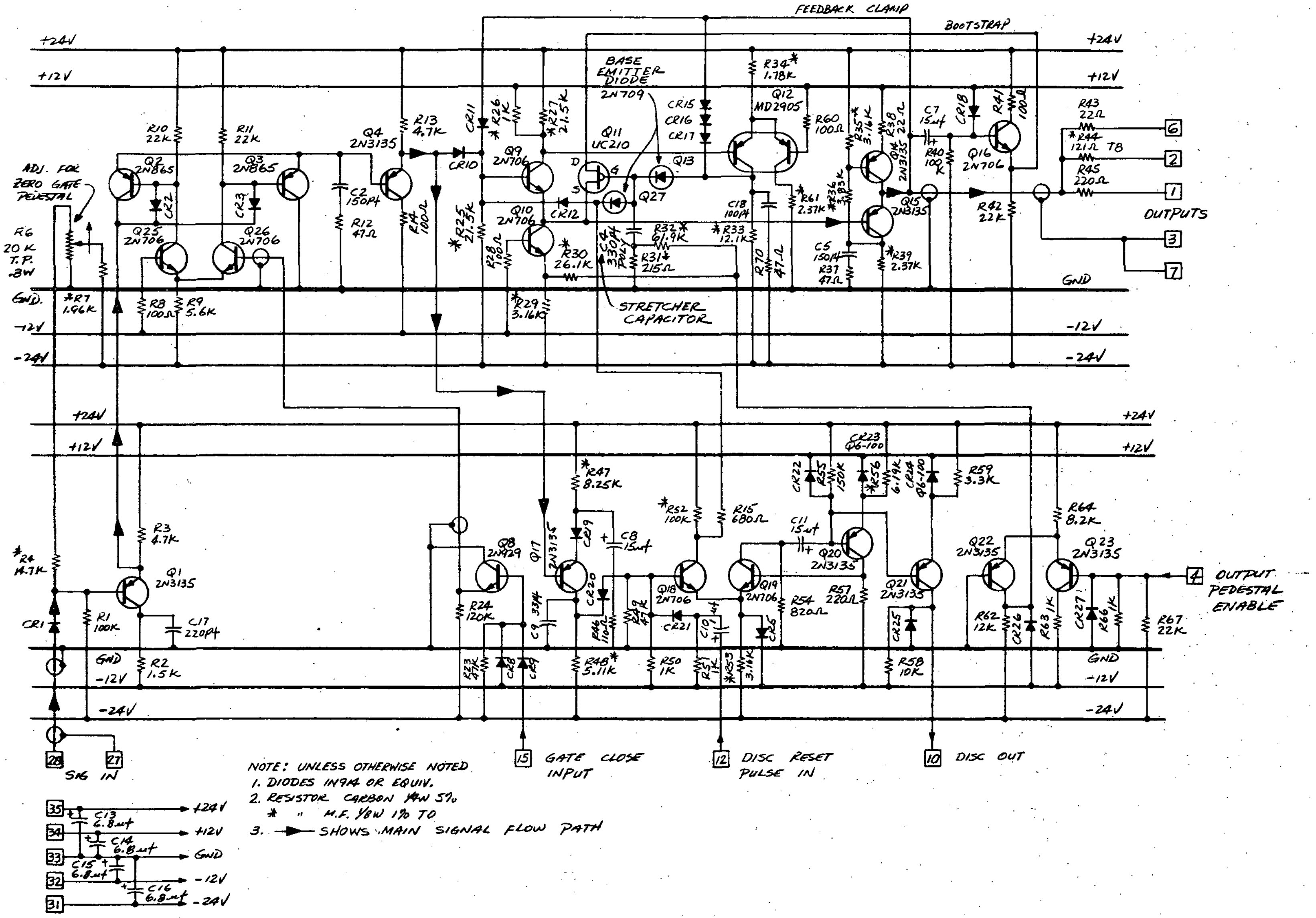

NOTE: UNLESS OTHERWISE NOTED
1. DIODES IN914 OR EQUIV.
2. RESISTOR CARBON 1/4W 5%
* " M.F. 1/8W 1% TO
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Fig. 3. Circuit for second and third stretchers.

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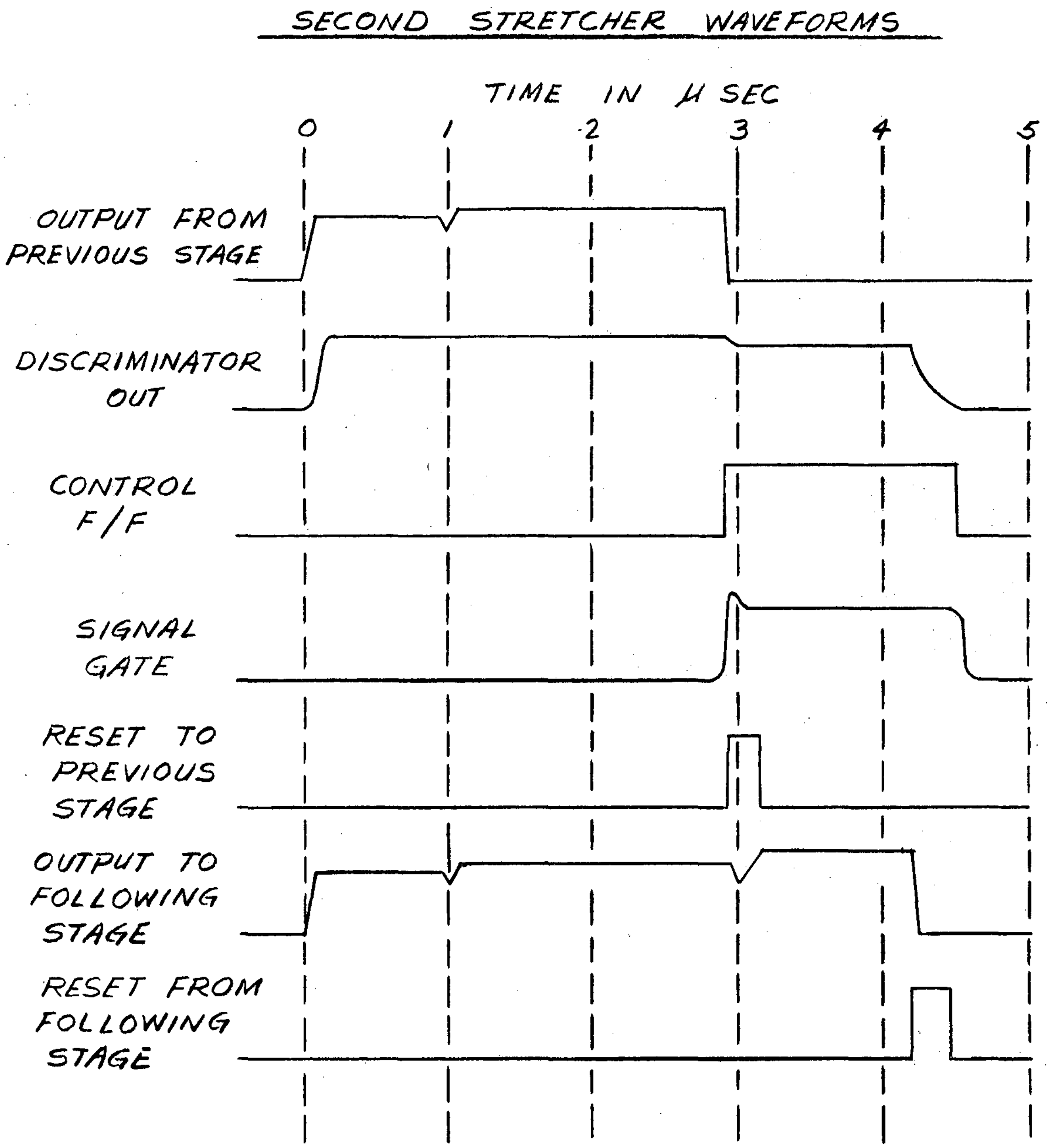

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Fig. 4. Waveforms appearing on the second stretcher.

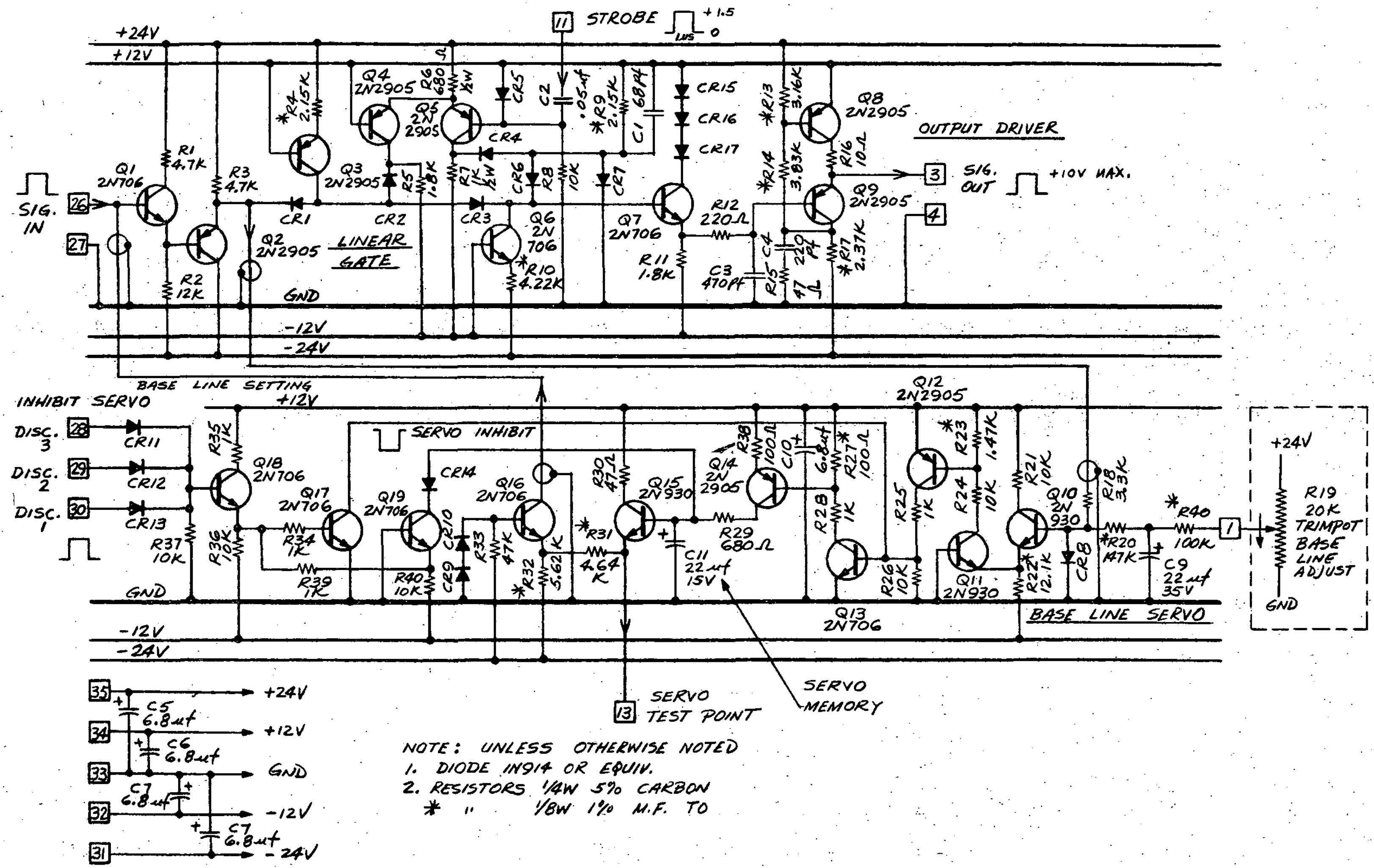

Fig. 5. Output baseline stabilizing and pulse forming networks.

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