UNIVERSITY OF CALIFORNIA

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Cross-domain (RF-analog-digital) techniques to enable power-friendly wireless transceivers

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical Engineering

by

Seyed Sam Gharavi

2013

ABSTRACT OF THE DISSERTAION

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power-friendly wireless transceivers

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Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2013

Professor Babak Daneshrad, chair

With the continuous scaling of CMOS technology, two opposite trends can be observed. First trend is exponential improvement of the digital logic and second trend is linear degradation of the analog and RF components. Traditional methodology for designing analog and RF focuses on optimizing the performance of individual blocks such as analog-to-digital converters, frequency synthesizers, etc. Unfortunately, such traditional approach is limited by the unforgiving power-consumption-performance tradeoffs encountered in the design of each circuit block. As a result, high power consumption of RF and analog has become a major bottleneck for implementation of new communication algorithms.

Alternatively, one can "assist" the underperforming RF and analog blocks using cross-domain (RF-analog-digital) techniques. Such cross-domain approach leads to a significant saving in the power consumption while achieving the desired system performance (e.g. bit-error rate).

This dissertation explores cross-domain techniques to assist the analog-to digital converter, frequency synthesizer and antenna arrays. Novel cross-domain techniques are proposed to optimize the usage of dynamic range of analog-to-digital converter, to track and correct phase noise of the frequency synthesizer and to increase the processing bandwidth of phased array antennas. The proposed techniques have either been directly verified in experiment or as a minimum their implementation aspects have been fully considered in order to close the bridge between theoretical studies and practice.

By applying the proposed techniques to the system design of a 60 GHz radio link, we could improve the bit error rate of the link by several orders of magnitude while consuming an order of magnitude less power than the power that would otherwise have been consumed using traditional approach.

The dissertation of Seyed Sam Gharavi is approved.

Danijela Cabric

Mario Gerla

Kung Yao

Babak Daneshrad, Committee Chair

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VITA

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List of dissertation-related publication and research contributions

- Proposed a novel and practical technique to overcome the latency issue in the digitally-assisted interference cancellation system for analog-to-digital converter dynamic range saving [1]
- Proposed a novel phase noise track- and- correct technique applicable to both receivers and transmitters , independent of waveform and modulation [2]
- Proposed a new, phased-array architecture for low-power and beam-squint-free operation at 60 GHz [3]
- Designed, fabricated and measured a low-power analog delay time alignment circuit in 65nm CMOS technology [3]
- Proposed application of the developed negative group delay scheme in [1] to the microwave domain [4]

References publications

[1] S. Gharavi, B. Daneshrad, "Enhancing the Bandwidth of Feedforward Active Cancellation Circuits by Latency Compensation" (to be) submitted to IEEE transaction on circuits and systems I, regular papers

[2]S. Gharavi, B. Daneshrad, "A New, Hybrid RF/Digital Phase Noise Cancellation Technique" accepted for presentation at IEEE circuits and systems conference 2013

[3] S. Gharavi, M.F. Chang, B. Daneshrad, "Improving the Power Efficiency of 60 GHz Phased Arrays by Eliminating the Array-Induced Inter-Symbol Interference" accepted for presentation at IEEE circuits and systems conference 2013

[4] C. M. Wu, S. Gharavi, B. Daneshrad, T. Itoh, "A Dual-Purpose Reconfigurable Negative Group Delay Circuit Based on Distributed Amplifiers" submitted to IEEE microwave component letters

Chapter 1
Introduction

1.1. Motivation

It has been envisioned that the future radios will be fully digital and the analog-to-digital converter (ADC) and digital-to-analog converter (DAC) will be placed next to the antenna [1]. Such fully-digital radio is still far from actuality and RF /analog components are still necessary parts of all radios.

On the other hand, with the continuous scaling of CMOS and other semiconductor technologies two opposite trends can be observed. First, the exponential improvement of the efficiency of the digital logic and second, the linear degradation of analog and RF components due to lower headroom voltages, higher device mismatches and other device-related issues [7]. As a result, the poor performance of the analog and RF components in a typical communication radio has become a major bottleneck.

Traditional methodology for RF and analog design is to focus on individual circuit blocks and to impose certain performance specifications such as ADC's dynamic range, voltage-controlled-oscillator (VCO's) phase noise, low-noise

amplifier (LNA)'s noise figure, etc. Unfortunately, however, analog and RF blocks are usually governed by unforgiving tradeoff rules between power consumption and performance. As two examples of unforgiving tradeoff rules, power consumption of a typical ADC increases exponentially with the resolution and phase noise of a typical oscillator is only inversely proportional to its power consumption, as described in more detail below.

Figure 1.1 from [2] shows the energy required for one sample analog to digital conversion as a function of the conversion resolution in different CMOS nodes. The data conversion energy has been normalized to the energy required for toggling a digital NAND gate in the corresponding technology node. As evident from the figure, a single, high-resolution analog to digital conversion costs hundreds of thousands of digital gate toggling and yet this cost increases as the technology scales down.

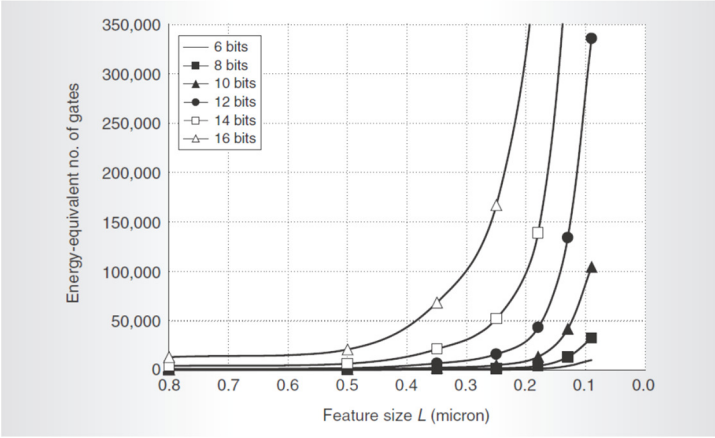


Figure 1.1 energy required for a single analog to digital conversion as a function of the conversion resolution in different CMOS nodes (from [2])

As another example, phase noise of a typical VCO is in general inversely proportional to its power consumption [3] as shown in Fig.1.2. One intuitive explanation for such noise-power tradeoff is that by increasing the power by N times, one can virtually have N independent VCOs and sum their outputs in phase. The power of uncorrelated noises will be increased by a factor of N while that of the carrier signal will be increases by square of N as shown in Fig.1.3. As a result, the ratio of power of the noise compared to the carrier signal (i.e. phase noise level) will be decreased by N.

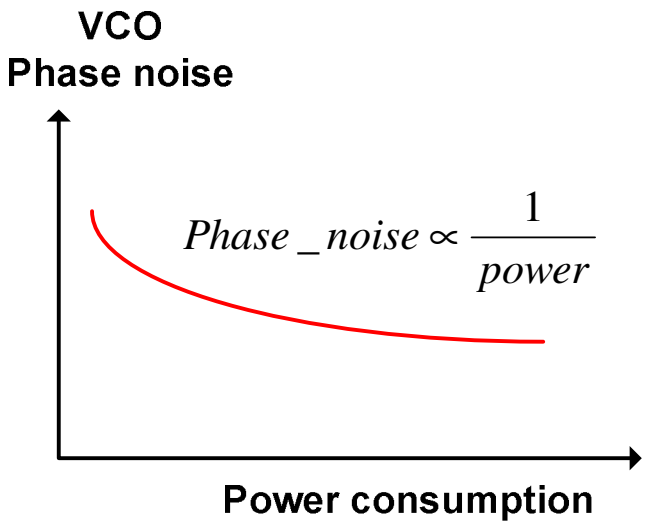


Figure 1.2 harsh noise-power-tradeoff in a typical VCO

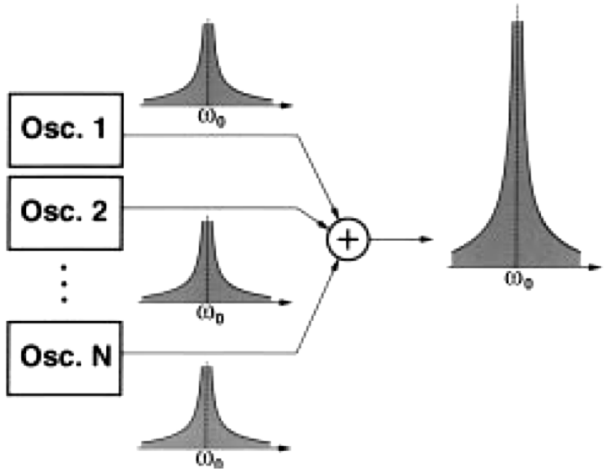
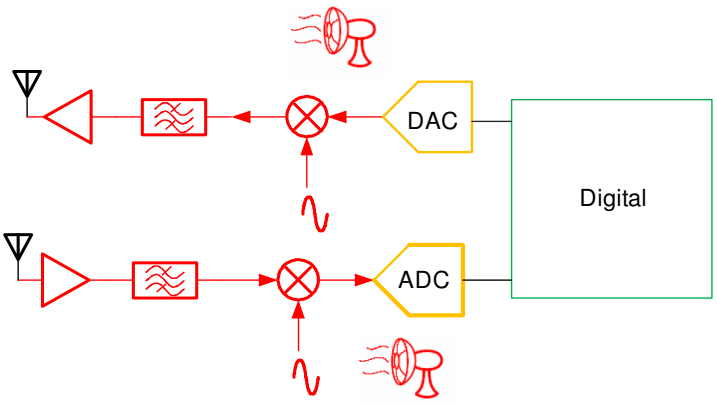


Figure 1.3 Intuitive explanation of the tradeoff in Fig.1.2 (from [3])

As a result of the traditional approach to RF/analog design, RF and analog blocks of radio transceivers consume significantly more power than their digital counterparts. This is despite the fact that the digital blocks play the role of the "brain" of the radio where sophisticated digital algorithms run. As a real-life example, Fig.1.4 depicts the power consumption breakdown of an integrated 802.11a/g radio [6]



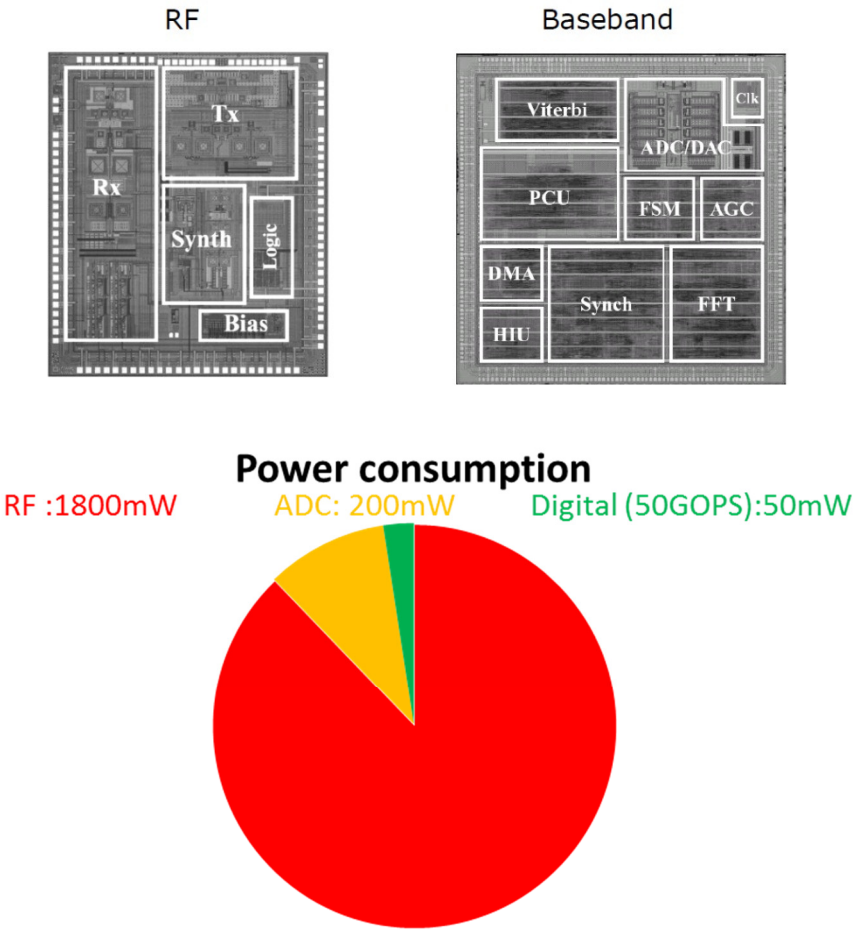


Figure 1.4 Breakdown of power consumption in a typical radio

Such irrational share of analog/RF power consumption has become a bottleneck for implementation of new communication algorithms and calls for a change of perspective in the system design of transceivers. Such a fresh perspective is the main focus of this dissertation.

We explore power-friendly alternatives to the traditional approach that was mentioned above. Our approach includes techniques that cross the three signal

processing domains: RF, analog and digital. These techniques "assist" the non-ideal RF and analog functions in other domains and henceforth save power.

The application that originally motivated us for this research was a millimeter-wave, line of sight (LOS), communication link for short-range (100-200m) outdoor mesh networks. Wireless millimeter-wave mesh networks are cost-effective alternatives to the fiber –optic backhaul [4]. A cornerstone of such mm-wave link is directional communication through the use of electronically-steerable antenna arrays. Given the very limited amount of transmitter power that can be generated at mm-wave, employing directional communication is essential.

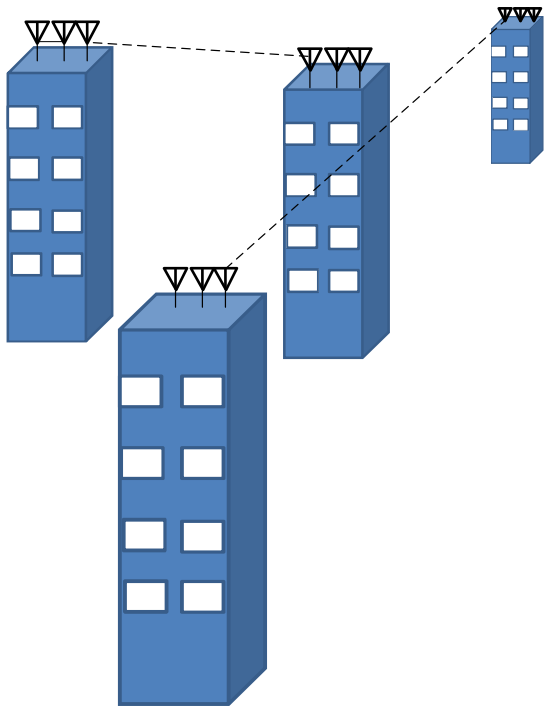


Figure 1.5 mm-wave backhaul network

The abovementioned application is a proper demonstration of many RF and analog impairments due to the large bandwidth and high frequency of operation. In particular, phase noise of the frequency synthesizer, limited dynamic range of the ADC, and beam-squinting of antenna array were identified as the major analog/RF bottlenecks. The following table lists the main parameters of the mm-wave system under study throughout this dissertation.

Table 1.1 system parameter for the mm-wave scenario

Carrier frequency	60 GHz
Channel bandwidth	2 GHz
Number of antennas	32-64
Modulation	Single-carrier QAM
Bit duration	0.5 nsec
Pulse shaping	Raised cosine
Wireless Channel	Line of sight
ADC number of bits	10
Integrated phase noise	5-10 deg

In order to thoroughly capture the effect of analog/RF impairments and also to demonstrate the inefficiency of the traditional approach, we consider a harsh yet realistic system design scenario. Let us assume that the receiver must co-exist with two interferers: a co-channel interferer and an adjacent-channel interferer as

depicted in Fig.1.6. The co-channel interferer is another transmitter in the network. The adjacent-channel interferer stems from the electromagnetic coupling of the receiver to the strong transmitter signal on the same transceiver chip.

The receiver relies on spatial filtering of the co-channel interferer. As we will see in chapter 4, however, such spatial filtering is only partially effective due to the array "beam-squinting". Roughly-speaking, beam-squinting is the variation of the array radiation pattern with frequency.

On the other hand, we assume a rather strong adjacent-channel interference coupling from the self-transmitter due to the frequency division duplexing (FDD) scheme. Unfortunately such strong adjacent-channel interference cannot be filtered spatially and can saturate the receiver's ADC.

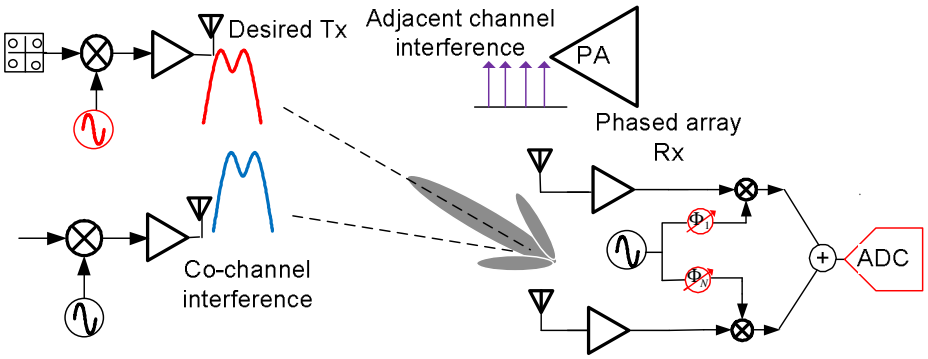


Figure 1.6 a severe yet realistic scenario to capture the analog/RF shortcomings

Figure1.7 shows the spectrum of receiver's ADC's input for the abovementioned scenario. The red curve represents the desired signal; the blue curve represents the co-channel interference and the purple curve represents the adjacent-channel interference. Simulated received constellation points of a QPSK modulation are shown in Fig.1.8. The simulated uncoded raw bit error rate (BER) is approximately 0.2 even at very high signal to noise ratio (SNR).

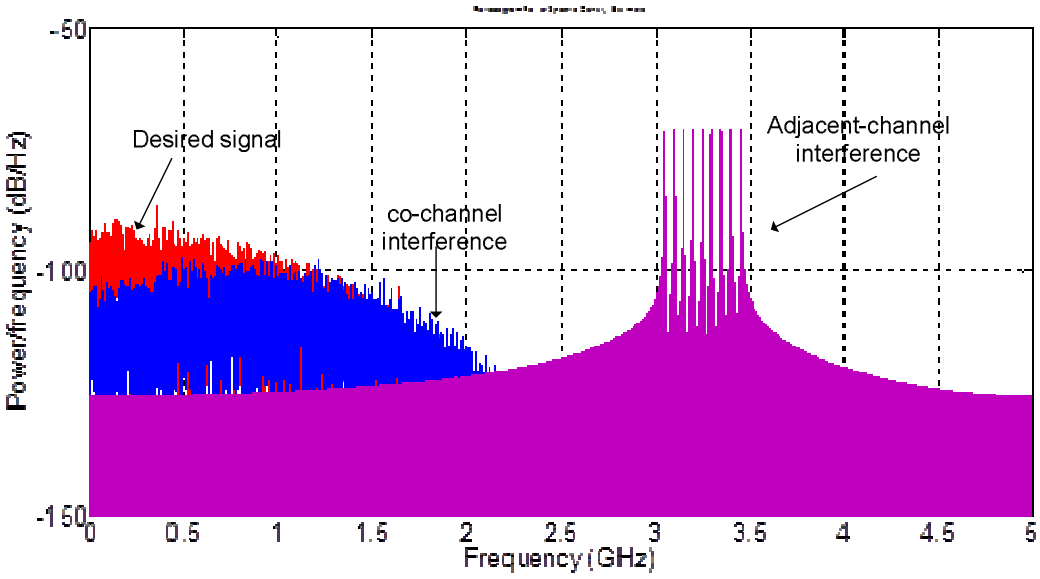


Figure 1.7 ADC input's spectrum for the reference scenario. The red curve is the desired signal; the blue curve is the co-channel interference and the purple curve is the adjacent-channel interference.

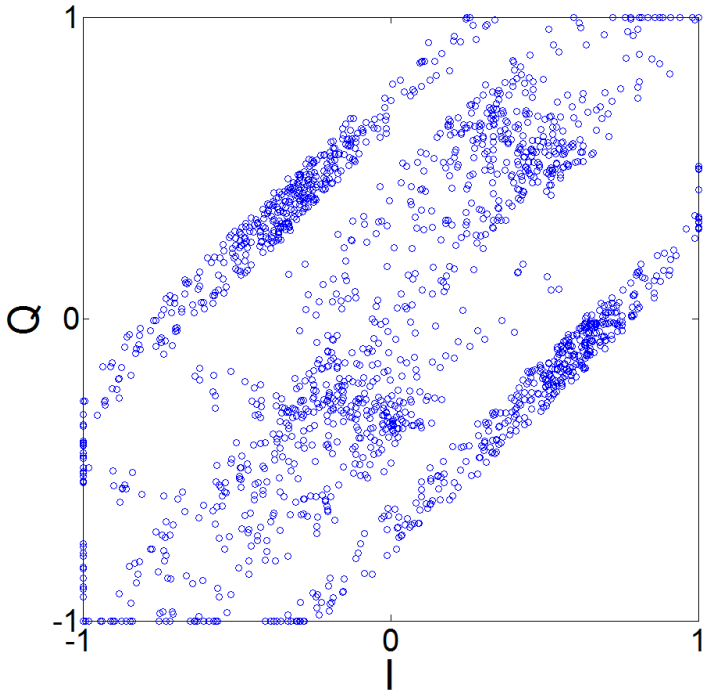


Figure 1.8 simulated received constellation points of QPSK modulation for the referenc scenario (BER=0.18)

In order to establish a link with reasonable BER, one must overcome the insufficient dynamic range of the ADC, beam-squinting of the array and high phase noise level of the frequency synthesizer. Traditional approach to suppress the abovementioned impairments would prescribe designing an ADC with higher dynamic range, a frequency synthesizer with lower phase noise and an antenna array with less beam squinting. Such approach, as we will show would require an enormous amount of extra power consumption. Using our proposed cross-domain approach, however, one would achieve the desired system performance while consuming much less power consumption.

1.2. Dissertation organization

In the upcoming chapters of this dissertation we will delve into the techniques that "assist" the ADC, frequency synthesizer and antenna array using cross-domain techniques. In chapter 2 we will delve into ADC digital assistance through the use of digital interference cancellation. Chapter 3 is devoted to frequency synthesizer assistance through a digital phase noise track and correct. Chapter 4 delves into the issue of array beam squinting and array assistance in analog baseband. Chapter 5 includes the summary and conclusions and future directions and possible extensions.

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Chapter 2

Assisting the ADC in digital domain with a novel, negative-group-delay-assisted, digital, interference canceller

2.1. Background

This chapter is devoted to "assisting" the ADC in digital domain. In a multiuser communication system, the desired received signal is accompanied with large interferers. Unfortunately, even with multiple stages of filtering at RF and analog baseband, interferers can still make their ways to the ADC's input. There are two RF impairments which "pull in" interferers to the ADC's input. First impairment is the phase noise through a mechanism known as "reciprocal mixing". Second is the nonlinearity through the mechanism known as "intermodulation". For a detailed explanation of these mechanisms please refer to [1]. Figure 2.1 depicts the conceptual route of two tone-like interferers from the antenna to the ADC's input.

One may consider employing a highly-selective, analog filter right before the ADC to reject the out-of-channel interferers before they reach the ADC. Unfortunately analog filters have limited frequency selectivity and they either introduce a significant amount of insertion loss if they are implemented as passive filters, or they have limited linearity and high power consumption if they implemented as active filters [11]. For example, the filter that is required to adequately suppress the adjacent-channel interference in the mm-wave link described in chapter 1 requires 40 dB of attenuation at 3GHz while passing DC-2.5 GHz with minimal loss. Implementing such filter in a classical, analog, Opamp-RC circuit requires an Opamp with 30GHz of gain-bandwidth-product, leading to absurdly high power consumption.

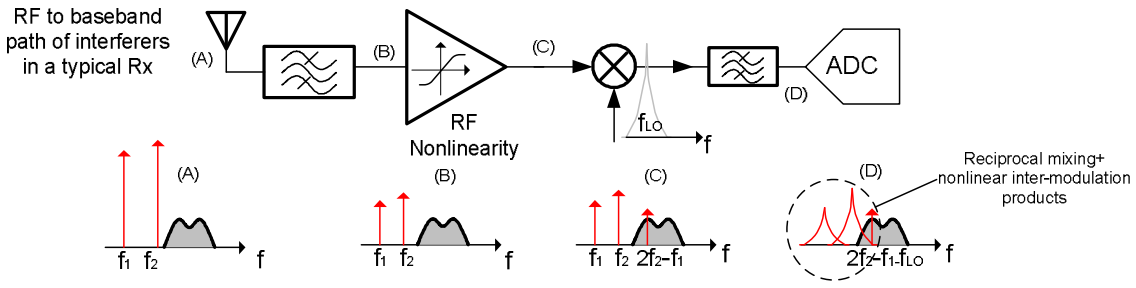


Figure 2.1 Route of two tone-like interferers from antenna to the ADC's input.

As we saw in the chapter 1, high-resolution data conversion is very energy-hungry, especially in modern CMOS. In presence of interferers, the costly dynamic range of the ADC will be misused to process interferers.

It was proposed by the authors of [2] that one can exploit an auxiliary pair of lower-resolution ADC/DAC and also the powerful and cheap digital filters to suppress the close-in interferers before they enter the main, high-resolution ADC. This concept, which is called "digitally-assisted interference canceller" (DAIC) hereafter, is shown in Fig.2.2. An intuitive explanation of the operating principle of this scheme is that a coarse replica of the strong and close-in interference that is accompanying the desired signal is extracted by the auxiliary path and then is subtracted from the input signal. Even though the interference replica is coarse and does not completely resemble the original replica of the interference, the signal to interference ratio (SIR) will be improved. Therefore, the dynamic range of the main ADC can now be devoted to the desired signal.

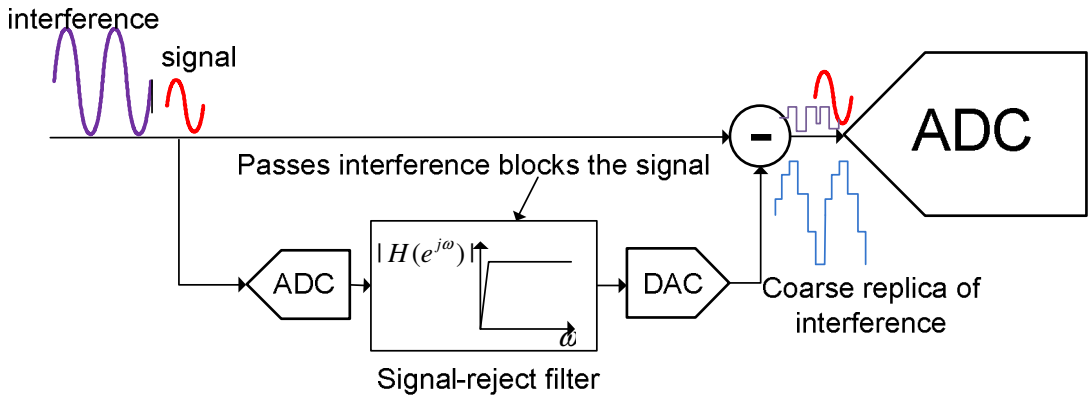


Figure 2.2 Digitally-assisted interference cancellation (DAIC)

In order to quantify the amount of power saving that can be potentially achieved by the DAIC scheme, let us have a numerical example. Tab.2.1 shows the cost of a single analog to digital conversion in 90nm CMOS technology [3]

Table 2.1 Energy cost of data conversion in 90nm CMOS

SNDR *[dB]	EADC [pJ]
30	21
40	60
50	168
60	476
70	1350

*SNDR is the signal-to-noise-and-distortion ratio

Let us assume that the SIR is -20dB and the resolution required for processing the desired signal is 8 bits. In absence of interference one would roughly need 50dB (6dB per bit) of SNDR for 8-bit resolution. However, in presence of interference one would need to budget for an extra 20dB of SNDR. Therefore the cost of 8-bit resolution processing at SIR=-20dB in 90nm CMOS becomes 1350pJ/conversion according to Tab.2.1. If we suppress the interference adequately using an auxiliary ADC/DAC of 40dB SNDR, we would save 1182pJ/conversion while spending only 120pJ/conversion on the auxiliary ADC/DAC.

2.2. The delay mismatch issue in DAIC

Delay is an inherent property of both digital and analog circuits. The underlying cause of delay is that propagation of information-bearing physical quantities such as voltage, current, electrical charge and electromagnetic waves occur at a finite speed. In the DAIC circuit in Fig.2.2, due to the data conversion latency associated with the auxiliary ADC/DAC and also due to the group delay of the digital filter, the coarse replica of the interference lags the main interference in time as conceptually depicted in Fig.2.3. This delay mismatch severely degrades the performance of the DAIC.

The problem of the delay mismatch in DAIC has already been identified in previous works. Quoting the author in [5]:

"An important drawback of this scheme is that it requires an analog delay line to align the signal in the main path with that of the interference estimation path. At present, there exists no efficient solution for implementing this delay line in standard CMOS technology".

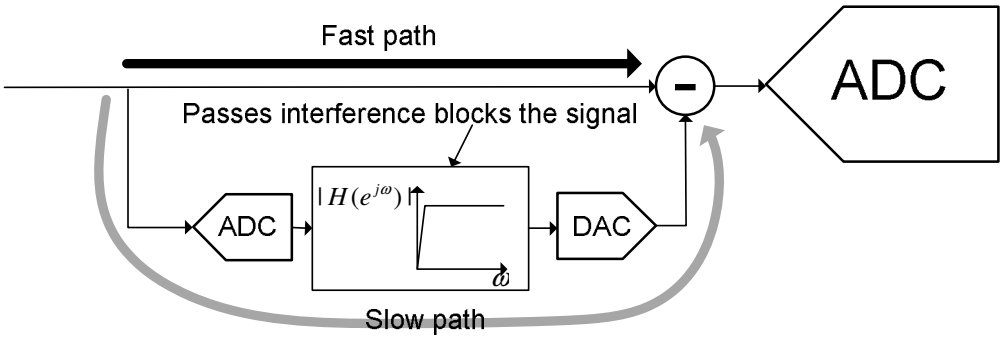


Figure 2.3 the delay issue in the digitally-assisted interference cancellations

Let us further illustrate the destructive effect of the delay mismatch by means of an example. Imagine that the desired signal occupies the normalized angular frequency[1] band of $F_S = [0,0.5]$ and the interference occupies the normalized frequency band of $F_I = [0.6,0.7]$ as shown in Fig.2.4.

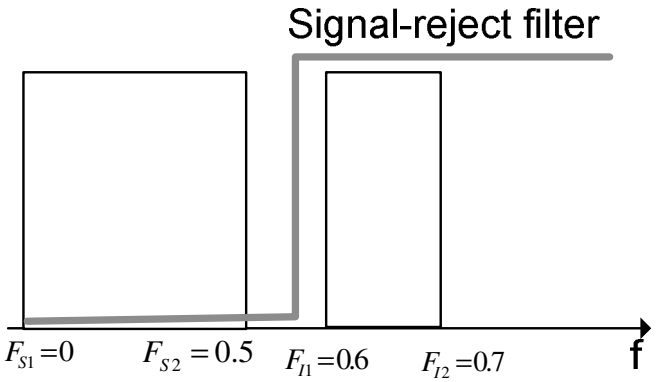


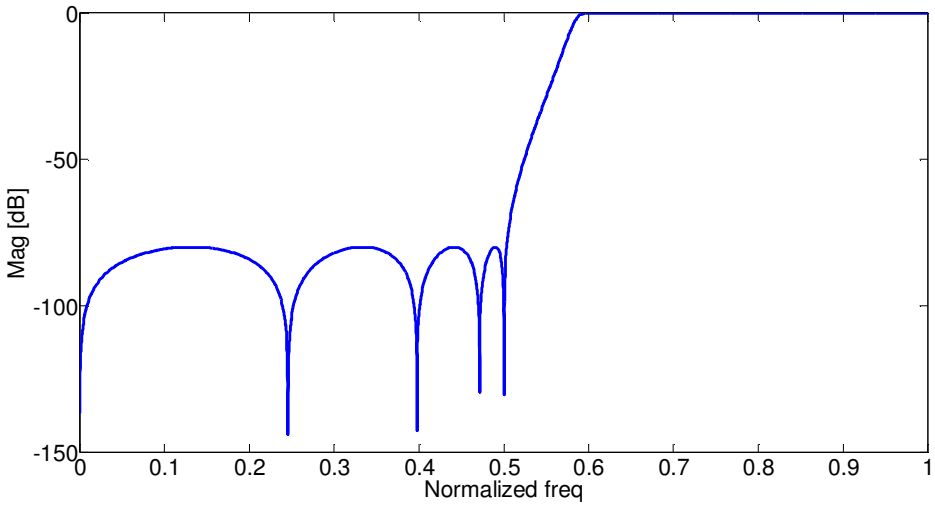
Figure 2.4 signal and interference bands in the example

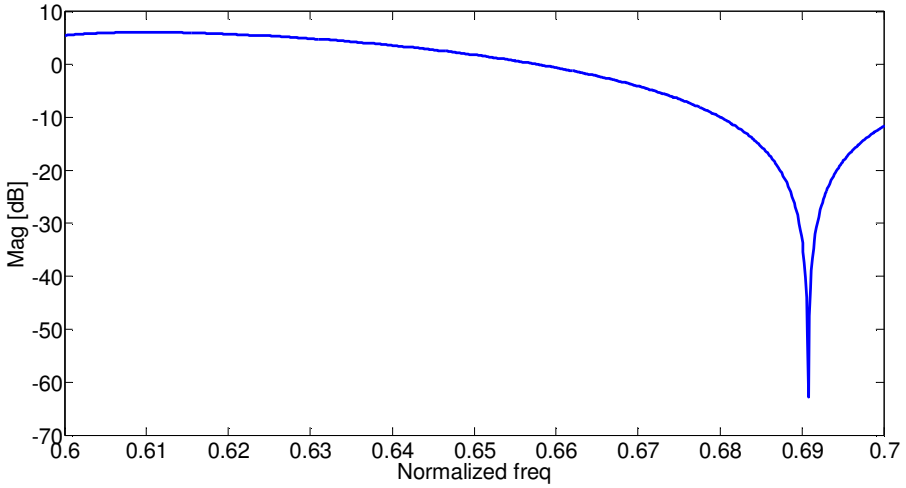
[1] Normalized frequency of one corresponds to the Nyquist frequency, which is half of the sampling rate

Let us also assume that the auxiliary ADC and DAC each introduce one sample of data conversion delay. If we denote the frequency response of the signal-reject filter (SRF) by $H_{SRF}(f)$, and neglect the nonlinear effect of the ADC/DAC, then the overall transfer function of the DAIC will be given by $H_{DAIC}(f) = 1 - e^{-4j\pi f} H_{SRF}(f)$.

We designed an Elliptic, infinite-impulse-response (IIR) SRF using the filter design tools in MATLAB. Figure 2.5 (a) shows the frequency response of the SRF. Figure 2.5(b) shows the overall DAIC magnitude response for this SRF. As evident from Fig.2.5 (b), the DAIC system completely fails to attenuate the interference. In fact, DAIC even amplifies the interference at certain frequencies in the interference band!

In order to show that the only reason for the malfunctioning of the DIAC is the delay, we have assumed a hypothetical, non-causal filter that has the same magnitude response as that of the SRF described above. The mentioned non-causal filter has a negative group delay (NGD) equal to -2 samples at all frequencies (negative of the data conversion latency). The DAIC frequency response using such non-causal filter is shown in Fig.2.5(c). As evident from Fig.2.5(c), the DAIC exhibits the desired frequency response in this hypothetical case.


0
-50
-100
-150
Mag [dB]
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Normalized freq


10
0
-10
-20
-30
-40
-50
-60
-70
Mag [dB]
0.6
0.61
0.62
0.63
0.64
0.65
0.66
0.67
0.68
0.69
0.7
Normalized freq

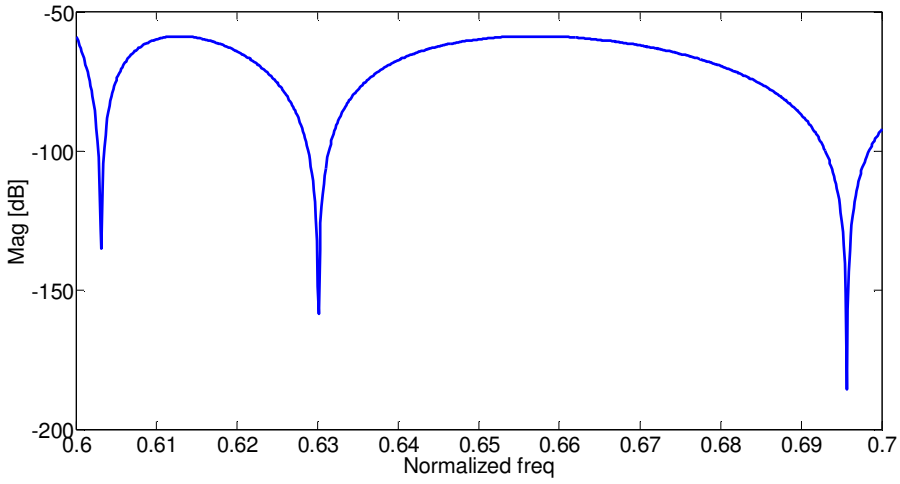

-50
-100
-150
-200
Mag [dB]
0.6
0.61
0.62
0.63
0.64
0.65
0.66
0.67
0.68
0.69
0.7
Normalized freq

Figure 2.5 (a) top- SRF magnitude response (b) middle the overall DAIC frequency response (c) bottom the DAIC frequency response using a hypothetical, non-causal version of the SRF

Unfortunately, filters that exhibit NGD at all frequencies are non-causal and hence not physically-realizable. Fortunately, however, causal filters can exhibit NGD in a limited bandwidth [12], as we will see in section 2.3. We will employ such NGD filters (which have a predicting nature) in section 2.3 to resolve the delay mismatch issue in DAIC.

2.3. Resolving the delay mismatch issue using a novel, linear predictor with negative group delay

Authors in [5] developed a method to overcome the delay mismatch issue in a very particular scenario. They assumed that the interference is frequency-shift-keying (FSK)-modulated, and developed a zero-crossing predictor block in the digital domain to minimize the delay associated with the interference estimation. Unfortunately this solution is scenario-specific and is not applicable to the general cases that the interference is not FSK-modulated.

On the other hand, authors in [2] inserted an analog-active delay line in the path of the desired signal to match the delay of the desired signal with that of the

interference estimation path. The major drawback of this scheme is that it introduces extra noise and distortion to the desired signal.

We propose using a digital linear predictor with negative group delay (NGD) in the interference estimation path to compensate the delay, as depicted in Fig.2.6. The only assumption that we make about the interference is that the interference is band-limited. Our proposed method is generic and does not add noise/distortion to the desired signal.

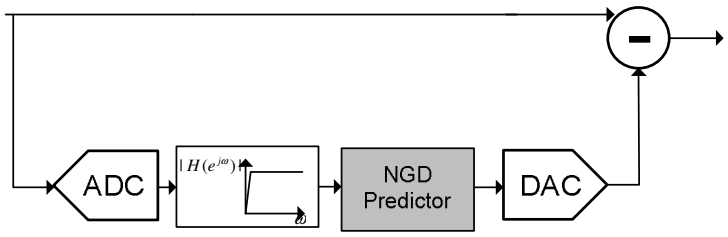


Figure 2.6 Proposed remedy for the delay mismatch issue using predictor FIR filters with negative group delay (NGD)

Linear prediction is a classical problem in the field of signal processing and has been predominantly studied in a stochastic setup. Wiener [6] was the first who derived a mathematical formulation for optimal least square predictor of a stationary, continuous-time random process. The discrete-time version of the same formulation was then derived by Makhoul [7]. Such optimal formulations are

based on the second-order statistics of the signal and therefore require a priori information about the statistics of the signal. If such a priori information is not available then it can be estimated using the time averages as an approximation to the ensemble averages. Such process however becomes cumbersome if the process is non-stationary as the second-order statistics should be updated to track the variations. Adaptive predictors resolve this issue by "learning" and tracking the signal statistics. Please refer to [8] for a reference on adaptive predictors.

Unfortunately in high data- rate applications such as the mm-wave scenario we introduces in chapter 1, we neither have a priori information about the second-order statistics of the signals nor can we afford to employ a power-hungry adaptive predictor. As a result, we seek after a non-adaptive predictor that does not require a priori knowledge about the second-order statistics of the signal. We will formulate the problem of designing the linear predictor filter as a convex optimization problem.

In order to start, we use the linear model of the DAIC depicted in Fig.2.7. We model the quantization noise as an additive component and we denote the SRF and the linear predictor by their frequency responses, $H_{SRF}(f)$ and $H_{LP}(f)$ respectively. We also assume that the ADC/DAC data conversion latency can be modeled as D samples of delay (D does not have to be integer). Finally, we limit

ourselves to finite-impulse-response (FIR) linear predictors with real tap coefficients.

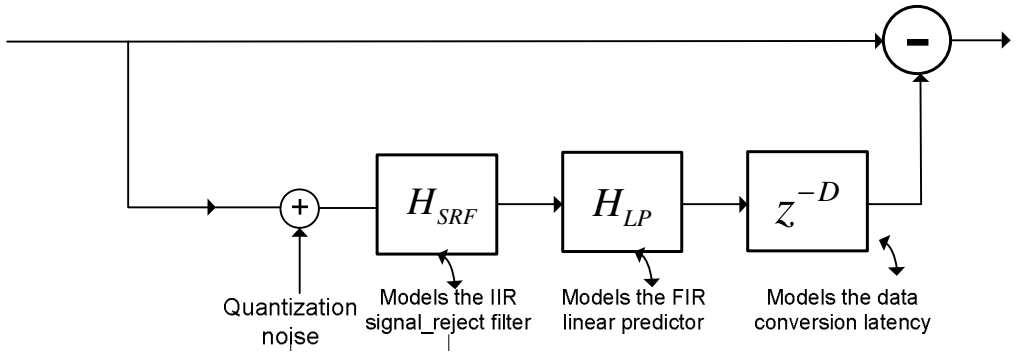


Figure 2.7 the linear model of the DAIC with the predictor

Given a $H_{SRF}(f)$ and D, we formulate the problem as follows:

$$Minimize\{\int_{F_{I1}}^{F_{I2}} |1 - H_{STF}(f)H_{LP}(f)e^{-j2\pi Df}|^2 \, df\}$$

Subject to

$$|H_{STF}(f)H_{LP}(f)| < A_1 \qquad F_{S1} \le f \le F_{S2} \quad (2.1)$$

$$|H_{STF}(f)H_{LP}(f)| < A_2$$

For a linear predictor with length Ntaps, we have the following relationship.

$$H_{LP}(f) = \sum_{n=0}^{Ntpas-1} a_n e^{-j2\pi fn} \quad (2.2)$$

The problem in 2.1 can be solved using the spectral factorization algorithm [9]. In the next section we will show how this formulation leads to a solution that resolves the delay mismatch issue.

From Fig.2.7, one can verify that the magnitude of the transfer function of the quantization noise to the output is given by the following equation.

$$QNTF(f) = | H_{STF}(f) H_{LP}(f) | \quad (2.3)$$

The two constraints that have been added to the optimization problem in 2.1 control the cancellation of the desired signal and the gain of the quantization noise respectively.

2.4. Numerical solution

Let us apply our convex optimization predictor design in 2.1 to the DAIC that we described in section 2.2. Let us assume Ntaps=32, $A_1 = -15dB, A_2 = 60dB$ in equation 2.1. We solve the convex optimization problem in 2.1 using a MATLAB-based, convex optimization solver called CVX [10]. Fig.2.8 shows the impulse response of the numerical solution of the predictor. Fig.2.9 shows the group delays of the SRF, the predictor and SRF/ predictor combined. Please note the NGD nature of the predictor in Fig.2.9.

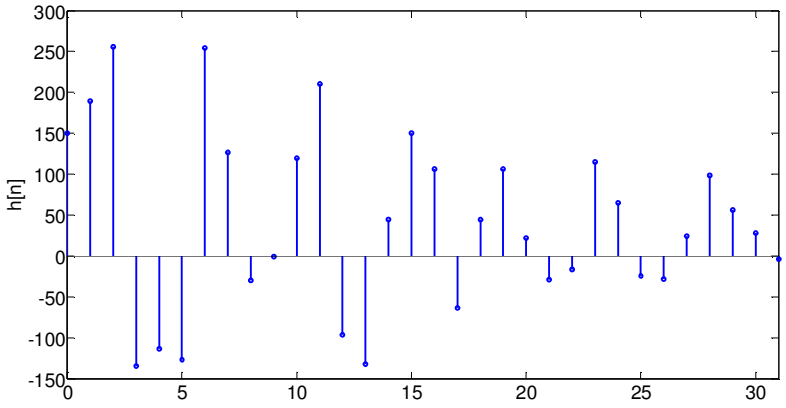


Figure 2.8 impulse response of the 32-tap FIR NGD predictor

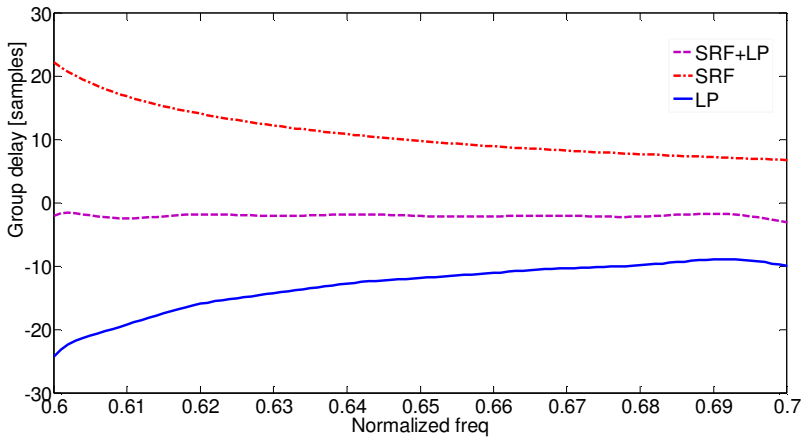


Figure 2.9 group delays of the SRF, predictor and combined SRF+ predictor in the interference band

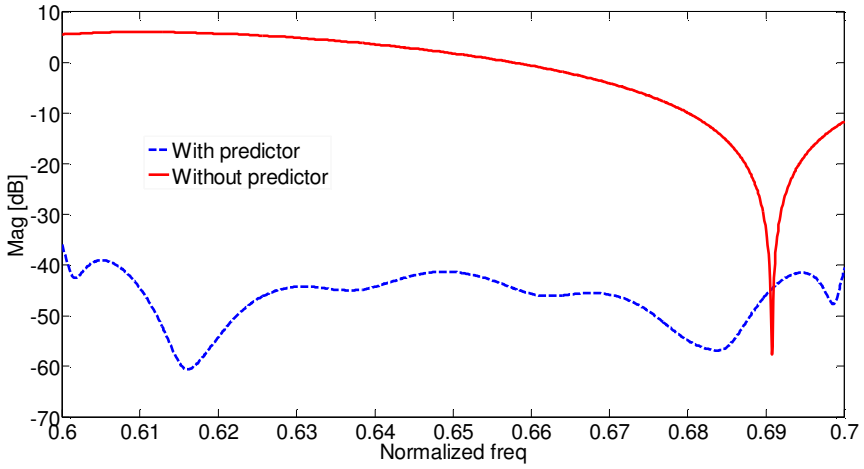


Figure 2.10 interference transfer function with and without the predictor

Fig.2.10 shows the DAIC frequency response with and without the predictor. As evident from Fig.2.10, the DAIC is only functional when the predictor is present.

Various tradeoffs exist among the parameters involved in the design of the NGD predictor and DAIC. As we mentioned in section 2.2, the predictor's gain at all frequencies should be controlled in order to control the amplification of the quantization noise. In this example we have simulated the power spectral density of interference and the DAIC output assuming 8 and 10 bit auxiliary ADCs, as depicted in Fig.2.11. As can be seen from Fig.2.11, quantization noise of the auxiliary ADC is amplified at higher frequencies. In the next section we discuss the optimal choice of parameters involved in the joint design of DAIC and predictor.

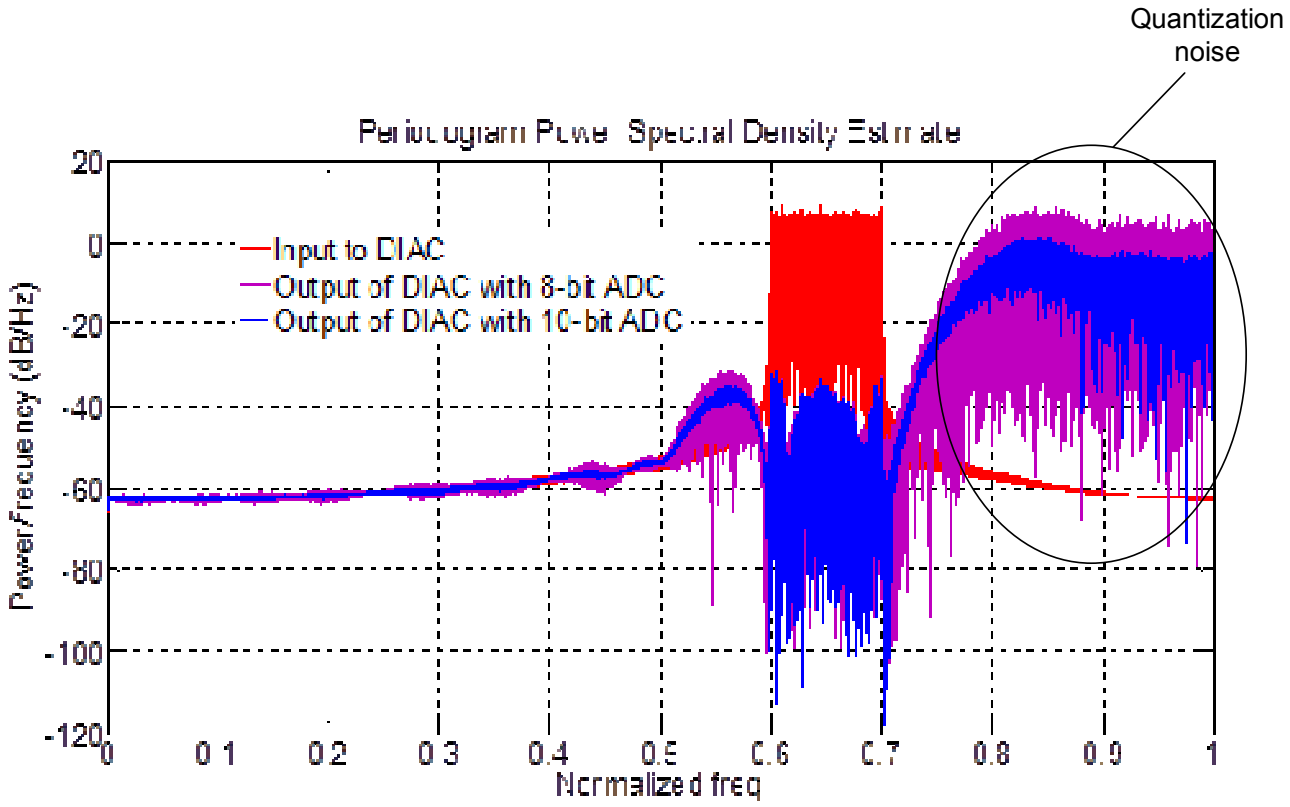


Figure 2.11 power spectral density of interference (red curve) and output of the DAIC with 8-bit (purple curve) and 10-bit (blue curve) auxiliary coarse ADC

2.5. Optimal choice of design parameters

Let us define the total "gain", G, of the DAIC as the ratio of power of the interference at DAIC's input to the power of interference at the DAIC's output (including the quantization noise). For a given SRF and data conversion latency, D, gain of the DAIC is a function of four parameters: Ntaps (number of taps of the

predictor), Nbits (number of bits of the auxiliary ADC/DAC), and A_1, A_2; the constraints of the optimization in equation 2.1.

$$G = f(Ntaps, Nbits, A_1, A_2) \quad (2.4)$$

In general, gain of the DAIC increases when Ntaps or Nbits or A_1 increases. For the constraint A_2, however, there exists an optimal value that balances the quantization noise at the output with the interference suppression ratio. Constraint A_1 is usually set by how much distortion can be tolerated on the desired signal. For the purposes of the following discussion we assume that -10dB of distortion on the signal is tolerable.

From another perspective, the energy consumption of the DAIC is determined by the Ntaps and Nbits according to the following approximate model.

$$E = \alpha N_{taps} + 2\ \beta^{Nbits} + C \quad (2.5)$$

In equation 2.5 the first term represents the energy consumption of the FIR predictor, the second term represents the energy consumption of the auxiliary ADC/DAC and the last term represents the energy consumption of the SRF. Assuming that the SIR is small at the input of the DAIC, the gross energy saving that is achieved by the DAIC is given by the following equation.

$$E' = \beta^{Nfine+\min(G,|SIR_{in}|)/6} - \beta^{Nfine} \quad (2.6)$$

In 2.6 Nfine is the required resolution of the desired signal. Therefore the total energy saving is given by the following equation.

$$\Delta E = E' - E =$$
$$\beta^{(Nfine+\min(f(Ntaps,Nbits,A_1,A_2)/6,-SIR_{in})} - (\beta^{Nfine} + \alpha N_{taps} + 2\ \beta^{Nbits} + C) \quad (2.7)$$

As can be seen from (2.7), for a given SIRin, Nfine and A_1 , total energy saving is determined by Ntaps, Nbits, and A_2.

Let us assume that Nfine=10 bits, and $A_1 = -10dB$. Also let's assume 90nm CMOS as the reference technology. Using the data in [3] and [4], we have the following approximate values for the constants: $\alpha = 10.1, \beta = 1.85$. [2]

We assume the same signal and interference bands described in section 2.2 and 2.3 example and total two samples of latency for the auxiliary ADC/DAC data conversion and SIRin. Our extensive simulations over a large set of (Ntaps, Nbits and A_2) revealed that the following setup maximized the energy saving in 2.7.

[2] Units of energies are chosen as pJ.

Table 2.2 Optimal parameters for energy saving in the example

Parameter	Optimal value for energy saving
Ntaps	64
Nbits	8
A2	40

Using the parameters in Tab.2.2, an energy saving of 230% relative to the traditional methods of using a "better" ADC can be achieved. The breakdown of the energy consumption of the DAIC and the energy saving can be found in Tab.2.3.

Table 2.3 Breakdown of DAIC energy consumption and the energy saving for the optimal setting

Component	Energy per sample [pJ]
80dB SNDR fine ADC (traditional)	3650
60dB SNDR fine ADC	470
8-bit auxiliary ADC+DAC	270
FIR predictor (64-tap)	650
IIR SRF (18-mutiplier)	180
Total DAIC (proposed)	1570
Total energy saving percentage compared to the traditional	**230%**

method	

2.6. Application of the DAIC to the mm-wave scenario

In chapter 1 of this dissertation we introduced the mm-wave link scenario that motivated us for this research. The 10GSPS ADC of the receiver needs to process strong, adjacent-channel interference in the 3-3.5 GHz band (which corresponds to the normalized interference band of F_I =[0.6,0.7]). 60dB of SNDR would normally (in absence of interference) be adequate for 10-bit resolution required by the demodulator. In presence of the interference, however, 80dB of SNDR needs to be provided by the fine ADC. This scenario is the case that we analyzed in section 2.5. We designed the DAIC using the parameters for optimal energy saving in Tab.2.2. We simulated the DAIC's input and output in time and frequency domains. Fig.2.12 shows the time-domain simulation results. As evident from Fig.2.12, DAIC significantly suppresses the interference. As a result, a 60dB SNDR ADC can provide the 10-bit resolution for the main signal. The power spectral density of the DAIC's input and output were also simulated and depicted in Fig.2.13. Also the received constellation points for an uncoded 4Gbps, QPSK modulation were simulated and depicted in Fig.2.14. **The NGD-assisted DAIC**

reduces the BER by two orders of magnitude at the power consumption cost that is 2.3 times smaller than the traditional method.

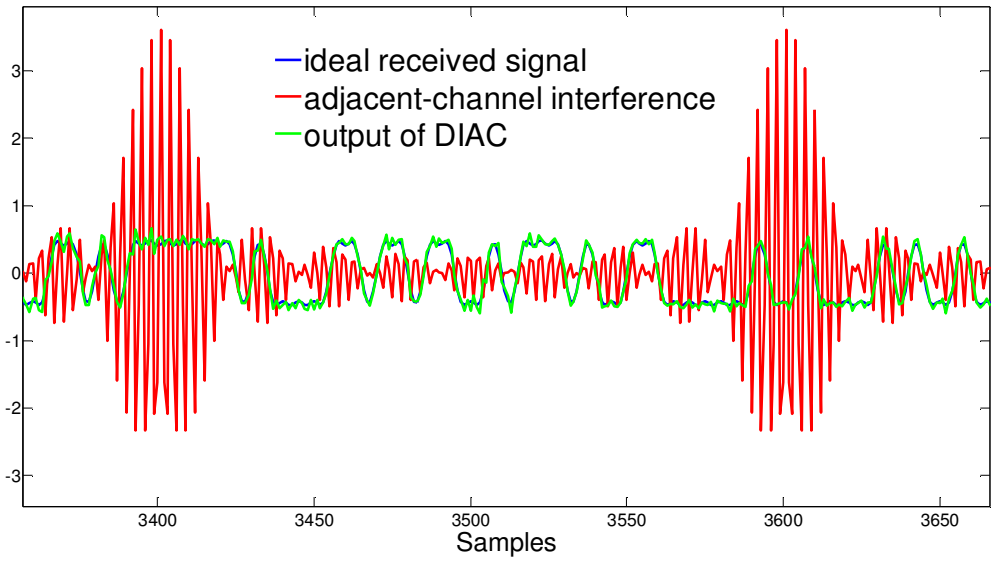


Figure 2.12 ideal received signal, adjacent-channel interference, and output of DAIC

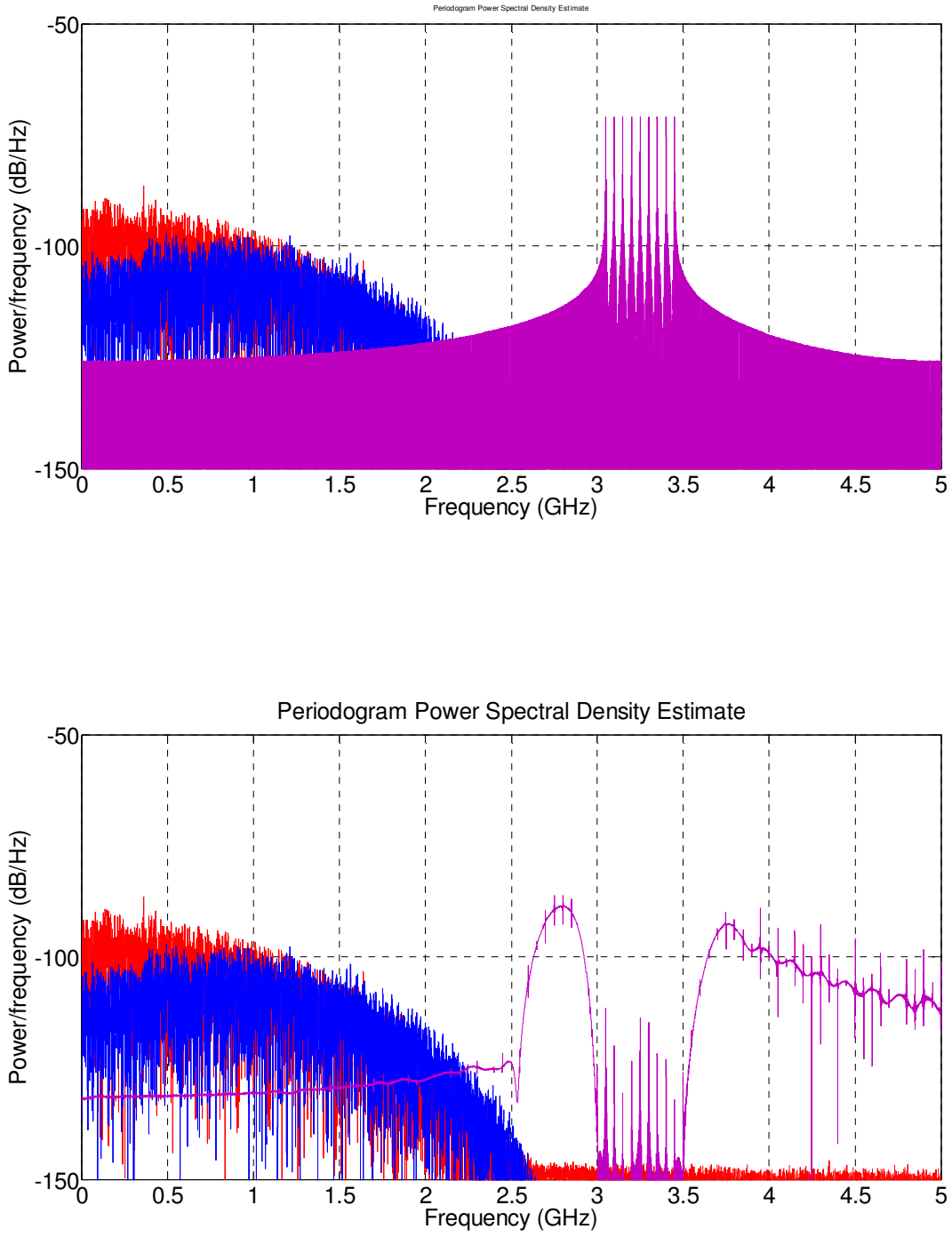


Figure 2.13 simulated spectrum for the reference scenario (top DAIC's input, bottom: DAIC's output). The red curve is the desired signal; the blue curve is the co-channel interference and the purple curve is the adjacent-channel interference

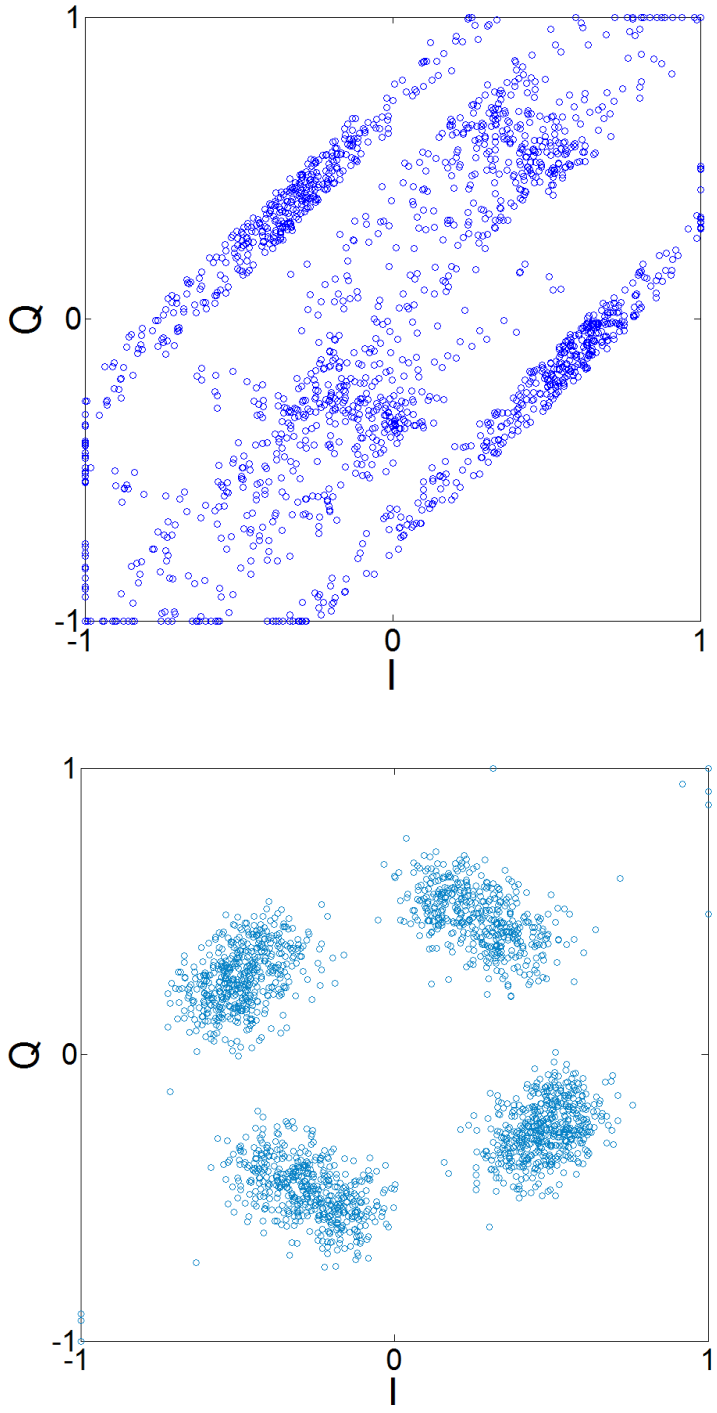


Figure 2.14 simulated received constellation points for the referenc scenario top without DAIC(BER=0.18) buttom with DAIC(BER=0.003)

2.7. Experimental results

In order to validate the NGD-assisted DIAC concept, we set up a proof-of-concept experiment using the Texas Instrument's TMS320C6713 evaluation board (EB) as the hardware platform for a DAIC. The mentioned EB is equipped with 16-bit 96KHz delta-sigma ADC and DAC and also with the TMS320C6713, digital signal processor (DSP). The SRF and the predictor were implemented on the TMS320C6713 DSP. The experimental setup is shown in Fig.2.15.

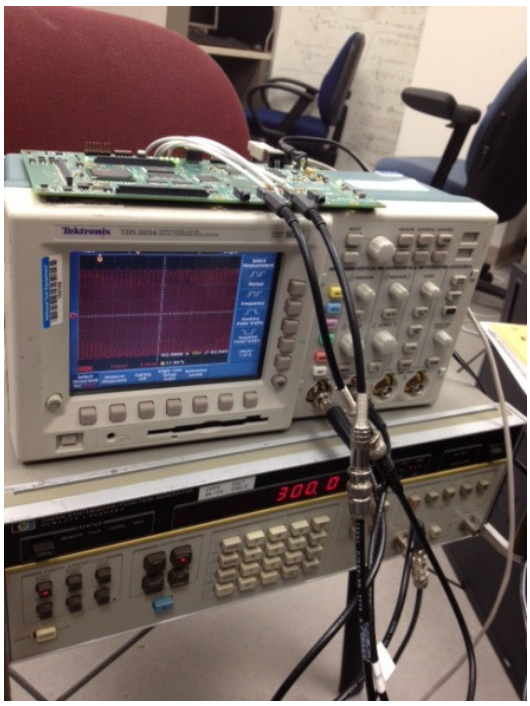
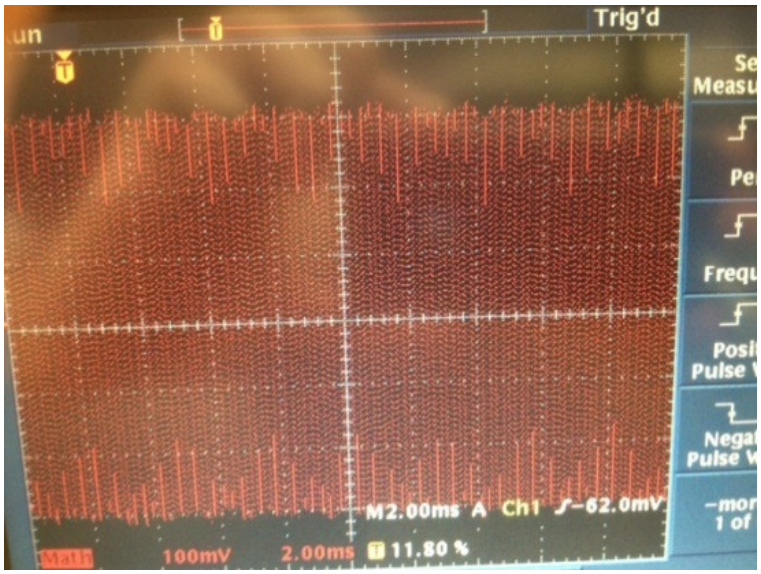


Figure 2.15 Experimental setup

.

In this experiment, a signal-interference-scenario corresponding to $(F_{I1}, F_{I2}, F_{S1}, F_{S2}) = (0.16,0.19,0,0.05,)$ was chosen. The overall latency of data-

conversion (including the group delay of anti-aliasing and image-reject filters) equals to D=32 samples. This latency is unusually high because of the frame-based data processing of the ADC on this particular DSP board. A chirp signal sweeping from f_1 =7.7KHz to f_2 = 9.2KHz with sweep time of 5 sec was used as the interference, generated by a HP 3325A signal synthesizer. Signals were captured by a 500 MHz, TDS 3054 digital oscilloscope. Figure 2.16 shows the interference signal before and after cancellation. More than 10 dB of interference suppression was achieved in our experiment. This is while, for the case that no NGD predictor was applied, no interference cancellation could be achieved.



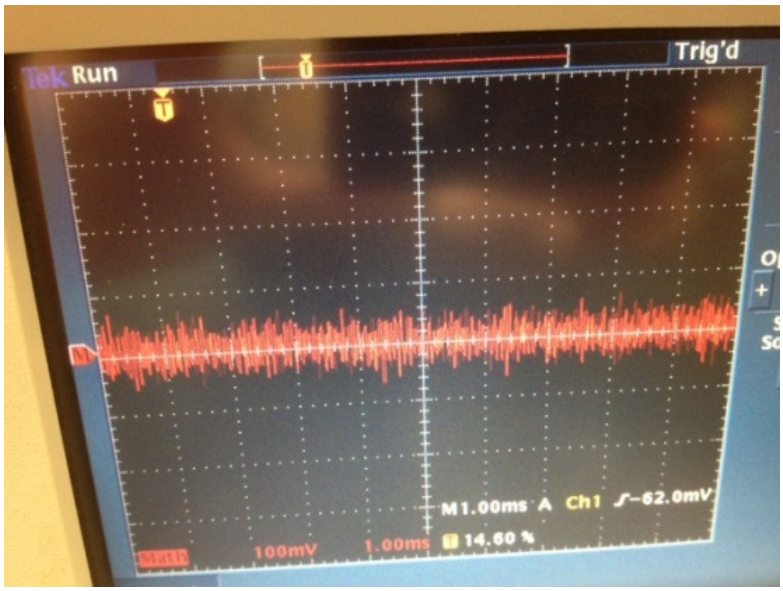


Figure 2.16 (top) interference (bottom) canceled interference

2.8. Chapter summary and conclusion

In this chapter we delved into the digitally-assisted interference cancellation (DAIC) technique. DAIC can potentially save a considerable amount of power consumption by suppressing strong and close-in interferers and henceforth reducing the required SNDR for the ADC in an interference-limited receiver. Unfortunately, however, DAIC inherently suffers from the delay mismatch issue. As we showed delay mismatch issue can completely impair the DAIC. Previous remedies for the delay mismatch issue in DAIC were scenario-specific and not power-efficient. We proposed a novel, generic and power-friendly solution to the delay mismatch issue in DAIC by using digital FIR predictor filters with negative group delay (NGD). We showed how the joint design of the DAIC and the NGD

predictor can be formulized and solved as a convex optimization problem. We also analyzed the tradeoffs amongst several design parameters and the energy saving achieved with DAIC. We then applied the proposed NGD-assisted DAIC to the mm-wave link that was described in chapter 1. We showed that NGD-assisted DAIC can reduce the BER of the link by two orders of magnitude at a power consumption cost that is 2.3 times less than the traditional method. A proof-of-concept experiment was setup to verify the validity of the NGD-assisted DIAC concept.

Glossary of abbreviations used in this chapter

ADC: analog to digital converter

BER: bit error rate

DAC: digital to analog converter

DAIC: digitally-assisted interference canceller (cancellation)

DSP: digital signal processor

FIR: finite-impulse-response

FSK: frequency shift keying

GBPS: Giga-bit per second

GSPS: Giga samples per second

IIR: infinite-impulse-response

NGD: negative group delay

QPSK: quadrature phase shift keying

SIR: signal to interference ratio

SNDR: signal to noise and distortion ratio

SRF: signal-reject filter

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Chapter 3

Assisting the frequency synthesizer in digital domain with a novel, phase noise track-and-correct system

3.1 Introduction

This chapter is devoted to the issue of phase noise in frequency synthesizers. As other analog circuits, oscillators are prone to noise. Noise that is injected to an oscillator causes random variations in both amplitude and phase of the oscillator. Amplitude variations of the oscillator in most cases are neither important nor significant [1]. Random deviations of the phase of the oscillator known as "phase noise", however, can severely affect the performance of communication systems. For detailed information regarding the underlying device and circuit mechanisms that lead to phase noise, please refer to [1].

For the purpose of this discussion we need to have a mathematical model for the phase noise in oscillators. Let us assume that an ideal oscillator has the time-

domain waveform of $V_{LO}(t) = \cos(\omega_0 t)$. Then an actual oscillator with phase noise will have the following waveform:

$$V_{LO}(t) = \cos(\omega_0 t + \phi_n(t)) \quad (3.1).$$

In equation 3.1, $\phi_n(t)$ represents the phase noise. Usually $\phi_n(t) << 1rad$ and we can make the approximation that follows.

$$\begin{gathered} V_{LO}(t) = \cos(\omega_0 t + \phi_n(t)) = \\ \cos(\omega_0 t)\cos(\phi_n(t)) - \sin(\omega_0 t)\sin(\phi_n(t)) \cong \\ \cos(\omega_0 t) - \sin(\omega_0 t)\phi_n(t) \end{gathered} \quad (3.2)$$

As a result, the spectrum of the local oscillator is the spectrum of the phase noise translated to the oscillator's frequency. The integrated rms phase noise (IRPN) of the oscillator is given by the following equations.

$$\Phi_{rms} = \sqrt{\lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \phi_n(t)^2 dt} \quad (3.3)$$

In this discussion we assume that the phase noise is a zero-mean, wide-sense-stationary (WSS) random process. If we represent the power spectral density of the phase noise by $\Phi_n(f)$, then the IRPN is also given by the following equation.

$$\Phi_{rms} = \sqrt{\int_{-\infty}^{+\infty} \Phi_n(f)df} \quad (3.4)$$

Both single-carrier and multi-carrier communication systems are adversely affected by phase noise. Please refer to [2] and [3] for reference. Albeit multi-carrier systems (e.g. orthogonal frequency division multiplexing or OFDM) and higher-order modulations (e.g. 64QAM) are often affected more severely by the phase noise.

Let us illustrate the adverse effect of the phase noise on the RF communication links by means of a simulation study. In this study, we simulate the uncoded bit error rate (BER) of a communication link that is described in Tab.3.1 with 5dB of SNR. The independent variable is the IRPN of the local oscillator. Result of this simulation is shown in Fig.3.1. As can be seen from Fig.3.1, phase noise severely affects the BER.

Table 3.1 System parameters

Carrier frequency	60 GHz
Channel bandwidth	2 GHz
Number of antennas	1
Modulation	Single-carrier 16QAM
Bit duration	0.5 nsec
Pulse shaping	Raised cosine, ROF=1
Wireless Channel	AWGN
ADC number of bits	10

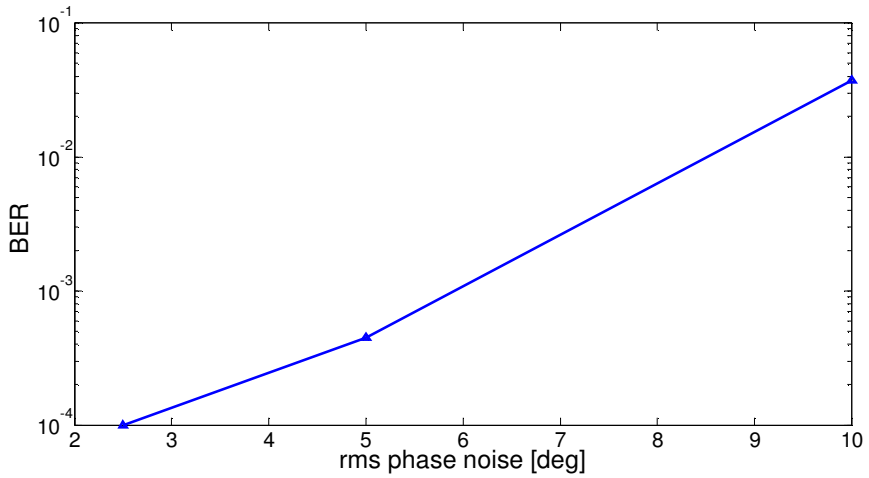

Figure 3.1 Simulated BER of 16-QAM modulation system described in Tab.3.1

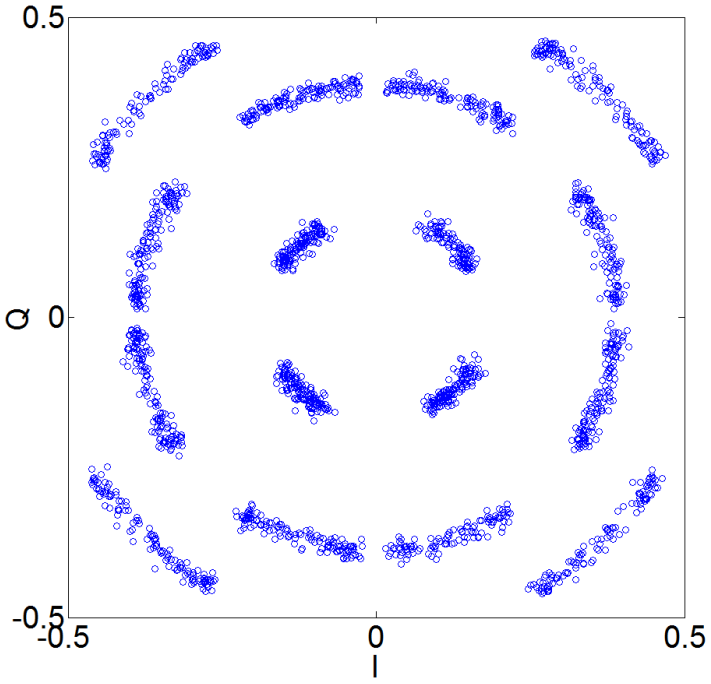

Figure 3.2 Received constellation points for a 16-QAM modulation with 10deg of rms integrated phase noise and 15dB SNR

Fig.3.2 shows the simulated received constellation diagram of the system with 15dB of SNR, in presence of 10deg rms phase noise.

3.2. Previous remedies to the phase noise issue

Numerous published works can be found which aim at alleviating the adverse effect of phase noise on communication systems. These works can be generally divided into two major categories. The first category consists of RF-domain, circuit techniques that aim at reduction of phase noise by optimizing the

frequency synthesizer block [4]-[6]. The second category, consists of algorithmic, digital-domain techniques that aim at estimation, tracking and undoing the adverse effect of phase noise [7]-[8].

The drawback of the first category mentioned above is that they usually are governed by the harsh power-noise tradeoff [1] that is shown in Fig.3.3.

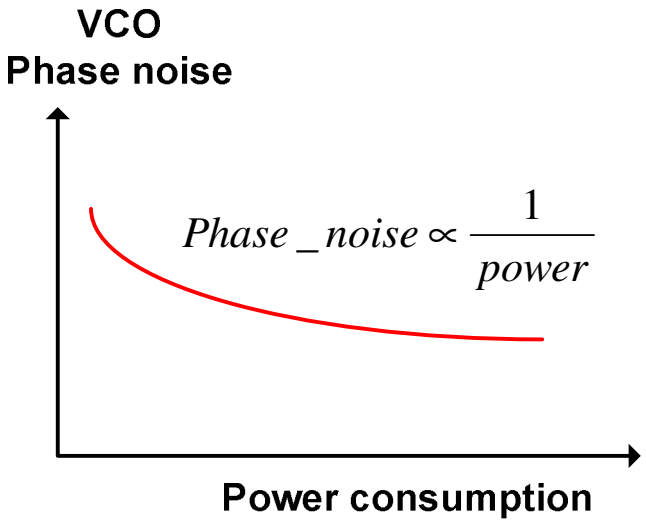

Figure 3.3 power-phase noise tradeoff

On the other hand, the second category of works mentioned above have three major limitations. First limitation is that these algorithms are usually exclusive to a specific waveform and packet structure. For example, most of these algorithms are pilot-aided [7]-[8]. Secondly, performance of these algorithms often deteriorates at lower SNR as they rely on the main receiver for phase noise

extraction. Thirdly, these algorithms are all limited to the receiver side and not on the transmitter side.

We propose a novel, cross-domain phase noise track-and-correct (PNTC) technique in this chapter. Our proposed technique, overcomes the limitations of the first and second category of phase noise suppression works mentioned above. First, due to its cross-domain (RF-digital) nature, this technique does not suffer from the harsh power-noise tradeoff. Second, as this technique tracks the phase noise independently from the main transceiver, it is generic and applicable to any waveform and packet structure. Finally, this technique can be applied to transmitters as well as receivers. Section 3.3 delves into the abovementioned, cross-domain technique.

3.3. A novel, generic, cross-domain, phase noise track-and-correct (PNTC) technique

A. general concept

Figure 3.4 shows the concept-level diagram of our proposed, cross-domain PNTC. In a nutshell, the phase noise of the local oscillator is sensed and down-converted to baseband using an auxiliary down-conversion path, is then digitized using an analog-to-digital converter (ADC) and after some signal processing is

provided to the modulator (in a transmitter) or demodulator (in a receiver) for constellation points correction.

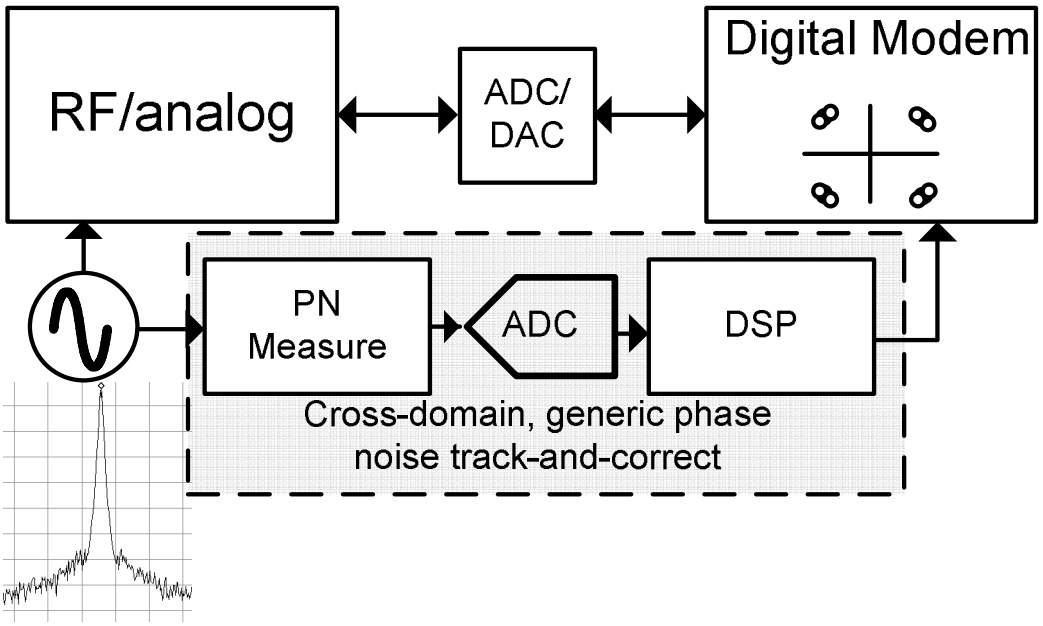

Figure 3.4 concept-level diagram of the proposed phase noise track-and-correct technique

B. frequency-discrimination mixing (FDM)

The proposed technique bypasses the harsh power-noise-tradeoff by moving to the digital domain. A prerequisite of moving to the digital domain is frequency translation to baseband. The question is how the local oscillator can be down-converted to the baseband? We proposed mixing the local oscillator with a

delayed version of itself as shown in Fig.3.5. This self-mixing technique is known as a "delay-line-frequency-discriminator" in the microwave community [9]. We call such mixing, "frequency discrimination mixing" (FDM) hereafter.

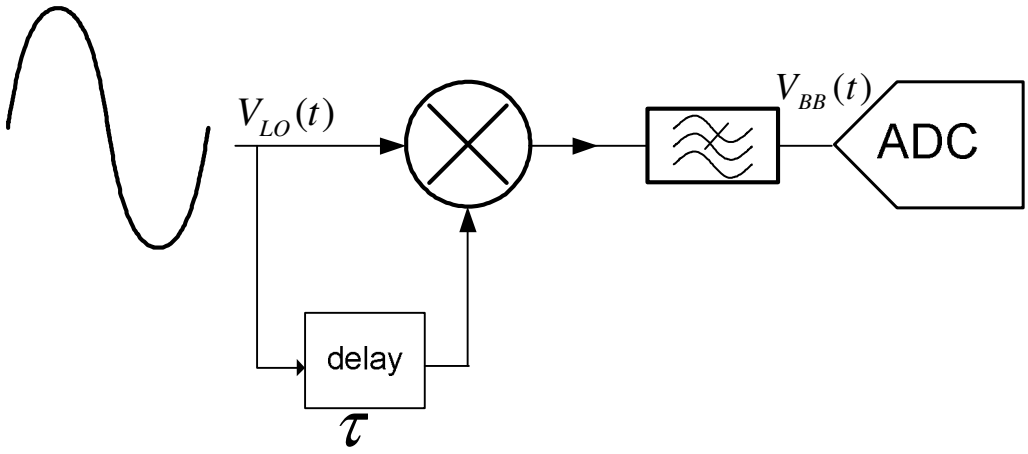

Figure 3.5 mixing the local oscillator with a delayed version of itself

Let us mathematically examine the FDM block shown in Fig.3.5. If the local oscillator's waveform is given by $V_{LO}(t) = \cos(\omega_0 t + \phi_n(t))$, then the down-converted waveform will be given by the following equation.

$$V_{BB}(t) = K\cos(\omega_0 \tau + \phi_n(t) - \phi_n(t-\tau)) \quad (3.5)$$

In equation 3.5, K is the conversion gain of the mixer. If we extract the phase of the baseband signal in 3.5, we can obtain the "differential" phase noise $\phi_n(t) - \phi_n(t-\tau)$.

Before continuing to the next subsection, however, we should mention an important issue in the DFM. The FDM is "blind" to harmonics of the frequency $1/\tau$. Consider two phase noise realizations $\phi_{n1}(t)$ and $\phi_{n2}(t)$ such that the following equation holds.

$$\phi_{n1}(t) - \phi_{n2}(t) = \sum_{k=0}^{\infty} A_k \cos(\frac{2\pi k}{\tau} t) \quad (3.6)$$

It can be shown that, the FDM does not distinguish between these two phase noise realizations.

C. complete system

The complete PNTC system for is depicted in Fig.3.6.

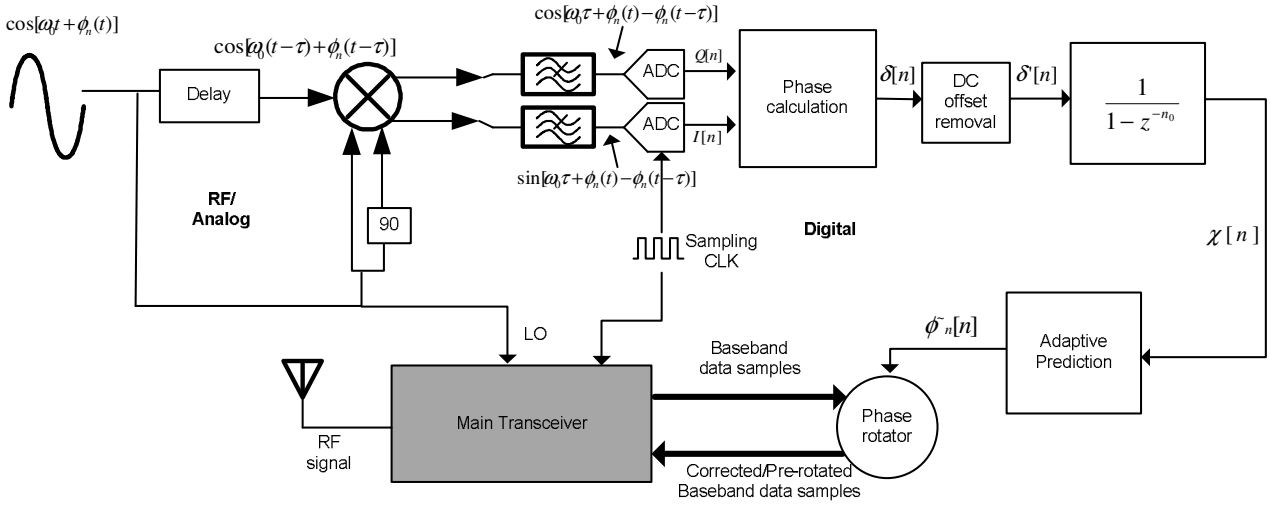

Figure 3.6 Complete phase noise track-and-correct system

The following relationships can be easily verified in the above-mentioned system.

$$I[n] = \cos[\omega_0 \tau + \phi_n(nT) - \phi_n(nT - \tau)]$$

$$Q[n] = \sin[\omega_0 \tau + \phi_n(nT) - \phi_n(nT - \tau)]$$

$$\delta'[n] = \phi_n(nT) - \phi_n(nT - n_0 T)$$

$$\delta[n] = \tan^{-1}(Q[n]/I[n]) = \omega_0 \tau + \phi_n(nT) - \phi_n(nT - n_0 T)$$

$$\Delta'(z) = (1 - z^{-n_0})\Phi_n(z)$$

In the above formulation, T is the sampling period of the phase noise-extraction ADC and $n_0 = \frac{\tau}{T}$. For the remainder of this discussion we assume $n_0 = \frac{\tau}{T} = 1$.

After the samples of the phase noise are tracked in digital domain, one may feed them to the modulator/demodulator to undo or prevent the phase noise effect on the constellation points. In a receiver, the constellation points are "de-rotated" and for a transmitter the constellation points are "pre-de-rotated". This concept is shown in Fig.3.7.

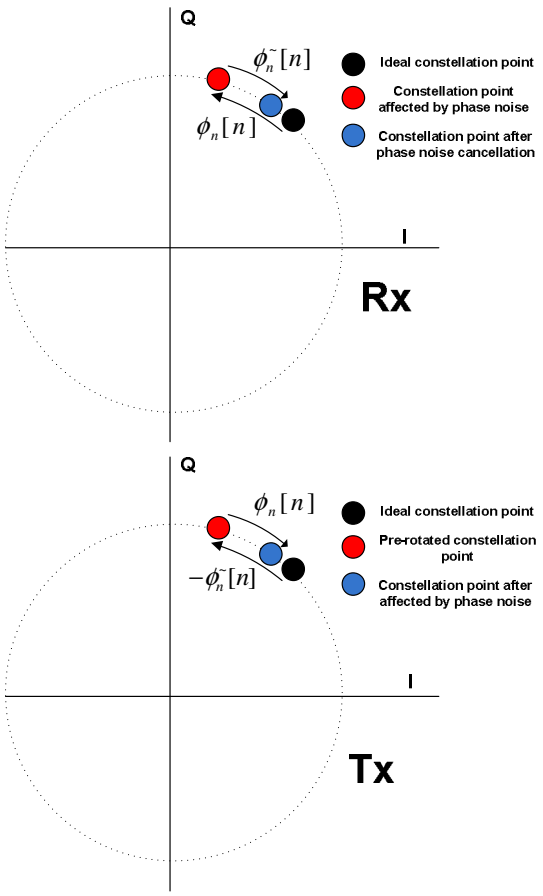

Figure 3.7 baseband correction of the constellation points based on the tracked phase noise samples in a receiver and a transmitter

One issue that may arise when the PNTC is applied to a transmitter is the latency issue. This is because by the time the pre-de-rotated baseband samples reach the up-conversion mixer, the phase noise estimate may have become outdated. Such latency can be compensated using an adaptive predictor filter, as shown in the diagram of Fig.3.6. We will come back to this issue section 3.4.

3.4. Simulation studies

We have conducted a set of simulation studies on the proposed PNTC. Throughout these simulation studies we assumed 10-bit-resolution ADCs for the PNTC and we assumed a 32-tap adaptive recursive least square (RLS) predictor. Let us first quantify the performance of the PNTC. We define the gain, G; of the PNTC as the ratio of the oscillator's phase noise power to the error of the tracking. Using the notations of Fig.3.6, we have the following definition

$$G = 10\log[\frac{Power(\phi_n)}{Power(\phi_{n-}\tilde{\phi_n})}] \quad (3.7).$$

In practice we may average the gain over many realizations of the phase noise process. In general, gain is function of five parameters: (*i*) delay of the frequency-discriminator mixing, τ , (*ii*) the SNR at the output of the FDM (which is determined by the conversion gain and noise figure of the FDM), (*iii*) the phase noise integrated rms, (*iv*) the phase noise power spectral density (PSD) profile and (*v*) the latency of the tracking.

Without loss of generality, we limit ourselves to the phase noise PSD profile shown in Fig.3.8 for the phase noise.

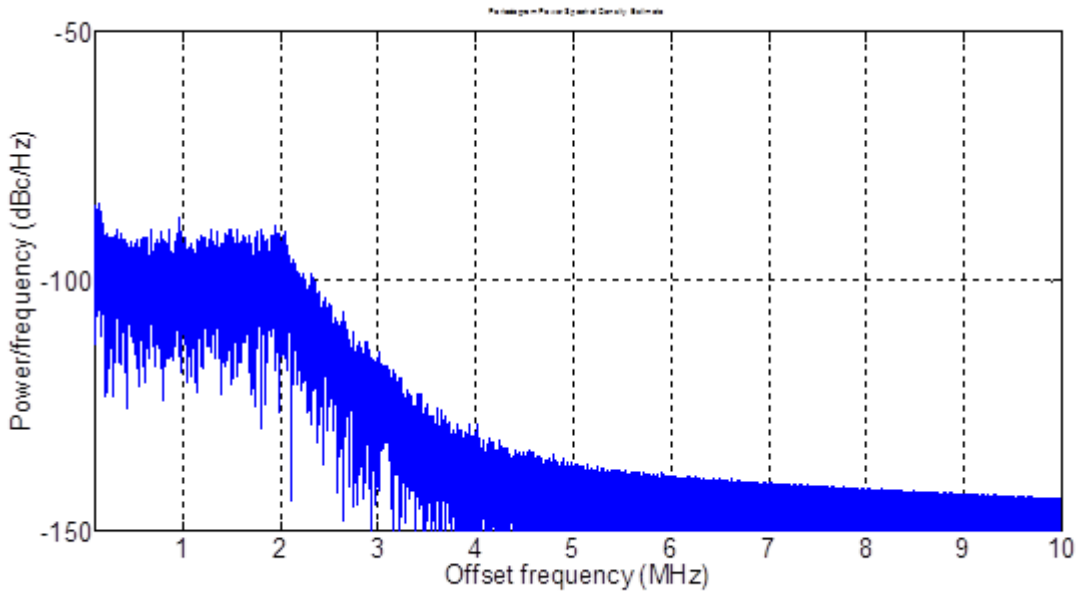

Figure 3.8 Phase noise PSD profile used in the simulation studies

A. effect of the DFM delay and DFM's noise

We observed that there exists an optimal value for the parameter τ that maximizes the gain of PNTC. The abovementioned optimal value for τ is a function of the phase noise PSD profile and also the SNR at the output of FDM. This observation can be explained by the two opposing mechanisms that affect the gain when τ changes. When τ decreases, on the one hand the "blind" frequencies of the DFM (see section 3.3.B) are pushed to higher frequencies and therefore the gain increases. On the other hand by decreasing τ, the differential phase noise and hence the signal to noise ratio of the DFM decreases.

For a given PSD profile, we expect the optimal value of the τ to increase for lower DFM's output SNR. Figure 3.9 shows the simulated gain of PNTC for three different SNR values for the DFM as a function of DFM's delay. As evident from the Fig.3.8, the optimal value for the delay increases as the SNR decreases.

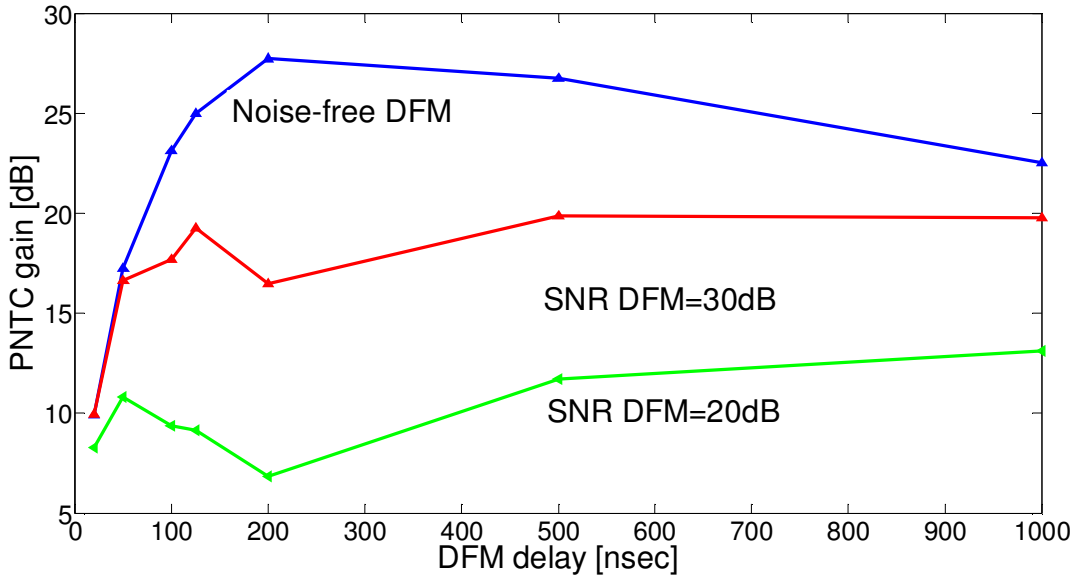

Figure 3.9 Effect of the DFM's delay and SNR on the PNTC's gain

B. effect of phase noise integrated rms

In general, higher IRPN leads to higher gain for the PNTC. This is because the differential phase noise increases for higher integrated phase noise rms. Figure 3.10 shows the PNTC gain as a function of the IRPN for two DFM SNR values.

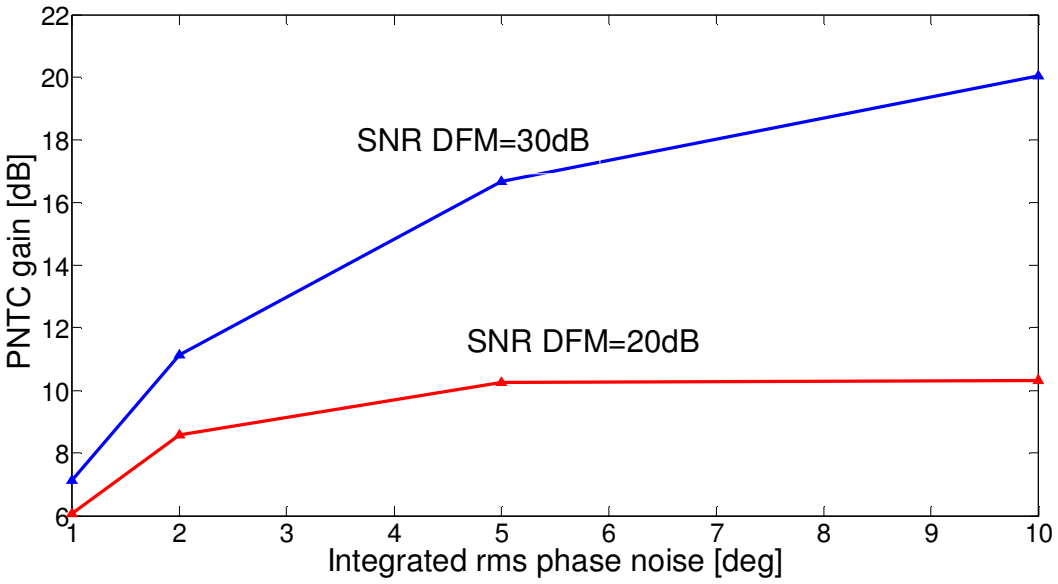

Figure 3.10 Effect of the phase noise integrated rms on the PNTC's gain

C. Effect of latency

As described in the previous section, the latency associated with the PNTC may make the phase noise estimates outdated. Such issue is more concerning in a transmitter as depicted in Fig.3.11. The abovementioned latency can be alleviated using an adaptive predictive filter. Figure 3.12

shows the result of a simulation study. In this simulation study, we used a 32-tap RLS predictor filter. Regarding the relatively low sampling rate (one to a few MHz) that is used for the PNTC, the amount of latency will be limited to one or two samples.

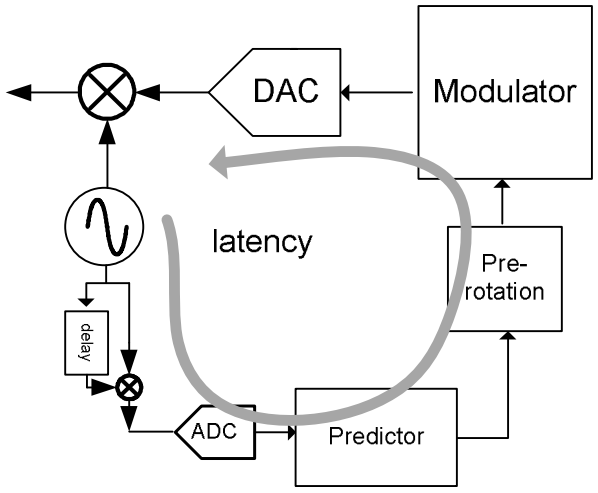

Figure 3.11 using an adaptive predictor to overcome the latency issue when applying the PNTC to a transmitter

Fig.3.12 shows the PNTC gain for one-sample latency under 30dB DFM SNR and 10degree IRPN with and without the adaptive predictor for different DFM delay values.

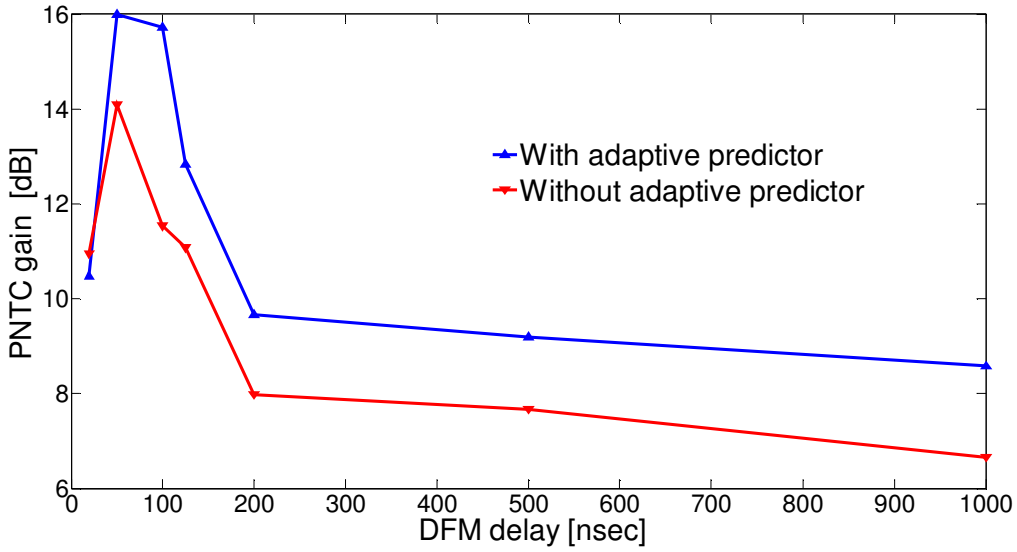

Figure 3.12 PNTC gain for one-sample latency under 30dB DFM SNR and 10degree integrated rms phase noise with and without the adaptive predictor for different DFM delay values

3.5. Application of PNTC to the mm-wave scenario

In this section we apply the proposed PNTC to the mm-wave scenario that was introduced in chapter1. Unfortunately, as the frequency of semiconductor oscillators increases so does their phase noise. This is because in a given semiconductor technology the available power of the transistors drops at higher frequency while the amount of noise increases. As such, the main carrier becomes weaker at higher frequencies while its noise skirt becomes stronger. A typical 60 GHz local oscillator in CMOS technology may exhibit 5-10 degree of IRPN. The

following table summarizes the IRPN and power consumption of a few, recently-reported frequency synthesizers in the 60 GHz band.

Table 3.2 Performance of a few, recently-reported 60 GHz frequency synthesizers

Reference number	**Calculated approximate integrated phase noise rms [deg][3]**	**Reported power consumption [mW]**	**Device technology**
10	7	161	SiGe 130nm
11	7	80	CMOS 90nm
12	8	72	CMOS 130nm

According to our simulation studies in the previous section, for a typical 7 degree rms IRPN, and under realistic assumptions of one sample latency, 20 dB of SNR at the output of the FDM and with 100nsec of FDM delay, one can suppress the effective phase noise by 10dB (i.e. effective phase noise of 2.2 degrees integrated rms after suppression). On the other hand, according to our link simulations in Fig.3.1, such phase noise reduction leads to an order of magnitude of reduction in BER for a 16QAM modulation.

[3] Total phase noises were calculated roughly based on the measurement PSD

Reducing the phase noise power by a factor of 10 using the traditional approach with the power-noise tradeoff shown in Fig.3.3 requires a 10x increase in the power consumption of the frequency synthesizer. A typical mm-wave frequency synthesizer consumes 80mW of power in 90nm CMOS. We estimate the power consumption of a typical PNTC with 10MSP, 10-bit ADC processing to be on the order of 20mW in 90nm CMOS according to the following table. Therefore one can achieve **an order of magnitude improvement in the BER with order of magnitude smaller power consumption than required by the traditional approach.**

Table 3.3 power consumption estimation of the PNTC and power saving achieved compared to traditional approach

Component	**Estimated power consumption in 90nm CMOS [mW]**
Conceptual 2.2 degree IRPN frequency synthesizer (traditional)	800
7 degree IRPN frequency synthesizer	80
2x10-bit auxiliary ADC@10MSPS [15]	5
Down-conversion mixer [13]	7
Digital processing (dominated by the 32-tap adaptive RLS predictor)	10
Total PNTC and 7-degree IRPN frequency synthesizer power consumption (proposed)	102
Total energy saving percentage compared to the traditional method	**800%**

3.6 Implementation considerations

The only hardware blocks in PNTC that we have so far assumed an idealistic model for are the RF delay component in the FDM and the sampling clock. In this

section, we briefly comment on the implementation aspects of these two hardware blocks.

A. Sampling clock jitter

Fortunately the effect of sampling clock jitter can be precluded by "coupling" the clock of the main transceiver with that of the PNTC as shown in Fig.3.6.

B. Delay element of the FDM

The FDM in Figure 3.5 requires an RF delay element. One may implement such delay element with a chain of inverters for lower frequency oscillators (few GHz) [14]. For mm-wave frequencies, however, a passive delay is required. Fortunately since the oscillator and phase noise are narrowband, high quality factor, passive resonance structure can be used to implement the delay [1].

3.7. Chapter summary and conclusion

In this chapter we first briefly reviewed adverse effects of the oscillator's phase noise on the performance of RF communication systems. We then introduced a novel, cross-domain technique called phase noise track and correct (PNTC). We showed that by using PNTC one can achieve an order of magnitude reduction in the phase noise at a negligible additional power consumption cost compared to the traditional methods. We also showed that unlike previous remedies for the phase noise, PNTC is applicable to any modulation and waveform and to both transmitter and receiver sides. We also reviewed the effect of different design parameters on the performance gain of the PNTC.

Glossary of abbreviations used in this chapter

ADC: analog to digital converter

BER: bit error rate

FDM frequency discrimination mixing

IRPN integrated rms phase noise

MSPS: Mega samples per second

PNTC phase noise track and correct

RLS recursive lease square

SNR: signal to noise ratio

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Chapter 4

Assisting the antenna array in analog baseband domain with a low-power baseband time-alignment technique

4.1. Introduction

This chapter is devoted to the antenna arrays. Electronically-steerable antenna arrays were first utilized in the military radar systems. Military antenna arrays usually employ thousands of antenna elements. The reason for using such large antenna arrays is that very long ranges of directional communication requires very fine spatial resolution and spatial resolution of an antenna array is inversely proportional to the number of elements.

There has been a recent trend of integration of phase-arrays on silicon at mm-waves [1]-[4] for commercial applications. Small wavelength at mm-waves makes it possible to integrate the transceiver, beamforming network and even the antennas on the same chip. Such integration drastically reduces the cost of the antenna arrays for commercial applications.

In the proposed commercial applications for antenna arrays, however, the target ranges are relatively short; from few meters in a wireless personal area network (WPAN) to hundreds of meters in mm-wave backhaul networks. As such, smaller-size arrays (from 4 to 64-element) is usually adequate in commercial applications.

There are multiple benefits in using an antenna array. Besides a gain in the SNR, one major benefit is the "spatial filtering" achieved by using the antenna array. The radiation pattern of an antenna array is spatially selective. A selective radiation pattern can significantly mitigate interference by rejecting interferers that impinge on the receiver from different angles than that of the desired signal as shown in Fig.4.1.

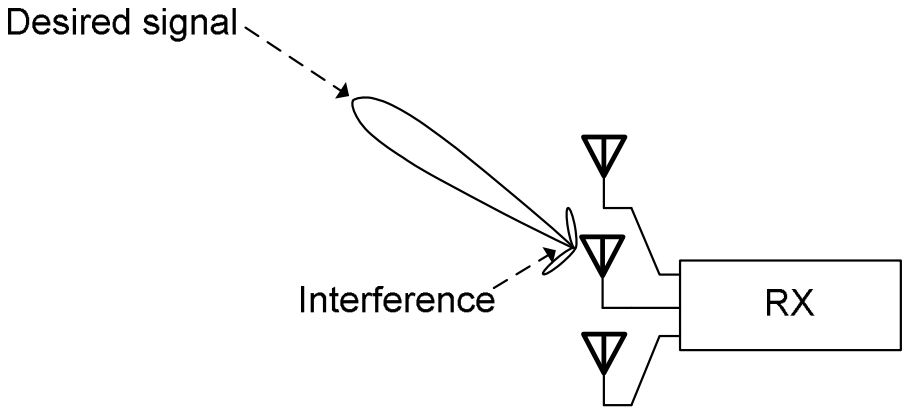

Figure 4.1 Interference -rejection through spatial filtering in an antenna array

Ideally, in a line-of-sight (LOS) communication link, the array function is achieved through introduction of tunable time delays in the path of antenna

elements to compensate for the difference of travel times to or from different antenna elements, as shown in Fig.4.2. Such antenna array is sometimes referred to as "timed-array" [5].

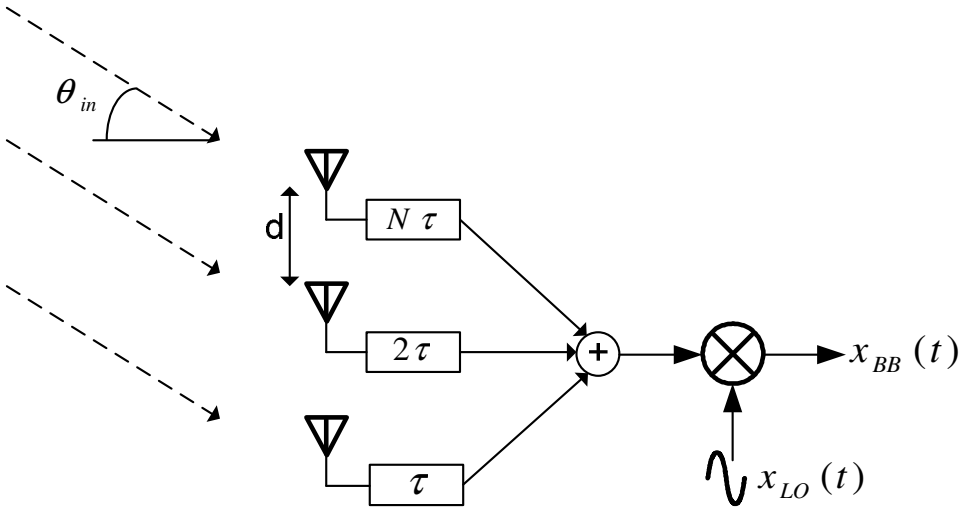

Figure 4.2 timed-array

If we represent the RF incident signal on the first antenna of an N-element, uniform linear array[4] by $x(t) = x_0(t)\cos(\omega_0 t)$, then one can show that if $\tau = \frac{d\sin(\theta_{in})}{c}$, [5]and $x_{LO}(t) = \cos(\omega_0(t - N\tau))$, then the following relationship exists between the baseband output of the array and the baseband envelope of the incident signal.

$$x_{BB}(t) = K_m N x_0(t - N\tau) \quad (4.1)$$

[4] All the antenna arrays in this chapter are uniform linear arrays even if not explicitly declared

[5] d is the spacing between consecutive antenna elements, c is the speed of electromagnetic waves . Unless otherwise stated we always assume that the antenna spacing is half of the wavelength at the center frequency of operation

In (5.1), K_m is the conversion gain of the mixer. As evident from equation 4.1, timed-array's baseband output is a scaled and delayed version of the original baseband signal.

From another perspective, for a given choice of delay τ, one can derive the array gain as a function of incidence angle and frequency of the baseband signal. Let us assume that the incident signal on the first antenna is $x(t) = \cos(\omega_{BB} t + \omega_0 t)$. Therefore the incident signal on the i'th antenna element will be given by $x(t-(i-1)\frac{d\sin(\theta_{in})}{c})$. The signal at the output of the combiner will be given by the $S(t) = \sum_{i=1}^{N} x(t-(i-1)\frac{d\sin(\theta_{in})}{c} - (N+1-i)\tau)$. It can be shown that, in such case:

$$x_{BB}(t) = K_m G(\theta_{in}, \tau, \omega_{BB}) \cos(\omega_{BB} t)$$

$$G(\theta_{in}, \tau, \omega_{BB}) = \frac{\sin(\frac{N}{2}(\omega_{BB} + \omega_{LO})(\frac{d\sin(\theta_{in})}{c} - \tau))}{\sin((\frac{1}{2}\omega_{BB} + \omega_{LO})(\frac{d\sin(\theta_{in})}{c} - \tau))} \quad (4.2)$$

In (4.2), G is the array gain.

For narrowband systems, the delay elements in the timed-array are usually approximated with phase shifters. Such approximation is mainly because it is much easier to build narrowband phase shifters than wideband tunable delay elements. In particular, wideband, tunable delay elements are difficult to build in

silicon [6]. The antenna array that is resulted from using phase shifters is called a "phased- array". A Phased-array is shown in Fig.4.3. It can be shown that for a phased-array the array gain is given by the equation (4.3).

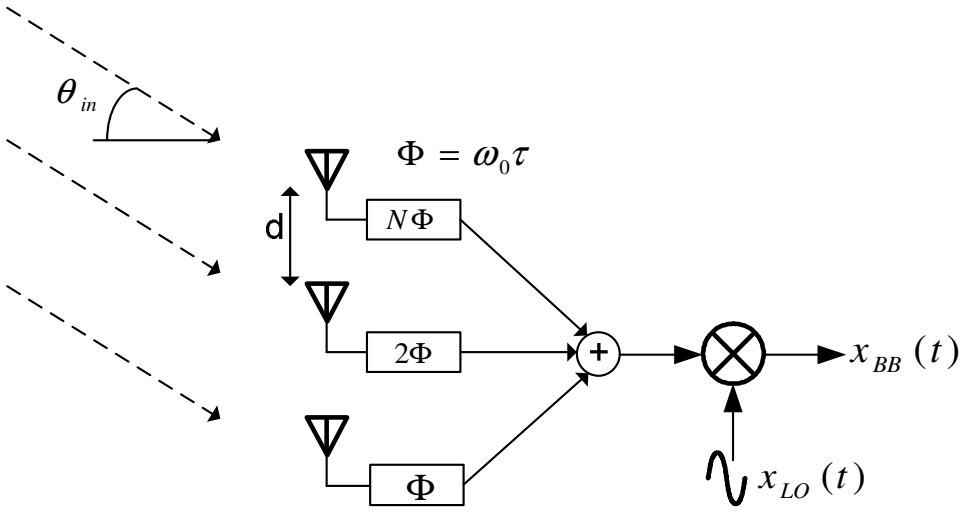

Figure 4.3 phased-array

$$x_{BB}(t) = K_m G(\theta_{in}, \tau, \omega_{BB}) \cos(\omega_{BB} t)$$

$$G(\theta_{in}, \tau, \omega_{BB}) = \frac{\sin(\frac{N}{2}(\omega_{BB} + \omega_{LO})\frac{d\sin(\theta_{in})}{c} - \frac{N}{2}\Phi))}{\sin(\frac{1}{2}(\omega_{BB} + \omega_{LO})\frac{d\sin(\theta_{in})}{c} - \frac{1}{2}\Phi))} \quad (4.3)$$

Depending on where the phase shifting operation is performed, integrated phased-arrays can be implemented in different architectures such as RF

beamforming, LO beamforming, baseband-analog beamforming and digital beamforming. Figure 4.4 shows these different architectures.

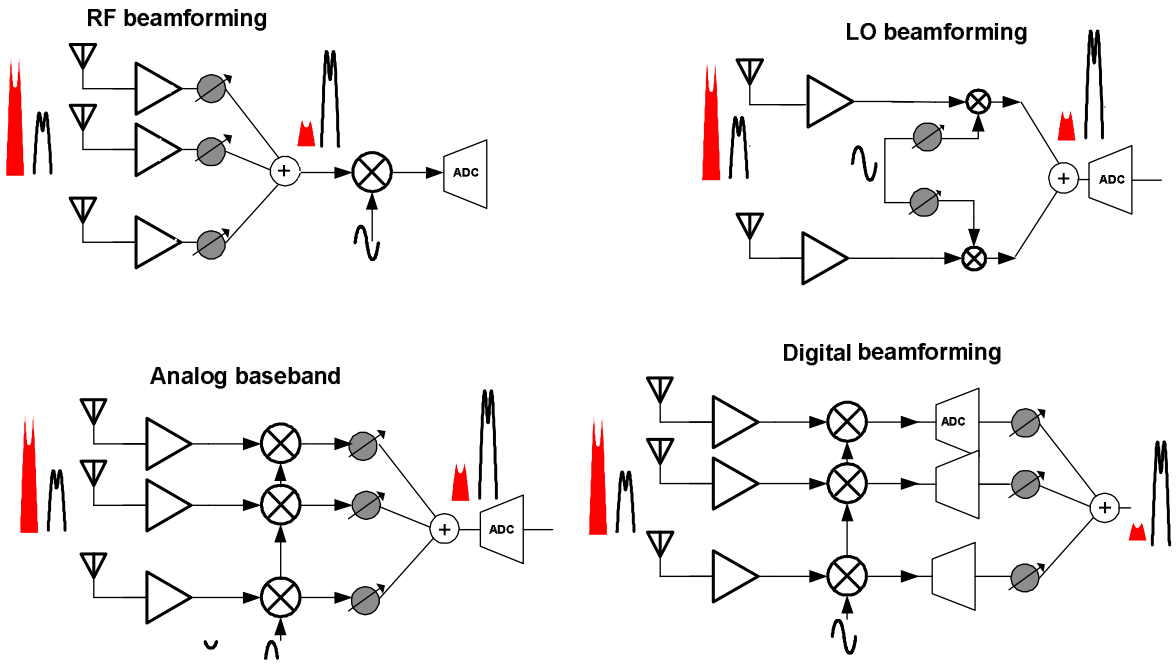

Figure 4.4 integrated phased-array architectures

In high data rate applications, digital beamforming requires several high-speed and high dynamic range ADCs and hence is very power-unfriendly. On the other hand since the phase shifting operation is done in the signal path in the RF beamforming architecture, extra noise and/or distortion is introduced to the signal which in turn reduces the dynamic range of the receiver. LO beamforming, proposed in [2], overcomes this issue by performing the phase shifting operation in

the LO path. LO beamforming architecture offers the best tradeoff between, interference cancelation capability, power consumption and area [6]. For the rest of this chapter we focus on the LO beamforming architecture, that is shown in Fig.4.5. It can be shown [6] that the baseband output of the array in Fig.4.5 is the same as the array in Fig.4.3.

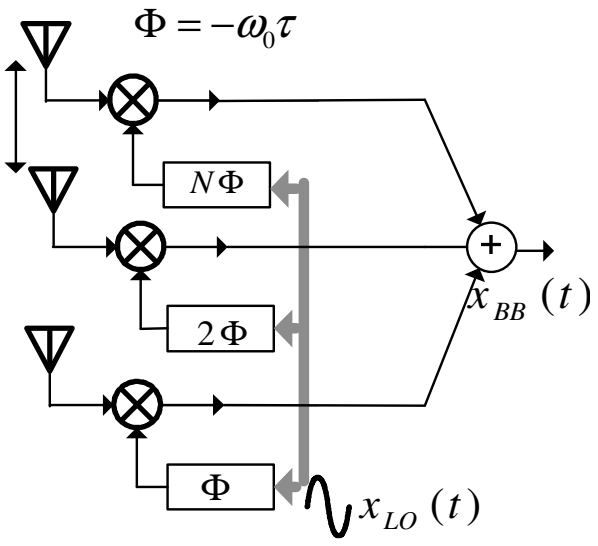

Figure 4.5 LO beamforming phased-array architecture

4.2. Beam-squinting and array-induced frequency fading issues

Phased-array approximation of timed-array is a hardware-friendly approach especially when the phased-array is implemented as the LO beamforming architecture. For 60 GHz applications with 2 GHz channels, the above-mentioned approximation works almost perfectly for small array sizes (4-8 elements).

Unfortunately, however, we found that for a medium-size array (32-64 elements), phase shift approximation causes two issues: beam-squinting and array-induced frequency fading. In this section we will quantify these two issues.

A. Array-induced frequency fading

Let us assume that the desired signal is impinging on the array from a given angle θ_{in}. Ideally, we would like the antenna array to exhibit a frequency-flat response in the direction θ_{in}. Unfortunately, however, phased-array introduces a frequency-selective response. We call this impairment "array-induced frequency fading" For example, Fig.4.6 shows the array-induced frequency fading for θ_{in}=90 degree in 16, 32, 64-element phased-array.

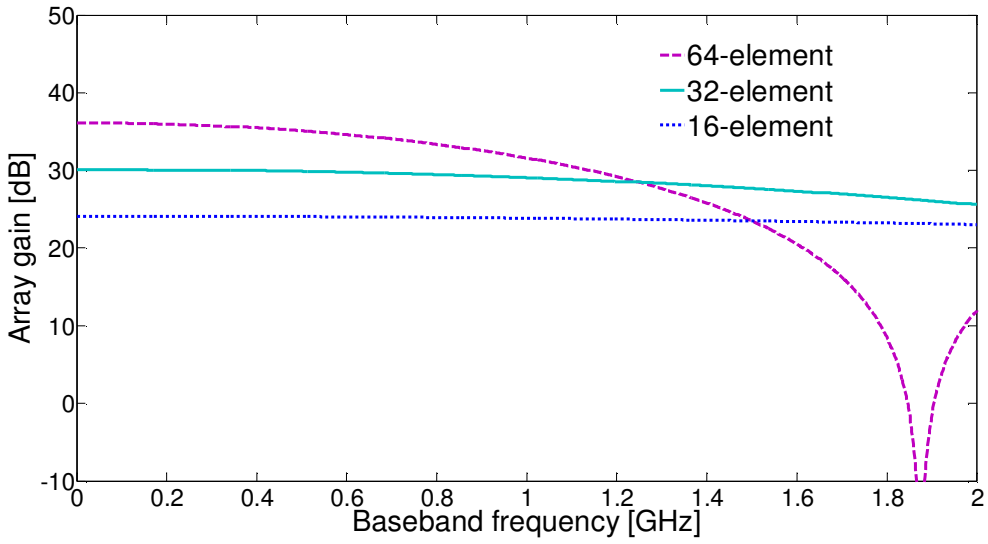

Figure 4.6 array-induced frequency fading for θ_{in}=90 degree in 16, 32, 64-element phased-arrays

If the array-induced fading is not severe inside the channel (for example for 32-element or smaller array), one may consider lumping the array-induced frequency fading and wireless channel's frequency response and compensate for the lumped frequency fading using a channel equalizer. For sever fading, such as the 64-element antenna array, however, even a channel equalizer might not be helpful.

Fig.4.7 shows the worst case, 50%-coherence bandwidth [7] of 60 GHz phased-arrays of different sizes. Worst case occurs when the array is set for the desired direction of θ_{in}=90.

Figure 4.8 shows received modulation for 5dB SNR, 16-QAM, 64-antenna phased-array versus timed-array for θ_{in}=90

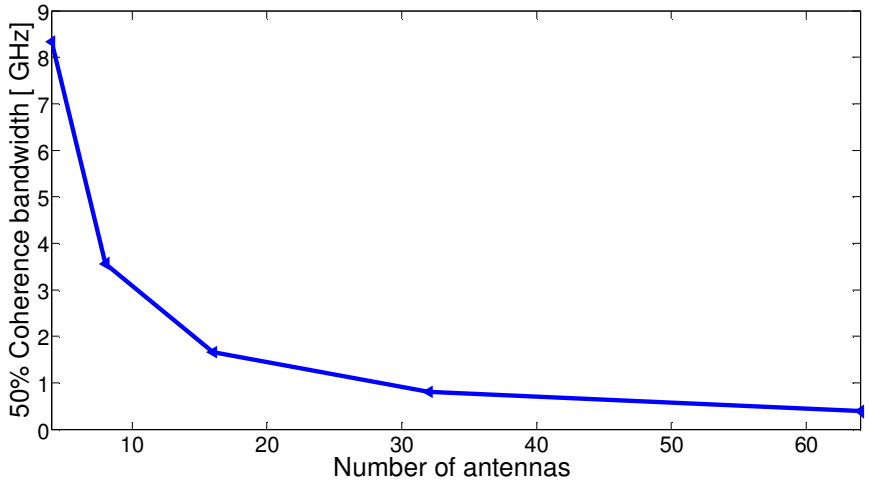

Figure 4.7 50%-coherence bandwidth of 60 GHz phased-arrays

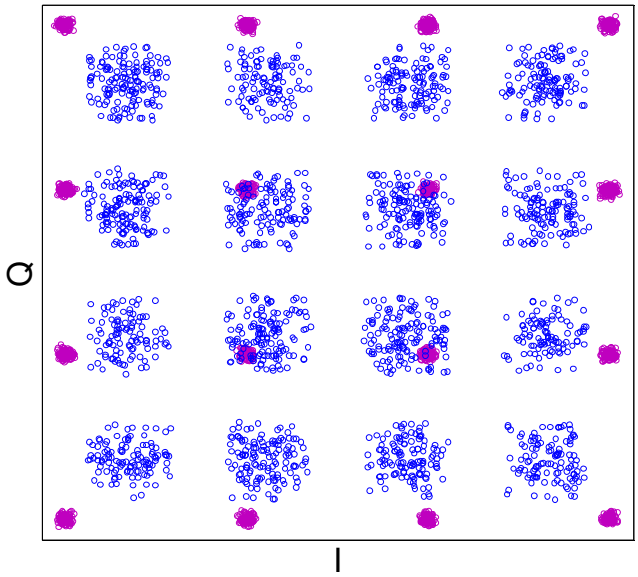

Figure 4.8 received modulation 5dB SNR at each antenna, 16-QAM, 64-antenna phased-array (blue) versus timed-array (purple)

B. Beam squinting

Beam squinting [13] is another issue in a phased-array. Unlike a timed-array that exhibits a fairly frequency-independent radiation pattern, phased-array's radiation pattern is frequency-dependent. For example, Fig.4.9 compares the radiation patterns of a 64-element phased-array and timed-array at two frequencies of 60 and 62 GHz (two edges of a 2-GHz channel). As evident from Fig.4.9, timed-array's radiation pattern is very similar at the two ends of the channel. Phased-array's radiation pattern, however, experiences a drastic shift from 60 GHz to 62 GHz. For

example, the direction of maximum gain of the phased-array moves from 90 degree to 75 degree at 62GHz, which is a beam null at 60GHz. Figure 4.10 shows the color-coded two-dimensional array gain of a 64-element phased-array versus timed-array.

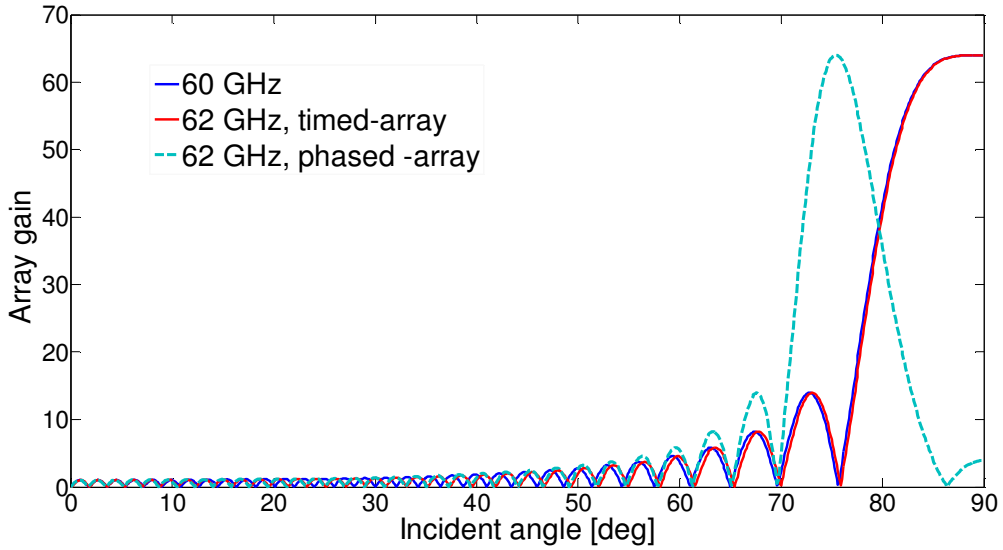

Figure 4.9 radiation patterns of a 64-element phased-array and timed-array at two frequencies of 60 and 62 GHz (edges of a 2 GHz channel)

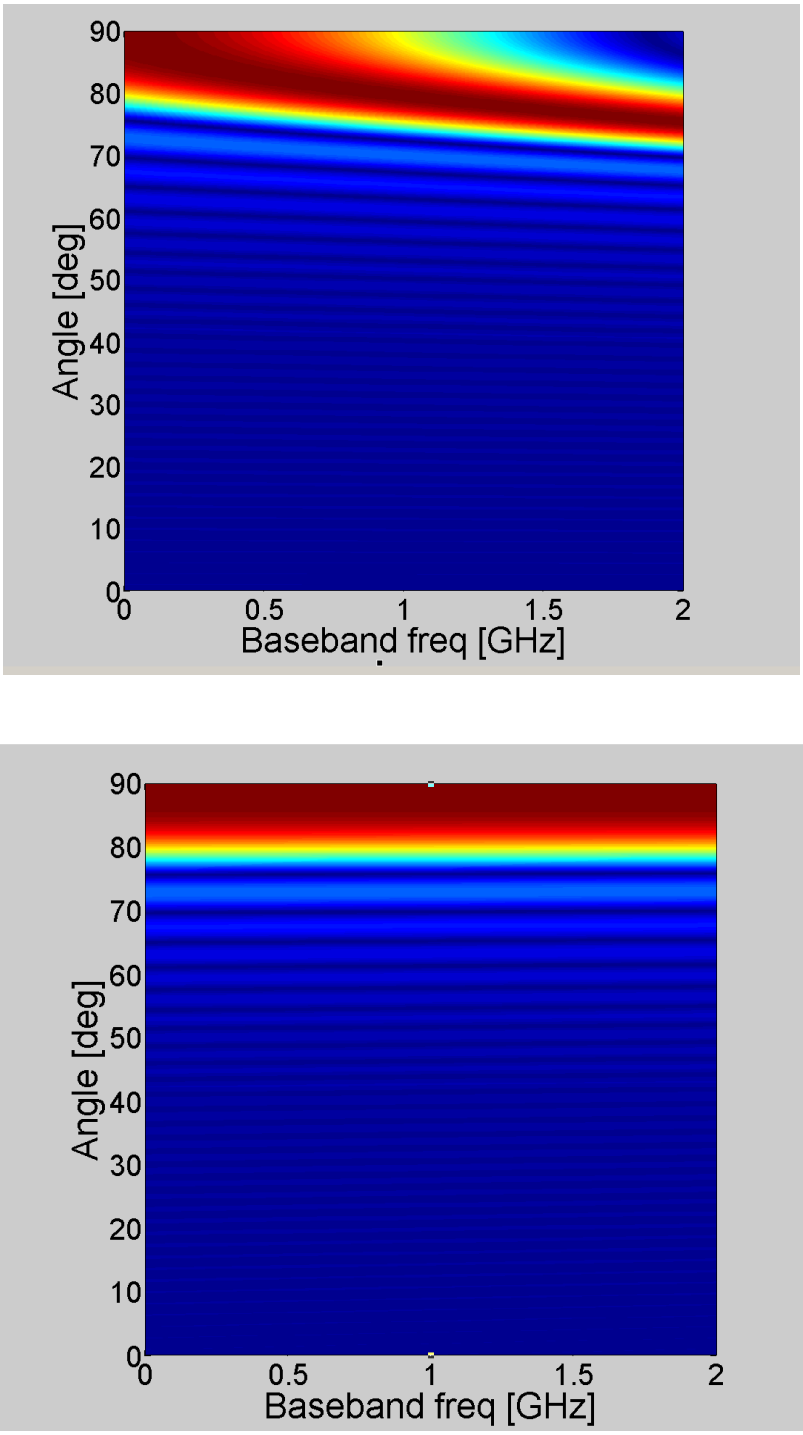

Figure 4.10 color-coded, two-dimensional array gain of a 64-element phased-array (top) versus timed-array (bottom)

Let us show the effect of the beam squinting and array-induced frequency fading on the communication link performance. Consider a scenario in which, a co-channel interferer is impinging on the antenna array from $\theta_{in} = 60$ degree and the signal to interference ratio (SIR) is 0dB. Assuming 16-QAM modulation and 5dB SNR at the antenna, Fig.4.11 shows the BER versus the number of antennas. Surprisingly the BER deteriorates when the number of antennas increases from 32 to 64 despite the increase in the SNR gain of the array! The reason for such unexpected increase in the BER for 64-element arrays is the two impairments mentioned above.

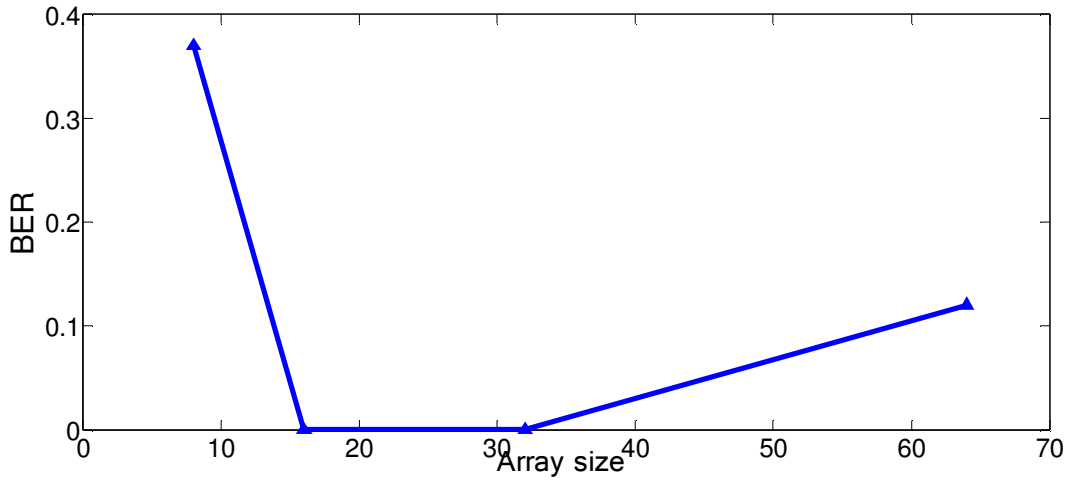

Figure 4.11 BER versus the number of antennas assuming 16-QAM modulation and 5dB SNR at the antenna and an interference impinging on the array from $\theta_{in} = 60$ with SIR=0dB

4.3 The proposed cross-domain solution

Unfortunately as we saw in section 4.2, the hardware-friendly LO beamforming fails for larger-size arrays due to array-induced frequency fading and also due to beam squinting. Two approaches can be imagined to overcome this problem. Traditional approach would prescribe using a timed-array as depicted in Fig.4.2. We will show that such approach would lead to an unnecessarily high amount of power consumption.

As a power-friendly alternative, we propose the following novel array architecture. The proposed architecture is LO-beamforming with analog baseband time alignment (BTA) assistance. It can be easily shown that the proposed architecture is mathematically equivalent to the original timed-array. As we will show, by means of real-life examples, however, the proposed architecture is much more power-friendly than the traditional timed-array counterpart. Intuitively, the reason for power-friendliness of the proposed architecture is shifting the problem of time-misalignment between the array channels to the analog baseband.

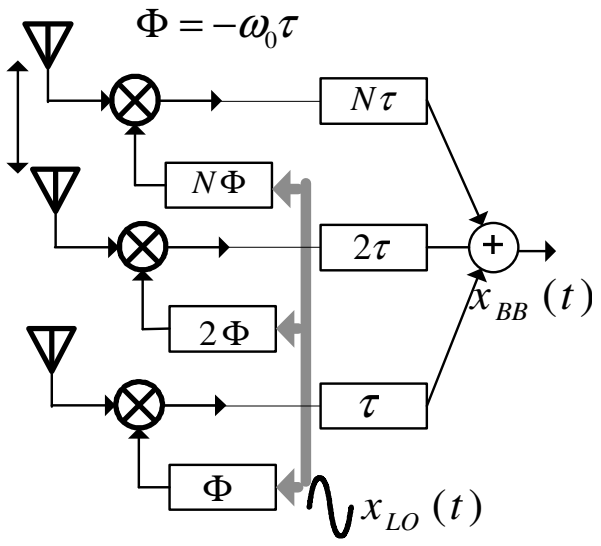

Figure 4.12 proposed novel array architecture: LO-beamforming with analog baseband time alignment assistance

4.4. Application of BTA to the mm-wave scenario

We applied the proposed BTA to the mm-wave scenario introduced in chapter 1. In our simulation, the delays are quantized to multiples of 1psec. Figure 4.13 shows the simulation results for a 64-element antenna array with 5dB SNR at the antenna and 16-QAM modulation. The BER is depicted as a function of the SIR. It has been assumed that an interference is impinging on the array from an angle $\theta_{in} = 60$. As can be seen from the figure, BTA-assisted array has orders of magnitude smaller BER at the same SIR.

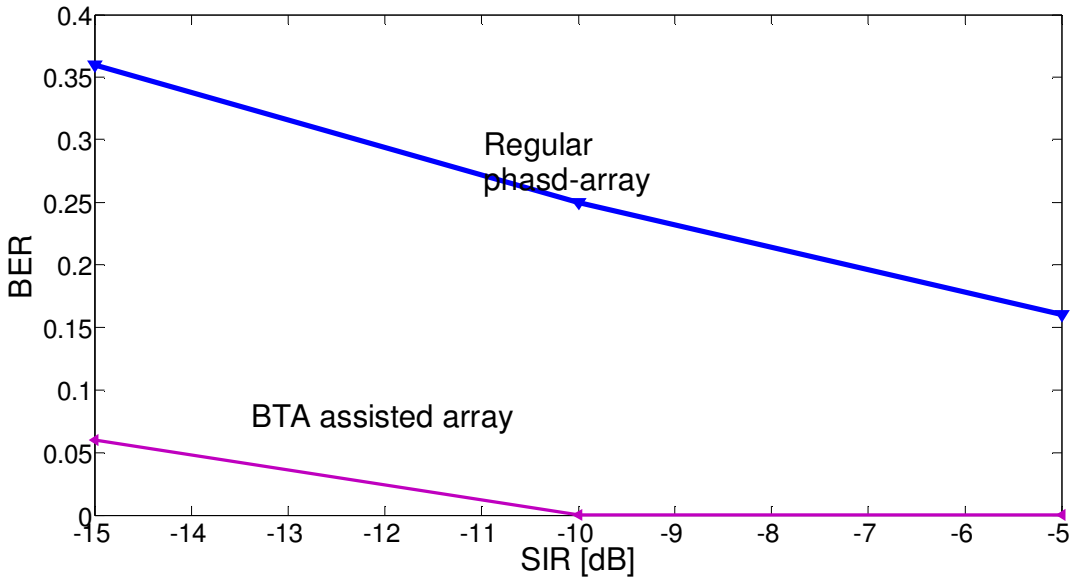

Figure 4.13 BER as a function of the SIR for a 64-element antenna array with 5dB SNR at the antenna and 16-QAM modulation

4.5 Implementation considerations

In order to show the power-friendliness of the proposed array architecture, we designed and fabricated a prototype of the programmable analog baseband delay in 65nm CMOS technology. Fig.4.14 shows the circuit schematic of our proposed programmable delay. Variable delay is achieved by means of tunable capacitors and resistors.

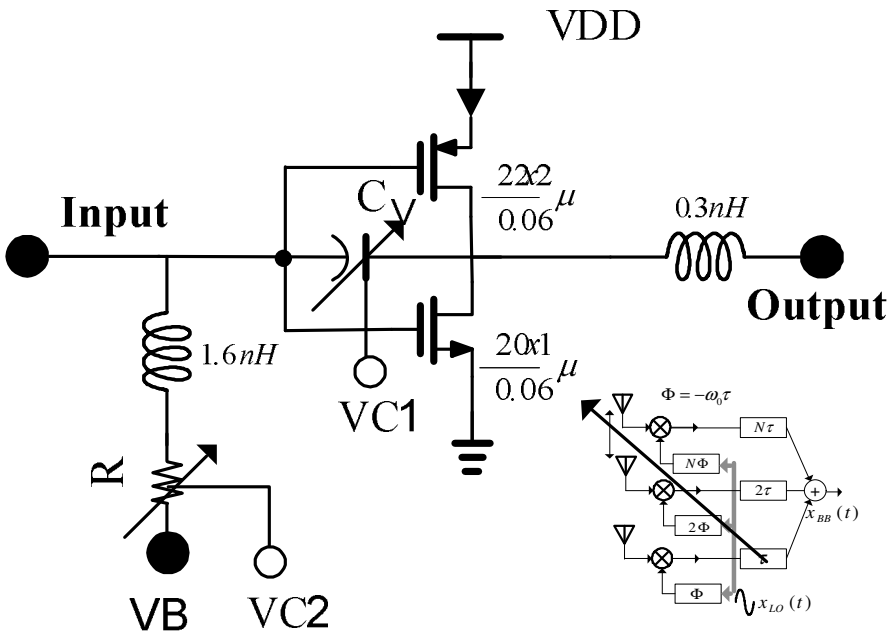

Figure 4.14 circuit schematic for the tunable delay element

Group delay of the circuit has a fine and a coarse control knob. Coarse delay control is achieved by turning a varactor (variable capacitor) on and off. Fine tuning is obtained by changing the resistance of the shunt-peaking [10], R-L branch at the input.

Inductors were implemented as spirals in the top thick metal and the varactor was implemented as MOSCAP. Variable resistor R is implemented as a high-voltage (2.8 volts) I/O NMOS in triode region. The resistance of R is controlled using an external voltage applied to the gate of the I/O transistor. All RF and DC paths are ESD-protected. Fig.4.15 shows the die photograph of the chip. DC power dissipation of the delay is 2.5mW (2.5mA at 1 volt VDD), while directly

driving 50 Ohm VNA load. This power dissipation would be significantly lower, if the delay is integrated with the whole transceiver.

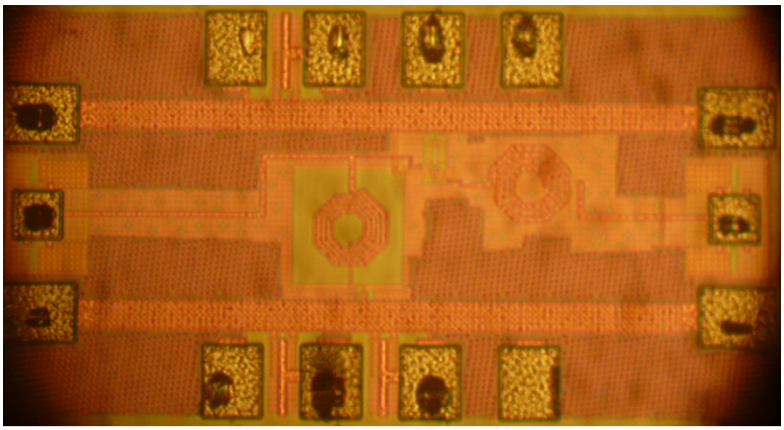

Fig. 4.15 die-photograph of the fabricate chip

The test-chip was on-die probe tested for calibrated two-port small signal S-parameters using a 67GHz VNA (vector network analyzer). Fig. 4.16 shows the magnitude and delay responses of the circuit as a function of the controlled voltage. The frequency band of the circuit was chosen to be 1.4- 3 GHz for a low-IF, 60 GHz transceiver currently being developed by our group. Measured group delay tuning range of more than 40 psec was achieved. Flat and loss-free amplitude and linear phase response were achieved in the band of interest.

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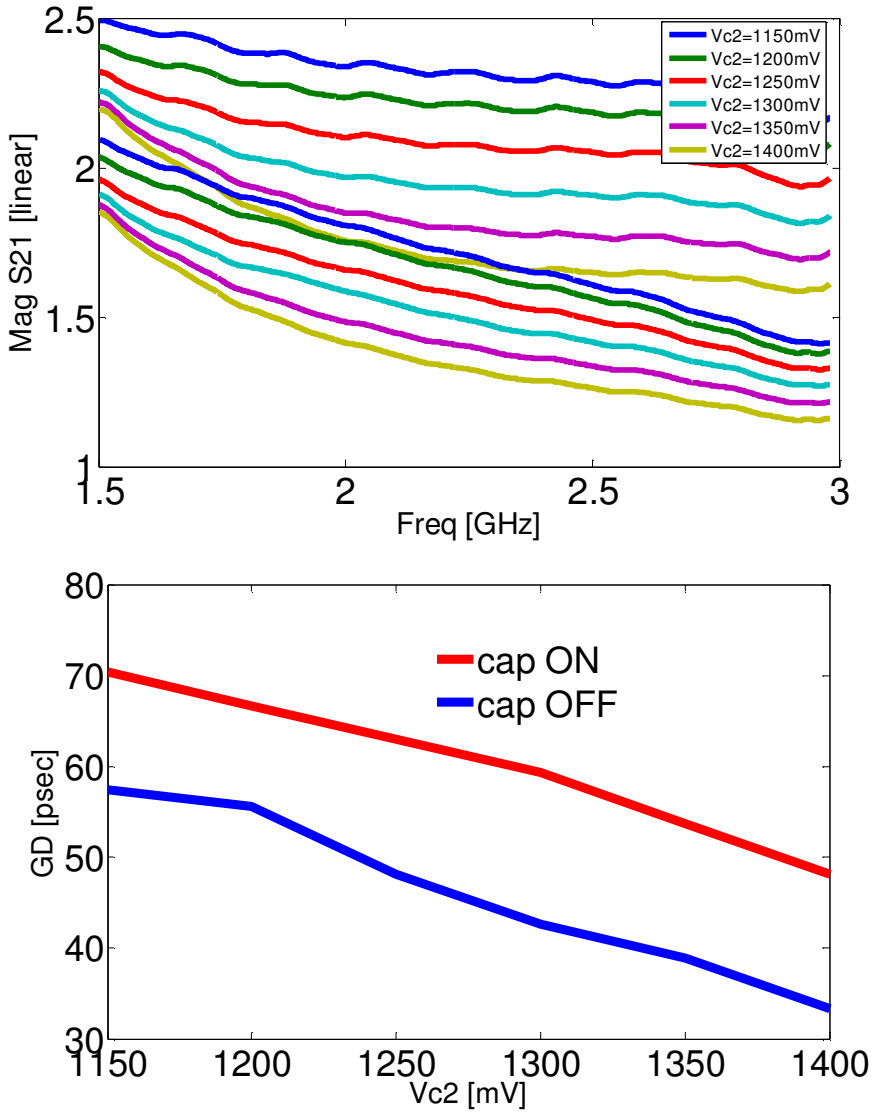

Figure 4.16 Measured results gain and group delay of the chip

4.6. Power saving figure of merit

We compare the power saving figure of merit of the proposed approach using real-life examples. The following shows the power saving figure-of-merit (FOM) of the proposed method versus the prior art. We have used our fabricated and measured 65nm delay prototype in this comparison. The chosen FOM is the product of the achieved delay times the center frequency divided by the power consumption.

Table 4.1 comparing the power saving FOM of the

Work	**Delay range [psec]**	**Power consumption [mW]**	**Operation frequency [GHz]**	$FOM = \frac{delay \times center\_freq}{power\_consumption}$
[8]	100	66	10	**15**
[9]	225	555	15	**6**
This	40	2.5	60	**960**

As evident from the comparison table, **the proposed baseband time-alignment archives an order of magnitude higher FOM.**

As a numerical example, in a 64-element, antenna array, using the traditional timed-array method requires 64 x 525psec x 60/ 15 =134 W power consumption.

This is while, the proposed architecture requires 2.1 W for the BTA, and 64 x 7=448 mW for mixers [11]. Passive phase shifter can be used for the LO beamforming [12]. These power estimates are summarized in Tab.4.2.

Table 4.2 comparing the power consumption of proposed and traditional/prior art arrays for 64-element antenna arrays

Component	**Estimated power consumption [mW]**
Mixers	7x 64=448
Delays	2.5/40 x 64 x 525=2100
LO phase shifters [12]	0
Total 64-element array (proposed)	2548
Total 64-element array (traditional/prior art)	134000

4.7 Chapter summary and conclusion

We showed in this chapter that larger-size, 60-GHz phased-arrays suffer from array-induced frequency fading and also beam-squinting, which severely affect the performance of the communication link. As a power-friendly solution we proposed a new array architecture called "LO beamforming with baseband time alignment (BTA)". We showed that the proposed array architecture resolves the array-induced frequency fading and beam-squinting while consuming much less power than the traditional method. In order to have a real-life reference for comparison, we designed and fabricated a baseband analog time-alignment delay element in 65nm CMOS technology. We showed by comparing real-life examples that the proposed architecture archives more than an order of magnitude higher power-friendliness figure of merit compared to prior, traditional methods.

Glossary of abbreviations used in this chapter

BER: Bit error rate

BTA: Baseband time alignment

FOM: Figure of merit

SNR: Signal to noise ratio

VNA: Vector network analyzer

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Chapter 5
Conclusions and suggestion for future works

5.1. Conclusion

This dissertation explores cross-domain and power-friendly techniques to assist underperforming RF and analog components. In order to assist ADC, we proposed a novel, generic and power-friendly solution to the delay mismatch issue in digitally assisted interference cancellers (DAIC) by using digital FIR predictor filters with negative group delay (NGD). We showed how the joint design of the DAIC and the NGD predictor can be formulized and solved as a convex optimization problem. We also analyzed the tradeoffs amongst several design parameters and the energy saving achieved with DAIC. We then applied the proposed NGD-assisted DAIC to the mm-wave link that was described in chapter 1. We showed that NGD-assisted DAIC can reduce the BER of the link by two orders of magnitude at a power consumption cost that is 2.3 times less than the traditional method. A proof-of-concept experiment was setup to verify the validity of the NGD-assisted DIAC concept.

We also introduced a novel, cross-domain technique called phase noise track and correct (PNTC). We showed that by using PNTC one can achive an order of magnitude reduction in the phase noise at an order of magnitude smaller power consumption cost compared to the traditional methods. We also showed that unlike previous remedies for the phase noise, PNTC is applicable to any modulation and waveform and to both transmitter and receiver sides. We also reviewed the effect of different design parameters on the performance gain of the PNTC.

We also proposed new array architecture called "LO beamforming with baseband time alignment (BTA)". We showed that the proposed array architecture resolves the array-induced frequency fading and beam-squinting while consuming much less power than the traditional method. In order to have a real-life reference for comparison, we designed and fabricated a baseband analog time-alignment delay element in 65nm CMOS technology. We showed by comparing real-life examples that the proposed architecture archives more than an order of magnitude higher power-friendliness figure of merit compared to prior, traditional methods

We also introduced a new phase noise suppression technique in MIMO systems with incoherent phase noise. We should that application of the proposed technique leads to significant performance improvement.

5.2. Suggestions for future work

Cross-domain techniques can be developed to assist other power-hungry blocks in wireless transceivers. In particular, power amplifier is a major consumer of power. Several research works can be found on the digital assistance of power amplifiers using methods such as digital pre-distortion, Cartesian feedback and dynamic power supply tracking. These works, however, suffer from such bottlenecks as latency in feedback and feedforward loops and still have a lot of room of improvement.

Glossary of abbreviations used in this chapter

ADC: Analog to digital converter

BTA: Baseband time alignment

DAIC: Digitally assisted interference cancellation

MIMO: multiple-input multiple-output

NGD: negative group delay

PNTC: phase noise track and correct