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***Abstract*—Drivetrain efficiency and weight represent significant barriers toward the development of future electric aircraft. Multilevel inverter designs have demonstrated high performance in these applications. The flying capacitor multilevel converter (FCML), in particular, has shown promise. It achieves very high efficiency due to its low-voltage, high figure-of-merit devices, and very low weight due to its reduced output filter size and reliance on capacitive energy storage. FCMLs contains many active devices with associated gate drive circuitry. In order to achieve simultaneous goals of high density, high efficiency, and good signal integrity, the layout of the converter is of utmost importance. In this work, a stacked PCB design is presented, which shields the low-voltage gate signals from interference, while also enabling an uninterrupted power path, low commutation loop inductance, and compact volume. A 400 V, 3.6 kW, 8-level FCML prototype is fabricated, which achieves >50 kW/kg specific power, >2 kW/in^3 power density and 98.1% peak efficiency.**

I. Introduction

Drivetrain efficiency and weight represent significant barriers toward the development of future electric aircraft. Multilevel topologies can provide reduced losses because they utilize low-voltage devices with high figure-of-merit [1], [2]. The FCML has also demonstrated high gravimetric and volumetric power density [3]–[7]. It generates a frequency multiplication effect such that the output filter size can be greatly reduced, and relies on capacitors for energy storage, which are far more dense than inductors at this scale [8]. FCMLs contain many active devices, gate drive circuitry, and flying capacitors. In order to achieve simultaneous goals of high efficiency, high density, and good signal integrity, converter layout is of utmost performance.

To minimize gate loop inductance, the gate drive circuitry must be placed close to the active devices. This takes board area away from the power path, which leads to increased routing resistance. Furthermore, it raises concerns for signal integrity, as the low-voltage control signals must be routed directly adjacent to the high dv/dt nodes of the power path. Switching performance is also heavily affected by the commutation loop inductance, a parasitic parameter which arises from the physical layout. This inductance causes voltage overshoot and electromagnetic interference (EMI) [9], [10]. For GaN-based power converters, this is of particular concern, because these devices switch fast and contain very little parasitics [11]–[14]. The gate resistance can be increased to mitigate these issues, but this will cause increased overlap loss. Alternatively, several advanced layout techniques have demonstrated reduced inductance. The use of decoupling capacitors with a hybrid routing loop can achieve below 1 nH of inductance, even for designs operating at 300 V or above [3], [15]. In this work, a stacked printed-circuit-board (PCB) design is proposed, which places all gate drive circuitry on a daughterboard, with the main power path located on the motherboard. This allows for reduced routing resistance and improved signal integrity. A novel commutation loop design is employed, consisting of 3 anti-parallel hybrid paths, which enables reduced switching loss and overshoot compared to prior solutions. A 400 V, 3.6 kW, 8-level FCML inverter prototype is fabricated, which achieves >50 kW/kg specific power, >2 kW/in^3 power density and 98.1% peak efficiency. Section II describes the hardware design. Next, Section III presents the experimental results. Finally, Section IV concludes the paper.

II. Hardware Design

A. Stacked PCB Design

The FCML topology contains many floating switches, each with isolated gate drive circuitry, which takes up a large portion of board area. The devices used in high-performance designs have very low on-resistance and high current limits (1.4 mOhm, 101 A for the EPC2302 used in this design [16]). The routing resistance must therefore be minimized to avoid excess conduction loss. The outer copper layers of the PCB are typically the thickest, so they should be reserved for the power path. The use of vias and inner layers for the conduction path reduces density. High-power converters generate considerable EMI from their switching actions, which can interfere with low-voltage control signals. Signal integrity is crucial in FCMLs because the switches are

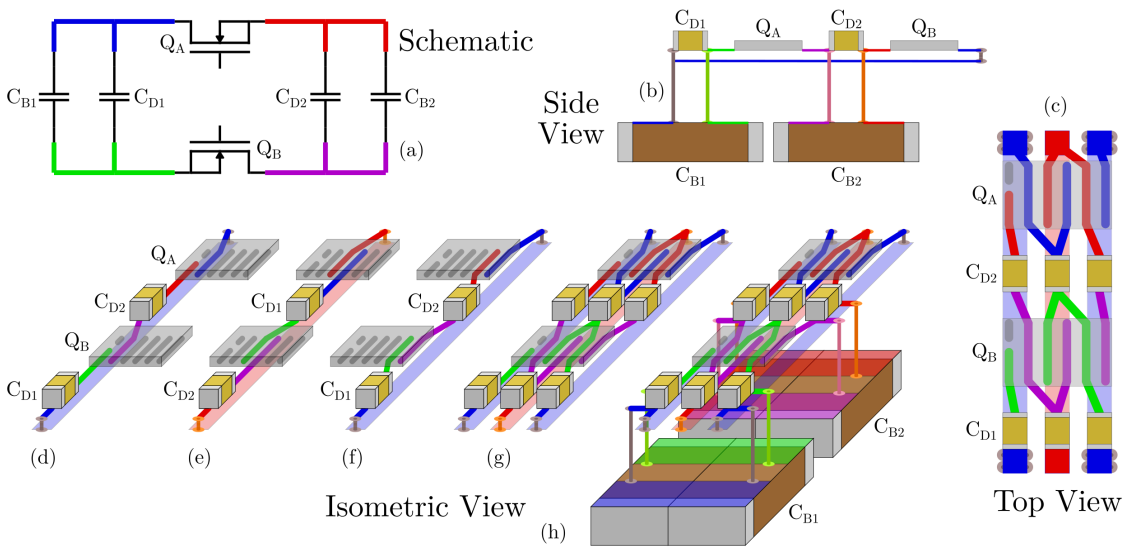

Fig. 1: Proposed commutation loop design. (a) schematic with color-coded nets, (b) side view, (c) top view, (d)-(f) isometric view highlighting separate paths, (g) combined hybrid paths, (h) including bulk capacitors.

not rated to the full input voltage, so false turn-ons can lead to complete system failure.

The use of a separate daughterboard PCB for the gate drive circuitry resolves both of these issues. In the proposed design, a 6-layer daughterboard is used. Layers 1 and 2 contain the gate drive components and routing, while layer 3 provides shielding pours. Layers 4-6 are empty so that there is 1 mm of FR4 separating the shields and the power path. The ground-referenced control signals enter from the top and bottom of the daughterboard through castellated vias soldered onto the motherboard. A digital isolator, with isolated power, provides gate signals referenced to the source of each switch. A high-current gate driver with split-gate outputs is connected to the switches again through castellated holes. Fig. 2a and 2b highlight the schematic and layout of the gate drive PCB switching cell, respectively. The area on the motherboard beneath the signal domain is used for routing gate signals from the main controller. The area on the motherboard beneath the switching domain is used for power path routing. This enables an extremely dense design where high-voltage clearances are satisfied and the sensitive ground-referenced control signals are distanced from noisy power nodes in both the vertical and horizontal directions, and have shielding layers beneath them. Moreover, the power path is completely uninterrupted on all layers of the motherboard.

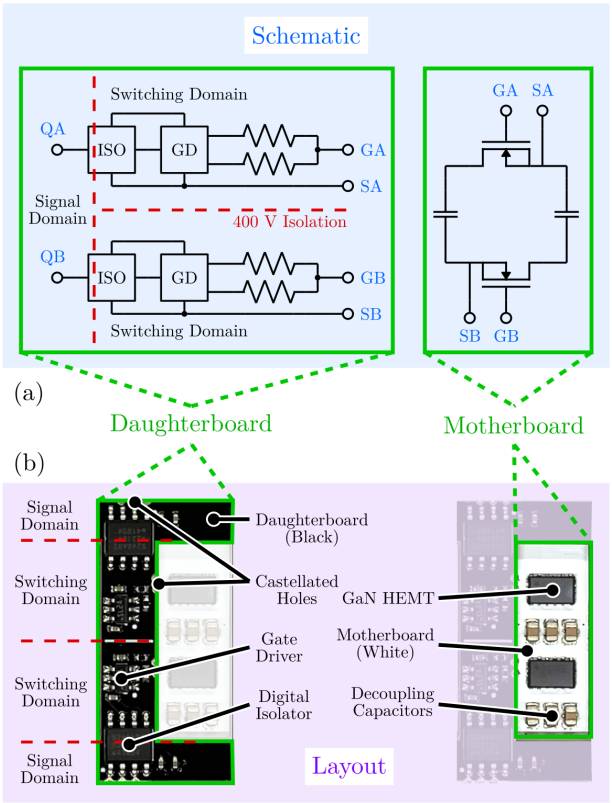

Fig. 2: Stacked PCB design with gate drive circuitry on daughterboard and power path on motherboard. (a) Schematic, (b) Layout with separate low-voltage signal domains and high-voltage switching domains on the daughterboard, which is matched by the motherboard.

B. Commutation Loop Routing

Prior work has demonstrated the severe impact that parasitic commutation loop inductance has on switching performance. It degrades both the reliability and efficiency [10]–[12]. A hybrid layout (utilizing the closest

Table 1: Commutation Loop Comparison

Switching Cell Design	Electrically Thin [9]	Hybrid & E-thin [3]	Hybrid Reference	Proposed Design
Simulated Inductance	1.15 nH	450 pH	521 pH	443 pH
Measured Inductance	2.85 nH	940 pH	—	1.14 nH
Board Area	370 mm^2	330 mm^2	420 mm^2	420 mm^2

Table 2: Hardware Prototype Component List

Component	Part Number	Parameters
GaN HEMT	EPC 2302	100 V, 1.4 mΩ
Bulk Capacitor	TDK C5750X6S2W225K250KA	450 V, 2.2 uF
Decoupling Capacitor	TDK C2012X7T2W473K125AA	450 V, 47 nF
Output Inductor	Vishay IHLP6767GZER3R3M5A	32 A, 3.3 uH
Output Capacitor	TDK C5750C0G2E154J230KE	250 V, 150 nF
Gate Driver	TI LM5114	5 V, 7.6 A
Digital Isolator	Analog ADUM5240ARZ	2500 V

Table 3: Key Converter Parameters

Parameter	Value
Input Voltage	400 V_{DC}
Output Voltage	135 V_{RMS}
Output Frequency	950 Hz
Effective Switching Frequency	714 kHz
Peak Output Power	3.67 kW
Peak Efficiency	98.1 %
Gravimetric Density	52.5 kW/kg
Volumetric Density	126 kW/L

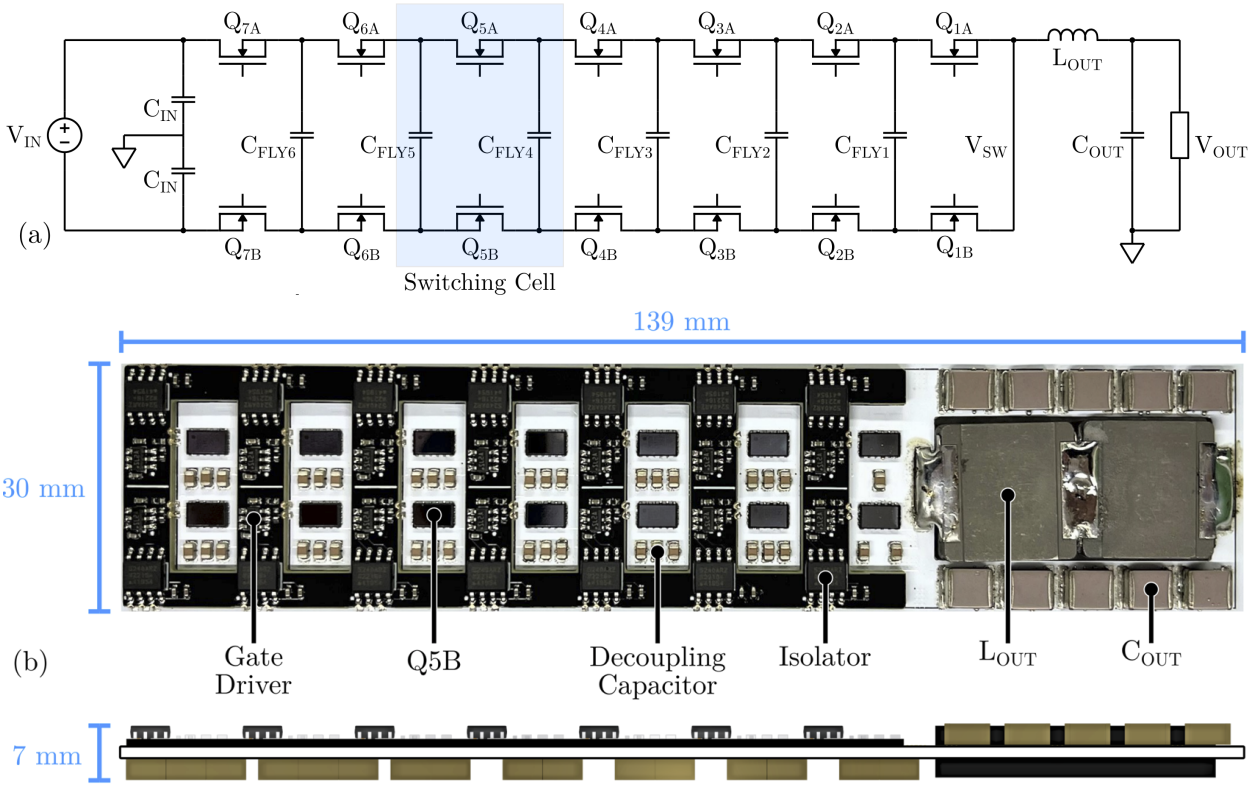

Fig. 3: Proposed 8-level FCML prototype. (a) Simplified schematic, (b) hardware image with labels

inner layer as a return path) with decoupling capacitors has been shown [3] to provide the lowest inductance to date for high voltage designs. In this work, a novel commutation loop layout is employed, which features 3 anti-parallel hybrid paths. It relies on the interleaved pads of the chip-scale packaged land-grid-array (LGA) EPC devices. It does not require any advanced manufacturing techniques from the PCB manufacturer, but does have smaller clearances than the standard hybrid approach, and thus a more limited voltage range.

The advanced commutation loop layout is shown from a variety of angles in Fig. 1. Fig. 1a shows the schematic

drawing of a single switching cell (as highlighted in Fig. 3a, with color-coded nets corresponding to the traces in other parts of the figure. Fig. 1b and 1c show side and top views respectively, while Fig. 1d-f highlight each hybrid path in isometric view. Note that the direction of current flow in each path is alternating. This provides flux cancellation which reduces inductance. Fig. 1g and 1h combine the paths and show the connections to bulk capacitors on the bottom of the motherboard, also in isometric view. The inductance values of both the decoupling and bulk capacitor loops are important for voltage overshoot during switching transitions [17]. Ansys Q3D was used to simulate the commutation loop inductance of this proposed design. Hardware measurement of the inductance was also performed with a Keysight E4990A Impedance Analyzer and 42941A probe, using the method in [15]. The simulated inductance is 443 pH while the measured value is 1.14 nH. The large difference between simulated and measured inductance is attributable to the package inductance of the devices and capacitors, which are not accounted for in simulation. The simulated value assesses the PCB routing only, with all components modeled as copper sheets. Table 1 compares the proposed design to prior art, both of which use blind and buried vias. As each design uses different components, the comparison is not entirely equal. To provide a fair reference, an alternate layout was made with a standard hybrid loop; this yielded a simulated inductance of 521 pH. The proposed design achieves comparable performance to the state of the art, without the need for blind or buried vias.

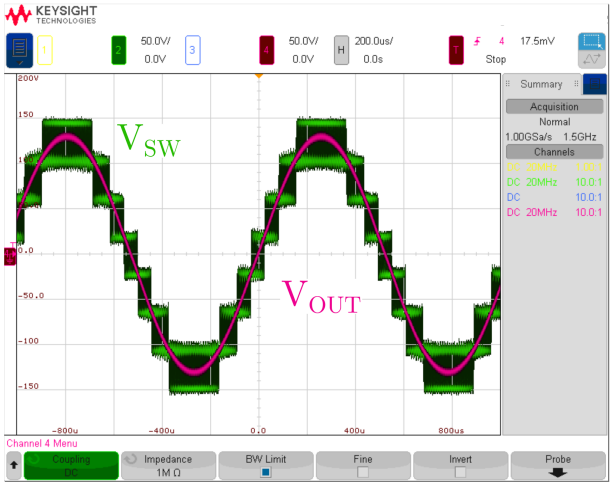

Fig. 4: Converter operating waveforms demonstrating 8-level operation with passive balancing.

III. Experimental Results

To validate the proposed design, a 400 V, 3.6 kW, 8-level FCML was fabricated. A simplified schematic is given in Fig. 3a, with the annotated hardware photograph depicted in Fig. 3b. Both boards are 6 layers and 1.6 mm thick. The output inductors are inset to a cutout in the motherboard. Relevant components are listed in Table 2. The FCML is operated as an inverter with 950 Hz sine wave output. The switching frequency is 102 kHz, which corresponds to a 714 kHz effective switching frequency for the output filter, due to the frequency multiplication effect of the FCML. Table 3 summarizes the converter parameters. Efficiency measurements are taken with a 400 V DC input voltage and 135 Vrms sine wave output voltage. These are shown in Fig. 5. The converter achieves a peak efficiency of 98.1 %, including gate drive losses, for an output power of 1.7 kW. Peak power is recorded at 3.67 kW, with an efficiency of 97.3 %. Given a mass of 70 g and box volume of 1.78

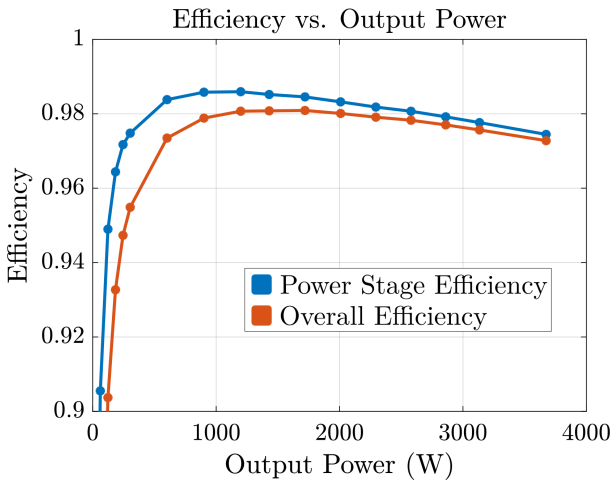

Fig. 5: Efficiency measurements for inverter operation with 400 V DC input voltage. Power stage efficiency (excluding gate drive loss) and overall efficiency.

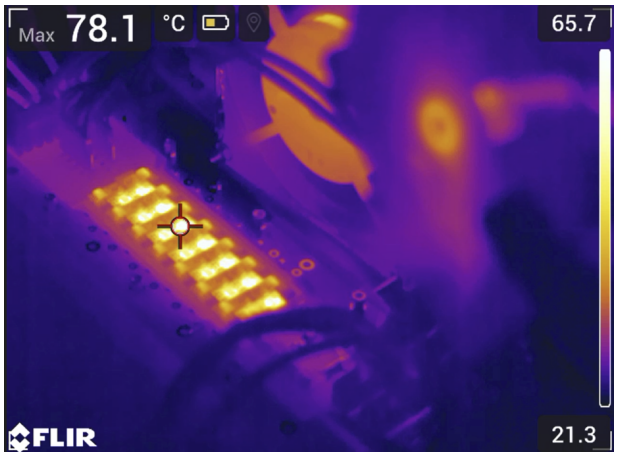

Fig. 6: Thermal image at full load. The active devices are hottest, with the isolators heating up as well.

in^3, this yields a gravimetric density of 52.5 kW/kg and volumetric density of 2.06 kW/in^3 (126 kW/L). Forced air cooling is used for these tests, but no heatsink is attached. Fig. 6 shows a full-load thermal image. The converter exhibits excellent passive balancing and low output distortion, as demonstrated by the V_{SW} and V_{OUT} waveforms in Fig. 4.

IV. Conclusion

This paper has presented a high power density FCML design for electric aircraft applications. It utilizes a stacked PCB system with the gate drive circuitry located on a daughterboard, and the main power path on the motherboard. This allows for improved density and signal integrity. In addition, the commutation loop is a novel triple-interleaved hybrid layout, which improves efficiency. The efficacy of the design is validated through experimental measurements; it achieves a measured commutation loop inductance of 1.14 nH, which enables a peak efficiency of 98.1% and a power density greater than 2 kW/in^3.

V. Acknowledgments

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