Silicon Carbide Bipolar Junction Transistors for High Temperature Sensing Applications

by

Nuo Zhang

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Committee in charge:

Professor Albert P. Pisano, Chair
Professor Tsu-Jae King Liu
Professor Liwei Lin

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Abstract

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An integrated sensing module capable of operating at high temperatures would be beneficial to a number of industrial applications, such as automotive industries, aerospace systems, industrial turbines and deep-well drilling telemetric systems. Consider industrial turbines as an example. It is important to monitor a variety of physical parameters within the hot sections of the turbines in order to increase turbine efficiency, reliability and to reduce pollution. In addition, real-time monitoring can help to detect and predict the failures of critical components in a timely fashion to reduce the maintenance costs of the systems. A high temperature integrated circuit is an important part of such systems, because it provides power management function for the energy scavenger, builds the electrical interface with MEMS-based harsh environment sensors, and amplifies the sensing signals. Therefore, it is essential to have transistors, the building blocks of integrated circuits, which can operate at high temperatures.

Silicon carbide (SiC) is a promising semiconductor for high temperature applications due to its excellent electrical and physical properties. The wide bandgap energy (3.2 eV for 4H-SiC) and low intrinsic carrier concentration allow SiC semiconductor devices to function at much higher temperatures. Moreover, high breakdown electric field (3-5 MV/cm), high-saturated electron velocity (2×10^7 cm/s) combined with high thermal conductivity (3-5 W/cm·°C) enable SiC devices to work under extreme conditions. There are growing interests on developing high temperature integrated circuits using SiC bipolar junction transistors (BJTs) because SiC BJTs are not as strongly affected by oxide quality as SiC metal-oxide-semiconductor field effect transistors (MOSFETs). In addition, SiC BJTs are normally-off devices and have higher transconductance compared with SiC junction field effect transistors (JFETs).

This dissertation presents comprehensive analytical and experimental results on 4H-SiC NPN BJTs capable of operating at high temperatures up to 400 °C. Comprehensive characterization including current gain, early voltage, output resistance, and intrinsic voltage gain was performed. At room temperature, the device has a current gain of 14.5

and an intrinsic voltage gain of 3300. At elevated temperatures, the intrinsic voltage gain increases to 5900 at 400 °C, although the current gain of the device is reduced to 6.7. This suggests that 4H-SiC BJT has the potential to be used as a voltage amplifier at extremely high temperatures. High temperature effects of 4H-SiC are theoretically studied. The incomplete ionization effect and the temperature dependence of minority carrier lifetime are the two main competing mechanisms for the change of device performance with rising temperature. To further enhance the current gain, fabrication process can be improved for reduction of interface traps residing between SiC and the passivation oxide layer.

This dissertation also presents the design, fabrication and characterization of a high-performance temperature sensor based on 4H-SiC pn diode. The device shows stable operation from room temperature up to 600 °C. Under forward bias condition, the temperature sensitivity of the sensor changes from 2.3 mV/°C at a forward current density of 0.44 A/cm^2, to 3.5 mV/°C at a forward current of 0.44 mA/cm^2. Higher sensitivity can be achieved at a lower forward current level. The experimental results indicate a good agreement with theoretical analysis. These results show that the device has the potential to be integrated with supporting circuitries to build a sensing module for high temperature applications.

To my parents and my husband

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Al	Aluminum
Al_2O_3	Aluminum oxide
Ar	Argon
A_v	Intrinsic voltage gain
α	Common-base current gain
α_T	Base transport factor
B	Boron
BJT	Bipolar junction transistor
β	Common-emitter current gain
C	Carbon
CF_4	Tetrafluoromethane
CHF_3	Trifluoromethane
Cl_2	Chlorine
CMOS	Complementary metal-oxide-semiconductor
CO	Carbon monoxide
CVD	Chemical vapor deposition
DC	Direct current
D_N	Diffusion coefficient of electrons
D_P	Diffusion coefficient of holes
ECR	Electron cyclotron resonance
E_g	Energy bandgap
E_A	Acceptor ionization energy
E_D	Donor ionization energy
E_{Fn}	Quasi-Fermi level for n-type semiconductor
E_{Fp}	Quasi-Fermi level for p-type semiconductor
ε_0	Vacuum permittivity
ε_s	Relative permittivity
GaAs	Gallium arsenide
G_m	Transconductance

HBr	Hydrogen Bromide
HF	Hydrogen Fluoride
HMDS	Hexamethyldisilazane
IC	Integrated Circuit
ICP	Inductively coupled plasma
I_B	Base current
I_C	Collector current
I_E	Emitter current
JFET	Junction field effect transistor
k	Boltzmann constant
L_N	Diffusion length of electrons
L_P	Diffusion length of holes
MESFET	Metal-semiconductor field effect transistor
MOSFET	Metal-oxide-semiconductor field effect transistor
N_B	Doping concentration in the base region
N_C	Doping concentration in the collector region
N_E	Doping concentration in the emitter region
N_A	Doping concentration of p-type semiconductor
N_A^-	Concentration of ionized acceptors
N_D	Doping concentration of n-type semiconductor
N_D^+	Concentration of ionized donors
N_c	Effective density of conduction band states
N_v	Effective density of valance band states
Ni	Nickel
NO	Nitric oxide
N_2O	Nitrous oxide
n	Electron concentration/Ideality factor of PN junctions
n_i	Intrinsic carrier concentration
O_2	Oxygen
PECVD	Plasma enhanced chemical vapor deposition
p	Hole concentration

ρ_c	Specific contact resistance
q	Electric charge
RIE	Reactive ion etching
RTD	Resistance temperature detector
RTA	Rapid thermal annealing
R_c	Contact resistance
R_{sh}	Sheet resistance
r_o	Output resistance
γ_E	Emitter injection efficiency factor
δ	Recombination factor
SEM	Scanning electron microscopy
Si	Silicon
SiC	Silicon carbide
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
SOI	Silicon-on-insulator
T	Temperature
TCP	Transformer coupled plasma
TLM	Transfer length method
Ti	Titanium
τ_e	Effective carrier lifetime
τ_n	Carrier lifetime of electrons
τ_p	Carrier lifetime of holes
μ_n	Electron mobility
μ_p	Hole mobility
V	Voltage
V_A	Early voltage
V_{BC}	Base-collector voltage
V_{BE}	Base-emitter voltage
V_{CE}	Collector-emitter voltage
V_{bi}	Built-in potential

W_B	Base width
W_{dep}	Depletion width

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Chapter 1

Introduction

There is a rising demand for harsh-environment integrated circuits and sensors for a wide variety of applications, ranging from structure health monitoring and process control to space navigation. The ability to continually obtain information *in situ* in high temperature environment such as a jet engine or a deep oil well can potentially save millions of dollars and even human lives. It also opens doors to space missions to locations with extreme conditions such as Venus, where devices would be required to operate around 500 °C. Wide bandgap materials are well suited for these applications due to their superior electrical and mechanical properties compared to the silicon incumbents. 4H-SiC, a polytype of silicon carbide (SiC), for instance, has a bandgap (3.2 eV) that is almost 3 times of that of silicon (1.12 eV) [1]. The wider bandgap results in a much lower intrinsic carrier concentration compared to that of silicon [1], which makes it an ideal candidate for high temperature (> 300°C) applications. These high temperature capabilities will be the main subject of investigation in this thesis. The overarching objective of the thesis is to develop 4H-SiC technologies for both transistor and sensor devices. Specifically, we investigate and develop the design, simulation, fabrication and characterization of 4H-SiC bipolar junction transistor (BJT) that is capable of operating at elevated temperatures up to 400°C. In addition, a high-performance temperature sensor based on 4H-SiC pn diode which can stably operate in a temperature range from 20°C to 600°C is demonstrated. This type of temperature sensor can be integrated with supporting circuitries to create a sensing module that is capable of working at extremely high temperatures.

1.1 High Temperature Sensing Applications

Harsh environment conditions are typically characterized by prolonged operation at high temperatures, exposure to intense radiation and exposure to corrosion and erosion. These conditions are common to combustion engines, chemical plants, oil wells, and space missions. Electronic and sensor components that can withstand such harsh environments can be highly beneficial to these applications. The ability to place sensing units at crucial

hot spots can be the key enabler for a multitude of innovations that are not possible with traditional silicon-based devices. For instance, in-cylinder monitoring of a combustion engine not only provides a means to gather accurate information about the status of the engine but also enables closed-loop control that can improve combustion efficiency. In this section, we first highlight some of these applications and describe in particular their high temperature requirements. We then review current available device technologies and discuss their limitations under these requirements.

Combustion Monitoring

The continual demand for increasing fuel efficiency and reducing environmental footprints require advances in combustion controls for automotive engines and gas turbines [2]. Optimizing an engine for these objectives require precise control of temperature, pressure, air-to-fuel ratio, and timing [3]. Traditional sensing mechanisms are based on indirect measurements, which limits the scope of control methods. In-cylinder sensing, on the other hand, holds the promise that it can provide accurate and timely information about combustion events, which in turn can be utilized to develop advanced closed-loop control systems for the engines to achieve the aforementioned objectives [4]. The temperature requirements in these environments can be quite stringent. A typical engine (gasoline or diesel) has an in-cylinder temperature ranging from 200 °C to 450 °C [5]. The temperature inside a gas turbine can reach as high as 650 °C [5]. Therefore, it is crucial to develop integrated sensing modules (sensors and electronic components) that can operate reliably over an extended period of time at high temperatures, in order to unleash the full potential of these advanced control systems.

Process Control

In production environments such as an oil refinery or a chemical plant, it is important to have proper process control to maintain quality, reduce operational cost and minimize waste. Current methods for performing process control rely on periodic data interrogation that lags behind the actual process, due to inability to directly gather information in harsh environments such as a deep oil well or a reactor plant. This leads to waste of resources and inferior products. Similar to combustion monitoring, a sensing module directly placed in these environments can enable real-time monitoring of process parameters, thus allows improved process control and detects hazardous scenarios in a timely manner [6]. The peak temperature requirements can range from 300°C in an oil or gas drill to 600°C in a geothermal extraction site [10].

Space Navigation

An important sensing module that is common to these navigation systems is the inertial measurement unit (IMU) [7]. A typical IMU contains a gyroscope, an accelerometer and the necessary electronic circuits, which together are used to harvest information on a

craft's velocity and orientation. However, traditional silicon devices are incapable of handling the stringent conditions often encountered by these navigation systems without extensive cooling, packaging and radiation shielding. These additional items would add volume and weight, thus placing a severe burden on the overall cost of the mission. NASA's Venus exploration mission, for instance, would require devices to operate around 500°C.

Structural Health Monitoring

Continual monitoring in environments such as a nuclear energy production plant or a steam generator tube and pressure vessel is crucial for ensuring operation inside the safety margins. It also reduces downtime for inspection and repair that may incur expensive labor cost and disrupt the services of these plants. Hence, measuring structural changes, also known as structural health monitoring, in the critical areas, can bring significant benefits to these applications [8]. An ideal sensing module for these applications would consist of sensors such as piezoelectric or piezoresistive sensors as well as integrated electronic components with wireless capabilities. The operating conditions of these applications such as inside a nuclear energy or a high-power processing plant, however, would also require the sensing module to work at high temperatures (> 300°C) over a long period of time. This thesis explores the development of high temperature transistors and sensors based on silicon carbide that can serve as the

Table 1-1. High temperature electronic applications [10]. BS stands for bulk silicon technology, SOI stands for silicon on insulator technology, WBG stands for wide bandgap semiconductor technology and NA stands for not presently available.

High Temperature Electronic Applications	Peak Ambient (°C)	Current Technology	Future Technology
Automotive			
Engine Control Electronics	150	BS & SOI	BS & SOI
On-cylinder & Exhaust Pipe	600	NA	WBG
Electric Suspension & Breaks	250	BS	WBG
Electric/Hybrid Vehicle PMAD	150	BS	WBG
Turbine Engine			
Sensors, Telemetry, Control	300	BS & SOI	SOI & WBG
	600	NA	WBG
Electric Actuation	150	BS & SOI	WBG
	600	BS	WBG
Spacecraft			
Power Management	150	BS & SOI	WBG
	300	NA	WBG
Venus & Mercury Exploration	550	NA	WBG
Industrial			
High Temperature Processing	300	SOI	SOI
	600	NA	WBG
Deep-Well Drilling Telemetry			
Oil and Gas	300	SOI	SOI & WBG
Geothermal	600	NA	WBG

building blocks of these integrated sensing modules.

Table 1-1 categorizes these applications and lists the peak temperature requirement for each of them. Silicon (Si) based devices cannot survive at high temperatures (> 300 °C) mainly due to the high intrinsic carrier concentration which exceeds the intentional doping, and high leakage currents. Silicon-on-insulator (SOI) technology enables silicon devices to approach their theoretical limits by cutting off leakage paths. At temperatures higher than 300 °C, wide bandgap semiconductors provide solutions capable of exceeding the limits of Si. They are listed as future technologies in Table 1-1.

1.2 Material Properties of Silicon Carbide

SiC-based semiconductor electronic devices and circuits are being developed for working under extreme conditions, such as high temperature, high power, and high radiation, thanks to its superior material properties compared to Si and other semiconductors. This section briefly surveys the basic properties and advantages of SiC material.

1.2.1 Crystal Structure

SiC is a group IV-IV compound semiconductor. Each silicon (Si) atom is tetrahedrally bonded with four carbon (C) atoms, and vice versa. The approximate distance between Si-C atoms is 1.89 Å, and the distance between Si-Si or C-C atoms is 3.08 Å. The tetrahedrally bonded Si-C cluster is shown in Figure 1-1 [1], [13].

SiC exists in many different crystal structures with the same chemical composition, called polytypes [1], [13]-[15]. There are over 100 known polytypes of SiC, and the most common polytypes of SiC that have been developed for electronic applications are 3C-

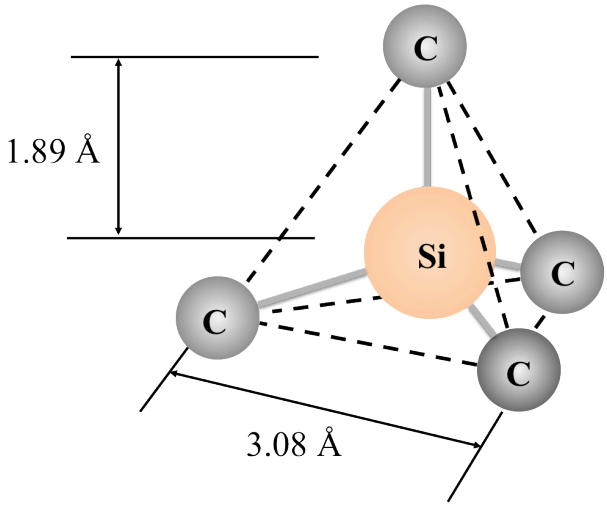

Figure 1-1. Tetrahedrally bonded Si-C cluster [1], [13].

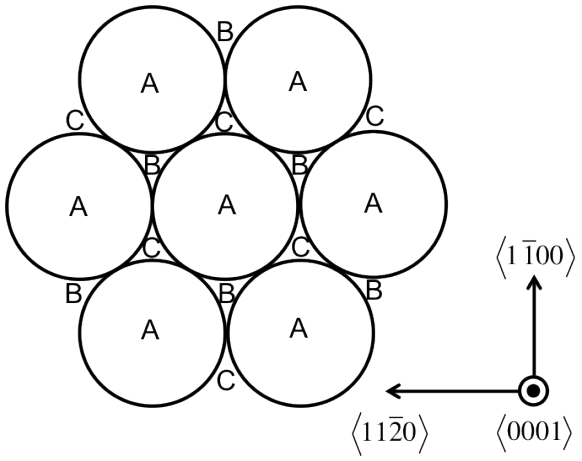

Figure 1-2. Hexagonal close packing positions of Si-C bilayers [1], [15].

SiC, 4H-SiC, and 6H-SiC.

Considering the Si-C pair as a sphere, they form hexagonal patterns when packed closely in a plane as a Si-C bilayer. The positions of the spheres in the first plane are denoted as A-site positions. For the next layer packed on top of the first layer, it can take either B-site positions or C-site positions. The hexagonal packing positions of Si-C bilayers are shown in Figure 1-2. Different polytypes are composed of different stacking sequences of Si-C bilayers. For instance, 4H-SiC has a stacking sequence of ABCB and it

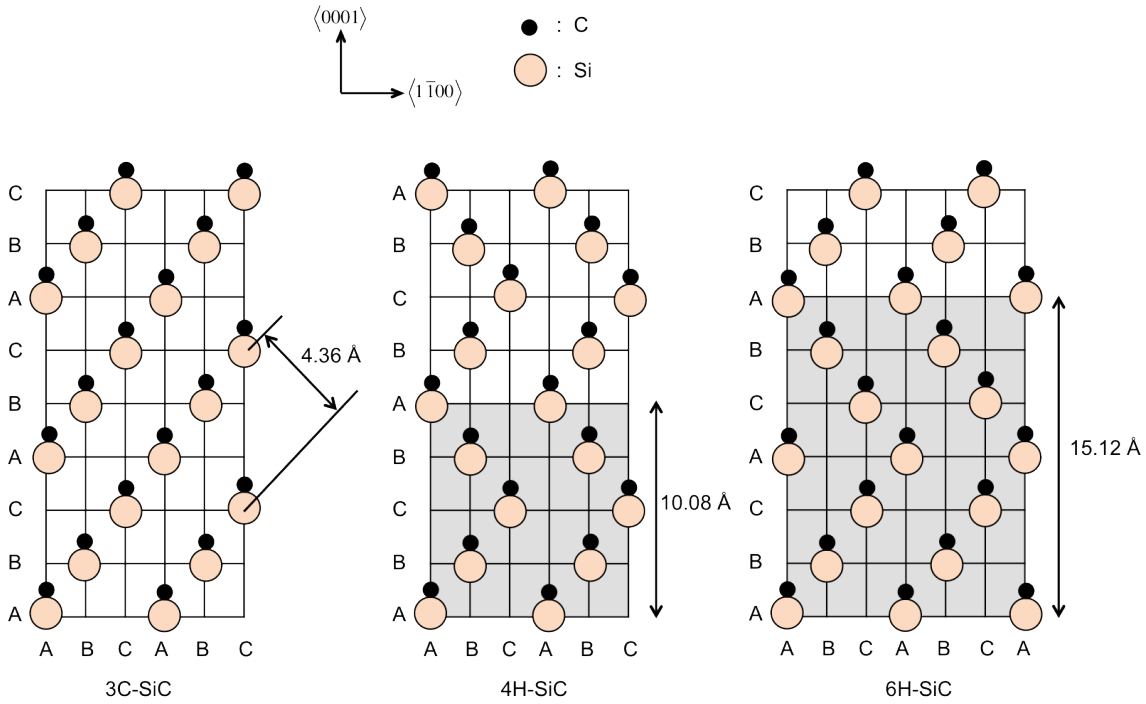

Figure 1-3. Stacking sequences of Si-C bilayers along c-axis for 3C-, 4H-, and 6H-SiC [15].

Table 1-2. Material properties of Si, GaAs and SiC [14]. ⊥ indicates perpendicular to c-axis, and || indicates parallel to c-axis.

Property	Si	GaAs	3C-SiC	6H-SiC	4H-SiC
Energy Bandgap [eV]	1.12	1.42	2.3	3.0	3.2
Critical Field at $N_D = 10^{17}$ cm^{-3} [MV/cm]	0.6	0.6	1.8	|| 3.2 ⊥ >1	|| 3.0 ⊥ 2.5
Thermal Conductivity [W/cmK]	1.5	0.5	3-5	3-5	3-5
Saturated Electron Drift Velocity [10^7 cm/s]	1.0	1.2	2.5	2.0	2.0
Electron Mobility at $N_D = 10^{16}$ cm^{-3} [cm^2/Vs]	1200	6500	750	|| 60 ⊥ 400	|| 800 ⊥ 800
Hole Mobility at $N_A = 10^{16}$ cm^{-3} [cm^2/Vs]	420	320	40	90	115
Relative Dielectric Constant	11.9	13.1	9.7	9.7	9.7

repeats every four layers throughout the crystal. Similarly, 6H-SiC has a stacking sequence of ABCACB. Both 4H-SiC and 6H-SiC have hexagonal crystal structures. 3C-SiC, sometimes referred to as β-SiC, has a stacking sequence of ABC and it is the only form of SiC with a cubic crystal structure. The schematic structures of common polytypes of SiC are shown in Figure 1-3.

1.2.2 Material Properties

SiC is a promising semiconductor for harsh environment sensing applications due to its excellent electrical and physical properties [1]-[15]. The wide bandgap energy and low intrinsic carrier concentration allow SiC based semiconductor devices to be functional at much higher temperatures. Moreover, high breakdown field, high-saturated electron velocity, and high thermal conductivity enable SiC devices to work under extreme conditions. The basic material properties of three SiC polytypes are summarized in Table 1-2 [14]. The critical field and mobility of SiC are anisotropic, and they strongly depend on crystallographic directions of applied electric field and current flow. For comparison, the properties of Si and gallium arsenide (GaAs) are also included in Table 1-2. 4H-SiC is used in this work since it has the widest energy bandgap.

1.3 High Temperature SiC Electronics

Si semiconductor devices are usually confined to operate at temperatures < 300 °C. The intrinsic carrier concentration increases exponentially with temperature, and these free carriers could exceed the intentional doping concentration and govern the device operation in Si devices. Furthermore, the undesired junction reverse-bias leakage currents are closely related to the intrinsic carrier concentration. As the temperature increases, the

undesired leakage current will grow unacceptably large. SiC semiconductor devices can function at much higher temperatures than Si mainly due to the wide bandgap energy and low intrinsic carrier concentration of SiC. High temperature operation of SiC-based devices and ICs has been reported for several technologies.

The gate-insulator reliability is a critical issue for high temperature operation of SiC metal-oxide-semiconductor field effect transistors (MOSFETs), which limits the highest operating temperatures under 350 °C for SiC MOSFETs. The first high temperature depletion-mode n-channel MOSFET was fabricated and characterized by Palmour *et al.* from North Carolina State University in 1987. Later, Brown *et al*. [16][17] from General Electric (GE) reported the development of the first SiC analog IC, a monolithic MOSFET operational amplifier, based on a 6H-SiC depletion-mode n-channel MOSFET technology. In that research, stable device operation was demonstrated up to 300 °C. However, circuit drift instabilities occurred at 350 °C. Complimentary metal-oxide-semiconductor (CMOS) technologies for SiC based devices have also been investigated. Recently, Clark *et al.* from Raytheon UK demonstrated SiC CMOS technologies that operate at elevated temperatures up to 350 °C with low gate leakage [18].

6H-SiC junction field effect transistors (JFETs) have been also investigated notably by NASA Glenn Research and Case Western Reserve University [19]-[21]. Prolonged stable operation of 6H-SiC JFETs for thousands of hours at 500 °C has been demonstrated. The devices have also been tested at low temperatures down to -125 °C. SiC JFET differential amplifier circuits capable of operating at up to 600 °C were demonstrated by Case Western Reserve University [22]. Subsequently, basic logic gates based on 6H-SiC JFETs were reported to work at temperatures up to 550 °C [23].

6H-SiC metal-semiconductor field effect transistors (MESFETs) have also been demonstrated for high temperature operation up to 500 °C [24]. However, they suffer from significant leakage currents at the Schottky gate electrodes at higher temperatures, which limits the duration of high temperature operation.

The research on 4H-SiC bipolar junction transistors (BJTs) originally focused on high power applications. The first high voltage NPN BJT in 4H-SiC was demonstrated by Ryu *et al.* from Cree, Inc. in 2001 [25]. Subsequently, many efforts have been made to develop SiC power BJTs from Purdue University, Rutgers University, and Royal Institute of Technology [26]-[30]. Recently, there are growing interests on developing high temperature integrated circuits using 4H-SiC BJTs. SiC BJTs are not as strongly affected by oxide quality as SiC MOSFETs. In addition, SiC BJTs are normally-off devices and have higher transconductance compared with SiC JFETs. 4H-SiC is used due to the fact that it has the widest energy bandgap compared with other SiC polytypes, which is preferred for high temperature applications. BJTs on semi-insulating 4H-SiC was demonstrated to operate up to 355 °C by Singh *et al.* in 2011 [31], [32]. In this dissertation, 4H-SiC NPN BJTs for low voltage applications are presented. The devices are capable of stable operation up to 400 °C [33].

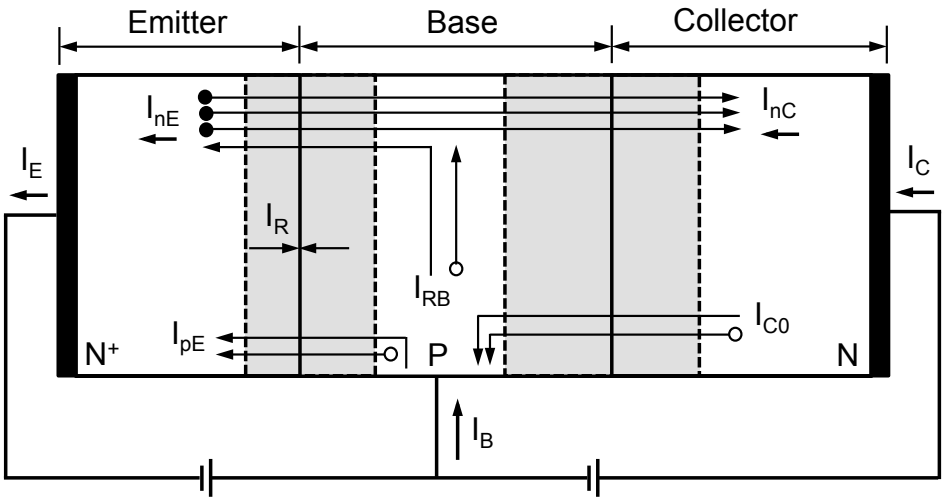

Figure 1-4. Schematic of a NPN BJT biased at forward active region [34].

1.4 Fundamentals of Bipolar Junction Transistors

A bipolar junction transistor is a three-terminal semiconductor device [34]. The middle region is referred to as the *base* and it is very narrow compared with the minority carrier diffusion length in this region. The other two regions are known as the *emitter* and the *collector*. Due to the fact that electron mobility is usually higher than hole mobility, NPN BJTs are more widely used than PNP BJTs. The schematic of a NPN BJT biased in the forward active mode with carrier flux components is shown in Figure 1-4 [34]. The two junctions are referred to as the emitter-base (E-B) junction and the collector-base (C-B) junction respectively.

As pictured in Figure 1-4, the E-B junction is forward biased and the C-B junction is reverse biased in the forward active mode. The E-B junction is an n^+-p one-sided junction. Therefore, more electrons are injected from the emitter to the base than holes injected from the base to the emitter. Since the quasineutral base width is much smaller than the minority carrier diffusion length, the vast majority of injected electrons that diffuses through the base can reach the depletion region of the reverse biased C-B junction. The electrons are then swept to the collector by the accelerating electrical field. The electrons injected from the emitter to the base constitute the current I_{nE}, and the holes injected from the base to the emitter give rise to the current I_{pE}. For the one-sided n^+-p junction, $I_{pE} << I_{nE}$. Some electrons are lost through recombination with holes in the base (I_{RB}). The current I_{nC} is associated with the injected electrons successfully cross the base and reach the collector. I_{C0} is the current of the minority carrier holes in the collector that are swept into the base in the reversed biased C-B junction. Since I_{C0} is a reverse biased current, $I_{C0} << I_{nC}$. The recombination-generation current associated with the depletion region of the

E-B junction is identified as I_R. The total currents of the emitter, base and collector regions are given by

$$I_E = I_{nE} + I_{pE} + I_R, \tag{1.1}$$

$$I_B = I_{pE} + I_{RB} + I_R - I_{C0}, \tag{1.2}$$

$$I_C = I_{nE} - I_{RB} + I_{C0}. \tag{1.3}$$

The three currents can be related by

$$I_E = I_B + I_C. \tag{1.4}$$

In the common-base mode, the emitter current (I_E) is the input variable while the collector current (I_C) is the output variable. α is the common base current gain, which is defined as the ration of I_C/I_E. It can be calculated as

$$\alpha = \gamma_E \alpha_T \delta = \left(\frac{I_{nE}}{I_{nE} + I_{pE}} \right) \left(\frac{I_{nC}}{I_{nE}} \right) \left(\frac{I_{nE} + I_{pE}}{I_{nE} + I_R + I_{pE}} \right). \tag{1.5}$$

In Equation (1.5), γ_E is the emitter injection efficiency factor, α_T is the base transport factor, and δ is the recombination factor [35]. The emitter injection efficiency factor is a measure of the ability of the emitter to inject electrons into the base. The base transport factor illustrates the capability of the injected electrons to diffuse through the base without recombination. The recombination factor takes into account the recombination-generation current in the forward biased B-E junction.

In the common-emitter mode, the base current (I_B) is the input variable and the collector current (I_C) is the output variable. The common-emitter current gain β is defined as the ratio of I_C/I_B, which can be calculated as

$$\beta = \frac{\alpha}{1 - \alpha}. \tag{1.6}$$

The common-emitter mode is the most widely used circuit configuration. Therefore, current gain is often referred to as the common-emitter current gain β.

1.5 Thesis Organization

This work focuses on the development and characterization of 4H-SiC NPN BJTs for high temperature sensing applications. This dissertation consists of six chapters including

this introduction. In Chapter 2, physical models of the device behaviors are studied. Chapter 3 presents the development of microfabrication technologies for SiC-based electrical devices. Chapter 4 discussed the simulation and characterization results of the fabricated 4H-SiC BJTs. In Chapter 5, the development and characterization of a high-performance temperature sensor based on 4H-SiC pn diode are presented. Finally, the contributions of this work are summarized and suggestions for future research directions are outlined in Chapter 6.

Chapter 2

Physical Models

Numerical device simulators are powerful tools to investigate electrical behaviors of semiconductor devices. They can provide information of internal physical parameters that are difficult or impossible to measure. Therefore, numerical device simulators are widely used to predict and explain device performance. A real semiconductor device is represented in the simulator as a non-uniform two-dimensional (2D) or three-dimensional (3D) grid of nodes. Physical properties of the real device are discretized onto the grid. By iteratively solving a set of coupled nonlinear partial differential equations, the transport of carriers through the structure under external fields can be described. The governing equations are Poisson equation, carrier continuity equations and drift-diffusion equations. In order to obtain accurate simulation results, it is essential to utilize appropriate physical models with proper material properties. In this chapter, important physical models applied in the device simulation are introduced and discussed. Temperature dependences of the models are investigated.

2.1 Band Structure

Energy band structure is the most fundamental property of a semiconductor. Realistic band structures are complicated. For device simulation, the band structure is described by energy bandgap, effective masses and effective density of states.

2.1.1 Energy Bandgap and Temperature Dependence

Energy bandgap is the difference between the lowest energy in the conduction band and the highest energy in the valance band. As we have discussed in Chapter 1, SiC has a wider bandgap compared with Si. The bandgap of 4H-SiC is 3.23 eV at 300 K. It is not a constant value when temperature varies, and the temperature dependence of the 4H-SiC bandgap can be modeled by Equation (2.1) from [36]:

$$E_g(T) = E_g(0) - 6.5\times10^{-4} \times \frac{T^2}{T+1300} \text{ eV}, \tag{2.1}$$

where $E_g(0)$ is the bandgap at 0 K, and T is the temperature in Kelvin.

2.1.2 Bandgap Narrowing

It has been reported that the bandgap of a semiconductor material shrinks when the impurity concentration is particularly high. This effect is called the *bandgap narrowing effect*. In a device containing adjacent regions with different doping concentrations, the displacements of band edges induced by the doping concentrations may heavily influence the device behavior. This is because the shifts of the band edges change the potential barriers in the device, which alters the carrier transport behavior across the junctions. In BJTs, the emitters are heavily doped, and therefore the bandgap narrowing effect in the emitters have to be considered in the device simulation.

Considering the bandgap narrowing effect, the effective bandgap $E_{g,eff}$ can be written as

$$E_{g,eff} = E_{g0} - \Delta E_{bng}, \tag{2.2}$$

where E_{g0} is the bandgap at a low doping concentration, and ΔE_{bng} is the shift of the bandgap due to the bandgap narrowing effect.

The intrinsic carrier concentration n_i for a lightly doped semiconductor is given by Equation (2.3)

$$n_i^2 = N_c N_v \exp\left(\frac{-E_{g0}}{kT}\right), \tag{2.3}$$

where N_c and N_v are the effective density of conduction and valence band states, k is Boltzmann constant, and T is the temperature in Kelvin [37]. For BJTs, the emitter is heavily doped. The effect of bandgap narrowing on the intrinsic carrier concentration in the emitter region is given by

$$n_{i,eff}^2 = n_i^2 \exp\left(\frac{\Delta E_{bng}}{kT}\right), \tag{2.4}$$

which changes exponentially with ΔE_{bng}. For a NPN BJT, the minority carrier concentration p_{E0} in the emitter region can be written as

$$p_{E0} = \frac{n_{i,eff}^2}{N_E} = \frac{n_i^2}{N_E}\exp\left(\frac{\Delta E_{bng}}{kT}\right), \tag{2.5}$$

Table 2-1. Parameters for bandgap narrowing model of 4H-SiC in Equation (2.6)-(2.9) [38].

	$\mathbf{A_{nc}}$	$\mathbf{B_{nc}}$	$\mathbf{A_{nv}}$	$\mathbf{B_{nv}}$
n-type	-1.50×10^{-2}	-2.93×10^{-3}	1.90×10^{-2}	8.74×10^{-3}
	$\mathbf{A_{pc}}$	$\mathbf{B_{pc}}$	$\mathbf{A_{pv}}$	$\mathbf{B_{pv}}$
p-type	-1.57×10^{-2}	-6.64×10^{-4}	1.30×10^{-2}	1.14×10^{-3}

where N_E is the doping concentration in the emitter region. Equation (2.5) shows that the bandgap narrowing effect increases the minority carrier concentration in the emitter region, which leads to a reduction of the emitter injection efficiency.

The doping-induced bandgap displacements and the bandgap narrowing effect in 4H-SiC have been modeled by Lindefelt [38]. The model is based on the theory of Jain and Roulston and is made applicable to 4H-SiC by considering the three electron effective mass components associated with hexagonal lattices. The band edge displacements for n-type and p-type semiconductors can be expressed as

$$\Delta E_{nc} = A_{nc}\left(\frac{N_D^+}{10^{18}}\right)^{1/3} + B_{nc}\left(\frac{N_D^+}{10^{18}}\right)^{1/2}, \tag{2.6}$$

$$\Delta E_{nv} = A_{nv}\left(\frac{N_D^+}{10^{18}}\right)^{1/4} + B_{nv}\left(\frac{N_D^+}{10^{18}}\right)^{1/2}, \tag{2.7}$$

$$\Delta E_{pc} = A_{pc}\left(\frac{N_A^-}{10^{18}}\right)^{1/4} + B_{pc}\left(\frac{N_A^-}{10^{18}}\right)^{1/2}, \tag{2.8}$$

$$\Delta E_{pv} = A_{pv}\left(\frac{N_A^-}{10^{18}}\right)^{1/3} + B_{pv}\left(\frac{N_A^-}{10^{18}}\right)^{1/2}. \tag{2.9}$$

The coefficients A_{nc}, B_{nc}, A_{nv}, B_{nv}, A_{pc}, B_{pc}, A_{pv}, and B_{pv} are listed in Table 2-1, with the band edge displacements given in eV.

2.1.3 Effective Masses and Effective Density of States

For 4H-SiC, the effective density of states in the conduction band N_c can be calculated from

$$N_c = 4.82\times10^{15}\times M\times\left(\frac{m_c}{m_0}\right)^{3/2}\times T^{3/2} = 3.25\times10^{15}\times T^{3/2}\ \text{cm}^{-3}, \tag{2.10}$$

where $M = 3$ is the number of equivalent valleys in the conduction band, and $m_c = 0.37m_0$ is the effective mass of the density of states in one valley of conduction band [36].
The effective density of states in the valance band is given by

$$N_v = 4.85\times10^{15}\times T^{3/2}\ \text{cm}^{-3}. \tag{2.11}$$

2.2 Mobility

The carrier mobilities are basic inputs for expressing currents in semiconductor devices. They are dependent on doping concentration and temperature. Using the empirical relation suggested by Caughey and Thomas [39], the electron mobility μ_n and hole mobility μ_p at low electric field can be modeled as

$$\mu_{n,p} = \mu_{n,p}^{\min} + \frac{\mu_{n,p}^{delta}}{1+\left(\frac{N_A+N_D}{N_{n,p}^{\mu}}\right)^{\gamma_{n,p}}}\left(\frac{T}{300}\right)^{\alpha_{n,p}}, \tag{2.12}$$

where N_A and N_D are local impurity concentrations, and the parameters are listed as below:

$$\mu_n^{\min} = 0\ \text{cm}^2/V\cdot S, \qquad \mu_p^{\min} = 15.9\ \text{cm}^2/V\cdot S,$$
$$\mu_n^{delta} = 947\ \text{cm}^2/V\cdot S, \qquad \mu_p^{delta} = 108.1\ \text{cm}^2/V\cdot S,$$
$$N_n^{\mu} = 1.94\times10^{17}\ \text{cm}^{-3}, \qquad \text{N}_p^{\mu} = 1.76\times10^{19}\ \text{cm}^{-3},$$
$$\gamma_n = 0.61, \qquad \gamma_p = 0.34,$$
$$\alpha_n = -2.15, \qquad \alpha_p = -2.15.$$

The parameters for the doping and temperature dependences of 4H-SiC mobilities are from the work of Schaffer *et al.* [40].

2.3 Incomplete Ionization

In Si, most impurity levels are shallow enough so that the dopants can be considered fully ionized at room temperature. However, this is not the case in SiC because the donor level (E_D) for nitrogen (N) and acceptor level (E_A) for aluminum (Al) in SiC are relatively deep compared to the thermal energy kT. Therefore, the incomplete ionization of the impurities in SiC has to be considered even at high temperatures.

The concentration of the ionized impurity atoms is given by

$$N_D^+ = \frac{N_D}{1 + g_D \exp\left(\frac{E_{Fn} - E_D}{kT}\right)}, \tag{2.14}$$

$$N_A^- = \frac{N_A}{1 + g_A \exp\left(\frac{E_A - E_{Fp}}{kT}\right)}, \tag{2.15}$$

where N_D^+ and N_A^- are the ionized donor and acceptor concentrations, N_D and N_A are the (active) donor and acceptor concentrations, $g_D = 2$ and $g_A = 4$ are the degeneracy factors for the donor and acceptor levels, E_D and E_A are the donor and acceptor ionization energies, and E_{Fn} and E_{Fp} are the quasi-Fermi levels [41].

Impurity atoms in SiC can substitute on either the silicon or carbon sublattice. Nitrogen atoms substitute on the carbon sites, while aluminum atoms occupy the silicon sites [42]. Due to the long unit cells, inequivalent lattice sites exist in many SiC polytypes, such as 4H-, 6H- and 15R-SiC. These inequivalent lattice sites are divided into two kinds: one is hexagonal-like atomic configuration (h) and the other one is cubic-like atomic configuration (k).

For nitrogen doped n-type 4H-SiC, two inequivalent lattice sites of nitrogen (h, k) have been identified by Hall-effect and IR absorption measurements with ground state $1s(A_1)$ binding energies of $E_D(h) = 52.1\ meV$ and $E_D(k) = 91.8\ meV$ [43]. The number of k-type donor sites is the same as h-type donor sites. It is worth noting that a simplification of a single donor level, $E_D = 65\ meV$ below the conduction band edge, is assumed in Equation (2.14), which can be obtained by [44]

$$\begin{aligned} N_{D\_4H-SiC}^+ &= \frac{0.5N_D}{1 + g_D \exp\left(\frac{E_{Fn} - E_D(h)}{kT}\right)} + \frac{0.5N_D}{1 + g_D \exp\left(\frac{E_{Fn} - E_D(k)}{kT}\right)} \\ &= \frac{N_D}{1 + g_D \exp\left(\frac{E_{Fn} - E_D}{kT}\right)}. \end{aligned} \tag{2.16}$$

For aluminum-doped p-type 4H-SiC, two inequivalent lattice sites should generate two energy levels in theory. However, the difference between the two acceptor levels are too small to be readily detected. Therefore, only one acceptor energy level $E_A = 191\ meV$ is assumed in the calculation [45].

2.4 Generation-Recombination

Generation-recombination processes are processes that create and eliminate mobile carriers (electrons and holes). They are very important to the operation of many semiconductor devices, especially for bipolar devices. There are several mechanisms that are crucial in SiC BJTs.

2.4.1 Shockley-Read-Hall Recombination

In the indirect-bandgap semiconductors, such as Si and SiC, indirect recombination process through localized states or recombination centers is dominant. This recombination process was originally modeled by Shockley and Read [47] and later by Hall [48], and the process is commonly called Shockley-Read-Hall (SRH) recombination. The rate of SRH recombination is given by

$$R_{SRH} = \frac{np - n_{i,eff}^2}{\tau_p \left(n + n_1\right) + \tau_n \left(p + p_1\right)}, \tag{2.17}$$

with n_1 and p_1 defined by

$$n_1 = n_{i,eff} \exp\left(\frac{E_{trap}}{kT}\right), \tag{2.18}$$

$$p_1 = n_{i,eff} \exp\left(\frac{-E_{trap}}{kT}\right), \tag{2.19}$$

where n and p are the electron and hole concentrations, $n_{i,eff}$ is the effective intrinsic carrier concentration, τ_n and τ_p are the lifetimes of electrons and holes, and E_{trap} is the energy difference between the defect level and the intrinsic level.

The lifetimes τ_n and τ_p depend on doping level and temperature. The doping dependence of the carrier lifetimes is described by the Scharfetter relation, and the temperature dependence is modeled by the power law.

$$\tau_{n,p} = \frac{\tau_{n,p}^{\max}}{1+\left(\frac{N_A+N_D}{N_{n,p}^{ref}}\right)^{\gamma_{n,p}}}\left(\frac{T}{300}\right)^{\alpha_{n,p}}, \tag{2.20}$$

where $\tau^{max}_{n,p}$ is the carrier lifetime in the material without impurities at 300 K, and the other parameters are listed as follows,

$N_n^{ref} = 3\times10^{17}\ \mathrm{cm}^{-3}$, $\quad N_p^{ref} = 3\times10^{17}\ \mathrm{cm}^{-3}$,

$\gamma_n = 0.3$, $\quad \gamma_p = 0.3$,

$\alpha_n = 1.72$, $\quad \alpha_p = 1.72$.

The parameters for the doping dependences of 4H-SiC career lifetimes are reported in [41] and [49], and the parameters for temperature dependence are taken from [41] and [50]. Since very limited studies on the doping dependence of carrier lifetimes in 4H-SiC have been reported, it is assumed that the parameters N_{ref} and $\gamma_{n,p}$ from Si can be applied to 4H-SiC.

2.4.2 Surface SRH Recombination

At surfaces or interfaces, an additional equation is used to describe the surface SRH recombination rate, which is structurally equivalent to expression of the bulk SRH recombination rate:

$$R_{SRH}^{surface} = \frac{np - n_{i,eff}^2}{(n+n_1)/s_p + (p+p_1)/s_n}, \tag{2.21}$$

where s_n and s_p are the surface recombination velocities for electrons and holes, n_1 and p_1 are defined in Equation (2.18) and Equation (2.19).

Surface recombination rate has strong impact on the current gain of SiC BJTs. It depends on the quality of the interface between silicon dioxide (SiO_2) and SiC. Some methods have been reported to reduce the interface state density at the SiO_2/SiC interface, which will be discussed in detail in Chapter 3.

2.4.3 Auger Recombination

In the Auger recombination process, the transition of an electron from the conduction band to the valance band is by transferring the energy to another free electron or hole by collision. Therefore, Auger recombination is a process in which three particles are involved: the recombining electron and hole, and the carrier by which the energy is absorbed. The highly energetic carrier, which gained the energy during the collision, then loses the energy in small steps through heat-producing collisions with the semiconductor

lattice. Auger recombination is typically important when the carrier densities are very high. Therefore, it is only likely to occur in highly doped semiconductor material or under high injection condition. The rate of Auger recombination can be modeled by [46]

$$R_{Auger} = \left(C_n n + C_p p\right)\left(np - n_{i,eff}^2\right), \tag{2.22}$$

where $C_n = 5\times10^{-31}\ cm^{-6}s^{-1}$ and $C_p = 2\times10^{-31}\ cm^{-6}s^{-1}$ [36].

Chapter 3

Microfabrication Technology of SiC Bipolar Junction Transistors

SiC single crystal material growth was first developed by Acheson process as byproducts for manufacturing industrial abrasives [51]. In 1955, Lely presented a sublimation method for SiC single crystal growth with higher quality [52]. However, Acheson process and Lely process can only produce small (~ 1 cm^2) and irregular shaped SiC crystal pieces. In the late 1970s, Tairov and Tzvetkov developed a modified seeded sublimation process for growth of single crystal 6H-SiC [53], [54]. This method is also known as modified Lely method. It was a big breakthrough in the SiC industry because it made mass-production of single crystalline SiC wafers possible. After years of development of the SiC crystal growth technology, Cree, Inc. became the first company to sell 2.5 cm diameter 6H-SiC wafers in 1989, and majority of the development of SiC semiconductor electronics took place afterwards. One of the main advantages of SiC fabrication technology is that many Si process techniques can be applied to SiC process. This chapter presents an overview of the microfabrication process technology of SiC BJT devices. A baseline six-mask fabrication process is described to manufacture the proposed devices. Some issues with SiC dry etching, metallization and surface passivation are addressed. It is worth noting that some fabrication limitations described here are due to the technological limits of the semiconductor fabrication tools used in the microfabrication process. Advanced tools would allow better fabrication process in the future.

3.1 Fabrication Process Flow of SiC Bipolar Junction Transistors

The devices were fabricated on 4° off-axis Si-face n-type 4H-SiC wafer purchased from SiCrystal AG. The fabrication process for manufacturing the SiC BJTs is based on surface micromachining techniques, and a baseline six-mask fabrication process is described as follows. The cross-sectional process flow is shown in Figure 3-1.

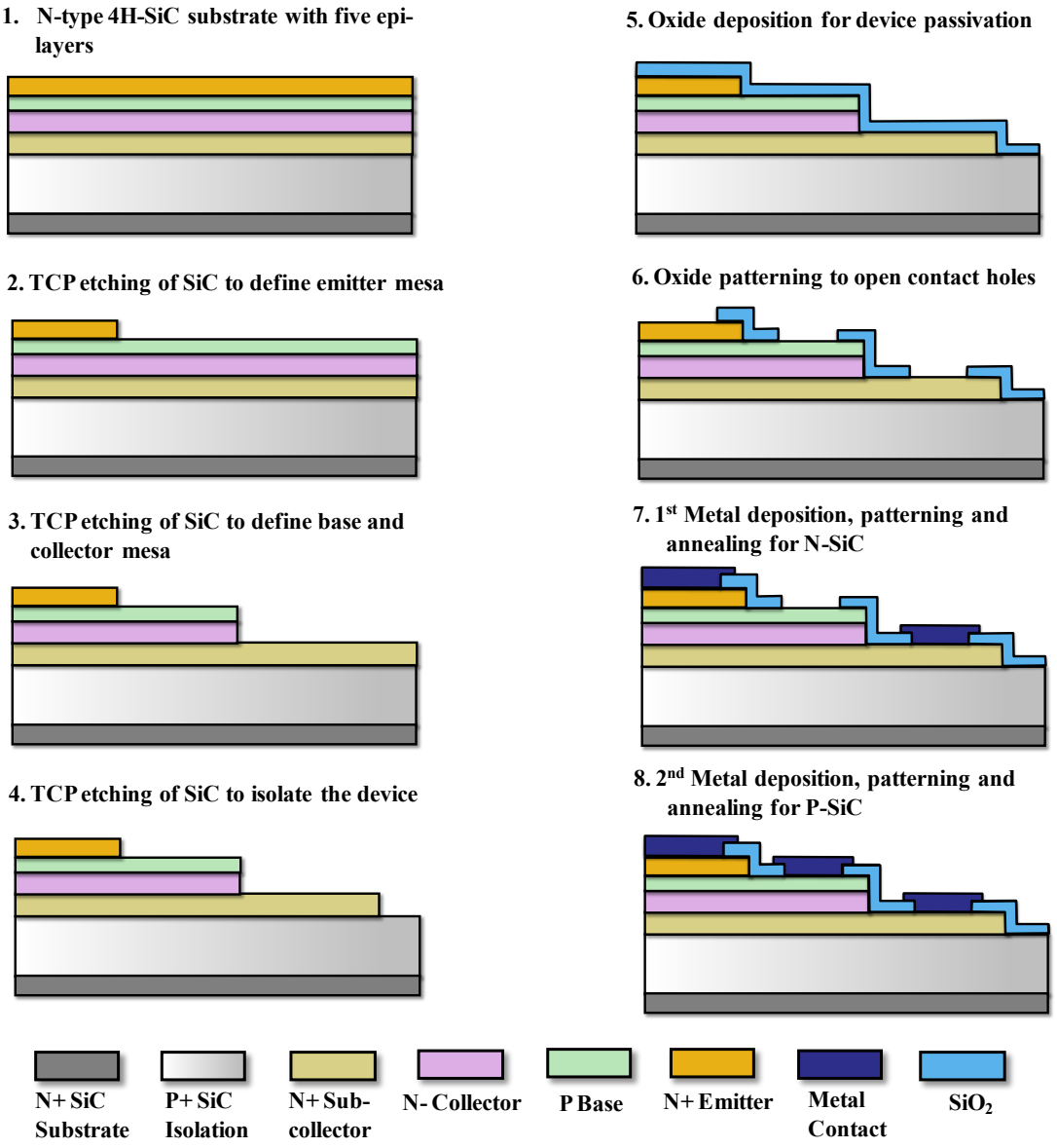

Figure 3-1. Cross-sectional process flow of the SiC BJT.

1. The process starts with a 4H-SiC wafer with designed epitaxial layers on top. The epitaxial layers were grown by Ascatron AB using chemical vapor deposition (CVD). The diffusion coefficients of impurities in SiC are negligible at temperatures below approximately 1800 °C [42]. Therefore, diffusion process is not considered as a doping method for SiC devices. To get the proper doping concentration, ion implantation and epitaxial growth are generally used in SiC devices. In this work, the doping profiles are formed by epitaxial growth to avoid the post-annealing step for ion implantation at extremely high temperatures (> 1600 °C) [55], [56].
2. There are three SiC etching steps in the fabrication process. The first one is used to

define the emitter mesa. First, a 1-μm-thick oxide layer was deposited by plasma enhanced chemical vapor deposition (PECVD) method. Next, the oxide layer was patterned using standard photolithography step and etched by reactive ion etching (RIE) method. A positive photoresist OiR 10i (I-Line) was used. Before spin casting the photoresist, wafers were dried and treated with hexamethyldisilazane (HMDS) vapor coating to promote adhesion of the photoresist. A Karl Suss MA6 Mask Aligner was used for the photolithography step. The patterned oxide layer acted as a hard mask for the following SiC etching step. Then, the first dry etching step of SiC was performed by a transformer coupled plasma (TCP) etcher using hydrogen bromide (HBr) and chlorine (Cl_2) as process gases. This step is to pattern the first N+ SiC epitaxial layer, which forms the emitter regions of SiC BJTs. The standard etch rate of SiC is around 90 nm/minute and the selectivity of SiC over oxide is about 3:1. Finally, the oxide mask was removed by 5:1 buffered hydrogen fluoride (HF) solution. It is worth noting that no etch stop layers exist in between different epitaxial 4H-SiC layers. Therefore, the etching thickness is controlled by doing a timed etch.

3. The second TCP etching of SiC is similar to step 2. It is used to etch through the second and the third SiC epitaxial layers to form the base and collector mesa for the SiC BJT.

4. The third TCP etching of SiC is also similar to step 2. It is used to etch through the fourth SiC epitaxial layer to isolate the devices.

5. A 50-nm-thick oxide layer was deposited using PECVD method. The process gases were nitrous oxide (N_2O), silane (SiH_4) and argon (Ar). This thin oxide layer is used to passivate the device. It has been shown that the interface traps existing between SiC patterns and the oxide layer have a large impact on the device performance. The trap density can be reduced if dry oxidation is used or a high temperature annealing step is performed after the oxide deposition. PECVD oxide is used in this work due to limitations of the equipment in our lab.

6. The passivation oxide layer was then patterned. First, photoresist was spin casted onto the wafer and standard photolithography step was used to pattern the photoresist. Then the oxide layer was etched by RIE using tetrafluoromethane (CF_4) and trifluoromethane (CHF_3). The standard etch rate of the oxide is about 300 nm/minute and the selectivity of oxide over photoresist is around 5:1.

7. The first metallization step is used to form good ohmic contacts for n-type SiC. A 100-nm-thick nickel (Ni) layer was deposited using E-beam evaporation. Then it was patterned by photolithography and lift-off processes. To obtain good ohmic contacts with low resistivity, a rapid thermal annealing (RTA) step was performed for 1 minute in Ar ambient at 1000 °C.

8. The second metallization step is used to form good ohmic contacts for p-type SiC. A nickel/titanium/aluminum metal stack was deposited using E-beam evaporation. Then

it was patterned by photolithography and lift-off processes. To obtain good ohmic contacts with low resistivity, a RTA step was performed for 1 minute in Ar ambient at 800 °C.

3.2 Fabrication Challenges

There are three main challenging steps in the fabrication process. It is important to overcome these challenges for enhancing device functionality and performance. These steps are dry etching of SiC, metallization and surface passivation. In this section, these fabrication challenges are first introduced and then addressed.

3.2.1 Etching of Silicon Carbide

The strong chemical bond between Si and C makes SiC very hard to be etched. There are no known wet chemicals that can etch single crystal SiC at room temperature. The wet etching of SiC has to be done using high-temperature (> 300 °C) and corrosive mixtures, which are hard to handle. Also, only a few materials can be used as masks. Therefore, dry

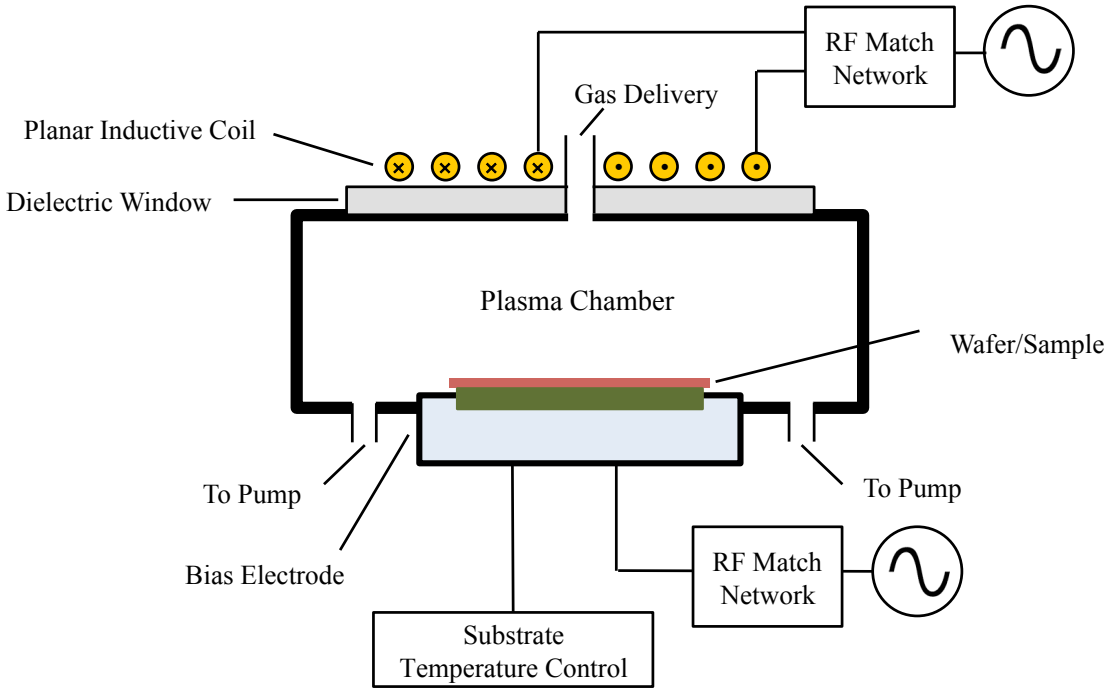

Figure 3-2. Schematic of TCP etching system (Lam Research) [63].

etching is the commonly used method to pattern SiC to fabricate SiC electronic devices.

In the early years, reactive ion etching (RIE) was commonly used to etch SiC using fluorinated plasmas [57], [58]. However, rough surfaces were often observed due to the high dc self-bias. With the advent of high-density plasma etching systems, such as electron cyclotron resonance (ECR) etcher, and transformer/inductively coupled plasma (TCP/ICP) etcher, significant improvements of the etching rate and the etching profile of SiC materials were obtained [59]-[62]. The key advantage of these high-density plasma systems is the decoupling of ion density and ion energy. In a TCP/ICP etcher, the high-density plasmas are generated by an inductive coil where RF power is applied. For TCP etchers, the inductive coils are mounted on the top of the plasma chamber. Whereas for ICP etchers, the inductive coils are mounted on the outside of the chamber. The ion energy is controlled by a separate RF power source that is connected to the wafer platen. Therefore, high-density and low-energy ion flux can be obtained, which is expected to achieve high etch rates and low surface damage at the same time. In this work, a TCP etcher from Lam Research is used. A schematic of the TCP etching system is shown in Figure 3-2.

Conventional mask materials for dry etching, such as hard-baked photoresist, SiO_2 and silicon nitride (Si_3N_4), are usually etched at higher rates than SiC in fluorine-based plasma chemistries. This is the reason why metal mask was used in some SiC etching processes. However, the residual metal leads to contamination in the subsequent process steps. As a result, etching process using a metal mask is not allowed in most laboratories. In addition, it has also been observed that due to sputtering of metal material onto the surface of SiC sample, grass-like structures are formed during the etching process. This is known as the *micromasking phenomenon*. Hence, it is of great importance to develop a

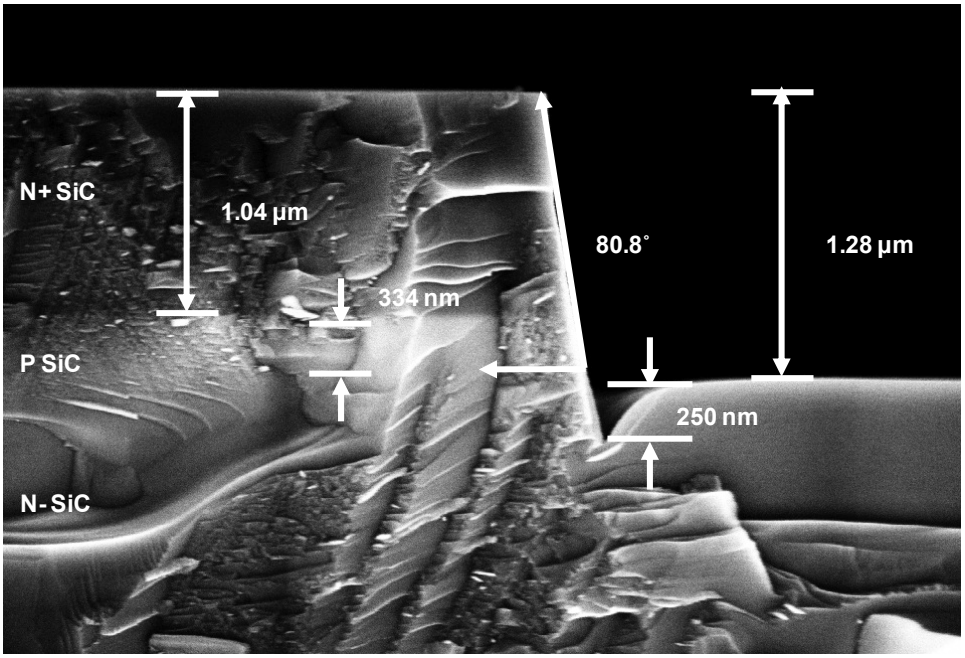

Figure 3-3. Scanning electron microscopy (SEM) image of the etching profile showing the trench effect.

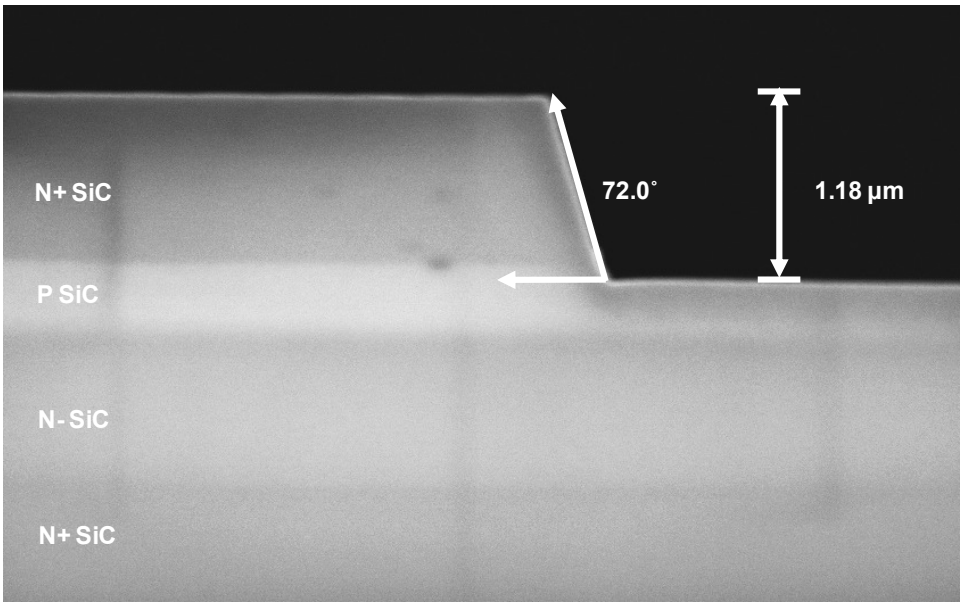

Figure 3-4. SEM image of the etching profile without trench effect.

dry etching process with high selectivity and nonmetallic mask. Hydrogen bromide (HBr) and chlorine (Cl_2) based dry etching chemistry has been widely used to etch Si material with high etch rate and high selectivity to SiO_2. Therefore, HBr and Cl_2 based chemistry is studied to etch SiC using SiO_2 as the mask material in this work. By changing the percentage of Cl_2 in the gas mixture, different etch rate, selectivity and etch profile can be obtained. Based on the previous study of dry etching of polycrystalline 3C-SiC by Gao *et al.* [61], [62], two etching recipes for crystalline 4H-SiC have been developed and tested. One common problem of TCP etching of SiC material is the so-called trench effect, which occurs at the bottom of the etched features along the sidewalls. The scanning electron microscopy (SEM) image of the etching profile in Recipe 1 is shown in Figure 3-3. Though a considerably high etch rate of about 120 nm/minute, a high selectivity of 2.3:1 and a profile angle of 80.8° have been achieved, the trench effect cannot be ignored. As shown in Figure 3-3, a trench of 250 nm in depth is observed after the crystalline SiC material has been etched for 1.28 µm. This recipe is preferred in many MEMS process due to the high etch rate and steep profile angle, but the deep trenches will cause many problems in electronic devices. Recipe 2 is then developed for fabricating SiC electronic devices. In Recipe 2, the gas flow of Cl_2 is reduced to 0, which completely removes the trenches. The SEM image of the etching profile using Recipe 2 is shown in Figure 3-4. An etch rate of around 90 nm/minute, a high selectivity of 3:1 and a profile angle of 72° have been achieved using Recipe 2. The two etching recipes are summarized in Table 3-1. As mentioned in the previous section, no etch stop layers exist in between different epitaxial 4H-SiC layers. The etching thickness is controlled by doing a timed etch. Therefore, an etch rate of about 90nm/minutes is preferred though a higher etch rate can be obtained by using a higher bias power.

Table 3-1. Summary of the etching recipes of crystalline 4H-SiC.

	Recipe 1	**Recipe 2**
Chamber Pressure [mtorr]	12	12
TCP Source Power [W]	300	300
Bias Power [W]	150	150
Bottom Electrode Temperature [°C]	40	40
HBr Gas Flow Rate [sccm]	125	200
Cl_2 Gas Flow Rate [sccm]	75	0
Etch Rate [nm/minute]	~ 120	~ 90
Selectivity of SiC/SiO_2	~ 2.3:1	~ 3:1
Profile Angle	81	72

3.2.2 Metallization

For SiC-based devices, one of the critical challenges is to develop chemically and electrically stable ohmic contacts with low electrical resistance. Some important factors need to be taken into consideration, such as surface preparation, choice of metal and annealing temperature. The quality of ohmic contacts is very important for the performance and operation of the devices at high temperature.

Surface preparation is required because the metal needs to be intimately in contact with the semiconductor. Therefore, the sample surface needs to be free of photoresist residue and native oxide. A descum process using oxygen (O_2) plasma was performed after developing exposed photoresist to eliminate any residual scum. Then the sample was dipped in buffered hydrogen fluoride solution for 30 seconds right before it was sent into the chamber for metal deposition. There are different techniques for depositing metal layers. E-beam evaporation is used in this work, which provides high deposition rate, precise control of film thickness and low as-deposited sheet resistance. Sputtering is an alternative option that has better step coverage and good adhesion of the metal to the substrate, but it is hard to precisely control the deposited film thickness. Lift-off process was used to pattern the metal contact. High temperature annealing process was performed at temperatures around 700 – 1050 °C in an oxygen-free ambient for reaction between metal and SiC to form silicides. The choices of metal and high temperature annealing condition are both critical for obtaining good ohmic contacts with low resistivity. For n-type SiC, Ni based metal stacks are commonly used and the typical specific contact resistance is in the range of 10^{-4} – 10^{-5} Ωcm^2 [64]-[69]. For p-type SiC, the specific contact resistance is usually higher than that of n-type. Al based metal stacks are commonly used for p-type SiC and the typical specific contact resistance is in the range of 10^{-3} – 10^{-4} Ωcm^2 [67]-[71].

Transfer Length Method (TLM)

For an ohmic contact with a total contact resistance of R_c, it is usually characterized by specific contact resistance ρ_c given by

$$\rho_c = R_c A, \tag{3.1}$$

where A is the contact area. The benefit of using ρ_c instead of R_c is the capability of evaluating contacts with different contact area.

Transfer length method (TLM) is widely used for the characterization of ohmic contacts. A typical TLM test structure consists of several contacts with unequal spacing between them. The total resistances between adjacent contacts are measured and have a linear dependence on the contact spacing. A schematic of a TLM test structure and a plot of total resistance as a function of contact spacing are shown in Figure 3-5 [72]. TLM test structures are fabricated on the same die together with SiC BJT devices.

For contacts with $L \geq 1.5L_T$, the total resistance R_T between any two contacts can be expressed as

$$R_T = \frac{R_{sh}d}{Z} + 2R_c \approx \frac{R_{sh}}{Z}\left(d + 2L_T\right), \tag{3.2}$$

where R_{sh} is the sheet resistance of the semiconductor, Z is the width of contacts, d is the spacing between any two adjacent contacts and L_T is the transfer length that can be determined as the intercept value with x-axis in Figure 3-5. R_c can also be determined from the TLM measurement as the intercept value with y-axis:

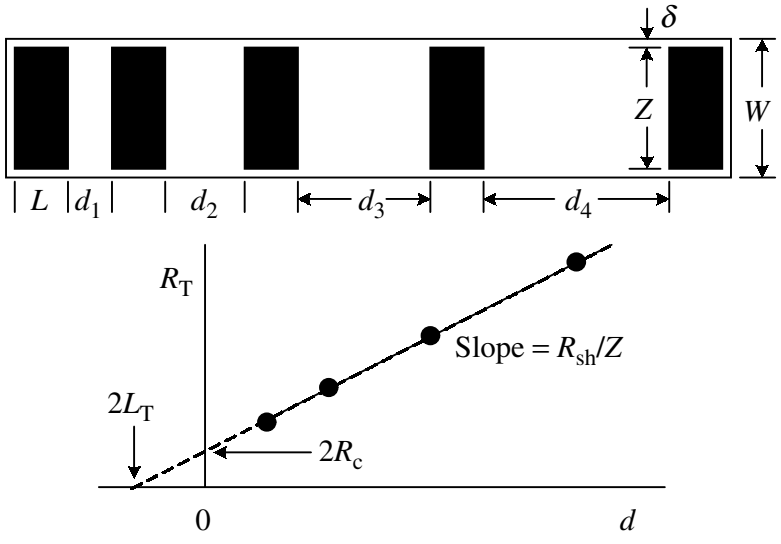

Figure 3-5. Schematic of a transfer length method test structure and a plot of total resistance (R_T) *vs.* contact spacing (d) [72].

$$R_T(d=0) = 2R_c = 2\frac{R_{sh}}{Z}L_T. \tag{3.3}$$

The sheet resistance can be obtained by solving Equation (3.3):

$$R_{sh} = \frac{R_c Z}{L_T}. \tag{3.4}$$

The potential distribution under the contact is such that the voltage is the highest near the contact edge and drops nearly exponentially with distance. The transfer length L_T is defined as the "1/e" distance of the voltage curve:

$$L_T = \sqrt{\rho_c / R_{sh}}. \tag{3.5}$$

Thus, the specific contact resistance ρ_c can also be obtained by TLM:

$$\rho_c = L_T^2 R_{sh}. \tag{3.6}$$

Characterization Results for Ohmic Contacts

Several metal stacks are tested for metal contacts with n-type SiC. Ni gives the best results with the lowest specific contact resistance. Figure 3-6 shows the TLM measurement results for Ni and n-type SiC contacts under different annealing conditions. It can be observed from the plot that annealing the contact at 1000 °C can improve the contact resistance compared to 950 °C. After annealing the contact at 1000 °C for 2 minutes, the contact resistance and specific contact resistance, as extracted by TLM, are 5.14 Ω and 1.37×10^{-4} Ωcm^2 respectively.

For metal contacts with p-type SiC, they are very sensitive to metal composition and annealing temperature. Ni/Ti/Al metal stack is used with a volume ratio of 1:1.5:8.5. The optimized annealing condition is 1 minute at 800 °C in Ar ambient. It is worth noting that there is only a small temperature range within which good ohmic contacts can be obtained. For the same metal stack, if the annealing temperature is lower than 740 °C, the contacts are Schottky-like with very high contact resistance. If the annealing temperature is higher than 820 °C, the color of the metal stack turns black and the contact resistance increases sharply. Figure 3-7 shows the TLM measurement results for Ni/Ti/Al and p-type SiC contacts. After annealing the contact at 800 °C for 1 minute, the contact resistance and specific contact resistance, as extracted by TLM, are 664 Ω and 2.18×10^{-3} Ωcm^2 respectively. It is common that the specific contact resistance of metal contact with p-type SiC is higher than that of metal contact with n-type SiC. The other reason for the high specific contact resistance for metal contact with p-type SiC in this work is due to the moderate doping concentration in the p-region which is 1.8×10^{18} cm^{-3}.

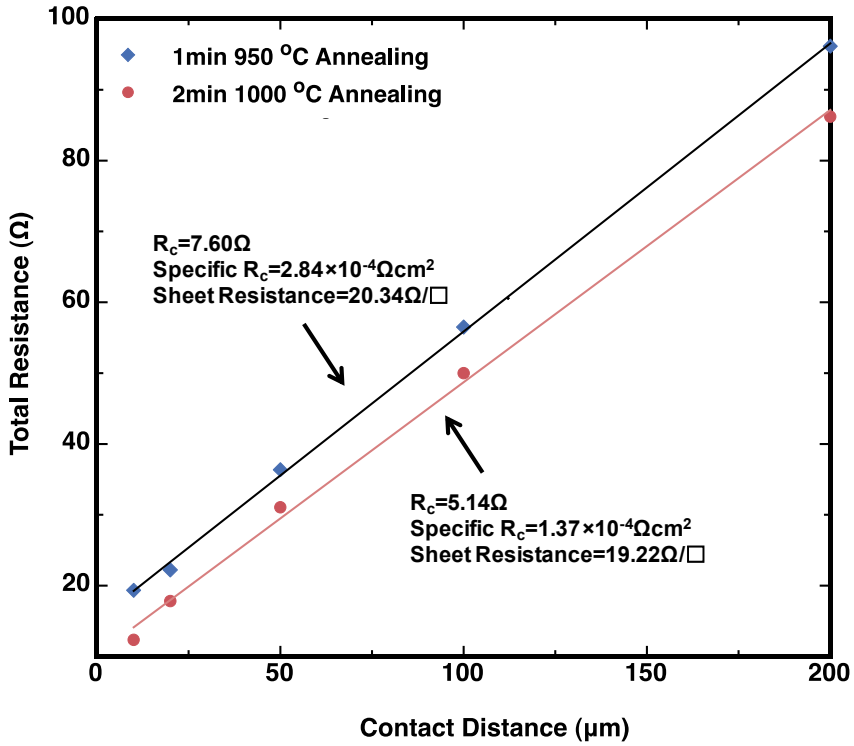

Figure 3-6. TLM measurement results for Ni and n-type SiC contacts under different annealing conditions.

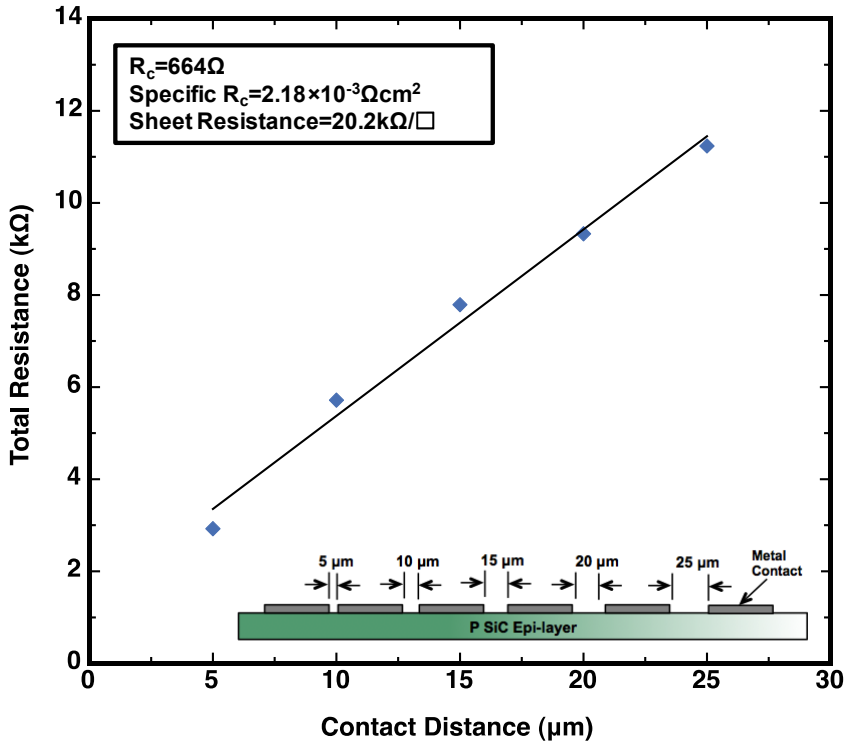

Figure 3-7. TLM measurement results for Ni/Ti/Al and p-type SiC contacts.

3.2.3 Surface Passivation

Dielectrics are needed for surface passivation of SiC devices as well as for gate dielectric layers of metal-oxide-semiconductor field effect transistors (MOSFETs). SiO_2 is an attractive dielectric for SiC devices due to the fact that it can be formed simply by thermal oxidation of SiC. However, improving the quality of the dielectric is still a challenging issue despite of significant progress in recent years.

Two possible chemical reactions are proposed for thermal oxidation of SiC at the interface [1]:

$$SiC + \frac{3}{2}O_2 \leftrightarrow SiO_2 + CO, \tag{3.1}$$

$$SiC + O_2 \leftrightarrow SiO_2 + C. \tag{3.2}$$

The thermal oxidation of SiC shows lower oxidation rate and needs higher temperature compared with Si due to the strong bond between Si and C. The oxidation rate is higher for C face compared with Si face [73]. But the oxide grown on the Si face is usually better in terms of electrical quality. Therefore, Si face is preferred for building devices. Unlike Si, one of the concerns of the thermal oxidation of SiC is the excess carbon. Though most of the carbon is removed during the oxidation process as CO gas, carbon clusters could still form at the SiO_2/SiC interface, which seriously degrade the quality of the dielectric layer [74]. This problem is more noticeable in 4H-SiC than in 6H-SiC [75], [76], [81].

Table 3-2. Summary of interface state densities for SiO_2/SiC interfaces.

Polytype	Process Condition	Interface State Density	Reference
4H	Dry/Wet Oxidation	2×10^{13} $cm^{-2}eV^{-1}$	[81]
4H	Dry/Wet Oxidation + NO Anneal	2×10^{12} $cm^{-2}eV^{-1}$	[81]
6H	Dry/Wet Oxidation	2×10^{12} $cm^{-2}eV^{-1}$	[81]
6H	Dry/Wet Oxidation + NO Anneal	2×10^{12} $cm^{-2}eV^{-1}$	[81]
4H	Dry Oxidation	1.3×10^{13} $cm^{-2}eV^{-1}$	[77]
4H	Oxidation in N_2O	2.3×10^{12} $cm^{-2}eV^{-1}$	[77]
4H	PECVD + N_2O anneal	4.3×10^{11} $cm^{-2}eV^{-1}$	[77]
4H	Dry Oxidation	$\sim 10^{13}$ $cm^{-2}eV^{-1}$	[82]
4H	Dry Oxidation + NO Anneal	$\sim 10^{12}$ $cm^{-2}eV^{-1}$	[82]
4H	CVD + Ar Anneal	3×10^{12} $cm^{-2}eV^{-1}$ (at $E_c - 0.2$ eV)	[86]
4H	CVD + N_2O Anneal	3×10^{11} $cm^{-2}eV^{-1}$ (at $E_c - 0.2$ eV)	[86]
4H	Oxidation in N_2O	7×10^{11} $cm^{-2}eV^{-1}$ (at $E_c - 0.2$ eV)	[86]
4H	Oxidation in NO + Oxidation in Dry O2 + NO Anneal	3×10^{11} $cm^{-2}eV^{-1}$	[78]

Many efforts have been made to improve the quality of the SiO_2/SiC interface. One promising method to reduce the density of interface states is nitridation of the oxide. This can be done by thermally growing the oxide in nitric oxide (NO) or nitrous oxide (N_2O) [77]-[79], annealing the thermally grown oxide in NO or N_2O [77], [81]-[85], or annealing the deposited oxide in NO or N_2O [77], [86], [87]. According to the work by Jamet *et al.*, nitridation process can provide critical improvements on the quality of SiO_2/SiC interface because: 1) NO and N_2O are able to passivate the dangling Si bonds and replace the strained bonds with S≡N bonds, and 2) NO and N_2O can help to remove the excess carbon and associated silicon-oxycarbon bonds from the interface [88]. The interface state density of the SiO_2/SiC interface has been studied and characterized by many research groups, and the results are summarized in Table 3-2. The numerical and experimental characterization shows that the profile of interface state density usually exponentially increases at the conduction band edge and the valence band edge [89], [90]. The typical interface state density in SiC devices ranges from 10^{11} to 10^{13} $cm^{-2}eV^{-1}$. The number is much higher compared with Si devices, which is on the order of 10^{10} $cm^{-2}eV^{-1}$. More investigation into improving the interface quality is still urgently needed for SiC devices.

For SiC BJTs, the quality of the interface between SiC and the surface passivation layer has a significant impact on the device performance, especially on current gain. This is because the recombination current caused by interface traps at the extrinsic base surface and along the base-emitter junction sidewall can be a main component of the base current. By reducing the density of interface traps, the recombination current caused by interface traps is reduced. Therefore, the base transport factor α_T is increased and higher current gain can be achieved. Due to the limitation of the highest temperature allowed in the furnaces, PECVD oxide without high temperature annealing is used in this work. The impact of the interface traps on the current gain is discussed in Chapter 4.

3.3 Conclusions

In this chapter, the baseline six-mask microfabrication process for SiC BJTs is presented. Several key steps in the fabrication process flow are discussed. For the etching process of SiC, TCP etching was employed using SiO_2 as the mask material. In order to avoid the trenching effect, HBr and Cl_2 based etching chemistry was studied. Good sidewall profile and high selectivity were obtained by using the optimized recipe. Metallization process was also studied because the quality of ohmic contacts is very important for the performance and operation of the devices. Ni was used for n-type SiC contacts and Ni/Ti/Al metal stack was used for p-type SiC contacts. High temperature annealing process was optimized for getting good ohmic contacts. The contacts were characterized using transfer length method. Some issues with the surface passivation method were addressed and discussed. Carbon clusters could form at the SiO_2/SiC interface during the oxidation process, which severely degrade the quality of the dielectric layer. Though nitridation of the oxide has been proved to be effective in reducing the interface state

density, more investigations into improving the interface quality are needed. These fabrication processes are employed to manufacture the SiC BJTs presented in Chapter 4.

Chapter 4

Simulation and Characterization Results of 4H-SiC Bipolar Junction Transistors

There are growing interests on developing high temperature integrated circuit using SiC BJTs. This is because the superior material properties of SiC allow SiC based semiconductor devices to be functional at extremely high temperatures. Also, SiC BJTs are not as strongly affected by oxide quality as SiC MOSFETs. Additionally, SiC BJTs are normally-off devices and have higher transconductance compared with SiC JFETs. In this chapter, design, characterization and simulation results of 4H-SiC BJTs are discussed. The device was first characterized at room temperature. Then high temperature characterization was performed. Comprehensive characterization including current gain, early voltage and intrinsic voltage gain are described. It has been found that the current gain of the device is reduced at elevated temperature. On the other hand, the output resistance increases when temperature rises. The intrinsic voltage gain is higher at 400 °C compared with at room temperature, suggesting 4H-SiC BJT has the potential to be used as a voltage amplifier at extremely high temperatures. The high temperature effects in 4H-SiC are studied to explain the high temperature performance of the device. The effects of SiC/SiO_2 interface traps on the electrical characteristics of SiC BJTs are also discussed.

4.1 Device Structure

The schematic cross-sectional illustration of the 4H-SiC BJT is shown in Figure 4-1 (a). The structure has 5 epitaxial layers grown on a 4° off-axis Si-face n-type 4H-SiC wafer. The emitter region is formed by a 1-μm-thick N+ 4H-SiC epitaxial layer doped at 10^{19} cm^{-3}, the base region is formed by a 0.3-μm-thick P-type epitaxial layer doped at 1.8×10^{18} cm^{-3}, and the collector region is formed by a 1-μm-thick N- epitaxial layer doped at 10^{16} cm^{-3}. The highly doped N+ epitaxial layer under the N- collector is the sub-collector region, which is used to form the collector contact on the topside of the structure. Finally, the P+ region grown on the 4H-SiC substrate enables junction isolation for

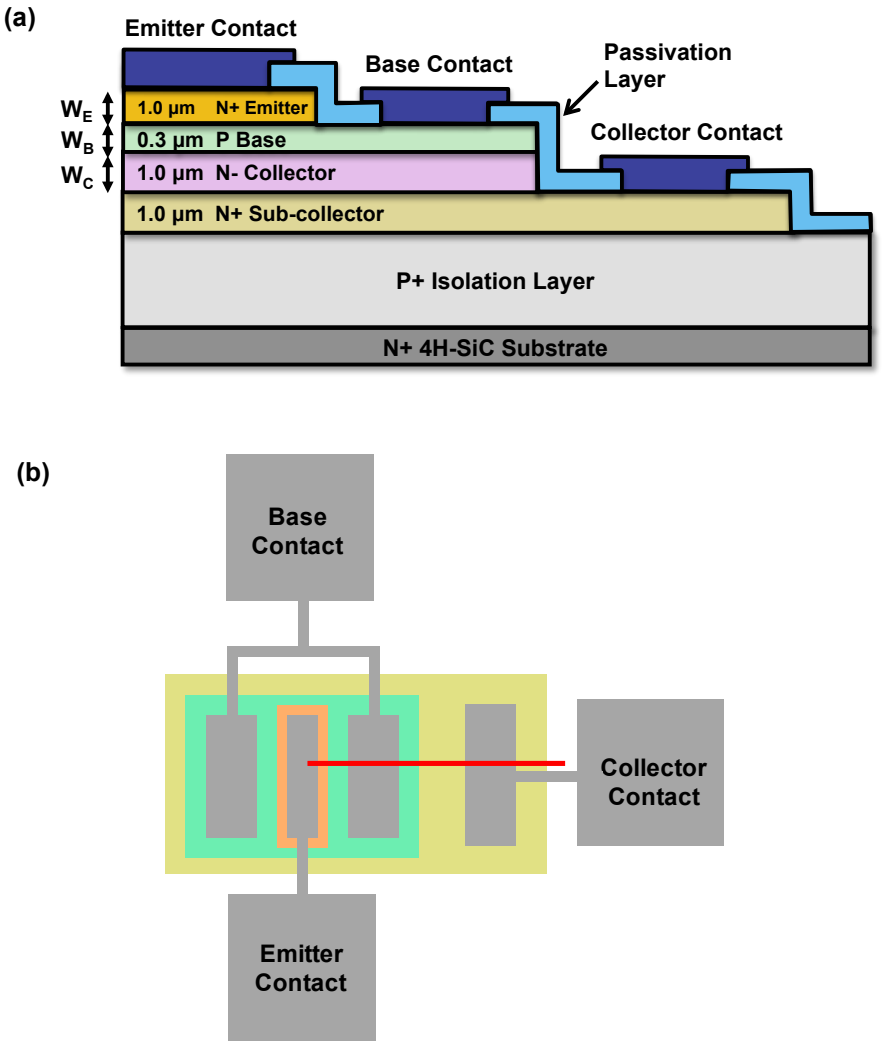

Figure 4-1. (a) Cross-sectional schematic and (b) schematic top view of the 4H-SiC BJT. The red line in (b) indicates the position of the cross-section in (a).

separate BJT devices. Figure 4-1 (b) shows the schematic top view of the device. By having all the metallic contacts at the top of the structure, the proposed BJT can be easily integrated into large-scale circuits for sensing applications. It is also worth noticing that the device has two base contact regions. As discussed in Chapter 3, the metal contact with p-type SiC has higher contact resistance compared with the metal contact with n-type SiC. By having double base contacts, the contact resistance can be reduced.

The thickness and doping concentration of the epitaxial layers are designed to have high current gain β and high output resistance r_o. This is because the devices developed in this work are used for high temperature sensing applications that usually require low voltage, analog integrated circuits.

As we have discussed in Chapter 1, the operating mechanism of bipolar junction transistors is quite complicated. In order to get a simplified expression for the current gain β, several assumptions have to be made: 1) the epitaxial layers are nondegenerate and uniformly doped; 2) the transistor is under steady-state condition; 3) low-level injection prevails in the quasineutral regions; 4) there is no photogeneration in the semiconductor regions; 5) thermal generation and recombination can be ignored in the depletion regions; 6) the quasineutral widths of the emitter and collector are greater than the minority carrier diffusion lengths in these regions; 7) $W_B/L_B << 1$. The current gain β of a NPN BJT can be derived as

$$\beta = \frac{1}{\frac{D_E}{D_B}\frac{N_B}{N_E}\frac{W_B}{L_E} + \frac{1}{2}\left(\frac{W_B}{L_B}\right)^2}, \tag{4.1}$$

where D_B is the diffusion coefficient of electrons in the base region and D_E is the diffusion coefficient of holes in the emitter region, N_B and N_E are the effective doping concentrations in the base and emitter regions, L_B is the diffusion length of electrons in the base region and L_E is the diffusion lengths of holes in the emitter region, W_B is the width of the base region. For the emitter region, a heavily doped emitter with the emitter width greater than the diffusion length of the minority carrier is desired. Combined with fabrication considerations, the emitter doping concentration is set at 10^{19} cm^{-3}, and the emitter width is chosen to be 1 μm. Also, a lightly doped base region with thin base width is preferred for improving the current gain.

The base width W_B changes with the applied voltages. This phenomenon is known as *base width modulation effect* or *early effect*. The output resistance r_o can be calculated by

$$r_o = \left(V_A + V_{CE}\right) / I_C, \tag{4.2}$$

where V_A is the early voltage, V_{CE} is the applied voltage between the collector and the emitter, and I_C is the current flowing through the collector under DC bias. In order to get high output resistance, low collector doping and high base doping are required. Also, the width of the collector region should be greater than the diffusion length of the minority carriers, while the base width should be as wide as possible. In this work, the collector doping concentration is 10^{16} cm^{-3}, and the collector width is 1 μm. It is worth noting that there are trade-offs for the design of the base region. A base doping of 1.8×10^{18} cm^{-3} was used to get a high output resistance. Additionally, this doping concentration allows good ohmic contact to the base layer without an ion implantation process. A thin base of 0.3 μm was utilized for a higher current gain. Figure 4-2 is a scanning electron microscopy (SEM) image of the cross-sectional view showing the thickness of each epitaxial layer. Figure 4-3 shows the SEM image of the fabricated device. The dimension of the emitter region is 60 μm × 100 μm.

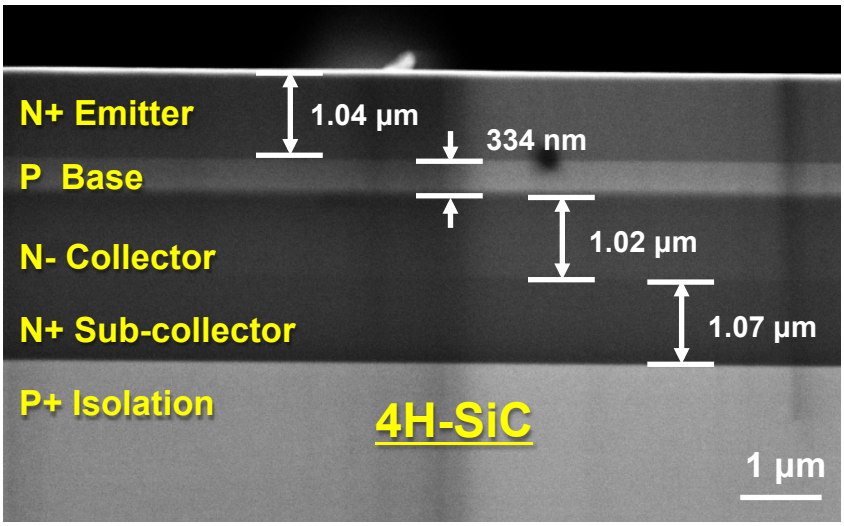

Figure 4-2. SEM image of the cross-section view showing the thickness of each epitaxial layer.

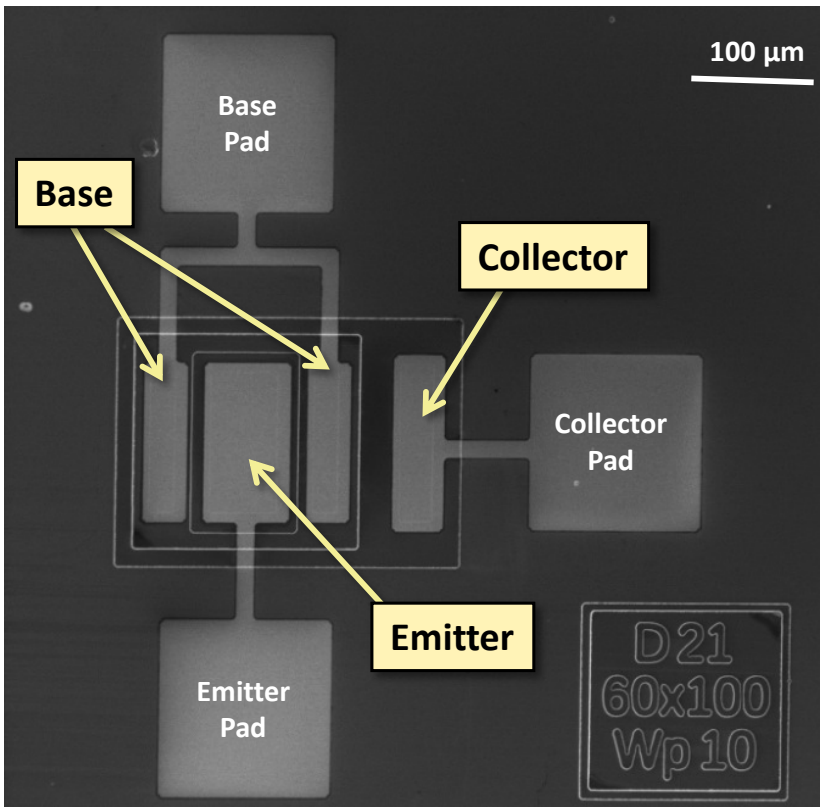

Figure 4-3. SEM image of the fabricated 4H-SiC BJT.

4.2 Room Temperature Characterization of the 4H-SiC BJT

The fabricated 4H-SiC BJT was first characterized at room temperature. Figure 4-4 shows the forward output characteristics of the device at 20 °C. While taking this measurement, the emitter is grounded. Different base currents from 0 μA to 200 μA with a 50 μA step were applied. At each base current, the collector voltage is swept from 0 V to 15 V. The dark cyan line in Figure 4-4 shows the collector current (I_C) *vs.* collector-emitter voltage (V_{CE}) curve at $I_B = 0\ \mu A$. A high transconductance (G_m) of 56 mS was reached at $I_C = 1.4\ mA$, and the output resistance r_o was extracted to be 50 kΩ. The intrinsic voltage gain (A_v), which is the product of G_m and r_o, is 2800 under room temperature at $I_C = 1.4\ mA$ and $I_B = 200\ \mu A$.

Figure 4-5 depicts the Gummel plot and the current gain (β) *vs.* base-emitter voltage (V_{BE}) curve under room temperature. The emitter was grounded when this measurement was taken. Also, the base voltage and collector voltage simultaneously increased from 0 to 20 volts. The base-collector junction is zero biased for all the measurements, *i.e.* $V_{CB} = 0\ V$. The current gain increases with V_{BE}, and the maximum value of the current gain is 12.4 at room temperature.

4.3 High Temperature Effects in 4H-SiC

To understand the device behavior at elevated temperatures, the high temperature effects on basic semiconductor physical properties need to be studied. As discussed in Chapter 2, nearly all the properties of semiconductors can change with temperature. For 4H-SiC BJTs, there are two effects that have the greatest impacts on the device performance. One is the *incomplete ionization effect*, which determines the carrier concentration in the semiconductor. The other one is the temperature dependence of the carrier lifetime.

4.3.1 Temperature Dependence of Carrier Concentration

For an extrinsic semiconductor (doped semiconductor), the carrier concentrations in the semiconductor are mainly controlled by the ionized impurity concentration and the intrinsic carrier concentration. In Si, most impurity levels, like Boron (B) and Phosphorus (P), are shallow enough so that the dopants can be considered fully ionized at room temperature. As discussed in Chapter 2, the donor level (E_D) for nitrogen (N) and acceptor level (E_A) for aluminum (Al) in SiC are relatively deep compared to the thermal energy kT. For 4H-SiC, a single donor level, $E_D = 65\ meV$ below the conduction band edge is assumed after simplification, and an acceptor energy level is $E_A = 191\ meV$ above the valence band edge. Therefore, the dopants cannot be considered fully ionized at room temperature and the concentration of the ionized dopants increases with rising temperature.

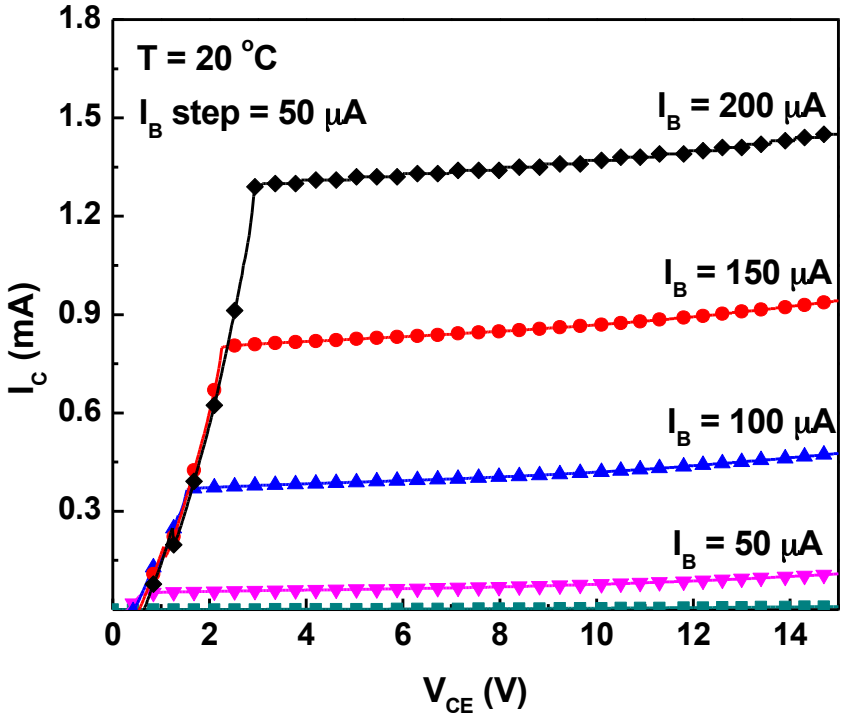

Figure 4-4. Measured forward output characteristics (I_C-V_{CE}) with I_B from 0 μA to 200 μA at room temperature (20 °C).

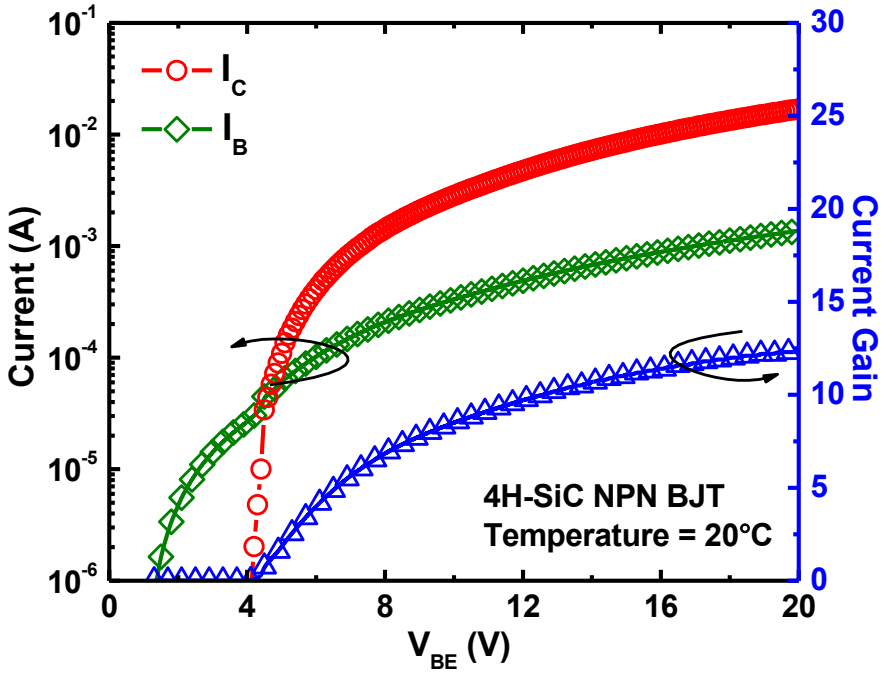

Figure 4-5. Measured SiC BJT base and collector current (I_B and I_C) and current gain (β) *vs.* base-emitter bias (V_{BE}) at room temperature.

To preserve electrical charge neutrality, the total positive charge and the total negative charge must be equal to each other. For n-type SiC, the ionized donors are positively charged. The charge neutrality relationship is given by

$$n = N_D^+ + p, \tag{4.3}$$

where n is the electron concentration, p is the hole concentration, and N_D^+ is the ionized donor concentration which is given by Equation (2.16). The electron and hole concentrations can be calculated from

$$n = n_{i,eff} \exp\left(\frac{E_F - E_i}{kT}\right), \tag{4.4}$$

$$p = n_{i,eff} \exp\left(\frac{E_i - E_F}{kT}\right), \tag{4.5}$$

where E_F is the Fermi energy or Fermi level, E_i is the intrinsic Fermi level, and $n_{i,eff}$ is the effective intrinsic carrier concentration which is given by Equation (2.4).

Substituting for n, p and N_D^+ in Equation (4.3) using Equation (4.4), Equation (4.5) and Equation (2.16), yields

$$n_{i,eff} \exp\left(\frac{E_F - E_i}{kT}\right) = \frac{N_D}{1 + g_D \exp\left(\frac{E_F - E_D}{kT}\right)} + n_{i,eff} \exp\left(\frac{E_i - E_F}{kT}\right). \tag{4.6}$$

Fermi level and carrier concentrations can be determined by solving Equation (4.6). Similar method can be used to calculate the carrier concentrations in the p-type SiC.

This model is used to calculate the electron concentration in the N+ emitter region and the hole concentration in the P base region. Figure 4-6 shows how the carrier concentrations vary with temperature. In the base region with a doping concentration of 1.8×10^{18} cm^{-3}, the hole concentration at room temperature is 8.0×10^{16} cm^{-3}, which suggests that only 4% of the dopants are ionized. When temperature increases to 400 °C, the hole concentration becomes 8.6×10^{17} cm^{-3}, which shows that the hole concentration is increased by 10.8 times. On the other hand, the electron concentration in the emitter region with a doping concentration of 10^{19} cm^{-3} is 2.7×10^{18} cm^{-3} at room temperature. This value increases by 2.6 times to 7.0×10^{18} cm^{-3} at 400 °C.

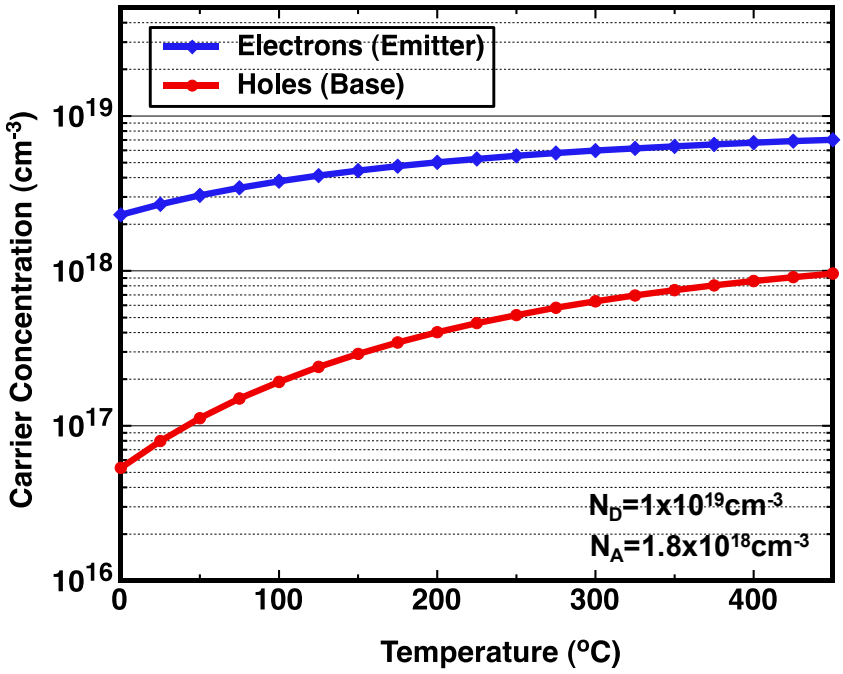

Figure 4-6. Simulated carrier concentration *vs.* temperature in the base and the emitter regions.

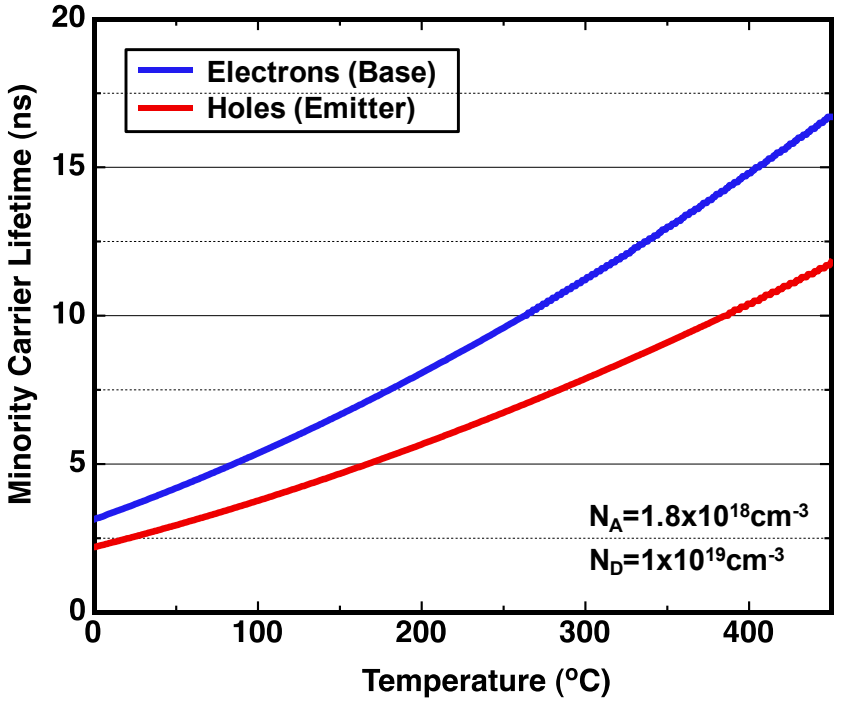

Figure 4-7. Simulated minority carrier lifetime *vs.* temperature in the base and the emitter regions.

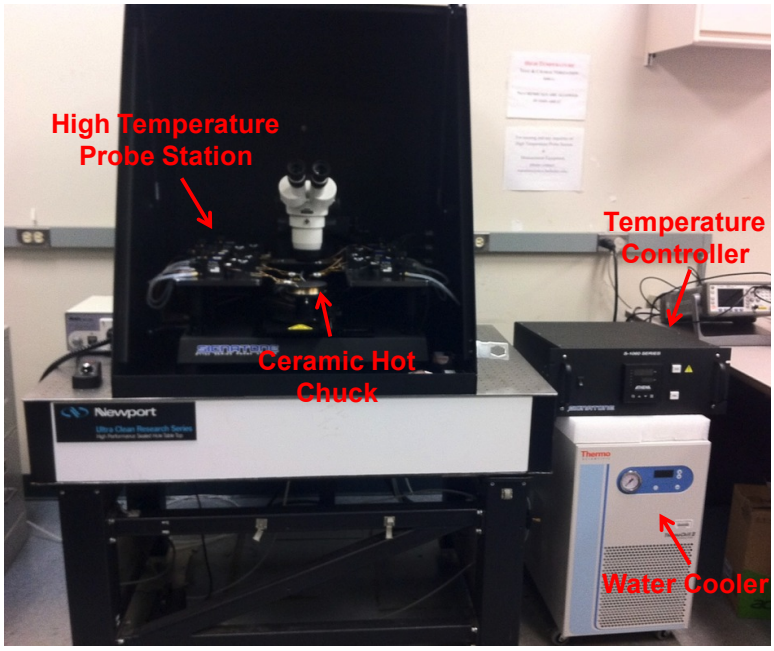

Figure 4-8. High temperature probe station made by Signatone.

4.3.2 Temperature Dependence of Carrier Lifetime

The minority carrier lifetimes in 4H-SiC depend on temperature and doping level, which can be modeled by Equation (2.20). The carrier lifetimes increase exponentially with rising temperature. The mechanism is still unknown and there is limited study on this topic. The parameters for the temperature dependence are taken from [41] and [50]. Figure 4-7 shows the simulation results on the temperature dependence of the minority carrier lifetimes in the base and emitter regions when $\tau^{max}_{n,p} = 10\ ns$. In the base region, the minority carrier lifetime (electron lifetime) increases from 3.5 ns at room temperature to 14.8 ns at 400 °C. In the emitter region the minority carrier lifetime (hole lifetime) increases from 2.5 ns at room temperature to 10.4 ns at 400 °C. At a given temperature, the electron lifetime in the emitter region is lower than the hole lifetime in the base region due to higher doping concentration in the N+ emitter.

4.4 High Temperature Characterization of 4H-SiC BJTs

The fabricated device was characterized at elevated temperatures using a high temperature probe station made by Signatone together with an Agilent B2912A Precision Source/Measurement Unit. The high temperature probe station is shown in Figure 4-8. It consists of a ceramic hot chuck, a temperature controller and a water cooler. Figure 4-9 shows the forward output characteristics of the 4H-SiC BJT with I_B from 0 μA to 600 μA

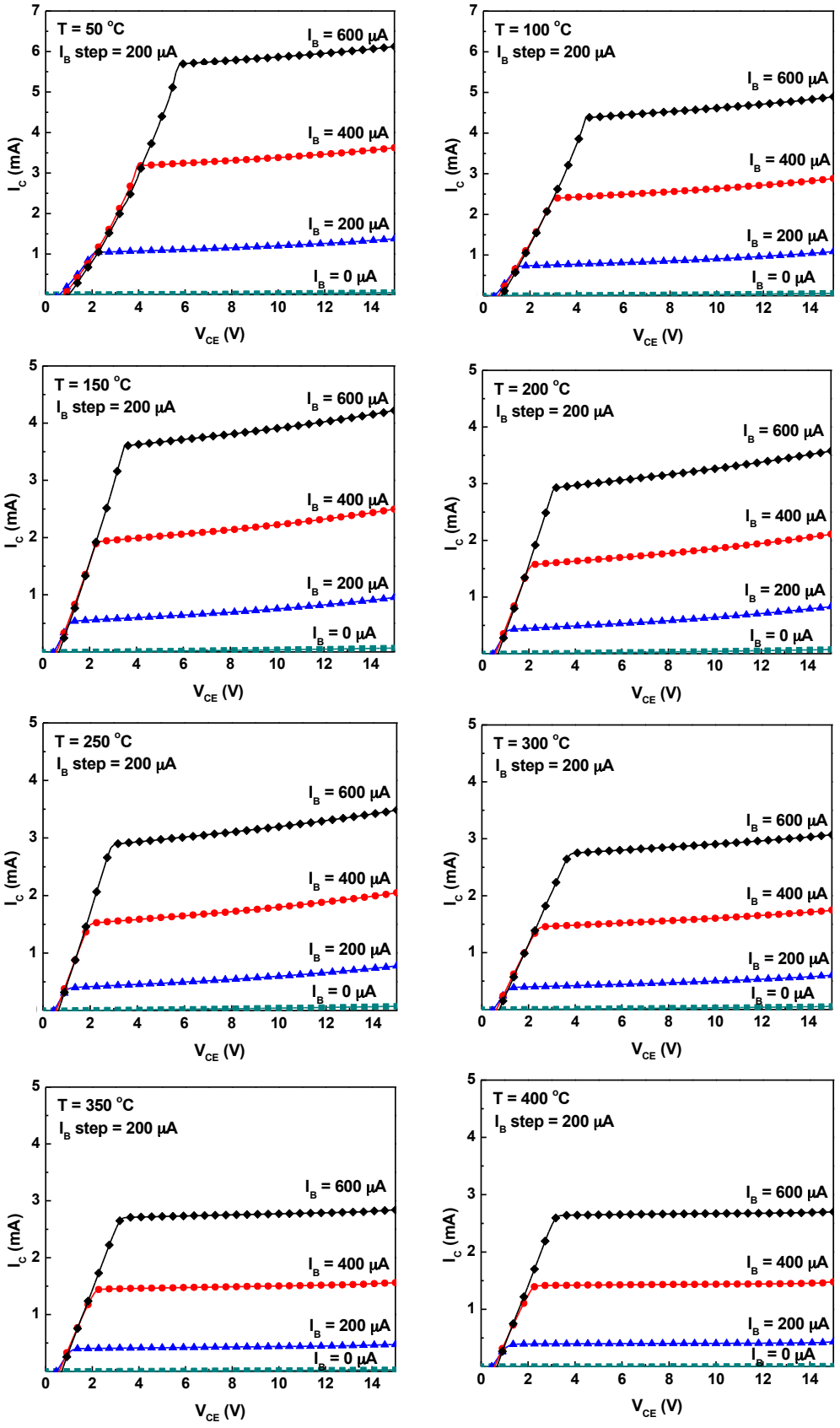

Figure 4-9. Measured forward output characteristics at different temperatures.

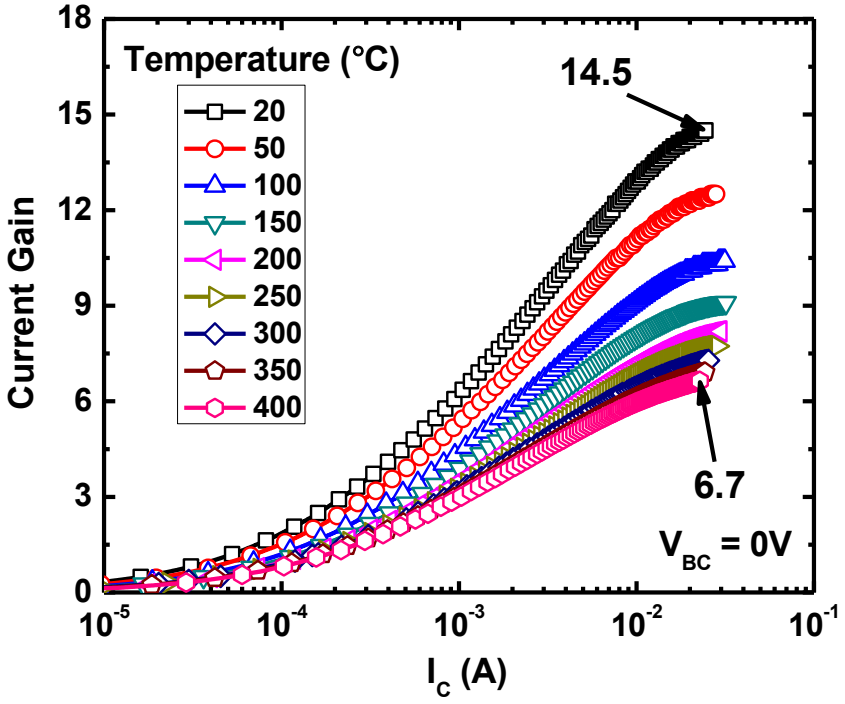

Figure 4-10. Measured SiC BJT current gain *vs*. collector current at different temperatures (up to 400 °C).

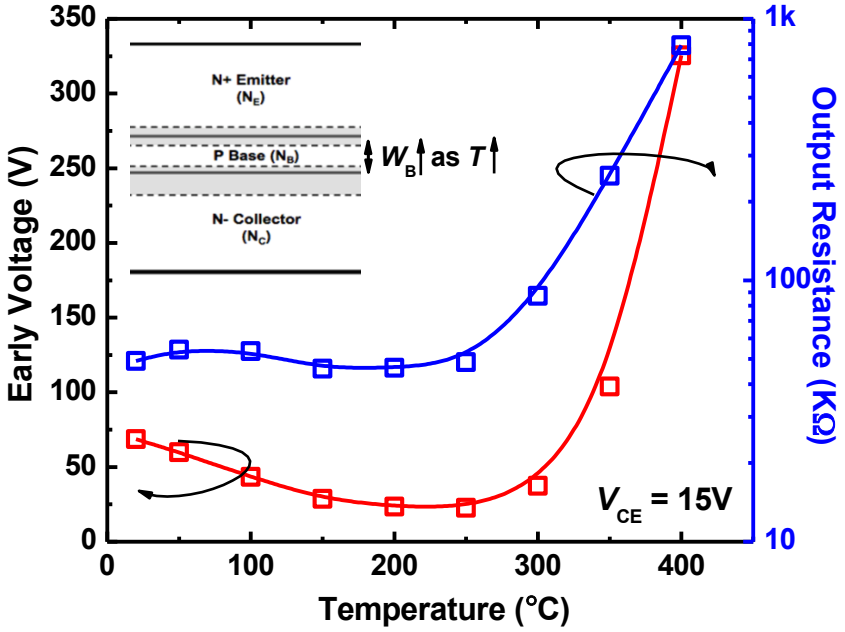

Figure 4-11. Measured SiC BJT early voltage (V_{EA}) and output resistance (r_o) *vs*. temperature; the inset illustrates the base width (W_B) widening effect at elevated temperatures.

with a 200 μA step over a temperature range from 50 °C to 400 °C. The device shows stable operation over the entire temperature range. At the same base current, the collector current decreases with increasing temperature, which corresponds to lower current gain at elevated temperatures. In addition, the slopes of the collector current curves in the saturation region decrease with rising temperature, which corresponds to higher output resistance at elevated temperatures.

The plot of current gain (β) *vs*. collector current (I_C) at different temperatures is shown in Figure 4-11. The maximum β degrades from 14.5 at 20 °C to 6.7 at 400 °C. The two high temperature effects discussed in Section 4.3 have the greatest impacts on the high temperature performance of the device. They compete with each other for the change of the current gain with rising temperature. One effect is the temperature dependence of carrier concentration. Due to the incomplete ionization effect, the impurities are only partially ionized at relatively low temperatures. Thus, the carrier concentration increases with increasing temperature as more dopants are ionized. As calculated in Section 4.3.1, only 4% of the acceptors are ionized under room temperature in the base region, and the hole concentration is increased by 10.8 times at 400 °C. On the other hand, the electron concentration in the emitter region increases by only 2.6 times at 400 °C compared with the value at room temperature. From Equation (4.1), it can be seen that higher N_B/N_E value at high temperature will end up with lower β. The other effect is the temperature dependence of carrier lifetime. The minority carrier lifetimes in the base and emitter regions increase exponentially with rising temperature. Since the diffusion length L is proportional to $\sqrt{\tau}$, L_E and L_B increase when temperature goes up. Thus, β increases with increasing temperature as indicated in Equation (4.1). Since the degradation of current gain with increasing temperature up to 400 °C was observed in the measurement results, the incomplete ionization effect is believed to play a more important role at high temperatures.

To comprehensively evaluate the device's performance for high temperature sensing applications, more characterization was performed. Figure 4-11 illustrates that the early voltage and output resistance of the device increase with rising temperature. This is because both the equivalent base doping concentration and base width increase with temperature. The intrinsic voltage gain (A_v) *vs*. temperature is plotted in Figure 4-12. A_v is calculated when $I_B = 200\ \mu A$ at all the temperatures. A_v first decreases from 3300 at 20 °C to 837 at 250 °C due to transconductance (G_m) degradation, then it increases rapidly to 5900 at 400 °C due to the enhancement in output resistance (r_o). The result shows that the device has even higher intrinsic voltage gains at high temperatures, which demonstrates the potential of 4H-SiC BJTs to be used as voltage amplifiers at extremely high temperatures.

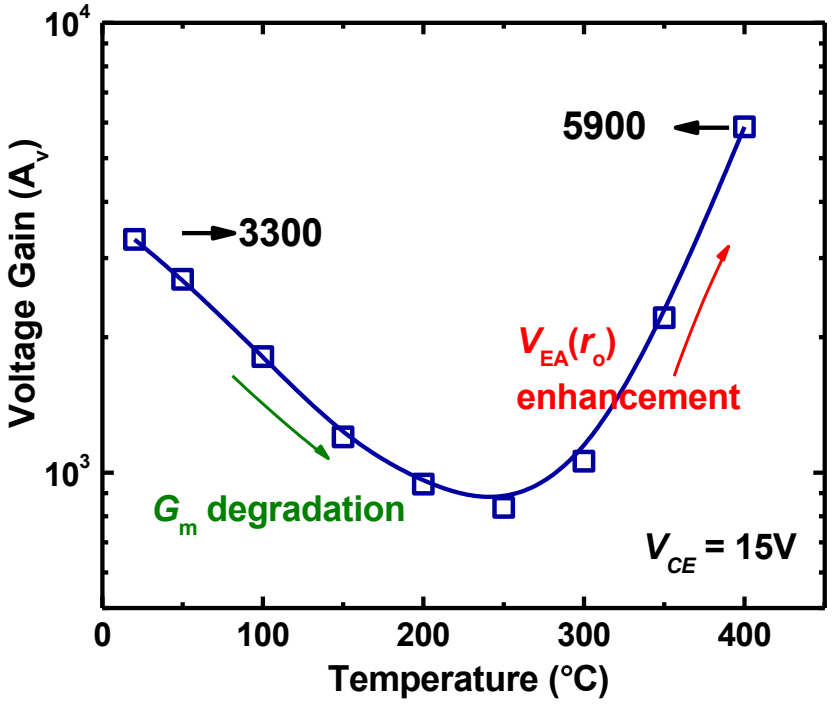

Figure 4-12. Measured SiC BJT voltage gain (A_v) *vs*. temperature.

4.5 Effects of SiC/SiO_2 Interface Traps

As discussed in Section 3.2.3, the quality of the interface between SiC and the surface passivation layer has a significant impact on the device performance of 4H-SiC BJTs, especially on the current gain. This is because the recombination current caused by

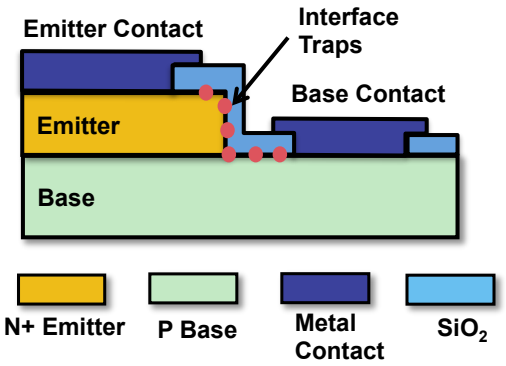

Figure 4-13. Schematic cross-sectional view of the 4H-SiC BJT presenting where the interface traps physically reside in the device.

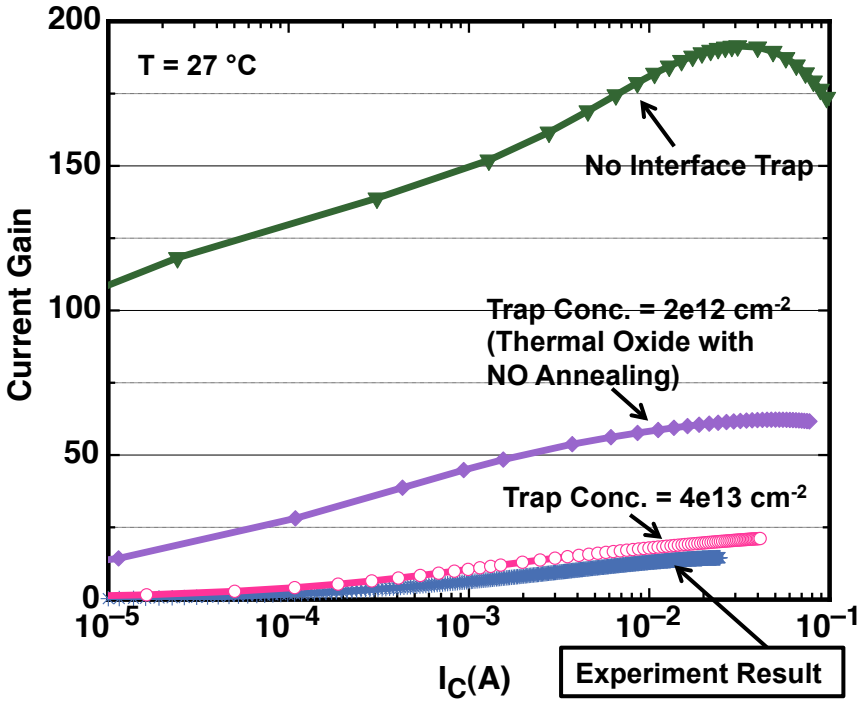

Figure 4-14. TCAD simulation results of SiC BJT current gain *vs*. collector current with different trap concentrations.

interface traps at the extrinsic base surface and along the base-emitter junction sidewall can be a main component of the base current. Due to the remaining carbon cluster at the SiO_2/SiC interface during the oxidation process, serious degradation of the dielectric layer quality is observed. High temperature annealing of the oxide in NO or N_2O has been proved to be an effective way to improve the quality of the interface. By reducing the density of interface traps, the recombination current caused by interface traps is reduced. Therefore, the base transport factor α_T is increased and higher current gain can be achieved. Figure 4-13 shows the schematic cross-sectional view of the 4H-SiC BJT presenting where the interface traps physically reside in the device.

2D numerical simulation using Sentaurus TCAD tools was performed to study the effects of SiC/SiO_2 interface traps. Figure 4-14 shows the simulation results of current gain (β) *vs*. collector current (I_C) with different trap concentrations. It is worth noting that, in theory, a maximum current gain of 191 can be achieved if the interface is perfect. This simulation result demonstrates the big impacts of interface traps on the current gain. By fitting to the experimental data, a trap concentration of 4×10^{13} $cm^{-2}eV$ can be extracted for the fabricated device. Since the typical interface state density after the nitridation process of the oxide is on the order of 10^{12} $cm^{-2}eV$, an interface trap density of 2×10^{12} $cm^{-2}eV$ is used to predict the expected current gain after improving the surface passivation process. The simulation results suggest that by performing the commonly used nitridation process, the current gain of the proposed device can be enhanced significantly. We plan to investigate this further in future work.

4.6 Conclusions

In this chapter, theoretical analysis, design and characterization of 4H-SiC NPN BJTs are presented. The device shows stable operation at high temperatures up to 400 °C. Comprehensive characterization including current gain, early voltage, and intrinsic voltage gain was performed. At elevated temperatures, although the current gain of the device is reduced, the output resistance increases. At 400 °C, an intrinsic voltage gain of 5900 is achieved, which is even higher than 3300 at room temperature. This phenomenon suggests that 4H-SiC BJT has the potential to be used as a voltage amplifier at extremely high temperatures. The high temperature effects of 4H-SiC are also studied. Higher current gain could be obtained if the surface passivation process is improved. This work shows that 4H-SiC BJT is a promising technology for harsh environment sensing applications.

Chapter 5

Fabrication and Characterization of SiC PN Diode for High Temperature Sensing Applications

Temperature sensing under extreme environments is important to various industrial applications. Among different types of temperature sensors, semiconductor diode sensors have the advantages of high sensitivity and compatibility with integrated circuits. Thanks to the superior material properties of SiC, semiconductor diodes made by SiC have been investigated as high temperature sensors. SiC Schottky diodes have been previously demonstrated as viable temperature sensors that can work up to 400°C [91]-[93]. However, SiC Schottky diode suffers from reliability issues of the Schottky contact as well as high leakage current at elevated temperatures. On the other hand, SiC pn junction is very stable and theoretically permits device operation at junction temperatures exceeding 800°C [14]. Hence, the temperature sensor based on SiC pn diode is a perfect candidate for operation at elevated temperatures [94]. In this chapter, a high-performance temperature sensor based on 4H-SiC pn diode is demonstrated. The device is capable of stable operation in a temperature range from 20 °C up to 600 °C. In forward biased region, the forward voltage of the 4H-SiC pn diode shows linear dependence on temperature at a constant current. This dependence is utilized to sense temperature variations and the proposed device achieves a sensitivity of 3.5 mV/°C. This type of temperature sensor can be integrated with supporting circuitries to build a sensing module that is capable of working at extremely high temperatures.

5.1 Fundamentals of PN Junction Diode

A pn junction is formed between two regions in a single crystal of semiconductor material with different doping concentrations. PN junctions are of great importance in modern electronics. They are the basic building blocks of most semiconductor devices. It is essential to know the fundamentals of pn junction diode in order to understand the

sensing mechanism of the temperature sensor. In this section, the electrostatics under equilibrium is first discussed. The subsequent segments are then devoted to current conduction mechanisms and current-voltage characteristics.

5.1.1 PN Junction Electrostatics Under Equilibrium

Suppose that the p- and n- regions are initially separated. Then a structurally perfect connection is made between these two regions. Since there are more holes in the p-region than in the n-region, the holes tend to diffuse into the n-side. As holes diffuse, they leave behind ionized acceptors, which are immobile (fixed within semiconductor lattice sites). Likewise, electrons from the n-region near the metallurgical junction begin to diffuse into the p-region, leaving fixed ionized donors in the n-region. Consequently, the near-vicinity of the metallurgical junction loses their neutrality and holds a significant non-zero charge, forming the space charge region or depletion region. The diffusion process generates more space charge, whereas the drift current associated with the electric field generated by the space charge counteracts the diffusion. The build-up of charge continues until the carrier diffusion and drift components balance each other out. Then the equilibrium condition is established. A conceptual pn junction and the energy band diagram under equilibrium are illustrated in Figure 5-1. The voltage drop across the depletion region under equilibrium conditions is called *built-in potential* (V_{bi}) [96].

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2} \right), \tag{5.1}$$

where q is the electric charge, k is Boltzmann constant, T is the temperature in Kelvin, N_D and N_A are the doping concentrations in n- and p-region , n_i is the intrinsic carrier concentration.

The total width of the space-charge or depletion region, also known simply as the *depletion width*, is given by

$$W_{dep} = \left[\frac{2\varepsilon_s \varepsilon_0}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) V_{bi} \right]^{1/2}, \tag{5.2}$$

where ε_s is the relative permittivity of the semiconductor material, and the ε_0 is the vacuum permittivity.

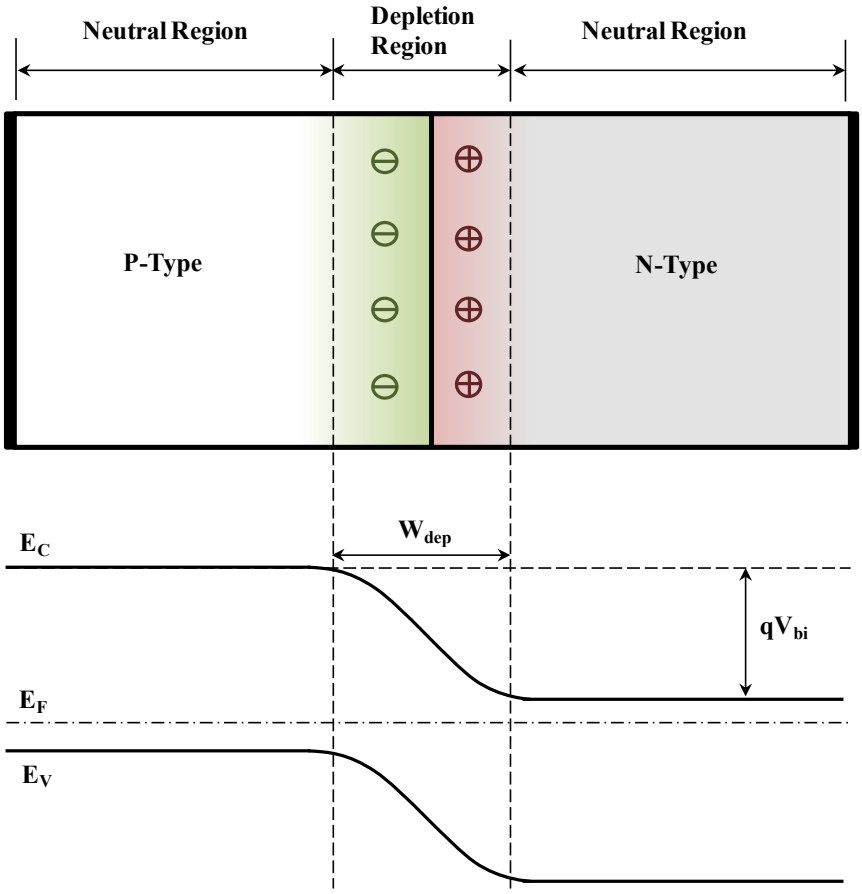

Figure 5-1. Conceptual pn junction and equilibrium energy band diagram.

5.1.2 Current Conduction Mechanisms

Several current transport mechanisms may occur at the same time in pn diodes. The ideal current-voltage characteristics are derived by Shockley [97] based on four assumptions: (1) the pn junction is abrupt; (2) Boltzmann approximation is valid throughout the depletion layer; (3) the injected minority carrier densities are much smaller than the majority carrier densities; (4) no generation in the depletion region. The current describe by the ideal diode equation is commonly referred to as the *diffusion current*.

However, the measurement results usually differ from the prediction by the ideal diode equation. One of the important effects that are responsible for the departure from the ideal is the generation and recombination of carriers in the depletion region. Wolf *et al.* [98] first reported that the current-voltage characteristics of Si pn diode could be more accurately represented by a double exponential relationship of the form

$$J_{total} = J_{0,diff}\left[\exp\left(\frac{qV_D}{n_1 kT}\right)-1\right] + J_{0,rec}\left[\exp\left(\frac{qV_D}{n_2 kT}\right)-1\right], \quad (5.3)$$

where J_{total} is the total current density, $J_{0,diff}$ is the saturation current density for diffusion, $J_{0,rec}$ is the saturation current density for recombination in the depletion region, n_1 and n_2 are the ideality factors. $n_1 = 1$ for the case of ideal diffusion current. The value of n_2 depends on the location of the recombination centers within the bandgap. Typically, the expected n_2 is close to 2.

Despite of the generation and recombination current in the depletion region, there are other non-ideal effects: (1) the surface effect; (2) the tunneling current via multiple defect sites; (3) the high-level injection effect (the injected minority carrier density is comparable to the majority carrier concentration); (4) the series resistance. The relative strength of the different current mechanisms depends on the properties of semiconductor materials, dopants, and the defects.

5.2 Temperature Sensing Mechanism

The diffusion current and the recombination current are the most important two current mechanisms in the temperature sensor based on 4H-SiC pn diode. At forward bias ($qV_F >> kT$), a general form of the current density J_F of the pn diode at a given applied bias-voltage V_F can be then expressed using the following equation [94]-[96]:

$$J_F = J_0 e^{\frac{qV_F}{nkT}}, \quad (5.4)$$

where q is the electric charge, k is Boltzmann constant, n is the ideality factor and has a value between 1 and 2.

When the diffusion current dominates, $n = 1$ and

$$J_0 = qN_C N_V\left(\frac{D_N}{L_N N_A} + \frac{D_P}{L_P N_D}\right)e^{-\frac{E_g}{kT}}, \quad (5.5)$$

where N_C and N_V are the effective density of conduction and valence band states, D_N and D_P are the diffusion coefficients of electrons and holes, L_N and L_P are the diffusion lengths of electrons and holes, N_D and N_A are the doping concentration in N-SiC and P-SiC, E_g is the bandgap energy.

When the recombination current dominates, $n = 2$ and

$$J_0 = \frac{qn_i W_{dep}}{2\tau_e}, \quad (5.6)$$

where n_i is the intrinsic carrier concentration, W_{dep} is the depletion width, and τ_e is the effective carrier lifetime.

Typically, recombination current dominates at low current levels in 4H-SiC pn diode, showing $n = 2$ [94], [95]. At forward bias ($qV_F >> kT$), the forward voltage of the pn diode can be calculated by

$$V_F = \frac{2kT}{q}\ln\left(\frac{J}{J_0}\right) = \frac{2kT}{q}\ln\left(\frac{2J\tau_e}{qW_{dep}}\right) - \frac{kT}{q}\ln\left(N_C N_V\right) + \frac{E_g}{q}. \tag{5.7}$$

If the temperature dependence of τ_e, W_{dep}, N_C and N_V is negligible, the theoretical sensitivity of the temperature sensor based on 4H-SiC pn diode can be expressed as [94], [95]

$$\frac{dV_F}{dT} \approx \frac{2k}{q}\ln\left(\frac{2J\tau_e}{qW_{dep}}\right) - 7.67mV/K. \tag{5.8}$$

5.3 Sensor Structure

The temperature sensor is based on 4H-SiC pn diode structure. The n-region is formed by a 1-μm-thick N+ 4H-SiC epitaxial layer doped at 10^{19} cm^{-3}, and the p-region is formed by a 0.3-μm-thick P 4H-SiC layer doped at 1.8×10^{18} cm^{-3}. The device is electrically isolated by a lightly doped N- region epitaxially grown on 4H-SiC substrate. It utilizes the same epitaxial layers as the NPN SiC BJTs. Both pn diode terminals are accessible at the top for easy circuit integration. The cross-sectional view of the device is illustrated in Figure 5-2, and Figure 5-3 shows the scanning electron microscopy (SEM) image of the fabricated temperature sensor. The dimension of the metal contact pads is 130 μm × 130 μm, and the dimension of the N+ SiC mesa is 150 μm × 150 μm. The active area of the device is 2.25×10^{-4} cm^2.

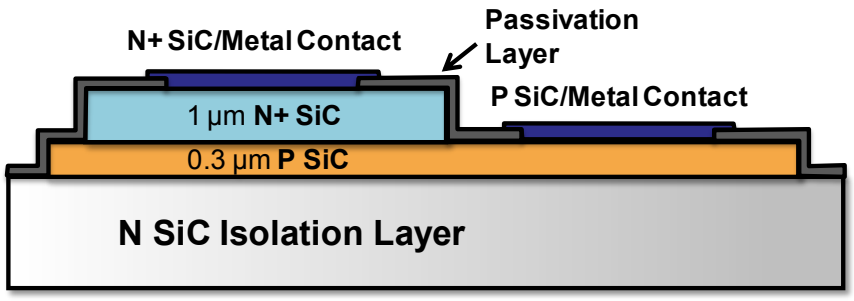

Figure 5-2. Cross-sectional schematic of the temperature sensor based on 4H-SiC pn diode.

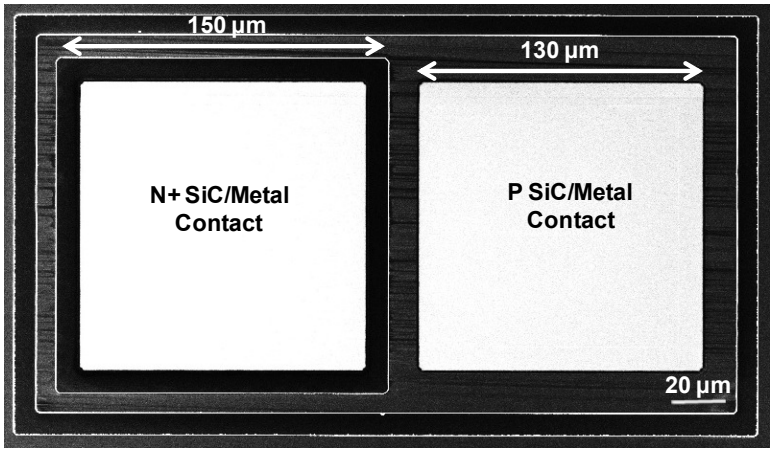

Figure 5-3. SEM image of the fabricated temperature sensor based on 4H-SiC pn diode.

5.3 Fabrication Process Flow of the Temperature Sensor

The process flow of the temperature sensor based on 4H-SiC pn diode is similar to that of 4H-SiC BJTs, and it is shown in Figure 5-3. Therefore, we only briefly describe the fabrication process herein. The devices were fabricated on 4° off-axis Si-face n-type 4H-SiC wafer purchased from SiCrystal AG. And the epitaxial layers were grown by Ascatron AB. First, a transformer coupled plasma (TCP) etching of the N+ SiC epitaxial layer was performed using deposited SiO_2 layer as hard mask to define the n-type-mesa. Next, a second TCP etching of the P-type SiC epitaxial layer was used to isolate the device. Then, plasma enhanced chemical vapor deposition (PECVD) of SiO_2 was performed for surface passivation. After that, the passivation oxide was patterned using reactive ion etching (RIE). E-beam evaporation was then used to deposit Ni for n-type SiC contacts, and Ni/Ti/Al metal stack for P-type SiC contacts. After each metal deposition, a lift-off process was used to pattern the contacts, and a rapid thermal annealing (RTA) step at high temperature was performed to obtain low resistive ohmic contacts. The scanning electron microscopy (SEM) image of the fabricated temperature sensor is shown in Figure 5-3.

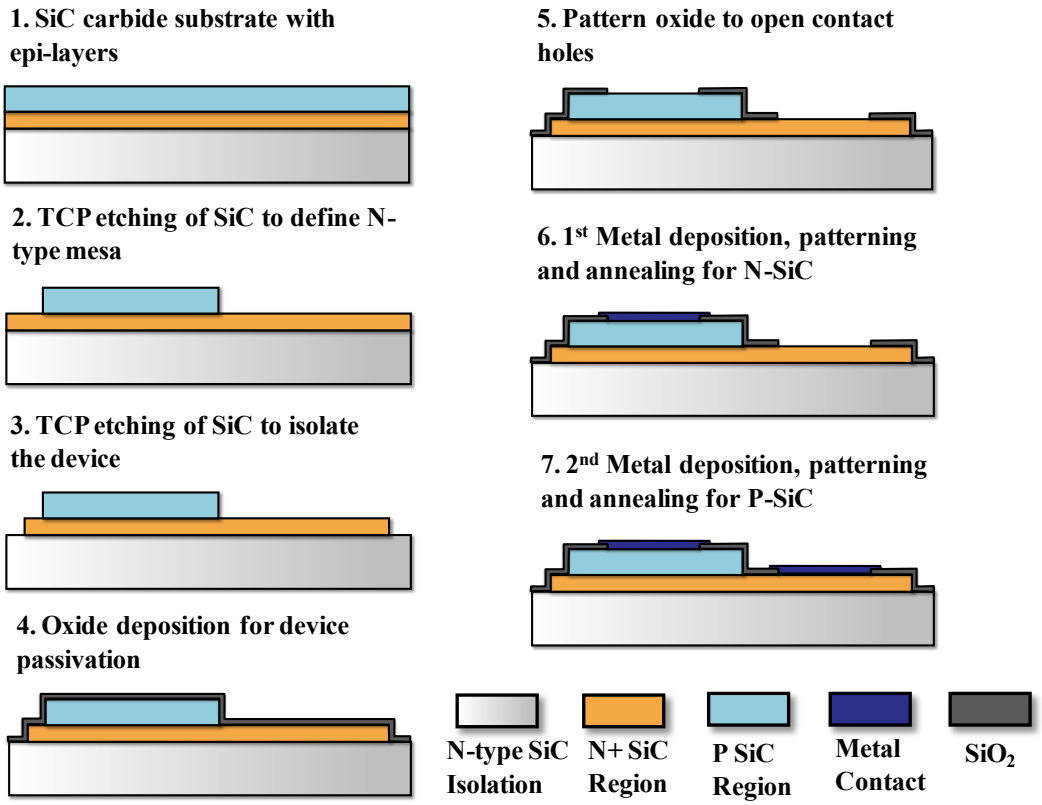

Figure 5-4. Cross-sectional process flow of the temperature sensor.

5.4 Characterization Results

In this section, the characterization results of the fabricated temperature sensor based on 4H-SiC pn diode are going to be discussed. First, the current-voltage (I-V) characteristics at different temperatures are investigated. Then the device performance as a temperature sensor is evaluated.

5.4.1 I-V Measurements at Different Temperatures

The fabricated device was characterized at different temperatures. Figure 5-5 presents the I-V measurement results of the device from room temperature up to 600°C. The peak temperature was not limited by the device, but by the high temperature probe station. The figure shows that, by taking advantages of SiC material properties, stable device performance can be achieved at extremely high temperatures. From Figure 5-5, the ideality factor *n* of the fabricated device at low current levels was extracted to be 2.08 at room temperature and has a small variation of around 15% over the temperature range.

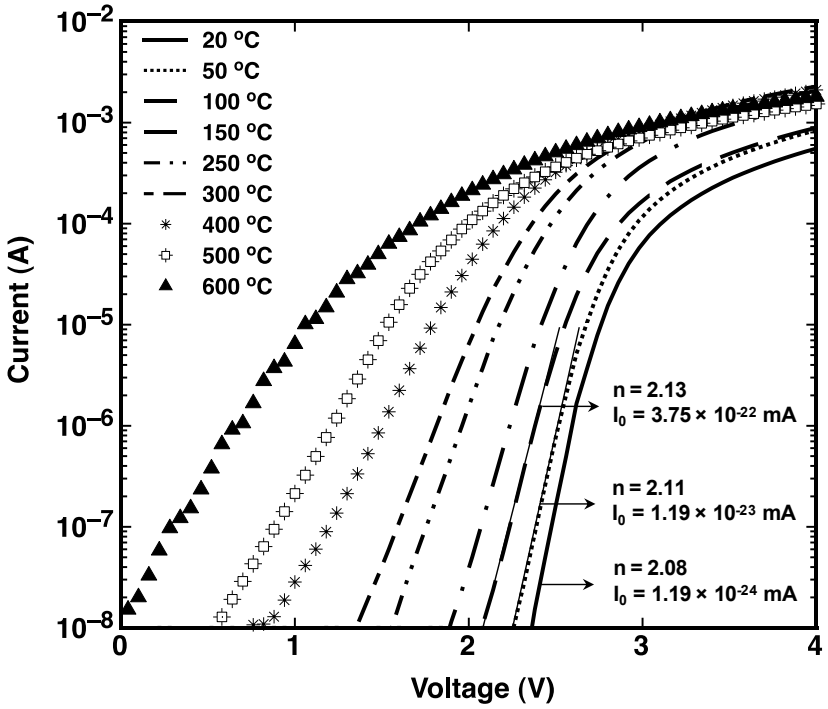

Figure 5-5. I-V measurement of the 4H-SiC pn diode based temperature sensor at different temperatures (20 – 600 °C).

The extracted ideality factors and leakage currents at 20°C, 50°C and 100°C are indicated on the graph. For a given forward current level, the voltage decreases with increasing temperature.

5.4.2 Evaluation of the Temperature Sensor

Figure 5-6 illustrates the forward voltage versus temperature of the fabricated device at different forward current densities, respectively. The graph shows that the forward voltage of the device has a linear temperature dependence at all forward current levels, and it decreases with increasing temperature. By calculating the slopes of these linear relationships, temperature sensitivities can be obtained. At a forward current density of 0.44 A/cm^2, a sensitivity of 2.3 mV/°C is achieved. At a lower current density of 0.44 mA/cm^2, the sensitivity increases to 3.5 mV/°C. From Equation (5.8), it can be observed that the absolute value of dV_F/dT, which is the sensitivity, is higher at lower current level.

Figure 5-7 shows the sensitivity versus forward current density relationship. A linear relationship is observed, and $n = 2.0$ can be extracted from the slope of the fitted curve showing that recombination current dominates the current flowing in the 4H-SiC pn diode in the measured current range. The results show a good agreement with the model described in Equation (5.8). Given the doping concentrations of the N+ and P regions, the corresponding depletion width is 0.047 μm. The carrier lifetime $\tau_e = 0.167$ *ns* can also be

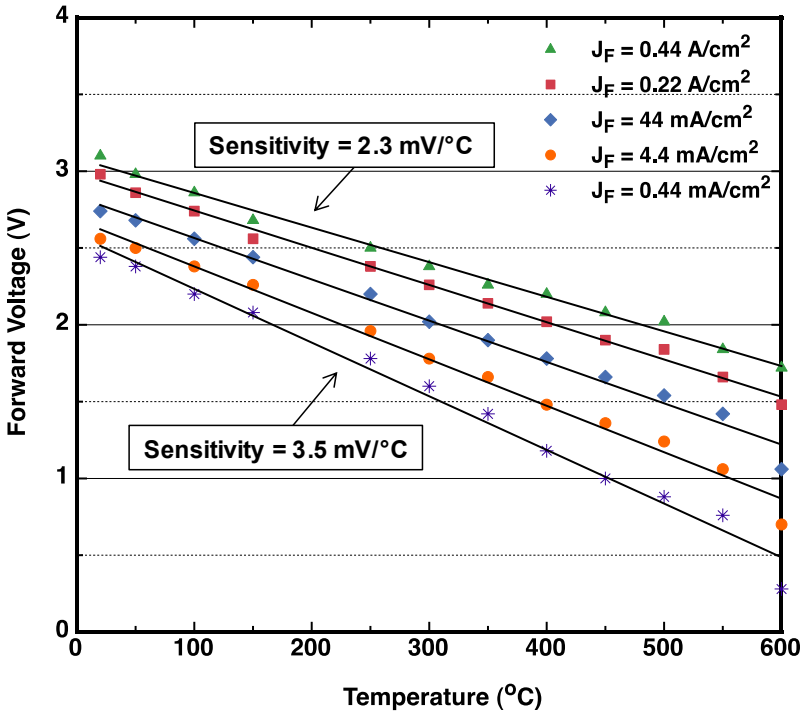

Figure 5-6. Measured forward voltage *vs.* temperature at different forward current densities.

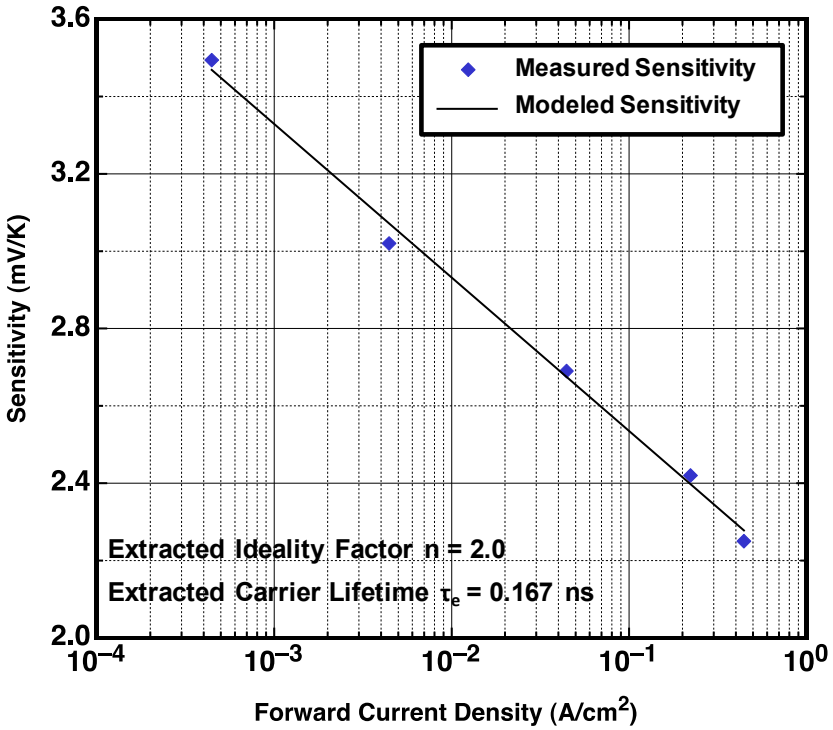

Figure 5-7. Measured and modeled sensitivity *vs.* forward current density of the 4H-SiC pn diode temperature sensor. The extracted ideality factor and carrier lifetime are indicated on the graph.

extracted from the sensitivity versus forward current density relationship. The low carrier lifetime is mainly caused by the high density of interface traps at the SiO_2/SiC interface.

In addition, the experimental results indicate that the proposed 4H-SiC pn diode achieves better sensitivities and higher operation temperatures in comparison with previously reported devices based on SiC Schottky diodes structures [91]-[93]. The sensitivity of the proposed device is also higher than the reported 4H-SiC pn diode betavoltaic cell [95] mainly due to the smaller depletion width and less impact of shunt resistance. The forward bias sensing mode can be used in the entire range from 20°C to 600°C and the forward voltage can be converted into a measurable variable by using a sensing circuit [91].

5.5 Conclusions

In this chapter, theoretical analysis and experimental results for a high-performance temperature sensor based on 4H-SiC pn diode are demonstrated. Thanks to the superior material properties of SiC, the temperature shows stable operation from room temperature up to 600 °C. Under forward bias condition, the temperature sensitivity of the sensor changes from 2.3 mV/°C at a forward current density of 0.44 A/cm^2, to 3.5 mV/°C at a forward current density of 0.44 mA/cm^2. Higher sensitivity can be achieved at a lower forward current level. The experimental results indicate a good agreement with the theoretical analysis. These results show that the device has the potential to be integrated with supporting circuitries to build a sensing module for high temperature applications.

Chapter 6

Conclusions and Future Research Directions

There are increasing interests on developing an integrated sensing module capable of operating at high temperatures. Such systems are beneficial to a number of industrial applications. A high temperature integrated circuit is an important part of such systems, because it can provide power management function for the energy scavenger, build the electrical interface with MEMS-based harsh environment sensors, and amplify the sensing signals. Therefore, it is essential to have transistors, the building blocks of integrated circuits, which can operate at high temperatures. This dissertation presents potential solutions for the above problems. This chapter concludes the research efforts on developing 4H-SiC BJTs, which are capable of operating at extremely high temperatures. A high temperature sensor based on 4H-SiC pn diode is also demonstrated. Finally, suggestions on possible future research directions are made.

6.1 Summary

The main outcomes of this work are 1) the study of physical models for describing the electrical behaviors of SiC devices, 2) the development of fabrication process for SiC based electrical devices, 3) the design and development of 4H-SiC NPN BJTs that are capable of stable operation up to 400 °C, 4) the design and development of temperature sensor based on 4H-SiC pn diode which shows stable operation in a temperature range from 20 °C to 600 °C, 5) the device characterization at room temperature and at elevated temperatures.

Physical models are studied to describe the device behaviors. Especially, the temperature dependences of material electrical properties are essential to understand the device performance at elevated temperatures. Numerical device simulators are used to design the devices and investigate the device behaviors. Appropriate physical models with proper material properties are necessary to obtain accurate simulation results. Physical models of band structure, mobility, incomplete ionization and generation-

recombination are discussed. Special emphasis goes to the temperature dependence of carrier concentration and carrier lifetime. The understanding of the current device will work as guidelines for optimization of the device performance in the future.

Fabrication process for SiC based electrical devices was developed. Though some of the Si processing technologies can be applied to SiC, there are still differences from standard Si process due to the chemical inertness and the thermal stability of SiC. For the etching process, there is no known chemical that can wet etch single crystal SiC at room temperature. TCP/ICP etching is commonly used instead. To avoid the trenching effect, which usually happens during the plasma etching process, HBr and Cl_2 based etching chemistry was studied. Good sidewall profile and high selectivity were obtained by using the optimized recipe. Metallization process is also important for getting good devices. The quality of ohmic contacts could affect the operation and performance of the devices. Different metal layers and metal stacks are tested, with various high temperature annealing conditions. Ni was chosen for n-type SiC contacts, and optimized annealing condition is 2 minutes at 1000 °C. The contact resistance and specific contact resistance are 5.14 Ω and 1.37×10^{-4} Ωcm^2 respectively. For the p-type SiC contacts, Ni/Ti/Al metal stack is utilized. After annealing the contact at 800 °C for 1 minutes, the contact resistance and specific contact resistance are 664 Ω and 2.18×10^{-3} Ωcm^2 respectively. Some issues with the surface passivation method were addressed and discussed. Due to the remaining carbon cluster at the SiO_2/SiC interface during the oxidation process, serious degradation of the dielectric layer quality is observed. Nitridation of the oxide has been shown to be an effective way to improve the quality of the interface. The device performance could be improved if this process can be applied in the future.

4H-SiC NPN BJTs were designed for high temperature sensing applications that usually require low voltage, analog integrated circuits. The thickness and doping concentration of the epitaxial layers were designed to have high current gain β and high output resistance r_o. The proposed device was fabricated and comprehensively characterized at room temperature and at elevated temperatures. The device showed stable operation up to 400 °C. At high temperatures, although the current gain of the device is reduced, the output resistance increases. The intrinsic voltage gain of 5900 is achieved at 400 °C, which is higher than 3300 at room temperature. The results show that 4H-SiC BJT has the potential to be used as a voltage amplifier at extremely high temperatures.

Finally, a high-performance temperature sensor based on 4H-SiC pn diode is demonstrated. The device showed stable operation from room temperature up to 600 °C. The operating mechanism of the temperature sensor was discussed based on pn junction diode physics. In forward biased region, the forward voltage of the 4H-SiC pn diode shows linear dependence on temperature at a constant current. This dependence is utilized to sense temperature variations and the proposed device achieves a high sensitivity of 3.5 mV/°C. This type of temperature sensor has the advantages of high sensitivity and compatibility with integrated circuits. The successful demonstration of the temperature sensor based on 4H-SiC pn diode opens the possibility to the integration with supporting circuitries to build a sensing module that is capable of working at extremely high temperatures.

6.2 Future Research Directions

Future work for this project is needed for the optimization of the device performance, and for the development of complementary circuit elements for high performance ICs that can reliably operate at extremely high temperatures.

- **Improvement of fabrication process**
  The surface passivation process needs to be improved to reduce the interface trap density. The quality of the interface between SiC and the surface passivation layer has a strong effect on the current gain of SiC BJTs. High temperature annealing of thermally grown or deposited SiO_2 in NO or N_2O should be studied. Substituting SiO_2 with other dielectric, such as AlN or aluminum oxide (Al_2O_3), could also be investigated.

  Metallization process also needs further investigation. In this work, Ni is used for N-type SiC contacts and Ni/Ti/Al metal stack is used for P-type SiC contacts. Though both contacts showed stable operation up to 600 °C, long-term stability test should be performed to study the electrical behaviors of the contacts. To further extend the operating temperature of the device, more metals need to be explored, especially for P-type SiC contacts. TiW is a strong candidate since it is very stable at high temperatures and can work for both N-type and P-type SiC.

- **Development of high performance 4H-SiC NPN BJTs**
  A further analysis on the influences of design parameters, such as geometry parameters, doping concentrations and thicknesses of the epitaxial layers, should be developed for achieving better current gain and output resistance. To further increase the current gain, poly-SiC emitter instead of all-crystalline emitter could be used. Poly-emitter structure can improved the emitter injection efficiency, and thus is widely used in Si BJTs to improve the current gain. TCAD simulation results show that a 15% increase of the maximum current gain can be obtained by using a poly-emitter SiC BJT.

- **Development of complementary circuit elements**
  By carefully designing the epitaxial layers, complementary circuit elements, such as PNP BJTs, can be fabricated together with NPN BJTs in the same fabrication run. In addition, other types of transistors can be fabricated as well with minimum additional process steps. JFETs have the advantage of high input impedance, which is a desirable feature for sensing circuitry. However, they are normally-on devices with low transconductance and high forward voltage drop, which make them less appealing. By redesigning the epitaxial layers, it is possible to have JFETs fabricated together with NPN BJTs. The capability of having multiple types of transistors on the same chip gives circuit designers more flexibility.

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