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# Improving Gain and Efficiency of N-polar GaN Deep Recess HEMT for mm-Wave Applications

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

Weiyi Li

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December 2022

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September 2022

Improving Gain and Efficiency of N-polar GaN Deep Recess HEMT for mm-Wave Applications

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by

Weiyi Li

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Liu, W.; Romanczyk, B.; Guidry, M.; Hatui, N.; Wurm, C.; **Li, W.**; Shrestha, P.; Zheng, X.; Keller, S.; Mishra, U.K. "6.25 W/mm and Record 33.8% PAE at 94 GHz from N-polar GaN Deep Recess MIS-HEMTs with ALD Ru Gates", IMS 2021, Atlanta, GA, USA, 2021, oral presentation

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Pasayat, S.S.; Hatui, N.; **Li, W.**; Gupta, C.; DenBaars, S.P.; Nakamura, S.; Keller, S.; Mishra, U.K. "Growth of high quality crack-free partially relaxed thick Al0.24Ga0.76N on porous GaN based GaN pseudo-substrates", 62nd Electronic Material Conference, Columbus, OH, USA, 2020, oral presentation

Zhang, Z.; Qin, S.; Fu, K.; Yu, G.; **Li, W.**; Zhang, X.; Sun, S.; Song, L.; Li, S.; Hao, R.; et al. "Normally-Off AIGaN/GaN MIS-HEMTs by Ionic Liquid Wet Etching & LPCVD-SiN Gate Insulator", International Workshop on Nitride Semiconductors (IWN 2016), Orlando, FL, USA, 2016

Zhang, Z.; **Li, W.**; Fu, K.; Yu, G.; Cai, Y.; Zhang, B. "High performance AlGaN/GaN MIS-HEMTs with In-Situ Pre-Deposition Plasma Nitridation and LPCVD-Si3N4 Gate Insulator", 10th National Annual Conference on Semiconductor Devices, Jilin, China, 2016, oral presentation

## PATENT APPLICATION

**Weiyi Li**, Hui Yang, Yong Cai, Baoshun Zhang, Kevin J. Chen, III-nitride HEMT module and a manufacture method thereof, filed, CHINA, CN201710097227.6

Zhili Zhang, Baoshun Zhang, Yong Cai, **Weiyi Li**, Kai Fu, Guohao Yu, Shichuang Sun, Liang Song, Weak polarization HEMT device through realization of electric charge engineering, filed, CHINA, CN201621264822.1

Liang Song, Kai Fu, Zhili Zhang, Shichuang Sun, **Weiyi Li,** Xiajun Li, Yong Cai, Baoshun Zhang, III-nitride HEMT devices of enhancement mode self-supporting vertical stratification and AlGaN/GaN HEMT device, filed, CHINA, CN201620554498.0

Zhili Zhang, Baoshun Zhang, Yong Cai, Kai Fu, Guohao Yu, Shichuang Sun, Liang Song, **Weiyi Li**, Method and system for fabricating recessed gate enhanced high electron mobility transistor (HEMT) device by in-situ etching monitoring, filed, CHINA, CN201610250596X

Zhili Zhang, Baoshun Zhang, Yong Cai, Kai Fu, Guohao Yu, Shichuang Sun, Liang Song, **Weiyi Li,** Method and system for realizing P-type nitride enhanced HEMT (High Electron Mobility Transistor) through in-situ etching monitoring, filed, CHINA, CN201610250471.7

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# ABSTRACT

Improving Gain and Efficiency of N-polar GaN Deep Recess HEMT for mm-Wave Applications

by

Weiyi Li

GaN-based high electron mobility transistors (HEMTs) have emerged to be a leading technology for RF millimeter-wave application. While GaN technologies utilizing the Ga-polar (0001) orientation have shown good performance in W-band, its performance is saturated due to the DC-RF dispersion and the limit on device gate to channel distance. As an alternative, the N-polar (000-1) GaN deep recess HEMTs can overcome those disadvantages and outperform Ga-polar GaN devices with excellent output power and efficiency at 94 GHz. However, the ability to enhance efficiency of GaN-based RF transistor simultaneously with high output power density is still limited by the gain of the device, making high gain a critical need at W-Band at mm-wave frequencies.

Works in this dissertation focus on improving gain and efficiency of N-polar GaN deep recess HEMTs. A predictive physics-based model on transport has been proposed to inspect the performance N-polar GaN RF transistor and understand electron transport in devices. The modelling results show good agreement with experimental data on device DC transfer characteristics and RF cut-off frequency. After understanding the predictive behaving manner of the devices, effects on fringing capacitance from ex-situ SiN passivation and GaN cap layer have been studied to evaluate electrostatics of N-polar GaN deep recess devices.

With knowledge acquired on transport and device electrostatics, thin GaN cap layer (20 nm) and Atomic Layer Deposition (ALD) Ru gate have been implemented with great commercial N-polar GaN-on-sapphire epi to improve the device gain. The fabricated GaN-on-Sapphire devices demonstrated record 94GHz large signal performance with high linear transducer gain of 9.65 dB, enabling excellent performance at 12 V with record 42% power-added efficiency (PAE) with associated 4.4 W/mm of output power density. Furthermore, at 8 V the device demonstrated even higher PAE of 44% with associated 2.6 W/mm of output power density. After 20 nm PECVD SiN passivation, devices show very high output power density of 5.83 W/mm with a high PAE of 38.5% at 94 GHz. The excellent results demonstrate the great potential of N-polar GaN-on-sapphire technology for mm-wave application with simultaneous high efficiency and power density.

Strain engineering on GaN has also been explored for improving the device gain. Both relaxed InGaN channel and strain GaN channel were proposed for electron velocity enhancement. The GaN/InGaN HEMT with a relaxed InGaN channel has been fabricated utilizing a porous GaN buffer achieved by the selective and controlled electrochemical etch of GaN. The results show ~70% of InGaN relaxation relative to GaN and ~10% 2DEG mobility enhancement with respect to the strained InGaN channel. For strained GaN channel, electron effective mass in GaN under the biaxial tensile strain was calculated using first principal DFT calculation. The effect of biaxial tensile strain on device performance of GaN HEMT are also investigated. The results demonstrated the enhanced electron velocity over 15% with 4% compressive biaxial strain and improvement in both DC and RF performance of the transistor with the improved electron velocity.

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# 1. Introduction

Nowadays, with the rapid development of the wireless communication technology, the 5G wireless network achieved the high data rate up to 20 Gbps. For future hyper-connective 6G wireless network at mm-wave frequency with higher data rate, high frequency RF power amplifier with high power is critical and it requires transistors operating with high power, high efficiency, and linearity for signal amplifier circuit to meet the high-power requirement.

Among all different material systems used in power amplifier, gallium nitride (GaN) has emerged to be a leading material for high frequency RF power amplifier application in mm-wave regime at high device- and chip-level power levels, and GaN technology utilizing N-polar (000-1) orientation has demonstrated excellent performance at W-band with high output power and high efficiency [1-4].

However, the ability to enhance efficiency simultaneously with high output power density is still limited by the gain of the GaN device at mm-wave, making high gain a critical need at mm-wave frequency for GaN technology. Device with high efficiency not only save power consumption but also reduce the heat dissipated and lower size and cost of power amplifiers. This dissertation discusses works on improving gain and efficiency of N-polar GaN HEMT for power amplifier application at mm-wave frequency. This chapter explains motivation on mm-wave transistor, the state-of-art N-polar GaN RF transistor and the challenge for high gain and high efficiency in GaN technology. It concludes with the synopsis of the entire dissertation.

## *1.1. Motivation: mm-wave power amplifier application*

As bandwidth at lower frequency becomes fully allocated (or significantly more expensive), communication and imaging in mm-wave frequency becomes even more

desirable for both commercial and military purpose with its potential for higher data rate. Compared with communication in lower frequency, the mm-wave wireless network uses electromagnetic spectrum from 30 to 300 GHz corresponding to wavelengths of about 1-10 mm in air, the smaller electromagnetic wavelength requires the size shrinking of power cell and the high output power is also critical to reduce the required number of base stations for covering enough area. The need of reducing the number of multiplying stages and thus improves the size, cost and efficiency of the system asks for high frequency RF power amplifier with high output power and it has driven the development in the semiconductor transistor technologies to high power and high efficiency.

### *1.2. Evaluation method and key metrics of RF power transistor*

For a typical monolithic microwave integrated circuit (MMIC) power amplifier, it generally includes matching networks, bias circuit, and several RF transistors with multi-stage combining networks for the increasing the gain and/or output power of the amplifier. This dissertation discusses design, fabrication, and characterization of individual device instead of full power amplifier for the consideration of focus on transistor optimization and university level device research. To evaluate individual transistor for high frequency application, several measurement techniques are used to characterize device with different metrics.

The small signal RF measurements can be applied to evaluate the small signal performance of the RF transistor, which measures the scattering parameters (S-parameters) of the transistor with a swept DC bias at microwave frequencies. From the small-signal measurements, the current-gain cutoff frequency($f_T$) and power-gain cutoff frequency($f_{max}$) can be extracted from measured small signal data. Both $f_T$ and $f_{max}$ are widely used to benchmark the small signal gain of the transistor at microwave frequency. The small signal

equivalent circuit can also be extracted from small signal measurement, which can provide physics insight into device operation and helps device performance projection. The detail of small signal equivalent circuit will be discussed in chapter 3.

With the indication on device gain from small signal measurement, load-pull measurement is generally used to evaluate transistor large signal performance. In load-pull measurement, external impedance tuners are implemented for providing input and output impedance matching at different bias condition so that transistor large signal performance can be characterized. In this dissertation, a W-band passive load-pull system has been used to evaluate power performance of N-polar GaN deep recess HEMT at mm-wave frequency. The detailed description of the W-band load pull system can be found in [5].

From the load pull measurements, four parameters are used as key metrics to evaluate transistor performance, and they are output power ($P_{out}$), gain (G), drain efficiency (DE) and power-added efficiency (PAE). The equations for describing these four metrics and given as below:

$$Gain = \frac{P_{out}}{P_{in}} \tag{1.1}$$

$$DE = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{V_{DC} \times I_{DC}} \tag{1.2}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}\left(1 - \frac{1}{G}\right) = DE\left(1 - \frac{1}{G}\right) \tag{1.3}$$

$$P_{out} = \frac{2(V_{DD} - V_{knee}) \times I_{knee}}{8} \tag{1.4}$$

In equation (1.1) $P_{in}$ is the input RF power density. In equation (1.2), DE means the drain efficiency, defined with $P_{DC}$ being the dissipated DC power density and $V_{DC}$ being the DC voltage, $I_{DC}$ being the DC current density. In equation (1.3) PAE is the power-added efficiency, and G = power gain of the device. Assuming harmonic shorted, the output power can be

calculated using method introduced in [57] with equation (1.4), in which the $V_{DD}$ is quiescent source-drain voltage, the $V_{knee}$ is knee voltage of the transistor's I-V curve, and $I_{knee}$ is transistor current at the knee voltage. As shown in the equations, device gain plays a critical role in transistor large signal performance. At same input power and DC bias condition, device with higher gain will have higher output power and higher PAE simultaneously.

### *1.3. GaN for mm-wave RF power amplifier*

Currently, CMOS, SiGe, InP and GaAs based technologies are used for high frequency applications, however their output power densities are limited by their narrow bandgaps, which necessitates larger arrays with chips leading to increased size and cost.

Gallium nitride (GaN) has emerged to be a promising technology for high frequency power transistor and has been employed in nowadays 5G wireless communication network. As a wide bandgap material with strong polarization field, GaN has several properties that makes it an ideal candidate for RF power amplification. The wide bandgap of GaN ($E_G$ = 3.4 eV) and large critical electric field (3.3 MV/cm) allows higher voltage operation compared with other material technology. With the strong built-in polarization field, a very high density ($n_s > 10^{13}$ $cm^{-2}$) two-dimensional electron gas (2DEG) can be formed using the AlGaN/GaN heterojunction, and this 2DEG can obtain high mobility (~2000 $cm^2/(V\cdot s)$) since no doping is needed [6]. High charge density combined with high mobility offer great conductivity to GaN HEMT. With these advantages, GaN technology can enables high current and high-voltage simultaneously, improving the output power of the transistor. Figure 1.1 shows the reported output power of power amplifier using different material technologies at different frequency. GaN HEMT-based amplifiers has demonstrated to provide highest output power among all

different material technologies at frequency up to 110 GHz, showing the advantages of GaN in mm-wave power amplifier application.

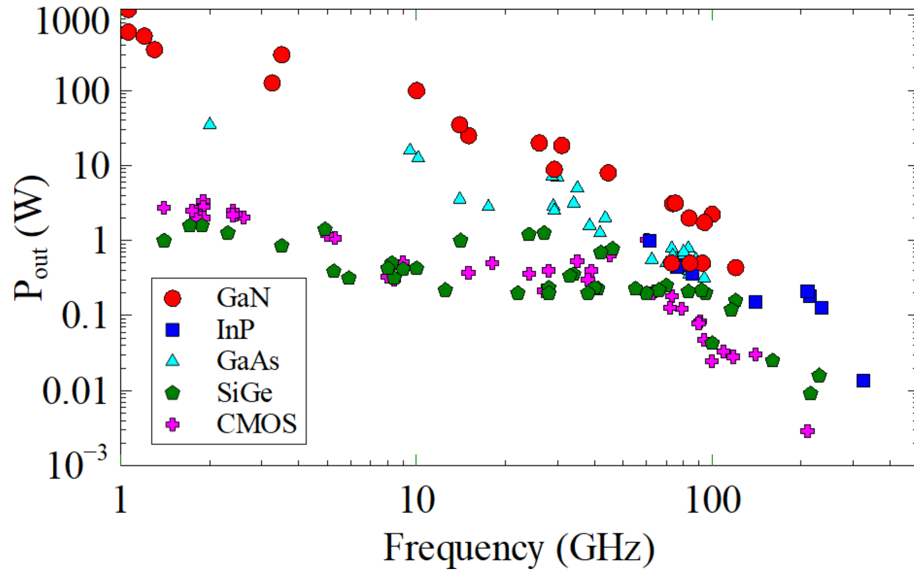



**Figure 1.1. Output power of reported literature and commercially available power amplifier using different material system versus frequency. As of 2021.**

### *1.3.1. Ga-polar GaN*

Because of strong polarization effect in GaN, different crystal orientation of GaN changes polarization field in the semiconductor and cause difference in corresponding device technology. The most basic structure of Ga-polar GaN HEMT consist of an AlGaN barrier layer grown on top of a GaN buffer layer as shown in Figure 1.2. a polarization charge discontinuity exists at the AlGaN/GaN interface and forms a 2DEG adjacent to the interface in the GaN buffer. Several structure modifications have been proposed to improve the Ga-polar GaN HEMT performance: i. a AlN interlayers for reduction of alloy scattering [7], ii. back barrier to offer the 2DEG confinement at the back [8], and iii. ternary and quaternary

(Al,In,Ga)N barrier layers for higher charge density in the 2DEG [9-10], iv. thin GaN cap layer for low surface states [11].

Solid performance has been demonstrated in mm-wave from Ga-polar GaN HEMT [12-19]. However, Ga-polar GaN technology suffers from i. DC-RF dispersion due to the lack of good surface passivation and the trapping effect and ii. the required AlGaN barrier limiting device gate to channel distance for achieving higher gain, causing the transistor performance to become saturated and hard to improve at W-band.

### *1.3.2. N-polar GaN*

As an alternative, the N-polar (000-1) GaN technology has its own uniqueness of reversed polarization field. Therefore, the basic structure of N-polar GaN HEMT become GaN channel layer grown on top of AlGaN layer with a 2DEG formed in the GaN channel right above the GaN/AlGaN interface. Compared with traditional Ga-polar GaN HEMT structure, this inverted polarization field and heterojunction give a variety of epi design advantages, including the natural back barrier, AlGaN cap layer and unintentionally doped (UID) GaN cap layer. The detailed discussion of N-polar GaN HEMT structure will be presented in next section.

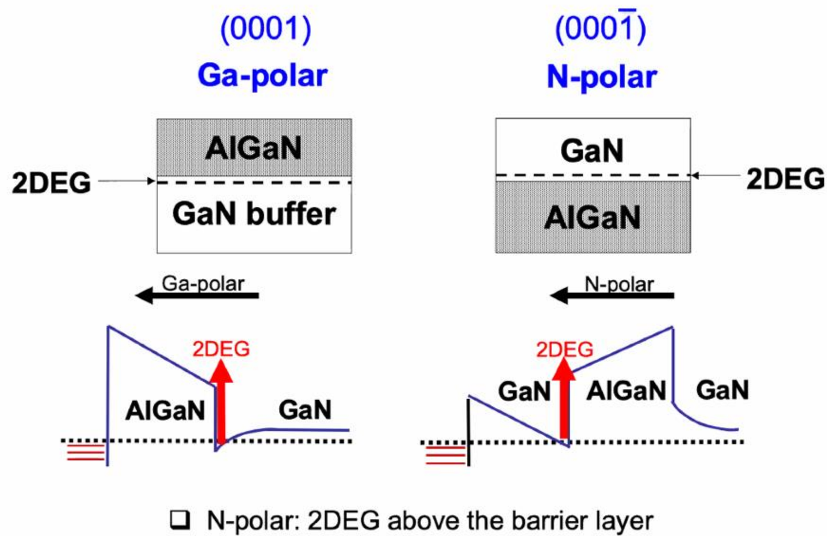



**Figure 1.2. Epi structure and band diagram of (a) basic Ga-polar GaN HEMT, (b) basic N-polar GaN HEMT**

### *1.4. N-polar GaN deep recess HEMT*

To exploiting unique advantages from the reversed polarization field and device development, the state-of-art N-polar GaN device use deep recess structure, as what is presented in Figure. 1.3. At W-band, the N-polar GaN deep recess HEMTs has outperformed Ga-polar devices and have set the record of output power and efficiency at 94 GHz with demonstration of record power density of 8.85 W/mm with associated PAE of 27% [1] and high PAE of 33.8% with associated 6.2 W/mm power density [2] at 94 GHz.

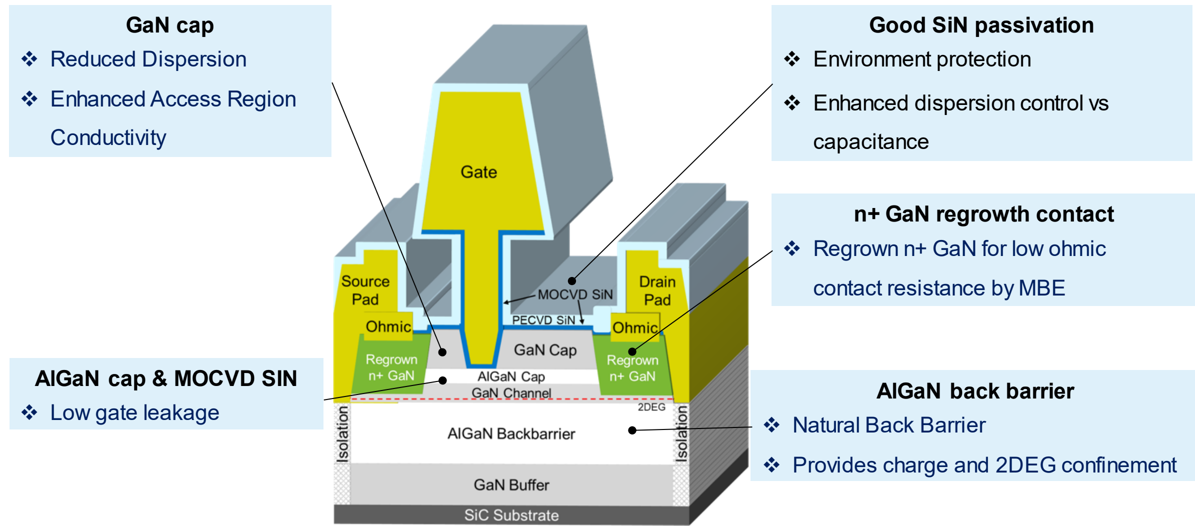



**Figure. 1.3. Device schematic of the N-polar GaN Deep Recess HEMT. Key properties of the device structure are highlighted.**

As shown in Figure.1.3, the N-polar GaN deep recess HEMT contains following advantage

i. Natural back barrier: With charge-inducing barrier below the GaN channel, N-polar GaN HEMT gets a built-in back barrier. This natural back barrier can provide 2DEG confinement from the back and maintains charge density independent of gate-to-channel distance, which is beneficial for achieving low contact resistance and helps N-polar GaN HEMT vertical scaling.

ii. Unintentionally doped (UID) GaN cap layer: the N-polar polarization field direction enables the GaN cap layer to enhance the conductivity of the access regions while simultaneously mitigating DC-RF dispersion. As shown in Figure.1.4, the introduction of GaN cap not only relax the electric field in the GaN channel, but also pulling the conduction band downwards, causing the 2DEG charge density increase and the

centroid of 2DEG moving further away from the back barrier. The 2DEG mobility got improved as the effect from back barrier alloy scattering is reduced. Combined with enhanced charge density, the implement of GaN cap layer really boost the conductivity in the channel. Besides, the introduction of GaN cap layer on the top also replace the ex-situ passivation/AlGaN cap interface with an epitaxially-defined GaN cap/AlGaN cap interface, this effect helps pushing the electrical surface away from the channel with GaN cap acting as an in-situ passivation layer. The DC-RF dispersion control of N-polar GaN deep recess HEMT got greatly improved because of the GaN cap layer.

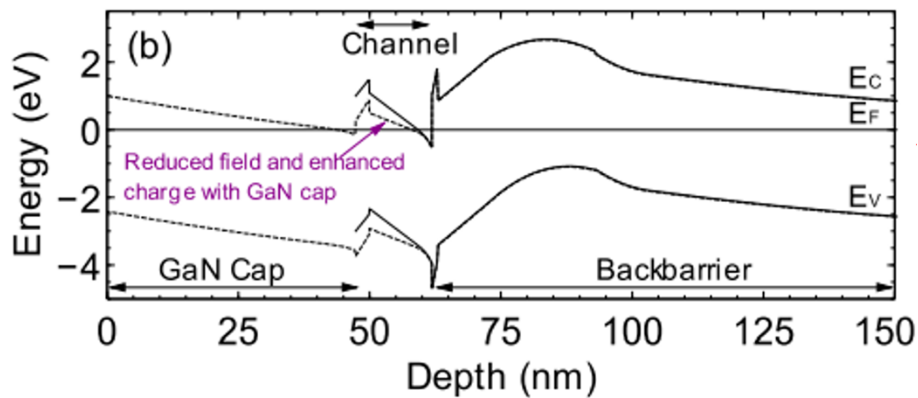



**Figure. 1.4 Band diagram comparing N-polar GaN HEMT with and without an GaN cap. With the addition of a GaN cap the vertical electric field is greatly reduced in the GaN channel and lower the conduction band relatively to the fermi level in the channel.**

### *1.5. Literature study on mm-wave RF GaN*

The application of ex-situ passivation and field plating can effectively control the DC-RF dispersion of Ga-polar AlGaN/GaN HEMT and enable high performance at lower frequency [20-22]. However, getting high gain, high efficiency with high power at mm-wave frequency is hard for GaN HEMT. As shown in the summary of the GaN RF HEMT performance at mm-wave

frequency presented (Figure. 1.5), Ga-polar device have demonstrated good performance at Ka-band with high output power density (Po) of 9.7 and 10.5 W/mm and associated PAE of 43% and 33% at 30 GHz and 40 GHz, respectively [12, 13]. Using high drain bias and optimized field plate design, the Ga-polar GaN HEMT can even achieved power density of 13.7 W/mm with 40% PAE at 30 GHz [14]. However, for device operation at higher frequency, the thick passivation and field plating become restricted because of the parasitic capacitance they introduce. As shown in Figure 1.5, the output power and PAE of Ga-polar device degrade with increasing frequency, which is mostly attributed to the DC-RF dispersion caused by the trapping effect.

At W-band, Ga-polar GaN device have been struggled to achieve high power and high efficiency, and the reported power density is generally around 1-3 W/mm [16-18]. A pre-matched device with 24.2% PAE and 1.5 W/mm was reported by Brown [18] and an output power density of 4 W/mm with 14.3% PAE was reported by Harrouche [19], both at 94 GHz. Severely affected by the DC-RF dispersion, except for device reported by Schwantuschke [17], which obtains a 8.6 dB linear gain but only 1.9 W/mm with 20% associated PAE, Ga-polar GaN device gain at W-band is also low and the linear gain of it is generally around 5 dB, limiting the power and efficiency.

The N-polar GaN device, as what have been discussed in previous section, have overperform the Ga-polar GaN device with excellent output power and efficiency at mm-wave [1-4]. The good DC-RF dispersion control in N-polar GaN enable large RF current swing with high voltage bias. Further, the advantages in device design also helps N-polar GaN achieving high gain at mm-wave. At 94 GHz, the N-polar GaN device linear gain is around 6-8 dB, benefitting output power and PAE simultaneously. As shown in Figure 1.5, N-polar GaN HEMT can provide more than 2x higher power density of Ga-polar GaN with over 27% PAE.

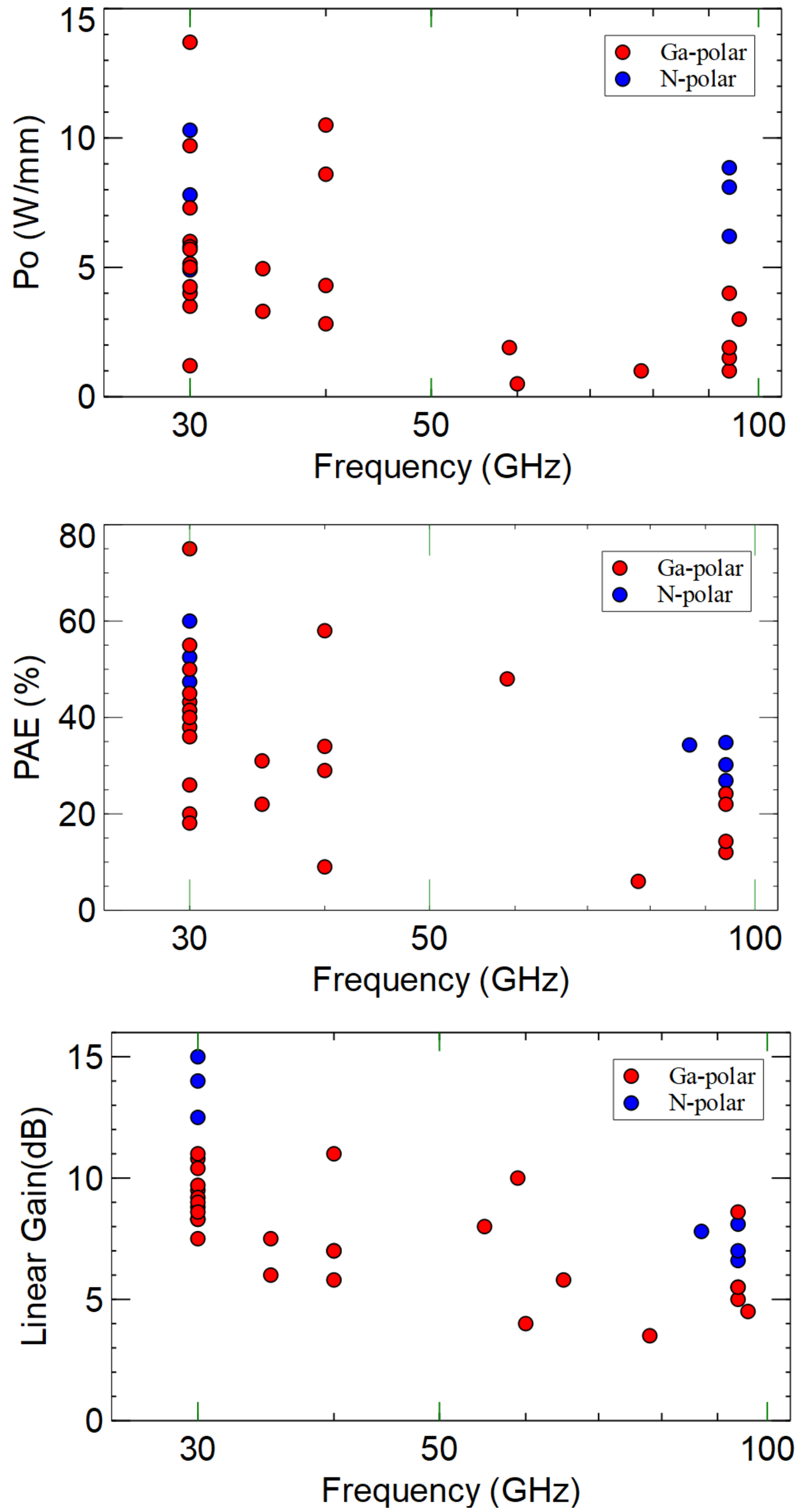



**Figure. 1.5 (a) Output power density, (b) PAE, and (c) linear gain of mm-wave GaN HEMTs as a function of frequency.**

Taking a closer look at the power performance of GaN at W-band, the associated gain in the peak PAE or peak $P_o$ condition are around 2-3 dB and 4-5 dB for Ga-polar GaN devices and N-polar GaN devices respectively. Compared with performance at lower frequency, the lower gain of GaN device at W-band is a major factor limiting the performance of the device. GaN-based RF transistor need higher gain to further improve the device performance at mm-wave frequencies.

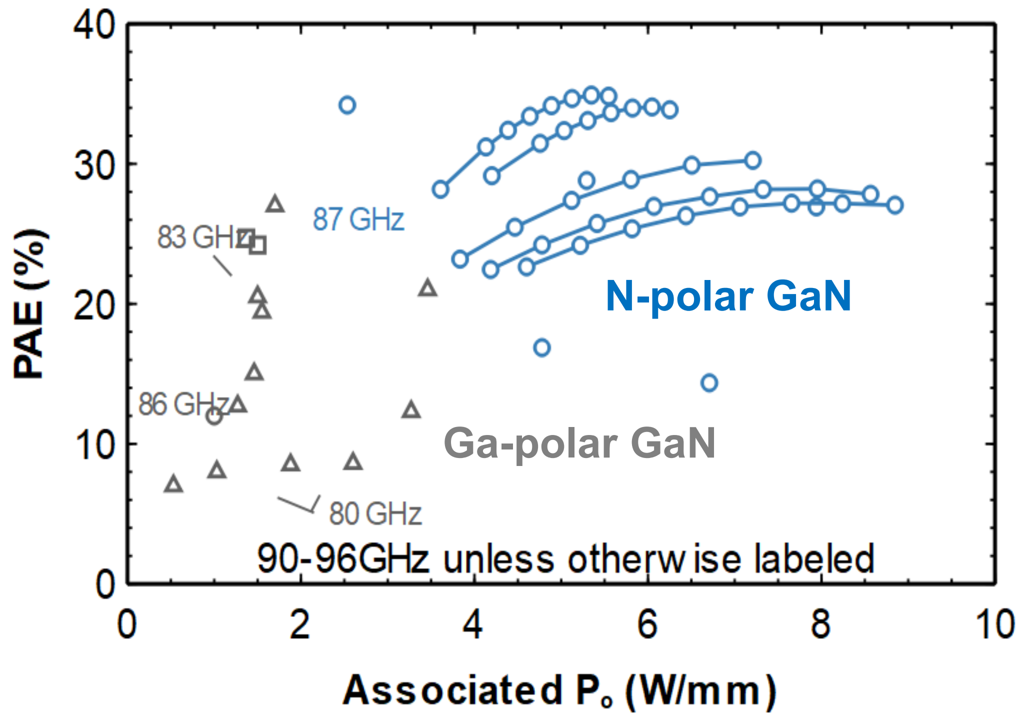



**Figure. 1.6 Benchmarking PAE-$P_o$ from prior N-polar GaN devices and Ga-polar device and circuit from literature**

### *1.6. Synopsis of the dissertation*

This dissertation investigates on improving gain and efficiency of N-polar GaN deep recess HEMTs for achieving high power and high efficiency simultaneously. Start with inspection and understanding of previous state-of-art device, a predictive physics-based model on transport of N-polar GaN deep recess HEMT is presented in Chapter 2. After understanding the predictive manner of the device's behavior with modelling, Chapter 3 discuss about electrostatics study on fringing capacitance from ex-situ SiN passivation and GaN cap layer. The optimized device design and fabrication are presented in Chapter 4 along with the W-band large signal performance results showing record gain and efficiency with high output power. In Chapter 5, strain engineering in GaN is discussed and both relaxed InGaN channel and strained GaN channel are investigated for electron velocity enhancement. Chapter 6 summarize the works in this dissertation and presents guidance for future work of N-polar GaN RF power transistor.

## II. Modelling N-polar GaN HEMT for guiding device design

As discussed in later chapter, N-polar GaN deep recess HEMT have demonstrated great large signal performance at 94 GHz [1-3]. To get guidance for device design achieving higher gain and efficiency, inspection and modelling the previous state-of-art device, especially the electron transport modelling, become a great starting point, because it not only offers deep understanding of the device operation for device design but also evaluate the behavior of the device by comparing the device performance from modelling and experiments.

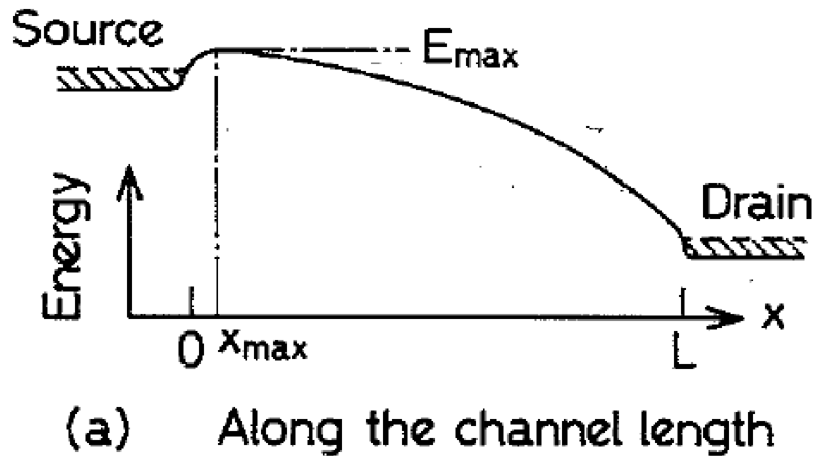



**Figure. 2.1 Schematic distribution of electronic potential energy in a scaled FET along the channel length in [23]**

For highly-scaled transistor like N-polar GaN deep recess HEMT, the physical picture used to describe short channel transistor transport is discussed in [23-24] and shown in Figure.2.1, The conduction band energy of the electron has a barrier near source (controlled by the gate voltage) and drops slowly from source potential to drain potential generally with a steeper slope near the drain edge. The point near source with highest potential energy is generally referred as top of the barrier [24-25] or virtual source point in MIT Virtual Source

(MVS) model [26-27], and it will be referred as virtual source point in this chapter. Discussion about electron transport in the channel usually focus on the virtual source point because it is considered to be in thermal equilibrium [28]. The electrons are injected into the channel from the source and across the barrier at the virtual source point. Assuming current continuity, the drain current ($I_D$) evaluated at the virtual source point can be applied to any point in the channel and it is written as:

$$\frac{I_D}{W} = Q_{ixmax} \times v_{xmax}$$

in which the W is the gate width of the transistor, the $Q_{ixmax}$ and the $v_{xmax}$ is the charge in the channel and electron velocity at the source injection point respectively.

To get physics-based model of N-polar GaN deep recess HEMT, the charge and velocity at virtual source point are two critical properties of the transistor. In this chapter, a physics-based current-voltage model has been proposed to describe the electron transport as well as the transfer characteristics in short-gate-length N-polar GaN transistor. The electron velocity in N-polar GaN deep recess HEMT were examined and compared with a theoretical model based optical phonon scattering in the Section 2.2. Then Section 2.2 discuss using the MIT virtual source model as a fitting function to provided charge model in N-polar GaN deep recess HEMT. The modelling results and discussion of device DC and RF performance is given at the last section.

### *2.1. Electron transport in N-polar deep recess HEMT*

Because of the rapid development of GaN technology, several compact device models have been proposed to develop insight into the device physics and help circuit design [29-32] for Ga-polar GaN. For N-polar GaN, compact modelling use MIT Virtual Source GaN-HEMT (MVSG) has been explored in [33]. However, many of these compact models are empirical

and employ fitting parameters for electron transport, which provide limited information about actual device physics. It is also hard to check predictive manner of transistor behavior and evaluate device performance with empirical model.

To get a more physics-based modelling on N-polar GaN RF HEMT, a purely physics-based description on electron velocity is needed and verified with experimental results. Because of the strong optical phonon scattering, GaN has a short electron mean free path (~3.5nm) and the electron transport is not ballistic even in highly scaled transistor. A model based on optical phonon scattering has been proposed and used to explain the transconductance behavior of scaled GaN transistor [82]. This transport model also inspects the electron properties at the virtual source point. Based on ballistic transportation model [23], the carrier distribution in k-space is calculated with the injected and back-scattered carrier and the difference of the quasi-Fermi level is determined by the optical phonon scattering energy of GaN, 92 meV. Using the Fermi-Dirac integral, the current flowing in the GaN transistor is calculated as:

$$J = \frac{J_{th}}{2\sqrt{\pi}}\left[\mathcal{F}_{1/2}(\eta) - \mathcal{F}_{1/2}\left(\eta - \frac{\hbar\omega_{op}}{k_B T}\right)\right] \tag{2.1}$$

Where the where $J_{th} = qv_{th}k_BTm^*/\pi\hbar^2$ is an effective thermal current, with $v_{th} = 2k_BT/m^*$ being the thermal velocity and $m^*$ being the effective mass. $\mathcal{F}_{1/2}(\eta) = (2/\sqrt{\pi})\int_0^\infty \sqrt{\mu}(1 + e^{\mu-\eta})^{-1}\, d\mu$ is the Fermi–Dirac integral. The parameter η is $\eta = E_{in}/k_BT$, where $E_{in}$ is the injection electron quasi-Fermi level. The two Fermi–Dirac integrals are for the right- and left-going carriers, respectively.

The electron density at the virtual source point can also be calculated by summing the electrons that are injected and back-scattered, given by:

$$n_{in} = \frac{m_e k_B T}{2\pi\hbar^2}\left[log(1 + e^{\eta}) + log\left(1 + e^{\eta - \frac{\hbar\omega_{op}}{k_B T}}\right)\right] \tag{2.2}$$

Using this the optical phonon scattering based model, the dependence of electron velocity on 2DEG density at the virtual source injection point can be calculated and presented in Figure 2.3. The results shows that the velocity peaks around 3e13 cm-2 with a value of 1.4e7 cm/s, and then decrease as carrier density increase. The peak velocity is lower than the drift velocity predicted using Monte Carlo simulation [34] and follows what has been observed in experiments [35-36]. To compare the velocity from the model and experimental results, velocity extraction on fabricated N-polar GaN deep recess HEMT are conducted using method described in [37]. Based on the delay analysis for a scaled FET, the $f_T$ of the devices is written as following formula with different delay term.

$$\tau_{total} = \frac{1}{2\pi f_T} = \frac{C_{gs} + C_{gd}}{g_m} + \frac{C_{gs} + C_{gd}}{g_m}\frac{R_S + R_D}{R_{DS}} + C_{gs}(R_S + R_D) \quad (2.3)$$

$$= \tau_{transit} + \tau_R + \tau_{miller} \quad (2.4)$$

As the delay term of resistor divider and Miller effect come from parasitics effects and do not contribute to the intrinsic transistor transport. After extraction of fringe capacitance, which will be discussed in detail in chapter 3, the velocity is extracted as following and plotted in Figure 2.3:

$$\tau_{transit} = \tau_{intrinsic} + \tau_{fringe} = \frac{C_{gs,intrisic} + C_{gd,intrinsic}}{g_m} + \frac{C_{gs,fringe} + C_{gd,fringe}}{g_m} \quad (2.5)$$

$$v_e = \frac{L_G}{\tau_{intrinsic}} \quad (2.6)$$

The N-polar GaN HEMT epi structure and device structure are presented in Figure 2.2. The device used for velocity extraction features conventional 48 nm GaN cap, $L_G$ of 58 nm.

As shown in Figure 2.3, the good matching result between model and experimental data demonstrates the effectiveness of the velocity model. The optical phonon scattering based

velocity model provides a physical model on electron velocity and is used in later section for modelling the N-polar GaN deep recess HEMT.

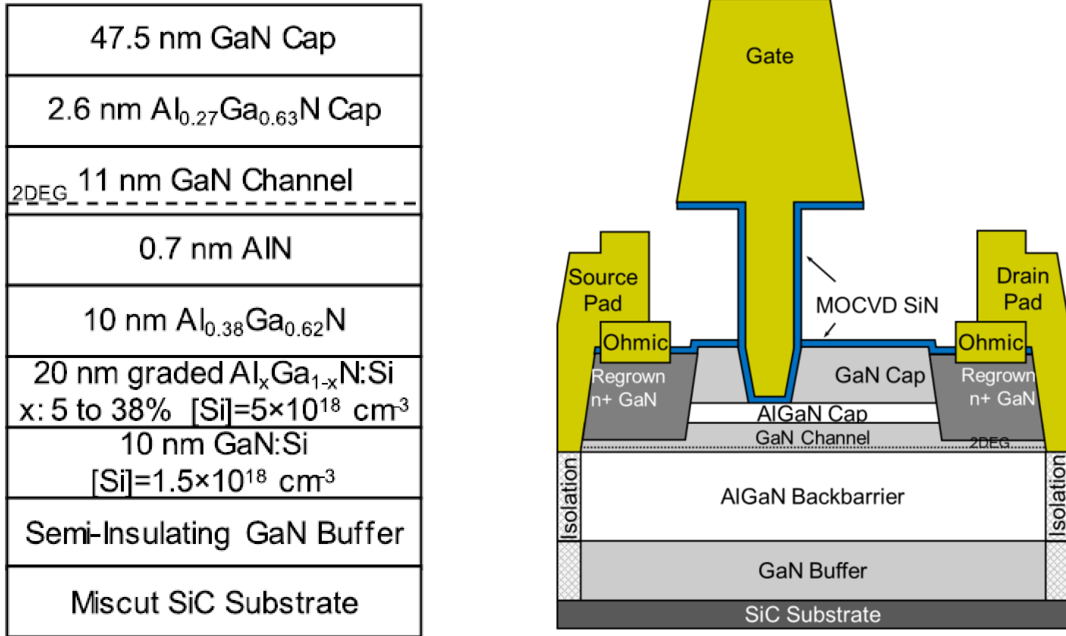



**Figure. 2.2 (a) Epitaxy structure and (b) cross-sectional device structure used for velocity extraction.**

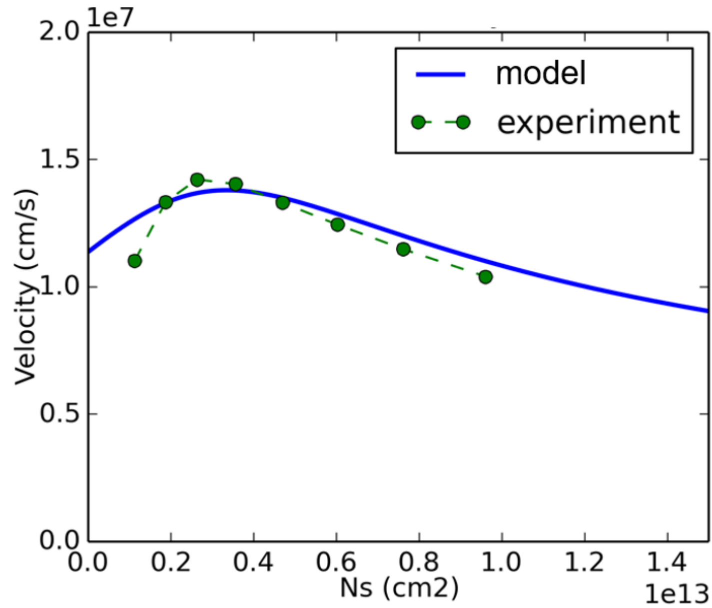



**Figure. 2.3 Velocity plotted as a function 2DEG charge density from experimental extraction and velocity model.**

### *2.2. Charge model used for N-polar GaN deep recess HEMT*

While the velocity model has been proposed based on optical phonon scattering in GaN and good agreement has been obtained with experimental results, the charge model of the device at virtual source point becomes the puzzle piece missing for modelling the N-polar GaN deep recess HEMT.

In the meantime, the MIT virtual source model has been previously implemented in N-polar GaN device modelling with a purely empirical velocity model as following [33]:

$$v_e = \frac{v_{inj}}{1 + \frac{\theta_v n_{ixo}}{C_g}} \tag{2.7}$$

And the $v_{inj}$ is the bias independent injection velocity at low 2DEG density and the $n_{ixo}$ is the charge density at virtual source point. $\theta_v$ is the fitting parameters and the $Cg$ is the gate capacitance in strong inversion. The term in the denominator accounts for carrier scattering. In this chapter we replace the empirical velocity model in MIT virtual source model with the physical model based on optical phonon scattering, offering more physics insight for device operation.

In MVS, the semi-empirical charge versus gate voltage characteristics, with the charge at the source injection point described as [33]

$$n_{ixo} = C_g n\phi_t ln\left(1 + exp\left(\frac{V_{gsi} - (V_{th} - \alpha\phi_t F_f)}{n\phi_t}\right)\right) \tag{2.8}$$

where the physical meaning of each parameter listed in Table 2.1 and the value of parameters are selected according to the extracted value from device DC performance.

| Parameters | Meaning |
| --- | --- |
| $C_g$ | Effective gate-to-channel capacitance |
| $n$ | Subthreshold coefficient |
| $\phi_t$ | Thermal voltage $K_BT/q$ |
| $V_{gsi}$ | Internal gate-source voltage |
| $V_{th}$ | Threshold voltage w/ DIBL |
| $\alpha$ | Fitting parameters |
| $F_f$ | Fermi function for $V_{th}$ transition considering inversion |

**Table 2.1 Parameters used in MVS charge function and definitions**

After deciding each parameter in equation with it physics meaning and corresponding value extracted from device performance, the charge vs gate voltage characteristics has been calculated and plotted in Figure 2.4, showing 1.09e13 $cm^{-2}$ 2DEG density at $V_G = 0$ V.

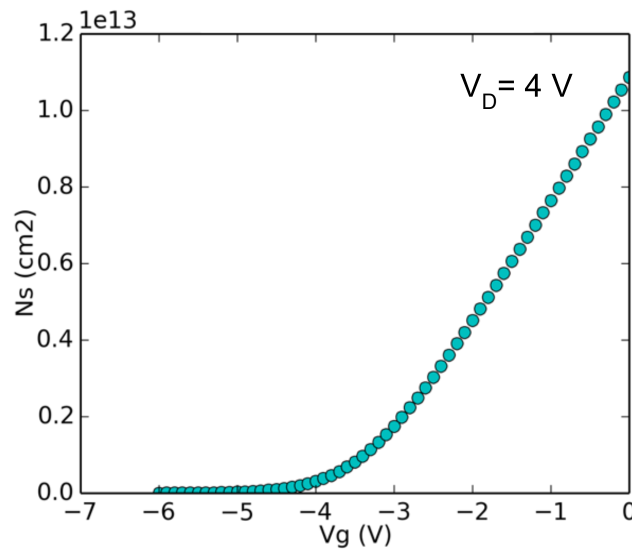



**Figure. 2.4 Calculated 2DEG vs gate voltage characteristics using MVS charge model**

With the methodology discussed with equation (2.8), the charge model in MVS has been implemented with each parameter reflects its own physics definition. With the incorporation of optical phonon scattering based velocity model, a physics-based $I_{DS}$ ($V_{GS}$) model is obtained, and the device DC transfer characteristics has been calculated and compared with experiments data.

### *2.3. N-polar GaN deep recess HEMT Modelling results*

Using the device discussed in Section 2.1 for velocity extraction, the calculated results using this model are compared with experimental results. The series resistance ($R_S$) is set to be 0.12 ohm.mm based on the extraction of experimental data and the calculated current transconductance are plotted in Figure.2.5 and Figure 2.6 respectively. Measured pulsed I-V at $V_D$ of 4 V is used to compare with model. The results show excellent agreement on the transfer characteristics with small difference for $V_G$ after -2 V, which can be attributed to other scattering mechanism at high 2DEG charge density and needs further investigation.

The transistor's cut-off frequency is also calculated using the method described in [38] with no $R_{DS}$ effect included, the equation used is as below:

$$2\pi f_T = \frac{1}{\frac{C_{gs}+C_{gd}}{g_m} + C_{gd}(R_s + R_d)} \tag{2.9}$$

The small signal equivalent circuit parameters used is shown in the inset in Figure. 2.7 with calculated cut-off frequencies shown in Figure.2.7. Without considering the nonlinear resistance in the access region and bias-dependent fringe capacitance, the model still obtains a good agreement with measured results, showing good potential of predicting device RF

performance and calculated S-parameters and large -signal performance with such a physics-based model.

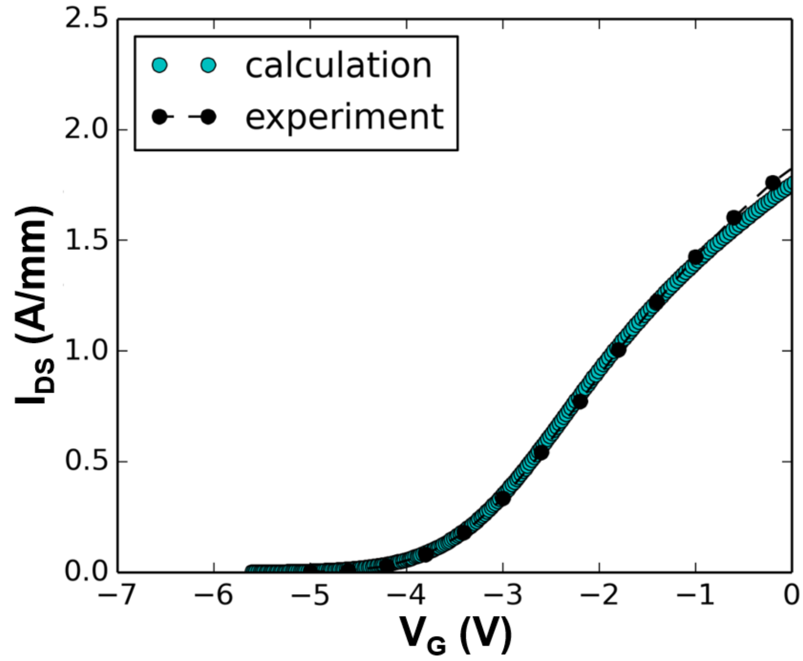



**Figure. 2.5 Device transfer characteristic with Lg=58nm from model calculation and experimental results**

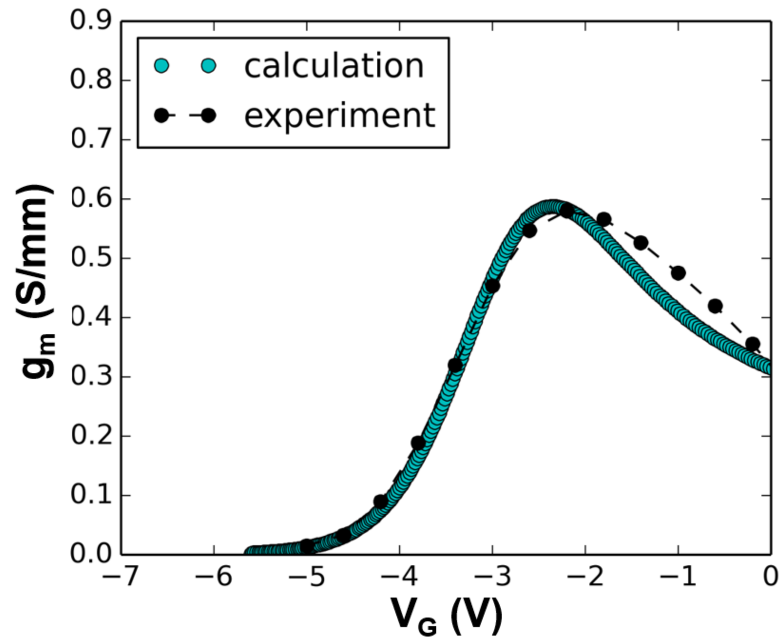



**Figure. 2.6 Device transconductance characteristic with Lg=58nm from model calculation and experimental results**

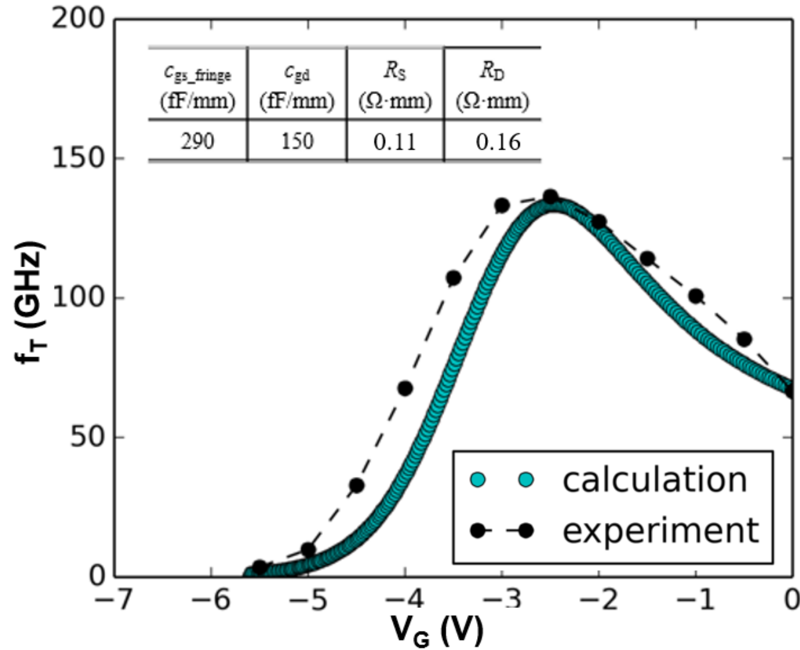



**Figure. 2.7 Calculated device performance $f_T$ with different gate voltage and experimental results**

### *2.4. Summary*

In this chapter, A physics-based I-V model has been proposed for scaled N-polar GaN transistor based on velocity transport based optical phonon scattering. Using MIT virtual source model as a fitting function for charge, the calculated results demonstrate a good fitting with DC and RF experiment data without considering the nonlinear resistance in the access region. This chapter explained the N-polar GaN deep recess device performance with such a physics-based model, showing good potential of predicting device RF performance, S-parameters and large signal performance with extensive work of this model. The modeling work also verified that the N-polar GaN deep recess HEMT obtain predictive manner on the DC and small signal RF performance. After the validation, delay terms in delay analysis are

evaluated and used for identifying major source of delay. The delay term extraction has been studied by Romanczyk [37] and the components consists of the delay is presented in Figure 2.8. As a device with low contact resistance and high conductivity in the access region, the N-polar GaN deep recess HEMT has well-control delay relaxed to resist divider and Miller effect, and the intrinsic delay and fringing capacitance related delay are two main components in device delay, with small variation with different device dimension (Lg, Lgs and Lgd). To further reduce the delay and improve the gain, an increased gm can benefit both intrinsic delay and fringing capacitance delay simultaneously, and the fringing capacitance in the deep recess structure needs to be reduced. Inspecting the device structure and fabrication, the GaN cap layer and extrinsic dielectric passivation are expected to result in increased fringing capacitance. As a tradeoff between great dispersion control and device delay, the GaN cap in N-polar GaN deep recess device is unique and needs more investigation. Further discussion on dependence of fringing capacitance on GaN cap layer and passivation is given in chapter 3 to better understand the design space and optimize the device performance.

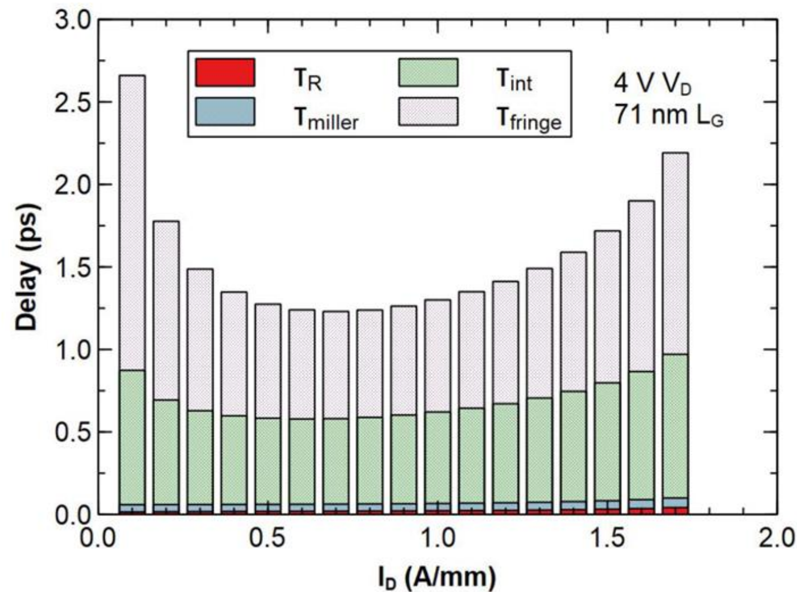



**Figure. 2.8 Extracted delay terms of the N-polar GaN deep recess device in [37] with a $L_G$ of 71 nm© 2020 IEEE.**

# III. Electrostatics study on fringing capacitance

The introduction of GaN cap and good passivation in N-polar GaN deep recess HEMT are critical for DC-RF dispersion control. N-polar GaN deep recess HEMTs with the self-aligned slant gate technology have demonstrated excellent performance [1-3] and the T-gate of the device is mechanically robust due to metal contact with the slant gate trench. However, the GaN cap layer and passivation can also add fringe capacitance.

This chapter discuss the studies on fringing capacitance in the N-polar GaN deep recess HEMT. Section 3.1 gives introduction of fringing capacitance problem in N-polar GaN deep recess HEMT. An experiment designed to investigate the impact on fringing capacitance from GaN cap layer and SiN passivation is presented in Section 3.2. Discussion on GaN cap for fringing capacitance is presented in Section 3.3 with both experimental and simulated results. Section 3.4 summarizes the works in this chapter.

## *3.1. Fringing capacitance in N-polar GaN deep recess HEMT*

The gate fringing capacitance is the extra parasitic capacitance in addition to the intrinsic gate capacitance, which has no contribution to the transconductance of the device and cause delay and reduces the device gain. In high aspect ratio device, fringe capacitance is generally small compared to intrinsic capacitance and has negligible effect on device performance. However, in short gate length devices like N-polar GaN deep recess HEMT, the fringing capacitance/intrinsic capacitance ratio got affected by the reduced aspect ratio and fringing capacitance becomes more important for device RF performance.

Investigation in fringe capacitance is especially important for N-polar deep recess devices because of the selective etch [39] used for gate recess gives out a slanted profile. Filling the slanted gate trench with metal naturally results in a higher fringe capacitance compared to

fully vertical gate stem. This chapter quantitatively studies the fringe capacitance dependence on the GaN cap layer and the passivation layer and examines the effect of passivation on device RF performance. This chapter aims to better understand the design space of needed passivation and GaN cap thickness for achieving high efficiency and high power.

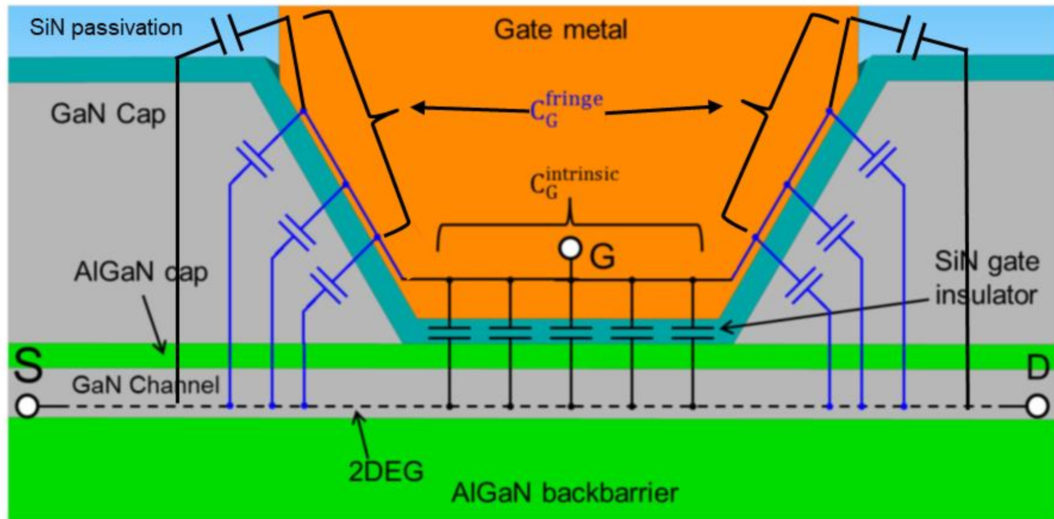



**Figure. 3.1 Gate capacitance and fringing fields resulting from the recess etch sidewall slope in N-polar GaN deep recess HEMT [40]**

### *3.2. Impact on fringing capacitance from passivation*

Figure 3.1 depicts the region under the gate and the fringing capacitances which arise from the slanted recess profile and SiN passivation. To examines the impact on fringe capacitance, experiments on N-polar GaN deep recess HEMT with different passivation and thin GaN cap layer were discussed in this section.

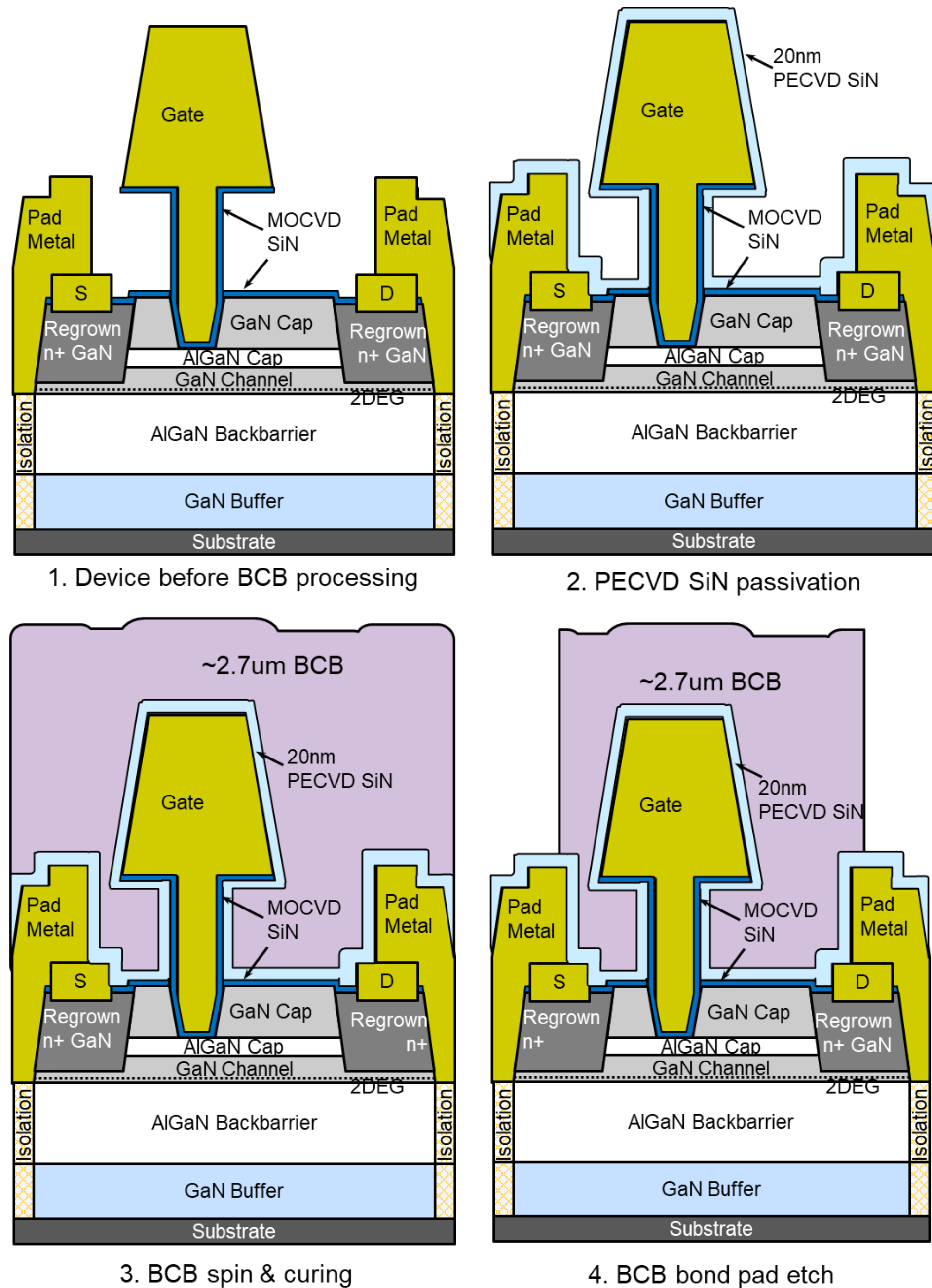



**Figure. 3.2 Device fabrication process steps after completion of the un-passivated N-polar GaN deep recess HEMT**

The N-polar GaN deep recess HEMTs analyzed in this report were grown using metal-organic chemical vapor deposition (MOCVD) on a miscut sapphire substrate with the

structure shown in Figure. 3.2 (a). The device structure has a 20nm GaN cap layer, which is different from the 47nm GaN cap used in previously reported N-polar GaN deep recess device [1-3] for investigate impact from GaN cap layer thickness. The devices were fabricated using the self-aligned deep recess process flow that will be detailly discussed in chapter 4. After the completion of transistor processing, the devices were passivated with 20 nm of plasma-enhanced chemical vapor deposition (PECVD) SiN. In addition, a 2.7 um bis-benzocyclobutene (BCB) are coated on the sample as a thick low dielectric constant passivation film. Both DC and RF characterization were taken prior-to and after SiN deposition, and again after BCB encapsulation to check impact of passivation on device performance and examines the implement of BCB as a RF wiring environment. Figure 3.2 illustrated the process flow of this experiment after transistor completion. The reported devices feature a 2×37.5 μm gate width, 70 nm source-to-gate spacing, and 420 nm source-to-drain spacing. Devices with a gate length (Lg) series of 51, 87 and 122 nm are measured.

### ***3.2.1. Device DC and RF performance at different passivation state***

Device DC performance has been measured at 3 different passivation stages, As shown in Figure 3.3, device obtains a maximum DC current density of 1.56 A/mm at $V_{DS}$ of 4 V and $V_G$ of 0 V with an on-resistance of 0.6 Ω-mm. At $V_{DS}$ of 6 V, the peak transconductance (gm) was measured to be 462 mS/mm. Using the drain current injection technique described in [41], the device breakdown voltage measured to be 46 V for 1 mA/mm of current density. Figure 3.3 shows the comparison of device output performance at different passivation states. No significant changes in the threshold voltage or other DC parameters were observed as a result of the SiN passivation or BCB encapsulation.

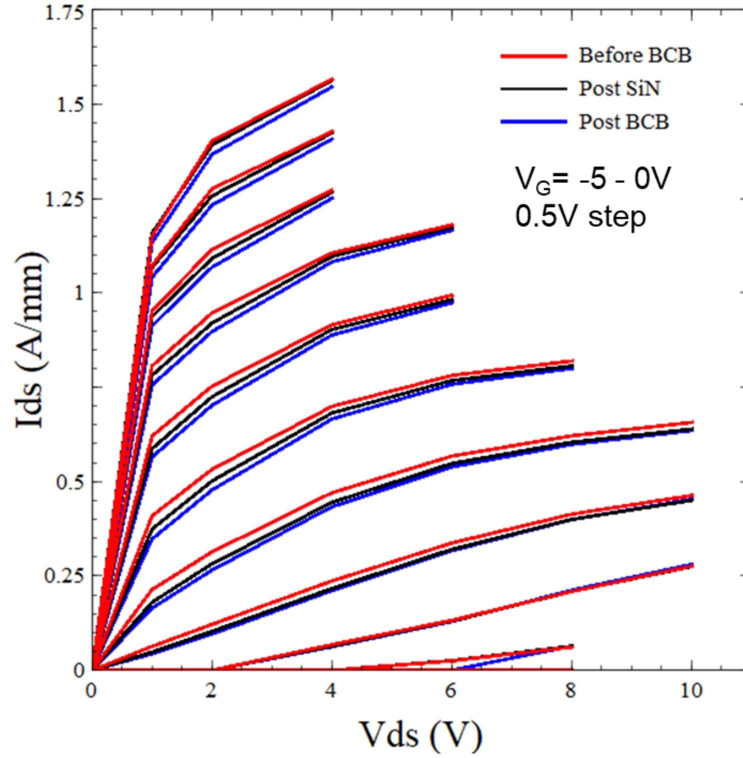



**Figure. 3.3 Device DC outputs performance at before PECVD SiN, after PECVD SiN, and after BCB coating**

Bias-dependent small-signal S-parameters were measured up to 67 GHz with probe tip calibration using Line-reflect-reflect-match (LRRM) method. On-wafer open and short de-embedding was performed. Current ($f_T$) and power-gain ($f_{max}$) cutoff frequency were extracted with $|h21|^2$ and the unilateral gain (U). Figure. 3.4 (a-b) show the peak $f_T$ and peak $f_{max}$ of different Lg devices prior to and after the dielectric coating. The passivation of SiN caused 6-10% decrease in $f_T$ and 1-3% decrease in $f_{max}$, the BCB encapsulation further lowered the $f_T$ by 10-13% and $f_{max}$ by 20-23%.

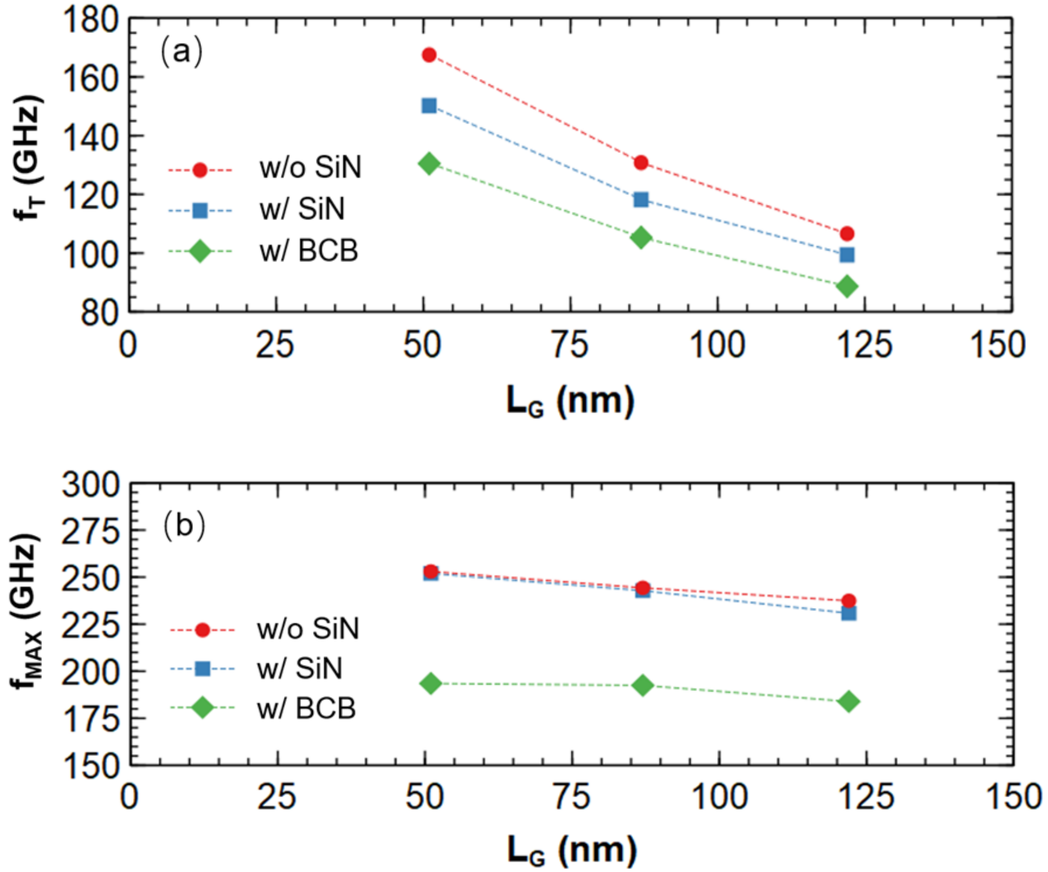



**Figure. 3.4 Devices peak $f_T$ (a) and peak $f_{max}$ (b) at 10V versus $L_g$ at before PECVD SiN, after PECVD SiN, and after BCB coating.**

### *3.2.2. Small signal equivalent circuit extraction*

To investigate the cause of $f_T$, $f_{max}$ changes with different passivation, small-signal equivalent circuit parameters were extracted at the peak fmax bias point using the methodology described in 328]. The small signal equivalent circuit model is presented in the Figure. 3.5 and the extracted results are presented in Table I.

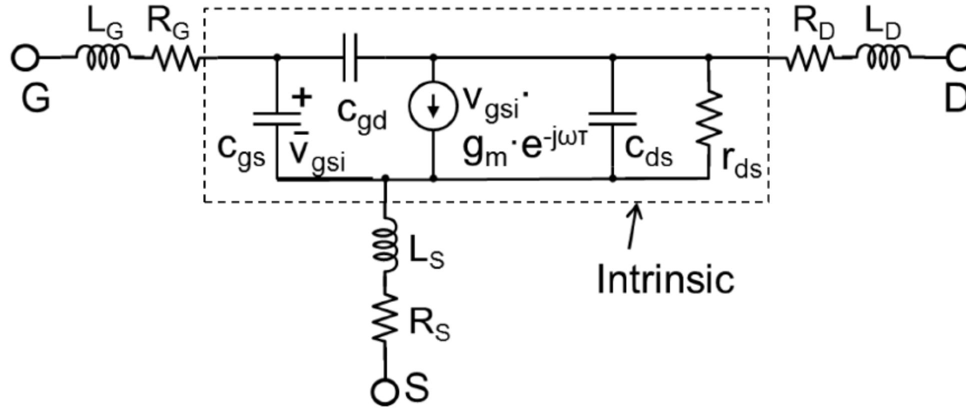



**Figure. 3.5 The small signal equivalent circuit model used for N-polar GaN deep recess HEMT [40]**

| | $C_{gs}$ (fF) | $C_{gd}$ (fF) | $C_{ds}$ (fF) | $g_m$ (mS) | $\tau$ (ps) | $R_{ds}$ (Ω) | $R_g$ (Ω) | $R_s$ (Ω) | $R_d$ (Ω) |
|---|---|---|---|---|---|---|---|---|---|
| Pre-SiN | 39.7 | 7.7 | 15.1 | 45.5 | 0.31 | 258 | 1.9 | 2.0 | 3.4 |
| Post-SiN | 42.1 | 8.1 | 16.5 | 44.3 | 0.38 | 264 | 1.5 | 2.0 | 3.8 |
| Post-BCB | 45.3 | 11.8 | 15.9 | 43.6 | 0.31 | 266 | 1.8 | 2.0 | 3.5 |

**Table 3.1 Summary of small signal parameters at the peak $f_{max}$ bias ($V_{GS}$ = -3.5 V, $V_{DS}$ = 10 V) for the 51 nm $L_g$ device**

The decreased device gain with passivation and encapsulation is mainly attributed to the increased gate-to-source capacitance ($C_{gs}$) and gate-to-source capacitance ($C_{gd}$). After the 20 nm SiN passivation, the device $f_T$ decreased by 11 GHz and the maximum stable gain (MSG) at 67 GHz was reduced by 0.26 dB, which in mainly cause by the 2.4 fF increase in the $C_{gs}$. Following the encapsulation of BCB, the device $f_T$ further decreased by 21 GHz and the MSG at 67 GHz has a reduction of 1.39 dB because of the 3.2 fF increase in $C_{gs}$ and 3.7 fF increase in $C_{gd}$. As shown in the Figure 3.6, the increase of gate capacitance is mainly the increase of fringing capacitance, as expected.

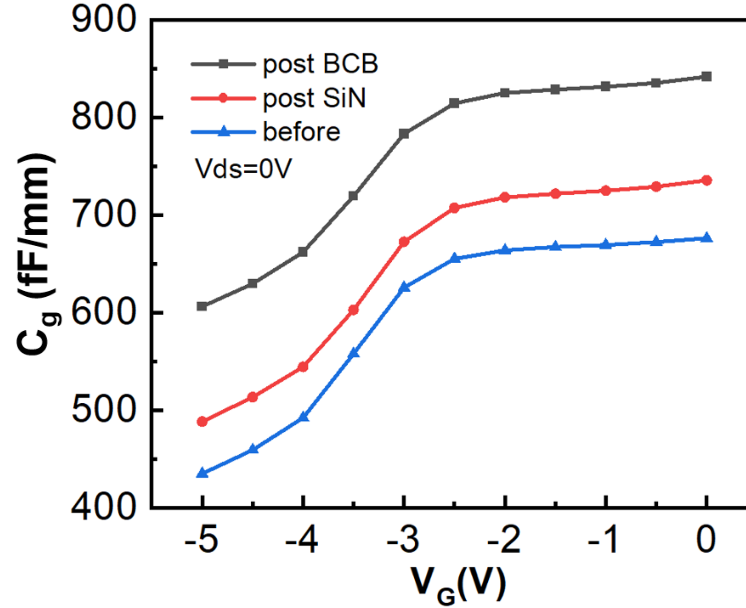



**Figure. 3.6 Extracted total gate capacitance as a function of gate voltage at different passivation states**

### *3.2.3. fringing capacitance extraction*

The fringe capacitances were extracted using y-intercept of $C_{gs}$ ($C_{gd}$) versus gate length ($L_g$) at constant current density using the method discussed in [37]. Figure. 3.7 shows the extraction of fringe capacitance prior to and after the passivation. The same slope shown in $C_{gs}$ ($C_{gd}$) vs $L_g$ proves that the intrinsic capacitance of the device is not affect by the passivation. As shown in Figure 3.8, the 20 nm SiN passivation slightly increased the fringe $C_{gs}$ and $C_{gd}$ by 25 fF/mm and 10 fF/mm. The effect on $C_{gd}$ is smaller due to the depletion of the 2DEG under bias. The BCB encapsulation has a stronger effect and increase the fringe $C_{gs}$ and $C_{gd}$ by 79 fF/mm and 42 fF/mm. The strong impact on fringing capacitance and device gain from BCB encapsulation suggests an airbox encapsulation may be preferred to implement BCB as RF wiring environment.

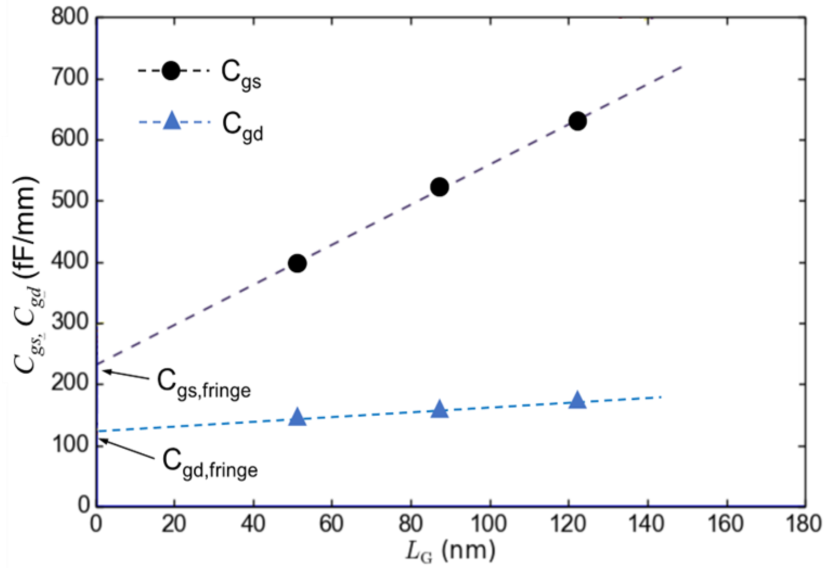



**Figure. 3.7 Extraction of fringing capacitance as a function of current density at 4V $V_{DS}$ from the measured $C_{gs}$ and $C_{gd}$ for devices before the PECVD passivation.**

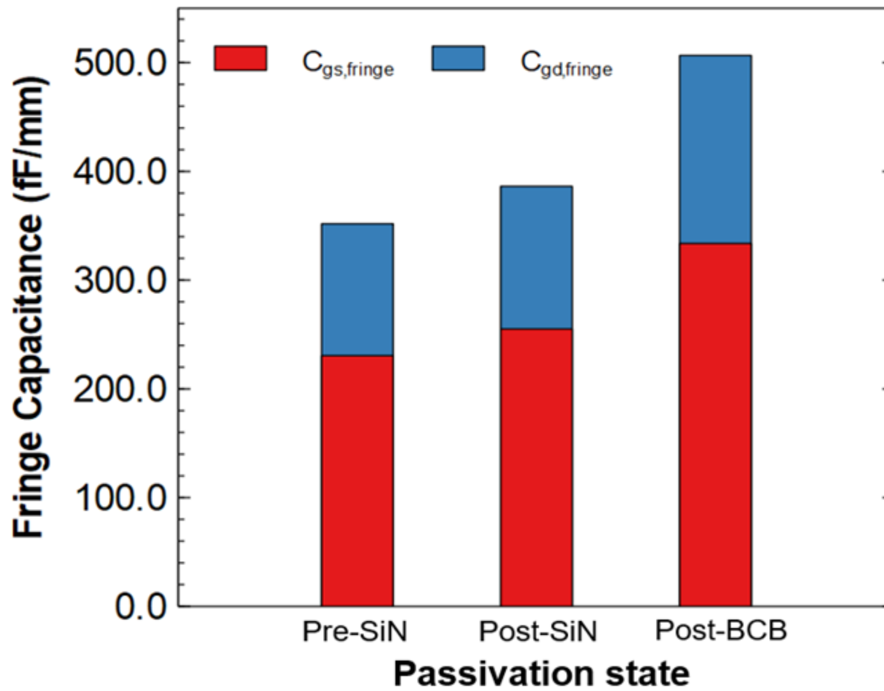



**Figure. 3.8 The extracted fringing capacitance of devices 4V $V_{DS}$ and 200mA/mm $I_D$ before PECVD SiN, after PECVD SiN, and after BCB coating.**

### *3.3. Impact on fringing capacitance from GaN cap*

One major focus of fringing capacitance analysis is the effect from the slope sidewall of GaN cap layer due to selective etch. As shown in the Figure 3.1, a slanted profile is formed after selective etch in the gate recess trench [39] and the slope of the sidewall is measured to be around 60° (90° being a perfectly vertical sidewall). Depositing gate metal on top of the sidewall will introduce fringing capacitance.

This section discusses the impact on fringing capacitance from thinning the GaN cap thickness. Results from experimental data and COMSOL electrostatics simulation are both presented and show good agreement, providing guidance on the design space of needed passivation and GaN cap thickness for improved device gain with high output power.

Since the devices discussed in section 3.3 use different GaN cap layer thickness from previous reported N-polar deep recess HEMTs, comparison of fringe capacitance has been performed to evaluate the effect from GaN cap layer. Figure. 3.9 shows the comparison of extracted fringe capacitance between the device with a 20 nm GaN cap layer and a previous reported 47 nm GaN cap device [1-3] with same device dimensions and similar epitaxial structure. The fringe $C_{gs}$ is reduced from 292 fF/mm to 231 fF/mm by reducing the GaN cap thickness from 47 nm to 20 nm, The fringe $C_{gd}$ decreased slightly from 126 fF/mm to 121 fF/mm with 20 nm GaN cap, as expected from the increased 2DEG depletion towards the drain.

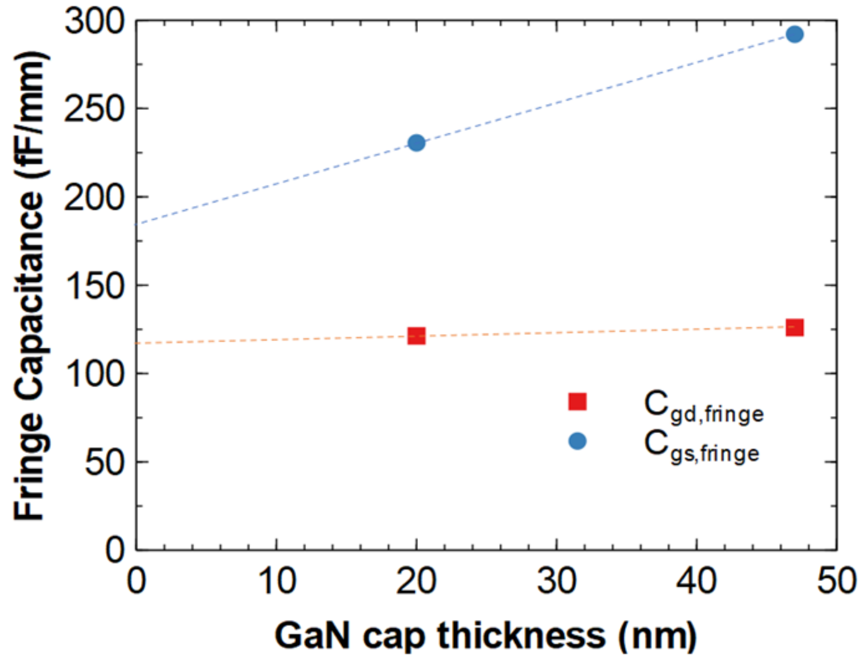



**Figure. 3.9 Comparison of fringe capacitance at 4V $V_{DS}$ and 200mA/mm $I_D$ without PECVD SiN, for devices with a 20nm GaN cap and a previously reported 47nm GaN cap [37].**

This result shows that lowering the GaN cap layer thickness from 48 nm to 20 nm can reduce the fringe capacitance while maintain good channel conductivity, which is attractive to device design of improved gain and efficiency.

***3.3.1 fringe capacitance analysis with 2D COMSOL simulation***

To understand the extracted fringe capacitance, the simulation on device fringing capacitance was done using 2D COMSOL Multiphysics software. By implementing the electrostatics model, device structure is built in 2D COMSOL simulation as shown in Figure 3.10. The gate metal, ohmic metal, regrown n+ GaN and 2DEG in the channel were treated as perfect conductors. AlGaN cap layer was absorbed in GaN cap as it has similar dielectric constant as GaN. Both SiN on the gate stem and SiN on the GaN cap surface resulted from device fabrication were included. No depletion of the 2DEG were presented in the simulated

structure as what would normally be the case at the source side of the gate for the bias condition of fringing capacitance extraction. This simulation is of most use for understanding $C_{gs}$ because $C_{gd}$ is generally small relative to $C_{gs}$ with the charge depletion and the electrostatics at the drain side of the gate is hard to simulate with the high electric field and depletion. To get better idea of fringing $C_{gd}$, Complicated TCAD simulation will be needed for such short channel device, which is not the focus of this section. The simulated device structure is symmetric, and half of the simulated gate capacitance represents the simulated $C_{gs}$.

The relative dielectric constants used in the simulation are 8.9 for GaN, 7 for SiN and 1 for air. The device dimensions are chosen based on the device fabrication and listed in Table 2. To extract the fringing capacitance, $C_{gs}$ was simulated with different gate length to get the y-intercept of $C_{gs}$ versus gate length.

| $t_{stem}$ (nm) | $t_{chan}$ (nm) | $t_{top}$ (nm) | $L_{g_top}$ (nm) | $t_{n+GaN}$ (nm) | $L_{gs}$ (nm) | $t_{ohmic}$ (nm) | $L_{s_n+GaN}$ (nm) |
|---|---|---|---|---|---|---|---|
| 250 | 11 | 500 | 420 | 50 | 75 | 120 | 100 |

**Table 3.2 Device dimension used in the COMSOL electrostatics simulation**

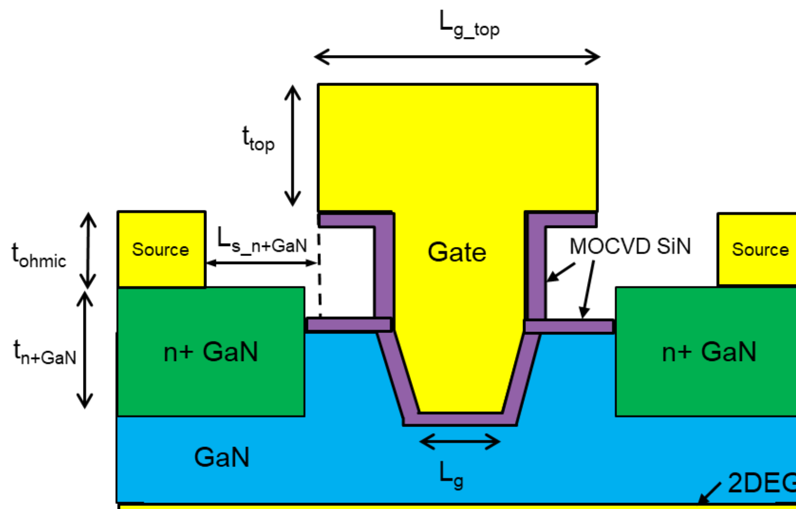



**Figure. 3.10 Simulated device structure with 60-degree slope side wall in the gate recess trench**

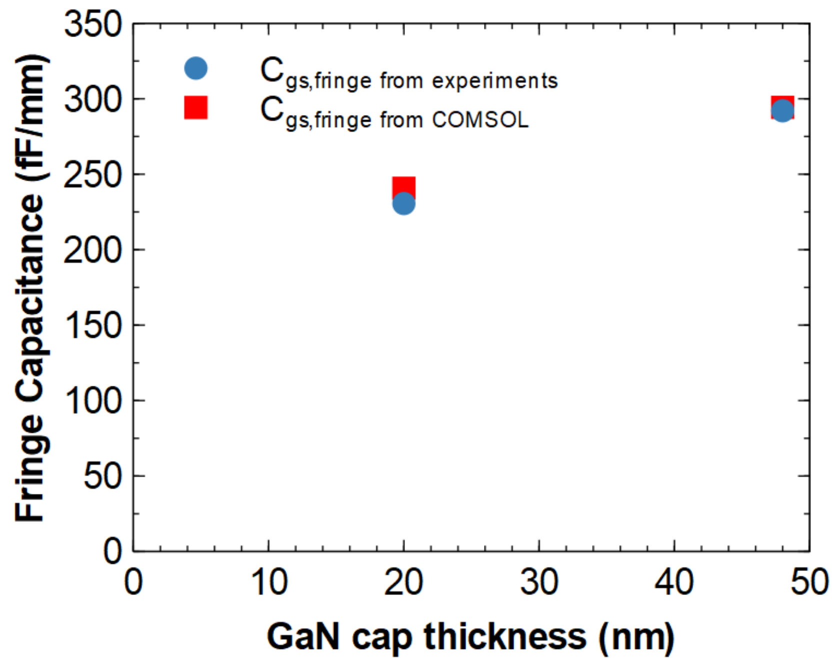



**Figure. 3.11 Comparison of fringe capacitance from COMSOL simulation and experimental extraction for devices with a 20nm GaN cap and 47nm GaN cap.**

As shown in Figure 3.11, the simulated fringe $C_{gs}$ agreed with the extracted fringe capacitance very well and demonstrated the reduction on fringe capacitance with thinning the GaN cap thickness to 20 nm. Moreover, the COMSOL simulation verified the predictive manner of N-polar GaN deep recess device again, showing the extracted capacitance agrees with the expected electrostatics.

### *3.4. Summary*

This chapter presents electrostatics study on fringing capacitance of the N-polar GaN deep recess HEMT. Experiments that aim to investigate the dependence of gate fringe capacitance on GaN cap layer and passivation for N-polar GaN deep recess HEMT were designed and

conducted. The results show that the GaN cap layer can affect the fringe capacitance mainly by introducing more fringe Cgs on the device. Reducing the GaN cap layer from 47nm to 20 nm helped to lower the fringe capacitance by 20%, while maintaining high channel conductivity. The thin SiN passivation has a small effect on fringe capacitance and thick dielectric coating, such as BCB encapsulation, has a large capacitive impact and cause the loss of gain. To understand the extracted capacitance, 2D COMSOL simulation was conducted to simulate the device gate capacitance. The COMSOL simulation shows good match with the fringing capacitance extracted from experiments, indicating device capacitance agrees with the expected electrostatics and predictive behavior manner of N-polar GaN deep recess HEMT.

The results provide guidance on the design of N-polar GaN deep recess HEMT to achieve less delay and higher gain. In the next chapter, 20 nm GaN with thin 20 nm passivation are chosen to be implemented into device design for improved gain and efficiency.

# IV. N-polar GaN deep recess HEMT with record efficiency at 94 GHz

After device modelling and electrostatics study on fringing capacitance of N-polar GaN deep recess HEMT, new designs have been made on the basis of previous state-of-art N-polar GaN deep recess HEMT.

As a device technology with record power performance at W-band, N-polar GaN deep recess HEMT has been developed based on many great works done by previous students and collaborators. Starting from utilizing the N-polar GaN RF device process developed by Denninghoff [42] and the $BCl_3/SF_6$ dry etch developed by Buttari [39], initial devices with the deep recess structure were demonstrated by Wienecke [43] and Romanczyk[44]. After investigations on device gate process [45], a self-aligned process was later selected for the N-polar GaN deep recess device process, which ensures well-controlled dispersion and also simplifies the fabrication process [1-4]. Device reported in this chapter follows the self-aligned process used in prior N-polar GaN deep recess HEMT work in many ways with new designs and improvement implemented. Optimization has been proposed and implemented on both sample epitaxy growth and device fabrication to increase the device gain and efficiency. Besides, great commercial GaN-on-sapphire epi with exceptional electron mobility in the channel was also applied to provide great channel conductivity.

This chapter describes the design, fabrication and measurement of the N-polar GaN deep recess HEMT with new designs. Section 4.1 discuss about the epitaxy structure and optimization implemented in epi growth of the sample. Detailed device fabrication and processing improvement are given in Section 4.2. Section 4.3 presents the device measurement results (DC, RF, pulsed I-V, breakdown) and demonstrates the N-polar GaN

deep recess HEMT with record gain and efficiency at W-band. A summary of the device optimizations and device performance is presented in Section 4.4.

### *4.1. Sample epitaxy growth*

The N-polar GaN HEMT sample reported in the chapter was grown as a 100 mm wafer on a commercial metal-organic chemical vapor deposition (MOCVD) platform at Transphorm on a miscut sapphire substrate [46-47]. The sample epitaxial structure is shown in Figure. 4.1. The layer structure consists of, from bottom to top, a semi-insulating GaN buffer, a 20nm graded and Si-doped AlGaN back-barrier and a 10nm $Al_{0.38}Ga_{0.62}N$ spacer, 0.7 nm AlN layer, 10 nm GaN channel and a 2.6 nm $Al_{0.27}Ga_{0.73}N$ cap layer, a 20 nm GaN cap layer, and a 5 nm in-situ MOCVD SiN film.

Sapphire substrate is chosen for this device for serval considerations: a. As a very attractive RF electronics platform that builds upon a wider ecosystem, GaN-on-sapphire is wildly used in GaN-based LEDs industry. Large-area and low-cost sapphire substrate is available and also used in power-switching electronics [48] and mm-wave electronics [49]. Recently, commercial N-polar GaN-on-sapphire epi for RF application has been demonstrated by Transphorm [46-47]. b. N-polar has already shown good power performance at W-band with GaN-on-sapphire RF HEMT with UCSB grown epi, the device demonstrated performance metrics comparable to those observed for N-polar GaN-on-SiC below 16 V $V_D$ bias, showing feasibility of this GaN-on-sapphire. c. For GaN RF transistor at W-band, the ability to enhance efficiency simultaneously with high output power density is still limited by the gain of the device, so the use of GaN-on-sapphire can be considered.

Compared with previous N-polar deep recess devices [1-4], several modifications in epitaxy layer have been made to improve device gain. Based on the discussion in chapter 3,

the GaN cap thickness was reduced to 20 nm to lower the fringing capacitance while still maintaining the high access region channel conductivity and good dispersion control [50]. Secondly, the commercial GaN-on-sapphire epi used in this work provides exceptional electron mobility in the GaN channel. Using the TLM and capacitance–voltage measurements, GaN-capped access region shows a low sheet resistance of 245 Ω/sq with 2DEG mobility being close to 2000 $cm^2/(V \cdot s)$, which is really beneficial for achieving high gain. Lastly, the GaN channel thickness was adjusted from conventional 12 nm to 10 nm for a potential better gate to channel distance and mobility consideration [51-52].

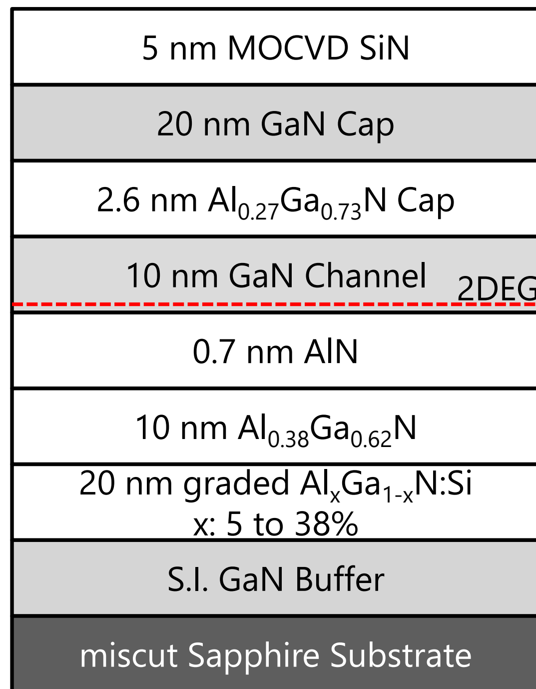



**Figure. 4.1 Epitaxy layer structure of the reported N polar GaN deep recess HEMT.**

### *4.2. Device fabrication*

In this section, the fabrication process of reported N-polar GaN deep recess HEMT is presented. The conventional process will be first described and then the gate process improvement is discussed.

After iterations of processing development from previous students and collaborators, the N-polar GaN deep recess HEMT fabrication is already complicated and contain hundreds of processing steps in university cleanroom fabrication. To elaborate the detailed device process, the fabrication is described in several modules.

The first module contains the contact regrowth of n+ GaN and isolation for devices (Figure 4.2). The N-polar GaN deep recess HEMT processing starts with the deposition of hard mask. The hard mask is deposited to protects the device source-to-drain region during the later n+ GaN regrowth. Using atomic layer deposition (ALD), Al2O3 is deposited as a etch stop layer, and a SiO2 is then deposited with plasma-enhanced chemical vapor deposition (PECVD) as the main body of hard mask. A thin Cr layer is deposited on top of SiO2 using electron beam evaporation and an EBL process is used to define the device source-to-drain spacing ($L_{sd}$). The EBL process is done with JEOL 6300 EBL system at UCSB. After O2 descum on Cr (oxidize the surface for better adhesion), a negative deep UV photoresist of UVN 30 is coated on the sample and used for patterning Cr. After EBL writing and development, an inductively coupled plasma (ICP) dry etch utilizing Cl2/O2 then etches the Cr mask and stops at the SiO2. Then PR is removed with O2 Asher and scanning electron microscope (SEM) is performed to measure the line width. After examining of the dimensions, ICP CF4/CHF3/O2 dry etch is used to pattern the SiO2 mask and stop at the Al2O3. ICP etch using Cl2/O2 chemistry is used again to remove Cr and has no etch on SiO2 and Al2O3, followed by using of AZ300

MIF developer (TMAH-based) for wet etch of Al2O3. Although it was demonstrated that N-polar GaN surface etches in developer, the in-situ MOCVD SiN can protects the sample surface.

After CF4/O2 based etch in ICP to remove the in-situ MOCVD SiN, GaN cap surface outside of the source-drain region is exposed. A BCl3/SF6-based ICP etch developed in previous N-polar GaN work [39] is performed to selectively remove the GaN cap and stops on AlGaN cap. Then, the thin AlGaN cap is etched using BCl3/Cl2-based reactive ion etch (RIE). After RIE etch, 20 nm UID GaN and 30 nm highly Si-doped n+ GaN is grown on the sample using plasma-assisted molecular beam epitaxy (PAMBE). The source-drain region won't have regrown n+ GaN because of the protection of Al2O3/SiO2 hard mask. Then, the Al2O3/SiO2 hard mask is removed by soaking the sample in 1:1 HF: HNO3 solution with ultrasonic. The photolithography is applied to define the device active region. Together with etch of the regrown n+ GaN outside the active region using ICP dry etch, ion implantation is performed on the sample to provide good isolation between devices. Photoresist and ALD SiO2 protection layer are then stripped and 7 nm MOCVD SiN is deposited on sample surface for protection of later process.

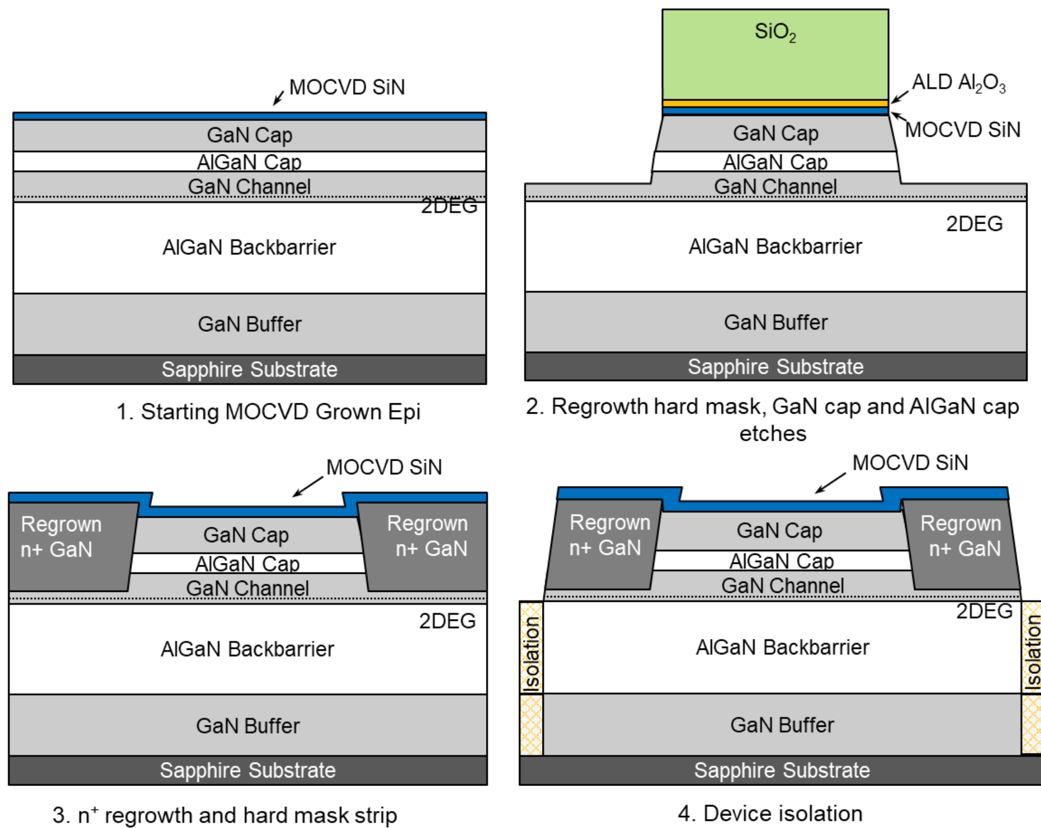



**Figure. 4.2 Device fabrication flow starting from n+ GaN regrowth to device isolation (schematics are not drawn to scale).**

Following device isolation, the next module includes the gate recess and T-gate process. A hard mask consists of ALD Al2O3 and 225-nm PECVD SiO2 is deposited. The thickness of hard mask is selected for the consideration of the height of the T-gate stem. To define the gate recess pattern, EBL process using E-beam resist CSAR is introduced. After the exposure and development, similar SiO2/Al2O3 hard mask etch in the regrowth module is used to etch the PECVD SiO2 and ALD Al2O3. After removing the SiN protection layer with CF4/O2 based ICP etch, the GaN cap layer in the gated region is etched using BCl3/SF6 selective etch and the etch stops on the AlGaN cap. Then the SEM imaging is used to check the gate recess and measure the actual gate length at the bottom of the recess. A 6 nm MOCVD SiN is then deposited on the recess bottom as gate dielectric. For conventional N-polar GaN deep recess

HEMT with self-align gate process, another EBL process is performed with UV6 resist to define the top-gate and Cr/Au is deposited using E-beam evaporation. After lift-off, the T-gate of the device is formed. Using the diluted buffered hydrofluoric acid (BHF), the hard mask is removed, and the T-gate is released (Figure 4.3).

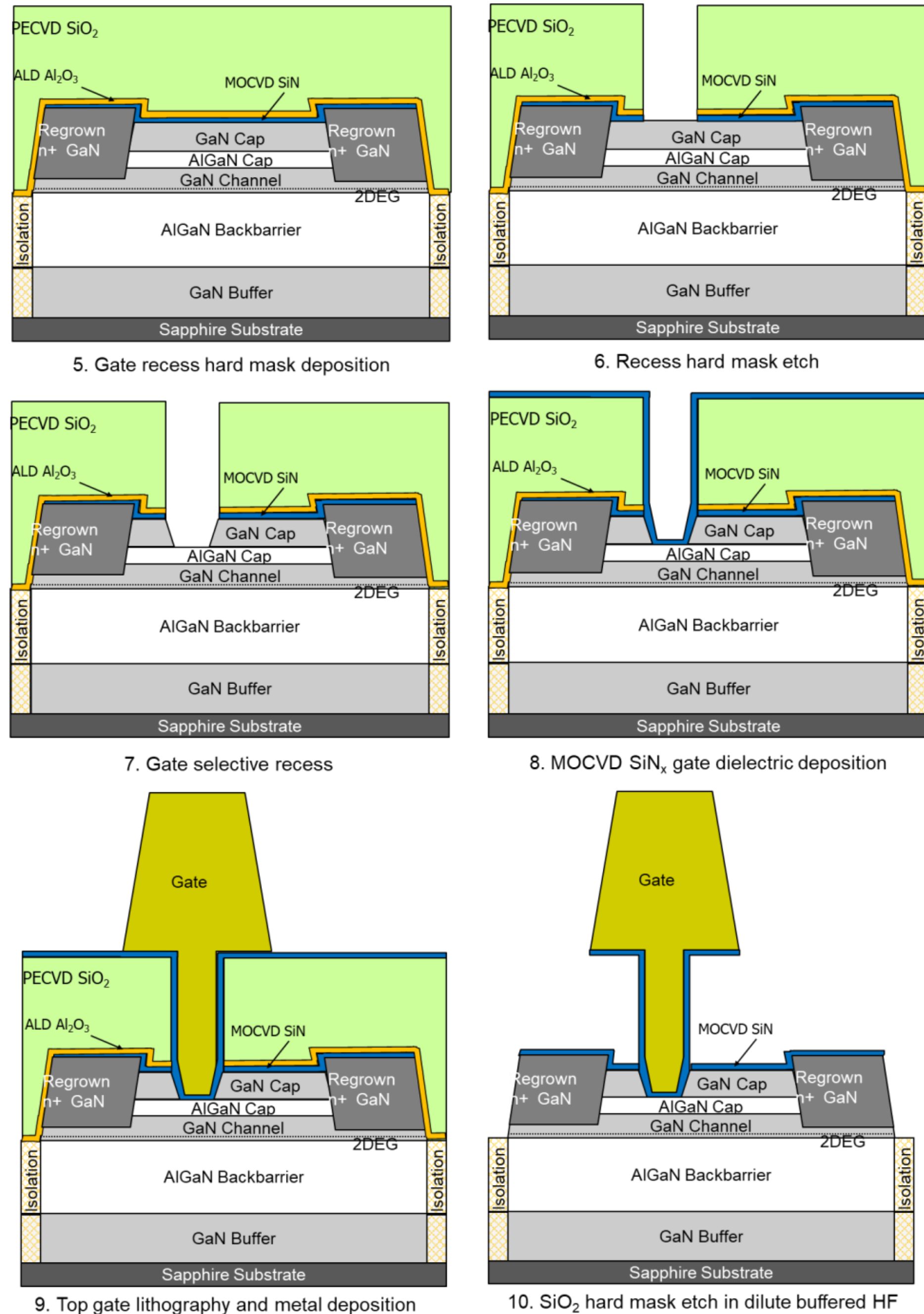



**Figure. 4.3 Device fabrication flow including gate recess and T-gate process (schematics are not drawn to scale).**

The final module of the device fabrication is for device ohmic contacts and probe pad metallization. Using photolithography with careful alignment, ohmic contact pattern is defined as N-polar GaN deep recess HEMT is high scaled. After etching the SiN protection layer in the ohmic contact region with ICP CF4/O2-based etch. A BCl3/Cl2 etch in RIE and dip in HCl are performed prior to the metal deposition to help achieving low contact resistance as discussed in [53]. Then, Ti/Au is deposited by E-beam evaporation and lifted off for ohmic contacts. The process ends with the patterning of probe pad and Ti/Au E-beam evaporation. The fabricated device structure is presented in Figure 4.4.

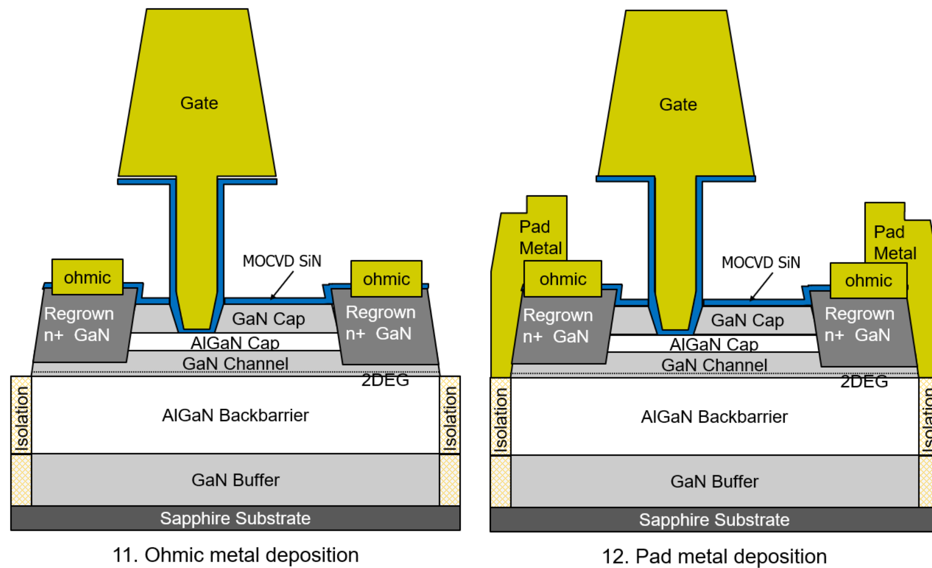



**Figure. 4.4 Final device fabrication steps of ohmic contact and probe pad metallization (schematics are not drawn to scale).**

### *4.2.1 ALD Ru gate process*

In the conventional N-polar GaN deep recess HEMT, Cr/Au gate process was used as for the T-gate metallization. The Cr is adopted as the initial metal to set the work function and used as an adhesion layer for contact with the Au to form the T-gate. First run of the device

fabrication was completed using this approach. The small signal measurement shows that on the long channel device with Lg of 138 nm, good peak $f_T$/ peak $f_{max}$ of 74/173 GHz was measured (Figure. 4.5 a-b). The extraction of small signal equivalent shows a low Rg of 2.7 ohm achieved on the device, demonstrating the effectiveness of good T-gate metallization.

However, when measuring the scaled device with Lg smaller than 100 nm, the power gain and fmax drops. As shown in Figure. 4.6 a-b, the device with 66 nm Lg, 420 nm Lsd and 2 x 37.5 μm gate width, the peak fT is measured to be 107.5 GHz, but the peak fmax is only 39 GHz. The extraction of gate resistance using small signal equivalent circuit is presented in Figure 4.7 and shows a high Rg (over 50 ohm) in the device, causing the degradation of gain an

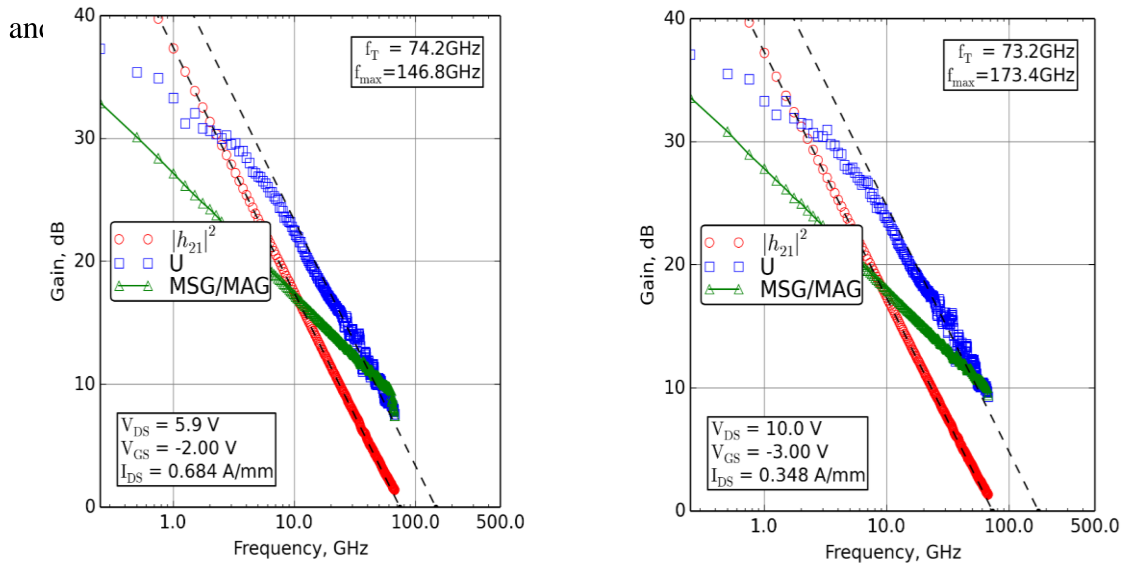



**Figure. 4.5. Small signal RF measurement at (a)peak fT and (b) peak $f_{max}$ bias condition for long channel device with 138 nm Lg and 600 nm Lsd**

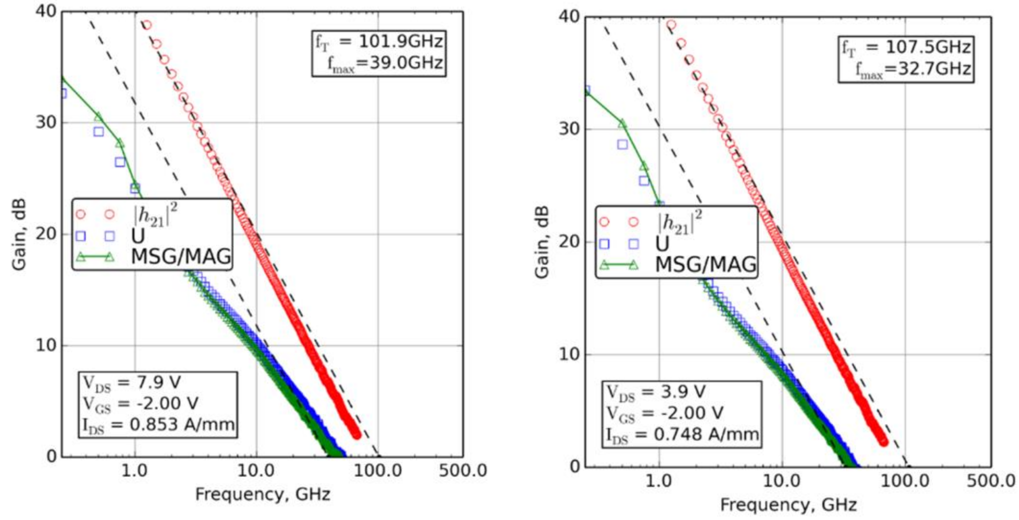



**Figure. 4.6 Small signal RF measurement at (a)peak $f_T$ and (b) peak $f_{max}$ bias condition for long channel device with 66 nm Lg and 420 nm $L_{SD}$, showing a low $f_{max}$.**

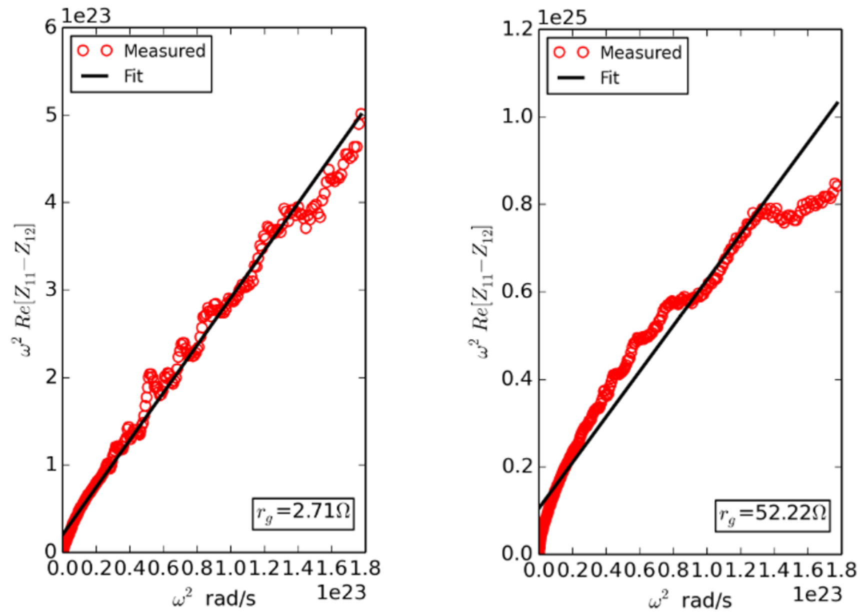



**Figure. 4.7 $R_G$ extraction from small signal equivalent circuit of (a) long channel device with 138 nm $L_G$ and 600 nm Lsd and (b) 66 nm $L_g$ device with 420 nm $L_{SD}$.**

It has been previously observed that fmax saturates at 60 nm of Lg and decrease rapidly for device with Lg smaller than 60 nm [54]. This degradation of Rg was attributed to the gate

recess trench filling with E-beam evaporation, as the gate trench being high-aspect ratio and very narrow. However, in the device reported in this chapter, the adoption of thinner GaN cap can shrink the process window of the Cr/Au gate process. Compared with device having a 48 nm GaN cap layer, the slope sidewall of the recess etch in 20 nm GaN cap device is shorter and the gate stem is narrower, getting the E-beam evaporated Cr/Au process closer to the process limit.

To solve the gate process issue, the ALD Ru gate process is proposed and implemented into the device fabrication. The ALD Ru gate was demonstrated in N-polar GaN Schottky diodes previously [55-56]. Recent application of ALD Ru gate on N-polar GaN deep recess HEMT with 48 nm GaN cap show great results of high PAE of 33.8% with high linear gain of 8.1 dB [2]. In the fabrication of device reported here, the ALD Ru gate metallization was adopted with the detailed process as follow:

After the completion of MOCVD SiN gate dielectric deposition, the sample is loaded into the ALD chamber for the deposition of Ru. The ALD Ru deposition is believed to have better gate trench filing than the conventional Cr/Au gate process. Then, similar EBL process as the Cr/Au gate process is used to define the top gate. Using E-beam evaporation Pt/Au and lift-off, the top gate is formed and used as a hard mask in O2/Cl2 based ICP etch so that the Ru under the top gate is protected, and Ru elsewhere is etched. To make sure the fully removal of Ru on non-gate region, wet etch using nitrate/nitric acid based Ru etchant is performed to remove the Ru on the sidewall of the deeply etched structures like alignment marks. After finishing the etch of Ru, the hard mask is then removed and release the T-gate, The ALD Ru gate process flow is described in Figure 4.8. The rest of the device fabrication follows the conventional process.

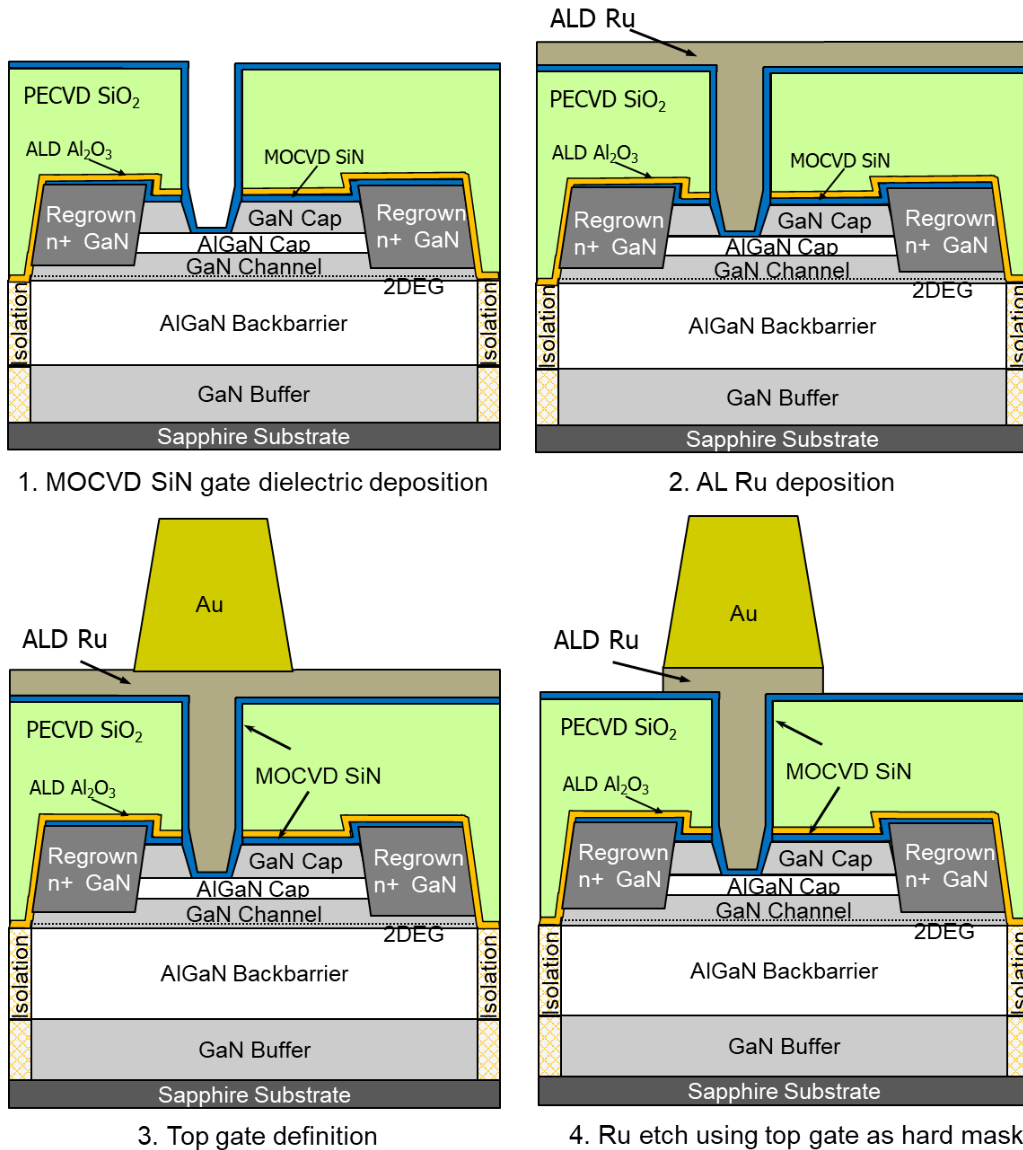



**Figure. 4.8 ALD Ru gate process flow starting from the deposition of gate dielectric (schematics are not drawn to scale).**

### *4.2.2 Fabricated device physical dimensions*

The fabricated N-polar GaN deep recess device is highly scaled in a lot of aspects to achieve high gain and high efficiency. To better understand the fabricated device structure, a schematic definition of the device physical dimensions is given in Figure 4.9. The gate length (Lg) is defined using the length of the bottom of the gate trench after gate recess. With the

intersection formed by the n+ GaN regrowth by MBE and the sidewall of GaN cap, the gate to source spacing ($L_{GS}$) is the distance between the edge of source n+ regrowth and the source-side edge of foot gate, and the gate to drain spacing ($L_{GD}$) is defined as the spacing between edge of drain n+ regrowth and the source-side edge of foot gate. To minimize the series resistance in the access region, both $L_{GS}$ and $L_{GD}$ need to be scaled. The $L_{GS}$ is designed to be 75 nm with the consideration of T-gate EBL process misalignment tolerance. For Lgd, the spacing is increased to 200-300 nm to provide enough breakdown voltage for $V_{DD}$ over 40 V in W-band RF operation. So, the device source to drain spacing ($L_{SD}$) is designed to be 420 nm. Lor,s and Lor,d represent the spacing between the edge of ohmic contact metal and the edge of n+ regrown GaN on the source side and the drain side respectively, and they are needed to be included in device design to accommodate the misalignment of ohmic contact photolithography and lateral extension of the top gate on the source side. To achieve low series resistance and ensure device having no short circuit, Lor,s and Lor,d are designed to be 300 nm. Lr,slope is defined as the base of the slant side wall of the gate recess trench. For device reported in this chapter with 20 nm GaN cap, Lr,slope is around 12 nm with 60° sloped side wall. $L_{TG}$ represents the length of the base of the trapezoid-shaped top gate, which is defined by the top gate EBL process. $L_{tg}$ is designed to be 420 nm to provide low $R_G$. The length of the foot gate stem is represented by $L_{fg}$, and it is defined by the Lg plus the Lr,slope at both drain and source side. The height of top gate relative to the GaN cap surface is defined by the Al2O3/SiO2 hard mask used in gate recess, which is designed to be 225 nm with a tolerance of ±15 nm.

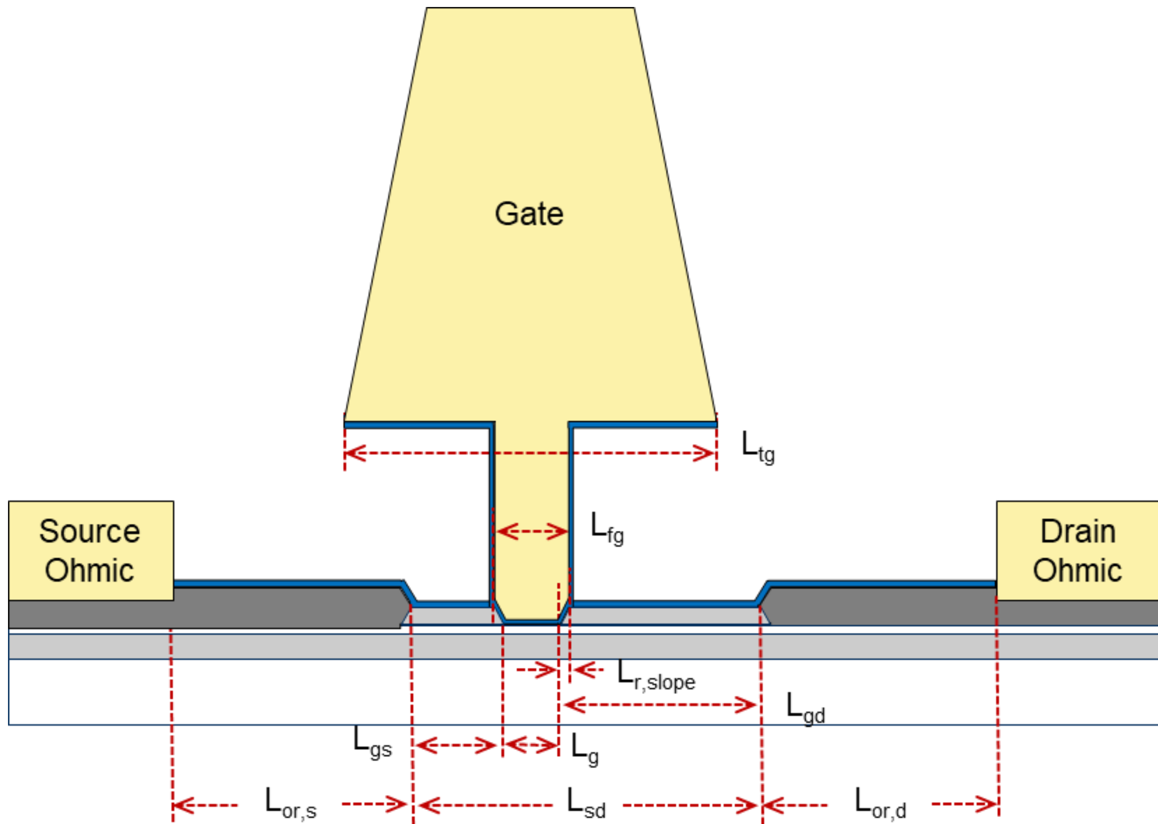



**Figure. 4.9 Definition of physical dimensions of the fabricated device (schematic is drawn to scale).**

### *4.3. Devices results before passivation*

Once the device probe pad is deposited and lifted off, the device is ready for the measurement. A series of device characterizations are performed on the device to evaluate the fabricated device from all different aspect. As SiN passivation can introduce capacitance and caused reduction of device gain, the fabricated devices are measured with DC, small signal S-parameters, pulsed I-V and W-band load pull at the stage of no extrinsic SiN passivation deposited to check device gain and efficiency.

### *4.3.1 Devices DC and breakdown results*

The DC measurement was first performed to check device performance and fabrication process. The peak extrinsic transconductance (gm) was measured to be 700 mS/mm at a $V_D$ of 3 V. The device shows a high current density ($I_D$) of 1.86 A/mm at 5 V $V_D$ and 2 V $V_G$. A low on-resistance of 0.68 Ω·mm were measured at 2 V $V_G$. The transfer and output characteristics of the fabricated device are presented in Figure. 4.10 (a-b).

The breakdown voltage was measured on a separate test device with 1 x 25 um gate width using a constant drain current injection method described in [41]. The result shows a breakdown voltage of 42 V at 1 mA/mm $I_D$, which is similar to previous N-polar GaN deep recess HEMT.

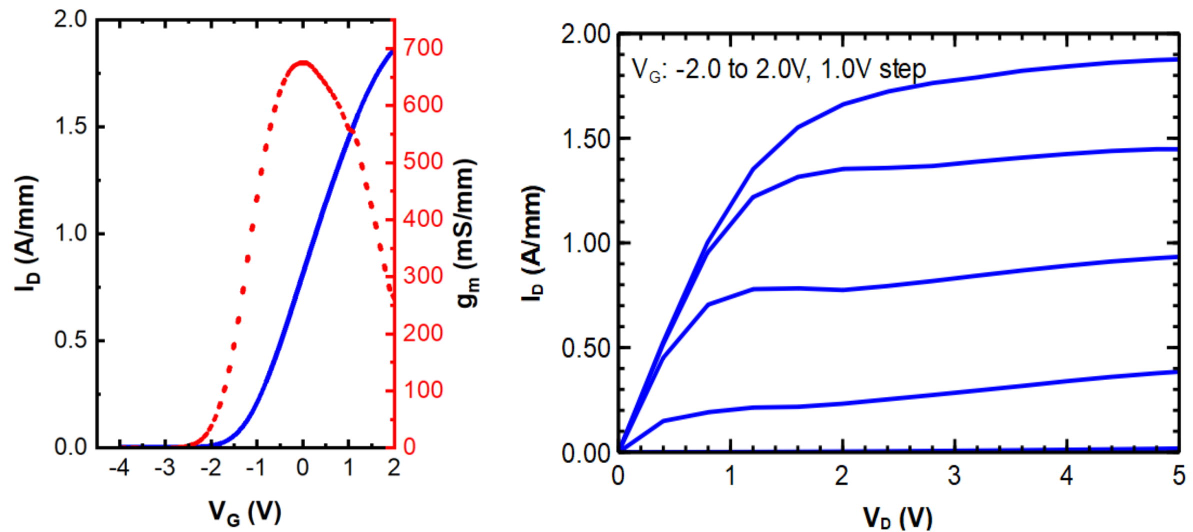



**Figure. 4.10 (a) Device transfer curve with peak extrinsic gm of 700 mS/mm at VDS of 3V. (b) Device outputs performance with $V_{GS}$ from -2 to 2V.**

### *4.3.2 Devices small signal performance*

With good DC performance demonstrated on the fabricated devices, the bias-dependent small signal S-parameters measurement were performed on the devices from 250 MHz to 67

GHz and it was calibrated using LRRM method on a separate impedance standard substrate. After de-embedding the probe pad with on-wafer open and short structures, the S-parameters measurements show that devices obtain a high peak oscillation frequency $f_{max}$ of 306 GHz with a corresponding current-gain cut-off frequency $f_T$ of 122 GHz at 10 V $V_D$, 485 mA/mm $I_D$ bias condition and a peak $f_T$ of 132 GHz with a corresponding fmax of 286 GHz (5.9 V $V_D$, 677 mA/mm $I_D$), as shown in Figure. 4.12 (a-b).

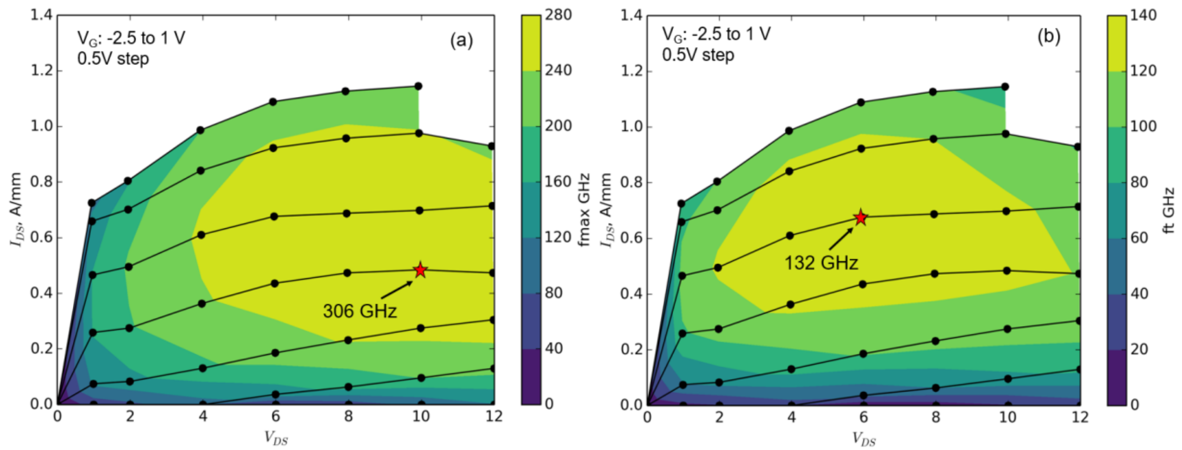



**Figure. 4.11 Devices (a) fmax and (b) fT contour plots after SiN passivation. A peak fmax of 306 GHz and a peak fT of 132GHz are measured on the N-polar GaN-on-sapphire device.**

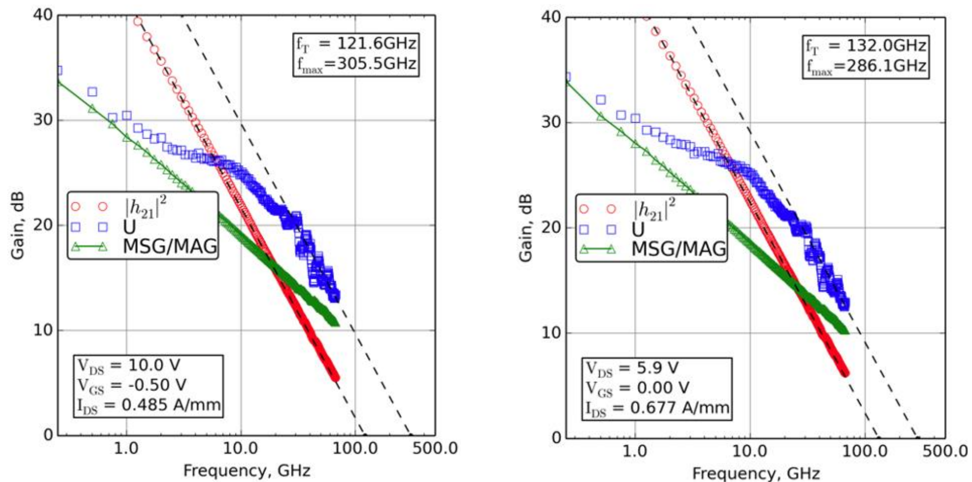



**Figure. 4.12 Small signal RF performance at (a) peak $f_{max}$ bias of $V_{DS}$ = 10 V, $V_{GS}$ = -0.5 V, and $I_{DS}$ = 485 mA/mm. (b) peak $f_T$ bias of $V_{DS}$ = 5.9 V, $V_{GS}$ = -0.5 V, and $I_{DS}$ = 677 mA/mm.**

### *4.3.3 Pulsed I-V measurement*

For the fabricated device before passivation, the effectiveness of 20 nm GaN for DC-RF dispersion control is verified by the pulsed I–V measurement. The device pulsed I–V characteristics is measured with AMCAD AM3200 PIV system. The gate pulse-width is 650 ns with 0.065% duty cycle. The device was biased in both pinch off ($V_{GS,Q}$ = −2.2 V) and semi-on ($V_{GS,Q}$ = −1.2 V) with a $V_{DS,Q}$ up to 14 V. As shown in Figure. 4.13 (a-b), the DC-RF dispersion was well controlled for both bias conditions using 20nm GaN cap layer as intrinsic passivation under the applied bias.

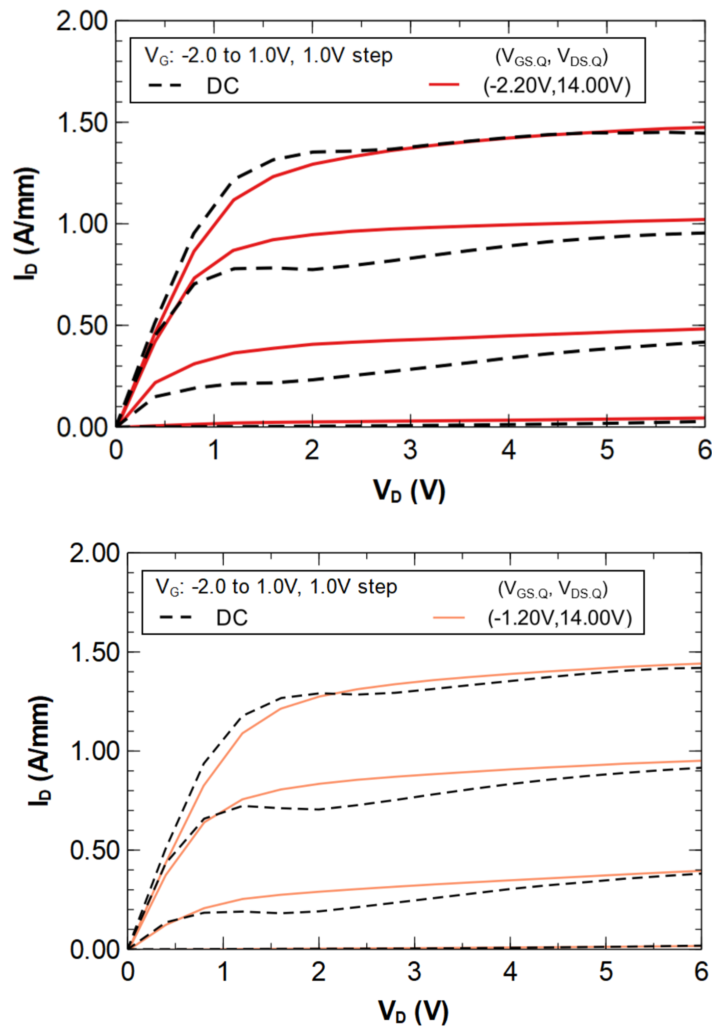



**Figure. 4.13. DC curve and pulsed I-V measurements wit 650 ns pulse width and 0.065% duty cycle under (a) $V_{GS}$ = -2.2 V, $V_{DS}$ = 14 V. (b) $V_{GS}$ = -1.2 V, $V_{DS}$ = 14 V**

### *4.3.4 Large signal performance: Load pull at 94 GHz*

To measure the devices large signal performance at W-band, continuous-wave (CW) large-signal load pull was performed on the devices at 94 GHz. The device was biased in class AB condition at 260 mA/mm quiescent drain current ($I_{DS,Q}$) to maximize PAE. The load pull power sweeps at 94 GHz for $V_{DS,Q}$ of 8 V and 12V are presented in Figure. 4.14(a-b). Figure. 4.14(a) shows that at 8 V VD, a record PAE of 44% was measured with an associated saturated output power, Po of 2.6 W/mm. Increasing the VD to 12 V, as shown in Figure. 4.14(b), a peak PAE of 42% with an associated output power density of 4.4 W/mm was measured on the device.

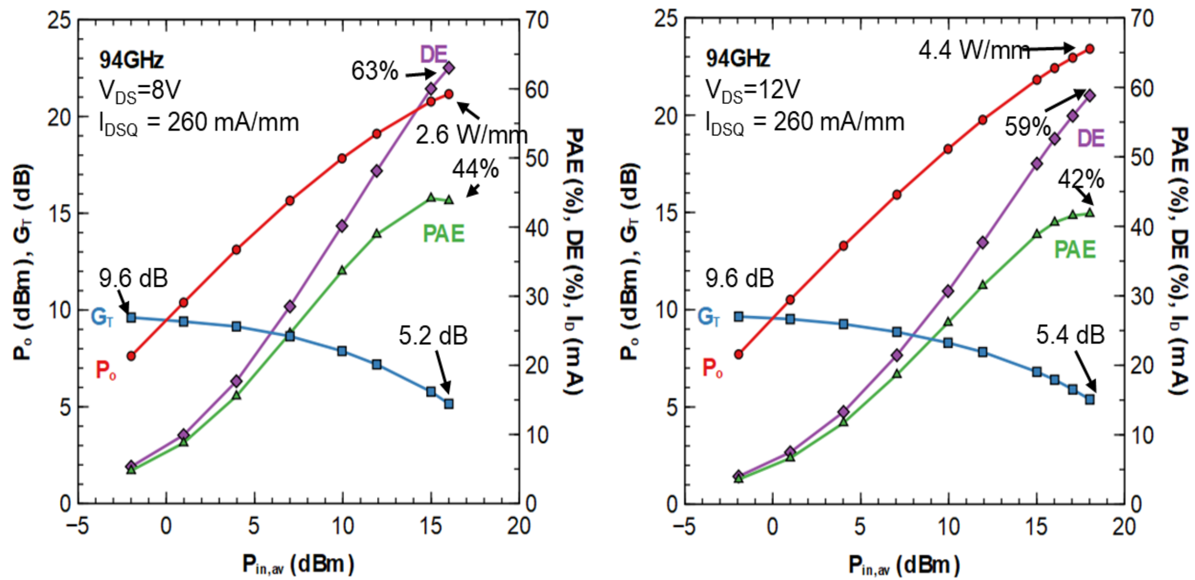



**Figure. 4.14. 94 GHz load pull power measurement at 260 mA/mm with (a) 8 V (b) 12 V, at 8 V a peak PAE of 44% was measured with associated 2.6 W/mm output power density. At 12 V the peak Po of 4.4 W/mm was measured with an associated 42% PAE.**

To validate the power and drain efficiency at saturation and understand device performance, the Cripps power amplifier analysis method [57] has been used to validate the, under the assumption of a second harmonic short at the device output. Using the knee voltage

and current of 2V $V_{knee}$ and 1.7 A/mm $I_{knee}$ for $V_{DS}$ = 12 V and $V_{GS}$ = 2V from the pulsed I-V and the quiescent current density of 260 mA/mm, the calculated drain efficiency and Po are 59% and 4.5 W/mm (Figure. 4.15). The calculated results have a great fitting with the measured data of device before passivation.

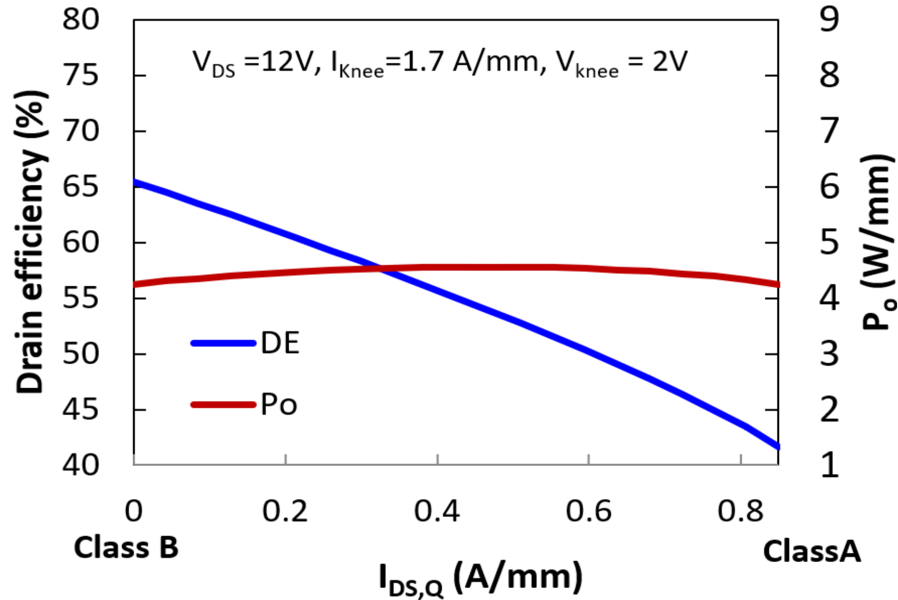



**Figure. 4.15. Calculated output power density and drain efficiency as a function of quiescent current density and class of operation using parameters from device pulsed I-V measurement.**

The benchmarking of the 94 GHz large signal results is shown in Figure. 4.16 with previous studies on N-polar GaN transistor, including GaN-on-sapphire devices and GaN-on-SiC devices along with Ga-polar devices and circuits from the literature. The fabricated N-polar GaN-on-sapphire deep recess HEMT show a great PAE improvement over previous N-polar GaN-on-sapphire [50] and GaN-on-SiC [1-4] HEMTs, as well as the Ga-polar device and MMICs, which is attributed to the high gain achieved in this device. Such high gain and high efficiency achieving on the fabricated devices validates the design and processing

improvements of the fabricated, showing the N-polar GaN deep recess HEMT being the great candidate for mm-wave RF application.

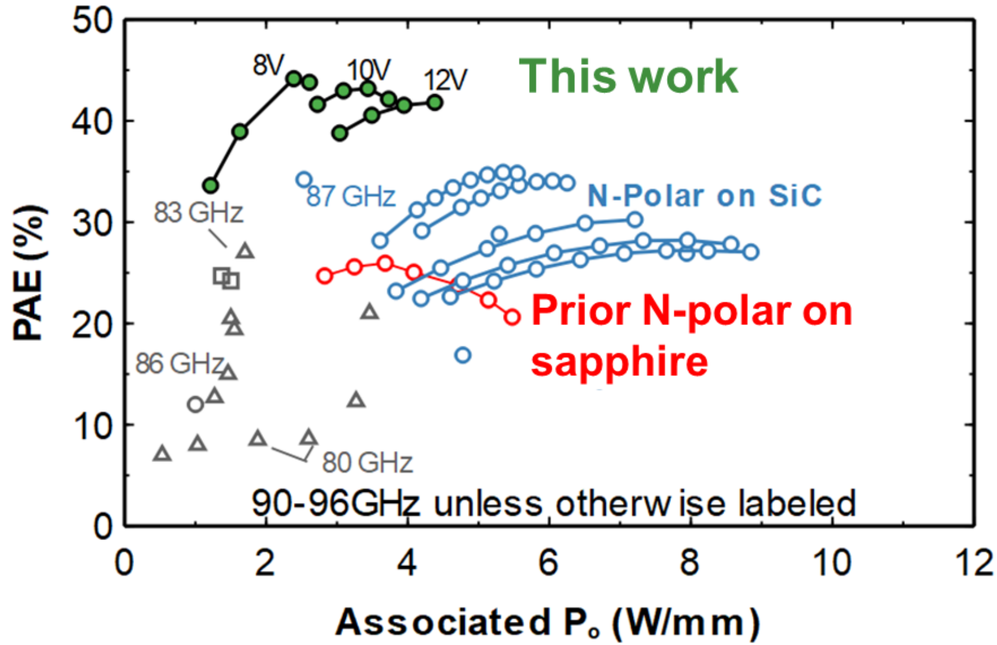



**Figure. 4.16. Benchmark plot of PAE-PO for the un-passivated device relative to prior N-polar GaN-on-sapphire and GaN-on-SiC results as well as Ga-polar devices and MMICs from literature.**

As shown in Figure. 4.17, the power density of the N-polar GaN-on-sapphire devices in this work is comparable as those observed on N-polar GaN-on-SiC for the bias range considered, showing the potential of sapphire substrate for mm-wave RF application. For the fabricated GaN-on-sapphire device, the dispersion and thermal conductivity issue are expected to have more effect on device performance with higher $V_D$ bias and high output power, so the application of thin SiN passivation might be needed to bias the device at high $V_D$ for high power with high efficiency.

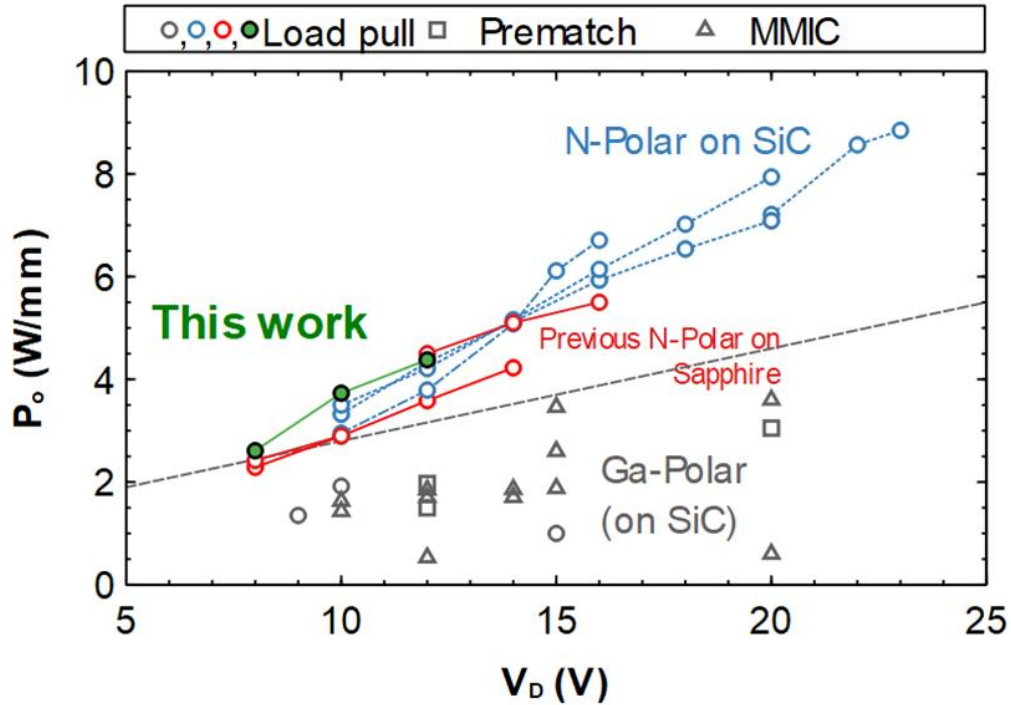



**Figure. 4.17 Comparison of W-band Po at a given $V_D$ for un-passivated deivce relative to prior N-polar GaN-on-sapphire and GaN-on-SiC results as well as Ga-polar literature. From 8 V to 12 V VD, this device shows comparable or slightly higher performance relative to previous N-polar GaN-on-SiC.**

### *4.4. Device results after passivation*

After the completion of characterization of devices prior to the passivation, a thin 20 nm PECVD SiN passivation was deposited on the sample to passivate the sample surface and enhance the dispersion control. Different from previous 40 nm PECVD SiN passivation [1], [3-4] 20 nm was used for the fabricated device to minimize the impact on fringe capacitance.

#### *4.4.1. Device small signal performance after passivation*

Small signal measurements were performed on the passivated devices to check effect on device gain from passivation. bias-dependent S-parameters were measured up to 67 GHz with LRRM calibration at the probe tips and an impedance standard substrate. After de-embedding

the effects of the probe pads from the measured S-parameters using on-wafer open and short structures, the devices demonstrated a peak oscillation frequency $f_{max}$ value of 291 GHz with a corresponding current-gain cut-off frequency $f_T$ value of 109 GHz ($V_D$=10 V, $I_D$=647 mA/mm) and a peak $f_T$ of 115 GHz with a corresponding $f_{max}$ of 269 GHz ($V_D$ =6 V, $I_D$=565 mA/mm) as shown in Figure. 4.19 (a-b).

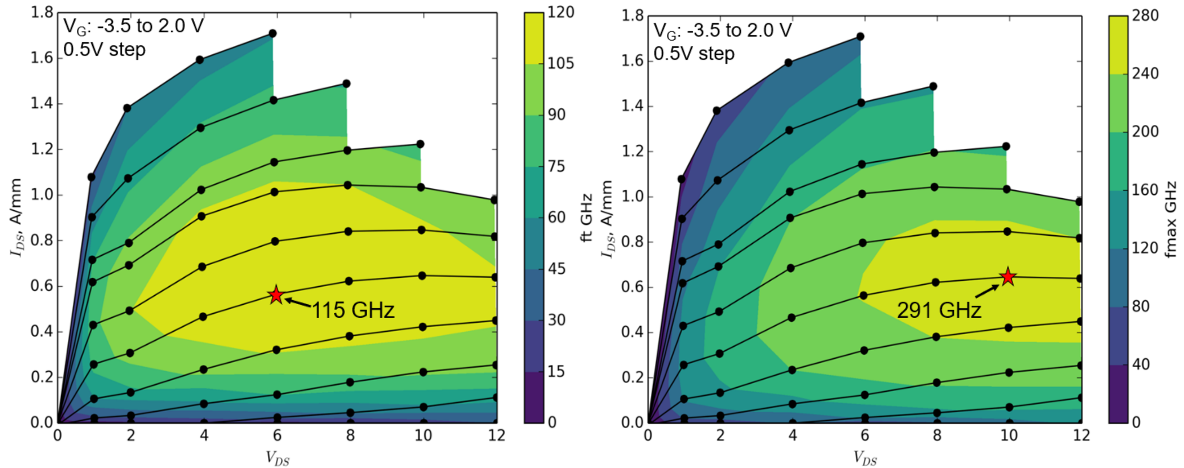



**Figure. 4.18 Device (a) $f_T$ and (b) $f_{max}$ contour plots after SiN passivation. A peak $f_T$ of 116 GHz and a peak $f_{max}$ of 291 GHz are demonstrated on the N-polar GaN-on-sapphire device.**

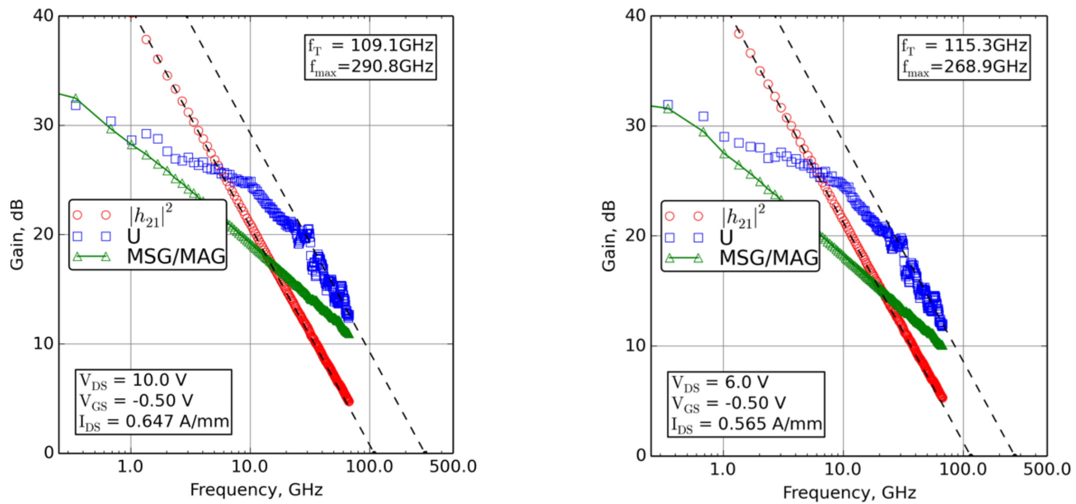



**Figure. 4.19. Small signal performance at (a) peak $f_{MAX}$ bias of $V_D$ = 10 V, $V_{GS}$ = -0.5 V, and $I_{DS}$ = 647 mA/mm. (b) peak $f_T$ bias of $V_D$ = 6V, $V_{GS}$ = -0.5V, and $I_{DS}$ = 565mA/mm**

### *4.4.2. Pulsed IV results after passivation*

Before SiN passivation, the fabricated device obtain good dispersion control as described in Section 4.3.3 with bias condition in both pinch off ($V_{GS,Q}$ = −2.2 V) and semi-on ($V_{GS,Q}$ = −1.2 V) with a $V_{DS,Q}$ up to 14 V. however, when biased in to deeper pinch off ($V_{GS,Q}$ = −3.5 V), the dispersion shows up and starts to affect device current with bias at drain. The Figure 4.20 (a) shows the current collapse caused by dispersion for device before passivation.

Pulsed I–V measurements (with a 650 ns pulse width and 0.065% duty cycle) of device with biasing in deep pinch off ($V_{GS,Q}$ = −3.5 V) and a $V_{DS,Q}$ up to 12 V is presented in Figure 4.20 (b). compared with device before passivation, the DC-RF dispersion control is greatly improved with small increase in the knee voltage.

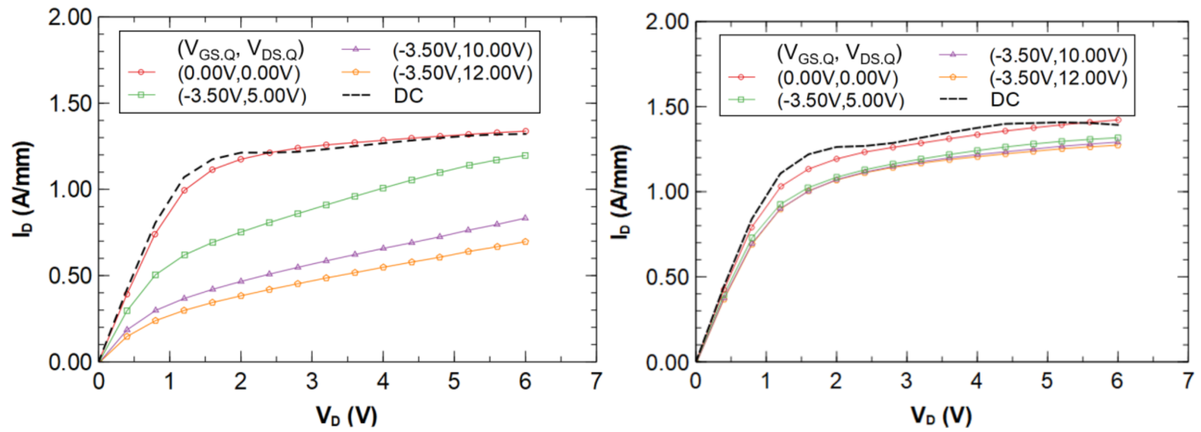



**Figure. 4.20 Comparison of pulsed I-V characteristics for device (a) before SiN passivation and (b) after SiN passivation, showing improved dispersion control with a 10% reduction in $I_D$ at the knee (1 V $V_G$, 2 .5V $V_D$) under 12 V $V_{DS.Q}$ after passivation**

### *4.3.6 Large signal performance after passivation*

94-GHz continuous-wave (CW) large-signal load pull was performed to evaluate the passivated device large signal performance at W-Band. The device was biased in class AB condition at a quiescent drain current ($I_{DS,Q}$) of 260 mA/mm to maximize PAE. The load-pull

power sweeps at 94 GHz for $V_{DS,Q}$ 12 V and 14V are presented in Figure. 4.21(a-b). Figure. 4.21(a) shows that at 12V $V_D$, the peak PAE was 40.2% with an associated output power, $P_o$ of 4.85 W/mm. Increasing the $V_D$ to 14 V, as shown in Figure. 4.21(b), a peak PAE of 38.5% with an associated output power density of 5.83 W/mm is achieved at this bias. A maximum total output power of 24.6 dBm (291mW) is achieved on this N-polar GaN-on-sapphire deep recess device. Both source and load impedance were limited by the available tuning range of the passive load-pull system.

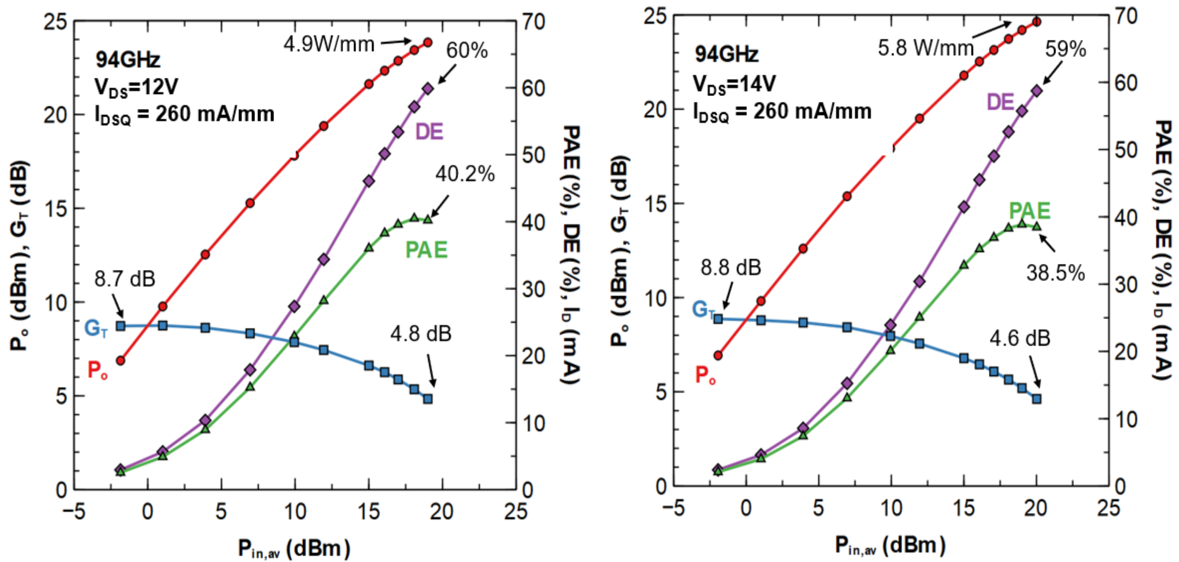



**Figure. 4.21 94GHz load pull power sweep at (a) 12V with 260 mA/mm $I_{DS,Q}$ demonstrating >40% PAE and 4.85W/mm associated Pout and at (b) 4V with 260 mA/mm $I_{DS,Q}$ demonstrating 5.83 W/mm Pout with associated 38.5% PAE.**

The benchmark plots about 94 GHz large signal results for the reported devices before and after passivation are summarized in Figure. 4.22 with previous works on N-polar GaN devices and Ga-polar devices and MMICs from the literature. Before extrinsic passivation, devices obtain over 9.6 dB linear gain and passivated device still demonstrate linear gain over 8.8 dB.

The improved device gain shows the effectiveness of optimization s in device design, epitaxy growth and fabrication process. Furthermore, this device also achieved very high output power density while using sapphire as the substrate. suggesting the performance of the device is still limited by gain instead of thermal conductivity of the substrate. This statement is corroborated in Figure. 23 where that the performance of the reported N-polar GaN-on-sapphire device is comparable to those observed on N-polar GaN-on-SiC for the bias range considered. With improved thermal management such as SiC substrates [1-4] and diamond heat sinks on devices [58], the N-polar GaN deep recess device performance is expected to be improved even further.

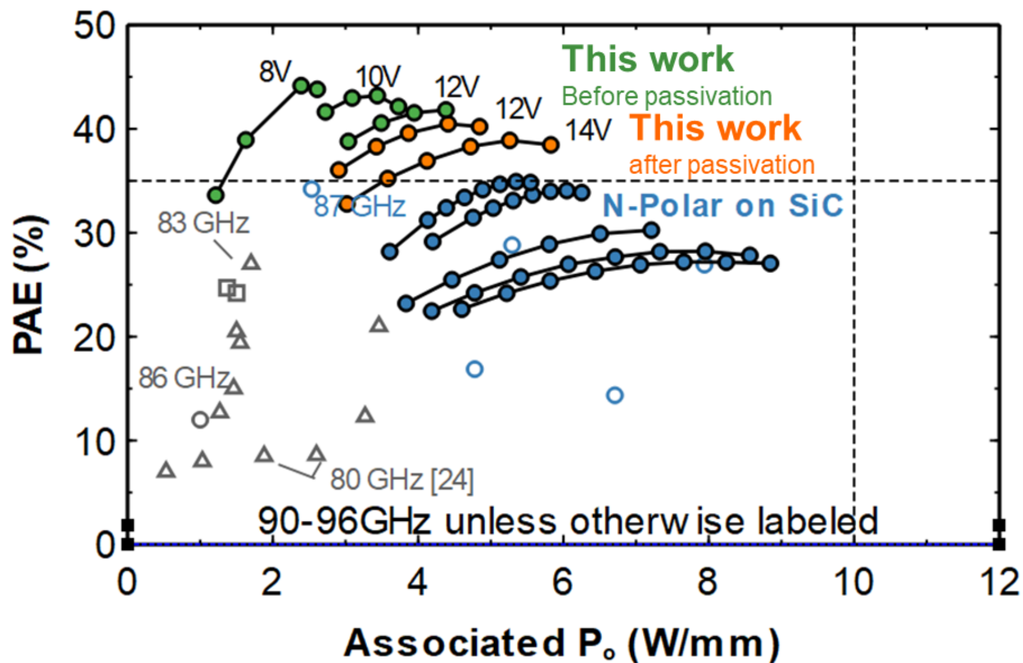



**Figure. 4.22 Benchmarking PAE-Pout of fabricated devices prior and after SiN passivation with prior N-polar GaN devices and Ga-polar device and circuit from literature**

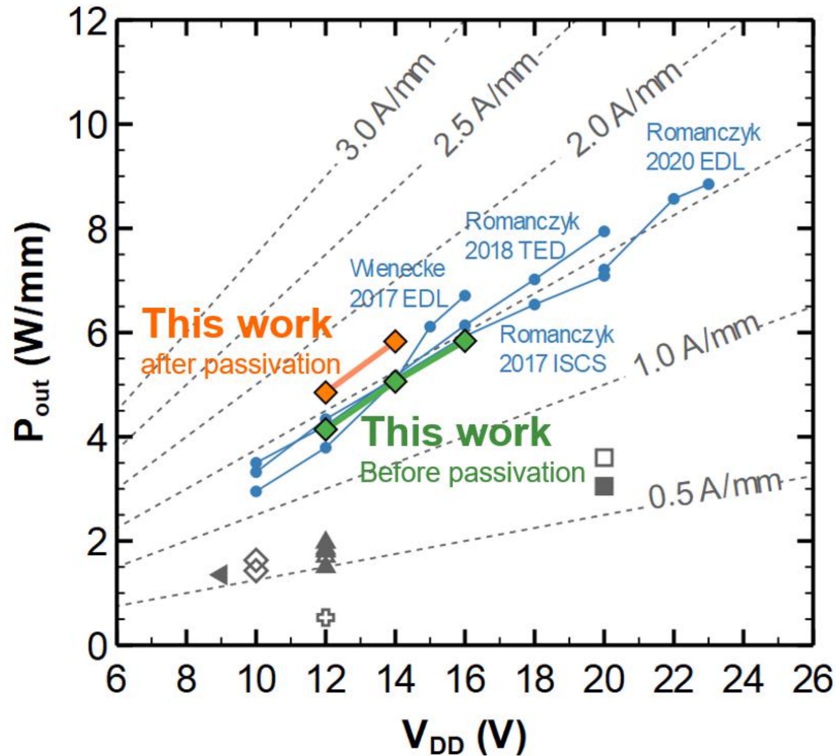



**Figure. 4.23 Summary of W-band Pout-$V_D$ of devices prior and after SiN passivation with previous N-polar GaN-on-SiC works as well as Ga-polar device results from literature. Compared with un-passivated devices, the passivated devices obtain higher power at same drain bias, indicating improved dispersion. control**

Compared with device without extrinsic SiN passivation, the device after SiN passivation shows around 0.8 dB loss of linear gain at 94 GHz, which is attributed to the introduction of fringing capacitance. The impact on gain from 20 nm SiN might be enlarged because of the highly scaled device structure with narrow spacing between gate and source. The SiN filling of the narrow trench in between T-gate and source can cause more reduction on device gain than pervious device [50]. This results also indicate extrinsic passivation might not be needed for device operation with quiescent bias $V_D$ less than 12 V and the 20 nm GaN cap layer can provided enough dispersion control. Although the pulsed I-V suggests dispersion presents when stressed at deep pinch off ($V_G$ = -3.5V), the 94 GHz large signal performance shows RF

current collapse of the un-passivated device is small. However, the 20 nm SiN passivation helps device achieving high power with high efficiency at high $V_D$ bias (>12 V), and high power density of 5.8 W/mm with associated 38.5% PAE is achieved on the passivated device. Compared with device before passivation, the passivation device shows higher RF current at same $V_D$ bias, suggesting the enhanced dispersion control at high $V_D$ with SiN passivation and 20 nm GaN cap. The drop of efficiency with higher quiescent $V_D$ bias is still under investigation. The possible reasons are a. the possible current collapse with high $V_D$. b. The thermal effect with sapphire substrate might start to limit the device performance at high $V_D$ with high output power. Such excellent performance with over 5.8 W/mm power density achieved on GaN-on-sapphire devices is encouraging and it suggests that the device gain which in turn enhances efficiency, is a major tool to achieve exceptionally high performance from GaN-based RF transistor on a less thermally conductive (than SiC) substrate.

### *4.5. Summary*

This chapter discussed about the development of N-polar GaN-on-sapphire deep recess HEMT showing over 9.6 dB linear gain and record efficiency performance at W-band. To increase the device gain, a 20 nm GaN cap layer, 10 nm GaN channel and ALD Ru gate metallization have been implemented with the high channel mobility provided by commercial N-polar GaN-on-sapphire epi. With optimized epitaxy design and device fabrication, record power performance of GaN HEMTs at 94 GHz has been demonstrated with N-polar GaN-on-sapphire deep recess HEMT. Prior to extrinsic SiN passivation, over 40% PAE with high output power density at 94 GHz has been demonstrated with the fabricated N-polar GaN-on-sapphire deep recess devices. Due to the excellent 9.65 dB linear gain at 94 GHz at low 260 mA/mm current density bias, the reported N-polar GaN-on-sapphire HEMTs show very high

PAE of 42% with associated 4.4 W/mm output power density at 94 GHz. The highest PAE measured on the device is 44% with 2.6 W/mm associated output power density. After 20nm SiN passivation, device still obtain an excellent 8.8 dB linear gain at 94 GHz, the fabricated N-polar GaN-on-sapphire HEMTs show very high output power density of 5.8 W/mm with a record 38.5% PAE at 94 GHz. This result validates the design and improvement in epitaxy and device fabrication and provide guidance for future device design, suggesting the gain being one of the target metrics for GaN RF device at mm-wave and the great potential of sapphire for mm-wave GaN power amplifier application as low-cost substrate

## V. Strain engineering on GaN

As one of the biggest semiconductor industry success, Si CMOS has implemented several innovative techniques to solve challenges in device scaling and accomplished great results. To solve device gain challenges in GaN HEMT and further improve the GaN RF HEMT for mm-wave or even higher frequency, innovative techniques applied on Si industry are also worthwhile to investigate in GaN HEMT. Mechanical stress to strain a semiconductor lattice is a well-known effect and has been applied in CMOS industry and achieved great success. With few efforts having been made to apply strain engineering in GaN [59-60], the effective mass reduction and electron velocity improvement expected from strain engineering can really be helpful to improve device RF performance.

For a well-designed GaN transistor with reduced parasitics, the transit time $\tau$ in the channel under the gate is given by:

$$\frac{1}{\tau} = f_T = \frac{v_e}{2\pi Lg} \tag{5.1}$$

Where the $f_T$ is current cut-off frequency and $v_e$ is the average electron velocity in the channel and Lg is the gate length of the transistor. An increase in velocity can be extremely beneficial for the $f_T$ and gain. Electron velocity in GaN ($2 \times 10^7$ cm/s) is limited by its high electron effective mass (0.2me), which is larger than that of InGaAs on InP (0.047me), and the strong optical phonon scattering as discussed in chapter 2.

To increase the electron velocity in channel, a reduction of effective mass with strain engineering has been known for semiconductor and have been implemented in many materials and device, but only a few explorations has been done on GaN HEMT for electrical property. This chapter will discuss investigation in strain engineering in GaN for velocity enhancement with narrower bandgap material of relaxed InGaN and strained GaN.

The approaches to achieve velocity enhancement is what called effective mass engineering, As showed in Figure 5.1, the biaxial tensile strain changes the band structure of GaN and increase the curvature of conduction band, which reduce the effective mass of GaN.

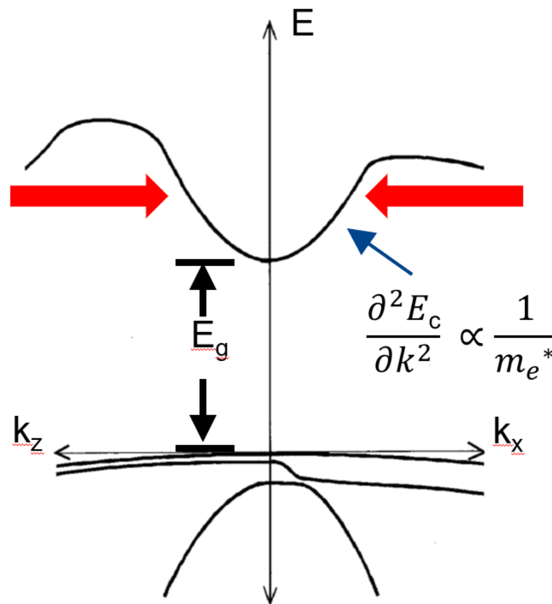



**Figure. 5.1 Band structure of GaN under effect of effective mass engineering**

To realize the effective mass engineering, two choices are available and discussed in this chapter: Using InGaN as channel material and applying biaxial tensile strain to GaN. This chapter presents investigation both on them Section 5.1 discuss the implement of relaxed InGaN into GaN HEMT with the first demonstration of Ga-polar GaN/InGaN HEMT utilizing relaxed InGaN channel. The study on strained GaN for reduced effective mass and velocity improvement is given in section 5.2. A summary of strain engineering on GaN is presented in section 5.3.

### *5.1. Relaxed InGaN*

As a narrower band gap material compared with GaN, InGaN offers a lower effective mass and a higher peak drift velocity [61-62]. Electron mobility more than 3500 $cm^2V^{-1}s^{-1}$ were measured for InN films with an electron carrier density of 1.5 x $10^{17}$ $cm^{-3}$, while mobility of around 600 $cm^2V^{-1}s^{-1}$ were measured in GaN with similar carrier density [63]. The 2DEG mobility in an $In_{0.2}Ga_{0.8}N$ channel was calculated to be more than 5000 $cm^2V^{-1}s^{-1}$ without considering the alloy scattering [64].

InGaN has been previously explored as a HEMT channel material [65-69]. However, relaxation of the InGaN channel is required since a fully strained InGaN channel does not provide an effective mass commensurate with the In mole fraction because the lattice constant and hence the Brillouin Zone and conduction band curvature of the InGaN is more akin to GaN, as previously observed for strained and relaxed InGaAs [70]. By relaxing the InGaN in the direction of electron transport the electron effective mass is determined by the relaxed lattice constant. Using porous GaN assisted elastic relaxation is an efficient approach for achieving relaxed $In_{0.25}Ga_{0.75}N$ channel device as it ensures no new defect or dislocation formation. As shown in Figure.5.2(a-b), theoretical calculations using Vegard's law predict a reduction in effective mass of electrons in the channel by 30%, which offers a 20% boost in electron velocity [71]. InGaN relaxation has been realized using porous GaN for photonics device previously [72-75]. In this section, porous GaN using electrical chemical (EC) etch is implemented in electronics device for the first demonstration of relaxed InGaN channel.

Experiments on HEMT relaxed InGaN channel was designed and are chosen to be conducted with Ga-polar GaN HEMT epi to explore the effective mass engineering with relaxed InGaN. As depicted in Figure 5.3. The structure was grown on sapphire by MOCVD

and consists of, from the bottom up, an UID GaN buffer followed by 600 nm Si-doped GaN with a doping of (4–5)×$10^{18}$ cm−3, 35 nm $In_{0.1}Ga_{0.9}N$ and 4 periods InGaN/GaN layer stack (30 nm $In_{0.1}Ga_{0.9}N$ /3.5 nm GaN), in which the 3.5 nm GaN acts as protection of the InGaN layers during growth to smooth the surface [76]. After that, a 40 nm $In_{0.1}Ga_{0.9}N$ channel and a 30 nm GaN barrier was grown on top of InGaN/GaN layer stack. The GaN:Si layer underneath the (In,Ga)N layer stack will be porosified to relax the (In,Ga)N layer stack. The as grown $In_{0.1}Ga_{0.9}N$ /GaN layer stack was observed to be fully strained to the GaN buffer, using high resolution x-ray diffraction (HR-XRD) (ω–2θ)–ω reciprocal space maps (RSMs).

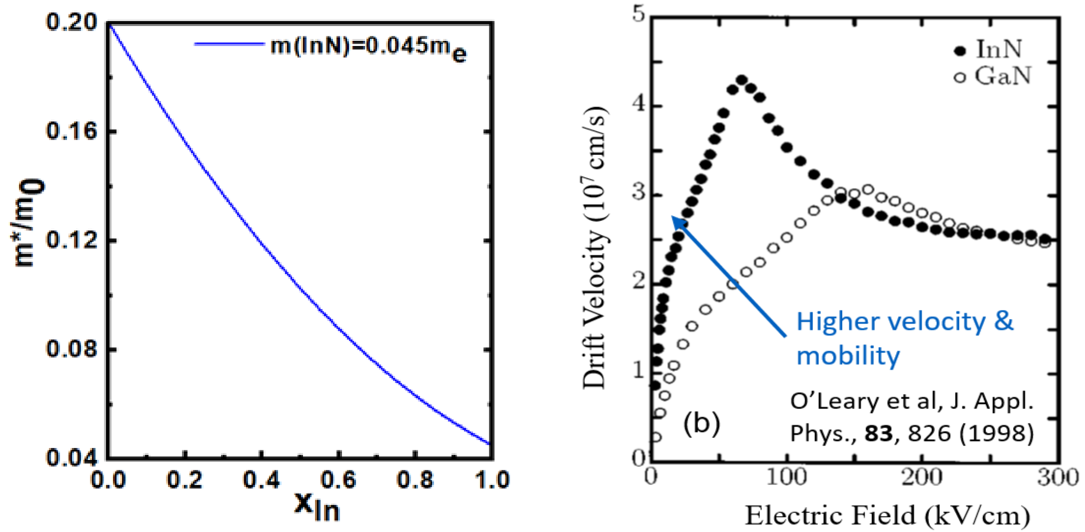



**Figure. 5.2 (a)Calculated bandgap and effective mass versus In composition for relaxed InGaN channels. (b) The velocity-field characteristics of InN and GaN**

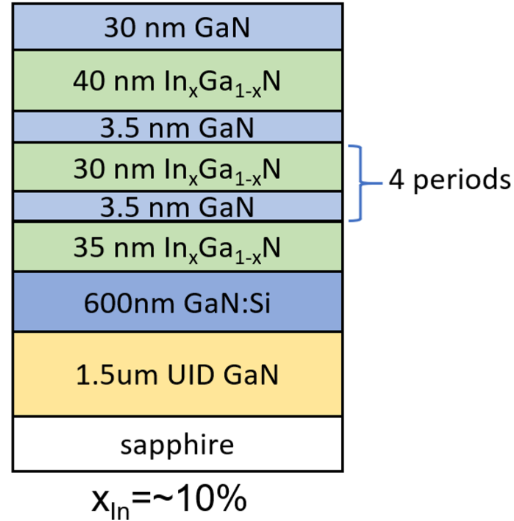
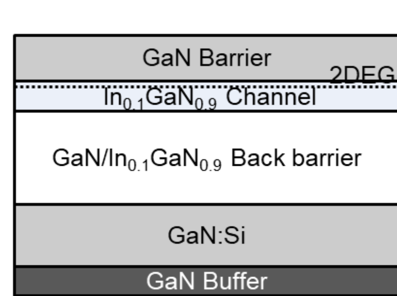
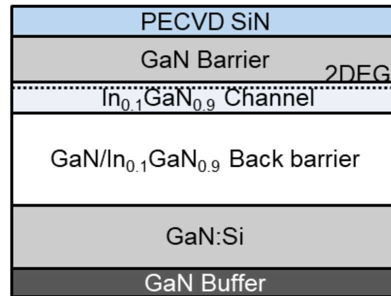



**Figure. 5.3 Schematic of the epitaxial structure used for relaxed InGaN channel HEMT**

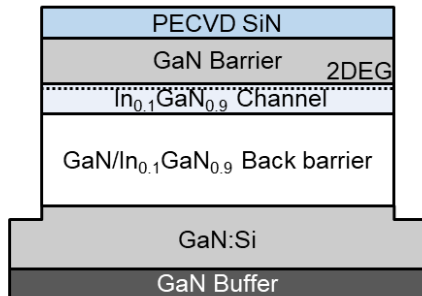
To start the strain relaxation process, the definition of the desired fin-type pattern was achieved using lithography followed in turn by a 100 W BCl3/Cl2 reactive ion etch (RIE) high power etch down into the UID GaN, exposing the n+ GaN along the sides of the fins for the selective EC etch as shown in Figure 5.4. Next, a doping selective EC etch was performed to make the n+ GaN porous, as described in [77]. A part of each die was protected from the EC etch so that the underlying n+ GaN remained non-porous and the InGaN channel remained strained to the GaN in these regions. This allowed for a direct comparison between the strained and the relaxed InGaN channels within the same dis on the wafer.



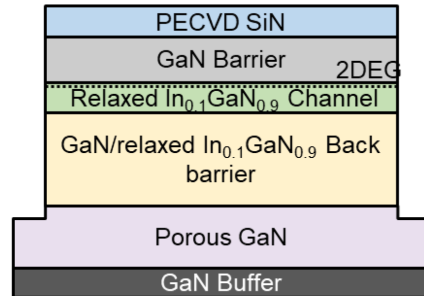

1. Epi structure



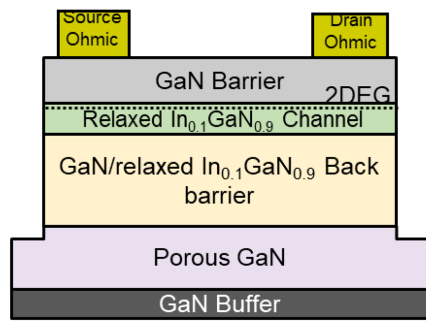

2. Protection layer deposit



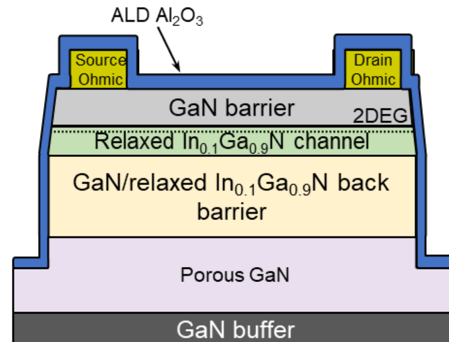

3. Fin etch (expose GaN:Si side wall)



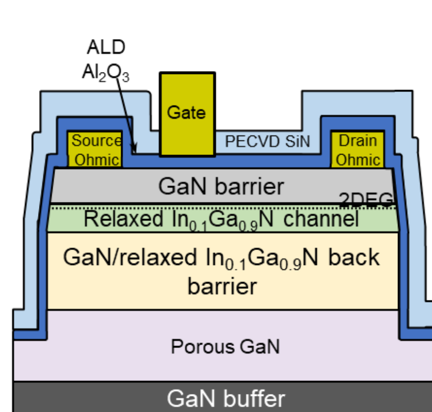

4. Selective electrical chemical etch



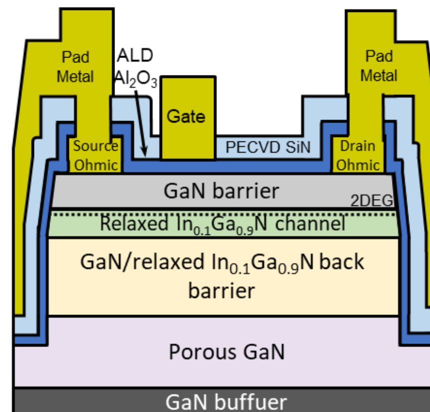

5. SiN removal & Ohmic metal deposition




6. Ohmic anneal and gate dielectric deposition




7. Gate deposition and passivation




8. Bond pad etch and Probe pad deposition

**Figure. 5.4 Process flow of the relaxed InGaN channel HEMT**

After the strain-relaxation process, an electron beam evaporated 20/100/10/50 nm of Ti/Al/Ni/Au metal stack was deposited as source/drain ohmic contact, followed by an annealing step at 800 C in a $N_2$ ambient for 30 s. The mesa isolation was completed by another 100 W BCl3/Cl2 RIE etch to remove Si-doped GaN left between devices. Afterwards, 12 nm of Al2O3 was deposited as the gate dielectric by ALD, and the gate was metalized with 30/500 nm Ti/Au deposition and liftoff. The device was then passivated with 200 nm plasma PECVD SiN, followed by a CF4/O2 inductively coupled plasma (ICP) dry etch of the SiN and 50 W BCl3 etch of the Al2O3 in RIE to open the via window for the probe pad. A 30/500 nm Ti/Au stack defined by evaporation and lift-off was used for the probe pad. With this process, devices can be fabricated at the relaxed and strained InGaN region simultaneously in the same die to enable a direct comparison.

An optical microscope image of the sample's top view, after applying the strain-relaxation process, is shown in Figure 5.5(a). The visual difference between the relaxed InGaN channel region and the strained InGaN channel can be clearly observed, and this can be attributed to the GaN porosity, and the refractive index change with the porous GaN buffer. A tilted SEM image of the sample in Figure 5.5 (b) shows the underlying porous GaN layer with the material above well-protected, because of the material doping selectivity of EC. To confirm the InGaN relaxation, x-ray diffraction (XRD) (ω–2θ)– ω (RSMs) were recorded around the GaN (1¯ 124) diffraction plane on the same wafer with high density fins defined in order to analyze strain state in the direction perpendicular to the the fins. Figure 5.6 shows that the strain relaxation of the InGaN layer stack was 70% relaxed in the direction perpendicular to the fins, which corresponds to the lattice constant of a fully relaxed In0.07Ga0.93N film.

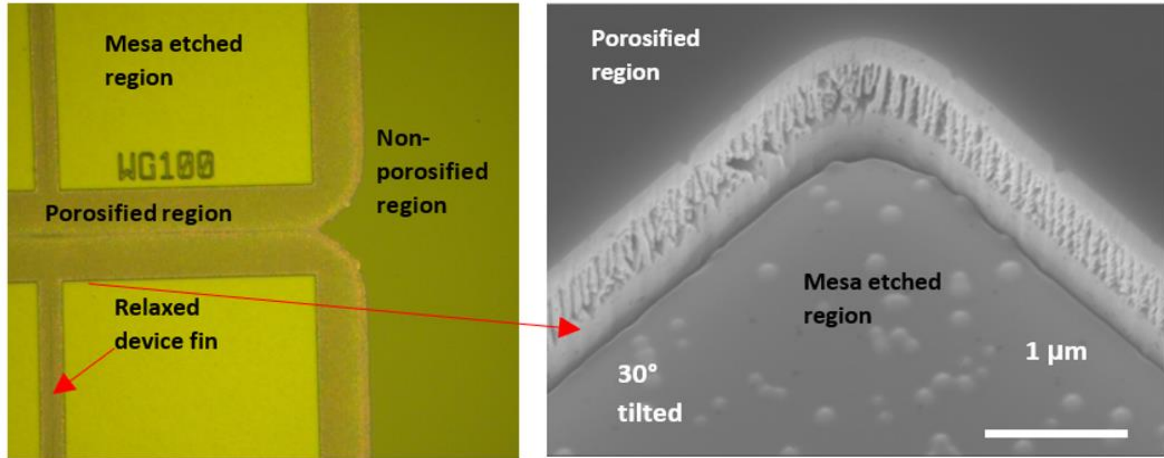



**Figure. 5.5 Top-view microscope image of sample after going through the selective EC etch (b) SEM image of the sample after selective EC etch showing that the Si-doped GaN became porous**

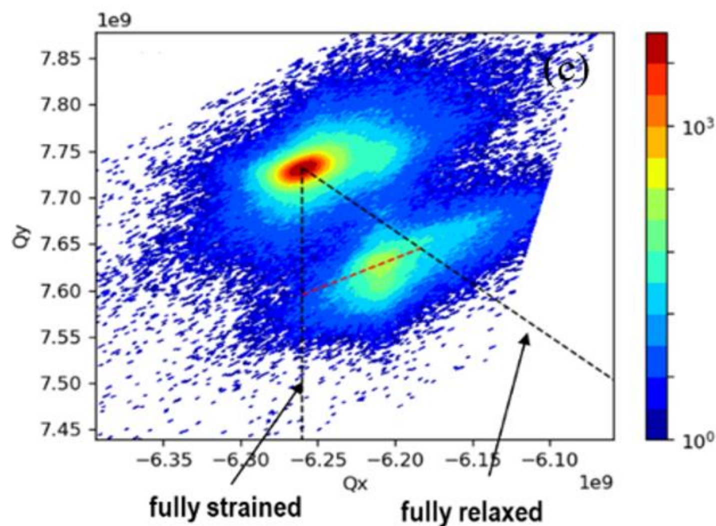



**Figure. 5.6 (ω–2θ)–ω RSM along the GaN ($\bar{1}\bar{1}$24) reflection after patterning of the fin structure and the selective EC etch demonstrating 70% InGaN relaxation perpendicular to the fins.**

The electron mobility in the channel was extracted for both the relaxed and strained InGaN channels using a combination of C–V and gated TLM measurements. For the strained InGaN channel at $V_G = 0$ V, the sheet resistance of 4760 Ω/sqr was measured and ns was $4.76 \times 10^{12}$

$cm^{-2}$ from the C–V measurement, giving a mobility value of 270 $cm^2V^{-1}s^{-1}$. For the relaxed InGaN channel, with the measured sheet resistance of 4600 Ω/sqr at VG = 0 V, the relaxed InGaN channel has a mobility of 296 $cm^2V^{-1}s^{-1}$. As shown in Figure 5.7, this is a 9.6% increase over the strained channel, and it is attributed to a reduced effective mass, and it fits the theoretical expectation based on Vegard's law. However, both relaxed InGaN and strained InGaN channel have high Rsh over 4500 Ω/sqr and mobility lower than 400 $cm^2\ V^{-1}\ s^{-1}$, this is because the severe alloy scattering is introduced by adding In into GaN, big difference in band gap of GaN and InN cause the non-uniformity of Indium composition and strong alloy scattering for carrier transport in InGaN channel.

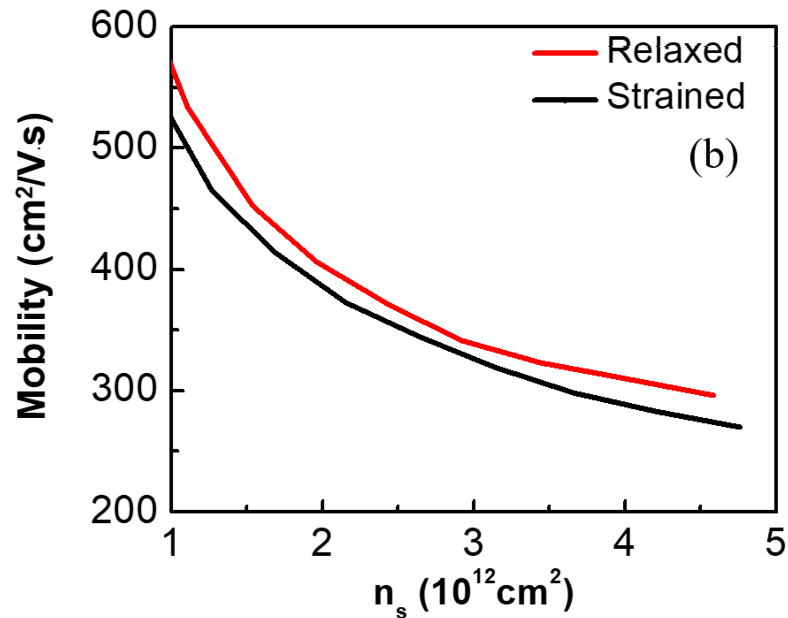



**Figure. 5.7 Extracted mobility of the relaxed and the strained InGaN channel with different charge density.**

To validate the electron mobility improvement from InGaN relaxation in transistor, the HEMT DC output IV characteristics of two representative devices were measured. The device structure for relaxed InGaN channel device and strained InGaN channel device are presented

in Figure 5.8. The results obtained for devices with 50 µm gate width, $L_{GS}$ of 700 nm, $L_{GD}$ of 700 nm. With the gate length of 1 µm, both devices with strained and relaxed InGaN channel are plotted in Figures 5.9(a-b), showing a drain current density of 350 mA mm−1 at Vg = 0 V and $V_{DS}$ = 5 V, and 9.7 Ω mm on-resistance for the relaxed InGaN channel device. The strained InGaN channel device shows an $I_{DS}$ of 330 mA mm−1 at Vg = 0 V and Vds = 5 V, and a 10.8 Ω mm on-resistance ($R_{ON}$) for the device with respectively. These results show a ~10% improvement of $R_{ON}$ for relaxed InGaN channel over the strained InGaN channel with similar saturation current, showing similar enhancement in device transport as what observed in TLM measurement. With the TLM and transistor results, the InGaN relaxation is believed to lower the effective mass and improve the electron transport in the InGaN channel. It is expected that further improvement in mobility and velocity can be achieved by high In composition InGaN with relaxation, while high In composition InGaN-on-GaN growth is challenging with some explorations done by MOCVD [78] and MBE [79], showing 20% In composition InGaN grown on GaN.

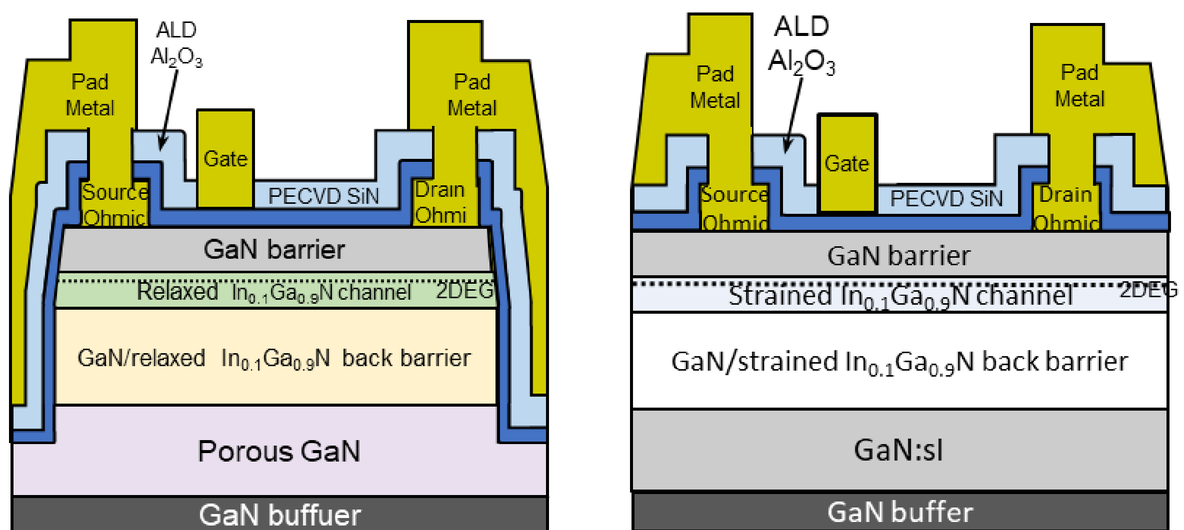



**Figure. 5.8 Schematic of GaN/InGaN HEMTs (a) with a relaxed InGaN channel. (b) with a strained InGaN channel.**

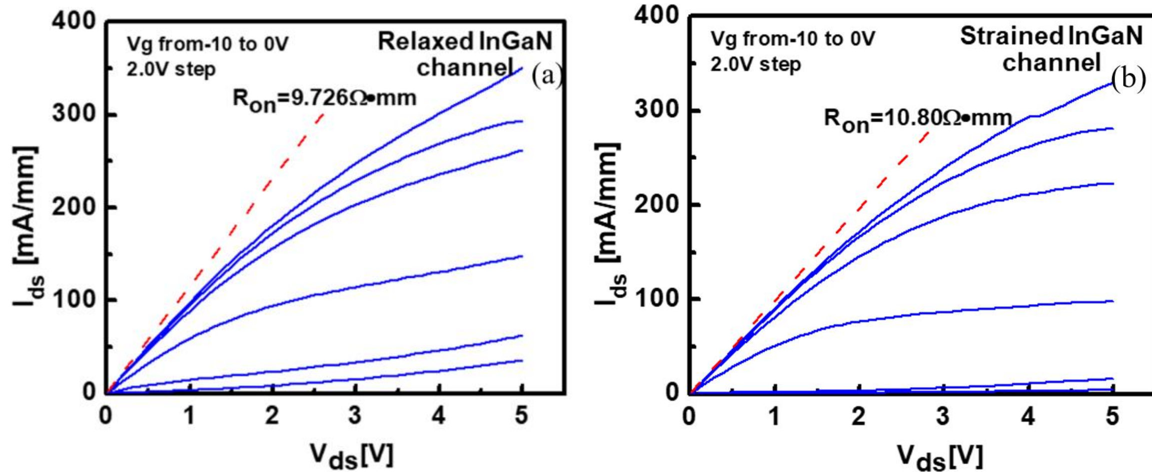



**Figure. 5.9 DC Ids-Vds output characteristics of devices with (a) the relaxed InGaN channel and (b) the strained InGaN channel.**

In summary, the first GaN/InGaN HEMT with a relaxed InGaN channel was fabricated using a porous GaN structure. The porous GaN buffer underlayer enabled the InGaN layer to elastically relax to obtain a reduced effective mass compared to a strained InGaN channel. Based on a direct comparison with a strained InGaN channel in the same die, the relaxed InGaN channel showed a ~9.6% improvement in electron mobility, which is consistent with the theoretical expectations based on a reduced effective mass. The device characteristics result also show 10% improvement of on-resistance with the relaxed InGaN channel comparing with the strained InGaN channel. Currently the improvement of relaxed InGaN is still limited by the In composition incorporated in MOCVD growth and relaxation process. However, the mobility of relaxed InGaN channel is strongly affected by the alloy scattering. These results demonstrated the feasible of effective mass engineering using relaxed InGaN and it is expected to lead to improvements in the $f_T$ of power RF GaN devices for mm-wave and THz applications if better control of alloy scattering can be achieved.

### *5.2. Strained GaN*

As shown in the section 5.1, the strong alloy scattering in InGaN severely reduced the mobility in the channel and remove the advantages from lower effective mass. In contrast to relaxed InGaN [80], low effective mass can be achieved with only applying strain in GaN with shrinking the Brillouin zone and has no sacrificing on the mobility. In this section, we examine the influence of biaxial tensile strain in GaN on electron effective mass and electron velocity and check the effects on GaN RF HEMT performance.

Effect on electron effective mass from strain in GaN was previously investigated in [81]. This chapter extents the discussion on biaxial strain in [81] and focus on biaxial global tensile strain generated by epitaxy of GaN on relaxed InGaN buffer because of the feasibility and reduction on effective mass.

To check the band structure of GaN under strain, Density function theory (DFT) first principal calculation with the VASP codes was performed. The Perdew--Burke-Ernzerhof (PBE) and the projector augmented wave (PAW) potentials were adopted with hybrid functional of Heyd, Scuseria, and Ernzerhof (HSE) used as the exchange-correlation functional. A mesh of $6\times6\times4$ $\Gamma$-centered k-point of the Brillouin zone, an energy cutoff of 600 eV for plane-wave basis set and a mixing parameter of 28% (used for HSE calculation) are used in this work. The GaN band structure was first calculated and plotted in Figure 5.10, showing a bandgap of 3.4 eV.

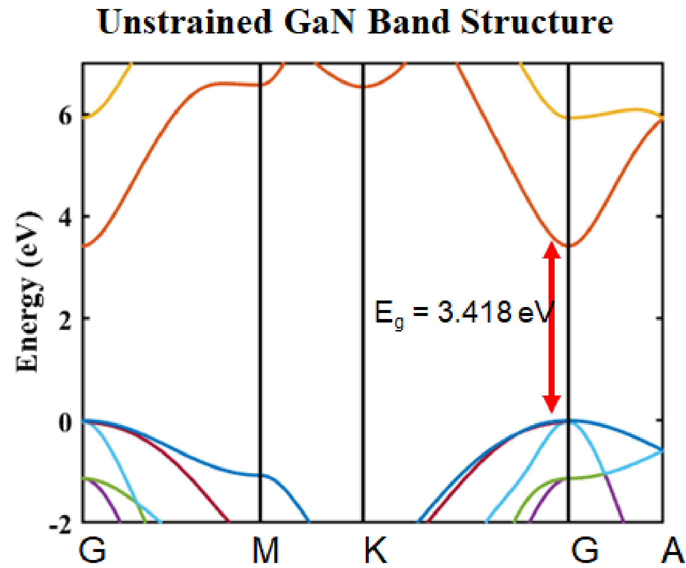



**Figure. 5.10 Calculated band structure of GaN with no strain**

For biaxial tensile strain calculations, macroscopic theory of elasticity was used for calculating the ratio of $\epsilon zz$ and $\epsilon xx$ ($\epsilon yy$) under in-plane biaxial tensile stress and the relation between strains is $\epsilon_{zz} = -2(C_{13}/C_{33})$. $C_{13}$(106 GPa) and $C_{33}$(398 GPa) are from experimental values [82]. The Results plotted in Figure.5.11 shows the effective mass gets reduced from 0.21 to 0.17 with 4% compressive biaxial strain. Figure.5.12 demonstrates the mechanism of reducing the effective mass with strain GaN and fully relaxed InGaN, where adding Indium shrinks the Brillouin zone and lower the bandgap, and strain in GaN only shrinks the Brillouin zone and maintain the bandgap.

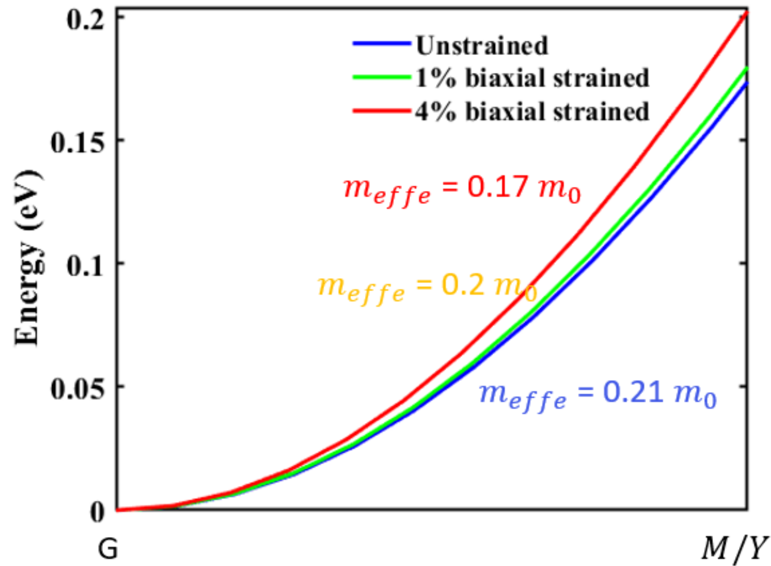



**Figure. 5.11 Calculated band structure of GaN under biaxial tensile strain**

Growing GaN on relaxed InGaN buffer can naturally achieve the biaxial tensile strain in GaN with GaN strained to InGaN. The biaxial tensile strain can be adjusted by changing the Indium composition of InGaN. Using Vegard's law, the reduced effective mass with different Indium composition can be calculated and plotted in Figure 5.13, including comparison with effective mass realized by relaxed InGaN channel. Comparing with relaxed InGaN, the strained GaN can achieve 50% of its reduction on effective mass without introducing In and associated alloy scattering in the channel. The device channel can get improvement on basis of high mobility achieved in 2DEG of GaN HEMT. Further, the strained GaN pay small penalty in bandgap while relaxed InGaN lose the wide bandgap from GaN. Table 6.1 presents the comparison of 3 different channel material unstrained GaN, strained GaN and relaxed InGaN.

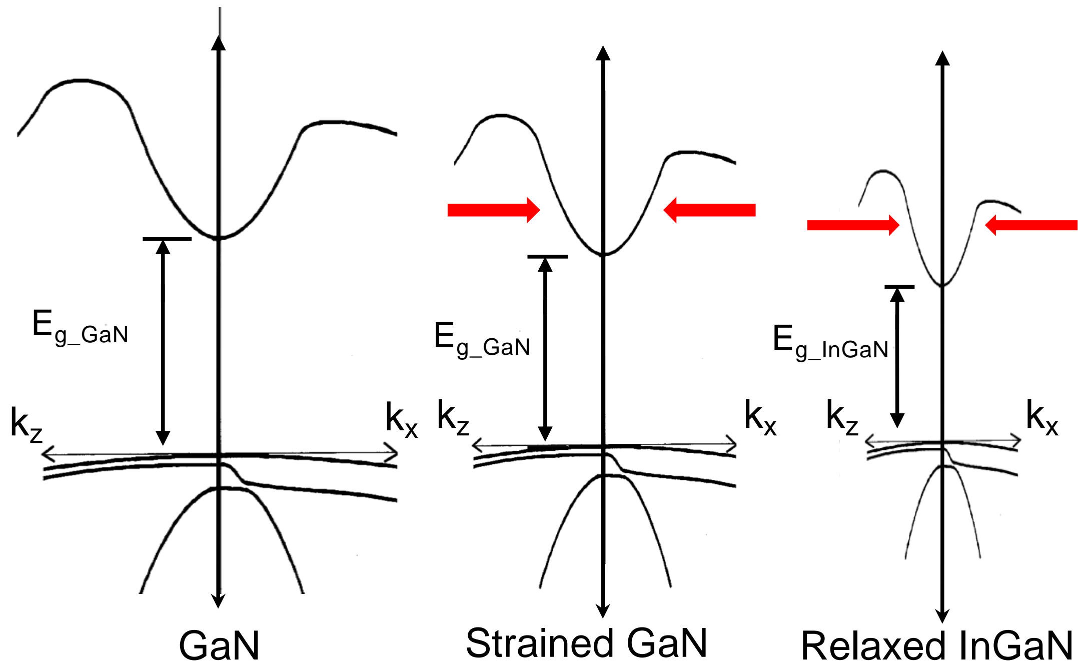



**Figure. 5.12 Illustration of band structure of GaN (a), strained GaN (b) and fully relaxed InGaN(c)**

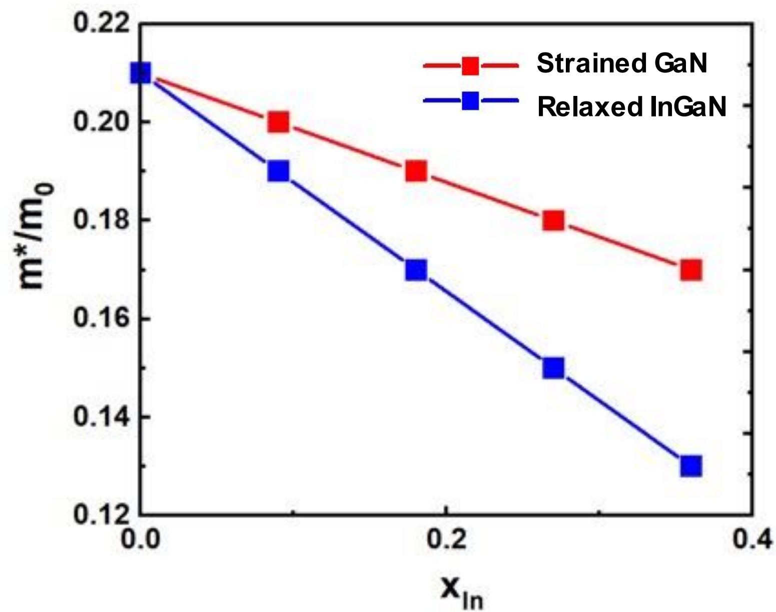



**Figure. 5.13 Effective mass dependence on In composition for strained GaN-on-InGaN and relaxed InGaN**

| | Unstrained GaN | Strained GaN | Relaxed InGaN |
|---|---|---|---|
| Electron mass | Good ($0.2 \cdot m_0$) | Good ($0.17m_0$) | Best ($0.13\ m_0$) |
| Bandgap | Best (3.4 eV) | Good (2.9 eV) | Low (2.1 eV) |
| 2DEG Mobility | Good (2000) | Best (>2000) | Low (<200) |

**Table. 5.1. Comparison of electron effective mass, bandgap and 2DEG mobility for channel material of unstrained GaN, strained GaN and relaxed InGaN**

Considering the electron velocity in GaN is strongly affected by optical phonon scattering, especially for high scaled device, the electron velocity in scaled GaN RF HEMT with strain GaN channel is predicted using a model based on optical phonon scattering discussed in chapter 2. As shown in the Figure.5.14, by reducing the effective mass from 0.21 to 0.17 with 4% compressive biaxial strain, the electron velocity gets an overall increase with different charge density and the peak velocity increase from $1.3 \times 10^7$ cm/s to $1.5 \times 10^7$ cm/s. With over 20% improvement in peak velocity, the device gm is expected to increase and achieve higher gain.

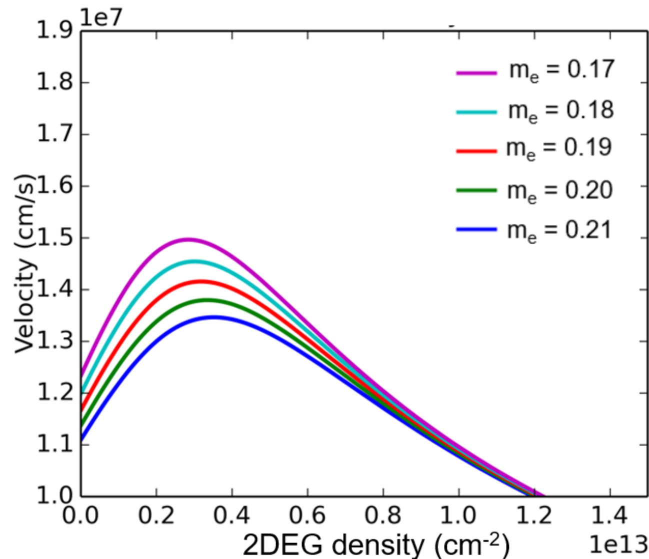



**Figure. 5.14 Injection velocity as a function of current density with different effective mass**

Device DC and RF performance are investigated with the effects from applying strain, The intrinsic transconductance and $f_T$ of scaled GaN RF HEMT are calculated with the method described in [83], using Cgs as a function of Vgs calculated by a self-consistent Poisson–Schrodinger solver with the device structure described in [37]. The gate length is selected to be 58 nm in the calculation and the series resistance used in calculation is set to be 0.13 Ω·mm, based on the extraction from small signal equivalent circuit model of device discussed in chapter 2. Figure.5.15 shows the peak transconductance increased by 10% with 4% compressive biaxial strain. The $f_T$ of the device with strained GaN channel was calculated using equation (2.9) from [38]:

The parameters used in the calculation are shown in the inset of Figure 5.16. As shown in Figure.5.16, the peak intrinsic $f_T$ of the calculated device increased from 240 GHz to 270 GHz with velocity enhancement caused by 4% biaxial strain. Both DC and RF performance of the transistor are expected to be improved with the enhanced electron velocity utilizing strained GaN channel.

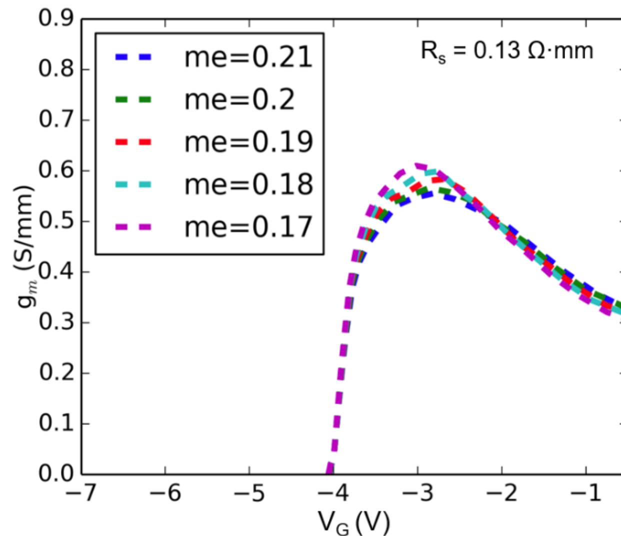



**Figure. 5.15 gm calculated by the optical-phonon-scattering based model [83].**

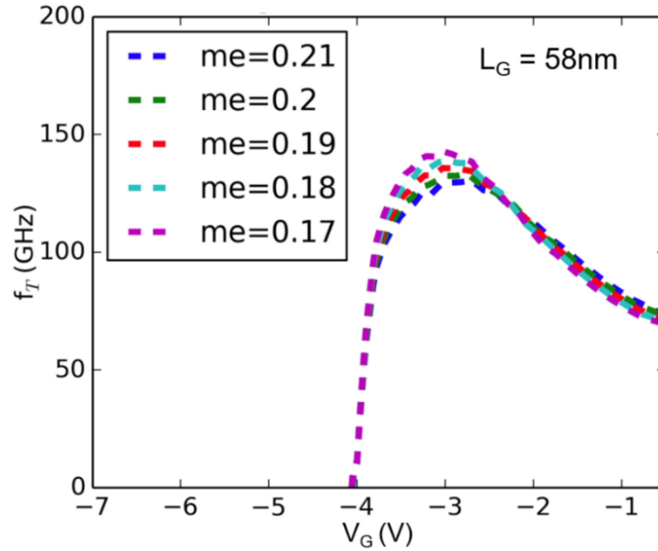



**Figure. 5.16 Device performance prediction of $f_T$ with different effective mass with Lg = 50 nm**

### *5.3. Summary*

Velocity enhancement with strain engineering in GaN is discussed in this chapter. Two methods are discussed, relaxed InGaN and strained GaN. For relaxed InGaN with low effective mass, experiments have been done utilizing porousificaiton to achieve porous GaN. With the demonstration of the first GaN/InGaN HEMT with a relaxed InGaN channel using a porous GaN structure, the extracted mobility in relaxed InGaN channel demonstrates ~10% 2DEG mobility improvement compared with the strained InGaN channel, and the results are consistent with a reduced effective mass predicted by theoretical analysis. The fabricated GaN HEMT with relaxed InGaN channel also show around 10% improvement of on-resistance comparing with the strained InGaN channel HEMT. The improvement in mobility is currently limited by the high Indium composition InGaN growth and the relaxation process. Severe

alloy scattering also reduces the electron mobility below 400 $cm^2 V^{-1} s^{-1}$, which required good alloy scattering control for application in GaN RF device for mm-wave and high frequency.

The strained GaN channel pays no penalty of Indium induced alloy scattering and reduced the effective mass. The electron effective mass in GaN under the effect of strain was studied with first principle calculation and the performance of GaN HEMT with a strained GaN channel are investigated, showing the effective mass can be reduced from 0.21 to 0.17 with 4% biaxial tensile strain. Comparison with relaxed InGaN channel shows that applying strain on GaN can realize 50% of its reduction on effective mass without adding In and associated alloy scattering. The effects of the strained GaN channel on device performance was also investigated using a model based on optical phonon scattering [83], showing the enhanced electron velocity over 15% with 4% compressive biaxial strain, suggesting improvement in both DC and RF characteristics.

However, it is still early to incorporate either of these two methods into state-of-art N-polar GaN RF device process, as more progress on material growth and compatible device fabrication process with the effective mass engineering are required to be developed for realizing strain engineering in GaN RF device for mm-wave application, more discussion will be given in the next chapter about future work.

# VI. Conclusion and guidance for future work

### *6.1. Summary and Conclusion*

This dissertation focusses on improving the performance of N-polar GaN deep recess HEMT and pushing it closer to the device limits. Although the N-polar GaN deep recess HEMTs overcome challenges faced by conventional Ga-polar AlGaN/GaN HEMT and have set the record in efficiency and power for GaN device at W-band, the ability to achieve higher power and higher efficiency simultaneously is still limited by the gain of the device at W-band. More electrostatics study and innovation is needed to further improve the performance of such well-defined device.

Works in this dissertation starts with learning from previous stat-of-art N-polar GaN deep recess HEMT and modelling devices with physical understanding and observation. A predictive physics-based model on device I-V characteristics has been proposed to understand device operation and inspect the performance N-polar GaN deep recess device to help device design. The modelling results show good agreement with experimental data for both DC and RF performance and demonstrated great potential of modelling device S-parameters and large signal performance with such straight forward physics-based model.

The device modeling also validates the predictive manner of device performance, showing increase the gm and reduction of fringing capacitance are two critical key to improve performance of N-polar GaN deep recess HEMT. For fringing capacitance, the electrostatics study on fringing gate capacitance in N-polar GaN deep recess HEMT is performed and evaluate the dependency of fringing capacitance on GaN cap layer and extrinsic passivation.

Based on the fringing capacitance study, the GaN cap layer is reduced from conventional 48 nm to 20 nm with no extrinsic passivation. Combined with improvements in device

fabrication of ALD RU gate and great commercial epi from Transphorm with reduced 10 nm GaN channel, the fabricated GaN-on-Sapphire deep recess HEMT demonstrated record gain and efficiency at 94GHz with high output power. Without any extrinsic passivation, record linear transducer gain of 9.65 dB is achieved, enabling record 42% PAE with associated 4.4 W/mm of output power density at 12 V drain bias condition. Highest efficiency is measured at 8 V drain bias with PAE of 44% and associated 2.6 W/mm of output power density.
After thin 20 nm PECVD SiN passivation, devices performance was pushed into high V bias and show very high output power density of 5.83 W/mm with a high PAE of 38.5% at 94 GHz. The excellent results verify the design ideas and show great potential of achieving even high-performance using N-polar GaN deep recess device with better thermal management, such as GaN-on-SiC and diamond heat sink integration.

As innovation technique, strain engineering in GaN has also been proposed and explored or improving the device performance. Both relaxed InGaN channel and strained GaN channel were investigated for electron velocity improvement. For relaxed InGaN, the GaN-based HEMTs with a relaxed InGaN channel has been fabricated utilizing a porous GaN technology and show ~10% 2DEG mobility enhancement compared with the strained InGaN channel, proving the benefits from strain engineering.

For strained GaN channel, impact on electron effective mass in GaN from the biaxial tensile strain was calculated using first principal calculation. The electron velocity with biaxial tensile strain in GaN is also studied with the consideration of optical phonon scattering in GaN. Using model developed in this dissertation, device performance of GaN HEMT with strained GaN channel are investigated, showing improvements in both DC and RF performance of the transistor with the enhanced electron velocity.

### *6.2. Guidance for future work*

The works in this dissertation focus on improvement of previous N-polar GaN deep recess HEMT for pushing device performance closer to its limit, the device definitely has not reached the maximum of its performance and there are ways to extend the works done in this dissertation to help N-polar GaN deep recess HEMT achieving high performance.

#### *6.2.1 Device dimension scaling*

The fabricated N-polar GaN deep recess HEMT in this dissertation features a $L_G$ of 57 nm, $L_{GS}$ of 75 nm and $L_{GD}$ of 288 nm. Further scaling in $L_{GS}$ is expected to reduce the series resistance in the transistor and improve gain but also introduce more difficulty in device fabrication, especially in a university clean room. However, considering the drain bias used in the large signal measurement in the reported device, the $L_{GD}$ is believed to afford more scaling to support drain bias of around 16 V and less $R_D$ for high gain. The $L_G$ of 57 nm is the smallest gate length fabricated on the wafer, so more scaled gate can be tried but it is expected that short channel effect and ALD Ru gate process limit the shrinking of $L_G$ to less than 30 nm.

#### *6.2.2. Device modelling*

As the modelling works discussed in this dissertation shows calculated transfer curve and fT vs gate voltage relation, further work on velocity before saturation can help calculated the output characteristics and consideration of non-linear resistance in the access region should be included. With the calculation capability of DC performance, S-parameters and large signal modelling are all feasible with the extensive work based on this physics-based model.

#### *6.2.3. Strain engineering in GaN*

As discussed in this dissertation, the relaxed InGaN channel can lower the effective mass but introduce severe alloy scattering which destroy the mobility. The calculation demonstrated the benefits expected from strained GaN channel with biaxial tensile strain, and the experiments can start with investigation on growing fully strained GaN on thick InGaN buffer. As a critical building block for achieving the strain engineering in GaN, enough thickness of fully strain GaN-on-InGaN is needed for the HEMT structure. As an innovative technique in GaN material system, strain engineering is attractive and still needs lot of investigation both in growth and device fabrication.

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