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Silicon Integrated High-density Electrocortical and Retinal Neural Interfaces

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#### UNIVERSITY OF CALIFORNIA, SAN DIEGO

#### Silicon Integrated High-density Electrocortical and Retinal Neural Interfaces

A dissertation submitted in partial satisfaction of the requirements for the degree

Doctor of Philosophy

in

Bioengineering

by

Sohmyung Ha

#### Committee in charge:

Professor Gert Cauwenberghs, Chair

Professor Todd P. Coleman

Professor David A. Gough

Professor Yu-Hwa Lo

Professor Patrick P. Mercier

Professor Gabriel A. Silva

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The dissertation of Sohmyung Ha is approved, and it is	3
acceptable in quality and form for publication on micro-	-
film and electronically:	
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Chair	-

University of California, San Diego

2016

# DEDICATION

Dedicated to my parents Young Tae Ha and Jung Ok Lee and my wife Seoyeon Lee.

#### **EPIGRAPH**

The Sovereign Lord has given me his words of wisdom, so that I know how to comfort the weary.

Morning by morning he wakens me and opens my understanding to his will.

—Isaiah 50:4

You will show me the way of life, granting me the joy of your presence and the pleasures of living with you forever. —Psalm 16:11

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Sohmyung Ha, Chul Kim, Jongkil Park, Siddharth Joshi and Gert Cauwenberghs, Energy-Recycling Integrated 6.78-Mbps Data 6.3-mW Power Telemetry over a Single 13.56-MHz Inductive Link, *Symposium on VLSI Circuits Digest of Technical Papers*, Honolulu, HI, USA, June 10-13, 2014.

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#### ABSTRACT OF THE DISSERTATION

#### Silicon Integrated High-density Electrocortical and Retinal Neural Interfaces

by

#### Sohmyung Ha

Doctor of Philosophy in Bioengineering

University of California, San Diego, 2016

Professor Gert Cauwenberghs, Chair

Recent interest and initiatives in brain research have driven a worldwide effort towards developing implantable neural interface systems with high spatiotemporal resolution and spatial coverage extending to the whole brain. Electrocorticography (ECoG) promises a minimally invasive, chronically implantable neural interface with resolution and spatial coverage capabilities that, when appropriately scaled, meet the needs of recently proposed brain initiatives. Current ECoG technologies, however, typically rely on cm-sized electrodes and wired operation, severely limiting their resolution and long-term use.

The work presented here has advanced micro-electrocorticography ( $\mu$ ECoG) technologies for wireless high-density cortical neural interfaces in two main direc-

tions: flexible active  $\mu$ ECoG arrays; and modular fully integrated  $\mu$ ECoG systems. This dissertation presents a systematic design methodology which addresses unique design challenges posed by the extreme densities, form factors and power budgets of these fully implantable neural interface systems, with experimental validation of their performance for neural signal acquisition, stimulation, and wireless powering and data communication. Notable innovations include 1) first demonstration of simultaneous wireless power and data telemetry at 6.78 Mbps data rate over a single 13.56 MHz inductive link; 2) integrated recording from a flexible active electrode ECoG array with 85 dB dynamic range at 7.7 nJ energy per 16-b sample; and 3) the first fully integrated and encapsulated wireless neural-interface-on-chip microsystem for non-contact neural sensing and energy-replenishing adiabatic stimulation delivering 145  $\mu$ A current at 6 V compliance within 2.25 mm<sup>3</sup> volume.

In addition, the work presented here on advancing the resolution and coverage of neural interfaces extends further from the cortex to the retina. Despite considerable advances in retinal prostheses over the last two decades, the resolution of restored vision has remained severely limited, well below the 20/200 acuity threshold of blindness. Towards drastic improvements in spatial resolution, this dissertation presents a scalable architecture for retinal prostheses in which each stimulation electrode is directly activated by incident light and powered by a common voltage pulse transferred over a single wireless inductive link. The hybrid optical addressability and electronic powering scheme provides for separate spatial and temporal control over stimulation, and further provides optoelectronic gain for substantially lower light intensity thresholds than other optically addressed retinal prostheses using passive microphotodiode arrays. The architecture permits the use of high-density electrode arrays with ultra-high photosensitive silicon nanowires, obviating the need for excessive wiring and high-throughput data telemetry. Instead, the single inductive link drives the entire array of electrodes through two wires and provides external control over waveform parameters for the common voltage stimulation. A complete system comprising inductive telemetry link, stimulation pulse demodulator, charge-balancing series capacitor, and nanowire-based electrode device is integrated and validated ex vivo on rat retina tissue. Measurements demonstrate control over retinal neural activity both by light and electrical bias, validating the feasibility of the proposed architecture and its system components as an important first step towards a high-resolution optically addressed retinal prosthesis.

# Chapter 1

# Introduction

My research aims at advancing the engineering and applications of silicon integrated technology interfacing with biology in a variety of forms ranging from implantable biomedical devices to unobtrusive wearable sensors. The engineering advances in the design of integrated circuits and system components target high performance, miniature form factor, and power autonomy in fully integrated interfaces under challenging energy and density constraints and noise conditions in the implantable or wearable biological setting. Targeted applications include self-powered biosensors for wearable health monitoring, subcutaneous glucose sensors for continuous monitoring in diabetes patients, nanoengineered silicon retinal interfaces to restore spatial vision in the severely visually impaired, and minimally invasive brain-computer interfaces for closed-loop remediation of neurological disorders such as epilepsy and Parkinsons disease.

Chapter 2 presents an overview of the fundamentals and state-of-the-art in physiological monitoring instrumentation with a focus on electrode and optrode interfaces to the body, and micropower integrated circuit design for unobtrusive wearable applications. Since the electrode/optrode-body interface is a performance limiting factor in non-invasive monitoring systems, practical interface configurations are offered for biopotential acquisition, electrode-tissue impedance measurement and optical biosignal sensing. A systematic approach to instrumentation amplifier (IA) design using CMOS transistors operating in weak inversion is shown to offer high energy and noise efficiency. Practical methodologies to obviate

1/f noise, counteract electrode offset drift, improve common-mode rejection ratio (CMRR), and obtain sub-Hz highpass cutoff are illustrated with a survey of the state-of-the-art IAs. Further, fundamental principles and state-of-the-art technologies for electrode-tissue impedance measurement, photoplethysmography (PPG), functional near-infrared spectroscopy (fNIRS) and signal coding and quantization are reviewed, with additional guidelines for overall power management including wireless transmission. Examples are presented of practical dry-contact and noncontact cardiac, respiratory, muscle and brain monitoring systems and their clinical applications.

Chapter 3 discusses the challenges and state-of-the-art technologies that are enabling next-generation fully implantable high-density ECoG interfaces, including details on electrodes, data acquisition front-ends, stimulation drivers, and circuits and antennas for wireless communications and power delivery along with state-of-the-art implantable ECoG interface systems.

Chapter 4 presents a telemetry IC with a new data modulation scheme for efficient simultaneous transfer of power and backward data over a single inductive link. Data-driven synchronized single-cycle shorting of the secondary LC tank conserves reactive energy while inducing an instantaneous voltage change on the primary side. Contrary to conventional LSK modulation, the recovery time of the secondary LC oscillation after shorting improves asymptotically with increasing quality factor of the secondary LC tank. Since quality factor does not reduce the data rate, the LC tank can be simultaneously optimized for power and data telemetry, obviating the conventional trade-off between power transfer efficiency and data rate. Cyclic on-off keying time-encoded symbol data mapping of the shorting cycle allows transmission of two data bits per four carrier cycles while supporting simultaneous power delivery during at least six non-shorting out of eight half cycles. All timing control signals for rectification and data transmission are generated from a low-power clock recovery comparator and a phased-locked loop. The 0.92-mm<sup>2</sup> 65-nm CMOS IC delivers up to 11.5-mW power to the load and simultaneously transmits 6.78-Mbps data while dissipating 64  $\mu$ W power. A BER of  $\leq 9.9 \times 10^{-8}$  was measured over a single 1-cm 13.56-MHz inductive link at

a data rate of 6.78-Mbps with a 10-mW load power.

Chapter 5 presents the design, implementation, and experimental characterization of a low-noise low-power biopotential recording integrated circuit (IC) in support of a fully implantable, high-density, actively multiplexed and flexible  $32\times32$  electrode array for electrocorticography (ECoG) neural recording. Each ECoG recording IC contains an 8-channel ADC, each serving one column and multiplexing up to 32 rows in the external ECoG array. Each column ADC converts signal coarsely by 10-bit successive approximation (SA), and performs fine conversion of the residue by 7-bit 1st order incremental delta-sigma ( $\Delta\Sigma$ ) conversion. One bit of overlap between SA and  $\Delta\Sigma$  stages supports wide dynamic range with an instantaneous core range of 3.9 mV, sufficiently larger than typical ECoG signals, while handling electrochemical and process variations in the ECoG electrode array up to  $\pm 1$  V. Tests show a measured dynamic range of 85 dB and CMRR of 87 dB at 19.5 kS/s and at 19.4  $\mu$ A from 3.3 V per ADC channel. The 8-channel IC occupies 18 mm<sup>2</sup> in 0.6  $\mu$ m 2P3M CMOS.

Chapter 6 presents advances towards a modular implantable high-resolution and miniature ECoG interface system. Multiple ENIACs can be placed across the cortical surface, enabling dense coverage over wide area with high spatiotemporal resolution. The circuit and system level details of ENIAC are presented, along with measurement results. This fully-integrated 16-channel wireless neural interfacing SoC employs an adiabatic stimulator powered directly from a 190-MHz on-chip antenna to eliminate bulky external components while simultaneously avoiding rectifier and regulator losses. Using a charge replenishing architecture, the stimulator outputs up to 145- $\mu$ A, while achieving a 63.1% charge replenishing ratio and a stimulation efficiency factor of 6.0. Analog front-ends (AFEs) and telemetry circuitry are also included.

Chapter 7 presents advances towards a nano-engineered high-resolution retinal prostheses. Despite considerable advances in retinal prostheses over the last two decades, the resolution of restored vision has remained severely limited, well below the 20/200 acuity threshold of blindness. Towards drastic improvements in spatial resolution, a scalable architecture is proposed in which each stimula-

tion electrode is directly activated by incident light and powered by a common voltage pulse transferred over a single wireless inductive link. The hybrid optical addressability and electronic powering scheme provides for separate spatial and temporal control over stimulation, and further provides for optoelectronic gain which is typically lacking in optically addressed retinal prostheses using passive microphotodiode arrays. The architecture permits the use of high-density electrode arrays with ultra-high photosensitive silicon nanowires, obviating the need for excessive wiring and high-throughput data telemetry. Instead, the single inductive link drives the entire array of electrodes through two wires and provides external control over waveform parameters for the common voltage stimulation. A complete system comprising inductive telemetry link, stimulation pulse demodulator, charge-balancing series capacitor, and nanowire-based electrode array is integrated and validated ex vivo on rat retina tissue. Measurements demonstrate control over retinal neural activity both by light and electrical bias, validating the feasibility of the proposed architecture and its system components as an important first step towards a high-resolution optically addressed retinal prosthesis.

Finally, Chapter 8 offers concluding remarks on the advances contributed in this thesis, their significance, and directions for future research.

# Chapter 2

# Integrated Circuits and Electrode Interfaces for Physiological Monitoring

## 2.1 Introduction

Physiological monitoring technology has advanced tremendously over the years making a substantial impact on medical diagnostics and personal health-care, from the early fundamental advances in non-contact and dry sensing technology [32,156,242] to most recent advances extending the range of physiological sensing using imaging and electrical sensing technology abundantly available in handheld devices and household appliances [117,169,307,334]. CMOS technologies and circuit techniques have facilitated the development and miniaturization of innovative physiological sensing devices, improving the performance, power and monetary costs while ensuring the validity of medical information through analog and digital signal processing methods. These IC developments have permitted reliable measurement of vital parameters and have spawned a variety of new instruments for clinical treatment and diagnosis.

Innovations by semiconductor technologies enable ambulatory continuoustime monitoring of patients even at home. This ubiquitous monitoring supported

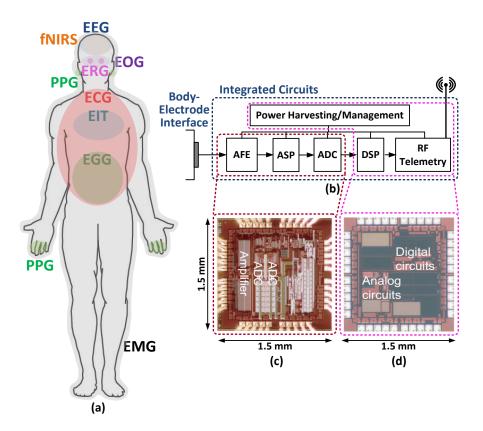


Figure 2.1: Non-invasive physiological monitoring. (a) Signal modalities of electrical and vascular activity internal to the body available for measurement on the periphery. See Table 7.1 for glossary. (b) Integrated circuits (ICs) and electrode interfaces for signal acquisition, coding, and transmission. Example micrographs are shown for (c) a biopotential front-end and acquisition IC interfacing through bit-serial daisy chain with (d) a power and data telemetry IC [277].

by modern IC technology can enable personalized healthcare and preemptive medicine, which are emerging solutions to soaring healthcare costs induced by the current demographical trend of increasing aging population. The patient-supporting sensors and systems not only extend the capability and accuracy of modern diagnostics, but also improve the patient's everyday life. In addition, miniaturized electronic systems for biosignal sensing can be tailored to many non-clinical applications such as sports and entertainment.

Fig. 2.1 (b) shows the main functional components of a generic IC for non-invasive physiological monitoring, comprising analog front-end (AFE), analog signal processor (ASP), analog-to-digital converter (ADC), digital signal processor

		<u> </u>	
	Name	Carrier	Activity
EEG	Electroencephalography	Voltage	Brain rhythms
ECG	Electrocardiography	Voltage	Cardiac rhythms
EMG	Electromyography	Voltage	Muscle activation
EOG	Electrooculography	Voltage	Eye movement
ERG	Electroretinography	Voltage	Retinal potentials
EGG	Electrogastrography	Voltage	Stomach activity
EIT	Electrical impedance	Impedance	Lung activity
	tomography		
fNIRS	Functional near-infrared	Optical	Neurovascular activity
	spectroscopy		
PPG	Photoplethysmography	Optical	Blood oxygenation

**Table 2.1**: Non-Invasive Physiology and Body Signals

(DSP), radio frequency (RF) communications, and power management. This review surveys these components with a focus on the core functions of AFE, ASP, and ADC implemented in low-noise, low-power custom integrated circuits, and tailored to the signal conditions and range of the physiological variables of interest. Foremost, a solid and thorough understanding of the electrode-body interface is of primary importance for accurate and reliable non-invasive physiological sensing and signal acquisition. The following section reviews fundamentals of electrode-body and optrode-body interfaces for biopotential acquisition, impedance measurement, and optics-based sensing.

# 2.2 Non-Invasive Electrode-to-Body Interfaces

# 2.2.1 Electrode Interfaces for Biopotential Sensing

The coupling of biopotential signals from the body into the front-end amplifier is accomplished through electrodes. At a fundamental level, the electrode interfaces ionic currents in the body with electrical currents in the electronic instrumentation. In practice, because the electrode comprises the first stage of the signal chain, its properties can dominate the overall noise and performance of the acquisition system making its design and selection crucially important.

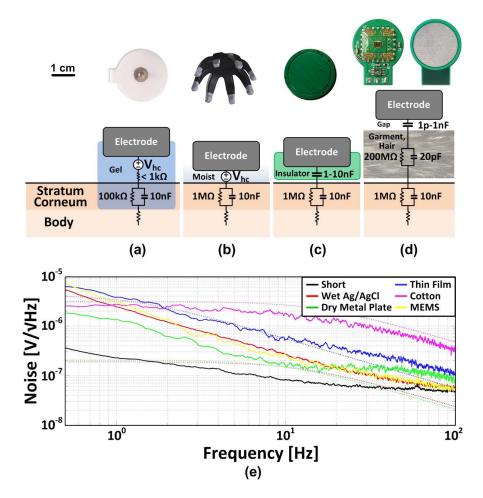


Figure 2.2: Electrical coupling of the skin-electrode interface for various electrode topologies, including (a) wet-contact gel-based Ag / AgCl [70], (b) dry-contact flexible thru-hair sensor [79], (c) thin-film insulated capacitive metal plate [69], and (d) non-contact metal plate coupling through hair or clothing such as cotton [71]. (e) Measured noise spectrum of various electrode types, placed at close proximity on forearm at rest, along with predicted (dotted lines) thermal noise limits from measured skin-electrode coupling impedance data [70]. The instrumentation noise floor of the shorted amplifier is also shown for reference.

Broadly speaking, there exist three classes of biopotential electrodes in the literature: wet, dry and non-contact as shown in Fig. 2.2 [70, 335]. All types of electrodes ideally measure the exact same biopotential signals and are largely

differentiated by the presence of a gel and the resulting contact impedance to the body.

Wet electrodes are the most common type and considered the "gold standard" for both clinical and research applications. A typical wet electrode consists of a silver-silver chloride (Ag/AgCl) metal that is surrounded by a wet or solid hydrogel, containing chloride. Other kinds of metals can be used (gold is common for EEG) if the DC stability of the Ag/AgCl electrode is not necessary. The primary drawbacks with wet electrodes are its longevity and comfort. Wet electrodes degrade as the moisture content evaporates limiting its useful lifetime to, at most, a few days. Many users also report skin irritation and discomfort from the gels and adhesives that contact the skin.

Dry electrodes operate without the use of an explicit wet/gel coupling media. The metal in the electrode directly contacts the skin to couple biopotential signals. In practice, however, virtually all dry electrodes still rely on some degree of moisture which is gathered from the environment or emitted from the body (e.g., sweat). Compared with the wet electrodes, the performance of a dry electrode usually increases over time as more moisture permeates the skin-electrode interface resulting in increased coupling. On bare skin, dry electrodes normally exhibit higher contact impedances than wet electrodes by one order of magnitude difference [22]. However, with modern high input impedance amplifiers, this is rarely an issue. As with wet electrodes, Ag/AgCl contact materials tend to show the best performance, especially in terms of drift noise, which is important for diagnostic ECG applications.

There are also dry contact electrodes with capacitive coupling between the electrode and the body instead of coupling via galvanic conduction. Capacitive contact electrodes utilize a thin dielectric layer to form an insulated contact to the body. Compared to standard dry contact electrodes, capacitive electrodes offer a galvanically isolated, chemically inert surface, maximizing user safety and electrode longevity. However, the capacitive interface precludes the measurement of true DC potentials and may result in long settling times depending on the bias resistor and the amount of coupling to the body. In other respects, the capacitive

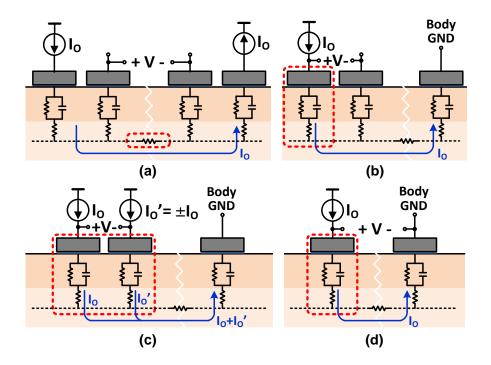
contact electrodes operate similar to dry contact electrodes.

The final type of electrodes, non-contact, can be thought of as a special case of dry electrodes. They operate not only without gel, but also through an insulation layer such as clothing, enabling signal acquisition without direct skin contact. As expected, the coupling impedance can be very high on the order of tens of pF in parallel with hundreds of  $M\Omega$ . Obtaining acceptable signals requires the use of special, very high input impedance active electrodes. Because there is no direct skin contact, movement artifacts are a major, unsolved issue especially for ambulatory use. Non-contact electrodes are also highly sensitive to environmental conditions such as humidity and the exact insulating material. Non-contact electrodes tend to work well on natural fabrics (e.g., cotton) under high humidity where the fabric actually becomes slightly conductive, offering a galvanic path to the skin. In contrast, it is difficult to obtain acceptable signals on high insulating synthetic fabrics (e.g., polyester) due to triboelectric artifacts.

#### 2.2.2 Electrode Interfaces for Impedance Sensing

Controlled activation of current sources at electrode interfaces for biopotential sensing directly extends their use to sensing of electrical impedance. Two applications of impedance sensing are of particular interest: electrical impedance tomography (EIT) for medical imaging by spatial mapping of tissue impedance across body parts, and tissue-electrode impedance (ETI) checking for electrode contact quality monitoring.

EIT across a suitably sized array of electrodes placed over the body surface offers a low-cost, low-profile, non-invasive medical imaging modality free of ionizing radiation [29,269] that has been applied to detection of breast cancer [193], imaging of brain function [24,384], and monitoring of lung function [152]. A basic four-electrode setup for one EIT impedance element is illustrated in Fig. 2.3 (a) [392]. High-impedance current sources inject complementary AC currents through two electrodes, while voltage is recorded between separate high-impedance sense electrodes. The recorded voltage is hence independent of any electrode impedance, and directly conveys tissue impedance between the body terminals interfacing with the



**Figure 2.3**: Body-electrode interfaces for (a) electrical impedance tomography (EIT) and (b-d) electrode-tissue impedance (ETI) measurements.

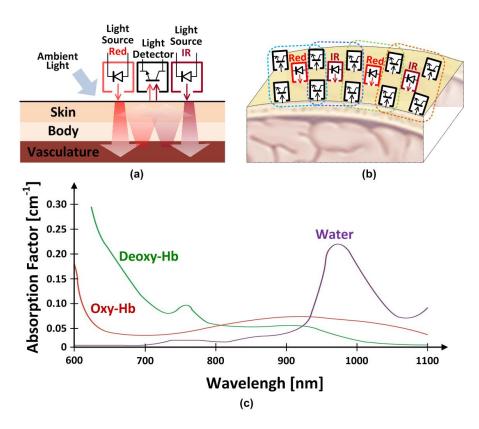
sense electrodes.

A simple scheme for measurement of electrode-tissue impedance using three electrodes as shown in Fig. 2.3 (b) has been implemented for the tracking of biopotential electrode quality and identification of movement artifacts [401, 443]. The voltage between one electrode driven by a high impedance current source and another high input-impedance sensing electrode is measured to obtain only the electrode-tissue impedance connected to the AC current source [443]. Although activation of one AC current source can be interchanged between the two electrodes in order to measure both impedances in sequence, more reliable measurement is obtained by simultaneous activation of two equal magnitude AC current sources as shown in Fig. 2.3 (c). The sum of electrode impedances is obtained from measurement of the voltage difference during activation of currents with opposing polarities, while the difference of impedances is obtained for same-polarity currents [47,211,441]. A simplified arrangement for directly estimating individual electrode impedance is shown in Fig. 2.3 (d). This arrangement takes advantage

of the availability of a low-impedance body ground connection and the fact that body tissue impedance is negligible in comparison to tissue-electrode impedance.

A standard driven right leg (DRL) scheme with high-gain negative feedback between separate ground sense electrode and the drive ground electrode ensures that the body is at the system ground potential regardless of the injected electrode current [420, 421].

#### 2.2.3 Optrode Interfaces for Spectrophotometric Sensing



**Figure 2.4**: Interface for (a) photoplethysmography (PPG) and (b) functional near-infrared spectroscopy (fNIRS). (c) Absorption factors of oxyhemoglobin, deoxyhemoglobin and water with respect to the light wavelength [44].

Spectrophotometric measurement of blood oxygen saturation has been widely adopted in clinical and outpatient settings as it simultaneously provides information about heart rate, blood pressure variation and respiratory function in a completely non-invasive modality at low power [326]. Light from two different

light-emitting diodes (LEDs), at red (660 nm) and infrared (940 nm) wavelengths, is shined upon a body area with good perfusion and quantification of either the transmitted or reflected light is done to calculate absorbance through the tissue by a photodiode. In this function, pulse oximeters are commonly presented as finger clips or rings and generally use transmission mode measurement, while more recent applications such as patches, wristwatches and smartphones require a reflection based system [141,236] as shown in Fig. 2.4 (a). Just like biopotential measurements, optical techniques can also be applied to quantify brain activity. Functional near-infrared spectroscopy (fNIRS) measures cerebral oxygenation, which is related to activity, through the skull [44]. fNIRS produces functional brain images from neighboring sources and detectors placed on the head as shown in Fig. 2.4 (b). Distance and configuration of sources and detectors placement determines spatial resolution of the fNIRS. Recently, advances in integrated silicon avalanche photodiodes have dramatically improved the performance and wearability [186].

#### 2.2.4 Problems and Challenges at the Interface

In addition to circuit noise from amplifier components, electrodes can be a significant noise contributor in the signal chain [70,165]. Unlike circuit noise, however, comprehensive models for electrode noise do not exist, in part because the mechanisms for electrode noise are not well understood. In general, electrode noise is strongly correlated with the contact impedance but the actual level is significantly higher than the thermal noise from the resistive portion of the impedance.

The aggregate sum of the electrode noise sources can be quite large, in the order of  $\mu V/\sqrt{Hz}$  at 1 Hz, even for wet electrodes. This far exceeds the noise contribution of circuit components, illustrating the importance of proper electrode selection. Due to integrated current noise, both wet and dry electrodes have sharp  $1/f^2$  spectra, which shows up as baseline drifts in the time domain.

Non-contact electrodes can pick up additional noise from the insulating material between the metal and the skin. As an example, acquiring signals through fabrics can be noisy due to the intrinsic high resistance of the fabric (>100 M $\Omega$ ). This amounts to the equivalent of inserting a large resistor in series with the

amplifier input and can add significant noise in the signal bandwidth.

Outside of controlled laboratory conditions, the largest noise sources will likely be electromagnetic interference (EMI) and movement artifacts. The most common symptom of EMI is seen as 50/60 Hz power line pickup. Triboelectric charging during subject movement is also a large, albeit less understood, source of interference. As a subject moves, the potential between the body and environment changes due to charge generation from striking the ground. This can couple into the system just like EMI and is often mistaken for movement artifacts induced by electrode-skin displacements.

EMI can be reduced or eliminated by a few simple techniques. Common-mode interference is easily attenuated through the use of a DRL circuit [420,421]. This technique is well understood and operates by actively biasing the body potential towards a fixed circuit reference potential through the use of negative feedback. This has the effect of reducing the magnitude of common mode interference seen by the amplifiers. Differential pickup of EMI is mitigated through the use of active electrodes with an amplifier placed in close proximity to the electrode [68, 90, 104, 288, 429]. Alternatively, the use of shielded lead wires is also highly effective at accomplishing the same goal, minimizing the total area of high impedance traces that are susceptible to external electric fields [104].

Movement artifacts are a difficult challenge due to the lack of quantified metrics and clear design methodology. Any physical displacement between the electrode and the skin will necessarily generate noise, sometimes many orders of magnitude larger than the actual signal.

Movement artifacts can be eliminated by increasing the physical coupling pressure between the electrode and skin but may conflict with the need for comfort and wearability. Reducing movement artifacts highly relies on mechanical and industrial design, and solutions are highly dependent on the specific end application. In addition, electrode-tissue impedance measurement and signal processing techniques can be used to quantify and suppress movement artifacts [47, 132, 208, 209, 211, 401, 441].

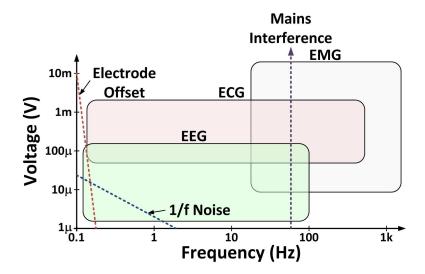
# 2.3 Analog Front-End for Non-Invasive Sensing

### 2.3.1 Physiological Requirements

The main design requirements of the AFE, ASP, and ADC are driven by characteristics of the physiological signals and the body-electrode interface.

#### **Biopotential Sensing**

Biopotentials, such as EEG, ECG, EMG, etc., are generated from volume conduction of currents made by collections of electrogenic cells. EEG is the electrical potential induced from collective activities of large number of neurons in the brain. ECG results from action potentials of cardiac muscle cells, and EMG from contractions of skeletal muscle cells. Various other biopotentials (EOG, ERG, EGG, etc.) also result from collective effects of large numbers of electrogenic cells or ionic distribution.



**Figure 2.5**: Characteristics of EEG, ECG and EMG, in relation to mains interference, electrode offset drift and 1/f noise [413, 444].

Almost all biopotentials, including EEG, ECG and EMG of which characteristics are shown in Fig. 2.5, range over very low frequency, typically less than 1 kHz. They are very low in amplitude ranging tens to hundreds  $\mu$ V when measured by a surface electrode. Since EEG and ECG range down to less than 1 Hz,

recording of these signals faces challenges in electrode offset voltage, which may reach up to 100 mV, varying slowly over time. In addition, 1/f noise needs to be suppressed if the application calls for low noise at low frequencies (< 1 Hz). Also, common-mode interference from the mains and other irrelevant biopotentials should be sufficiently rejected.

#### Electrode-Tissue Impedance Measurement

The measurement of electrode-tissue impedance (ETI) is implemented by sensing a potential between electrodes while injecting an alternating current. Therefore, most of the requirements for biopotential sensing also apply to ETI measurement circuit. However, in order to identify and suppress movement artifacts, the electrode-tissue impedance and biopotential signal should be sensed simultaneously [211, 401]. This requires chopper stabilization schemes for the impedance measurement to separate electrophysiological from resistive and reactive impedance signals, each occupying different frequency bands (Sec. 2.3.8).

As additional advantage, chopper stabilization shields the electrode from any DC currents, such as caused by imbalances between source and sink currents and which lead to harmonic distortion and saturated outputs [47]. The high dynamic range of k $\Omega$ -range electrode-tissue impedances amidst  $\Omega$ -range body tissue impedances [210], could further be a potential source of saturation, mitigated by varying the amplitude of the AC current. Larger injected AC currents lower the input-referred noise at the expense of power.

#### **Optics-based Sensing**

Pulse oximeters and fNIRS systems have similar system requirements. The bandwidth of the hemodynamic and oxygenation signals ranges from approximately DC to 20 Hz. However, it is preferable to sample these signals at greater than 240 Hz, the Nyquist frequency of fluorescent light, to prevent aliasing of 60-Hz background interference [236]. Light attenuation is in the range of  $10^{-4}$  to  $10^{-3}$ , with reflection-based systems showing greater attenuation than transmission systems [125]. AC/DC contrast ratio can be as low as 0.25-1% of which accuracy

must be within 2% [326]; thus contrast detection in front-end system must have a resolution of around 0.01% while being able to reject a large range of DC light incidence due to the variability in application (patients, environment, movement artifact, etc.). Peak LED driving currents for pulse oximetry range in the few tens mA range and duty cycle for low power pulsed system can be as low as 1-3% [125, 376]. The light source to detector distance is approximately 3 mm in reflection oximetry systems [141], while in fNIRS this separation must be around 3 cm to be able to image the cerebral cortex non-invasively [72]. Additionally, fNIRS systems require higher CMRR to reject interference [185].

**Table 2.2**: Design Factors and Trade-Offs in Integrated Electrode Interfaces for Non-Invasive Physiological Monitoring

Design Factors	Trade-Offs and Inter-Relations	Typical Range (Biopotentials)	Comments / Examples	
Input Referred Noise	<b>∀</b> ∀	1–5 μVrms	Dominated by electrode interface and front-end amplifier [Wu 2009, Zou 2009, Tseng 2012]	
Power Consumption		0.1–100 μW	Lowered by biasing, or duty cycling/multiplexing above Nyquist rate [Ng 2005, Wu 2009, Zou 2009]	
Bandwidth	X 1	0.1–10 kHz	Application specific or configurable [Mollazadeh 2009, Yazicioglu 2007, Zou 2009]	
Dynamic Range (DR)		40–120 dB	Variable gain compounds signal-to-noise ratio for extended DR [Xu 2011, Yazicioglu 2007, Zou 2009]	
Variable Gain		1-1,000 V/V	Typically digitally selectable with auto-ranging capability [Ng 2005, Yazicioglu 2007, Zou 2009]	
Power Supply Rejection Ratio (PSRR)		40–80 dB	Frequency dependent, limiting switching regulator frequency [Yazicioglu 2007, Yazicioglu 2008, Zhang 2011]	
Common-Mode Rejection Ratio (CMRR)	<b>│                                    </b>	60-120 dB	Mostly mains interference rejection; through active grounding (DRL) [Yazicioglu 2008, Yazicioglu 2007, Wu 2009]	
Input Impedance	\ <b>&gt;</b> \ //</td <td>100 ΜΩ–10 ΤΩ</td> <td>Resistive/capacitive; depending on the contact type and application [Chi 2011, Xu 2011, Fan 2011]</td>	100 ΜΩ–10 ΤΩ	Resistive/capacitive; depending on the contact type and application [Chi 2011, Xu 2011, Fan 2011]	
DC and Low-Frequency Rejection		0.1–1 Hz	AC coupling; with CDS or chopping for 1/f noise and offset reduction [Harrison 2003, Verma 2010, Fan 2011]	
Movement Artifact Rejection	\\\ <b>^</b> *\		Mostly reduction of relative motion through mechanical restraint [van Helleputte 2012, S. Kim 2012, H. Kim 2012]	
Area / Size	<b>\</b> √ <b>/</b>	0.1-10 cm <sup>2</sup>	Dominated by electrodes and battery; minimizing off-chip components [Yazicioglu 2008, Xu 2011, Muller 2011]	

▲: factors to be maximized; ▽: factors to be minimized

# 2.3.2 Design Factors, Inter-Relations, and Trade-Offs

Several factors quantifying metrics of performance and cost in the design, their inter-relationships, and typical ranges from the literature, are summarized in Table 2.2. Several of these relationships, such as between noise, power, bandwidth, gain, and dynamic range are generally well understood deriving from fundamental physical and information theoretic principles, e.g., power is typically linear in bandwidth but subject to noise considerations. Other relationships, such as be-

tween input impedance and movement artifact rejection, are specific to the physiological signals and environmental factors at the electrode interface. The various intertwined relationships between these factors must be co-optimized in the design trade-offs at the electrode, circuit, and architectural levels. A deep understanding of fundamental principles linking these factors and driving the trade-offs is thus required. Specific trade-offs and architectural design topologies that take advantage of properties of low-power CMOS integrated circuits and systems are elaborated in the following sections.

#### 2.3.3 Subthreshold Operation of MOS Transistors

Counter to standard practices in analog CMOS circuit design, the weak inversion (subthreshold) region of CMOS operation has proven a favorable regime for low-power biomedical circuit design. In conventional design, particularly for high-speed applications, weak inversion operation has been considered as non-ideality in a cut-off region and its current has been labeled as leakage current. Recently, weak inversion has become increasingly important because its low power and low bandwidth characteristics are well suited for biomedical and other low-power sensor applications, owing to superior transconductance efficiency. Also, it does not suffer from many process-dependent problems plaguing the above-threshold region in deep submicron technology, such as gain-limiting effects of velocity saturation in electron and hole mobility [258].

Transistor model equations in weak inversion are simpler, more transparent, and scale over a wider range than in strong inversion. The electron energy of a transistor in weak inversion is based entirely on the Fermi-Dirac distribution, independent of process technology. The drain current through the transistor channel flows not by drift, but by diffusion, and changes exponentially with gate voltage [326]. Drain current  $i_{DS}$ , transconductance  $g_m$  and unity-gain frequency  $f_t$  in weak inversion are as follows:

$$i_{DS} = i_{DS0} \frac{W}{L} e^{v_{GS}/(nV_t)} \left(1 - e^{-v_{DS}/V_t}\right)$$
 (2.1)

$$g_m = \frac{I_{DS}}{nV_t} \tag{2.2}$$

$$f_t = \frac{I_{DS}}{2\pi n V_t \left( C_{gs} + C_{gd} + C_{gb} \right)} \propto I_{DS}$$
 (2.3)

Because the transconductance is linearly proportional to drain current, so is unity-gain frequency. Thus, the trade-off between current and bandwidth is very straightforward: the larger the current, the wider the bandwidth.

Thermal noise in saturation and weak inversion is proportional to drain current as follows [327]:

$$\overline{i_{n,th}^2} = 2q\overline{I_{DS}}\Delta f \tag{2.4}$$

where  $\Delta f$  is the signal bandwidth. The relative noise power (inverse of the signal-to-noise ratio) is inversely proportional to drain current:

$$\frac{\overline{i_{n,th}^2}}{\overline{I_{DS}^2}} = \frac{2q\Delta f}{\overline{I_{DS}}} \tag{2.5}$$

Therefore, signal-to-noise ratio is linearly proportional to bias current in weak inversion. For a majority of biomedical applications with narrow signal bandwidth, the lower currents of circuits in weak inversion still offer adequately large signal-to-noise ratio at maximum energy efficiency.

Flicker noise, also known as 1/f noise or pink noise, is also a significant noise source at low frequency. Random captures of carriers in traps near the Si/SiO2 interface and some other mechanisms are known to be a main source of 1/f noise [257,399]. PMOS transistors are known to have less 1/f noise than NMOS transistors, and therefore should be used in the input differential pair of a frontend amplifier for low-noise low-frequency applications in biosensing. Enlarging the MOS device size also decreases 1/f noise inversely proportional to area. For low-noise biomedical applications such as EEG acquisition, chopper stabilization technique is widely used to reduce 1/f noise further (Sec. 2.3.6). Other techniques such as auto-zeroing and correlated double sampling can be used to reduce 1/f noise as well [100].

# 2.3.4 Instrumentation Amplifier Design

One of the most challenging parts in the design of wearable physiological monitoring system is the implementation of instrumentation amplifiers (IAs),

which acquire biosignals from electrodes and perform analog signal processing and conditioning. IAs are subject to almost all the challenging design specifications aforementioned in Sec. 2.3.2.

A classic three-opamp IA is adequate for achieving large input impedance, large CMRR and sufficient gain. However, it consumes large power and area [45] since it uses three amplifiers. For a micropower biopotential acquisition front-end, the configurations shown in Fig. 2.6 (a) (similar to [148]) and (b) (similar to [275]) are widely used. The ac-coupling input capacitors  $C_C$  block electrode offset voltages. Owing to favorable matching performance of capacitors in integrated CMOS processes, the gain can be precisely controlled. A large resistor  $R_f$ , typically implemented by a pseudoresistor or a switched-capacitor circuit (Sec. 2.3.5), establishes DC biasing of the voltage at the input nodes of the amplifier and performs highpass filtering together with  $C_f$ . Mismatch in capacitor values results in degradation of CMRR. A practical CMRR that this architecture can achieve is about 60 to 70 dB. In addition,  $C_C$  dominates the input impedance. Therefore, the value of  $C_C$  needs to be set by considering CMRR and the input impedance.

The passband gain is determined by the ratio of capacitors  $C_C$  to  $C_f$ . The highpass cutoff frequency is set by the product of  $R_f$  and  $C_f$ . The lowpass cutoff frequency is approximately  $g_m C_f/2\pi C_C C_L$ , which can be controlled by the load capacitor  $C_L$ . The right-half-plane zero at  $g_m/C_f$  can be cancelled by inserting a  $1/g_m$  resistor in series with  $C_f$ . However, it can be ignored in many cases because it is located at much higher frequency than the frequency range of interest for biomedical applications.

The main noise contributors of the single-stage IAs are the operational transconductance amplifier (OTA) and the feedback resistor  $R_f$ . In practical circuits, the noise from the OTA is dominant over the noise from  $R_f$  [147].

As a benchmark in the design of front-end IAs for low noise and low supply current, the noise efficiency factor (NEF) is used to compare the current-noise performance:

$$NEF = V_{rms,in} = \sqrt{\frac{2I_{tot}}{\pi V_t \cdot 4kT \cdot BW}}$$
 (2.6)

where  $V_{rms}$  is the total input-referred noise,  $I_{tot}$  the total current drain in the

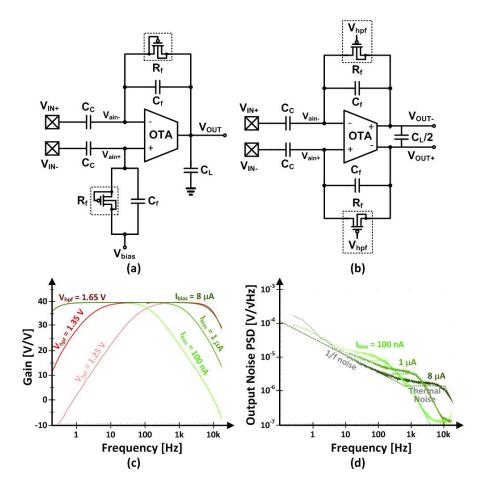


Figure 2.6: Generic architectures of (a) single-ended output [148], and (b) fully differential instrumentation amplifiers. Measured (c) transfer function and (d) output noise power spectral density for different configuration settings of the OTA bias current  $I_{bias}$  and pseudoresistance voltage bias  $V_{hpf}$  [275].

system,  $V_t$  the thermal voltage, and BW the -3-dB bandwidth of the system [362]. NEF corresponds to the normalized supply current relative to that of a single BJT with ideal current load for the same noise level, defining the theoretical limit (NEF = 1). In practice, differential IAs with input differential pairs incur twice the supply current for the same transconductance, with NEF values greater than 2. The state-of-the-art IAs typically have NEF of 2.5 to 10. As a point of reference, measured NEF and performance of state-of-the-art IAs are shown in Fig. 2.7 (a) and (b) respectively [94, 102, 148, 275, 287, 394, 404, 424, 425, 429, 442, 443, 449, 457, 465].

Note that even though NEF is widely used to benchmark IAs, NEF is nothing more but a trade-off between only three performance metrics: bandwidth, noise

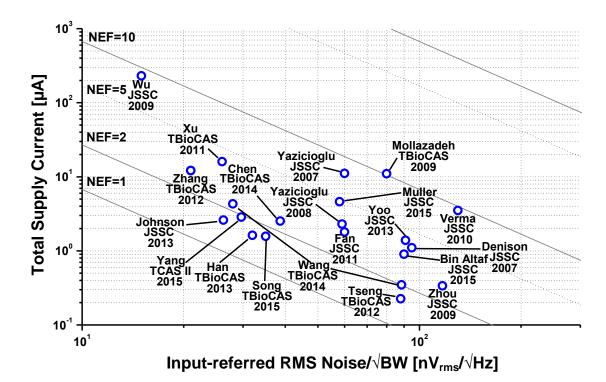
and current—excluding many other critical performance factors such as CMRR, input impedance, power consumption, input dynamic range, etc. Modified NEF metrics, one comparing power consumption instead of current [281], and another including power consumption and dynamic range [144], have been proposed as more comprehensive NEF alternatives.

#### 2.3.5 Pseudoresistors for Sub-Hz Highpass Cutoff

Highpass cutoff frequency needs to be well below 1 Hz in typical biomedical sensors, requiring ultra-high resistance in the  $T\Omega$  range. Realizing sub-Hz time constants with on-chip capacitors and poly resistors consumes an impractically large area for integrated implementation.

The most prevalent solutions are combinations of 1-10 pF capacitors with PMOS-based MOS-bipolar pseudoresistors as shown in Fig. 2.8 (a-f) [92,148]. The most basic topology among these is a PMOS whose gate and body terminals are connected as Fig. 2.8 (a) [92]. This PMOS pseudoresistor combines a pn-junction in the forward direction  $(V_A > V_B)$  with a diode-connected subthreshold PMOS in the reverse direction  $(V_A < V_B)$ . Owing to the source-bulk connection, the gate-connected drain terminal is leakage free and is ideally connected to a leakagesensitive side such as a floating input to an OTA. The measured resistance of a single MOS-bipolar pseudoresistor is shown in Fig. 2.8 (i) [148]. A configuration with the PMOS gate connected to a bias voltage in Fig. 2.8 (e), results in a controllable resistance by gate voltage [56, 144, 275, 297, 411]. However, the resistance of the PMOS-based pseudoresistors in Fig. 2.8 (a-e) drops drastically when the voltage across moves away from zero, inducing signal-dependent distortion while limiting the voltage dynamic range [465]. The pseudoresistor in Fig. 2.8 (f) has balanced resistance with wider linear range up to a few hundred mV. An even wider linear range can be achieved by using an auxiliary amplifier [341].

However, standard MOS-bipolar pseudoresistors suffer from process, voltage and temperature (PVT) variations in addition to possible light and electromagnetic interference sensitivities, leading to variations in cutoff frequency. Switched capacitors can be used to implement on-chip PVT-insensitive high resistance as shown



(a)

	Xu TbioCAS 2011	Yazicioglu JSSC 2008	Zou JSSC 2009	Verma JSSC 2010
Application	Neural	EEG	Multimodal	EEG
VDD [V]	5	3	1	1
Power [mW]	80	6.9	0.337	3.5
Bandwidth [kHz]	7.2	28k	0.292	100
Low-Frequency Cutoff [Hz]	0.025	0.5	0.005 - 3.6	0.5
Input-Referred	1.6	0.59	2.5	1.3
Noise [mV <sub>rms</sub> ]	(0.025 – 7.2k Hz)	(0.5 - 100 Hz)	(0.05 - 292 Hz)	(0.5 - 100 Hz)
NEF	4.0	4.3	3.26	N/A
CMRR [dB]	≥ 83	> 120	≥ 71.2	> 60
PSRR [dB]	≥ 85	> 89	≥ 84	N/A
Input Impedance [MΩ]	N/A (~ 20 pF)	> 1000	N/A (~ 8 pF)	> 700
Area [mm²]	0.16	0.45	> 0.5	0.3

(b)

Figure 2.7: (a) Noise efficiency factor and (b) performance summary of state-of-the-art IAs for non-invasive biomedical applications

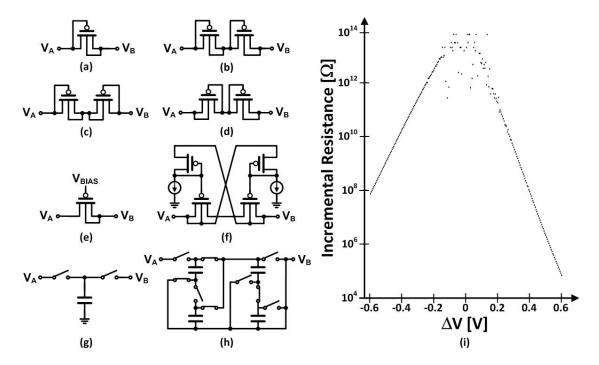


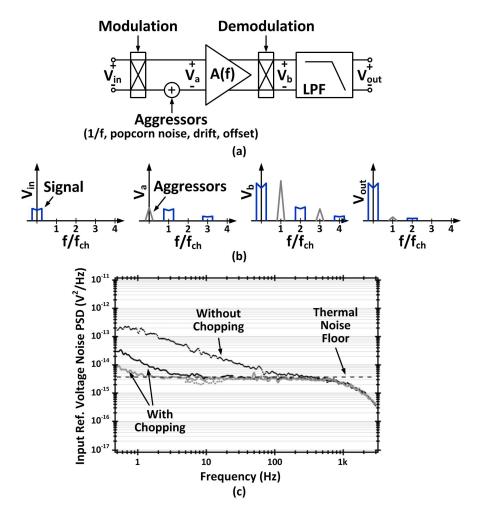
Figure 2.8: On-chip pseudoresistor implementations: (a) single MOS-bipolar pseudoresistor [92]; (b) pseudoresistor with two MOS-bipolar elements in series for twice higher resistance and greater voltage range [39, 148]; (c) symmetrical version with outwardly connected gates; (d) symmetrical version with inwardly connected gates [424,429,458]; (e) voltage-biased pseudoresistor for resistance tunability [56,144,275,297,411]; (f) balanced tunable pseudoresistor with wider linear range [465]; (g) switched-capacitor implementation [94]; (h) switched-capacitor implementation with 10-times larger effective resistance than (g) [404]. (i) Measured resistance of a single MOS-bipolar pseudoresistor (a) as a function of voltage [148].

in Fig. 2.8 (g) [94]. In this topology, switching frequency  $f_s$  and the capacitor in the middle determine the resistance precisely as  $1/f_sC$ . The switched-capacitor resistor in Fig. 2.8 (h) mitigates manufacturability and interference issues by realizing a 10 fold resistance increase by charge sharing in the switched-capacitor circuits [404].

## 2.3.6 Offset and 1/f Noise Cancellation Techniques

Autozeroing switched-capacitor techniques are often used to suppress electrode voltage offset and 1/f noise of the amplifier [100]. However, opening of the reset switch on the sampling capacitor after autozeroing introduces significant

Nyquist-Johnson noise (kT/C noise) [179, 293] and random charge injection that contaminate the sampled signal. The kT/C noise of a 1-10 pF capacitance alone is about tens of  $\mu\text{V}$ . To resolve this noise issue referred to the input of the AFE, signal folding and digital-assisted signal stitching can be used, resulting in relieving the specification of voltage dynamic range [62]. Instead, almost all of the IAs utilize chopper stabilization techniques to obviate 1/f noise.



**Figure 2.9**: (a) Block diagram and (b) frequency-domain illustration of the chopper technique for low-frequency noise and drift cancellation [100,101,159,260]. (c) Input-referred noise spectrum with and without chopping [442].

#### Chopper stabilization techniques

The chopper modulation technique is widespread and essential to mitigate 1/f noise and other low-frequency noise, such as popcorn noise, voltage offsets and drifts, for EEG and other low-noise ( $< 1\text{-}2~\mu V_{rms}$  input-referred noise) biopotential acquisition. The principles of the chopper modulation technique for amplifiers, which have been extensively studied [100,101,159,260], are illustrated in Fig. 2.9. The low-frequency band-limited input signal  $V_{in}$  is modulated in front of the amplifier by a square-wave chopping signal. The resulting waveform  $V_a$  for the signal is shifted to the chopping frequency  $f_{ch}$ , and the aggressors do not fall within the signal band. After the amplification and demodulation with the same chopping signal, the amplified input signal components are shifted to DC baseband frequency at  $V_b$  while the aggressors are moved to  $f_{ch}$  outside of the signal band. All the undesired aggressors and the harmonics are filtered out through the low-pass filter, and the desired input signal is ideally restored at the output  $V_{out}$ .

The residual offset is mainly caused by the non-idealities of the input chopper modulator. The mismatch of the clock-feedthrough and the charge injection in the input chopper generates switching transient spikes, which are demodulated at the output chopper into a residual output offset. In order to minimize the offset, at first, careful design and layout need to be done. A continuous [94,404,425,443] or digital [429] DC servo-loop can reduce the residual offset, and mitigate the signal distortion problem that is caused by the finite bandwidth of the amplifier. Alternatively, filtering techniques [46,261,442] can be applied. Output ripple is induced by the input offset of the amplifier, and can saturate the output of the amplifier since offset is also amplified. The ripple can be reduced by a continuous ripple-reduction loop [425] and a digital foreground calibration [429].

#### 2.3.7 CMRR Enhancement Techniques

Common-mode interference is a difficult challenge for biomedical signal sensing systems. The major source of the interference comes from electric power lines, which are electrically coupled to the human body. High CMRR is required in the system to reject the common-mode interference in order to ensure high signal quality.

Accurate component matching between differential signal lines and between the channels is the most fundamental requirement to accomplish high CMRR. Good matching involves techniques from careful layout to smart architectural design choices.

#### Driven right leg technique

The DRL technique feeds the amplified input common-mode voltage into the body through an additional electrode, which has been placed on the right leg for ECG measurements. This negative feedback reduces the impedance in the feedback loop, attenuating the common-mode interference voltage at the sensor inputs [420, 421] by factor of the feedback loop gain. Through the DRL negative feedback, the electrode impedance and common-mode voltage are reduced by the factor of the DRL loop gain. Hence in order to obtain higher gain, an open-loop DRL amplifier can be employed [103]. Digitally assisted DRL circuits offer larger gain at the mains frequency for higher rejection and lower gain elsewhere for stability [142]. In dry electrode applications, common-mode feedback to the negative inputs of individual amplifiers on the active electrodes also increases CMRR, and ensures stability unaffected by electrode impedance variations [429].

#### Input impedance boosting techniques

The variation and mismatch of electrode impedances also degrade CMRR, reduce signal amplitude, and make the system more susceptible to movement artifacts. Thus, the input impedance of the biopotential sensor should be much higher than the electrode impedance and the interface impedance between the body and the electrode. A positive feedback can bootstrap the AC-coupled input capacitors to boost the input impedance [102, 401, 429], achieving input impedance in the order of  $G\Omega$ . In order to further boost input impedance to the  $T\Omega$  level, a unity-gain amplifier with active shielding can be used to bootstrap capacitance of the input transistor and all other parasitic capacitance [71].

#### 2.3.8 Impedance Measurement

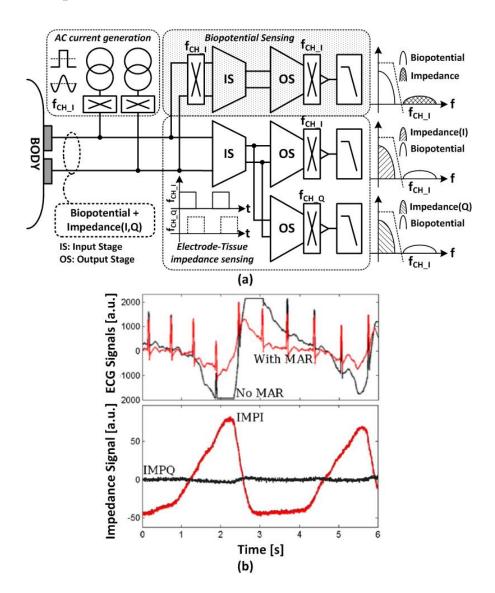


Figure 2.10: Electrode-tissue impedance measurement concurrent with biopotential recording. (a) Periodic current injection and synchronous detection of resistive and reactive components of impedance along with the chopped biopotential signal. (b) Movement artifact reduction (MAR) in ECG signal through linear correction with the estimated impedance signals [401].

Movement artifacts can be suppressed by sensing electrode-tissue impedance and biopotentials simultaneously. In Fig. 2.10. (a), a AC current generation block with a chopper injects AC current into the sensing electrodes [211,401,441]. Due to the electrode-tissue impedance, voltage signals including the impedance informa-

tion are superimposed on the original biopotentials. Note that the electrode-tissue impedance has resistive and capacitive components resulting in real and imaginary components, respectively. All signals are directed to readout circuits. To separate biopotential and impedance signals, only the IA for biopotentials has a chopper at its input. For distinguishing real and imaginary parts in impedance signals, the output chopper blocks use two phases in quadrature,  $f_{CH_{-}I}$  and  $f_{CH_{-}Q}$ . The IA with  $f_{CH_{-}Q}$  projects the voltage corresponding to the electrode reactance into the low-frequency band while other signal components are either canceled or projected to high frequencies and subsequently rejected by low pass filters, such that only signals in low-frequency band are shown at the output [211, 401, 441].

A purely sinusoidal current generator for impedance probing without a chopper block is reported in [434]. Due to large power consumption of the sinusoidal AC current source, a simple pulse-wave current source is implemented in [211,441,443]. However, since a pulsed current contains large higher harmonics that get folded into baseband, it leads to 23% measurement error. To avoid large power consumption and harmonic distortions, a 16-level quantized-sinusoidal current source is proposed in [210].

The sensed signals by the circuit structure in Fig. 2.10 (a) are the input of an adaptive filter with a LMS algorithm [47,211]. Fig. 2.10 (b) clearly shows that this method is able to reduce the effect of movement artifacts with the estimated impedance signals shown in Fig. 2.10 (c) [401].

# 2.3.9 Optics-based Sensing

Pulse oximetry is accomplished by spectrophotometric measurement of the relative absorbances of arterial blood to red and infrared light. The absorbance of the background tissue and other interferences are rejected by sampling several times throughout the period of a heartbeat, while the amount of blood that perfuses the probed area varies. The actual physical quantity observed is the ratio of the red over the IR contrasts, where contrast is defined as the quotient of the AC amplitude over the DC magnitude of the current generated at the photodiode for each color. Once this ratio is computed, blood oxygen saturation can be

computed with a simple formula [326]. The general architecture of a pulse oximeter includes a probe, a photoreceptor, analog signal conditioning, and a digital processor and controller [125]. The probe consists of the two LEDs that generate the monochromatic signals, along with drivers, switching and pulse modulation circuitry. The photoreceptor consists a photodiode to sense the incoming light and a transimpedance amplifier (TIA) to amplify and convert the current driven by the sensor into a voltage. Consequently, analog lowpass filtering removes artifacts from the switching and pulsing of the probe light, which is generally much faster than the pulse signal of interest. Finally, the ratio between the red and IR signals (which can come in parallel channels) can be computed in analog domain before digitization.

Integrated circuit advances in photoplethysmography have dramatically decreased the power consumption of these devices. An ultra-low power version of a whole system can consume 4.8 mW, or last 60 days on 4 AAA batteries [376]. This is possible by reducing the duty cycle of the probe LEDs, by an innovative logarithmic TIA with adaptive filtering and gain and by analog ratio computation. Imaging brain activity with fNIRS systems has a similar architecture with pulse oximetry. Advances include integration of silicon avalanche photodiodes in the photoreceptor IC, along with a linear TIA for very low noise and high gain detection [186]; and improvements in the spatial and temporal resolution of multichannel systems by code-division-multiple-access (CDMA) modulation of different emitters and detectors [72].

# 2.4 Signal Coding and Digitization

Digitization of the recorded and processed analog physiological signals is required for further digital signal processing and digital RF communication. The tight power and low noise constraints demand ultra-low power ADCs at low frequency range (1-10 kHz) without sacrificing noise performance, while requiring no or very little static current drain and scalable power consumption with respect to sampling rate for multi-modal recording applications. Both successive-

approximation ADC and oversampling  $\Delta\Sigma$  ADC are superior architectures for achieving the specifications with lowest power dissipation.

#### 2.4.1 Successive-Approximation ADC

Successive-approximation register (SAR) ADC is the dominant architecture for low-power medium-resolution (8-12 bits) biomedical applications due to its simple architecture involving few analog circuits and its low power consumption at low frequency without static power consumption [194, 230, 271, 401, 403, 436, 443, 449, 465]. Successive approximation of the sampled input performs a binary search over the input range using a time-multiplexing switched-capacitor digital-to-analog converter (DAC) based on iterative partial one-bit quantization results in the order from the most significant bit (MSB) to the least significant bit (LSB) [256, 367].

Several techniques and architectures can be applied to minimize power consumption of the SAR ADC. Using a main and sub binary weighted DAC arrays with a series attenuation capacitor can reduce the total size of the capacitor array; leading to reduced power consumption in the ADC driver and also in the capacitor DAC [11]. Also, the folded capacitor DAC architecture with divided reference voltages reduces the size of capacitor DAC, resulting in further power saving [436]. Using charge-recycling switching methods results in further power savings in the switching of the capacitor DAC [124].

SAR ADCs are generally considered to be most energy efficient for medium-precision low-sampling-rate digitization. However, most micropower SAR ADCs operate at signal levels substantially (3-4 orders of magnitude) greater than typical signal level of physiological signals (Fig. 2.5). They require significant amplification before analog-to-digital conversion for sub- $\mu$ V resolution. Furthermore, sampling at the Nyquist frequency demands substantially more stringent anti-aliasing analog filtering than required using oversampling techniques. The cost of amplification and anti-aliasing filtering are often not accounted for in ADC energy metrics. Most critically, sampling of biosignals at  $\mu$ V resolution is problematic due to kT/C sampling noise on capacitors which may amount to several tens of  $\mu$ V for typical pF-range capacitors in integrated circuits.

#### 2.4.2 $\Delta\Sigma$ Oversampling ADC

 $\Delta\Sigma$  ADCs are an alternative solution with the following strengths [66, 86, 118, 140, 275]: 1) Resolution and sampling rate can be dynamically reconfigured, with sampling rate proportional to power consumption, so they are adequate for multimodal biopotential sensor applications; 2) They require only few and simple analog components; 3) They are suited for low-power and low-voltage operation; 4) They easily achieve 12-16 bits or higher resolution without complex circuit and layout techniques; 5) Continuous-time  $\Delta\Sigma$  topologies are free of kT/C sampling noise and less subject to aliasing and noise folding.

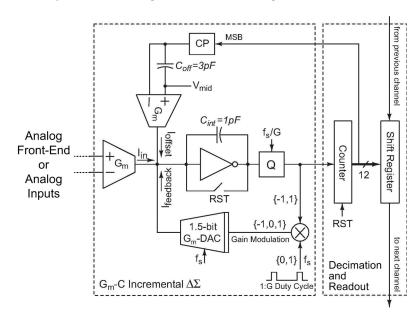


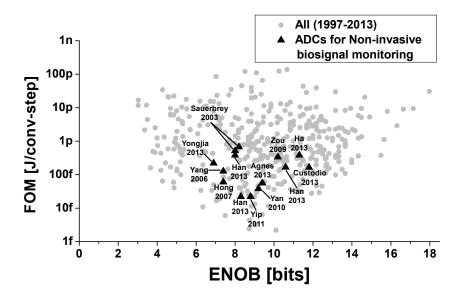
Figure 2.11: An oversampling, aliasing-free biopotential acquisition system utilizing Gm-C incremental  $\Delta\Sigma$  ADC [275].

A Gm-C incremental  $\Delta\Sigma$  ADC with widely configurable resolution and sampling rate is shown in Fig. 2.11 [275]. A transconductance  $(G_m)$  cell converts the differential input voltage signal to a current, approximately linear over the voltage range of typical biopotentials. The difference between this current and a feedback current is integrated and the resulting voltage is compared for three-level quantization of the feedback current, implementing a continuous-time first-order  $\Delta\Sigma$  modulator. A continuous-time oversampling ADC avoids the need for anti-aliasing filter and sample-and-hold circuits preceding the ADC. In addition,

direct digital control over duty cycle in the feedback offers precise digital gain programmability from 1 to 4,096.

Another example incremental  $\Delta\Sigma$  ADC for non-invasive biopotential recording is given in [66]. It receives unbuffered biopotential signals and performs amplification, signal conditioning, and digitization using only a single OTA. Other alternative ADC architectures include a hybrid architecture of SAR and  $\Delta\Sigma$  ADC [140], asynchronous level-crossing ADCs [374,447] and a bio-inspired ADC with the successive integrate-and-fire operation [438].

The performance of ADCs can be measured and compared by the Walden figure-of-merit (FOM), which quantifies energy consumed per conversion step as  $Power/(2^{ENOB}f_S)$ . Fig. 2.12 shows this FOM for all major ADCs reported from 1997 to 2013 [284] including ADCs for non-invasive physiological monitoring systems. [11,86,140,144,157,329,403,436,438,445,447,465].



**Figure 2.12**: Figure of merit (FOM) vs. effective number of bits (ENOB) of the state-of-the-art ADCs for biomedical applications.

# 2.4.3 Application-Specific Signal Encoding

Digital signal processing (DSP) compressed encoding of the digitized data prior to RF wireless transmission may lead to substantial energy savings, particularly in high-dimensional or high-bandwidth physiological sensing applications where the amount of useful information is significantly lower than the data rate requirements of the raw signals. For example, in EEG sensing for epileptic seizure detection [404, 449], 18 electrodes produce 200-Hz 12-bit data resulting in a total data rate of 43.2 kbps. Employing digital processing for feature extraction and seizure detection reduces this data bandwidth to 2 kbps with a 10-fold reduction in power dissipation [404].

Equally importantly, energy-efficient analog preprocessing can lead to significant reduction of data bandwidth and power in the ADC in addition to the RF block. A low-power ADC and digital blocks can substitute a high performance ADC and digital signal processor. For example, typical EEG/ECoG-based brain-computer interface (BCI) applications do not need raw data, but spectral characteristics of the recordings. Thus, extracting spectral power of the required frequency bands in the AFE can reduce power dissipation and/or complexity in the ADC, DSP and RF blocks [458]. Other applications of analog and mixed-signal preprocessing for low-power high-performance biosignal processing include ECG physiological monitoring systems for efficient QRS detection and coding [271,441].

# 2.5 Architectural Design for Low-power Biopotential Acquisition

System-level architectural design may lead to significant advances in minimizing power consumption without compromising performance. Block-level design approaches should be considered before optimization within each block. This section reviews architectural design choices for low-power biopotential acquisition with some examples.

# 2.5.1 Architectural Design Strategies

An intelligent choice for functional block allocation in a system can result in significant improvements in power consumption and performance of the whole system. A typical architecture of wearable biopotential sensors comprises an analog front-end, a digital signal processor, an ADC between the two, an RF transmitter and a power harvesting and management unit as shown in Fig. 2.13.

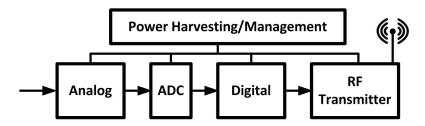


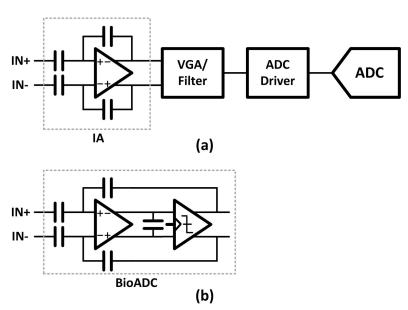
Figure 2.13: General architecture for wireless biopotential acquisition.

Preprocessing inside of the sensor is more favorable than transmitting all raw data out, particularly in high-dimensional or high-bandwidth sensor applications where the amount of useful information may be significantly lower than the data rate requirements of the raw signals. Transmitting the processed data instead of all raw data reduces power consumption in the RF transmitter considerably. In the aforementioned example of seizure detection in EEG sensing, 18 electrodes produce 200-Hz 12-bit data resulting in a total data rate of 43.2 kbps. Employing digital processing for feature extraction and seizure detection reduces the data bandwidth to 2 kbps with a 10-fold reduction in power dissipation [57, 147].

Equally importantly, energy-efficient analog preprocessing can lead to significant reduction of data bandwidth and power in the ADC and the digital block. A low-power ADC and digital blocks can substitute a high performance ADC and digital signal processor. For example, typical EEG/ECoG-based brain-computer interface applications do not need raw data, but spectral characteristics of the recordings. Thus, extracting spectral power of the required frequency bands in analog front-end can reduce power dissipation and complexity in the other blocks [458]. There are many other kinds of analog preprocessing for low-power high-performance biosignal processing such as the QRS detection in ECG [271].

Manipulating functional positioning within the analog block is also very important to maximize the performance while minimizing the power consumption. There are various block-level designs in the analog domain for each application-

specific requirement. Separating functions into each block can optimize each function respectively and maximize programmability on gain and bandwidth [45]. Fig. 2.14 (a) shows such an architecture comprising an instrumentation amplifier, a variable-gain/bandwidth amplifier and an ADC driver, which is connected to an ADC. In contrast to the separation of all functions into each block, the other extreme alternative is an architecture combining all of analog signal conditioning function and analog-to-digital conversion into one block as shown in Fig. 2.14 (b). This architecture removes unnecessary power consumption in the VGA/filter stage and the ADC driver. In addition, it achieves digital controllability in gain and bandwidth by changing duty cycle of integration clock and over-sampling ratio [66].



**Figure 2.14**: Alternative signal acquisition architectures. (a) Standard modular approach with isolated blocks for amplification, filtering, and ADC. (b) Hybrid architecture combining all functions into a single analog block including embedded ADC [66].

#### 2.5.2 Power Domain Design

How the power domains are designed in a system may contribute more to power savings in system performance than improvements by circuit techniques. In most wearable sensors, power is harvested in various ways or supplied from a battery. In any case, the amount of the power is very limited. Therefore, power should be managed wisely. The first step of power management is to design power domains in the system.

Having only one lowest possible power supply in the system is most preferable and does not involve complicated power management schemes and level shifts. However, having different kinds of power levels can be more beneficial in order to reduce the power consumption further. Each block may require different supply voltage VDD. A block with narrower voltage dynamic range can operate with a lower VDD, resulting in lower power. Higher VDD is necessary for blocks requiring a wide dynamic range. In addition, higher VDD is favorable for better performance in some applications such as a switch, which requires lowest possible turn-on resistance [303]. In a system with multi-power domains, more careful design is required at the interfaces where different power levels meet. Many techniques such as level shifting, AC-coupling, etc., can be utilized at the interface.

There are several ways to design multi-power domains. 1) A multiple of power levels can be generated directly from the power-harvesting circuit [59]. This method meets different VDD requirements of different blocks and optimizes the power consumptions. However, it requires more complex design in the energy-harvesting block. 2) Multiple power levels can be generated by regulators from a high VDD, which is scavenged or supplied from a battery. This approach can decrease current consumption in some blocks, but the headroom is still wasteful. 3) Contrary to the method 2), some higher voltages can be generated from a lower voltage using a power management unit (PMU) such as a charge pump. It can be optimized in terms of power consumption. However, it may induce more complexity because of adding a PMU block [144].

# 2.6 System Examples

Examples of complete non-invasive physiological monitoring systems covering a range of cardiac, respiratory, muscular, and brain activity signals under a variety of environmental conditions, including underwater and non-contact sensing,

are given below. Application-specific design of the electrode interfaces contribute to extend the applicable scope to ambulatory monitoring outside of the hospital.

#### 2.6.1 Non-contact ECG Bed

One highly promising application of non-contact capacitive electrode interfaces is ECG monitoring embedded in beds [238, 395, 397, 398]. Integration of electrodes underneath a commercial bed sheet (e.g. Fig. 2.15) enables non-contact electrode coupling, through thin common nightwear, to a subject lying on the bed. This implementation relieves the user not only of skin irritation but also of cumbersome electrode attachment, connecting to ambient health monitoring and increased patient compliance for every night use. Combined monitoring of ECG with breathing activity also extends the application area to neonatal supervision [396,433] and sleep apnea screening. The breathing signal is obtained by capacitive sensing of displacement using the same capacitive coupling electrode used for ECG sensing.

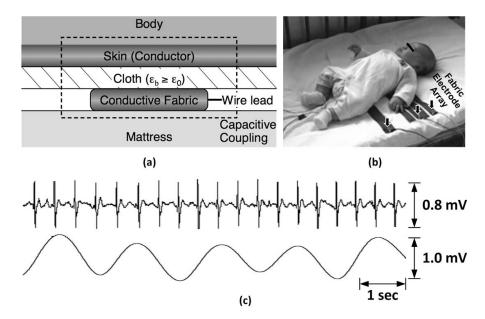
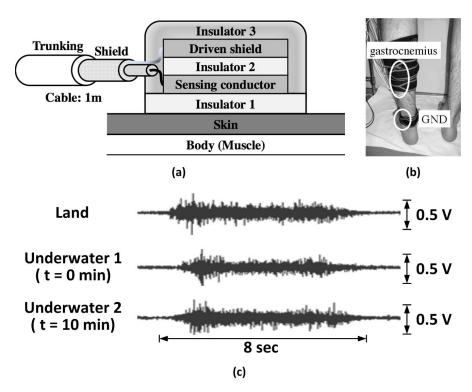


Figure 2.15: Example of non-contact electrode interface for monitoring ECG and breathing on bed. (a) Fabric electrode placed on a bed and coupled indirectly to the skin [395]. (b) Fabric bed electrodes placed on a bed for monitoring ECG and breathing activity [398]. (c) Signal recording of narrow-band ECG (top) and simultaneously measured breathing activity (bottom) [396].

#### 2.6.2 Underwater EMG Sensing

Another novel application of the insulated capacitive electrode interface is underwater EMG monitoring [296]. Coating the electrodes with a thin water-proof insulating material (e.g. Fig. 2.16) prevents them from short-circuiting due to ions in water, and hence enhances the selectivity of the electrode coupling to the physiological voltage source (i.e. muscles in [296]) even in the case where the target source is immersed in conductive liquid.



**Figure 2.16**: Example of insulated electrode interface for measuring underwater EMG. (a) Schematic of electrode configuration coated wholly with hydrophobic insulator, (b) electrode placement and (c) measured EMG signal from gastrocnemius muscle during plantar flexion with the electrode in (a) [296].

# 2.6.3 Wearable ECG and EEG Systems

Mobile applications of wireless non-invasive physiological sensing include wearable systems for continuous ambulatory biopotential monitoring, made possible by advancements in electronics miniaturization, low noise dry sensors and innovative mechanical form-factors. Fig. 2.17 show two examples of ECG and EEG systems.

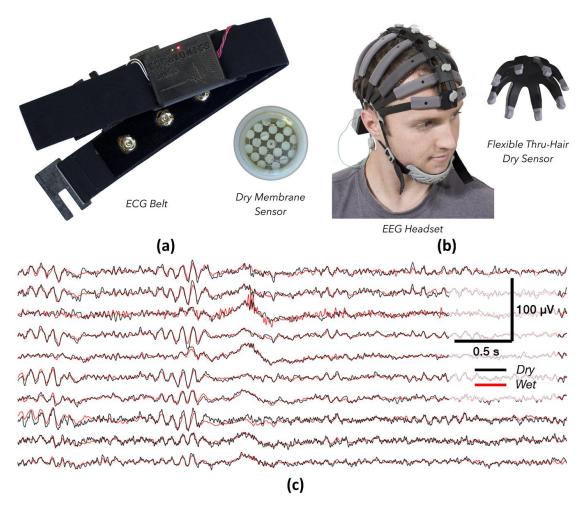


Figure 2.17: Examples of wearable dry electrode systems. (a) Dry contact ECG belt with low noise membrane-based sensor [78]. (b) High density dry EEG head-set with flexible electrodes that can operate through hair [79]. (c) Simultaneous recording between wet (Ag/AgCl conductive gel) and the dry EEG headset showing the high signal quality [79].

The ECG belt utilizes a linear array of membrane based dry contact sensors. Unlike conventional metal based electrodes, the membrane signal utilizes a semi-permeable surface which encapsulates a hydrogel. The membrane allows for ionic conduction between the body, through the membrane and into the hydrogel. This buffers the electrochemical interface by providing a stable gel-metal layer away from the skin and reduces the sensor noise [78].

For EEG, head hair presents a challenge for dry electrodes which must reach the scalp. A flexible electrode is made from an elastomeric material which bends to brush aside hair and avoids the need for hard metallic prongs. An array of flexible sensors (up to 64) is placed within a mechanical headset that is adaptable to variety of head shapes and sizes. All of the AFE, ASP, ADC, DSP, and RF electronics are integrated onto the headset enabling mobile EEG acquisition [79].

#### 2.7 Conclusion

The advent of ubiquitous wearable physiological monitoring promises to reduce some of the rising healthcare costs affecting developed and developing nations. Customized applications bring opportunities for better preventive care and increasing public awareness of their own medical conditions. In this paper we focused on the integrated circuit techniques to improve the performance and expand the applications of non-invasive physiological monitoring instrumentation and discussed the challenges at the electrode-body interface. From these interface considerations we developed system requirements for reliable signal acquisition in biopotential, electrode-tissue impedance and spectrophotometric measurements. Some of the main techniques for implementing CMOS subthreshold integrated instrumentation amplifiers in a low-noise and power-efficient manner were covered: pseudoresistors, chopping, driven right leg circuits, impedance bootstrapping, and application-specific design for electrode-tissue impedance measurements and photoplethysmography. Highly efficient data conversion and signal encoding for digital transmission were also reviewed. Finally, examples of wearable and unobtrusive systems for physiological monitoring in novel applications were presented. These innovations, and others to come in the next decade, will continue to benefit from interdisciplinary collaborations between developers and users of the non-invasive physiological monitoring technology such as: new physiological signal modalities; innovative electrode interfaces; improvements in integrated circuit design methodologies and silicon technologies; improved system-level design optimizing for human factors and ergonomics; and clinician and patient perspectives on medical diagnostics and personal healthcare.

Chapter Two is largely a combination of material in the following two venues: Sohmyung Ha, Chul Kim, Yu M. Chi, Abraham Akinin, Christoph Maier, Akinori Ueno and Gert Cauwenberghs, "Integrated Circuit and Electrode Interfaces for Non-Invasive Physiological Monitoring," *IEEE Transaction on Biomedical Engineering*, Vol.61, No.5, pp.1522-1537, May 2014. Sohmyung Ha, Chul Kim, Yu M. Chi, and Gert Cauwenberghs, "Low-Power Integrated Circuit Design for Wearable Biopotential Sensing," *Wearable Sensors: Fundamentals, Implementation and Applications* (Edward Sazonov and Michael Neuman Ed., ISBN: 978-0-12-418662-0), *Elsevier*, pp. 323-352, September 2014. The author is the primary author and investigator of this work.

# Chapter 3

# Silicon Integrated Electrocortical Interfaces

#### 3.1 Introduction

The Brain Research through Advancing Innovative Neurotechnologies (BRAIN) Initiative envisions expanding our understanding of the human brain. It targets development and application of innovative neural technologies to advance the resolution of neural recording, and stimulation toward dynamic mapping of the brain circuits and processing [378, 379]. These advanced neurotechnologies will enable new studies and experiments to augment our current understanding of the brain, thereby enabling tremendous advances in diagnosis and treatment opportunities over a broad range of neurological diseases and disorders.

Studying the dynamics and connectivity of the brain requires a wide range of technologies to address multiple temporal and spatial scales. Fig. 3.1 shows spatial and temporal resolutions and spatial coverage of the various brain monitoring methods that are currently available [114, 153, 290, 314].

Noninvasive methods such as magnetic resonance imaging (MRI), functional magnetic resonance imaging (fMRI), magnetoencephalography (MEG), and positron emission tomography (PET) provide whole-brain spatial coverage. Although fMRI achieves high spatial resolution down to 1 mm, its temporal resolu-

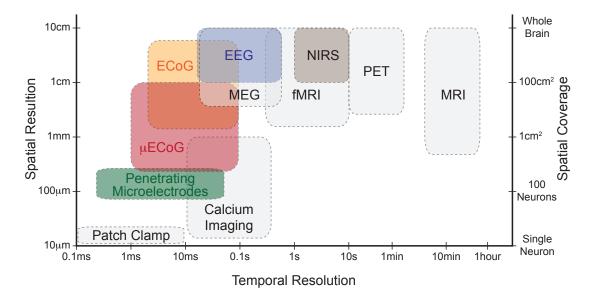


Figure 3.1: Spatial and temporal resolution as well as spatial coverage of various neural activity monitoring modalities [114,290,314]. For each modality shown, the lower boundary of the box specifies the spatial resolution indicated on the left axis, whereas the upper boundary specifies the spatial coverage on the right axis. The width of each box indicates the typical achievable range of temporal resolution. Portable modalities are shown in color. Bridging an important gap between non-invasive and highly invasive techniques,  $\mu ECoG$  has emerged as a useful tool for diagnostics and brain-mapping research.

tion is severely limited (1-10 s) as the system measures neural activity indirectly by quantifying blood oxygenation to support regions with more elevated metabolism. In contrast, MEG provides higher temporal resolution (0.01-0.1 s) at the expense of poor spatial resolution (1 cm). Whereas fMRI and MEG provide complementary performance in spatiotemporal resolution, PET offers molecular selectivity in functional imaging at the expense of lower spatial (1 cm) and temporal (10-100 s) resolution, and the need for injecting positron emitting radionuclides in the blood-stream. However, neither fMRI, MEG or PET are suitable for wearable or portable applications, as they all require very large, expensive, and high power equipment to support the sensors as well as extensively shielded environments.

In constrast, electrophysiology methods, which directly measure electrical signals that arise from the activity of neurons, offer superior temporal resolution. They have been extensively used to monitor brain activity due to their ability to capture wide ranges of brain activities from the subcellular level to the whole brain oscillation level as shown in Fig. 3.2 (a). Due to recent advances in electrode and integrated circuit technologies, electrophysiological monitoring methods can be designed to be portable, with fully wearable or implantable configurations for brain-computer interfaces having been demonstrated.

One of the most popular electrophysiological monitoring methods is electroencephalography (EEG), which records electrical activity on the scalp resulting from volume conduction of coherent collective neural activity throughout the brain, as illustrated in Fig. 3.2 (a). EEG recording is safe (non-invasive) and relatively inexpensive, but its spatiotemporal resolution is limited to about 1 cm and 100 Hz, due largely to the dispersive electrical properties of several layers of high-resistive tissue, particularly skull, between the brain and the scalp. In contrast, recording with intracranial brain-penetrating microelectrodes (labelled as EAP+LFP in Fig. 3.2 (a)) can achieve much higher resolution due to the much closer proximity to individual neurons. Thus, it is also widely used for brain research and braincomputer interface (BCI) applications. Using microelectrodes, extracellular action potential (EAPs) and local field potentials (LFPs) can be recorded from multiple neurons across multiple cortical areas and layers. Even though penetrating microelectrodes can provide rich information from neurons, they can suffer from tissue damage during insertion [187, 226, 255], and have substantial limitations in longterm chronic applications due to their susceptibility to signal degradation from electrode displacement and immune response against the electrodes [308]. Because of the more extreme invasiveness and longevity issues, chronic implantation of penetrating microelectrodes in humans is not yet viable.

Between the two extremes of EEG and penetrating microelectrode arrays, a practical alternative technique is electrocoticography (ECoG), or intracranial / intraoperative EEG (iEEG), which records synchronized postsynaptic potentials at locations much closer to the cortical surface, as illustrated in Fig. 3.2 (a). Compared to EEG, ECoG has higher spatial resolution [111, 231, 349], higher signal-to-noise ratio, broader bandwidth [360], and much less susceptibility to artifacts from movement, electromyogram (EMG), or electrococulargram (EOG) [26, 110].

In addition, ECoG does not penetrate the cortex, does not scar, and can have superior long-term signal stability recording through subdural surface electrodes.

ECoG recording was pioneered in the 1920s by Hans Berger [31]. He recorded ECoG signals with electrodes placed on the dural surface of human patients. In the 1930s through 1950s, Wilder Penfield and Herbert Jasper at the Montreal Neurological Institute used ECoG to identify epileptogenic zones as a part of the Montreal procedure, which is a surgical protocol to treat patients with severe epilepsy by removing sections of the cortex most responsible for epileptic seizures. In addition, intraoperative electrical stimulation of the brain has been used to explore the functional mapping of the brain including brain areas for speech, motor, and sensory functions. This localization of important brain regions is important to exclude from surgical removal. Although ECoG is still the gold standard for decoding epileptic seizure foci and determining target regions for surgical removal, the role of ECoG has been reduced due to recent advances in imaging techniques for functional brain mapping such as fMRI, PET, and MEG.

With advances in high channel count and wireless operation, however, ECoG has again emerged as an important tool not only for more effective treatment of epilepsy, but also for investigating other types of brain activity across the cortical surface. ECoG recording provides stable brain activity recording at a mesoscopic spatiotemporal resolution with a large spatial coverage up to whole or a significant area of the brain. Advanced miniaturized electrode arrays have pushed the spatial resolution of ECoG recording to less than 1 mm, offering a unique opportunity to monitor large-scale brain activity much more precisely. Moreover, wireless implantable microsystems based on flexible technology or via modular placement of multi-channel active devices, both illustrated in Fig. 3.2 (b), have recently emerged as a new paradigm to record more closely to the cortical surface (in many cases on top of the pia), while enabling coverage along the natural curvature of the cortex without penetration. These micro ECoG, or  $\mu$ ECoG, devices enable even higher spatial resolution than conventional ECoG systems, and are beginning to enable next-generation brain mapping, therapeutic stimulation, and BCI systems.

This paper discusses the challenges of designing next-generation ECoG in-

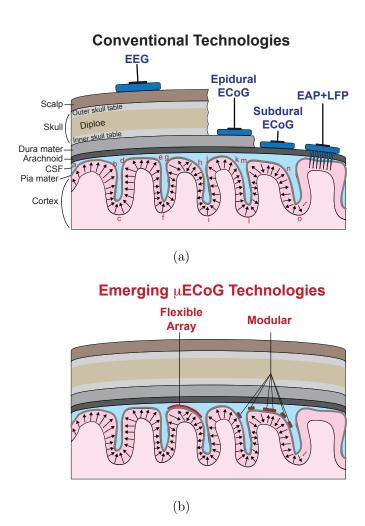


Figure 3.2: (a) Conventional electrophysiology methods including electroencephalography (EEG), electrocoticography (ECoG) and neural spike and LFP recording with penetrating microelectrodes. Both EEG and ECoG can capture correlated collective volume conductions in gyri such as regions of a-b, d-e and j-k. However, they cannot record opposing volume conductions in sulci such as regions of b-c-d and e-f-g and random dipole layers such as regions of g-h and l-m-n-o [292]. (b) Emerging fully implantable  $\mu$ ECoG technologies enabled by flexible substrate ECoG microarrays and modular ECoG interface microsystems. Such technologies are capable of capturing local volume conducting activities missed by conventional methods, and are extendable to cover large surface area across cortex.

terfaces, including recording, miniaturization, stimulation, powering, and data communications. Solutions are presented by first surveying state-of-the-art technologies, and then through a detailed exploration of a state-of-the-art modular system implementation.

# 3.2 ECoG Interfaces: Recording and Stimulation

#### 3.2.1 Volume Conduction with Differential Electrodes

Volume conduction of ionic currents in the body is the source of biopotentials such as EEG, ECoG, ECG, and EMG. In the frequency band of interest for biopotential recording (typically less than 1 kHz), the quasi-static electric field equations with conductivities of tissue layers are a good approximate representation [291]. To first order, a volume conducting current monopole I spreads radially through tissue with an outward current density of magnitude  $I/4\pi r^2$  at distance r, giving rise to an outward electric field of magnitude  $I/4\pi\sigma r^2$  and a corresponding electrical potential  $I/4\pi\sigma r$ , where  $\sigma$  is the tissue volume conductivity.

#### Differential Recording

For EEG, a current dipole as a closely spaced pair of opposing current monopoles is typically an adequate model representing distant sources of synchronous electrical activity across large assemblies of neurons or synapses [291]. In contrast, for implanted neural recording including ECoG and single-unit neural spike/LFP recording, a set of monopole currents resulting from individual neural units is a more appropriate model at the local spatial scale, especially for high density recording with electrodes spaced at dimensions approaching inter-cellular distances. Since the volume conducting currents from neural action potentials are spatially and temporally distributed, only a few effective current sources at a time are typically active near an electrode, one of which is illustrated in the vicinity of two closely spaced electrodes in Fig. 3.3 (a). Furthermore, unlike the ground-referenced recording with single-ended electrodes for EEG, high-density electrode arrays typically require differential recording across electrodes, particularly in  $\mu$ ECoG integrated recording since the miniaturized geometry does not allow for a distal ground connection.

In Fig. 3.3 (a), the recorded differential voltage V as a function of the

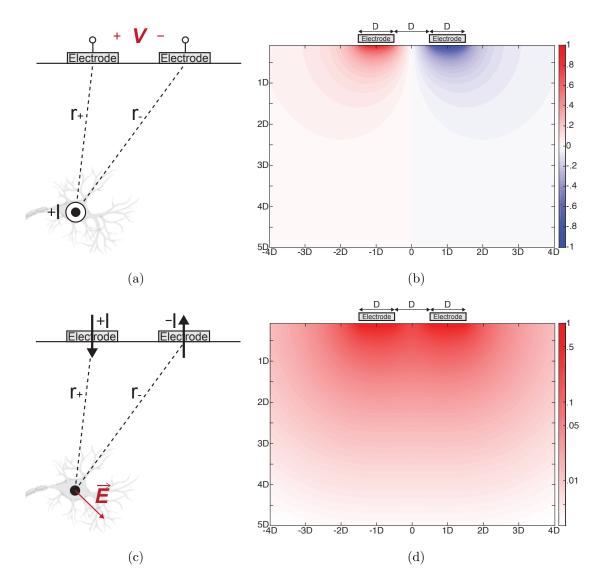


Figure 3.3: (a) Neural recording setting with closely spaced differential electrodes interfacing below with neural tissue of volume conductivity  $\sigma$ . (b) Spatial map of the effect of the location of a current source +I in the tissue on recorded differential voltage V, in units  $1/\sigma D$ . (c) Neural stimulation setting with differential currents injected into the surrounding tissue through the same two closely spaced electrodes. (d) Spatial map of the resulting electric field magnitude  $|\vec{E}|$  in the tissue, in units  $1/\sigma D^2$ .

distances  $r_{+}$  and  $r_{-}$  of the two electrodes from a current source I induced by the activity of adjacent neurons can be expressed as:

$$V(r_+, r_-) \cong \frac{I}{2\pi\sigma} \left( \frac{1}{r_+} - \frac{1}{r_-} \right) \tag{3.1}$$

valid for distances  $r_+, r_-$  substantially larger than the electrode diameter D. Although the expression is similar to that for an EEG current dipole recorded with a single electrode, it is fundamentally different in that here the difference in monopole activity results from differential sensing with two closely spaced electrodes rather than from dipolar distribution of two closely spaced currents. The factor 2 rather than 4 in the denominator arises from the semi-infinite boundary conditions along the horizontal plane of the electrode substrate, in that volume conduction is restricted to the tissue below the substrate. Fig. 3.3 (b) shows a spatial map of the effect of a current source located in tissue below the electrode pair, with electrode diameter D and pitch 2D, on the measured differential voltage V. Its recording penetration depth is roughly 2D, the electrode pitch, vertically, and about 4Dhorizontally. Note again that this is for a single monopolar source; in the presence of dipolar activity with two opposing nearby currents (i.e., charge balancing across a soma and dendrite of a neuron extending below the electrodes) the measured voltage (3.1) becomes double differential, leading to a quadrupolar response profile.

#### Differential Stimulation

The same pair of closely spaced electrodes can be used for differential stimulation by injecting currents into the surrounding tissue. Again, the absence of a distal ground connection in miniature integrated electrode arrays necessitates local charge balancing so that the currents through the two electrodes need to be of equal strength and opposing polarity, constituting a current dipole sourced within the electrode array. The resulting differential current stimulation can be modeled with the diagram shown in Fig. 3.3 (c). The current dipole from the pair of differential stimulation currents flowing through the two electrodes induces an electrical field  $\vec{\bf E}$  in the brain tissue expressed by:

$$\vec{\mathbf{E}}(r_+, r_-) \cong \frac{I}{2\pi\sigma} \left( \frac{\vec{\mathbf{u}}_{r_+}}{r_+^2} - \frac{\vec{\mathbf{u}}_{r_-}}{r_-^2} \right)$$
 (3.2)

where again  $r_+, r_- \gg D$ , and  $\vec{\mathbf{u}}_{r_+}$  and  $\vec{\mathbf{u}}_{r_-}$  represent unit vectors pointing outwards along the direction of  $r_+$  and  $r_-$ , respectively. With the same electrode

configuration of Fig. 3.3 (b), the magnitude of the electric field  $|\vec{\mathbf{E}}|$  is shown in Fig. 3.3 (d) indicating a shallow region near the electrodes being electrically stimulated. Note that the electrical field for stimulation is inversely proportional to the square of distance to each electrode, while the potential measured for recording is inversely proportional to linear distance. Thus, the available depth of differential stimulation is shallower than that of differential recording. In general, the penetration depth of stimulation and recording are roughly a few times larger than the electrode pitch.

#### **Electrode Array Configurations**

While this is a simplified model, it is sufficiently representative to demonstrate the effectiveness of differential electrode configurations for both recording and stimulation without a global reference, as required for fully integrated  $\mu$ ECoG in absence of a distal ground connection. As the analysis and simulations above show, the spatial response of differential recording and stimulation are quite localized near the electrode sites, on a spatial scale that matches the electrode dimensions and spacing. Thus, aside from spatial selection of recording or stimulation along the 2-D surface by translation of selected pairs of adjacent electrodes, depth and spatial resolution of recording or stimulation can be controlled via virtual electrode pitch, by pooling multiple electrodes in complementary pairs of superelectrodes at variable spacing between centers.

#### 3.2.2 Electrode Interfaces for ECoG

Electrodes, which couple ECoG signals from the brain into the analog frontend amplifiers, are the first interface to ECoG systems. Thus, their properties, including materials, geometries, and placement are of crucial importance in building entire acquisition and actuation systems [136].

Given the distance between the scalp and individual neuronal current sources and sinks, EEG recording is unsuitable for detecting small local field potentials as shown in Fig. 3.2 (a). Electrical dipole signals travel a minimum distance of 1 cm between the outer surface of the cerebral cortex to the scalp, including layers of

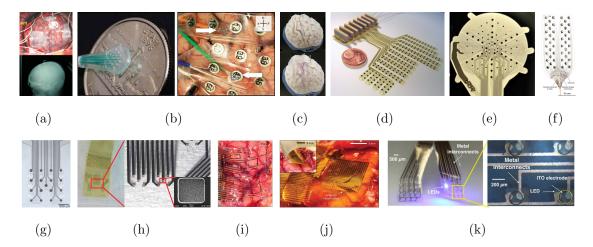


Figure 3.4: Conventional and state-of-the-art ECoG electrode arrays. (a) Example of a conventional electrode array placed on the subdural cortex (top) with post-operative radiograph showing electrode array placement (bottom). The pitch and diameter of electrodes are 1 cm and 2 mm, respectively [232]. (b)  $\mu ECoG$ electrode array placed along with a conventional ECoG electrode array [189, 190]. (c) Patient-specific electrode array for sulcal and gyral placement [279]. (d) Flexible 252-channel ECoG electrode array on a thin polyimide foil substrate [323]. (e)  $\mu ECoG$  electrode array with 124 circular electrodes with three different diameters [389]. (f) Parylene-coated metal tracks and electrodes within a silicone rubber substrate [216]. (g) A transparent  $\mu$ ECoG electrode array with platinum electrodes on a Parylene C substrate [316]. (h) An electrode array with poly(3,4ethylenedioxythiophene) (PDOT) and PEDOT-carbon nanotube (CNT) composite coatings for lower electrode interface impedance [51]. (i) A flexible electrode array on a bioresorbable substrates of silk fibroin [207]. (j) Flexible active electrode array with two integrated transistors on each pixel for ECoG signal buffering and column multiplexing for high channel count [405]. (k) Flexible ECoG array with embedded light-emitting diodes for optogenetics-based stimulation [222].

cerebrospinal fluid, meninges, bone and skin, all with varying electrical properties. Through this path the effect of a small-localized dipole source is not only greatly attenuated but also spatially averaged among a myriad of neighbors, resulting in practical and theoretical limits to the spatiotemporal resolution of EEG [128]. As implied in Eq. (3.1), cm-sized electrode arrays with cm spacings in conventional ECoG recordings are better than EEG, but have limitations in resolving current sources of neural activity of size smaller than the electrode pitch. A conventional clinical ECoG array with electrodes at the cm scale is depicted in Fig. 3.4 (a).

A miniaturized surface electrode array in direct contact with the cerebral cortex can resolve the activity of smaller source populations down to mm or even sub-mm resolution as shown in Fig. 3.4 (b)-(k). Furthermore, site specific purposeful electrical stimulation is only possible at  $\mu ECoG$  scale. Improvements in the quality and applications of ECoG data have resulted from technological developments at the interface: microfabrication of electrode and substrate materials and interconnect. Simply miniaturizing existing electrode array is not typically sufficient: for example, miniaturized electrodes in <1 mm pitch arrays have very high impedance, which results in poor signal quality, and reduced charge transfer capacity, which typically reduces stimulation efficiency. Such limitations have been addressed by micro-patterning increased surface area, and carbon nanotube [65] or conductive polymer coatings (Fig. 3.4 (h)) [51]. Flexible substrates have also reduced the effective distance between source and electrodes through tight, conformal geometries [216, 323]. Aside from creating ultra-flexible thin materials, dissolvable substrates leave behind a mesh of thin unobtrusive wires and electrodes with a superior curved conformation and biocompatibility as shown in Fig. 3.4 (i) [207,331].

Even with advances in flexible electrode arrays, the number of channels in practical systems are still limited to approximately 100 because of the high density of interconnections between electrode arrays and corresponding acquisition systems. Active electrodes are an emerging approach to maximize number of electrode channels while maintaining small number of wired connections to the electrode array. Advanced fabrication techniques can produce arrays of electrodes with direct integration of transistors on the flexible substrate as shown in Fig. 3.4 (j) [405] This approach can be supplemented with additional in situ devices capable of multiplexing several 100s of recording channels, thereby reducing the required number of wires and interconnections. Another emergent approach combining active recording electrodes and new polymeric materials has led to the development of organic electrochemical transistors in ECoG arrays [195]. However, one limitation of current active arrays is that the same electrode cannot be used for stimulation. Recently, transparent electrode arrays with integrated light path for simultaneous ECoG recording and optogenetic stimulation have been demon-

strated as shown in Fig. 3.4 (k) [222]. The active development of novel electrode interfaces has not only improved conventional ECoG recording, but also generated new applications and therapeutic opportunities.

## 3.2.3 Integrated Circuit Interfaces for Data Acquisition

Neural data acquisition with a high spatial resolution poses several challenges in the design of application-specific integrated circuits (ASICs) used to perform data acquisition. Higher channel density in ECoG arrays typically results in smaller electrode size, and if the area overhead of the ASIC should be kept small, as is desired in most applications, then the area dedicated to amplify and digitize each channel should also reduce. Unfortunately, area trades off with several important parameters. For example, a more dense array of analog front-end (AFE) amplifiers dissipates more power and generates more heat for each channel, and thus power dedicated to each front-end channel must reduce to meet thermal regulatory limits. Power then trades off with noise, causing signal fidelity issues. The area/volume constraint of front-ends typically also precludes the use of external components such as inductors or capacitors. As a result, AC coupling capacitors employed to reject DC or slowly time-varying electrode offsets are not typically employed, so other techniques are instead necessary. Small electrodes also have higher impedance, requiring even higher AFE input impedance to avoid signal attenuation. In addition, high power supply rejection ratio (PSRR) is required because miniaturized implants typically condition DC power from an external AC source, and further may not be able to accommodate large power decoupling capacitors. Higher channel counts also require higher communication throughput, increasing the power consumption of communication. All these requirements are interrelated and trade off with each other in many ways, as indicated in Table 2.2 [136,147,391].

The noise-current trade-off in instrumentation amplifiers (IAs) is well represented by the noise efficiency factor (NEF), which is expressed as:

$$NEF = V_{rms,in} \sqrt{\frac{2I_{tot}}{\pi V_t \cdot 4kT \cdot BW}}$$
 (3.3)

where  $V_{rms,in}$  is the total input-referred noise,  $I_{tot}$  the total current drain,  $V_t$  the

thermal voltage, and BW the -3-dB bandwidth of the system [362]. To minimize noise with a given current consumption or minimize current consumption with a upper-bound noise limit, various design techniques have been proposed and demonstrated to address this challenges [63, 94, 102, 145, 146, 148, 178, 276, 356, 394, 404, 409, 425, 429, 439, 442, 443, 449, 457, 465]. Such techniques to minimize NEF include i) utilizing the weak inversion region of CMOS operation to maximize transconductance efficiency [137, 147, 148, 326], ii) chopper stabilization techniques to to reduce 1/f noise and other low-frequency noise [94, 100, 260, 404, 425, 429, 443], iii) dynamic range manipulation to reduce power supply voltages [63, 145] using spectrum-equalizing analog front-end [305, 351], iv) using current-reusing nMOS and pMOS input pairs to maximize transconductance and achieve a NEF below two [145, 146, 356, 409, 439].

Challenges in meeting the other specifications listed in Table ?? have also been addressed using various circuit techniques. For example, several DC-coupling IAs have been demonstrated in order to avoid external AC-coupling capacitors at the input of the AFE [442,443]. In these designs, electrode offsets are canceled by feedback currents via a DC-servo loop [442,443] or by capacitive feedback [282].

Integration of higher channel count on a single chip has been pursued, as well. Thus far, chips with approximately 100 to 300 data acquisition channels have been reported [21, 116, 145, 149, 343]. One of the strategies to reduce area and power consumption in order to maximize channel density is the use of scaled processes such as 65 nm CMOS [282], achieving 64 channels with a silicon area of 0.025 mm<sup>2</sup> per channel. For higher density, in some designs, a SAR ADC is shared by about 8 to 16 AFEs using a time-multiplexer [145]. In doing so, power efficient multiplexers [435] and time-interleaving sample-and-hold circuits in SAR ADCs have been demonstrated. Alternatively, a dedicated ADC per AFE channel has been also pursued due to its ease of integration with larger number of channels [276, 282].

## 3.2.4 Integrated Circuit Interfaces for Stimulation

Historically, electrical stimulation on the cortical surface was pioneered by Wilder Penfield [306] as intraoperative planning for epileptic patients, demonstrating the localized function of different regions of the cortex [254]. Since then, functional neural stimulation has been extensively investigated and developed during the past decades, making great progress for various clinical applications such as deep brain stimulation, cochlear implants, cardiac pacemakers, bladder control implants, and retinal prostheses. Given that many epilepsy patients already require implantation of ECoG monitoring instrumentation, there is a great opportunity for closed-loop electrical control of seizure activity at much higher resolution and precision than transcranial electric [30] and transcranial magnetic stimulation [180,273]. These embedded stimulators would not require any additional invasive risks, and could potentially prevent more drastic treatments such as partial removal of the cortex. An implantable recording and stimulation system can contain a digital signal processor capable of deciding when to stimulate [61]. Other applications of cortical stimulation include closed-loop brain computer interfaces (BCI) which aim to generate functional maps of the brain [41], restore somatosensory feedback [180], restore motor control to tetraplegics [171], aid stroke survivors [98,233], restore vision [234], reduce pain [254], or even change emotional state [49].

Pushing the form factor and channel density of the neural interface systems to the limit requires addressing several challenges in ASICs for stimulation. Smaller form factor and higher channel density require smaller electrode size, which limits charge transfer capacity for effective stimulation. Hence, higher voltage rails of more than  $\pm 10$  V and/or high-voltage processes are required typically [221,241,298], in turn this results in higher power consumption, larger silicon area, and system complexity to generate and handle high-voltage signals. Instead of maintaining a constant high-voltage power supply, some designs save power by generating a large power rail only when actively stimulating [36,61,133].

For further power savings, adiabatic stimulation has been also actively investigated. Adiabatic stimulators generate ramping power rails that closely follow the voltages at the stimulation electrode, minimizing unnecessary voltage drops

across the current source employed for conventional constant-current stimulation. Various designs have been implemented with external capacitors [192], external inductors [18], and charge pumps [36]. Still, there is much room for improvement in the implementation of adiabatic stimulators in fully-integrated, miniaturized implantable ICs.

It is generally desired to minimize the area occupied per stimulation channel for high-density integration. To date, integration of 100 to 1600 channels has been achieved [221,241,278,298,321,383]. In order to integrate such high channel counts, programmability of waveform parameters, individual connectivity to each channel, and/or charge balancing need to be compromised to some extent. For example, groups of 4 to 8 electrodes in [278,321,348,446] can share a single digital-to-analog converter for optimized, high density integration.

Safety is of the utmost importance in chronic neural interfaces, so charge balancing is imperative [267]. Residual DC currents result in tissue damage, production of toxic byproducts, and electrode degradation [267]. However, it is quite challenging to assure charge balance for each channel in high-channel neural interface systems. One of the most straightforward strategies is to employ serial DCblocking capacitors, inherently forcing the net DC current to be zero all the time. This method has been employed for neural stimulation applications [17, 163, 366] due to its intrinsic safety when area permits. However, the required blocking capacitance is often prohibitively large for on-chip integration, and is thus inadequate for high-density and/or miniaturized implants. Instead of external capacitors, capacitive electrodes made with high-k dielectric coatings have been investigated for safe neural interfaces [133, 224, 332]. Several other techniques for better charge balancing have been demonstrated: i) shorting electrodes to ground [240], ii) utilizing a discharging resistor [348], active current balancing by feedback control [289, 347], generating additional balancing current pulses by monitoring electrode voltages [357], and embedded DAC calibration [131, 278].

## 3.2.5 Integrated Electrocortical On-line Data Processing

The integration of signal processing with neurophysiological sensing and actuation enables real-time on-line control strategies towards realizing adaptive, autonomous closed-loop systems for remediation of neurological disorders [43,95]. On-line signal processing of ECoG data has tremendous potential to improve patient outcomes in diseases currently lacking therapy or requiring resection of otherwise healthy neural tissue such as intractable epilepsy. As one of the treatments for epilepsy, functional neurostimulation in response to detected seizures has been proved effective in reduction of seizures [123,150]. For real-time close-loop therapeutics, on-line automated seizure prediction and/or detection based on ECoG or EEG recordings of epileptic patients is imperative [27,82,311,459], and their on-chip implementation has been actively investigated and demonstrated utilizing extraction and classification of various signal features such as power spectral densities and wavelet coefficients [8,37,61,299,404,448].

In addition, ECoG has proven a powerful modality for BCI applications owing to richer features present in the higher resolution ECoG signals compared to surface EEG, which can be harnessed to more precisely infer sensory recognition, cognition, and motor function. Since ECoG-based BCI systems widely utilize spectral power density for their inputs [330], frequency band power extraction techniques have been implemented immediately following AFEs avoiding digitization and RF data transmission of whole ECoG raw signals [19,458].

Such on-chip real-time ECoG data processing offers two distinct advantages over off-line as well as on-line off-chip processing. First, constrains on data bandwidth and power consumption on the implant can be largely relieved. In many implementations, raw recorded data is wirelessly streamed out and delivered to either a unit worn on the top of the head, or directly to a local base station such as a smartphone. The power of such approaches is typically proportional to the communication distance. Thus, the overall power consumption of designs that stream over long distances can be dominated by the power of communication circuits [404]. In order to reduce system-level power consumption, several on-chip data processing techniques have been applied for EEG- and ECoG-based BCI systems and epilep-

tic seizure detection. By doing so, power consumption of RF data transmission can be drastically reduced [404]. Second, local processing may alleviate stringent latency and buffer memory requirements in the uplink transmission of data for external processing, especially where multiple implants are time-multiplexed between a common base station.

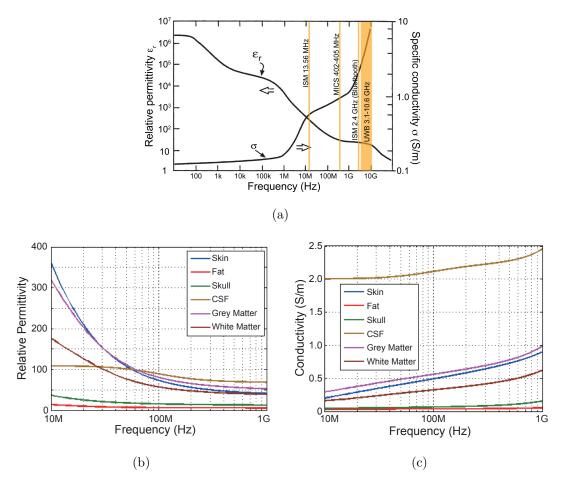
## 3.3 System Considerations

## 3.3.1 Powering

Major challenges in implantable medical devices (IMD) for high-density brain activity monitoring are fundamentally posed by their target location. Some of these IMDs can be wholly placed on the cortex within a very limited geometry as shown in Fig. 3.2 (b) In other cases, only the electrode array is placed on the cortex while the other components can be located in the empty space created by a craniotomy [268], or under the scalp with lead wires connected [353,354]. Regardless of placement, this constrained environment poses a difficult power challenge.

There are three primary methods for powering an implanted device: employing a battery, harvesting energy from the environment, and delivering power transcutaneously via a wireless power transmitter [126,204]. A natural first choice would be a battery, as they have been extensively used in other implantable applications such as pacemakers. While it makes sense to use a battery in a pacing application, where the power of the load circuit is small (microwatts) and a large physical volume is available such that the battery can last 10 years of more, the power consumption in high-density neural recording and stimulation applications is typically much larger (milliwatts), and the physical volume available for a large battery is small, combining to dramatically reducing operational lifetime prior to necessary surgical re-implantation. The medical risks of regular brain surgery and recovery, just to replace a battery, are unacceptable to most patients, and thus batteries are typically only employed in high-density neural applications as temporary energy storage in systems with a different power source: either energy scavenging or wireless power transfer.

Harvesting energy from ambient sources in the local environment has been a potentially attracting powering option since at least the 1970s during the development of cochlear implants. Many scavenging methods continue to be actively developed: 1) solar cells, 2) biofuel cells, 3) thermoelectric generators, 4) piezoelectric generators, 5) ambient RF, etc. While such approaches are theoretically attractive, the limited volume available near the brain, coupled with the stochastic nature of many energy harvesting sources, results in power that is too small and too variable to reliably operate multi-channel neural technologies.



**Figure 3.5**: (a) Relative permittivity and specific conductivity over frequency range from 10 to 100 GHz with most popular frequency communication bands for ECoG implants [270,313]. (b) Relative permittivity and (c) specific conductivity of various kinds of tissues including skin, fat, skull, CSF, grey and white matter [53].

The most popular means to power an implanted device with higher power

than single-channel pacing applications is to wirelessly delivery power via a transcutaneous link. Power can be delivered transcutaneously using one of three primary mechanisms: i) optics (typically near infrared light), ii) acoustics (typically at ultrasound frequencies), and iii) electromagnetics (either near-, mid-, or far-field waves). Each method can deliver from 10  $\mu$ W up to the mW range of power. However, the total deliverable power highly depends on the geometry and make-up of the receiving transducer, along with the implant depth and orientation.

Optical powering through transmission of infrared light has a very short penetration depth of a few millimeters, limiting its utility to subcutaneous and very shallow implant applications [14, 127, 283]. Ultrasound, on the other hand, can penetrate much deeper into tissue, potentially powering implants located on the cortical surface. In fact, it has been demonstrated that ultrasound can more efficiently power mm-scale devices implanted deep into soft tissues than electromagnetic approaches [73]. However, it has also been shown that ultrasonic energy does not efficiently penetrate bone, limiting opportunities to directly power cortical implants from outside the skull. To overcome this, researchers have proposed two-tiered systems, where electromagnetic energy is coupled through the skull, then converted to acoustic energy via an intermediate transducer system, and finally delivered to the miniaturized implant through soft tissue [336]. However, in addition to non-trivial packaging and transducer design challenges, this is likely only a reasonable approach when the implant to be powered is either very deep, or very small (sub-mm scale). For these reasons, ultrasonic power delivery is not typically considered for ECoG systems.

The most popular transcutaneous power delivery approach utilizes electromagnetics. For devices implanted to a depth of a few centimeters, and that are on the order of mm-to-cm in diameter, near- or mid-field electromagnetic power transfer is generally considered to be the most efficient and practical method to power such devices. Near-field power transfer, which operates at frequencies up to approximately 100 MHz for typical implants, has been extensively used for cochlear implants [456], retinal prostheses [241, 278], and various research IMD systems [23,172,215,228,268], and has been investigated and characterized to max-

imize its usage and power transfer efficiency for implants [25, 181, 253, 312, 428, 431].

Most conventional designs operate in the near-field between 1 and 20 MHz, since it is well known that conductivity (and hence losses) in tissue increase at higher frequencies, as shown in Fig. 3.5. Operating at higher frequencies, it was previously argued, would encounter higher losses and thus be less efficient. In addition, governmental regulatory agencies limit the amount of power that can be dissipated in tissue for safety reasons - the US Federal Communications Commission (FCC) sets a specific absorption rate (SAR) of less than 1.6 W/kg, for example. For these reasons, conventional transcutaneous power transfer links operate in the low-MHz range, often at the 6.78 and 13.56 MHz ISM bands [126, 253, 428].

However, it is also well known that the quality factor and radiation resistance of electrically-small coil antennas increases with increasing frequency. Thus, miniaturized implants, which have electrically small coils for wireless power reception, tend to prefer to operate at higher frequencies, at least in air. In biological tissues, the trade-off between coil design and tissue losses results in an optimal frequency for wireless power transmission where efficiency is maximized. For example, the inductance of coils located on miniaturized, mm-scale implants ranges from 10 to 100 nH [12,133,282,455]. To compensate reduced magnetic flux through the miniaturized receiving coil, the carrier frequency for wireless power transfer should be increased, often into the hundreds of MHz to single-digit GHz range [12,282,309,454,455]. These prior studies have demonstrated that it is possible to efficiently deliver milliwatts of power to small, implanted devices under regulatory limits, and thus electromagnetic approaches are the primary means to deliver power to implanted ECoG devices.

#### 3.3.2 Wireless Data Communication

Implanted ECoG monitoring devices need to convey the acquired data to the external world through wireless communication. The information received by the external base station can be monitored, processed and used by users and care takers for health monitoring, treatments, or scientific research. For ECoG monitoring implants, data transmission from the implant to the external device, known as

uplink or backward telemetry, requires much higher data rate and is subject to more stringent power consumption constraints than data transmission from the external device to the implant, known as downlink or forward telemetry, because the available power and geometric volume are much smaller on the implanted side than the external side. This power constraint on backward data transmission is more exacerbated as the number of channels increases, as higher data rates are required in a typically more compact area, leading to severe power density challenges.

Backward data communications typically employ electromagnetics operating either in the far- or near-field. Far-field communication uses electromagnetic radiation to transmit data over a distance much longer than the size of the actual device. Hence, the implant can send data to a external base station located up to a few meters, such as mobile phone. Far-field up-conversion transmitters are currently the most well-established communication technology. Due to the wide availability of far-field radio products and a myriad of different infrastructures (e.g., Bluetooth Low Energy, WiFi, etc.), far-field radios can be quickly adopted for robust operation [268]. However, even state-of-the-art low-power radios consume >1 nJ/bit [126, 264], which is order-of-magnitude larger than what typical ECoG recording IMDs require.

As an alternative far-field transmission method, impulse radio ultra-wide band (IR-UWB) transmission has emerged recently due to its low power consumption in the range of a few tens of pJ/bit [16, 58, 265]. Avoiding generation of a carrier with an accurate frequency, non-coherent IR-UWB transmitters generates short pulses with on-off keying (OOK) or pulse position modulation (PPM). Due to its high and wide frequency range (3.1-10 GHz), data rates of more than 10 Mbps with tens of pJ/bit have been reported. [272] In addition, antennas for this type of transmission do not need to be large. However, there are a couple of critical reasons against their usage for IMDs [126]. Foremost, their peak transmission power is large due to the inherently duty-cycled nature of IR-UWB transmitters. Thus, while the average power may be low, a large high-quality power supply with a large battery of capacitor is required to supply large peak currents, which

may be prohibitively large for many ECoG applications. Moreover, since IR-UWB operates at very high frequency over 3 GHz, tissue absorption rate is higher.

In contrast to far-field communication methods, near-field radios operate over short distances, typically within one wavelength of the carrier frequency, and are thus suitable for use when an external device is located directly on the head. In fact, since this configuration is naturally present in wirelessly-powered devices, near-field communication can easily be implemented along with this wireless powering. One of the most popular data communication methods that can be implemented along with forward power delivery is the backscattering method [138, 227, 245, 328, 375]. This method modulates the load conditions of forward powering signals, and reflecting this energy back to the interrogator. Since only a single switch needs to be driven, the power consumed on the implant side is minimal, as carrier generation and active driving of an antenna are not required. Since, with this technology, a few pJ/bit to tens of pJ/bit can be achieved [138], it has been widely adopted by various IMDs [33,239,241,282,419,426,432]. However, external data reception in backscattering systems can be challenging in some cases because of the large power difference between the large power carrier signal and the weak backscattered signal.

Forward telemetry for neural recording IMDs is typically used for sending configuration bits to the implant, requiring a relatively low data rate typically much less than 100 kbps. Hence, amplitude shift keying (ASK) has been widely employed in such IMDs [133, 229, 451], modulating the power carrier signals. For IMDs with stimulation capability, forward telemetry for closed-loop operation is typically time-multiplexed with backward telemetry.

## 3.3.3 Hermetic Encapsulation

Implanted devices containing silicon ICs need packaging in a protective enclosure to mitigate corrosion and other contamination by surrounding electrolyte in the body [176, 402]. Thus far, titanium-, glass- or ceramic-based enclosures have been the primary means for hermetic sealing in long-term implants, since these hard materials have been shown to be biocompatible and impermeable to

water [176]. Even though such hard enclosures are used in the majority of long-term implants [5,10,82,88,153–155,268,310,322,369], their very large volume and weight, typically much larger than the ICs and supporting components they contain, prohibits their use in high-dimensional neural interfaces heavily constrained by anatomical space such as retinal prostheses [412] and  $\mu$ ECoG arrays [405]. In addition, hard packaging requires intricate methods for hermetic sealing of feedthroughs to polymer insulated extensions of the implant such as electrode array cabling, limiting the density of electrode channels due to feedthrough channel spacing requirements.

To overcome these challenges, conformal coating of integrated electronics with polymers such as polyimide, silicone, and parylene-C have been investigated as alternatives. They are superior over metal, glass, and ceramic hard seals in miniaturization, flexibility, and compatibility with the semiconductor process [173]. However, polymers are susceptible to degradation and are not long-term impermeable to body fluids. While polymer encapsulation has been used for relatively simple and short-term (less than 1-2 years) implants, substantial improvements are needed for viable solutions to long-term hermetic encapsulation [402,415]. Recent next-generation advances in miniaturized hermetic sealing of silicon integrated circuits, such as multi-layer multi-material coating [416], and encapsulation using liquid crystal polymers (LCP) [173], are promising developments towards highly miniaturized implantable electronics for chronic clinical use. Furthermore, recent advances in dissolvable flexible electronics [168,452] offer alternatives to hermetic encapsulation for acute applications without the need for post-use surgical extraction.

## 3.4 State-of-the-Art ECoG Interface Systems

Various types of implantable devices for ECoG interfaces have been developed for clinical use and neuroscience research. Their target applications include treatment of neurological disorders and ECoG-based BCIs. Fig. 3.6 illustrates several state-of-the-art ECoG interface systems for clinical and research applications.

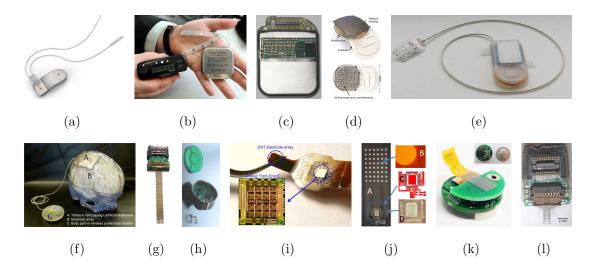


Figure 3.6: State-of-the-art ECoG interfacing systems. (a) NeuroPace RNS System [5, 369]. (b) NeuroVista Seizure Advisory System [82, 88, 310]. (c) The neural interface (NI) system of Medtronic [10, 322]. (d) The Wireless Implantable Multi-channel Acquisition system for Generic Interface with NEurons (WIMAGINE) [268]. (e) BrainCon system for a general-purpose medical BCI [107, 217, 333] (f) The Wireless Human ECoG-based Real-time BMI System (W-HERBS) [153, 154], (g)  $\mu$ ECoG recording system of Cortera Neurotechnologies, Inc. [3,282]. (h) A ECoG recording system with bidirectional capacitive data Telemetry [274]. (i) An ECoG recording system with a carbon nanotube microelectrode array and a corresponding IC [65]. (j) A wireless ECoG interface system with a 64-channel ECoG recording application-specific integrated circuit (ASIC) [93]. (k) A 8-channel low-cost wireless neural signal acquisition system made with offthe-shelf components [120]. (1)  $\mu ECoG$  recording system with an electrode array fabricated on a transparent polymer for optogenetics-based stimulation [316].

On the clinical side, implantable devices shown in Fig. 3.6 (a)-(c) have been developed mostly for use in closed-loop treatment of intractable epilepsy as an alternative to tissue resection. These devices monitor ECoG signals and deliver stimulation to the seizure foci in response to epileptic seizure detection. The NeuroPace<sup>®</sup> RNS<sup>®</sup> System, shown in Fig. 3.6 (a), is the first such system to receive FDA approval for closed-loop treatment in epilepsy patients, proven effective to reduce the frequency of partial-onset seizures in human clinical trials [151, 368].

However, clinically proven devices are severely limited in the number of ECoG channels, typically less than ten, and rely on batteries, limiting implantation life time up to a few years. In addition, their physical size is too large to be implanted near the brain, so the main parts of these systems are implanted under the chest with a wired connection to the brain. Further developments in ECoG technology have striven to conquer these challenges: increasing number of channels, wireless powering, and miniaturization.

One such device is the Wireless Implantable Multi-channel Acquisition system for Generic Interface with NEurons (WIMAGINE), which features up to 64 channels, targeting long-term ECoG recording fully implanted in human patients [268] as shown in Fig. 3.6 (d). This active IMD (AIMD) is fully covered by a 50-mm diameter hermetic housing made of silicone-coated titanium with a silicone-platinum electrode array on the bottom side. Its silicone over-molding is extended to include two antennas for RF communication and wireless power transfer. The housing fits inside of a 50-mm craniotomy, and its upper surface is just below the skin, with the implant replacing the previously existing bone. Two 32-channel ECoG recording ASICs [318] are implemented for ECoG recording, and commercial off-the-shelf components are employed for data processing, communication, power management, etc, leading to relatively high power consumption—75 mW for 32 channels. Its operation and biocompatibility has been evaluated in vivo in non-human primates.

Another example is the BrainCon system with 16-channel ECoG recording and 8-channel stimulation designed for chronic implanted use in closed-loop human BCI [107]. Shown in Fig. 3.6 (e), this device consists of an ECoG electrode array and an electronic package with a magnet, an inductive coil, and electronic components for data acquisition, stimulation and communication. Targeted for long-term recording and cortical stimulation in human patients, it is enclosed in a hermetic package with medical grade silicone rubber [217, 333], and was validated in vivo for more than 10 months [107].

Further miniaturization and advances in functionality have been pursued through integration of circuits for ECoG recording, wireless powering, and wireless communication as shown in Fig. 3.6 (f)-(j). In addition, low-cost ECoG interfaces shown in Fig. 3.6 (k) for acute animal research have been developed [120], as have ECoG interfaces with transparent electrode arrays for compatibility with

optogenetic stimulation shown in Fig. 3.6 (l) [316].

Each of these devices offer substantial advances in wireless and integrated ECoG technology with improved functionality and increased density and channel counts. Yet, most rely on substantial cabling in connecting to the array of electrodes, or at least a wired connection to a distal ground as reference.

## 3.5 Conclusion

In this chapter we highlighted the importance of high density electrocorticography for brain activity mapping, brain computer interfaces, and treatments for neurological disorders. We reviewed the critical design challenges on fully implantable ECoG interface systems in their major aspects including electrode interface, recording and stimulation circuitry, wireless power and data communications. In addition, we surveyed state-of-the-art systems at the forefront of clinical and research applications and noted the rapid evolution of the technology in the past few years.

Chapter Three is largely a reprint of material that was submitted to the Proceedings of the IEEE: Sohmyung Ha, Abraham Akinin, Jiwoong Park, Chul Kim, Hui Wang, Christoph Maier, Patrick P. Mercier and Gert Cauwenberghs, "Silicon Integrated High-Density Electrocortical Interfaces," *Proceedings of the IEEE*, 2017, *Accepted*. The author is the primary author and investigator of this work.

## Chapter 4

## Energy-Recycling Telemetry with Simultaneous Power and Backward Data Delivery over a Single Inductive Link

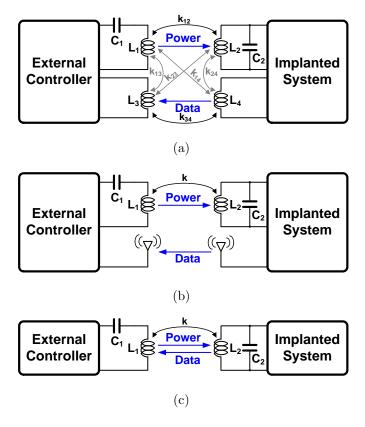
## 4.1 Introduction

The proliferation of power and form-factor constrained devices like implanted medical devices (IMDs), radio-frequency identification (RFID) and wireless sensors has led to the extensive use of inductive wireless links for short-range power and data telemetry. For these applications including IMDs with an implantation depth of a few cm, such as cochlear implants, visual prostheses and brain-computer interface (BCI) systems with high-throughput neural recording, wireless inductive powering is a natural choice as the primary mode of power transfer due to its high efficiency and well known robustness in comparison to competing technologies such as ultrasound telemetry and energy scavenging. Thus, over the past decades, inductive power telemetry has been the focus of extensive studies resulting in the development of many efficient designs and methodologies [25, 164, 181, 253, 312, 428, 431, 454].

Since near-field communication (NFC) using inductive links offers lower cost of communication than far-field communication methods, it has become the primary means of communication with IMDs [33, 239, 241, 282, 419, 426, 432] and sensors [9, 77, 177, 235, 266, 359], and further has been adopted as a secondary communication channel between power-constrained mobile devices such as smartphones and tablets. Along with NFC, RFID applications also use inductive links to power battery-less tags and sensors while transferring stored data [34, 81].

In both biomedical and sensor applications, available power and geometry on the primary and secondary sides are very asymmetric. Implanted devices and sensor nodes have much more stringent constraints both in power consumption and size while those constraints are significantly more relaxed on the primary side [253]. Thus, both uplink and downlink data telemetry need to be substantially more power and area efficient on the secondary side than on the primary side. Hence, transmitters on the implanted or sensor side for uplink telemetry require more stringent optimization for efficiency than receivers on the external side. In addition, simpler antennas are preferred on the the implanted and the sensor side due to size and reliability constraints. While several power efficient schemes for high-data-rate forward telemetry [183,203,241,324,346,460] have been demonstrated for implants and sensor nodes, efficient high-data-rate backward telemetry in these settings has remained challenging.

To highlight the challenges in the design of such systems we specify the requirements that must be met by a typical high-density brain activity monitoring IMD. These IMDs typically have one of three configurations: an entire device placed on the cortex [282]; an electrode array placed on the cortex with the primary device on the craniotomy [268]; or the primary device placed under the scalp [345, 354]. In all these configurations, the devices are highly geometry and power constrained and the implant location poses a major challenge of power acquisition and data communication. The data rate requirement for 1,024-channel ECoG recording with a sampling rate of 600 S/s and a data resolution of 10 bits is 6.15 Mbps. Similarly, for 64-channel recording of neural spikes and local field potentials at 10-kS/s rate and 10-bit resolution, a data rate of 6.4 Mbps is required.



**Figure 4.1**: Power and uplink data telemetry topologies: (a) separate inductive links for power and data telemetry, (b) inductive link for power transfer and active radio for data telemetry, and (c) single inductive link.

State-of-the-art IMDs recording and transmitting data at these high rates typically consume several mW of power [42, 56, 140, 149, 268, 282, 337, 353]. Since the antenna geometry and ASIC placement near the implant site constrain available power, achieving both the power transfer and data rate specifications proves to be a challenging task.

To meet these requirements, one popular approach is to use multiple dedicated inductive links for power and data telemetry as shown in Fig. 4.1 (a) [121, 245, 346]. Since each link can be optimized independently, this approach allows to achieve high data rate [170, 201, 245, 324] while maintaining high power transfer efficiency (PTE). However, this approach requires a more complicated antenna structure and suffers from cross-talk between the links [121, 345, 346, 407].

Active transmission using higher radio frequency (RF) bands as illustrated

in Fig. 4.1 (b) can also be adopted. This scheme can easily achieve the required data rate. However, it consumes an order of magnitude more energy and incurs the cost of increased complexity in circuit and antenna structures. Recently, various kinds of carrier-less pulse-based transmission technologies such as impulse radio ultra-wideband (IR-UWB) have been developed for short range communication between low-power sensors [56,97,115,263]. These type of transmitters do not need high precision frequency/phase reference generation resulting in lowered power consumption and greater amenability for adoption in wireless sensors. However, strong attenuation by electromagnetic absorption in the body at UWB bands from 3.1–10.6 GHz reduces its effectiveness in implantable applications.

The simplest approach uses a single inductive link to transfer both power and data as depicted in Fig. 4.1 (c). Typically, back scattering is used for passive backward telemetry. By not actively driving the antenna, power consumption on the implanted side can be minimized. One of the most widely used back-scattering schemes is Load shift keying (LSK), which modulates the load on the secondary side by shorting and/or opening the secondary LC tank [122,245,375]. A major drawback of LSK over a single inductive link is that the conditions for efficient power transmission and high data rate are incongruent: PTE requires a high quality factor Q of the inductive link, at the expense of reduced data rate [253]. In particular, the maximum data rate with LSK is inversely proportional to the quality factor as  $\sqrt{2}(f_{carrier}/Q)$  [96]. With simultaneous power transfer, achievable data rates have been limited to 100-500 kbps over a 13.56-MHz inductive link [227, 430].

Moreover, there are two often-neglected sources of power loss in LSK. Shorting the tank depletes all the stored energy. Also, while the tank is shorted, the rectifier does not receive power from the coil, leading to reduction of delivered power to the load. These two aspects are not typically accounted for in the reported power consumption of telemetry ICs.

Recently increased data-rates were achieved in [76] by using the transient response from passive phase shifts by shorting the secondary LC tank for a half cycle, resulting in 0.858 Mbps with simultaneous power transfer over a single in-

ductive link. However, this scheme suffers from double loss of tank energy because of complete phase reversal of LC resonance, and still is subject to the trade-off between PTE and data rate due to resonance recovery time after each bit transmission.

The increasing density and bandwidth requirements from emerging IMDs and sensors motivate development of alternative modulation schemes that obviate the PTE and data rate trade-off. To this end we present a new back-scattering data modulation method over a single inductive link that achieves high data rate at low power consumption while not compromising PTE, by recycling most of the energy circulating in the resonant tank during data transmission. Initial results reported in [138] demonstrated transmission of two data bits for every four carrier cycles while minimally depleting the resonant tank energy. For neural recording implants, forward (downlink) telemetry requires a very low data rate with infrequent transmission for sending configuration bits. Thus, such forward telemetry can share the same inductive link by time multiplexing, or very slow amplitude modulation can be used simultaneously for full duplex communication.

In this work we extend the work reported in [138] with detailed analysis and extensive experimental validation over wide range of load and geometry conditions including inter-coil distance and lateral misalignment, and a simplified and improved data reception scheme resulting in lower bit error rate at higher power transmission level. Section 4.2 presents detailed analytical and simulated results for the modulation scheme, and Section 4.3 provides architectural and implementation details. Experimental results characterizing modulation performance and comparison with state of the art are reported in Section 7.6.2. Finally, Section 7.7 concludes contributions of the work.

## 4.2 COOK Modulation Scheme

## 4.2.1 Operation Principle

The proposed uplink data modulation scheme, cyclic on-off keying (COOK), utilizes a shorting switch across the secondary LC tank to modulate data in a man-

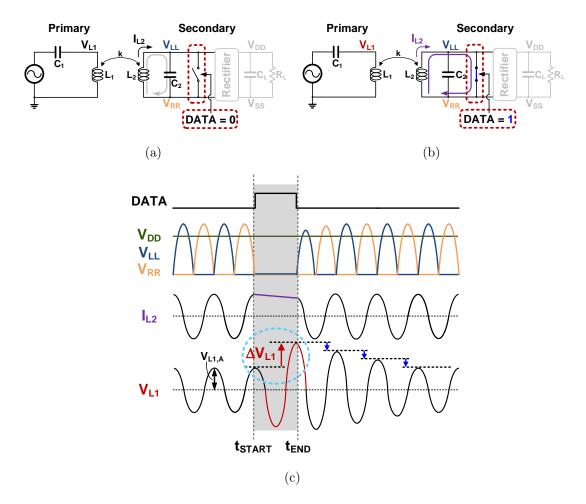


Figure 4.2: Conceptual illustration of the proposed cyclic on-off keying modulation scheme. (a) The secondary LC tank is at resonance when the switch is open (DATA = 0), cycling energy between  $L_2$  and  $C_2$  in the form of quadrature current and voltage. (b) Closing the switch (DATA = 1) when the secondary tank voltage reaches zero recirculates all resonant energy as DC current through the loop formed by  $L_2$  and the switch, while maintaining zero voltage across the tank. Reopening the switch after a complete cycle reestablishes the initial conditions for the secondary tank resonance. (c) Voltage and current waveforms throughout the modulation operation.

ner similar to conventional LSK, but with some fundamental differences. Whereas LSK modulation typically closes the switch for tens to hundreds of cycles, COOK modulation closes the switch for a single cycle only. Fig. 4.2 shows the operation of the circuit when the modulation switch is (a) open (DATA = 0), and (b) closed (DATA = 1). Unlike LSK closing and opening the switch across the secondary LC tank at random phases, COOK starts closing the switch when the voltage across the secondary inductor  $L_2$  is zero and the current through the inductor  $I_{L2}$  is at an extremum. At this time instance ( $t_{START}$  in Fig. 4.2 (c)), all the energy in the secondary LC tank is in the current through the inductor. During the synchronized shorting cycle (from  $t_{START}$  through  $t_{END}$  in Fig. 4.2 (c)), the current through the inductor and the switch remains constant, circulating and maintaining all energy (except for energy loss through parasitic resistances  $R_2$  and  $R_{sw}$  of the secondary inductor and the modulation switch) as shown in Fig. 4.2 (b). The instantaneous disruption of the inductive coupling to the primary side results in a voltage change at  $V_{L1}$ , indicated as  $\Delta V_{L1}$  in Fig. 4.2 (c).

The COOK synchronized shorting does not disturb resonance and thus, unlike most other data telemetry schemes, does not compromise the high Q of the secondary coil for resonant power transfer. Unlike LSK, the shorting does not dissipate energy in the secondary LC tank except for losses due to the parasitic resistances of the inductor and the switch. Shown in Fig. 4.2 (c), the secondary coil voltages  $V_{\rm LL}$  and  $V_{\rm RR}$  resume their normal course immediately after the COOK shorting and recover to the peak resonance amplitudes within a few cycles. In addition, a large fraction of the secondary coil energy is preserved after synchronized shorting, in contrast to LSK and other conventional schemes where this energy loss is not accounted for in the calculation of transmission energy per bit.

On the primary side, a voltage rise is immediately induced during the short of the secondary coil as shown on the bottom panel of Fig. 4.2 (c). Under typical under-coupled conditions of the inductive link, the primary coil voltage amplitude exponentially decreases to baseline after the transient increase during the short, until the next shorting cycle. Hence a rise in the peak of the primary coil voltage  $V_{L1}$  occurs only during a shorting cycle, and transmitted data can be decoded directly

from the consecutive-cycle peak differentials  $\Delta V_{L1}$  as indicated in Fig. 4.2 (c). By locking on to the phase of  $V_{L1}$  on the primary side, peak detection circuitry for data decoding is greatly simplified.

## 4.2.2 Dependence on Primary and Secondary Quality Factors

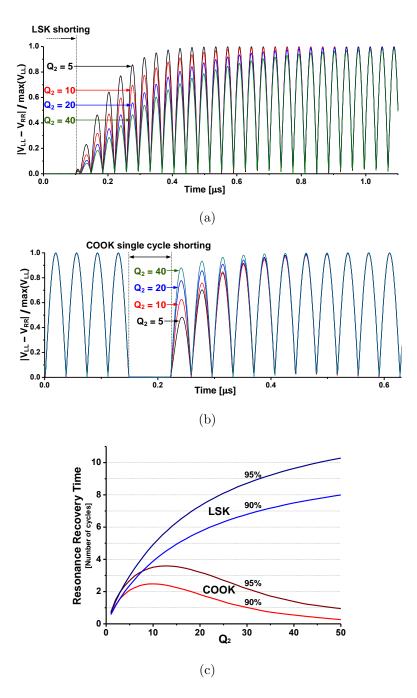
Fig. 4.3 compares simulated resonance recovery times for COOK and conventional LSK after shorting of the secondary coil switch. Recovery time for LSK modulation increases with increasing  $Q_2$  as shown in Fig. 4.3 (a). Hence, achievable data rate with LSK is inversely proportional to  $Q_2$ . On the contrary, recovery time for COOK modulation shown in Fig. 4.3 (b) is shorter, and even decreases for  $Q_2$  beyond 10 as shown in Fig. 4.3 (c). The decreasing recovery time despite longer time constant of the resonant tank at higher  $Q_2$  is mainly due to a reduced amplitude droop in the resonance voltages  $V_{\rm LL}$  and  $V_{\rm RR}$  immediately after the COOK synchronized single-cycle shorting. This is because the droop, caused by I<sup>2</sup>R losses through the parasitic resistances  $R_2$  and  $R_{sw}$  of  $L_2$  and the data-modulation switch, decreases with  $Q_2$ . As a result, the  $Q_2$  trade-off between PTE and data rate for LSK modulation is obviated for COOK modulation. As illustrated in Fig. 4.3 (c), increasing  $Q_2$  for greater PTE and energy savings reduces resonance recovery time and hence increases achievable data rate.

The initial increase of the recovery time for low  $Q_2$  is due to longer time constants of the secondary resonant tank. At higher  $Q_2$ , the recovery time decreases even with longer time constant because of a reduced amplitude droop in the resonance voltages  $V_{LL}$  and  $V_{RR}$ . As  $Q_2$  increases, the parasitic resistance  $R_2$  of the inductor  $L_2$  decreases and so does the amplitude droop. Thus, the recovery time decreases for higher  $Q_2$ .

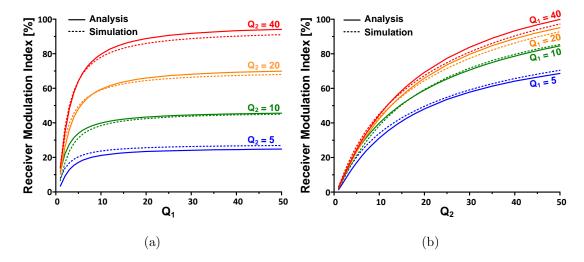
Fig. 4.4 shows the effect of  $Q_1$  and  $Q_2$  on receiver modulation index (RMI), expressed as:

$$RMI = \Delta V_{L1}/V_{L1,A} \tag{4.1}$$

where  $\Delta V_{L1}$  is the data-driven voltage increase in  $V_{L1}$ , and  $V_{L1,A}$  is the baseline



**Figure 4.3**: Simulated transient voltage waveforms of the secondary coil after shorting with (a) LSK and (b) COOK modulation. (c) Recovery time of tank resonance after shorting for LSK and COOK modulation to reach 90% and 95% of the original voltage amplitude.

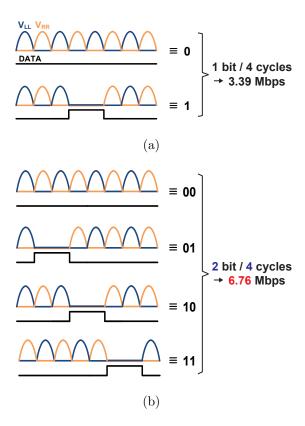


**Figure 4.4**: Analytical and simulated dependence of receiver modulation index of COOK modulation as a function of primary and secondary quality factors  $Q_1$  and  $Q_2$ . The parameters are: k = 0.15,  $L_1 = 3 \mu H$ ,  $L_2 = 470 \text{ nH}$ ,  $f_{res} = 13.56 \text{ MHz}$ ,  $C_1 = 46 \text{ pF}$ ,  $C_2 = 293 \text{ pF}$ ,  $R_{sw} = 1 \Omega$ ,  $R_{L,ac} = 1 \text{ k}\Omega$ .

amplitude of  $V_{L1}$ , denoted in Fig. 4.2 (c). RMI directly quantifies the effect of COOK data modulation on resolvable voltage differences at the receiver, and hence gives a measure for how well the data decoding can be performed. Detailed analysis of RMI is in the Appendix, the results of which are superimposed on the simulated data in Fig. 4.4. RMI increases both with increasing  $Q_1$  and  $Q_2$ , although the dependence on  $Q_2$  is much stronger.

In summary, maximizing quality factors of the inductive link in COOK modulation yields not only optimal PTE, but also maximizes data rate, maximizes decoding quality, and minimizes energy losses.

The principle of synchronous resonant data transmission also extends to the primary side for greater energy efficiency and data bandwidth of forward power and data telemetry. However, the series LC tank on the power transmitting side requires synchronous opening of the series tank [393] at the expense of stringent timing control at high-voltage power.



**Figure 4.5**: (a) Simple COOK modulation scheme with binary symbol data encoding. (b) Enhanced COOK modulation scheme with quaternary symbol data encoding resulting into two-fold increase in data rate. Both schemes support at least 6 out of 8 half cycles of power rectification over the same inductive link.

## 4.2.3 Symbol Data Encoding

As outlined in Sec. 4.2.1 and illustrated in Fig. 4.2 (c), the COOK synchronized shorting of the secondary coil produces an immediate step increase  $\Delta V_{L1}$  in peak voltage amplitude at the primary that can be detected for data decoding right upon completion of the cycle. Hence the timing of shorting cycles can be chosen to encode data symbols. For concurrent power delivery through full-wave rectification, the average number of non-shorting cycles in the encoding scheme must be maximized. Here we consider 4-cycle encoding schemes which ensure at least 6 non-shorting rectification half cycles out of 8 total half cycles, guaranteeing at least 75% of peak power delivery regardless of data. Simple binary encoding, shown in Fig. 4.5 (a), permits transmission of a single bit for every four carrier

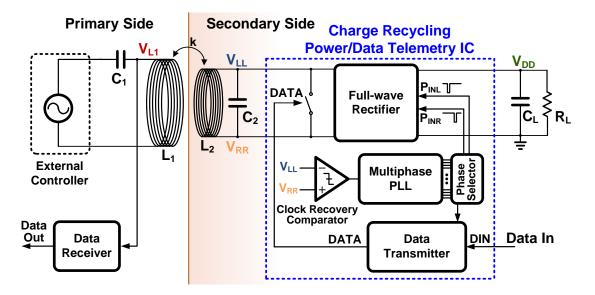
cycles, at an average 7 non-shorting out of 8 half cycles (87.5% rectification duty cycle). In contrast, varying the position of the single shorting cycle within the four-cycle time interval allows enhanced data rate. As illustrated in Fig. 4.5 (b), encoding of three positions at integer cycle offsets achieves two bits for every four carrier cycles, or a 6.78 Mbps data rate at half the 13.56-MHz carrier frequency, and an average of 6.5 non-shorting out of 8 half cycles (81.25% rectification duty cycle).

## 4.2.4 Resonance Recovery and Data Rate

Considerations of resonance recovery also govern the achievable data rate: energy in the tank needs to be sufficiently replenished between consecutive coil shortings. Hence the maximum data rate is inversely proportional to resonance recovery time. For the COOK modulation data encoding scheme at half the carrier frequency, the average interval between consecutive shortings is 4.33 carrier cycles (13 non-shorting cycles for every 3 shorting cycles). For this average interval, Fig. 4.3 (c) shows that regardless of the quality factor  $Q_2$ , the secondary tank recovers to greater than 95% of its original voltage amplitude between consecutive shortings.

## 4.3 System Implementation

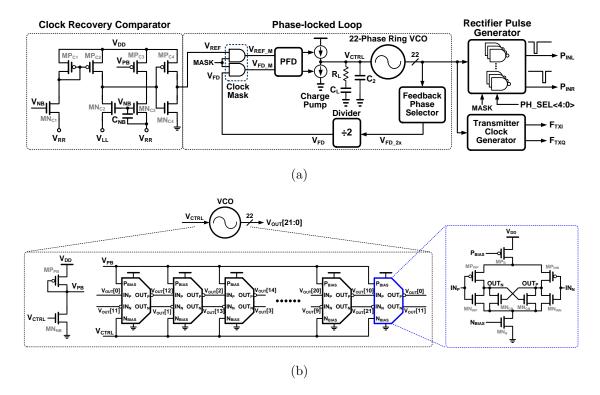
For the experimental validation a prototype COOK modulation IC and board-level telemetry system were implemented as shown in Fig. 4.6. The IC integrates a full-wave rectifier, clock recovery comparator, phase-locked loop (PLL), bias blocks, switch for data modulation, and auxiliary circuitry for data transmission and system control, as highlighted in the dashed box in Fig. 4.6. Outside the IC, the secondary side includes a parallel LC tank ( $L_2$  and  $C_2$ ), a load capacitor  $C_L$ , and a load resistor  $R_L$  for modeling load current. On the primary side, a series LC tank ( $L_1$  and  $C_1$ ) is located concentric to the parallel LC tank of the secondary side for power and data transfer. Measured geometries and parameters of the primary and secondary coils are as follows:  $L_1 = 5.27 \ \mu\text{H}$ ,  $R_1 = 5.92 \ \Omega$ ,  $Q_1 = 75.85$ ,  $D_1 =$ 



**Figure 4.6**: Block diagram of the implemented system for power and data telemetry.

6.5 cm,  $N_1 = 6$ ,  $L_2 = 2.47 \,\mu\text{H}$ ,  $R_2 = 2.79 \,\Omega$ ,  $Q_2 = 75.43$ ,  $D_2 = 4.2 \,\text{cm}$ , and  $N_2 = 8$  where  $L_{1,2}$  represent the inductances,  $R_{1,2}$  the parasitic resistances,  $Q_{1,2}$  the quality factors,  $D_{1,2}$  the diameters, and  $N_{1,2}$  the numbers of windings for the primary and secondary coils, respectively for each link. Values of the external surface-mount device (SMD) chip capacitors ( $C_1$  and  $C_2$ ) were chosen for 13.56-MHz resonance on both sides. For precise control of distance between the coils, plastic spacers of calibrated lengths were inserted in between. Data bit streams were generated in field-programmable gate-array (FPGA) on the secondary-side board, and were fed to the telemetry IC capturing the data bit stream and producing the data pulse (DATA) to drive the modulation switch across the coil accordingly. On the primary side, a signal generator generated a 13.56-MHz sine wave input to the primary LC tank. The voltage  $V_{L1}$  across the primary coil was sampled with an oscilloscope and decoded in Matlab to determine bit error rates.

Detailed circuit diagrams of major system blocks are depicted in Figs. 4.7 and 4.9. As shown on the left side in Fig. 4.7 (a), the common-gate comparator detects the timing when the voltage across the tank is zero for generation of synchronized single-cycle shortings by comparing the two tank voltages  $V_{\rm LL}$  and  $V_{\rm RR}$ . While comparators in conventional rectifiers compare coil voltages with  $V_{\rm DD}$ 

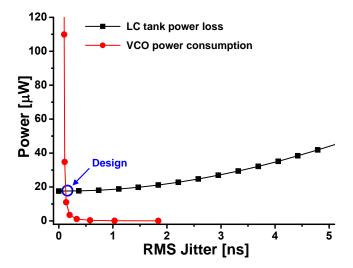


**Figure 4.7**: Circuit diagrams of (a) the comparator, PLL and pulse and clock generation blocks and (b) voltage-controlled oscillator.

to directly generate switch signals for rectification, the comparator in this work is used for clock recovery as reference to a PLL generating the switching signals instead, lowering the comparator power consumption and design complexity.

The recovered clock from the comparator  $V_{\rm REF}$  is fed as the reference clock to the 22-phase frequency-doubling type-2 PLL shown in Fig. 4.7 (a). Its voltage-controlled oscillator (VCO) consists of 11 delay cell stages as depicted in Fig. 4.7 (b). Currents to the delay cells are controlled through both pMOS and nMOS current sources for balancing the voltage range of the delay cell outputs. For differential operation, cross-coupled nMOS differential pairs are inserted across the differential outputs in each cell.

The PLL directly controls the timing of the data pulse (DATA) shorting the LC tank for data transmission. Hence PLL timing accuracy is critically important for maintaining low BER and high energy efficiency in data transmission. At the same time, the power consumption of the PLL should be contained to minimize



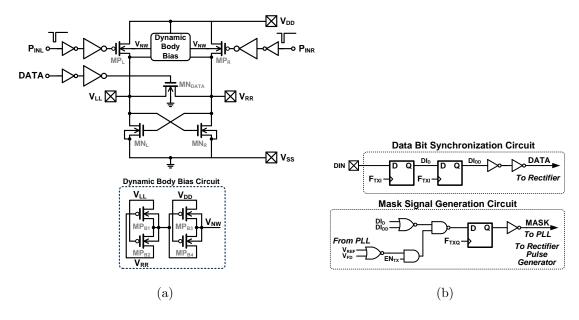
**Figure 4.8**: LC tank power loss and VCO power consumption as a function of the PLL RMS period jitter. The LC link was simulated in Cadence to obtain power loss of the secondary LC tank by varying the jitter. The PLL jitter was simulated using a behavioral simulator (CppSim [1]).

the total power for overall energy efficiency. Simulations of the trade-off between LC tank power loss and VCO power consumption as a function of RMS VCO jitter in Fig. 4.8 demonstrate minimal impact on data transmission efficacy and overall energy efficiency for VCO jitter less than 1 ns. The measured jitter of 440 ps (Fig. 4.14 (b)) is near the optimal trade-off point in Fig. 4.8.

The PLL and the rectifier pulse generator produce the phase-tuned pulses  $P_{\text{INL}}$  and  $P_{\text{INR}}$  gating the pMOS switches of the full-wave rectifier shown in Fig. 4.9 (a). During data transmission, the clocks to the PLL phase-frequency detector (PFD) are blocked by a mask signal not to disturb the PLL locking.

As illustrated in Fig. 4.10, the 22 phases of the VCO are aligned over each half cycle of the resonant tank. Among the 22 phases, one is selected to generate  $P_{\rm INL}$  and  $P_{\rm INR}$  for full-wave rectification, alternating between  $V_{\rm LL}$ -active and  $V_{\rm RR}$ -active half-cycles. Hence, any delay in the clock recovery due to the comparator can be compensated by selecting a shifted phase signal in the PLL feedback  $V_{\rm FD.2\times}$  to align the PFD feedback  $V_{\rm FD}$  to the delayed recovered clock  $V_{\rm REF}$ . As a result, design requirements on comparator delay can be relaxed to minimize power consumption.

The schematic of the full-wave rectifier with two cross coupled nMOS tran-



**Figure 4.9**: Circuit diagrams of (a) full-wave rectifier with data modulation switch across the LC tank, and (b) data bit synchronization and PLL/rectifier mask generation timing circuits.

sistors and two pMOS switches driven by buffered phase pulses  $P_{\rm INL}$  and  $P_{\rm INR}$  is shown in Fig. 4.9 (a). An additional nMOS switch across  $V_{\rm LL}$  and  $V_{\rm RR}$  is provided for COOK synchronous shorting by the buffered DATA signal during data transmission. While the body terminals of the nMOS transistors connect to the grounded substrate, the body terminals of the pMOS transistors share an n-well connected to a three-way dynamic body bias generator shown in the inset of Fig. 4.9 (a). The dynamic body bias generator tracks the highest voltage among the three source/drain voltages:  $V_{\rm LL}$ ,  $V_{\rm RR}$ , and  $V_{\rm DD}$ .

As shown in Fig. 4.9 (b), the data bit synchronization circuit receives external data bits (DIN) to generate the shorting signal (DATA), which drives the switch across the LC tank. As depicted in Fig. 4.11, this circuit synchronizes the data signal with  $F_{TXI}$ , generated from the PLL and transmitter clock generator as shown in Fig. 4.7 (a).

Shorting of the LC tank signals ( $V_{\rm LL}$  and  $V_{\rm RR}$ ) for data transmission may lead to missed clock recovery, the disturbance of the PLL loop, and current leakage in the rectifier. These potential problems are avoided in this design by generating a mask signal MASK in the circuit shown on the bottom of Fig. 4.9 (b). As shown

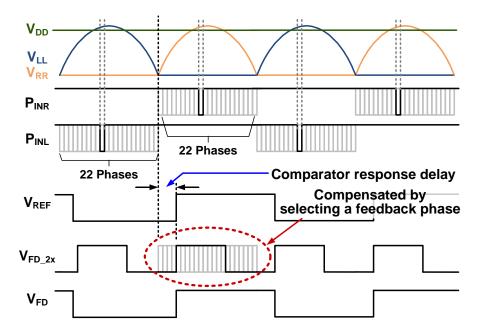


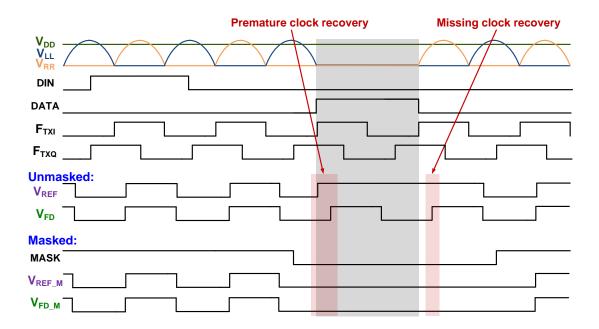
Figure 4.10: Timing diagram of the multiple phases of the PLL aligning with the LC tank signals  $V_{\rm LL}$  and  $V_{\rm RR}$ , the switching signals for rectifier  $P_{\rm INL}$  and  $P_{\rm INR}$ , and the PLL input and feedback signals  $V_{\rm REF}$ ,  $V_{\rm FD.2\times}$  and  $V_{\rm FD}$ . Comparison delay of the clock recovery comparator shown in  $V_{\rm REF}$  is compensated by feeding a delayed phase back to the PLL look.

in Fig. 4.11, the recovered clock from the comparator serving as the PLL reference clock  $V_{\text{REF}}$  rises too early during the short, and misses the next rising edge after the short. By applying the MASK signal,  $V_{\text{REF}\_M}$  and  $V_{\text{FD}\_M}$  are free of false and missing clock edges into the PLL. Similarly, the mask signal is also applied to the rectifier to prevent any reverse current leakage during the shorts.

#### 4.4 Measurement Results

The power and data telemetry IC with the proposed COOK modulation scheme was fabricated in 65 nm CMOS. A micrograph of the IC is shown in Fig. 4.12. The rectifier occupies an active area of 0.017 mm<sup>2</sup>, and other circuits including the PLL, transmitter, and bias circuits measure 0.029 mm<sup>2</sup>.

Fig. 4.13 validates the PTE of the inductive link used in this work, measured with the method outlined in [13,202] using a network analyzer. Note that the



**Figure 4.11**: Timing diagram of data bit reception and synchronization (DIN and DATA), and mask signal generation for stable PLL and rectifier operation. By masking  $V_{\text{REF}}$  and  $V_{\text{FD}}$  during data bit transmission, clock edge misalignment and edge missing issues are resolved in the masked signals  $V_{\text{REF}\_M}$  and  $V_{\text{FD}\_M}$ .

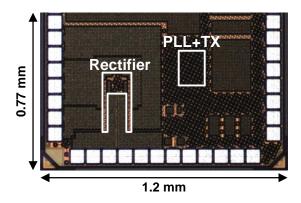


Figure 4.12: Chip micrograph.

measured quality factors of both the primary and secondary inductors are higher than 75. At  $100-\Omega$  load impedance and 1-cm inter-coil distance, the measured PTE peaks at 89.2% and decreases with increasing distance as given in Fig. 4.13 (a). Fig. 4.13 (b) shows that the inductive link is optimized around  $100-\Omega$  load impedance, for about 10-mW power transfer at 1.2-V power supply.

Fig. 4.14 (a) shows measured VCO frequency over VCO input voltage

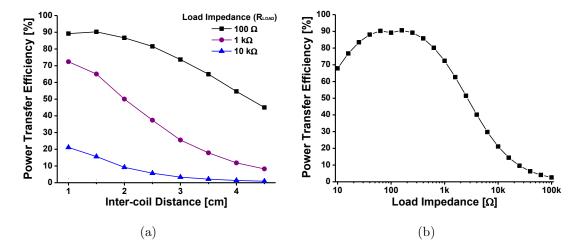
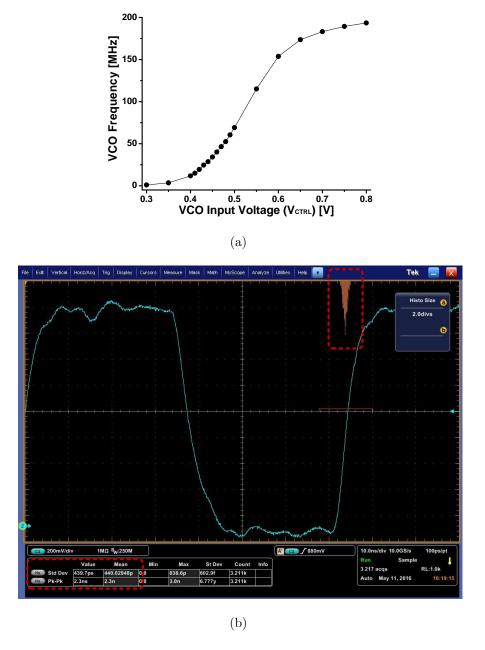


Figure 4.13: Measured power transfer efficiencies of the LC link. Geometries and parameters of the primary and secondary coils are as follows:  $L_1 = 5.27 \ \mu\text{H}$ ,  $R_1 = 5.92 \ \Omega$ ,  $Q_1 = 75.85$ ,  $D_1 = 6.5 \ \text{cm}$ ,  $N_1 = 6$ ,  $L_2 = 2.47 \ \mu\text{H}$ ,  $R_2 = 2.79 \ \Omega$ ,  $Q_2 = 75.43$ ,  $D_2 = 4.2 \ \text{cm}$ , and  $N_2 = 8$ . Values of the external surface-mount device (SMD) chip capacitors ( $C_1$  and  $C_2$ ) were chosen for 13.56-MHz resonance on both sides.  $R_{\text{LOAD}}$  is inserted across the secondary parallel LC tank to model the resistive load on the secondary side. (a) PTE as a function of distance between the primary and secondary coils at  $R_{LOAD}$  of 100 Ω, 1 kΩ and 10 kΩ. (b) PTE as a function of  $R_{\text{LOAD}}$  at 1-cm distance.

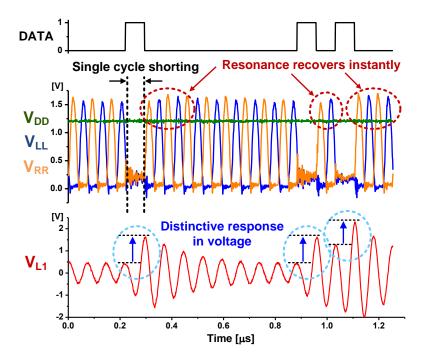
 $V_{CTRL}$ . At a  $V_{CTRL}$  around 0.45 V, the PLL output frequency is at its target of 27.12 MHz. The corresponding PLL phase noise is 104.1 dBc at 1 MHz offset. Fig. 4.14 (b) shows the measurement and histogram of the period jitter in  $F_{TXI}$ , the two-fold frequency divided signal output of the PLL. This signal at 13.56 MHz is directly utilized to generate the modulation pulse. Measured RMS jitter is 440 ps and peak-to-peak jitter is 2.3 ns, which contributes less than 4% of overall LC tank energy losses based on the results shown in Fig. 4.8. As shown in Fig. 4.8, the measured jitter is well within acceptable levels such that it does not contribute to reduction in energy efficiency and timing integrity in data transmission.

Fig. 4.15 shows typical recorded secondary and primary coil voltage waveforms during data transmission. As shown in the figure, the IC shorts the LC tank at times when the LC tank voltages  $V_{\rm LL}$  and  $V_{\rm RR}$  coincide, and maintains the shorts for single cycles. As expected, because the initial phase of the LC resonant oscillation is resumed at the end of each shorting, the LC oscillation recovers to



**Figure 4.14**: (a) Measured VCO frequency as a function of VCO input voltage. (b) RMS and peak-to-peak jitter of the two-fold frequency divided output signal of the PLL.

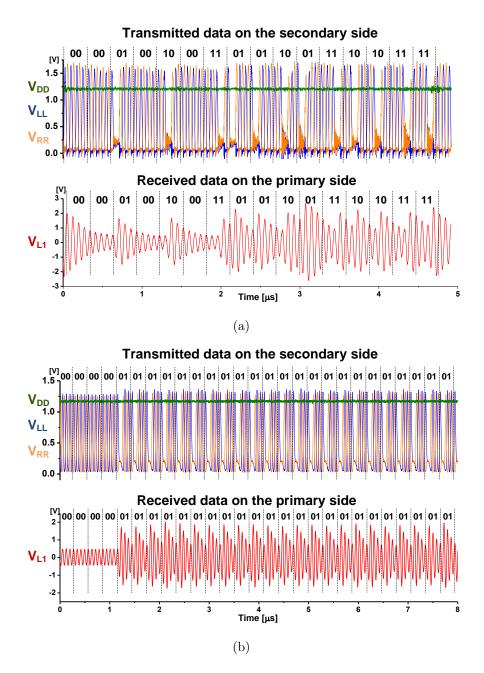
the original amplitude within a few cycles. In the bottom of Fig. 4.15, data-driven responses induced by the single-cycle shortings on the primary side are also shown. At  $V_{L1}$  the voltage across the primary coil  $L_1$ , step increases of the peak voltages are induced by the shortings on the secondary side. These step increases are clearly



**Figure 4.15**: Measured voltage waveforms of COOK modulation scheme. The secondary LC tank voltages  $V_{\rm LL}$  and  $V_{\rm RR}$  recover their amplitudes right after datadriven single-cycle shortings. In response to the shortings, clear voltage increases are induced at  $V_{L1}$  on the primary side.

distinguishable in the amplitude and timing of the voltage waveform. Other than these cycles with data-driven step increases, the peak amplitude of  $V_{L1}$  decreases monotonically or reaches an asymptote. Hence, reliable data decoding can be performed by detecting step increases in the peak voltages of  $V_{L1}$  beyond a positive threshold.

As a proof-of-concept for data transmission, a pseudo-random data bit stream was generated from sequence combinations of 16 2-bit data units, where the sequence included all possible transitions in the COOK 2-bit encoded modulation, i.e., 00-00, 00-01, 00-10, ..., 11-10, and 11-11. Fig. 4.16 (a) shows measured waveforms on the secondary and primary sides during transmission of pseudo-random data bit stream at a data rate of 6.78 Mbps, at half the carrier frequency of 13.56 MHz. The top panel of Fig. 4.16 (a) shows voltage waveforms  $V_{\rm LL}$ ,  $V_{\rm RR}$  and  $V_{\rm DD}$  on the secondary side during data transmission, showing pulse position encoding of the data over a four-cycle window. As expected, the resulting step increases in the



**Figure 4.16**: Measured voltage waveforms for data transmission and reception at a rate of 6.78 Mbps with (a) a pseudo-random bit sequence, and (b) a repeating '01' pattern sequence.

peak of voltage  $V_{L1}$  at the primary in the bottom panel of Fig. 4.16 (a) align with the timing of shortings on the transmitter side. Fig. 4.16 (b) further validates that the data transmission is robust to effects of recurring patterns in the bit stream such as repeating sequences of '01' in the data.

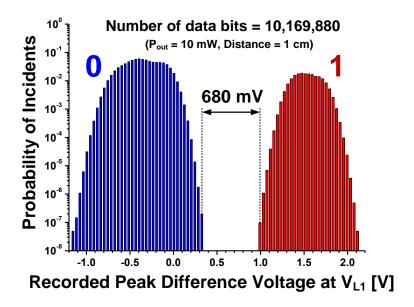


Figure 4.17: Histogram of the peak value differences of  $V_{L1}$  at  $P_{out} = 10$  mW and coil distance d = 1 cm. More than 10 million bits were transmitted and no error was detected. "1" represents the peak voltage difference when shorted, and "0" when not shorted. A large voltage gap of 680 mV is observed between the two groups.

For extensive validation, over several million bits were transmitted over the COOK link and bit-error rates (BERs) were measured under varying load, distance, and alignment conditions. Fig. 4.17 shows recorded peak-difference in voltage  $V_{L1}$  at 1 cm distance d between the two coils and at 10 mW of output power  $P_{out}$  simultaneously delivered to the load on the secondary side. Under these conditions, over 10 million bits were transferred without error in decoding, for a BER  $\leq 9.84 \times 10^{-8}$ . As shown in the figure, the voltage gap between the two groups of detected data "0" and "1" is 680 mV, providing large margin for threshold decoding. Accounting for this margin, the achievable BER by threshold decoding estimated from a Gaussian fit of the empirical probability distribution shown in Fig. 4.17 is  $2.3 \times 10^{-11}$ .

The experiment was repeated, each over 1 million transmitted bits at the same 6.78-Mbps data rate, varying three parameters: output power delivered to the load  $P_{out}$ , inter-coil distance d, and lateral misalignment between the two coils. Fig. 4.18 shows the BER and RMI varying  $P_{out}$  from 100  $\mu$ W to 11.5 mW at

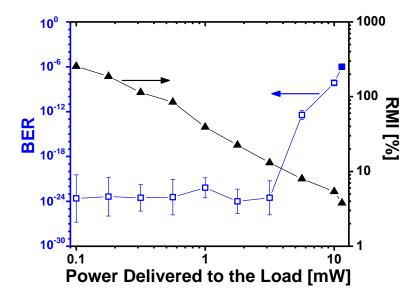
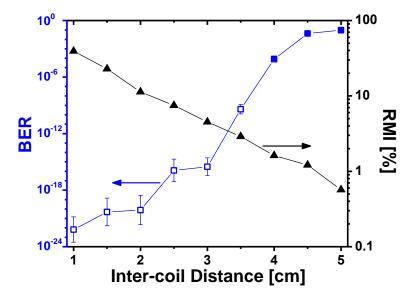


Figure 4.18: Bit-error rates (BER) and receiver modulation indices (RMI) as a function of  $P_{out}$ , the power delivered to the load, at coil distance d=1 cm. In these and the following BER experiments, filled box symbols indicate direct measurement of BER as the frequency of errors, while empty box symbols indicate estimated BER in the absence of observed errors. For the BER estimates, mean and standard deviation are shown as obtained from Gaussian fit extrapolation of the '0' and '1' histograms in Fig. 4.17.

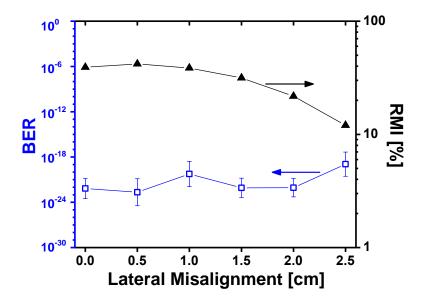
fixed 1-cm inter-coil distance. At each delivered power level, again no errors were detected. The estimated BERs using the same Gaussian-fit procedure are given in Fig. 4.18. As expected, the BER increases and RMI decreases as  $P_{out}$  increases. Up to 11.5 mW of delivered power, a BER better than  $10^{-6}$  can be achieved.

Fig. 4.19 shows BER and RMI for varying distance d between the coils, at fixed  $P_{out}$  of 1 mW. Up to 3.5 cm distance, again no errors were detected with more than 1 million bits transmitted, validating robust operation of data and power telemetry for the given coil geometries. Gaussian-estimated BERs from the voltage measurements are shown for these distances up to 3.5 cm, whereas the empirical BER measures are shown for distances from 4 to 5 cm.

Fig. 4.20 shows BER and RMI for varying lateral misalignment in the axial distance between the two coils at fixed d = 1 cm and  $P_{out} = 1$  mW, again validating robust error-free operation up to 2.5 cm in lateral misalignment, which is 77% of the primary coil radius.

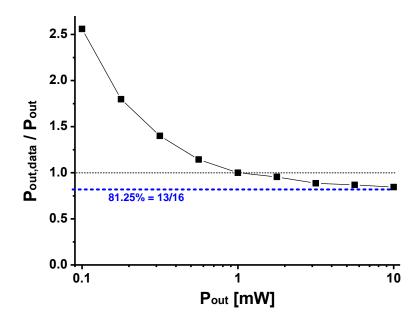


**Figure 4.19**: Bit-error rates (BER) and receiver modulation indices (RMI) as a function of coil distance at  $P_{out} = 1$  mW.



**Figure 4.20**: Bit-error rates (BER) and receiver modulation indices (RMI) as a function of lateral coil alignment at  $P_{out} = 1$  mW and d = 1 cm.

Fig. 4.21 illustrates the effect of data transmission on power delivery, revealing a perhaps counterintuitive benefit. Shown is the ratio of the amount of power delivered to the load in both cases:  $P_{out,data}$  during data transmission ("on") and  $P_{out}$  without data transmission ("off"). During data transmission, on average



**Figure 4.21**: Ratio of  $P_{out}$  (the delivered power to the load with data transmission off) and  $P_{out,data}$  (the delivered power to the load with data transmission on). The blue dashed line indicates 81.25% (13/16), the average duty cycle of non-shorting cycles for data transmission at half-carrier 6.78 Mpbs data rate.

three shortings of the LC tank occur every 16 cycles, so power is delivered only a 81.25% fraction of the time, and a corresponding reduction in the power ratio  $P_{out,data}/P_{out}$  may be expected between the "on" and "off" conditions. However, a  $P_{out,data}$  greater than 81.25% of  $P_{out}$  is observed at all measured power levels, and even greater than  $P_{out}$  at power levels less than 1 mW. The cause for the power boost in the "on" condition can be inferred from Fig. 4.15 and 4.16. As shown, each cycle shorting induces increased voltage and current swing on the primary side, which persist over several cycles, and which through induction increase the voltage and current in the secondary coil as well. The result is that during non-shorting cycles actually more power is delivered from the primary to the secondary, amply compensating for the skipped power delivery during shorting cycles. At smaller levels of  $P_{out}$ , the RMI increases with a larger voltage increase in the primary, resulting in increased power delivery  $P_{out,data}$  to the secondary. This phenomenon can be partially interpreted as a form of energy recycling. A single cycle shorting delays transmission of energy from the primary for a few cycles, which circulates in

the primary and is then added to the energy transmitted in subsequent cycles. The greater than unity ratio in  $P_{out,data}/P_{out}$  owes to a larger fraction of the secondary tank power captured by the rectifier during transient higher voltage levels.

Table 4.1: Performance Comparison of Inductive Uplink Telemetry Systems

Reference	Number	Modulation	Carrier Freq.	Data Rate	Carrier Cycle	BER	Energy per bit
	of Links	Scheme	[MHz]	[Mbps]	per bit	DLIC	[pJ/bit]
[430]		LSK	13.56	0.1	135.6	N/A	N/A
[227]	Single	LSK	13.56	0.5	27.1	N/A	N/A
[76]	Single	PPSK	13.56	0.85	16	N/A	N/A
[282]		LSK	400	1	400	$< 1.7 \times 10^{-7}$	N/A
[245]	Multiple	LSK	25	2.8	8.9	$< 10^{-6}$	35.7
[324]	Muniple	BPSK	48	3	16	$2{\times}10^{-4}$	1962
This Work	Single	COOK	13.56	6.78	2	$< 9.9 \times 10^{-8}$	9.5

Table 5.1 compares the COOK modulation scheme with state-of-the-art uplink telemetry. As expected, conventional single-link modulation schemes achieve relatively low data rates. Multiple-link schemes are capable of achieving a few Mbps with relatively low BER ( $< 10^{-6}$  for [245] and  $2 \times 10^{-4}$  for [324]), at the expense of the need for a separate link for power transfer. In contrast, single-link COOK excels in data rate even compared to the multiple-link schemes, achieving a data rate at half the carrier frequency with one of the lowest BERs. The high Q of the inductive link permits 11.5-mW power delivery to the load simultaneously with 6.78-Mbps data over 1-cm distance. The measured total power consumption of the circuits including the PLL, transmitter, bias, and switch driving buffers is 64.44  $\mu$ W at 6.78-Mbps data rate, resulting in an energy per transmitted bit, as total consumed energy divided by data rate, of 9.50 pJ/bit, an order of magnitude lower than the state-of-the-art.

#### 4.5 Conclusion

We have presented and demonstrated cyclic on-off keying (COOK) as a new modulation scheme for simultaneous transmission of power and broadband data over the same resonant inductive link. The key principle of COOK is conservation of energy in data-synchronous single-cycle adiabatic switching of the LC resonant tank during data transmission, minimizing power losses while also minimally disturbing LC resonance conditions. Time-based encoding of the data allows to transmit two bits per four carrier cycles, substantially larger than conventional transmission data encoding schemes that deplete and hence require recovery of LC tank energy. A 0.92 mm<sup>2</sup> CMOS COOK prototype in 65 nm CMOS transmits 6.78 Mbps data at 9.5 pJ/bit simultaneously delivering up to 11.5 mW of power over a single 13.56-MHz inductive link.

Chapter Four is largely a combination of material in the following two venues: Sohmyung Ha, Chul Kim, Jongkil Park, Siddharth Joshi and Gert Cauwenberghs, "Energy-Recycling Telemetry IC with Simultaneous 11.5-mW Power and 6.78-Mbps Backward Data Delivery over a Single 13.56-MHz Inductive Link," *IEEE Journal of Solid-State Circuits*, 2016 (submitted after revision). Sohmyung Ha, Chul Kim, Jongkil Park, Siddharth Joshi and Gert Cauwenberghs, Energy-Recycling Integrated 6.78-Mbps Data 6.3-mW Power Telemetry over a Single 13.56-MHz Inductive Link, *Symposium on VLSI Circuits Digest of Technical Papers*, Honolulu, HI, USA, June 10-13, 2014. The author is the primary author and investigator of these works.

## Chapter 5

# High Dynamic Range Biopotential Recording for High-Density ECoG Flexible Active Electrode Array

#### 5.1 Introduction

Electrocorticography (ECoG) records cortical biopotentials from electrodes placed on the brain surface. Recent advances in flexible integrated electronics have enabled ECoG recording with both higher spatial resolution and signal quality than obtained with conventional planar passive ECoG electrode arrays [405]. An  $18\times20$  500- $\mu$ m-spacing flexible ECoG electrode array with active multiplexing, shown in Fig. 5.1 (a), has been developed and tested *in vivo* [405], and a 1,024-channel flexible electrode array is in development. Each recording electrode is buffered and multiplexed through a two-transistor nMOS source follower and row-select switch.

The presented IC serves as column-parallel, row-multiplexing ADC at the periphery of the ECoG flexible active electrode array. As shown in Fig. 5.1 (b) for the envisioned 32×32-channel wireless array, daisy-chain I/O interconnects support cascading of several 8-channel ADC ICs to a separate wireless IC for wireless

transmission of the ECoG data.

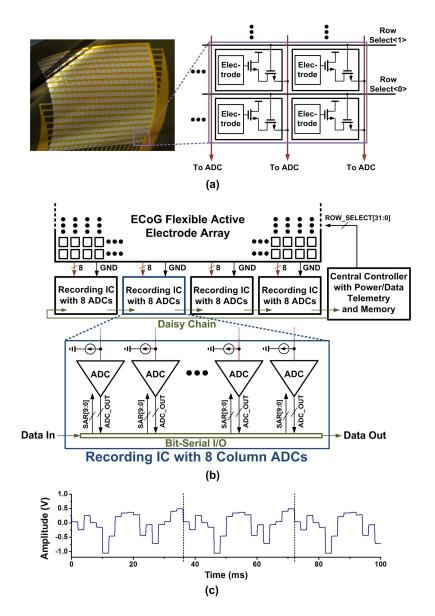
Electrochemical and process variations at each active electrode site cause voltage variations in row-multiplexed ECoG recordings up to  $\pm 1$  V, as illustrated in Fig. 5.1 (c). In a traditional biopotential acquisition system, such large offsets are eliminated through AC coupling or other high-pass filtering of the signal prior to ADC. Neither such solution, nor an alternative solution based on correlated double sampling, are available with the two-transistor row-multiplexed electrode arrangement of Fig. 5.1 (a). Therefore a resolution of 16-bit is required of the ADC to cover a 2 Vpp range of electrode offsets while resolving ECoG signals in the  $\mu$ V range.

The presented 8-channel ADC implements a hybrid architecture cascading a successive approximation (SA) ADC for coarse signal ranging, with a  $\Delta\Sigma$  first-order incremental ADC for fine ECoG signal resolution. As alternative to repeated cascaded SA- $\Delta\Sigma$  ADC operation, the successive approximation register (SAR) is optionally preloaded with a previous SAR value, stored in external frame memory and presented serially through the daisy chain, to re-establish a previous coarse range. Stitching across overlapping neighboring  $\Delta\Sigma$  ranges is implemented by incrementing or decrementing the SAR and differencing consecutive  $\Delta\Sigma$  readings accordingly to cancel effects of SA DAC nonlinearity.

#### 5.2 ADC Architecture

The architecture of the ADC is depicted in Fig. 5.2. The ADC consists of a pair of SA differential DAC capacitor arrays, two unit-size  $\Delta\Sigma$  feedback capacitors at each input side, an OTA, a latched comparator, switches, SAR logic, a counter, auxiliary digital logic and serial I/O. This architecture is similar to one proposed and demonstrated for temperature sensing in [358]. A full conversion cycle of the ADC comprises three phases: sampling, successive approximation (SA) and incremental  $\Delta\Sigma$ . The SA phase is optional and can be bypassed with a preloaded SAR value when desired.

Fig. 5.3 (a) shows a simplified circuit diagram of the ADC during the



**Figure 5.1**: (a)  $18\times20~500\mu$ m-spacing ECoG flexible active electrode array [405] and equivalent circuit diagram. (b) Envisioned wireless 1,024-channel flexible ECoG recording system using the column-parallel ADC ICs. (c) ECoG recording of a column from the flexible active electrode array showing  $\pm 1$  V variation in electrode offsets.

sampling phase. Input capacitor arrays sample input signals differentially, and inputs and outputs of OTA are connected through switches to compensate offset of the OTA while two dummy capacitors at each side connect to reference voltages, one to  $V_{REF+}$  and the other to  $V_{REF-}$ .

After the sampling phase, capacitor DACs and SAR perform successive approximation with the OTA and the comparator as shown in Fig. 5.3 (b). In this phase, the OTA serves as a preamplifier for the cascaded comparator. The dummy capacitors remain connected to the reference voltages. At the end of each comparison cycle, the outputs of the OTA are shorted by reset switch  $\Phi_{rst}$  for memoryless comparison in the subsequent cycle. Ten such cycles in the SA phase generate the 10-bit SA output.

The next incremental  $\Delta\Sigma$  phase is depicted in Fig. 5.3 (c). Now, the OTA serves as a  $G_m$ -C integrator with a capacitor across its differential outputs and the comparator as a one-bit quantizer. The two dummy capacitors on each side are connected to output of the comparator to give feedback to inputs [67]. The resolution of the  $\Delta\Sigma$  phase is reconfigurable depending on the number of cycles. 256 such cycles in this  $\Delta\Sigma$  phase result in 7-bit incremental ADC output, including one bit overlap with the SA output.

The operation of the overall ADC over the three phases is summarized in Fig. 5.4, with transient waveforms of inputs/outputs of the OTA and main digital signals in each phase.

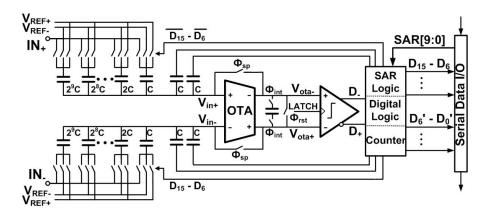


Figure 5.2: Diagram of the overall ADC architecture.

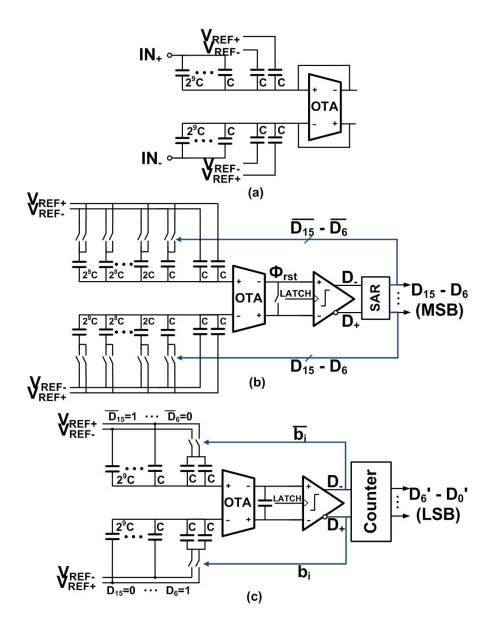


Figure 5.3: Operation phases of the ADC.

#### 5.3 Circuit Details

#### 5.3.1 Input Capacitor Array

A quad common-centroid structure was adopted in the input capacitor arrays for mismatch reduction. Each quad array contains 256 unit capacitors and is wired in two-level (split 4-4 bit) thermometer code [361]. The higher 4-b level

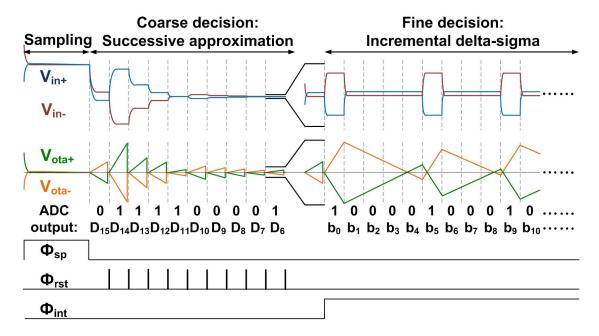


Figure 5.4: Waveforms of OTA inputs/outputs and digital signals in each phase.

thermometer code increments 15 columns of 16-unit capacitors each. The lower 4-b thermometer code increments 15 unit capacitors in the remaining 16th column.

#### 5.3.2 OTA and Comparator

The fully differential folded-cascode OTA is shown in Fig. 5.5 (a). The input differential pair is implemented with large-width source-bulk connected pMOS devices for low thermal and 1/f noise and high CMRR and PSRR. In addition to the external reset switch  $\Phi_{rst}$  in Fig. 5.2 shorting the outputs at the end of each SAR cycle, an extra internal reset switch is simultaneously activated in order to remove any residue from previous comparison for more accurate memoryless subsequent comparison. The two-stage latched comparator [400] is shown in Fig. 5.5 (b). It does not consume static power, rather consumes a fixed amount of energy for each comparison. To first order, both differential outputs of the OTA are subject to the same amount of kickback noise, and also the amount of clock feedthrough is recovered when the comparator is reset. Thus, the effect of kickback noise is negligible.

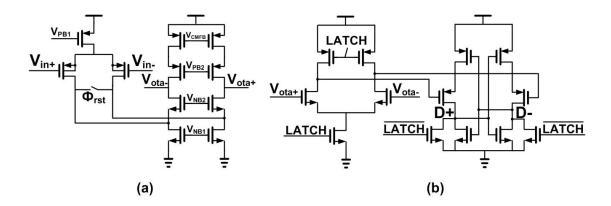


Figure 5.5: Circuit diagrams of (a) OTA and (b) latched comparator [400].

#### 5.4 Autoranging and Stitching

The electrode voltage offset varies significantly between electrodes, but is sufficiently constant between consecutive samples of the ECoG signal for each single electrode, typically contained within 2 mVpp. Hence, it is unnecessary to repeat each coarse-ranging SA ADC. In our recording IC, previous SAR outputs for each electrode may be recalled from external frame memory and delivered through the same daisy chain that conveys subsequent ADC outputs. In this manner, restored previous SAR values reconstitute previous SA DAC levels, and  $\Delta\Sigma$  conversion is run directly skipping SA conversion.

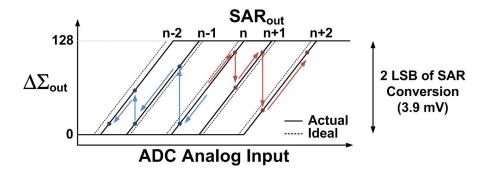


Figure 5.6: Principle of stitching in equalizing transitions between consecutive  $\Delta\Sigma$  ranges under SAR increments/decrements.

This technique is more comprehensively illustrated in Fig. 5.6. With two unit capacitors used for feedback in  $\Delta\Sigma$  phase, the  $\Delta\Sigma$  conversion range spans two SA LSBs, or 3.9 mV, providing 1 LSB overlap between adjacent SAR conversion

curves, denoted by n-2, n-1, n, n+1 and n+2 in the figure. By overriding previous SAR value, only  $\Delta\Sigma$  conversion takes place. When the  $\Delta\Sigma$  output exceeds a given positive or negative threshold, the SAR increments or decrements, hopping the SA DAC and autoranging to the corresponding neighboring  $\Delta\Sigma$  curve. Proper stitching of two adjacent conversion ranges is obtained by digitally subtracting the digital outputs for the same input in both ranges, and accumulating this difference with each transition. With the one-bit overlap, such stitching provides for seamless  $\Delta\Sigma$  conversion, essentially free of differential nonlinearity (DNL) across ranges as long as SA DNL is contained within 1 LSB at 10-b level. The measured effect of stitching on compensating for SA DNL on a sinusoidal signal crossing and spanning two  $\Delta\Sigma$  ranges is illustrated in Fig. 5.7 (a) and (b), and corresponding uniformity improvements in SFDR and SNDR across the SA ADC range are shown in Fig. 5.7 (c) and (d).

#### 5.5 Dynamic Range and Energy Efficiency

Measured SNDR and SFDR, without stitching, are shown as a function of input amplitude in Fig. 5.8 (a), and as a function of frequency in Fig. 5.8 (b). The SNDR measurements support a total input dynamic range of 84.6 dB. Peak SNDR is 70.07 dB and ENOB is 11.35 bit at 2 Vpp input amplitude. Greater SNDR and ENOB may be obtained by on-line stitching or stitching-based off-line SA DAC mismatch calibration where desired and feasible. The FFT spectra for 2-Vpp and 2-mVpp 300-Hz inputs are depicted in Fig. 5.8 (c) and (d) respectively. The measured CMRR is 87 dB for a 50 Hz 1 Vpp common-mode input, and the measured PSRR is 90 dB at 50 Hz 500 mVpp supply variation.

Fig. 5.9 shows the ADC recording of a ECoG epileptic seizure signal prerecorded from the 18×20 array in Fig. 5.1 (a) and reconstituted by a 16-b onboard DAC. The correlation coefficient between the ECoG signal and ADC output is 0.9952, and the integral error between the 16-b digital DAC input and ADC output is 2.4 LSB rms.

Measured current drawn per ADC operating at 19.5 kS/s is 19.4  $\mu$ A from

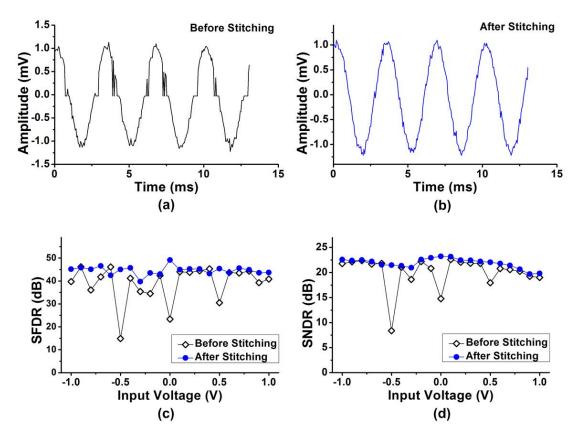
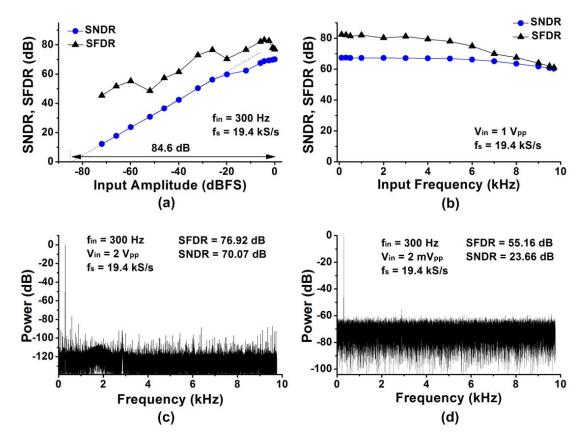


Figure 5.7: Measured results before and after stitching for 2 mVpp 300 Hz sinusoidal input.

3.3 V supply. The global clock generation circuit and serial data I/O consumes 197  $\mu$ A from 3.3 V. Total power consumption of the IC is 1.16 mW yielding an energy efficiency figure-of-merit (FOM) of 2.9 pJ per conversion level. The recording IC with eight column ADCs measures 18 mm<sup>2</sup>, with each ADC occupying 1.64 mm<sup>2</sup> in a 2P3M 0.6  $\mu$ m CMOS process. The micrograph is shown in Fig. 5.10.

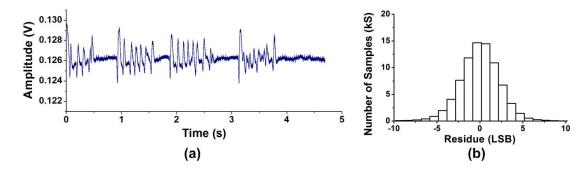
#### 5.6 Conclusion

A low-power 8-column row-multiplexing ECoG recording IC designed for use with flexible active electrode arrays has been presented. Measured characteristics of the IC and related EEG and ECoG recording ICs are summarized in Table 5.1.



**Figure 5.8**: Measured SNDR and SFDR (a) over input amplitude, and (b) over input frequency with 1 Vpp amplitude. FFT spectra (c) with 2 Vpp 300 Hz input, and (d) with 2 mVpp 300 Hz input.

Chapter Five is largely a reprint of material that appeared in the 2013 Proceedings of European Solid-State Circuits Conference: Sohmyung Ha, Jongkil Park, Yu M. Chi, Jonathan Viventi, John Rogers and Gert Cauwenberghs, 85 dB Dynamic Range 1.2 mW 156 kS/s Biopotential Recording IC for High-Density ECoG Flexible Active Electrode Array, *Proceedings of European Solid-State Circuits Conference*, Bucharest, Romania, September 16-20, 2013. The author is the primary author and investigator of this work.



**Figure 5.9**: ADC output of ECoG seizure signal pre-recorded from the array and presented through a 16-bit DAC (a), and histogram of the integral error difference between DAC applied and ADC recorded 16-bit digital signals (b).

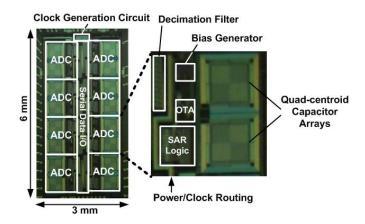


Figure 5.10: ECoG recording IC micrograph.

**Table 5.1**: Comparison between Biopotential ICs

Reference	[443]	[404]	[427]	[318]	This Work
Application	EEG	EEG	EEG	ECoG	ECoG
$Process(\mu m)$	0.5	0.13	0.35	0.35	0.6
Num. of Channels	8	1	32	32	8
Total Sampling Rate (kS/s)	8	11	10	24	156
Total Power $(\mu W)$	198	75	22	3288	1162
ENOB of ADC (bits)	10.5	10.6	9.1	10.7	11.3
FOM (pJ/conv)	17.1	4.5	4.1	107	2.9
CMRR (dB)	124	60	83.2	51	87
PSRR (dB)	89	-	75.2	69	90

## Chapter 6

# Fully Integrated Modular ECoG Recording and Stimulation

#### 6.1 Introduction

Recent demand and initiatives in brain research have driven significant interest towards developing chronically implantable neural interface systems with high spatiotemporal resolution and spatial coverage extending to the whole brain. Electroencephalography-based systems are noninvasive and cost efficient in monitoring neural activity across the brain, but suffer from fundamental limitations in spatiotemporal resolution. On the other hand, neural spike and local field potential (LFP) monitoring with penetrating electrodes offer higher resolution, but are highly invasive and inadequate for long-term use in humans due to unreliability in long-term data recording and risk for infection and inflammation. Alternatively, electrocorticography (ECoG) promises a minimally invasive, chronically implantable neural interface with resolution and spatial coverage capabilities that, with future technology scaling, may meet the needs of recently proposed brain initiatives.

# 6.2 Encapsulated Neural Interfacing Acquisition Chip (ENIAC)

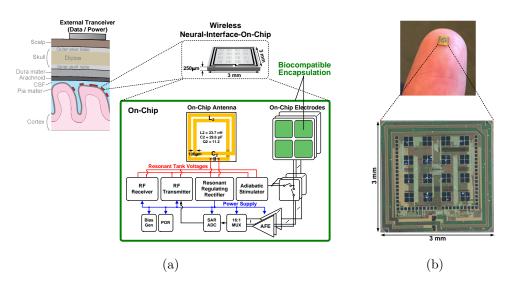


Figure 6.1: Encapsulated neural interfacing acquisition chip (ENIAC) [133,205]. (a) System diagram showing the fully integrated functionality of the ENIAC comprising on-chip antenna, electrodes, and all the circuitry for power management, communication, ECoG recording and stimulation. No external components are needed, and galvanic contact to surrounding tissue is completely eliminated in the fully encapsulated device. (b) Chip micrograph and dimensions of the prototype ENIAC.

As highlighted in Chapter 3, most current state-of-the-art ECoG ASICs rely on external components, such as flexible substates, electrode arrays, and antennas [93, 107, 217, 268, 274, 282, 316, 333, 405]. In doing so, integration of all the components into a complete system requires special fabrication processes, and, importantly, requires a large number of connections between the readout ASIC and the electrodes, which are very difficult to manage in a hermetic environment. Furthermore, electrodes typically make direct metal-electrolyte contact to the surrounding tissue, which can lead to generation of toxic byproducts during electrical stimulation. In addition, most systems do not support electrical stimulation, while those that do offer limited stimulation efficiency, or require large external components for efficient operation. Finally, the silicon area occupied by the ASIC limits the span and density of electrodes across the cortical surface. For ultra-high chan-

nel count experiments, as needed for next-generation neuroscience and called for by several brain initiatives, such limitations must be overcome.

Instead of separating the electrodes and the ASIC, a promising approach that we present below is to integrate everything on a single encapsulated neural interfacing and acquisition chip (ENIAC), including electrodes, antennas for power and data telemetry, and all other circuits and components [133]. Thus, no external wires, substrates, batteries, or any other external components are required. Complete encapsulation of the ENIAC with a biocompatible material removes direct contact to tissue, including the electrodes for recording and stimulation. As such, the chip itself serves as a complete stand-alone neural interfacing system.

As shown in Fig. 6.1 the ENIAC is designed to be small enough  $(3\times3\times0.25 \text{ mm}^3)$  to be placed among the folds and curves of the cortical surface (see Fig. 3.2 (b)), and to be implanted through small skull fissures. Hence it offers greater coverage of the cortical surface while being much less obtrusive than other minimally invasive ECoG approaches, permitting even insertion without surgery. As seen in the block diagram in Fig. 6.1, the chip contains an LC resonant tank, electrodes, recording channels, stimulator, power management units, and bidirectional communication circuits.

Its first prototype, fabricated in a 180- $\mu$ m CMOS silicon-on-insulator (SOI) process, is shown on the upper right side of Fig. 6.1. With two turns and 100- $\mu$ m thickness, the on-chip coil results in an inductance of 23.7 nH. The same single coil is shared for wireless power transfer and bidirectional RF communication. Sixteen electrodes, that can be individually configured as recording or stimulating channels, are integrated directly on the top metal layer of the chip. To enhance energy efficiency and remove the need for separate rectification and regulation stages, an integrated resonant regulating rectifier  $IR^3$  [205] is implemented. In addition, an adiabatic stimulator generates constant-current stimulation pulses from the RF power input in an adiabatic manner, much more energy efficient than conventional stimulation from DC static power supplies.

#### 6.3 Power and Communication

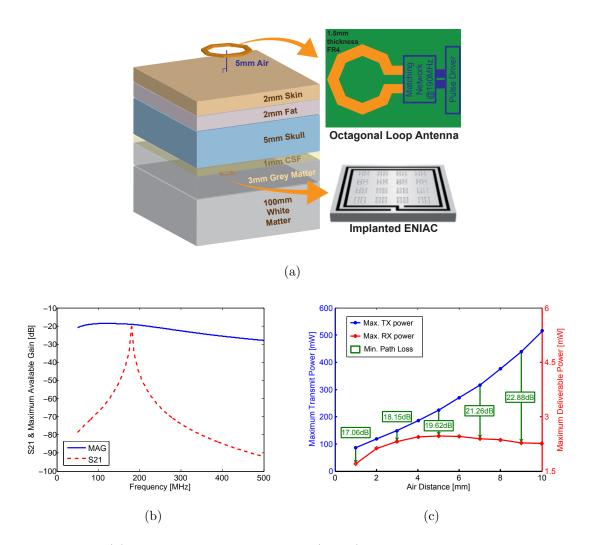


Figure 6.2: (a) 3-D finite element method (FEM) modeling of brain tissue layers between external transmitter and implanted ENIAC. (b) Simulated forward transmission coefficient  $S_{21}$  and maximum available gain (MAG) from the transmitter to the implanted ENIAC. The optimal frequency for wireless power transfer is around 190 MHz. (c) Maximum transmit power limited by specific absorption rate (SAR) and maximum receivable power at the implanted ENIAC, as a function of distance of air gap between the transmitter and the scalp, optimum around 5 mm. Green arrows denote minimum path losses at each air distance.

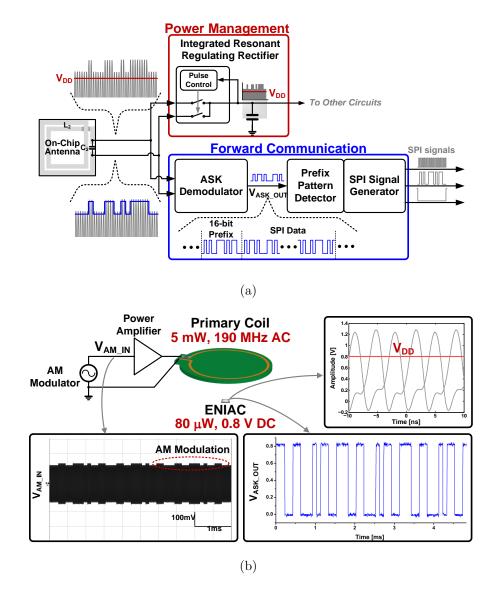
As highlighted in Sec. 3.3.1, RF inductive powering is the most efficient means for power delivery at this implantation depth, and has been adopted in ENIAC. To model the inductive link through tissue, a detailed finite element

method (FEM) model of the octagonal loop transmitter antenna and the 3×3-mm<sup>2</sup> ENIAC shown in Fig. 6.2 (a) was constructed in ANSYS HFSS, using tissue spectral permittivity and absorption properties as shown in Fig. 3.5 (b) and (c). Optimal power transfer between the transmitter coil and ENIAC is reached at a resonance frequency of 190 MHz as shown in Fig. 6.2 (b). At this frequency, substantially more than the required 2 mW power can be delivered under the Specific Absorption Rate (SAR) limit (2 W/kg in IEEE std. 1528). Fig. 6.2 (c) shows the maximum transmit power at the SAR limit, and corresponding maximum deliverable power at the implant, for varying distance of the air gap between the loop transmitter and the scalp. The optimal distance for maximum power delivery, trading between reduced SAR-limited transmit power at lower distance and increased path losses at higher distance [175], was found to be around 5 mm.

ENIAC minimizes power losses in the received power from the RF coil owing to an integrated resonant regulating rectifier (IR<sup>3</sup>) architecture that combines power management stages of rectification, regulation, and DC conversion, eliminating typical losses due to inefficiencies at each stage when implemented separately. As illustrated in Fig. 6.3 (a), IR<sup>3</sup> generates a constant power supply 0.8 V independent of fluctuation in the LC tank voltages. IR<sup>3</sup> operates by adapting both width and frequency of pulsed rectifier switching based on a feedback signal derived from  $V_{DD}$  [205].

Concurrently, the amplitude-shift-keying (ASK) demodulator tracks and amplifies the envelope of the LC tank voltages to decode transmitted configuration data as illustrated on the bottom of Fig. 6.3 (a). The ASK communication is used to wirelessly configure the operation modes and parameters of the chip. To synchronize data reception, a 16-bit pre-determined identification code is used as prefix followed by serial peripheral interface (SPI) signals.

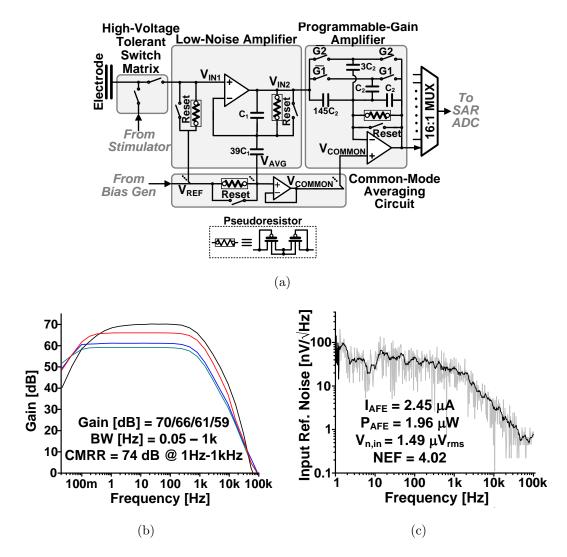
Fig. 6.3 (b) shows test setup and sample data for the IR<sup>3</sup> power delivery and the ASK data transmission. For these tests, a primary coil built on a printed-circuit board was placed 1 cm above the ENIAC. The top right panel in Fig. 6.3 (b) shows the measured coil voltages simultaneously rectified and regulated by the IR<sup>3</sup> [205, 206] to produce the supply voltage  $V_{DD} \approx 0.8$  V. The total transmitted



**Figure 6.3**: (a) System diagram of ENIAC power management and ASK forward communication, sharing the same single on-chip loop antenna. The integrated resonant regulating rectifier (IR<sup>3</sup>) generates a stable 0.8 V DC output voltage directly from the 190 MHz RF coil voltage while the ASK demodulator decodes and amplifies the modulated signal. (b) Simplified test setup for wireless powering and communication along with measurement samples at the transmitter and the receiver.

power is about 5 mW, of which around 80  $\mu$ W is received by the ENIAC. The bottom panel of Fig. 10 (b) shows shows the AM modulated input on the primary side, and the demodulated ASK signal in the ENIAC.

#### 6.4 Recording



**Figure 6.4**: (a) Circuit diagram of the recording module of ENIAC with 16 analog front-end (AFE) channels, 16:1 analog multiplexer (MUX), and successive approximation register (SAR) analog-to-digital converter (ADC). (b) Measured frequency and noise characteristics of one AFE channel.

The recording module integrates 16 analog front-ends (AFEs), a 16:1 analog multiplexer (MUX), and an analog-to-digital converter (ADC) as shown in Fig. 6.4 (a). Each of the 16 capacitively coupled electrodes is connected either to its local AFE channel, or to the global stimulator, multiplexed by a high-voltage tolerant switch matrix. The AFE amplifies the biopotential  $V_{\rm IN1}$  from the capacitively coupled non-contact electrode with two amplification stages and a common-

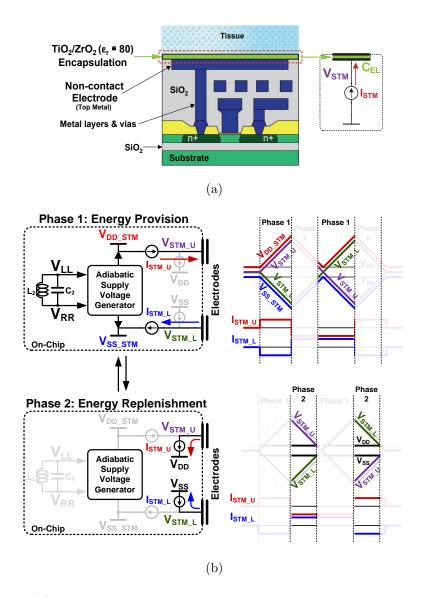
mode averaging circuit. The common-mode averaging circuit constructs a single reference signal  $V_{\text{AVG}}$  as the average of all  $V_{\text{IN}i}$  electrode voltages through capacitive division. Similar to differential recording across a pair of adjacent electrodes (Sec. 3.2.1), the internal common-mode reference  $V_{\text{AVG}}$  allows single-ended recording over all 16 electrodes without the need for a distal external ground connection. A pMOS-based pseudoresistor (in the inset of Fig. 6.4 (a)) is used to set the DC operating point at  $V_{\text{REF}}$  for the capacitive division to allow for very high (T $\Omega$ -range) resistance in very small silicon area [92, 148].

The first low-noise amplifier stage has a non-inverting configuration with a feedback capacitor  $C_1$  and a common-mode coupling capacitor of  $39 \cdot C_1$ , which connects to the common-mode averaging node  $V_{\text{AVG}}$ , resulting in a differential voltage gain of 40 (V/V).  $V_{\text{AVG}}$  is buffered and used for common-mode rejection in the second AFE stage. The second AFE stage provides variable gain by manipulating the connections of two capacitors, connected either as input or as feedback capacitors [145, 465]. Output signals of the AFEs are multiplexed and buffered to the SAR ADC, which has time-interleaving sample-and-hold input DACs to ensure longer sampling time, leading to power saving in buffering the input DAC of the ADC.

Measurement results for the AFE, characterizing its frequency response and noise performance, are shown in Fig. 6.4 (b) and (c). Variable 50-70 dB gain is supported, and the input-referred noise is 1.5  $\mu$ V<sub>rms</sub> at 2.45  $\mu$ A supply current for a noise efficiency factor (NEF) of 4.

#### 6.5 Stimulation

As illustrated in Fig. 6.5 (a), ENIAC on-chip electrodes are implemented on top metal, as used for bond pads and on-chip inductors. The exposed electrodes allow for direct coating with a thin film of high-k materials such as  $\text{TiO}_2/\text{ZrO}_2$  to achieve high capacitance for high charge delivery capacity. With 30-nm coating and  $250\times250~\mu\text{m}^2$  area, the coupling capacitance  $C_{EL}$  is about 1.5 nF, one order of magnitude smaller than that of a platinum electrode of same area. Total deliverable

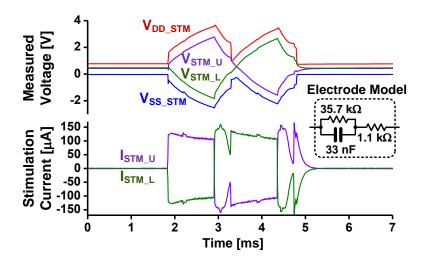


**Figure 6.5**: (a) Simplified stack-up of ENIAC showing an electrode coated with high-k materials for capacitive interface. (b) Principle of adiabatic stimulation with ENIAC. During the first phase, adiabatic voltage rails are generated directly from the LC tank for energy efficient stimulation. During the second phase, the energy stored across the capacitive electrodes is replenished for further energy savings.

charge per phase  $Q_{ph}$  can be expressed as:

$$Q_{ph} = I_{STM} \cdot T_{ph} = C_{EL} \cdot V_{DD\_STM} \tag{6.1}$$

where  $I_{STM}$  is the stimulation current,  $T_{ph}$  the time duration of the phase, and  $V_{DD\_STM}$  the total voltage dynamic excursion. Relatively low capacitance  $C_{EL}$  can thus be compensated by an increased total voltage excursion  $V_{DD\_STM}$  to



**Figure 6.6**: Measured stimulation voltage and current waveforms with platinum model electrode.

deliver the required charge per stimulation phase. In order to achieve  $Q_{ph}=10$  nC per stimulation phase, needed for effective neural stimulation under typical electrophysiological conditions, a dynamic voltage rail with a total excursion of more than 8 times the static supply voltage  $V_{DD}$  (= 0.8 V) is required.

Conventionally, this can be implemented by generating the required high power supply voltages and supplying constant currents from fixed power rails. However, drawing currents in this manner incurs large energy penalties due to the large voltage drop across the current source.

Instead, a much better way to perform stimulation is to slowly ramp up the supply rails in an adiabatic fashion to minimize the voltage drop across the current source. Generation of the adiabatic voltage rails can be implemented in various ways. External capacitors [192] or an external inductor [18] can be employed. Alternatively, pulse width control in rectifier can be used [52]. However, all of these methods have output ranges within the LC tank swing voltages or  $V_{DD}$ . Recently, on-chip charge pumps are employed to generate a wide voltage excursion for adiabatic stimulation [36]. Because this approach utilizes the DC power supply as the input of charge pumps, series of power efficiency loss cannot be avoided in implantation settings. In addition, this method could generate discrete levels of power supplies only, so the energy losses due to the voltage drops across the

current source were considerable.

In contrast, ENIAC implements an adiabatic stimulator that generates, at minimum energy losses, ramping voltage power rails with greater than 8 times the voltage excursion of the LC tank, and with no need for any external components. Consistent with the observations in Sec. 3.2.1, differential adiabatic stimulation across a selected pair of electrodes is implemented, since the miniaturized and enclosed ENIAC system permits no access to a distal ground electrode. As illustrated in Fig. 6.5 (b), the ENIAC stimulator operates in two phases. During the first phase, constant complementary currents are provided through the differential capacitive electrodes. The ramping voltage adiabatic power rails  $V_{DD,STM}$ and V<sub>SS\_STM</sub> providing the complementary currents are generated directly from the LC tank utilizing a foldable stack of rectifiers. During the second phase energy is replenished, by returning the charge stored on the electrode capacitors to the system  $V_{DD}$  and  $V_{SS}$  for reuse by other ENIAC modules. For triphasic rather than biphasic stimulation, as shown, the two phases are repeated but now with opposite polarity. This is accomplished by swapping the electrode connections through the switch matrix prior to executing the same two-phase sequence. Finally, the electrodes are shorted to even out any residual charge on the electrode capacitors. Fig. 6.6 shows measured voltage and current waveform for the triphasic stimulation with a platinum model electrode, consistent with the model in Fig. 6.5 (b), and showing 145  $\mu$ A of current delivered per electrode channel. This is 4 times larger than other integrated ECoG systems even though no external components are used and system volume is substantially smaller (Table 6.1).

#### 6.6 Conclusion

This chapter makes the case for a new type of device that promises to expand the applications of implantable brain monitoring: modular  $\mu$ ECoG. We demonstrate a new approach to miniaturization of modular  $\mu$ ECoG with our fully integrated Encapsulated Neural Interfacing Acquisition Chip (ENIAC). This system-on-a-chip is capable of recording, stimulation, wireless power conditioning

**Table 6.1**: Comparison of State-of-the-Art Wireless Integrated ECoG Recording and Stimulation Systems

	Reference	[61]	[15]	[268, 318] WIMAGINE	[38, 282]	This Work ENIAC	
Numb	per of Channels	8 <sup>a</sup>	64	32	64	16	
7	Геchnology	$0.18~\mu\mathrm{m}$	$0.18~\mu\mathrm{m}$	$0.35~\mu\mathrm{m}$	$65~\mathrm{nm}$	$0.18~\mu\mathrm{m}$ SOI	
Pow	er Supply [V]	1.8	1.8	3.3	0.5	0.8	
Total Power	r Consumption [mW]	2.8	$5.4^b$	72.1	0.22	< 0.1	
IC	$\rm Area\ [mm^2]$	13.47	$26.83^{b}$	$86^{b}$	5.76	9	
Total Sys	tem Volume [mm <sup>3</sup> ]	N/A	$77,200^{c}$	>4,000	N/A	2.25	
		LC, electrodes	LC, electrodes	LC, electrodes	L, electrodes		
Extern	nal Components	Antenna	Antenna	Antenna	Antenna	None	
		Capacitor	Off-chip ICs for powering and communication				
AFE	Input Ref. Noise $[\mu V]$	5.2	5.4	1	1.3	2.5	
AFE	NEF	1.8	N/A	4.5	4.8	4.0	
ADC	Туре	SAR	SAR	SAR	VCO	SAR	
ADC	Resolution [bits]	10	12	12	15	10	
Stimulation	Max. Output Current $[\mu A]$	30	No	No	No	145	
M. 1 D .	Frequency [MHz]	13.56	0.266	13.56	300	190	
Wireless Powering	Antenna	Off-chip	Off-chip	Off-chip	Off-chip	On-chip	
	F2 1	OOK	Zigbee	N.	No	ASK	
Communication	Forward	$401\text{-}406~\mathrm{MHz}$	N/A	No		$190~\mathrm{MHz}$	
	D 1 1	OOK	IR-UWB	FSK	LSK	LSK	
	Backward	$401\text{-}406~\mathrm{MHz}$	$7.3\text{-}8.5~\mathrm{GHz}$	$402\text{-}405~\mathrm{MHz}$	$300~\mathrm{MHz}$	$190~\mathrm{MHz}$	

 $<sup>^</sup>a8$  recording channels and 2 stimulation channels.  $^b\mathrm{Only}$  for the data acquisition unit.  $^c\mathrm{Only}$  for the communication unit.

and bidirectional communication without the need for any external components. Its major specifications, performances and functionalties are summarized in comparison with other state-of-the-art ECoG interface systems in Table 6.1. Having a fully integrated neural interface system, including electrodes and antenna is a new milestone for miniaturization that sets the stage for exciting clinical and research developments.

Chapter Six is largely a combination of material in the following two venues: Sohmyung Ha, Abraham Akinin, Jiwoong Park, Chul Kim, Hui Wang, Christoph Maier, Patrick P. Mercier and Gert Cauwenberghs, "Silicon Integrated High-Density Electrocortical Interfaces," *Proceedings of the IEEE*, 2017, *Accepted*. Sohmyung Ha, Abraham Akinin, Jiwoong Park, Chul Kim, Hui Wang, Christoph Maier, Gert

Cauwenberghs and Patrick P. Mercier, A 16-Channel Wireless Neural Interfacing SoC with RF-powered Energy-Replenishing Adiabatic Stimulation, *Symposium on VLSI Circuits Digest of Technical Papers*, Kyoto, Japan, June 16-19, 2015. The author is the primary author and investigator of this work.

# Chapter 7

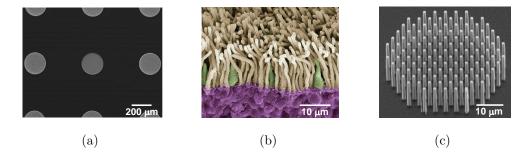
# Towards High-resolution Retinal Prostheses with Direct Optical Addressing and Inductive Telemetry

# 7.1 Introduction

Recent initiatives are targeting development of innovative neural technologies to advance the spatial and temporal resolution of neural recording and stimulation towards dynamic mapping of brain function [378,379]. As one of the most accessible regions of the brain, the retina is the most characterized and mapped in its different cell types and their connections [105, 237, 247, 250, 344]. Despite the substantial progress in retinal activity mapping, retinal prostheses for remediating blindness have remained at an early stage of technological development. More than three million people suffer from vision loss due to photoreceptor degeneration by retinitis pigmentosa (RP) and age-related macular degeneration (AMD) worldwide [143,300,377,380]. Therefore, restoration of the retina's lost sensory functions in the visually impaired through new-generation high-resolution implantable device technologies is of paramount importance [99,244,378,415,466].

A retinal prosthesis replaces the phototransduction function of degenerated photoreceptor cells by applying electrical stimulation to the remaining tissue to induce visual sensation. Patients with inheritable RP begin losing rod photoreceptors, suffering from poor night vision and peripheral vision loss, while AMD first affects the dense concentration of cones around the fovea, the optical focus of the retina [85, 108, 414]. The damaged photoreceptors cannot be repaired by any treatment or surgery available to date, and can eventually progress to a complete loss of vision [55, 339, 414]. Thankfully, even in the case of severe photoreceptor loss, the visual information pathway, from retinal neurons including bipolar cells and retinal ganglion cells (RGCs) to visual processing neurons in the visual cortex, largely remains intact [259,325]. To restore vision, surviving retinal neurons may be activated by electrical stimulation. To date, such electrical prosthetic intervention to the intact retinal neurons is the most viable and promising avenue to restore vision in patients with RP and AMD while other approaches utilizing optogenetic [28, 35, 106, 130, 223, 315, 390], photo-thermal [119, 249, 338, 417, 450] or ultrasonic [119, 262, 285] stimulation have been investigated as alternatives.

Many research groups around the world have been developing various types of retinal prostheses over the last two decades, and some are even available commercially [166, 467]. Major developments in retinal prostheses [4,6,7,20,40,50,74,75,89,91,112,113,129,155,158,166,167,173,174,184,191,214,220,230,243,251,252,280,286,295,317,319,321,340,342,364,365,381,385–388,408,410,422,423,437,440,



**Figure 7.1**: Retina and electrode geometries. (a) Planar platinum gray electrodes of the *Argus II* retinal prosthesis [461]; (b) Retinal photoreceptor cells with rods (yellow) and cones (green) [Image: Science Photo Library]; and (c) fabricated silicon nanowires at the same spatial magnification as (b).

Electrode Electrodes Clinical Trial Device Image Sensor Powering References Team Name Location Method Location Number Diameter Pitch Acuity Argus I Second Sight External camera Inductive Epiretinal 16  $260 \mu m^{1}$  $800 \mu m$ 20/3240 [50, 89, 167, 437] Argus II Second Sight External camera Inductive Epiretinal  $200 \mu m$  $525 \mu m$ 20/1260 [155, 166, 461]EPIRET3 RWTH External camera Inductive Epiretinal 25  $500 \mu m$ [214, 319] $100 \mu m$ Light perception IRIS I IMI External camera Inductive Epiretinal 49  $360 \mu m$ N/A Object localization [158] IRIS III Pixium Vision External camera Inductive Epiretinal 150 N/AN/AUnder human trials BRI BRIP External camera Inductive 15  $400 \mu m$ N/A Preclinical [191, 317, 340, 381] STSOsaka Univ.-NIDEK External camera Inductive Suprachoroidal<sup>2</sup> 49  $500 \mu m$  $700 \mu m$ Object localization [6, 112, 113]Wide-view BVA-Sydney External camera Inductive Suprachoroidal  $98^{4}$  $430 \mu m$  $1 \mathrm{mm}$ Preclinical [129, 184, 252, 422, 453] N/A BVA-Melbourne External camera  $Wired^5$ Suprachoroidal  $33^{6}$  $600 \mu m^6$  $1 \mathrm{mm}$ 20/8397 [20, 286, 342] N/A SNU External camera Inductive Suprachoroidal<sup>3</sup> 16  $200 \mu m$ N/A Preclinical [173, 174, 462] Alpha IMS Retina Implant Internal MPDA Inductive Subretinal 1500  $50 \mu m^7$  $70 \mu m$ 20/546[321, 364, 365, 467] N/A Tohoku Univ Internal MPDA Wired<sup>5</sup> Epiretinal 100  $70 \mu m$  $150 \mu m$ Preclinical [91, 220, 230, 280, 410] N/A NAIST Internal MPDA Wired<sup>5</sup> Suprachoroidal  $108^{8}$  $100 \mu m$  $240 \mu m^{9}$ Preclinical [295, 385-388] Internal MPDA Light<sup>10</sup>  $9 \mu m^{11}$  $20/400^{12}$ [74, 75, 244]ASR. Optobionics Subretinal 5000 N/A Bio-Retina Epiretinal N/AN/A Preclinical [4] PRIMA  ${
m Light}^{13}$  $75 \mu \text{m}^{15}$ Preclinical [7, 40, 243, 251, 408] Stanford-Pixium Ext. camera + MPDA Subretinal 142  $20 \mu m$ NTHU-NCTU  ${
m Light^{13}}$ Preclinical Ext. camera + MPDA Subretinal 16  $75 \mu m^{16}$ 490*µ*m [423, 440] N/A

**Table 7.1**: Comparison of Retinal Prostheses

453, 461, 462, 467] are summarized in Table 7.1 according to key characteristics and clinical test status. To the best of our knowledge, eight retinal prostheses have undergone clinical trials in human patients reporting some level of artificial sensation of light [20, 75, 112, 158, 166, 167, 319, 467], and at least one is ongoing [7]. Furthermore, some patients with implanted prostheses have demonstrated regained ability to distinguish line orientations, recognize objects, perform simple navigation tasks, and/or even read large letters [87, 166, 364, 365, 467]. Regained visual acuity (VA) in some patients reached about 20/1200 [155, 166, 364, 365, 467], and a VA up to 20/546 has been reported in one patient [364, 365]. However, more than 75% of patients who received retinal implants could not achieve measurable VA [166, 364, 365]. Thus far, none of the reported devices are capable of overcoming the legal blindness threshold of 20/200 VA [2]. Significant improvements in the VA achievable by retinal prostheses are necessary to restore blind patients autonomy

<sup>\*</sup> Second Sight: Second Sight Medical Products, Inc., IRIS: Intelligent Retinal Implant System, RWTH: Rhine-Westphalia Institute of Technology Aachen, IMI: Intelligent Medical Implants, ASR: Artificial Silicon Retina, BRI: Boston Retinal Implant, BRIP: Boston Retinal Implant project, STS: suprachoroidal transretinal stimulation, SNU: Seoul National University, BVA: Bionic Vision Australia, MPDA: micro photodiode array, NAIST: Nara Institute of Science and Technology, Stanford-Pixium: Stanford University and Pixium Vision S.A., NTHU: National Tsing Hua University, and NCTU: National Chiao Tung University

<sup>&</sup>lt;sup>1</sup>Argus I was implanted in six patients (P1-P6). The electrode diameters were 520 μm in P1 and P2, 260 μm in P3, and alternating 260- and 520-μm electrodes were used in P4, P5, and P6 [89].

<sup>2</sup>Intra-scleral. <sup>3</sup>Both suprachoroidal and subretinal. <sup>4</sup>14 channels; each channel with one stimulation electrode and six return electrodes. <sup>5</sup>Percutaneous wires used for tests only; inductive powering to be used for future generations. <sup>6</sup>3 × 400-μm diameter and 30 × 600-μm diameter stimulating electrodes. <sup>7</sup>Square electrode with 50 μm × 50 μm. <sup>8</sup>12 unit chips, each with 9 electrodes. <sup>9</sup>240μm within the unit-chip and 620 μm between two adjacent unit chips. <sup>10</sup>Ambient light was used without any additional power. Light intensity was not sufficient to generate stimulation currents above threshold [244, 415]. <sup>11</sup>Square electrode with 9 μm × 9 μm. <sup>12</sup>Indirect improvement. <sup>13</sup>Laser light; intensity of ambient light is not sufficient to elicit visual sensation through the devices. Thus, an external system including light amplification and laser projection is used. <sup>14</sup>500 pixels in the first generation, and 2,000 in the second. <sup>15</sup>Estimated value from text and figures. <sup>16</sup>Square electrode with 75 μm × 75 μm.

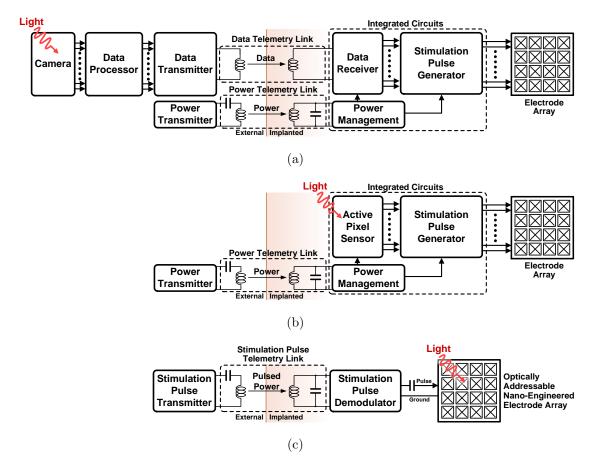


Figure 7.2: Architecture types of retinal prosthesis: (a) Conventional system with external camera and inductive power link [7, 20, 112, 158, 166, 167, 173, 184, 319, 340], (b) Alternative system with implanted light sensor [91, 388, 467], and (c) Proposed system with stimulation pulse telemetry link and direct optically addressed nanowire-based electrode array.

and improve their quality of life.

Improvements in VA are tightly related to the prosthesis spatial resolution, which is generally proportional to size and pitch of electrodes [244]. By definition, normative 20/20 VA implies visual ability to resolve an angle of one arc min, 1/60 degree [350]. Because one degree of vision spans 288  $\mu$ m on the retina [219], one arc min corresponds to a spatial resolution of about 5  $\mu$ m. For a VA of 20/20, an electrode pixel size of 5  $\mu$ m is required while the 20/200 VA blindness threshold requires 50  $\mu$ m [300]. However, most current retinal prostheses feature electrodes of larger size and pitch, and some larger by more than an order of magnitude

(Table 7.1). For instance, for the 60-element array of 200  $\mu$ m electrode diameter and 525  $\mu$ m spacing in figure 7.1 (a) [461], the maximum measured VA was 20/1260 [155, 166], limited by the dimension of the electrodes [244]. For normal vision electrode dimensions need to be reduced to around 5  $\mu$ m resolution, matching the physiological scale of photoreceptors as seen in figure 7.1 (b). To this end, our research group has been pursuing a high spatial-resolution electrode array made with vertically aligned nanowires as shown in figure 7.1 (c) and further elaborated in section 7.3.

Along with VA, the total range of the restored visual field is equally important for patients to perform useful navigation functions [453]. A larger number of electrodes are required to sense a larger visual field at the same resolution. The minimum electrode number required for pattern recognition or reading text is estimated to be about 600 [54, 248, 355, 382]. Implementation of retinal prostheses counting more than 600 electrode channels poses several tough challenges. From a systems standpoint, main challenges are in 1) electrode material and fabrication (high charge injection capacity per given electrode area, and high-density fabrication), 2) connectivity (lead connections between the application-specific integrated circuit (ASIC) and the electrode array), 3) circuit complexity and integration (stimulus pulse generation for high number of channels), and 4) telemetry (wirelessly transferring the stimulation data and power). Substantial engineering efforts are required to tackle these challenges. Advantageously, some of the challenges can be overcome and circumvented by architectural design, as presented next.

# 7.2 Types of System Architectures

Typically, retinal prostheses are categorized into three kinds by their electrode locations: epiretinal, subretinal, and suprachoroidal implants. This distinction informs strengths and limitations involved in the electrode location, but it fails to differentiate key system-level attributes. Alternatively, classifying differences in hardware architecture highlights more fundamental properties of the systems' functionality. Two important aspects in system-level classification are

image sensor location, and powering method. Following these criteria, the retinal prostheses in Table 7.1 are divided into several groups.

Image sensors are located either externally, typically as a camera, or internally, typically as a micro photodiode array (MPDA). Similarly, powering methods are distinguished mainly in two ways: inductive electromagnetic telemetry, and laser light projection. Powering through electromagnetic induction is one of the most prevalent wireless powering methods, developed specifically for retinal prostheses [7,20,91,112,158,166,167,173,184,319,340,388,467] and with parallel developments for general biomedical applications [23,138,172,182,213,215,268,320,406]. The first human implanted retinal prosthesis used incident light onto the retina to power an implanted MPDA [74,75], but the light intensity turned out too weak to generate sufficient stimulation current [244,415]. For this reason, subsequent research groups have used amplified laser light, which requires an external system for visual acquisition (i.e., camera) and amplification by laser projection, to provide enough power to the implanted MPDA [4,243,440].

The architecture types distinguished by these criteria are illustrated as block diagrams in figure 7.2. The topology depicted in figure 7.2 (a) is most widely adopted by research groups for epiretinal, subretinal and suprachoroidal implants as seen in table 7.1. In this system, a vision sensor and image processor are placed on the external side. The external unit performs image processing to extract relevant information for stimulation and delivers the resulting information to the implanted unit over an inductive link. Based on the received data, the ASIC implanted in the eye generates and supplies stimulus currents to the retina through an electrode array. This architecture has a couple of advantages. First, it offers the flexibility of programming video processing algorithms owing to the external position of the camera and image processor; replacement and amendment of algorithms are straightforward. In addition, the inductive power link is able to carry a substantial amount of power.

However, this approach involves considerable hardware complexity both on the external and the internal sides. Also, it necessitates heavy data traffic from the external camera over the inductive link through the stimulation pulse generators to the electrode array. Compared to other hardware topologies, it faces severe challenges in scaling towards larger count electrode arrays, in particular for implementing more than the 600 channels required for useful vision (section 7.1). Additionally, this approach does not intrinsically track the eye's saccadic movement necessitating unnatural head scanning by the patient to integrate the visual scene [60,99,415]. Typically, an eye tracking system is required to couple gaze direction with the visual scene. Alternatively, a miniaturized camera could be implanted in the crystalline lens [363].

The second architecture depicted in figure 7.2 (b) has been employed in epiretinal, subretinal, suprachoroidal prostheses [91, 220, 294, 321, 385–388, 467]. This topology integrates light sensing located in the eye near the retina. Unlike the approaches using an external camera, the movement of the light sensor is directly coupled with that of the eye ball so that an eye tracking system is unnecessary. As seen in figure 7.2 (b), the external system is much simpler. In addition, it does not require high-throughput data telemetry for relaying visual information from the outside to the implanted side. As a result, larger numbers of electrode channels can be readily achieved; for instance, Alpha IMS features 1,500 channels [467]. The increased spatial resolution of the retinal prosthesis comes at the expense of increased hardware complexity and power consumption on the implant side for image sensing, high-dimensional processing, and electrode-specific pulse generation.

Towards high-resolution retinal prostheses, a few groups have investigated another approach that implants only MPDAs without additional circuitry inside the eye. Based on this approach, a retinal implant powered using only incident light onto the retina was developed as early as the 1990s, and a prototype was implanted into human patients as the first retinal prosthesis clinical trial in 2000 [74,75]. While the device improved visual acuity in retinal regions outside of the implant due to a reported neurotropic effect, no visual sensation directly due to the implant was observed in blind patients [244,415]. Hence, subsequent research groups employed an external system with image acquisition and laser projection in order to deliver sufficient power to the implanted MPDA [4,243,440]. Recently,

feasibility of this approach has been demonstrated in vitro [251] and in vivo [243]. This scheme overcomes the limitations of direct visual optical powering at the expense of increased complexity and power of an external goggle system for high-intensity infrared (IR) laser projection. However, the required IR irradiance for supra-threshold stimulation is 0.55 to 10 mW/mm<sup>2</sup>, which is more than 100 times higher than the irradiance onto the retina under bright sunny conditions [243].

Here we present an alternative such architecture for high-resolution retinal prostheses with direct optical addressing and optoelectronic gain by inductive powering. As shown in figure 7.2 (c), the proposed architecture includes a silicon nanowire-based optically addressable electrode array [198], an external stimulation pulse transmitter, an internal demodulator, and an inductive link. This topology enables the use of low-intensity incident light to directly deliver the stimulus, owing to high sensitivity of the photovoltaic array with additional optoelectronic gain by pulsed voltage biasing. This allows greater densities of photosensitive electrodes without the need of individual lead wires and high-data telemetry in addressing stimulation sites, simplifying integration and packaging. Hence a single inductive link solution is sufficient for both power and data delivery, directly providing optoelectronic gain to the electrode array, and stimulation pulse parameters. Power transfer over the inductive link is pulsed over time only when needed to drive stimulation, allowing event-driven operation and minimizing power losses [135].

As seen in figure 7.2 (c), the proposed architecture incurs low hardware complexity on both the external and internal sides. The implant connects to the nanowire electrode array and ground electrode only over two wires, and in addition to the inductive link secondary coil contains only a few additional circuit components including resonant tank capacitor, rectifying elements, and charge-balancing series capacitor. Its external unit with stimulation pulse transmitter is as simple as the architecture in figure 7.2 (b). Scaling this architecture to higher resolutions with larger number of electrodes incurs almost no increase in hardware beyond the density and size of the electrode array itself.

Three key system elements of the proposed architecture are described, analyzed, and experimentally validated in the following three sections. Section 7.3

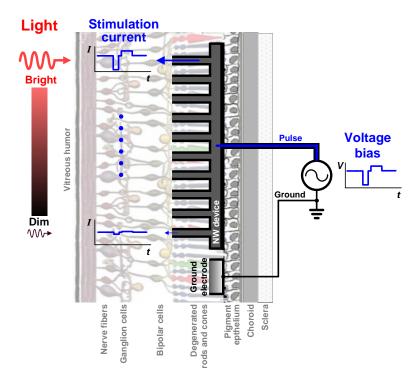
covers the photosensitive nanowire-based electrode array; section 7.4 covers charge balancing considerations addressed in the system; and section 7.5 describes circuit architectures for wireless stimulation pulse telemetry. System validation with *ex vivo* experiments follows in section 7.6. Finally, section 7.7 concludes by summarizing our contributions.

# 7.3 Light-Sensitive Electrode Array

Vertical nanowire (NW) arrays have been extensively investigated for phototransduction due to their relatively high quantum efficiency [48, 160, 162, 188, 301, 302, 371, 429, 464] with applications to solar cells, light detectors, and others [64, 83, 84, 161, 212, 225, 352, 370, 371, 373]. Our research group has been developing NW-based light-sensing electrode arrays for retinal prostheses [196–200]. Here we summarize characteristics and functionality of the NW device for light-induced neural stimulation.

# 7.3.1 Light-induced stimulation with the NW device

The NW array operates as an optoelectronic neural stimulator simultaneously performing two critical functions: i) light detection and ii) neural stimulation. Figure 7.3 illustrates the simplified concept of the light-induced stimulation
with a NW electrode array implanted in the subretinal region. The array has a single lead wire connection to the stimulation pulse generator, with another lead wire
to the nearby ground electrode. When a biphasic pulsed voltage bias is applied
across the NW device between the lead wires, the device produces a corresponding
biphasic pulsed current that scales with locally incident light intensity on the NW
device. NWs that are illuminated by higher intensity incident light produce stimulation currents into the retina of higher amplitude, while other NWs under lower
intensity illumination supply lower stimulation currents. Hence the incident light
gives direct spatial control over stimulation limited by the spatial resolution of
the NW array. In addition, the timing of stimulation is directly controlled by the
timing of the electrical bias pulse supplied over the telemetry link. These relations



**Figure 7.3**: Conceptual illustration of direct light-induced and voltage-pulsed subretinal stimulation with the nanowire (NW) device. The background retinal image is reproduced with permission from [218].

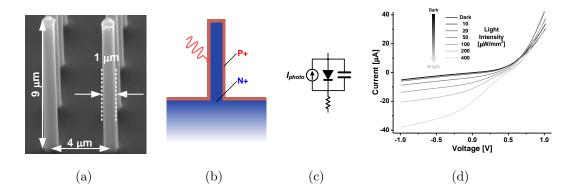
can be conceptually represented, to first order, with the following equation:

$$I(x, y, t) = G_{photo}(x, y) \cdot V(t)$$
(7.1)

where I(x, y, t) is the stimulation current produced by the NW-based electrode array at location (x, y) in the retinal plane and at time t;  $G_{photo}(x, y)$  is the local photo-induced effective conductance of the NW-based electrode array; and V(t) is the pulsed voltage bias. That is, the current I(x, y, t) is modulated spatially by the incident light  $G_{photo}(x, y)$ , and temporally by the bias V(t).

# 7.3.2 Photodiode-type (PN-type) NW device

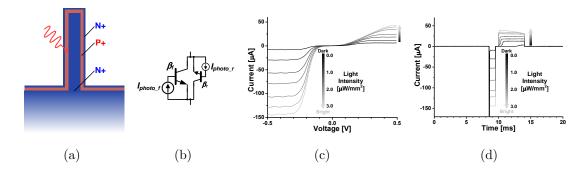
The NW device comprises a grid of vertical NWs etched on a silicon substrate. As shown in figure 7.4 (a), a single NW measures 1- $\mu$ m diameter, 9- $\mu$ m height and 4- $\mu$ m pitch, comparable to dimensions of retinal photoreceptor cells as shown in figures 7.1 (b) and (c). As shown in figure 7.4 (b), the device forms



**Figure 7.4**: (a) Dimensions, (b) simplified cross section and (c) equivalent circuit model of a photodiode-type NW. (d) Measured current-to-voltage (I-V) curve of a 200  $\mu$ m × 200  $\mu$ m 2,500-element parallel-shunt NW device (Sec. 7.3.4) under various light intensity conditions.

a p-n junction implementing a micro-sized photodiode, modeled schematically in figure 7.4 (c). The photocurrent  $I_{photo}$  scales with the intensity of the incident light as shown in the measured I-V curves in figure 7.4 (d).

The use of vertical silicon NWs provides two main advantages over other types of phototransducers such as flat and thin-film microphotodiodes [40, 408]. First, the NW has higher light absorption efficiency. The NW geometry has been shown by our research group and others to reduce losses in light-to-electricity conversion and improve light absorption [160, 188]. This high absorption efficiency in NWs is due to an increased light path length enhancement factor leading to better light trapping along the length of the NW structure [160, 188]. On the contrary, flat and thin microphotodiodes have shorter light path length, resulting in reduced efficiency due to photon quenching [48,161,162,188,301,302,371,429,464]. Second, NWs perform carrier collection and charge separation more efficiently [188]. In order to be collected by photodiodes, electrons must diffuse into the metal contact. The NW geometry of a core-shell structure provides fast radial charge separation that in turns allows for efficient carrier collection through band conduction [80, 188].



**Figure 7.5**: (a) Cross section and (b) equivalent circuit model of an NPN-type NW phototransistor device. (c) Measured I-V curve and (d) pulse response of the model phototransistor device under various light intensities.

# 7.3.3 Phototransistor-type (NPN-type) NW device

Additional optoelectronic gain can be obtained from active current amplification in bipolar junction transistors (BJT) formed by a silicon NW device with an additional junction as shown in figures 7.5 (a) and (b). The NPN junction can be modeled as two BJT devices in parallel, one in each direction providing forward and reverse current gains  $\beta_f$  and  $\beta_r$  in amplifying the base photocurrents. The relative current gains in forward and reverse directions depend on the doping profile of the two junctions. To explore the parameter space and physically emulate and optimize the NPN-type device under varying conditions, we implement the circuit model with discrete components (SFH 3310 and LPT 80 A from Osram Opto Semiconductors). DC voltage-to-current (I-V) curves measured under different illumination conditions are shown in figure 7.5 (c). For pulse response characterization, a cathode-leading voltage biphasic pulse was applied to the device through a charge-balancing AC-coupling capacitor. The measurements in figure 7.5 (d) show light intensity modulation of the current amplitude in response to the voltage pulse consistent with the model (7.1).

## 7.3.4 Fabrication procedure

We fabricated the photodiode-type NW devices using the following procedure [198,463]. Photolithography was used to pattern nickel (Ni) dot arrays on an

n-type silicon (Si) substrate with a doping concentration of  $1.1 \times 10^{-18}$  cm<sup>-3</sup>. The Ni dots were formed by E-beam evaporation, then the base resist was removed by a lift-off process while keeping the Ni dots as etch masks. After solvent cleaning, the samples were etched for 40 minutes using reactive ion etch (RIE) and inductively coupled plasma (ICP) process (gases: C4F8 and SF6). Then, the Ni dots were etched off via wet etching. Subsequently, the Si NW radial p-n junctions were formed by boron spin-on-dopant (SOD) and diffusion. The Si NW samples were treated in close proximity to a source wafer coated with layer of SOD under rapid thermal annealing at 800°C in N<sub>2</sub>; then went through a drive-in process in a furnace at 800°C for 3 hours in N<sub>2</sub>. The oxide formed during the diffusion process was removed using buffered oxide etcher (BOE). Next, the NWs were passivated with a layer of Al<sub>2</sub>O<sub>3</sub> via atomic layer deposition. The NW arrays were then embedded in transparent polydimethylglutarimide (PMGI) resist (MicroChem Corp., USA), and O<sub>2</sub> plasma dry etch followed by BOE wet etch was used to expose the tips of the NWs. A transparent ITO layer was deposited on top of the device, connecting exposed tips to bundle multiple nanowires into individual electrode sites. Electrodes of various sizes were implemented to trade between spatial resolution and intensity thresholds (Sec. 7.6.2). For the experiments reported here, a  $200 \ \mu \text{m} \times 200 \ \mu \text{m}$  die was cut to form a single electrode combining 2,500 NWs, and a 30 nm layer of iridium oxide was sputtered on top of the ITO layer as the external interface contact.

# 7.4 Capacitive Coupling Interface

Charge balancing between anode and cathode phases of a stimulation waveform, with near-zero net DC charge transfer over the electrode, is crucial for chronic neural stimulation. Any unbalanced residual charge induces irreversible electrochemical reactions resulting in electrode dissolution, which typically generates toxic byproducts.

The NW devices are subject to typical photovoltaic non-linearities in their I-V characteristics as shown in Section 7.3. In addition, these non-linearities vary

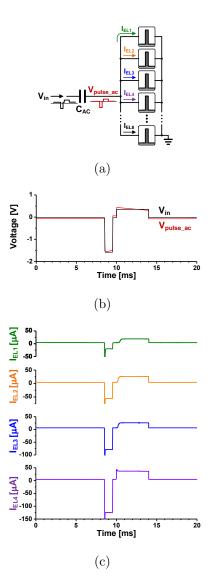
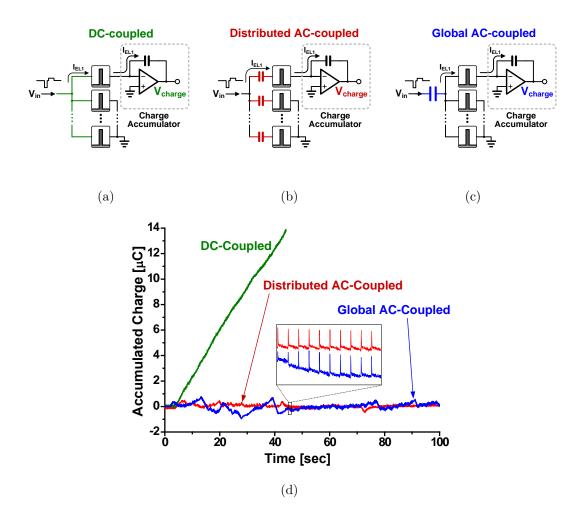


Figure 7.6: (a) Test setup with an array of the phototransistor devices and a single AC-coupling capacitor  $C_{AC}$  (22  $\mu$ F). (b) Voltage waveforms of the applied biphasic input pulse  $V_{in}$  and the measured AC-coupled pulse  $V_{pulse\_ac}$ . (c) Simultaneously measured currents from four devices under non-uniform light illumination conditions.

over light intensity. Due to the light-dependent non-linearity, it is impractical to control charge balancing in the stimulation current by manipulating amplitude and duration of the positive and the negative phases of the voltage bias pulse across the array.

A capacitor in series with each electrode is commonly used in stimulation



**Figure 7.7**: Validation of charge balancing across a single device in the phototransistor array under different coupling conditions: (a) DC-coupled, (b) distributed AC-coupled, and (c) global AC-coupled. (d) Measured accumulated charge for all three configurations under time-varying non-uniform intensity illumination conditions.

circuits since it inherently blocks any DC current through the electrode [163]. However, the large size of the series capacitor ( $\sim$ 100 nF) required for effective stimulation [347] prohibits scalable high-density integration for each electrode in the array [298]. As a practical solution, a single AC-coupling capacitor  $C_{AC}$  is inserted between the light-sensitive electrode array and the pulse generator as illustrated in figure 7.6 (a). The series capacitor shared among multiple electrodes also ensures net zero charge transfer into tissue. Although individual charge balancing for each electrode is not guaranteed, this technique has been beneficially

employed in neural stimulator applications [366]. As shown in the Appendix, the coupling capacitance  $C_{AC}$  primarily serves a DC shift in the voltage bias under periodic pulsed stimulation. This DC shift depends on light illumination in order to dynamically balance the net charge on average, independent of the device nonlinearity.

To validate the operation of the light-sensitive electrode array with the AC-coupling capacitor, we performed experiments with eight of the phototransistor devices connected as shown in figure 7.6 (a). Figure 7.6 (b) shows the applied voltage waveform  $V_{in}$  and the resulting voltage bias across the array  $V_{pulse\_ac}$ , coupled to  $V_{in}$  through  $C_{AC}$  (= 22  $\mu$ F). In addition to the expected DC shift,  $V_{pulse\_ac}$  shows slight relaxation in the biphasic pulse waveform due to the finite RC time constant. Although the voltage pulse  $V_{pulse\_ac}$  is shared across all devices, the resulting individual device currents, measured in figure 7.6 (c), are different due to differences in local light intensity.

To validate individual charge balance across devices in the array in figure 7.6 (a), the current through one of the devices was integrated by a capacitive transimpedance amplifier (TIA) for net charge monitoring. Three different configurations were tested as depicted in figure 7.7: (a) the voltage input was directly connected (DC-coupled) to the array, (b) each device was supplied an individual series capacitor for distributed AC-coupling, and (c) a single series capacitor was shared across the array for global AC-coupling as in figure 7.6. The transient voltage  $V_{charge}$  at the output of the TIA represents the excursion in the total amount of accumulated charge across the feedback capacitor over the measurement period to indicate charge balancing performance. The measured excursions  $V_{charge}$  in the three configurations under intensity-varying illumination conditions are shown in figure 7.7 (d). In the DC-coupled case, the voltage clearly diverges as time goes by, indicating lack of charge balancing. As expected, distributed AC-coupling ensures charge balancing at the individual device level. However, the measurements under global AC-coupling show that despite temporary fluctuations in net charge across the device, the long-term charge remains balanced. The temporary fluctuations are due to local light intensity variations, which average out on the longer term

owing to uniformity in average lighting conditions.

These experiments constitute a simplified model of the electrode-retina interface that does not account for variations in electrode impedance which may give rise to local charge imbalances even under uniform illumination. However, the shunting effect of volume conduction in surrounding retinal tissue mitigates any such local charge imbalances. We further note that the any residuals due to mismatch are small compared to the charge imbalance that is intrinsic to purely passive approaches with monophasic pulsed photocurrents carried through microphotodiodes.

# 7.5 Wireless Telemetry for Stimulus Pulse Delivery

This section addresses a central system component of the proposed architecture described in figure 7.2 (c) and section 7.2: the combination of wireless power and data telemetry for stimulus pulse generation. Three architectures for wireless pulse delivery for neural stimulation are considered here: *i*) direct inductive, *ii*) rectified direct inductive, and *iii*) amplitude-modulated. We analyze the first two architectures and demonstrate why they are inadequate for long-term implantable use. Then, the third architecture is proposed and experimentally validated.

#### 7.5.1 Direct inductive stimulation

One of the simplest candidate architectures for wireless pulse delivery is one that couples the LC resonant tank directly to the electrodes as depicted in figure 7.8 (a). To be effective, the stimulation pulse frequency must operate near the resonant frequency of the inductive link. This architecture has been studied for implanted neural interfaces and shown impractical due to fundamental gaps in these frequencies [135]. Space constraints on the implant side severely limit the size and quality factor of the implanted coil at frequencies lower than 1 MHz. Conversely, the dynamics of electrode-tissue interface and neuron membrane excitability are

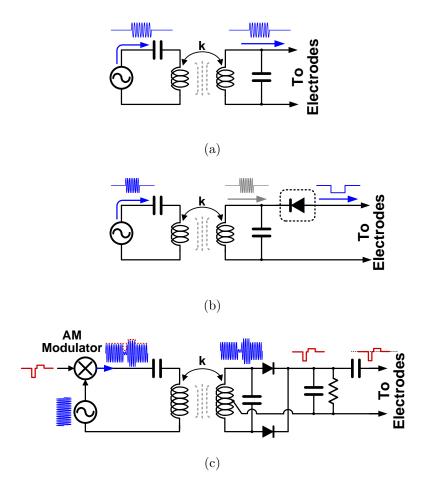


Figure 7.8: Wireless telemetry pulse delivery architectures for (a) direct inductive stimulation, (b) rectified direct stimulation, and (c) the proposed amplitude-modulated direct stimulation.

severely suppressed at frequencies above 100 kHz [109].

#### 7.5.2 Rectified direct inductive stimulation

To bridge the gap between operational frequency ranges for high-Q induction and neural stimulation, we consider rectification of an incoming sine-wave pulse train to generate a voltage pulse on the electrodes tracking the carrier envelope. The rectification could be explicit using a discrete series diode as shown in figure 7.8 (b), or may be intrinsic to the electrode. For instance, our previous work [196, 198–200] and section 7.3 shows such rectification in a PN-junction nanowire array for photoconductive and neural stimulation in a retinal prosthe-

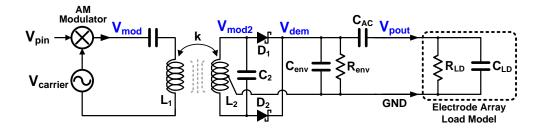
sis. Amplitude and width of the rectified stimulation pulse are easily controlled by changing the parameters of the input pulse train on the external side [135]. However, this architecture can produce only monophasic pulses and hence is problematic for charge-balanced stimulation.

#### 7.5.3 Proposed architecture

The proposed architecture for wireless stimulus pulse generation is shown in figure 7.8 (c). On its external side, a stimulation pulse is amplitude-modulated onto a carrier of sufficiently high frequency (i.e. in the MHz range) for the inductive link to be efficient. The modulated carrier signal is wirelessly transferred, and is demodulated on the implant side to recover the stimulation pulse. The demodulator on the implant side performs full-wave rectification and low-pass filtering to track the envelope using two low-threshold diodes and a few passive circuit components, extending on previous half-wave rectification architectures [372]. In addition, an AC-coupling capacitor is inserted in series for charge balancing.

This architecture offers the following advantages over more conventional architectures for wireless pulse delivery. First, it only uses a few simple circuit components, obviating the need for ASICs or other complex circuits for data communication, voltage regulation and stimulation waveform shaping. Second, this architecture only uses a single inductive link for both data and power transfer, relaying the pulse waveform as the envelope of the delivered power. Third, full control over the pulse waveform shape in the modulator on the external side gives great flexibility in tailoring globalstimulation parameters in the implant, including pulse frequency, width, height, slope, and gap time in typical biphasic stimulation waveforms.

The complete circuit diagram of the implemented architecture is shown in figure 7.9, including a load model of the electrode array. The prototype was implemented with a PCB-based inductor and off-the-self components. Specific circuit parameters for the target stimulation parameters and load conditions are as follows:  $L_2 = 1.88 \ \mu\text{H}$ ,  $C_2 = 293 \ \text{pF}$ ,  $R_{env} = 100 \ \text{k}\Omega$ ,  $C_{env} = 100 \ \text{pF}$ ,  $C_{AC} = 1 \ \mu\text{F}$ ,  $R_{LD} = 100 \ \text{k}\Omega$ ,  $C_{LD} = 1 \ \text{nF}$ , and  $D_{1,2}$  are Schottky diodes (UPS115Ue3,



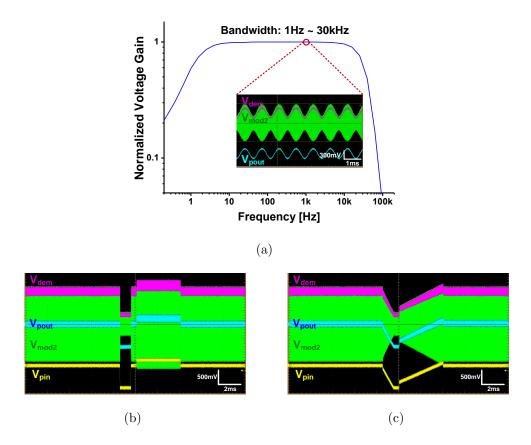
**Figure 7.9**: Detailed circuit diagram of the proposed wireless telemetry pulse delivery system. The electrode array is modeled as a resistive and capacitive load in the inset.

Microsemi Corporation, CA, USA).

The measured frequency response transfer function  $|V_{pout}(j\omega)/V_{pin}(j\omega)|$  of the prototype is given in figure 7.10 (a), showing a bandwidth from 1 Hz to 30 kHz, adequate for typical stimulation waveform delivery. The prototype was tested with two types of stimulation pulse waveforms to illustrate its versatility in configuring waveform parameters to varying electrode-tissue interface conditions: biphasic constant voltage stimulation, and biphasic constant current stimulation. Ramping of the voltage bias is generally needed for constant current stimulation in order to compensate for capacitive loading of the electrode-tissue interface, thereby avoiding the typical decaying exponential relaxation of stimulation current for constantvoltage stimulation. With the increasing electrode-tissue impedances at shrinking electrode dimensions for high-resolution prostheses, such capacitive loading effects become dominant. Figures 7.10 (b) and (c) show the input waveform  $V_{pin}$  and the resulting modulated, demodulated and AC-coupled output voltage waveforms  $V_{mod2}$ ,  $V_{dem}$  and  $V_{pout}$ . As shown, the output waveform  $V_{pout}$  received on the implant side reproduces the target input waveform  $V_{pin}$ . Width, height and shape of the stimulation pulse can be easily programmed on the external side.

# 7.6 Proof-of-concept System Validation

As a proof-of-concept in validating the entire system in a biological setting, this section presents the integration of all above system components and demonstrates neural responsivity to combined light and electrical activation *ex vivo* in



**Figure 7.10**: (a) Measured frequency response transfer function of the wireless telemetry pulse delivery system in Fig. 7.9. Measured voltage waveforms: (a, Inset) 1 kHz sine wave input; (b) biphasic constant voltage stimulation; and (c) biphasic constant current stimulation.

degenerated rat retina tissue.

#### 7.6.1 Methods

#### Retina preparation

We isolated intact neural sensory retinal explants from P23H degenerated rats. The rats were summarily euthanized by carbon dioxide inhalation. After the enucleation of the eye, the retina was cut into a  $4 \times 4$  mm piece and maintained in Ames (Sigma-Aldrich Co. LLC, MO, USA) saline solution at 30°C. As depicted in figure 7.11 (a), the retina segment in Ames solution was transferred onto a multichannel microelectrode array (MEA), connected to a multichannel data acquisition

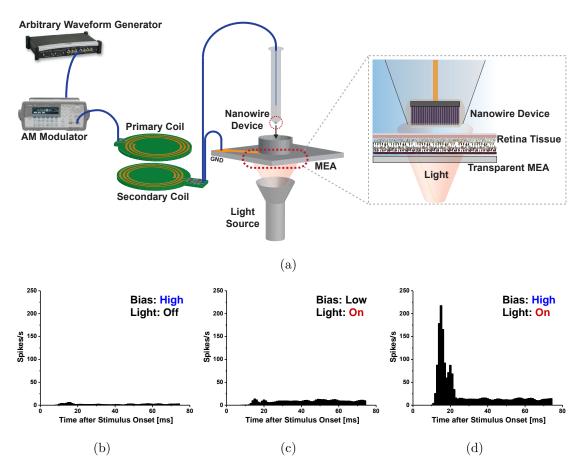


Figure 7.11: (a) Test setup for ex vivo demonstration of the entire system including the NW-based electrode array (figure 7.4) and the wireless telemetry pulse delivery system (figure 7.9). Post-stimulus time histograms (PSTHs) of RGC neural spike activity from rat retina tissue interfacing with the MEA neural recording system showing stimulus responses under three conditions: (b) stimulation with the high bias but with no light; (c) stimulation with the low bias but the light on; and (d) stimulation with both the high bias and the light on. The bin size in the histograms is 1 ms.

system (Multichannel Systems, Germany). The retina tissue was placed with the bipolar cells facing the NW device side to enable subretinal stimulation and with the ganglion cells facing the MEA to enable spike recording. An experimental 200  $\mu$ m  $\times$  200  $\mu$ m photodiode-type NW device (section 7.3) was lowered via a computer-operated micromanipulator to contact the subretinal surface. Contact was verified visually with an assistance of an inverted microscope.

#### Test setup

We generated the biphasic stimulation waveforms with an arbitrary waveform generator (Arbstudio 1104, Teledyne LeCroy, NY, USA), the output of which was connected to the amplitude modulation (AM) input of a signal generator (33220A, Keysight Technologies Inc., CA, USA) to produce an amplitude-modulated waveform with 6.78 MHz carrier frequency in the industrial, scientific and medical (ISM) radio bands. On the receiver side of the wireless telemetry pulse delivery system, the demodulated biphasic pulse at the output ( $V_{pout}$  in figure 7.9) was fed to the NW device through a copper wire. For proper encapsulation in the saline solution, the wire was soldered directly onto the back of the NW device and insulated with epoxy. A second wire connection (GND) established the MEA ground return as shown.

We used two scaled bias levels ("high" and "low") of identically shaped biphasic pulses, each with 5 ms anode phase followed by a 1 ms gap, and a 15 ms cathode phase. For each, the amplitude during the cathode phase was one third the amplitude during the anode phase. The bias levels were set on the external waveform generator to maintain the peak voltage  $V_{pout}$  across the NW device during the anode phase well within the water window for iridium oxide: at 0.5 V for the "high" bias setting, and at 0.07 V for the "low" bias setting. The high bias condition produced 2.67  $\mu$ A dark current during the anode phase, and the low bias condition 0.333  $\mu$ A. Hence the total charge delivery across the dark, single-electrode 2,500-NW device per phase of the high bias condition was 13.3 nC/phase, below the threshold for RGC spiking.

The NW device in contact with the retina was illuminated from below with an 850 nm infrared LED for a light intensity of 7.53  $\mu$ W/mm<sup>2</sup> in 5 ms pulses, under dark ambient conditions. Neural spikes were recorded from the MEA for three minutes in each of three conditions: i) stimulation with the high bias but with the light off; ii) stimulation with the low bias with the light on; and iii) stimulation with both the high bias and the light on. To provide control and consistent timing for PSTH collection under each of the three conditions, the onset for pulsed light stimulation was made to coincide with the anodic phase onset of electrical stimu-

lation. RGC spike activity was monitored by the MEA recording system for each stimulus, with valid data starting 8 ms after each stimulus onset. Offline spike sorting software (Plexon Inc, Dallas, TX) was used to process the neural spike data. A threshold of 4 times the standard deviation of the background noise was set to identify spike activity.

#### 7.6.2 Results and Discussion

Figures 7.11 (b), (c) and (d) show post-stimulus time histograms (PSTHs) of RGC neural spike responses recorded from one of the P23H degenerated rat retinas. By synchronizing the onset of pulsed bias and light stimulation it was possible to observe relative differences in PSTHs under two control conditions in which either one of the high bias or light on conditions was muted. As shown in figure 7.11 (d), a significant increase in neural response above baseline was observed 10-20 ms after the stimulus onset under the combined conditions of the high bias and the light on. As shown in figure 7.11 (c), pulsed light stimulation by itself, at low bias, did not elicit a neural response discernable from baseline. Similarly, under light off conditions no discernible difference from baseline was observed even under the high bias condition (figure 7.11 (b)).

These results suggest that the combination of optical addressing and electrical biasing for the vertical NW array provides sufficient optoelectronic gain for effective retinal stimulation at substantially lower intensity light illumination than for unbiased operation as in passive microphotodiode arrays. Although  $7\times$  brighter than typical irradiance on the human retina in sunlit outdoor conditions, the  $7.53~\mu\text{W/mm}^2$  illumination level in the experiments is a factor  $50\times$  dimmer than the 0.4 to  $6.9~\text{mW/mm}^2$  illumination for the laser-projected illumination levels for passive flat photovoltaic devices [243, 246, 251].

For a fair comparison of performance, responsivity of the devices should also be considered. The photodiode-type (PN-type) NW device used in the *ex vivo* experiments measures a visible to near-infrared (600-800 nm) responsivity of 0.70 A/W at 0.5 V bias, a three-fold improvement over the 0.24 A/W responsivity at zero bias. Recent refinements in the PN-type NW device shown in figure 7.12 (a)

have yielded more than two-fold further improvement, achieving unpulsed 850-nm IR responsivities of 1.73 A/W at 0.5 V bias and 2.12 A/W at 1.5 V bias as shown in figure 7.12 (b) through (d). Over conventional passive (unbiased) MPDAs with typical 0.40 A/W IR responsivities [408], this constitutes a five-fold improvement in responsivity measured in saline rather than dry environment, and with unpulsed rather than pulsed light.

In addition to the five-fold improvement in responsivity, the pulsed voltage biasing supports further control to increase the total stimulation current. As shown in figure 7.12 (c) and (d), the effect of increasing voltage bias amplitude is primarily an increase in base current, and to lesser extent an increase in responsivity. External electrical control over base current can thus be harnessed to accommodate varying illumination and stimulation threshold levels.

We expect additional optoelectronic gain from current amplification in the NPN-type NW device (Sec. 7.3) to substantially boost spectral responsivity for effective retinal stimulation at high spatial resolution, and possibly without external optical amplification at medium resolution. Such direct optical addressing by the visual scene requires the prosthesis to operate not only at low intensity thresholds, but also with unpulsed light. The experiments using the 1,512-electrode NW device in figure 7.12 have verified combined optical addressing and electrical biasing under continuous rather than pulsed light illumination.

The spatial resolution of stimulation is limited by two main considerations. First, the responsivity and maximum safe intensity levels set a lower limit on the electrode pitch of the array to reach supra-threshold stimulation. Second, more importantly, crosstalk due to volume conduction in tissue limits the effectiveness of stimulation for an electrode pitch substantially smaller than the axial distance of the target cells from the array [418]. The effect of crosstalk in tissue for the fabricated 1,512-electrode array with 50  $\mu$ m pitch of figure 7.12 (a) is illustrated in figure 7.13, indicating focal electric field strength at physiologically relevant axial distances for subretinal stimulation.

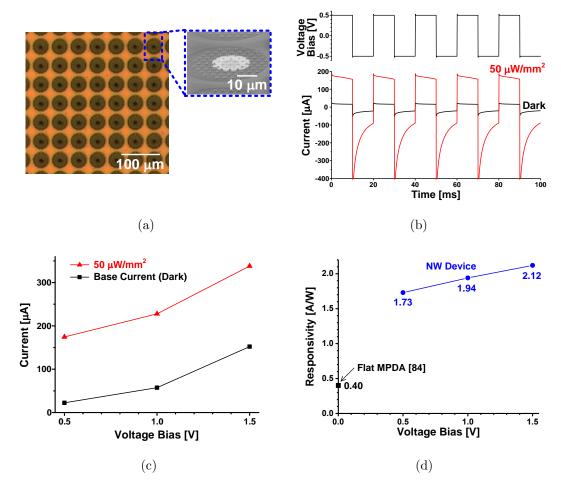


Figure 7.12: (a) Spatially resolved 1,512-electrode NW array device. (b) Measured pulsed voltage bias response of the NW array in saline solution under constant (unpulsed) intensity 850-nm IR illumination conditions: dark, and 50  $\mu$ W/mm<sup>2</sup>. (c) Measured current amplitude as a function of pulsed voltage bias amplitude, showing base current at dark illumination, and total current under illumination. (d) Measured responsivity of the NW array device for different pulsed voltage bias levels in comparison with a flat unbiased MPDA [408].

# 7.7 Conclusion

We presented a new retinal prosthesis architecture that combines spatial optical addressing and pulsed electrical biasing for scalable high-resolution retinal stimulation by a photosensitive electrode array activated over a single inductive telemetry link. The use of a vertical silicon NW array supports electrode densities approaching the dimensions of retinal neural circuits, and in conjunction with the

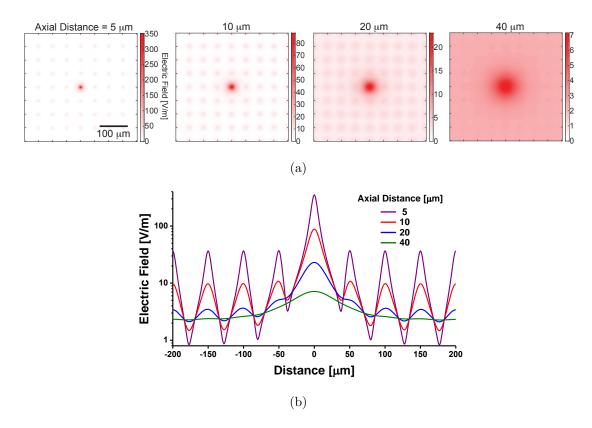


Figure 7.13: Simulated electric field in uniform tissue with  $2 \Omega^{-1} \text{m}^{-1}$  conductivity above the NW-based electrode array of figure 7.12 (a) at axial distances ranging from 5 to 40  $\mu$ m. Electrode currents injected into tissue are derived from the measurements in figure 7.12 (b) at 0.5 V pulsed voltage bias, and at 50  $\mu$ W/mm<sup>2</sup> unpulsed IR intensity over the center electrode, with dark surround over the other electrodes.

pulsed electrical biasing provides sufficient optoelectronic gain for neural stimulation at relatively low light intensity compared to passive flat microphotodiode arrays. Stimulation parameters such as frequency, widths, heights and gap time of typical biphasic waveforms can be entirely controlled on the external side through combined power and data telemetry over the inductive link, while charge-balancing is achieved by biphasic pulsed voltage biasing through a single AC-coupling capacitor in series with the array. Proof-of-concept demonstration of the entire system in ex vivo rat retina tissue validated RGC neural responses under combined pulsed bias and light conditions, with suppressed response when either the bias or light condition was muted. We also validated in a 1,512-electrode NW array a five-

fold improvement in responsivity over conventional flat microphotodiode arrays, with additional gains in stimulation currents contributed by the pulsed electrical biasing.

As such, this work presents an important step towards engineering realization and eventual clinical use of optically addressable retinal prostheses. Continued advances towards realization of a clinically viable high-resolution retinal prosthesis call for device-level refinements in the NW array structures for increased opto-electronic gain and greater electrode density; hermetic coating of the NW active elements for chronic implanted operation; and ex vivo and in vivo validation of optical resolution and visual acuity consistent with electrode densities.

Chapter Seven is largely a combination of material in the following two venues: Sohmyung Ha, Massoud L. Khraiche, Abraham Akinin, Yi Jing, Yu-Hwa Lo, William R. Freeman, Gabriel A. Silva and Gert Cauwenberghs, "Towards High-resolution Retinal Prostheses with Direct Optical Addressing and Inductive Telemetry," *Journal of Neural Engineering*, 2016 (submitted after revision). Sohmyung Ha, Massoud L. Khraiche, Gabriel A. Silva and Gert Cauwenberghs, Direct Inductive Stimulation for Energy-Efficient Wireless Neural Interfaces, *Proceedings of the 34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, San Diego CA, August 28-September 1, 2012. The author is the primary author and investigator of this work.

# Chapter 8

# Conclusion and Future Work

# 8.1 Silicon Integrated Neural Interfaces

### 8.1.1 Summary and Significance of Results

Wireless neural-interfacing microsystems based on CMOS technology have been widely used for brain monitoring, diagnostic, therapeutic, and prosthetic applications, such as deep-brain stimulation, epileptic seizure detection and intervention, and brain-computer interface (BCI). However, even recent neural interfacing devices still rely on bulky external components such as antennas, capacitors, or inductors for system functionality and/or efficiency improvements, limiting their utility when ultra-miniaturized integration is required. To address this challenge, we developed and presented the first prototype of wireless neural-interface-on-chip that incorporates all functionality on a single chip: antenna, adiabatic stimulator, analog front-end, ADC, and wireless power and data telemetry, requiring no external wires, substrates, batteries, or any other external components. This system is one of the smallest neural-interfacing microsystems with a volume of  $3\times3\times0.3$ mm<sup>3</sup>, small enough to be placed amongst the folds and curves of the cortical surface, and to be implanted through minimally invasive surgical procedures inserted through small skull fissures. We validated each component of the system on the electrical bench-top and have proceeded with first in vivo tests [133].

#### 8.1.2 Future Research Plan

I plan to pursue three main research directions in this area. First, I plan to further refine the development of neural-interface-on-chip platforms targeting neurological applications in close collaboration with clinical and neuroscience partners. In doing so I will continue to address challenges in aspects of EMI interference, biocompatible encapsulation, interrogator, multi-user communication, etc. This work will truly enable a chronic implanted BCI system that makes enormous impact on neuroscience research and clinical treatments for numerous patients with neurological disorders and paralyzed limbs.

Second, I plan to pursue fundamental limits of performance in core sub-components for wireless power and data telemetry, stimulation, recording, on-chip signal processing, and sensor networking. For example, the power and data telemetry technology presented in Chapter 4 breaks through the conventional performance barrier of single-link inductive telemetry, achieving the highest data rate normalized to RF carrier frequency. This simultaneous power and data transfer scheme was validated to achieve data rates up to 10 Mbps, greater than half the 13.56 MHz carrier frequency, with simultaneous delivery of more than 10 mW power over the same inductive link [139]. This technology is applicable not only to neural recording systems, but also various RFID-based sensor systems and near-field communication between hand-held devices. Likewise, I anticipate further innovation on sub-components in various developments of ADCs, stimulators, analog front-ends, PLL and RF transmitters will greatly impact further advances of biomedical instrumentation.

The third research direction I plan to pursue here is non-amperometric in vitro neural/cellular interfacing as a more advantageous tool for investigating cellular-level functions and interactions than in vivo settings. By applying the technique we developed for non-amperometric (capacitive) recording and stimulation, I plan to develop a non-contact MEA-based neural interface platform that minimally interferes with the targeted neurons and cells, tailoring to new emerging research opportunities.

# 8.2 Retinal Prostheses

#### 8.2.1 Summary and Significance of Results

Despite considerable advances in retinal prostheses over the last two decades, the resolution of restored vision has remained severely limited, well below the 20/200-acuity threshold of blindness. To address this challenge, we have worked on a scalable retinal prosthesis, in which each stimulation electrode based on ultrahigh photosensitive silicon nanowires is directly activated by incident light. For ex vivo validation with rat retina tissues, we integrated a complete bench-top system comprising inductive telemetry link, stimulation pulse generator, charge-balancing scheme, and nanowire-based electrode array [134]. Currently, an implantable version of the device is under *in vivo* testing subretinally in rabbit eye in collaboration with Nanovision Biosciences, Inc., a UC San Diego spin-off company for retinal prosthesis development. Hence this work is progressing to practical development and, ultimately, clinical trials of the envisaged nano-engineered retinal prosthesis, leading a first viable path towards restoring high-acuity vision in the severely visually impaired.

#### 8.2.2 Future Research Plan

I plan to develop an innovative retinal prosthesis design that includes in situ recording of retinal activity in conjunction with high-density stimulation. This work will require thinning of a custom designed silicon-on-insulator (SOI) chip down to 1  $\mu$ m for flexibility, and encapsulation with a biocompatible substrate such as a liquid crystal polymer. I anticipate this work to lead to the first CMOS-based flexible retinal prosthesis with in situ recording. This retinal prosthesis will not only enhance the resolution by characterizing and resolving different types of retinal ganglion cells, but also provide an unprecedented in vivo tool to revolutionize research on the retina activity mapping and development of retinal prostheses. Thankfully, this task leverages my previous work on retinal prostheses, an event-driven CMOS imager, on-chip integration of antenna and electrodes, and neural signal recording and stimulation.

# 8.3 Wearable Health Monitoring

### 8.3.1 Summary and Significance of Results

Unobtrusive wearable health monitoring devices promise to make more widespread and more prompt impact on medical diagnosis and quality of life than implantable devices owing to their ease, comfort, and accessibility of use. For autonomous operation, these sensors are required to harvest energy directly from the environment, the interrogator, or the signal of interest. The technologies and design techniques I developed and acquired throughout my Ph.D. studies can be directly applied in the wearable setting as well [136]. For example, the wireless power and data telemetry systems that I developed for implantable use [138,139] can be immediately adopted into RF-powering wearable sensors. In addition, a non-contact sensing technology with a high front-end gain that I recently developed, and a fully asynchronous vision sensor [304] will be essential elements for various sensor applications.

#### 8.3.2 Future Research Plan

I plan to attack three main research directions in this research theme. First, I plan to investigate flexible-substrate-based sensors for ambulatory health monitoring, entertainment and sport applications. In doing so I will extend my work on power and data telemetry and recording ICs for flexible electrode arrays [140] towards self-powered sensors of a wearable form factor integrated in shoes, gloves or watches.

The second direction I plan to pursue in the area of wearable sensors is to develop energy harvesting and ultra-low-power circuit components such as analog front-end, ADC, temperature sensor, capacitance sensor, and RF transmitter. These are for extreme applications in the Internet-of-Things paradigm with self-power-havesting from solar, thermal, piezoelectric transducers. Typically, the scavenged power level is very low, less than  $\mu$ W, so conventional electronics are difficult to operate. This will require to utilize two techniques: event-driven computing and ultra-low-power circuit design technique, which I have acquired while

working with my advisor Prof. Cauwenberghs as well as Prof. Mercier, a close collaborator and thesis committee member.

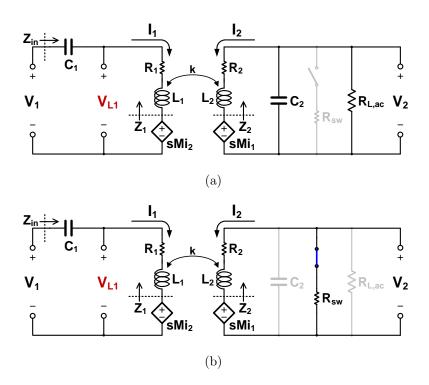
The third research direction will entail development of smartphone-connected base stations to network with the sensors, utilizing myriad resources related to smartphones, and provide user-friendly interface. This will include development of a smartphone-connected communication module using magnetic body-channel communication, such as recently proposed and demonstrated here at UC San Diego. This mobile base station will integrate all the wearable and implantable sensors into a complete integrated system applicable in everyday life and clinical settings.

## 8.4 Conclusion

Each investigation detailed above will advance me towards a common goal, which is to improve human health through technological innovation. The everything-on-chip integrated framework will provide a unique flagship tool for my future research group, and will offer an integration platform to host various sensors and actuators in ubiquitous healthcare and fitness monitoring settings. Some of these along with more exploratory endeavors are likely to become full-fledged research projects in the intermediate future, further expanding the interface between neuroscience, biomedical and electrical engineering. In addition, I hope these technology innovations will foster new start-up ventures, bringing the technologies to the real-life applications and vibrancy to the industry. I believe that the pursuit of these research subjects will enable me to contribute to the well-diversified and dynamic research environment in the future.

# Appendix A

# A.1 Derivation of COOK Receiver Modulation Index



**Figure A.1**: Analytical circuit models when the data switch is (a) open and (b) shorted.

In this section we derive the receiver modulation index RMI for COOK modulation. As explained in Sec. 4.2.2 and expressed in Eq. (4.1), RMI quantifies the profile of amplitude change in the primary coil voltage  $V_{L1}$  during the synchro-

nized COOK shorting for data transmission. Since there are two distinctive causes for the amplitude change, RMI can be expressed as:

$$RMI = RMI_Z + RMI_{exp} \tag{A.1}$$

where  $RMI_Z$  represents amplitude change due to reflected impedance change by single-cycle shorting, and  $RMI_{exp}$  the change in  $V_{L1}$  incurred by the exponentially decreasing current through the secondary inductor during the shorting.

The increased portion of the amplitude due to change of the reflected impedance  $Z_{rfl}$  in RMI<sub>Z</sub> is reflected from the secondary side on to the primary side. The input impedance  $Z_{in}$  from the voltage source is expressed as:

$$Z_{in} = Z_1 + Z_{rfl} = Z_1 - \frac{s^2 M^2}{Z_2(s)} \tag{A.2}$$

At the resonance frequency, and while the switch is open as shown in Fig. A.1 (a),  $Z_{in}$  can be expressed as:

$$Z_{in}^{o} = \frac{1}{j\omega C_{1}} + j\omega L_{1} + R_{1} + Z_{rfl}^{o}$$

$$\simeq R_{1} \left( 1 + k^{2}Q_{1}R_{1}Q_{2L} \right) \tag{A.3}$$

where  $Q_{2L} = \omega L_2 / (R_2 + \frac{L_2}{C_2 R_{L,ac}})$ .

Conversely,  $Z_{rfl}$  and  $Z_{in}$  during the short as shown in Fig. A.1 (b) can be expressed as:

$$Z_{rfl}^{s} = \frac{k^{2}\omega^{2}L_{1}L_{2}(R_{2} + R_{sw})}{(R_{2} + R_{sw})^{2} + (\omega L_{2})^{2}} + j\omega L_{1} \frac{k^{2}\omega^{2}L_{2}^{2}}{(R_{2} + R_{sw})^{2} + (\omega L_{2})^{2}}$$
(A.4)

$$Z_{in}^{s} = \frac{1}{j\omega C_{1}} + j\omega L_{1} \left( 1 - k^{2} \frac{Q_{2sw}^{2}}{Q_{2sw}^{2} + 1} \right) + R_{1} \left( 1 + k^{2} \frac{Q_{1}Q_{2sw}}{Q_{2sw}^{2} + 1} \right)$$
 (A.5)

where  $Q_{2sw} = \omega L_2 / (R_2 + R_{sw})$ .

Due to this impedance change from  $Z_{in}^o$  to  $Z_{in}^s$ , the voltage amplitude is increasing over the single cycle shorting as follows:

$$RMI_{Z} = \left(\frac{1 + Z_{in}^{o}}{1 + Z_{in}^{s}} - 1\right) \left(1 - e^{-T\frac{R_{1s}}{2L_{1s}}}\right)$$
$$= \left(\frac{Z_{in}^{o} - Z_{in}^{s}}{1 + Z_{in}^{s}}\right) \left(1 - e^{-\pi/Q_{1s}}\right)$$
(A.6)

where T is the resonance period, and where

$$Q_{1s} = \omega L_{1s}/R_{1s} = \frac{\omega L_1 \left(1 - k^2 \frac{Q_{2sw}^2}{Q_{2sw}^2 + 1}\right)}{R_1 \left(1 + k^2 \frac{Q_1 Q_{2sw}}{Q_{2sw}^2 + 1}\right)}.$$
 (A.7)

 $RMI_{exp}$  is induced by the current  $I_2$  flowing through  $L_2$ ,  $R_2$  and the switch  $(R_{sw})$  during the single-cycle shorting. At the start of the short, the current through the secondary inductor is at its maximum  $I_{2max}$ . During the short, the current decreases exponentially with time constant formed by  $L_2$ ,  $R_2$  and  $R_{sw}$  as follows:

$$I_2(t) = I_{2max}e^{-t\left(\frac{R_2 + R_{sw}}{L_2}\right)}$$
 (A.8)

This exponential decaying current is reflected to  $V_{L1}$  during the single cycle shorting as follows:

$$RMI_{exp} = sMI_2(T)/V_{L1}^o = -\frac{\eta M e^{-2\pi \left(\frac{1}{Q_2} + \frac{1}{Q_{2sw}}\right)}}{L_1 + \eta M}$$
(A.9)

with current peak conversion ratio  $\eta = I_{2max} / I_{1max} = k \sqrt{R_1 Q_1 Q_{2L} / (R_2 + \frac{L_2}{C_2 R_{L,ac}})}$  and link mutual inductance  $M = k \sqrt{L_1 L_2}$ .

## A.2 Derivation of the Optoelectronic Gain in Capacitively Coupled Photodiode-type NW device

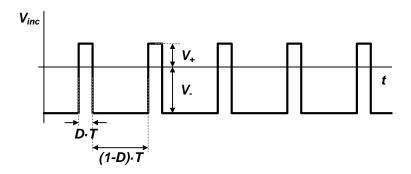
The following analysis establishes that a series AC-coupling capacitor balances anode and cathode currents to zero the net average charge transfer across the photodiode-type NW device of figure 7.4 by shifting the DC offset. The current I through the photodiode device as a function of voltage V across the device under illumination is modeled as the current produced by a standard diode without illumination, in parallel with photocurrent  $I_{photo}$  induced by the illumination:

$$I = I_0 \left( e^{V/nV_T} - 1 \right) - I_{photo} \tag{A.10}$$

where  $I_0$  is the diode saturation current, n the ideality factor typically between 1 and 2, and  $V_T$  the thermal voltage, which is 26.7 mV at body temperature

(36.5°C). The photocurrent  $I_{photo}$  results from photogenerated electron-hole pairs, and is typically proportional to the incident light power  $P_{in}$  as:

$$I_{photo} \propto P_{in}.$$
 (A.11)



**Figure A.2**: Charge-balanced voltage biasing of a capacitively coupled photodiode array.

Consider that the substrate side of the NW device is connected to the AC-coupling capacitor  $C_{AC}$  in series, and the wireless telemetry pulse delivery system drives the  $C_{AC}$  capacitor with a periodic rectangular voltage pulse  $V_{in}$  while grounding the other node of the device (GND). It is assumed that  $C_{AC}$  is sufficiently large so that the high-pass cutoff frequency formed with the resistive load of the device is substantially lower than the frequency range of  $V_{in}$ . As a result, the voltage across the device  $V_{inc}$  at convergence is mostly DC-shifted from  $V_{in}$ . Figure A.2 illustrates  $V_{inc}$  and its parameters: duty cycle ratio D between 0 and 1, period T, and positive and negative phase amplitudes  $V_+$  and  $V_-$ .

The device currents during the positive  $(V=V_+)$  and negative  $(V=-V_-)$  phase are expressed as:

$$I_{+} = I_{0} \left( e^{V_{+}/nV_{T}} - 1 \right) - I_{photo}$$
 (A.12)

$$I_{-} = I_0 \left( e^{-V_{-}/nV_T} - 1 \right) - I_{photo}.$$
 (A.13)

The total charge delivered over each cycle is zero, and thus:

$$I_{+} D T + I_{-} (1 - D) T = 0$$

$$\left(I_{0} \left(e^{V_{+}/nV_{T}} - 1\right) - I_{photo}\right) D T$$

$$+ \left(I_{0} \left(e^{-V_{-}/nV_{T}} - 1\right) - I_{photo}\right) (1 - D) T = 0. \tag{A.14}$$

With  $V_{inc,pp} = V_+ + V_-$  the peak-to-peak amplitude of  $V_{inc}$ , (A.14) simplifies to:

$$I_0 e^{V_+/nV_T} \left( D + (1-D)e^{-V_{inc,pp}/nV_T} \right) = I_{photo} + I_0.$$
 (A.15)

This further simplifies to:

$$I_0 D e^{V_+/nV_T} \simeq I_{photo} + I_0$$
 (A.16)

since  $V_{inc,pp} \gg nV_T$ .

The current  $I_{+}$  can be rewritten with (A.16) as:

$$I_{+} = I_{0} \left( e^{V_{+}/nV_{T}} - 1 \right) - I_{photo}$$

$$= I_{0} \left( \frac{I_{photo} + I_{0}}{I_{0} D} - 1 \right) - I_{photo}$$

$$= \left( I_{photo} + I_{0} \right) \left( \frac{1}{D} - 1 \right). \tag{A.17}$$

Since  $I_{photo} \gg I_0$  under typical illumination conditions,  $I_+$  and  $I_-$  are approximated as:

$$I_{+} \simeq I_{photo} \left(\frac{1}{D} - 1\right)$$
 (A.18)

$$I_{-} \simeq -I_{photo}.$$
 (A.19)

As shown, the device currents  $I_+$  and  $I_-$  are determined by both the photocurrent  $I_{photo}$  and the duty cycle ratio D, not related to the diode characteristics of the device to first order. Moreover, (A.18) establishes a multiplicative gain factor  $G = (\frac{1}{D} - 1)$  in the anode current  $I_+$ . Since D typically is much smaller than 1, a gain factor G much larger than 1 can be achieved, providing additional optoelectronic gain over unbiased photovoltaic operation.

Appendix A is largely a reprint of material that appeared in Sohmyung Ha, Massoud L. Khraiche, Abraham Akinin, Yi Jing, Yu-Hwa Lo, William R. Freeman, Gabriel A. Silva and Gert Cauwenberghs, "Towards High-resolution Retinal Prostheses with Direct Optical Addressing and Inductive Telemetry," *Journal of Neural Engineering*, 2016 (submitted after revision). The author is the primary author and investigator of this work.

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