Title

A Dickson-Squared Hybrid Switched-Capacitor Converter for Direct 48 V to Point-of-Load Conversion

Authors

Zhu, Yicheng
Ge, Ting
Ye, Zichao
et al.

Publication Date

2022-03-24

DOI

10.1109/apec43599.2022.9773567

Proceedings of the 37th Applied Power Electronics Conference and Exposition (APEC 2022), Houston, TX, USA, March 20-24, 2022

A Dickson-Squared Hybrid Switched-Capacitor Converter for Direct 48 V to Point-of-Load Conversion

Y. Zhu
T. Ge
Z. Ye
R. C. N. Pilawa-Podgurski

A Dickson-Squared Hybrid Switched-Capacitor Converter for Direct 48 V to Point-of-Load Conversion

Yicheng Zhu, Ting Ge, Zichao Ye, and Robert C. N. Pilawa-Podgurski
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
Email: {yczhu, gting, yezichao, pilawa}@berkeley.edu

***Abstract*—More energy-efficient and power-dense solutions to 48 V to point-of-load (PoL) power conversion are required for modern and future data center power delivery. This paper proposes a Dickson-squared hybrid switched-capacitor (SC) converter for direct 48 V-to-PoL conversion with high efficiency and high power density. The proposed topology comprises a 9-to-1 SC stage that can be viewed as two 3-to-1 Dickson SC converters combined together and a nine-phase interleaved buck stage. The proposed topology can achieve complete soft-charging operation with a simple control, ensure naturally balanced interleaved inductor currents, enable reduced conversion burden on the buck stage, and eliminate the need for large bus capacitors with a switching bus architecture. A 48 V-to-PoL hardware prototype is built to verify the performance of the proposed converter, achieving 93.8% peak efficiency and 360 W/in^3 power density at 1.0 V output voltage.**

I. Introduction

Data-center electricity consumption has been forecasted to increase dramatically in the next decade [1], [2]. Modern computer processors and computation engines that typically operate at extreme low voltage (e.g., around 1.0 V) tend to consume higher current (e.g., hundreds of amperes) with the growth in computing power, which requires more energy-efficient and power-dense solutions to 48 V to point-of-load (PoL) power conversion.

Two challenges of 48 V-to-PoL power conversion are high conversion ratio and high load current. To address these challenges, two solutions are typically adopted: 1) transformer-based solution [3]–[6], and 2) hybrid switched-capacitor (SC) solution [7]–[16]. The former solution typically consists of a fixed-ratio LLC converter to carry the majority of the conversion burden and a buck stage for output voltage regulation, while the latter solution performs the step-down conversion with a single-stage [13]–[16] or two-stage [7]–[12] SC converter and regulates the output voltage with the augmenting inductors in the buck stage. On the one hand, compared to the transformer-based solution, the hybrid switched-capacitor (SC) solution can leverage the superior energy density of capacitors compared to inductors and transformers [17]. On the other hand, hybrid SC converters can eliminate the capacitor charge sharing loss in conventional pure SC converters and achieve complete soft-charging operation [18]. For hybrid SC solutions, since the efficiency and power density of a buck converter decreases with a higher conversion ratio, the overall performance can be improved if the SC stage can achieve a higher conversion ratio without much extra loss or many additional components [11].

This paper proposes a Dickson^2 hybrid SC converter that can achieve direct 48 V-to-PoL conversion with high efficiency and high power density. The proposed topology comprises a 9-to-1 SC stage and a nine-phase interleaved buck stage, in which the SC stage can be viewed as two 3-to-1 Dickson converters directly combined together without an intermediate DC bus. The proposed topology can achieve complete soft-charging operation with a simple control and ensures naturally balanced interleaved inductor currents. Compared with the existing 48 V-to-PoL hybrid SC converters, the proposed topology achieves the highest conversion ratio at the SC stage, thus reducing the conversion burden on the buck stage. Moreover, the proposed topology requires no large bus capacitors by using a switching bus architecture. A 48 V-to-PoL hardware prototype is built to verify the performance of the proposed converter. At 1.0 V output voltage, the prototype achieves 93.8% peak efficiency, 88.4% full-load efficiency, and 360 W/in^3 power density (by box volume).

II. Proposed Topology and Operating Principles

Fig. 1 shows the schematic drawing of the proposed Dickson^2-PoL converter, with the key waveforms and control signals illustrated in Fig. 2. As illustrated in Fig. 1(a), the proposed topology consists of two stages. The first stage is a 3-to-1 Dickson SC topology with three separated output terminals. The second stage is composed of three modules with the same circuit structure and cyclic control signals as shown in Fig. 1(b). Inside each module is a three-phase series-capacitor buck converter, which can also be viewed as a 3-to-1 Dickson converter with the top switch moving to the bottom and the three output branches replaced by three inductors. Since this SC topology can be viewed as two Dickson converters merged together with redundant components removed, it is given the name *Dickson^2*.

The proposed Dickson^2-PoL converter has the following features.

A. Complete Soft-Charging Operation With Simple Control

As explained in [19], to achieve complete soft-charging operation in resonant Dickson SC converters, a more complex control technique such as the split-phase control [20] has to be employed. However, despite the simple three-phase control of

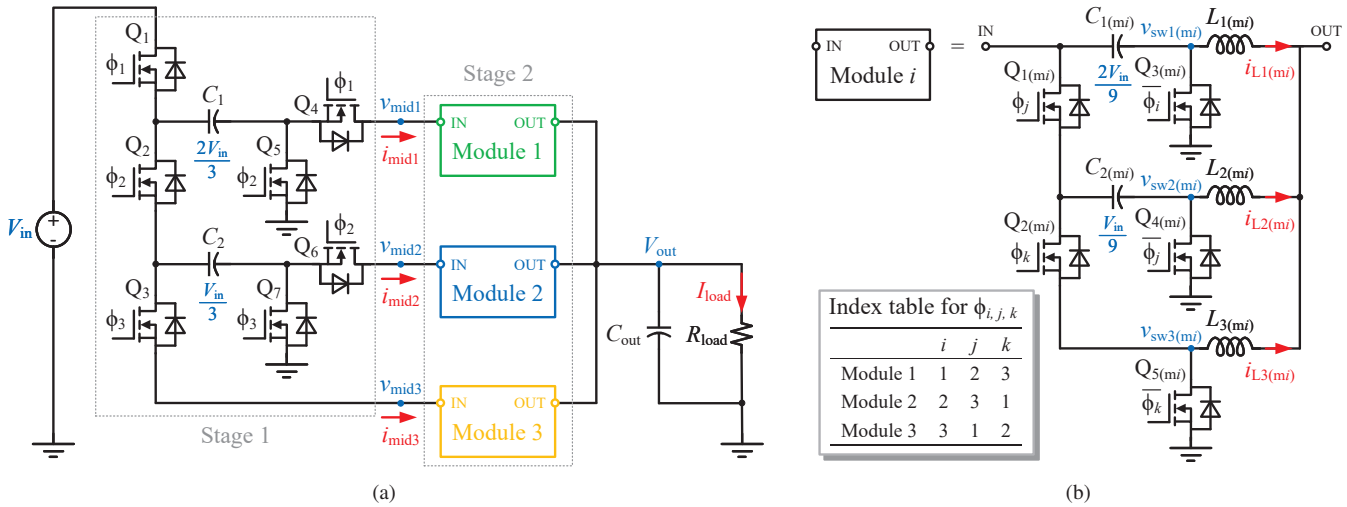

Fig. 1: Schematic drawing of the proposed Dickson^2-PoL converter. (a) Overall architecture. (b) Structure of Module i in Stage 2. The components labeled with the subscript (mi) are in Module i. The values of the label indexes (i, j and k) for circuit components and control signals (ϕ_i, ϕ_j and ϕ_k) in each module are listed in the index table.

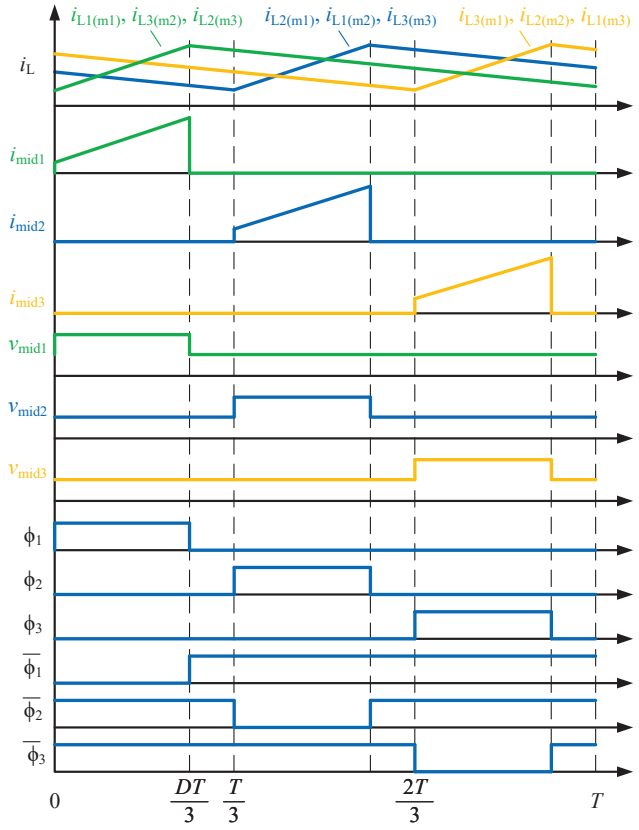

Fig. 2: Key waveforms and control signals of the proposed Dickson^2-PoL converter.

the proposed topology shown in Fig. 2, the capacitor charge sharing loss can be completely eliminated with the three modules in the second stage inserted into the 3-to-1 Dickson SC topology in the first stage at the three output terminals. This can help improve efficiency without compromising on control complexity.

TABLE I: Comparison of the conversion ratio division over the SC and buck stages among different 48 V-to-PoL hybrid SC works (assuming 48 V to 1.0 V conversion)

Topology	SC stage ratio	buck stage ratio
Crossed-coupled QSD buck [13]	4:1	12:1
CaSP-PoL [7]	6:1	8:1
LEGO-PoL [12]	6:1	8:1
VIB-PoL [8]	8:1	6:1
MLB-PoL [10], [11]	8:1	6:1
This work	9:1	5.33:1

B. Naturally Balanced Interleaved Inductor Currents

With the cyclic control shown in Figs. 1(b) and 2, the operation of the SC and buck stages is merged seamlessly so that the three-phase inductor currents in each model are interleaved with each other, which can reduce the net output current ripple. Moreover, the interleaved inductor currents are naturally balanced due to an inherent negative feedback mechanism between the inductor currents and flying capacitor voltages as explained in [7]. In addition, the bottom switches in the buck stage $Q_{3-5(\mathrm{m1})-(\mathrm{m3})}$ can operate with zero-voltage switching (ZVS).

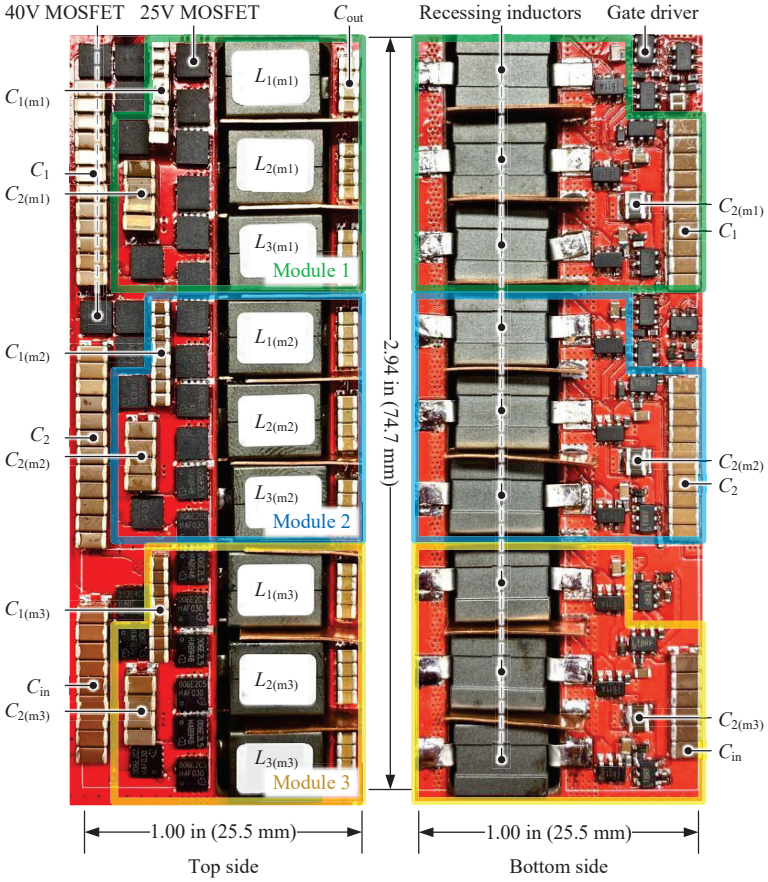

Fig. 3: Photograph of the hardware prototype. Dimensions: $2.94\times1.00\times 0.25$ in ($74.7\times25.5\times6.45$ mm). (6 layers, 4 oz copper on outer layers, 2 oz copper on inner layers)

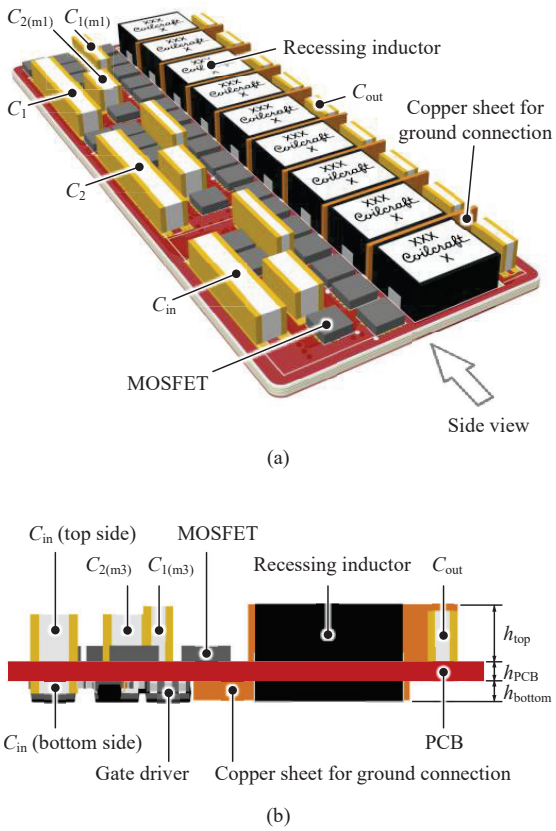

Fig. 4: 3D view of the hardware prototype. (a) Assembly drawing. (b) Side view. ($h_{\text{top}} = 3.75$ mm, $h_{\text{PCB}} = 1.6$ mm, $h_{\text{bottom}} = 1.1$ mm)

C. Reduced Conversion Burden on the Buck Stage

As listed in Table I, compared to the existing 48 V-to-PoL hybrid SC works, the proposed topology achieves the highest conversion ratio at the SC stage, resulting in less conversion burden on the following buck stage. Since the efficiency and power density of the buck stage will increase with a lower conversion ratio, the overall performance can be improved with the SC stage carrying more conversion burden without much extra loss or many additional components.

D. Switching Bus Architecture Without Large Bus Capacitors

In most two-stage conversion architectures, an intermediate DC bus is needed to connect the two stages, which requires large bus capacitors to stabilize the DC bus voltage that hinders converter miniaturization. By contrast, in the proposed Dickson^2-PoL topology, the two Dickson stages are merged directly and seamlessly without an intermediate DC bus. As illustrated in Fig. 2, the middle points between the two stages see switching voltages $v_{\text{mid1}-\text{mid3}}$. This *switching bus architecture* not only eliminates the need for large bus capacitors but also enables further topology simplification by removing the redundant switches.

The output voltage of the proposed converter can be derived by multiplying the conversion ratios of the fixed-ratio SC stage and the regulated buck stage as

$$V_{\text{out}} = \text{Ratio}_{\text{SC}} \times \text{Ratio}_{\text{buck}} = \frac{V_{\text{in}}}{9} \times \frac{D}{3} = \frac{D}{27} V_{\text{in}} \qquad (1)$$

where D is the duty ratio with respect to $\frac{T}{3}$, as illustrated in Fig. 2. Thus, V_{out} can be regulated by adjusting D.

III. Hardware Implementation

A 48 V-to-PoL hardware prototype is designed and tested up to 270 A load current to verify the functionality and performance of the proposed topology. The key parameters of the hardware prototype are listed in Table III. Fig. 3 shows the annotated photograph of the hardware prototype, with the 3D view of its assembly drawing and the side view presented in Fig. 4. As shown in Figs. 3 and 4, the modular structure of the proposed topology eases the PCB layout design. The inductors are recessed in the board cut-out to reduce the overall height. As can be seen in Fig. 4, S-shape copper sheets are placed between the inductors for ground connection with tight packaging.

TABLE II: Component list of the hardware prototype

Component	Part number	Parameters
MOSFET $Q_{1,4,6}$	Infineon IQE006NE2LM5	25 V, 0.65 mΩ
MOSFET $Q_{2,3}$	Infineon IQE013N04LM6CG	40 V, 1.35 mΩ
MOSFET $Q_{5,7}$, $Q_{1,2(\mathrm{m1})-(\mathrm{m3})}$	Infineon IQE006NE2LM5CG	25 V, 0.65 mΩ
MOSFET $Q_{3-5(\mathrm{m1})-(\mathrm{m3})}$	Infineon IQE006NE2LM5CG, IQE006NE2LM5	25 V, 0.65 mΩ (in parallel)
Flying capacitor C_1	TDK CGA5L3X5R1H106M160AB (top side)	X5R, 50 V, 10 μF*×24 (in parallel)
	TDK C3216X5R1H475K085AB (bottom side)	X5R, 50 V, 4.7 μF*×12 (in parallel)
Flying capacitor C_2	TDK C3216X5R1E476M160AC (top side)	X5R, 25 V, 47 μF*×24 (in parallel)
	TDK C3216X5R1E106M085AC (bottom side)	X5R, 25 V, 10 μF*×12 (in parallel)
Flying capacitor $C_{1(\mathrm{m1})-(\mathrm{m3})}$	TDK C2012X5R1C226M125AC	X5R, 16 V, 22 μF*×24 (in parallel)
Flying capacitor $C_{2(\mathrm{m1})-(\mathrm{m3})}$	TDK C3216X5R1A686M160AC (top side)	X5R, 10 V, 22 μF*×8 (in parallel)
	TDK C2012X5R1A226M085AC (bottom side)	X5R, 25 V, 10 μF*×2 (in parallel)
Inductors $L_{1(\mathrm{m1})}$-$L_{3(\mathrm{m3})}$	Coilcraft SLR1065-301KEC	300 nH, 0.48 mΩ, 32 A
Input capacitor C_{in}	TDK CGA5L3X7S2A335M160AB (top side)	X7S, 100 V, 3.3 μF*×18 (in parallel)
	Kyocera AVX 12061C225KAT2A (bottom side)	X7R, 100 V, 2.2 μF*×9 (in parallel)
Output capacitor C_{out}	Murata GRM219R60J476ME44D	X5R, 6.3 V, 47 μF*×108 (in parallel)
Gate driver	Analog Devices LTC4440-5	High-side gate driver, 80 V
	Texas Instruments UCC27511ADBVT	Low-side gate driver
Bootstrap diode	Infineon BAT6402VH6327XTSA1	Schottky diode, 40 V

* The capacitance listed in this table is the nominal value before DC derating.

TABLE III: Key parameters of the hardware prototype

Parameter	Value
Input voltage	48 V
Tested output voltage	1.0-1.5 V
Maximum output current	270 A
Switching frequency	280 kHz
Gate drive voltage	6.5 V
Prototype box volume*	0.750 in^3
Power component volume+	0.381 in^3
Current density	360 A/in^3

* The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry.

+ The power component volume is calculated as the total volume of all switching devices, capacitors and inductors in the power stage, excluding the gate drive circuitry.

Table II tabulates the components used in the hardware prototype. Two paralleled MOSFETs are used for the bottom switches in the buck stage $Q_{3-5(\mathrm{m1})-(\mathrm{m3})}$ to reduce the ON-resistance and achieve higher heavy-load efficiency. Low-profile capacitors (thickness: 0.85 mm) are selected for the bottom side so that the overall component height on the bottom side (i.e., h_{bottom} in Fig. 4(b)) will not be increased. The shielded power inductor Coilcraft SLR1065-301KEC with low DCR is chosen for higher heavy-load efficiency. The cascaded bootstrap and gate-driven charge pump circuits introduced in [21] are adopted to power the floating switches.

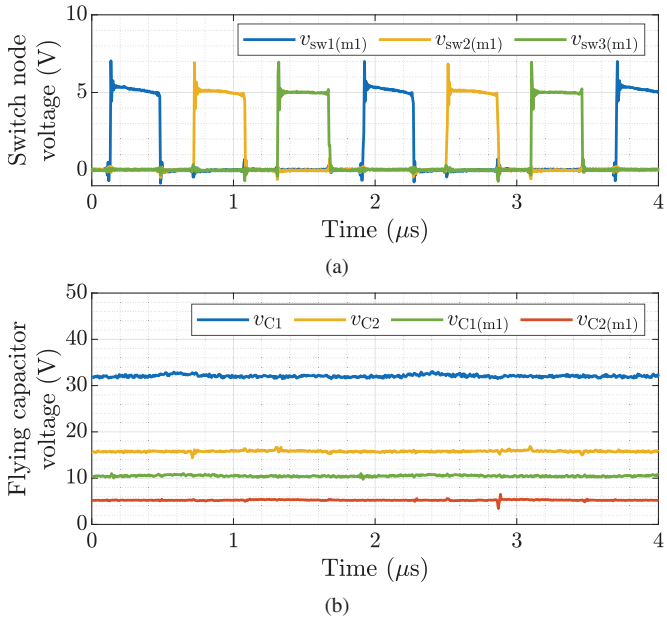

Fig. 5: Measured waveforms at $V_{\mathrm{out}} = 1.0$ V, $I_{\mathrm{out}} = 200$ A. (a) Switch node voltages in Module 1. (b) Flying capacitor voltages.

IV. Experimental Results and Performance Comparison

Fig. 5 shows the measured waveforms of the switch node voltages in Module 1 (i.e., $v_{\mathrm{sw1-3(m1)}}$ in Fig. 1(b)) and the flying capacitor voltages, which verifies the functionality of

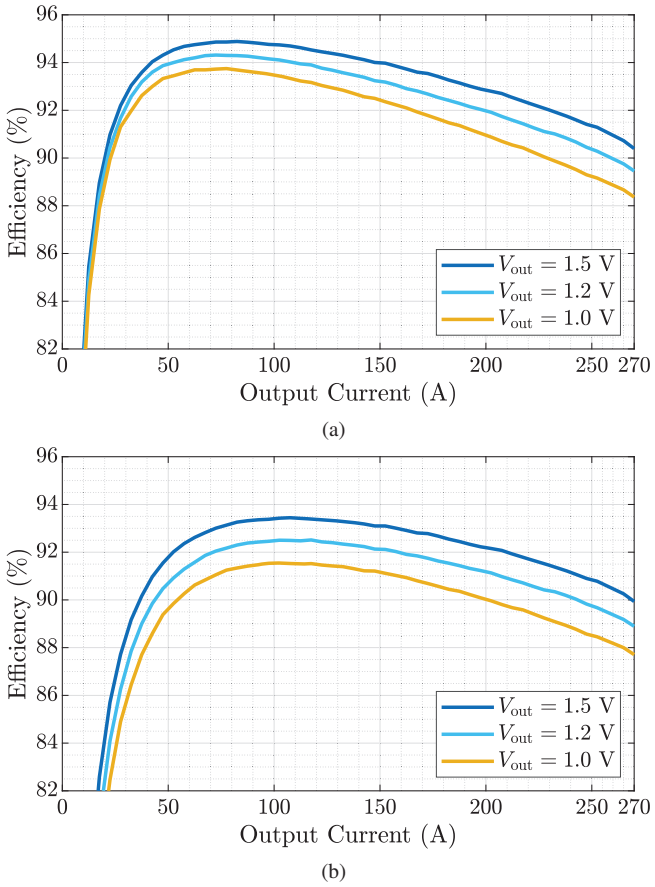

Fig. 6: Measured efficiency of the hardware prototype at various output voltages. (a) Power stage efficiency. (b) Overall system efficiency (including gate drive loss).

TABLE IV: Measured efficiency and power density of the prototype at various output voltages

Output voltage	Power stage efficiency	System efficiency (including gate drive loss)	Power density*
1.5 V	Peak: 94.9% Full load: 90.4%	Peak: 93.5% Full load: 89.9%	540 W/in^3 137 W/in^2
1.2 V	Peak: 94.3% Full load: 89.5%	Peak: 92.5% Full load: 88.9%	432 W/in^3 110 W/in^2
1.0 V	Peak: 93.8% Full load: 88.4%	Peak: 91.6% Full load: 87.7%	360 W/in^3 91 W/in^2

* The volumetric power density listed here is calculated based on the prototype box volume in Table III. The areal power density listed here is calculated based on the prototype area 2.94×1.00 inch (74.7×25.5 mm) shown in Fig. 3.

the hardware prototype. The output voltage is regulated with a hysteretic control on the duty ratio D. Figs. 6(a) and (b) show the measured power stage efficiency and overall system efficiency (including gate drive loss) of the hardware prototype at various output voltages, with the measured efficiency and power density summarized in Table IV. The input voltage,

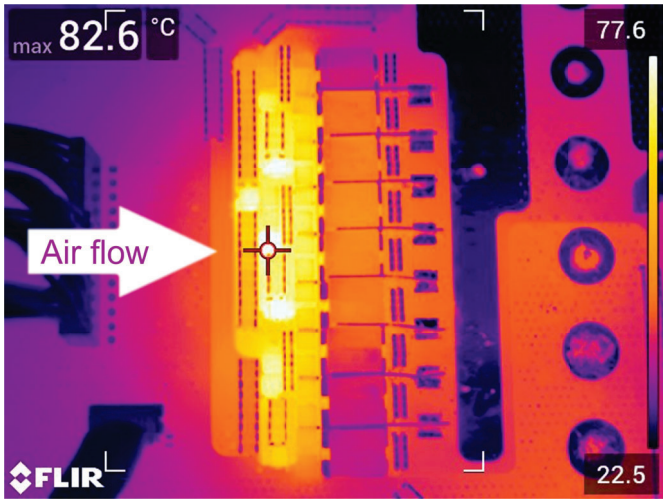

Fig. 7: Thermal image at equilibrium with fan cooling only. (V_{out} = 1.0 V, I_{out} = 270 A)

input current, and output voltage are measured with a high-precision Yokogawa WT3000E power meter, and the load current is measured with an electronic load Chroma 63203. The prototype is tested up to 270 A. At 1.0 V output voltage, the prototype achieves 93.8% peak efficiency (91.6% including gate drive loss) and 88.4% full-load efficiency (87.7% including gate drive loss), and 360 W/in^3 power density (by box volume).

Fig. 7 shows the thermal image of the hardware prototype at equilibrium with fan cooling only at V_{out} = 1.0 V and I_{out} = 270 A. As can be seen in Fig. 7, the hot spots are the floating switches in the middle of the converter. This is because they are neither connected to large pieces of copper in the PCB nor close to the ground plane that can serve as a good heat extractor. Since there is still space left above the MOSFETs, as illustrated in Fig. 4(b), heat sinks can be added to the top of the switches for more effective cooling if better thermal performance is desired.

Table V compares the performance of this work with several existing hybrid SC works. It can be seen that the proposed Dickson^2-PoL converter not only achieves a high power density but also maintains excellent peak and full-load efficiency, demonstrating great potential for both high efficiency and high power density. Further optimization can be achieved with advanced magnetic components (e.g., customized coupled inductors [11]) and better thermal design (e.g., 3D printed heat sink and immersion cooling).

V. Conclusion

This paper presents a Dickson^2 hybrid SC converter for direct 48 V-to-PoL conversion with high efficiency and high power density. The SC stage in the proposed topology can be viewed as two 3-to-1 Dickson SC converters directly merged together without an intermediate DC bus, and thus given the name *Dickson^2*. The proposed converter achieves complete soft-charging operation with a simple control, ensures natu-

TABLE V: Comparison between this work and existing 48 V-to-PoL hybrid SC works

Year	Reference	Output Voltage	Output Current	Power Density[+]	Power Stage Efficiency
2022	This work	1.5 V	270 A (30 A/phase)	540 W/in^3 (by box volume) 1062 W/in^3 (by power component volume)	Peak efficiency: 94.9% Full load efficiency: 90.4%
		1.0 V	270 A (30 A/phase)	360 W/in^3 (by box volume) 708 W/in^3 (by power component volume)	Peak efficiency: 93.8% Full load efficiency: 88.4%
2022	MLB-PoL [11]	1.0 V	60 A (30 A/phase)	263 W/in^3 (by box volume)	Peak efficiency: 92.7% Full load efficiency: 88.6%
2021	CaSP-PoL [7]	1.5 V	90 A (30 A/phase)	527 W/in^3 (by box volume)	Peak efficiency: 93.3% Full load efficiency: 88.8%
2021	VIB-PoL [8]	1.0 V	450 A (28.1 A/phase)	232 W/in^3 (by box volume)	Peak efficiency: 95.2% Full load efficiency: 89.1%
2021	On-chip series capacitor buck [9]	1.0 V	8 A (4 A/phase)	198 W/in^3 (by box volume)	Peak efficiency: 90.2% Full load efficiency: $\sim$76%
2020	LEGO-PoL [12]	1.5 V	300 A (25 A/phase)	171 W/in^{3*} (by box volume)	Peak efficiency: 96.0%* Full load efficiency: 87.7%*
2020	Crossed-coupled QSD buck [13]	1.5 V	40 A (20 A/phase)	150 W/in^3 (by power component volume)	Peak efficiency: 95.1%* Full load efficiency: 92.7%*

[+] The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry. The power component volume is calculated as the total volume of all switching devices, capacitors, and inductors in the power stage, excluding the gate drive circuitry.

[*] According to direct correspondence with the author.

rally balanced interleaved inductor currents, has a high SC stage conversion ratio and reduced conversion burden on the buck stage, and requires no large bus capacitors due to the switching bus architecture. A 48 V-to-PoL hardware prototype is built and tested up to 270 A load current (30 A/phase), achieving 93.8% peak efficiency, 88.4% full-load efficiency, and 360 W/in^3 power density (by box volume) at 1.0 V output voltage.

VI. Acknowledgements

This work was partially supported by Intel Corporation.

References

[1] N. Jones, "The Information Factories," *Nature*, vol. 561, pp. 163–166, 09 2018.

[2] A. Andrae and T. Edler, "On Global Electricity Usage of Communication Technology: Trends to 2030," *Challenges*, vol. 6, pp. 117–157, 04 2015.

[3] R. Miftakhutdinov, *Improving System Efficiency with a New Intermediate-Bus Architecture*, 2009. [Online]. Available: https://www.ti.com/download/trng/docs/seminar/Topic_4_Rais.pdf.

[4] S. Oliver, *From 48 V direct to Intel VR12. 0: Saving 'Big Data' $500,000 per data center, per year*, 2012. [Online]. Available: http://www.vicorpower.com/documents/whitepapers/wp_VR12.pdf.

[5] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "48-V Voltage Regulator Module With PCB Winding Matrix Transformer for Future Data Centers," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 12, pp. 9302–9310, 2017.

[6] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "Single-Stage High-Efficiency 48/1 V Sigma Converter With Integrated Magnetics," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 1, pp. 192–202, 2020.

[7] Y. Zhu, Z. Ye, T. Ge, R. Abramson, and R. C. N. Pilawa-Podgurski, "A Multi-Phase Cascaded Series-Parallel (CaSP) Hybrid Converter for Direct 48 V to Point-of-Load Applications," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 1973–1980.

[8] Y. Chen, P. Wang, H. Cheng, S. Allen, G. Szczeszynski, D. Giuliano, and M. Chen, "Virtual Intermediate Bus CPU Voltage Regulator," *IEEE Transactions on Power Electronics*, 2021. doi: 10.1109/TPEL.2021.3130213.

[9] H. Cao, X. Yang, C. Xue, L. He, Z. Tan, M. Zhao, Y. Ding, W. Li, and W. Qu, "A 12-Level Series-Capacitor 48-1V DC–DC Converter With On-Chip Switch and GaN Hybrid Power Conversion," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3628–3638, 2021.

[10] Z. Ye, R. A. Abramson, Y. L. Syu, and R. C. N. Pilawa-Podgurski, "MLB-PoL: A High Performance Hybrid Converter for Direct 48 V to Point-of-Load Applications," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, pp. 1–8.

[11] T. Ge, R. A. Abramson, Z. Ye, and R. C. N. Pilawa-Podgurski, "Core Size Scaling Law of Two-Phase Coupled Inductors – Demonstration in a 48-to-1.8 V Hybrid Switched-Capacitor MLB-PoL Converter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022.

[12] J. Baek, P. Wang, Y. Elasser, Y. Chen, S. Jiang, and M. Chen, "LEGO-

PoL: A 48V-1.5V 300A Merged-Two-Stage Hybrid Converter for Ultra-High-Current Microprocessors," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 490–497.

[13] M. Halamicek, T. McRae, and A. Prodić, "Cross-Coupled Series-Capacitor Quadruple Step-Down Buck Converter," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1–6.

[14] R. Das, G. Seo, D. Maksimovic, and H. Le, "An 80-W 94.6%-Efficient Multi-Phase Multi-Inductor Hybrid Converter," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 25–29.

[15] R. Das and H. Le, "A Regulated 48V-to-1V/100A 90.9%-Efficient Hybrid Converter for PoL Applications in Data Centers and Telecommunication Systems," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 1997–2001.

[16] J. S. Rentmeister and J. T. Stauth, "A 48V:2V Flying Capacitor Multilevel Converter Using Current-Limit Control for Flying Capacitor Balance," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 367–372.

[17] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and Comparison of Passive Component Volume of Hybrid Resonant Switched-Capacitor Converters," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–8.

[18] R. C. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 4008–4015.

[19] Y. Lei and R. C. N. Pilawa-Podgurski, "A General Method for Analyzing Resonant and Soft-Charging Operation of Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650–5664, 2015.

[20] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 770–782, 2016.

[21] Z. Ye, Y. Lei, W. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5965–5977, 2020.