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Design Techniques in CMOS LC Quadrature Oscillators for Broadband Applications

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Mahdi Bagheri

Committee in charge:

Professor Lawrence E. Larson, Chair
Professor Jim F. Buckwalter, Co-Chair
Professor Peter M. Asbeck
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2018

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The dissertation of Mahdi Bagheri is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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University of California San Diego

2018

DEDICATION

To my parents,

my brother, Rahim,

my sisters, and my wife, Soolmaz.

EPIGRAPH

”We choose to go to the moon in this decade and do the other things,

not because they are easy, but because they are hard, ...”

—John F. Kennedy, Rice University, September 12, 1962

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ABSTRACT OF THE DISSERTATION

Design Techniques in CMOS LC Quadrature Oscillators for Broadband Applications

by

Mahdi Bagheri

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2018

Professor Lawrence E. Larson, Chair
Professor Jim F. Buckwalter, Co-Chair

New standards are emerging every few months as wireless bands and services are proliferating across the world. End users of mobile headsets, wireless speakers, appliances controlled by internet, and many other devices want as many as possible new services and manufacturers have a hard time to keep up. Therefore, wireless radio solutions which can cover more bands and standards are in high demand. Multi-band multi mode radios by stacking up of multiple modules can be a choice to cover more bands in one system at a higher cost and larger area. Newer multi-band multi-mode radios integrate multiple radios into one chip and by reducing the

packaging cost, sharing the peripheral components, and lowering the size, cover larger frequency range at lower cost. Software defined radios (SDRs) and cognitive radios (CRs) can address the increasing demand of users to have seamless connection at low service cost and support wide range of applications [26]. Ultra-wideband (UWB) radios also cover a wide spectrum supporting universal applications in different countries. The WiMedia UWB radio technology requires the frequency synthesizers to cover the 3.1 GHz to 10.6 GHz spectrum. Different communication systems take advantage of millimeter-wave phased arrays such as 60 GHz short-range communication and point-to-point communication at the $E-$band (71-76 and 81-86 GHz) and the $W-$band (75-110 GHz). All the mentioned radios need carrier frequency generators which are able to cover all the frequency bands of interest which is several GHz. Also, these frequency generators must be able to generate quadrature local oscillator signal (LO).

Quadrature signals are essential in modern transceivers which can be generated in different ways. Among different ways, quadrature oscillators show better performance. The LC-QOSCs show a superior phase noise performance with excellent quadrature accuracy. To practically use CMOS LC quadrature oscillators, the randomness of the quadrature phase of the QOSCs should be fixed. The random phase sequence in LC-QOSCs results in limited tuning range which might be even zero. The series coupled QOSCs proposed in here address the quadrature phase sequence ambiguity by guaranteeing oscillation in one mode. Furthermore we have proposed a novel idea where the S-QOSC quadrature mode can be selected, and since each mode has a different frequency, in this way a wider tuning range can be achieved from the QOSC which is essential in wide tuning range frequency synthesizers and is useful in multi-band radios, SDR, CR, and UWB radios.

Replacing the crystal oscillators (XTALs) which are the main reference frequency generators in transceivers has a high priority to reduce the overall cost and power consumption of different wireless systems. CMOS frequency generators mostly cannot compete with the accuracy and phase noise performance of XTALs and even with the aid of calibration cannot achieve descent frequency stability due to temperature variation as they are very sensitive to temperature.

The focus of this work is on wide tuning range oscillators applicable in broad-band radios. This work presents a wide tuning range series coupled quadrature $S - QOSCs$ which is able to oscillate in desired quadrature mode of oscillation and eliminate the randomness in the quadrature sequence. By selecting the mode, the proposed $S - QOSC$ (Chapter 4) has a very wide tuning range which is the combination of tuning range of different modes. It has also been shown (Chapter 5) that the proposed $S - QOSC$ can be designed to show two orders of magnitude less temperature sensitivity compared to other LC oscillators and can be implemented in a system to be calibrated to achieve the required frequency accuracy of various applications. In this work an LO-phase shifting approach based on ILO at frequency range of 71 to 86 GHz will be presented.

Chapter 1

Introduction

The wireless industry is proliferating fast and offering users more convenient ways of data transfer technologies. Every often new application for wireless appears, often resulting in a new standard. End users want to access more of a single handset, therefore, for manufacturers it is hard to keep up. Hence, a universal wireless radio which is able to support more bands and standards is in high demand. Such radio should cover more frequency bands while keeping the cost low. In this chapter we summarize various broadband wireless services and standards including multi-band multi-mode radios, software defined radios (SDRs), cognitive radios, and ultra-wideband (UWB) radios.

1.1 Multi-band Multi-mode Radios

To address low service cost and with support of wide range of applications; manufacturers are including more and more wireless radio technologies into their platform. If they must

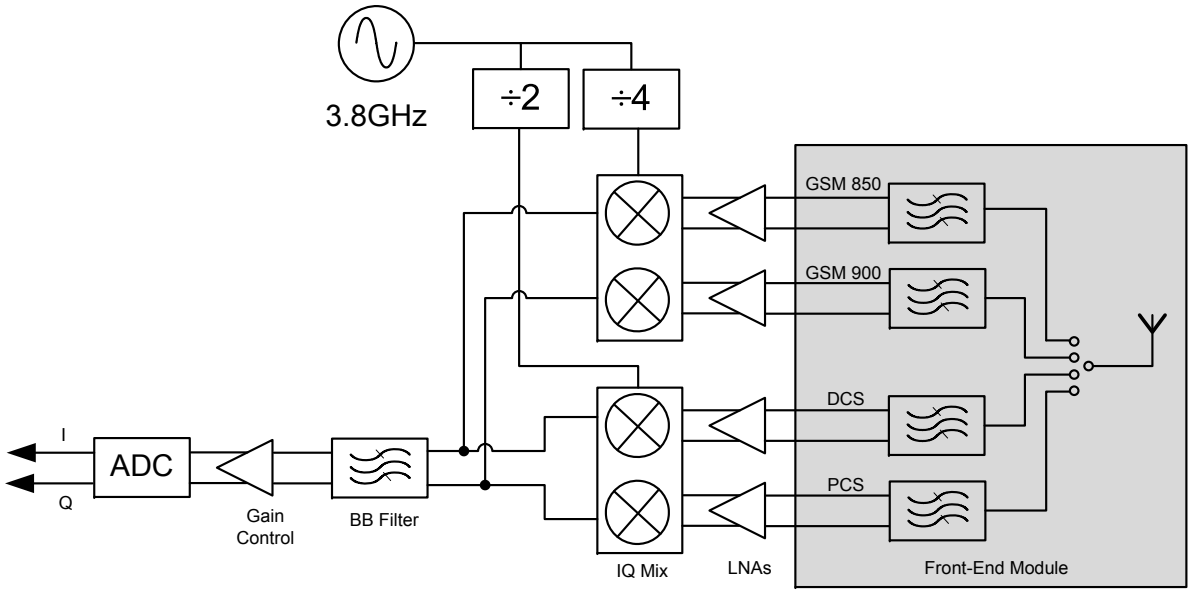

Figure 1.1: Quad-band GSM/GPRS radio; multiple RF nlocks and off-chip components are stacked up [1, 2].

achieve this by just stacking different radio modules (module stack-up), their equipment will take up a larger area and cost more which represent an unacceptable result to the market. Instead, industry has moved toward multiband multimode radios. Such radios aim to provide operation over multiple frequency bands for multiple RATs at a lower cost than brute force stack-up. Several examples of such radios significantly outperform radios using the module stack-up approach [1].

The multiband, multimode approach integrates multiple radios into one chip and so offers lower packaging cost, lower size and some sharing of peripheral components. Digital portions of the link could be also shared for different RATs. Even if it is not possible to benefit from this sharing, integrating more digital circuitries can be afforded by moving to lower technology nodes. Furthermore, the analog IF stages may be partially shared, depending on how similar

different RATs are. For example, GSM, GPRS and EDGE may share many digital and analog IF blocks. However, GSM, WCDMA and 802.11a share few. However as Fig. 1.1 shows, multiband multimode radios often have several specific RF front-ends stacked up for each band or mode [1, 2]. Typically, when the number of covered bands and technologies grows to more than four, the extra expense compared to a single radio becomes quite noticeable, and a different approach is needed.

1.2 Software Defined Radio

A radically different approach to addressing users' need for seamless connection has been conceptualized in a single radio capable of covering all bands and all standards [26].

In the early 1990s, Mitola used the term software- defined radio, or SDR, to refer to a radio which is completely programmable by software and has no analog block except for ADC/DAC Fig. 1.2. As will be described in following chapter, Mitola's SDR is not suitable for portable applications [3].

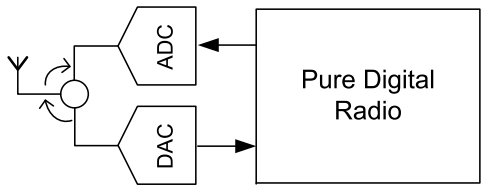

Figure 1.2: Mitola's SDR concept [3].

Blust uses SDR as a practical way of implementing the all-band all-standards radio idea which includes many analog processing blocks too [27]. It uses SR as the next stage of evolution,

where the only analog blocks are ADC and DAC; this is similar to Mitola's SDR. He uses SBR as the general term for the idea, which can be realized either as SDR or SR. The definition of SDR is targeted towards mobile terminals and is a platform which can be programmed to receive any single channel, with any modulation, located anywhere in a broad but finite predefined band. To be tuned to any channel, the transmitter frequency generator needs to cover wider frequency spectrum, therefore, there is a need for wide-band frequency synthesizers.

1.3 Cognitive Radios

The heavy usage of cellular and wireless bands has made cognitive radios (CRs) attractive. Conventional wireless transceivers operate in only predefined frequency bands, while CRs are envisioned to utilize any unoccupied channel frequency in the wide frequency range of few megahertz to about 10 GHz [14]. CR can sense and detect any unused frequency band [28, 29] and use it as needed. If SDR could be realized both on the base station (access points) and user side (handset, user unit), then it will be an extremely exciting achievement for CR. CR adds more intelligence to SDR to use the very expensive frequency spectrum efficiently. This removes the need to allocate a specific frequency band to a specific application and keep it inaccessible even when not in use. CR is certainly one future technology waves, but there are technological and regulatory problems to be solved, one of which is SDR availability.

1.4 Untra-wideband Radios

Ultra-wideband (UWB) wireless communication is a revolutionary technology for transmitting large amounts of digital data over a wide frequency spectrum using short-pulse and low powered radio signals. UWB commonly refers to a signal or system that uses either a large fractional bandwidth (BW) greater than 20% or an absolute bandwidth of more than 500 MHz. A 14 February 2002 report and order by the Federal Communications Commission (FCC) authorizes the unlicensed use of UWB in the frequency range from 3.1 GHz to 10.6 GHz. The original application of UWB was radar imaging with low data rate, while later it targeted wireless universal serial bus (WUSB), sensor data collection, precision locating and tracking, and wireless personal area network (WPAN). UWB provides an efficient use of the scarce radio bandwidth by enabling both high data rate in a short range or low data rate for longer-range applications [30, 5, 21].

Most of electronic devices such as printers, cameras, phones, high-speed data storages, video streaming devices use the standard interfacing of USB 2.0 with fast data transfer speed of $480Mbps$. By increasing the use of PAN and USB interface, a wireless solution to replace the USB cables is inevitable and UWB is a possible solution which is able to match the data rate of USB in short-range applications. Fig. (1.3) shows the application of a WPAN solution replacing USB cable connection with Wireless USB (WUSB) in homes and offices.

A significant difference of UWB compared with the conventional transmission systems, which use amplitude modulation (AM), the frequency modulation (FM), and/or phase modulation (PM) of a sinusoidal wave, is the way that information is transmitted in UWB. In UWB,

Figure 1.3: WUSP application by replacing USB cable connection in PAN [4]

the information is transmitted by generating radio energy at specific time intervals in a large bandwidth, thus enabling pulse-position or time modulation. It can also be done by modulation of UWB signals (pulses) by encoding the polarity of the pulse, its amplitude, and/or by using orthogonal pulses [31].

UWB transmission unlike spread spectrum, does not interfere with narrowband and carrier based transmission in the same frequency band and FCC regulated the efficient use of bandwidth enabling high-data-rate WPAN for short-range and low-data-rate with longer range for radar and imaging systems [5]. As defined by FCC's first report, UWB refers to a system with bandwidth of greater than 500 MHz or a fractional bandwidth larger than 20% at all times of transmission. The fractional bandwidth is defined as

$$B_f = \frac{BW}{f_c} = \frac{2(f_h - f_l)}{f_h + f_l} \tag{1.1}$$

where f_h and f_l are the highest and lowest cutoff frequencies of a UWB spectrum, respectively. While UWB has a fractional bandwidth of greater than 20 percent, wideband signals are classified with fractional bandwidth of less than 20% and narrowband signals have fractional bandwidth of less than 1%. Table 1.1 shows the classification of signals based on the fractional bandwidth. Bluetooth and 802.11n with fractional bandwidth of 0.04% and 0.74%, respectively, are classified as narrowband signals.

The Multi-Band Orthogonal Frequency Division Modulation (MB-OFDM) scheme for UWB divides the spectrum of 3.1 GHz to 10.6 GHz into fourteen bands with bandwidth of 528 MHz and center frequencies of

Table 1.1: Classification of signals based on their fractional bandwidth.

	Fractional Bandwidth
Narrowband	$< 1\%$
Wideband	$1\% < B_f < 20\%$
Ultra-wideband	$> 20\%$

$$f_c = (2n + 11) \times 264MHz \tag{1.2}$$

where n refers to the band number 1 to 14. These fourteen bands are grouped into six band groups as shown in Table 1.2 [21, 32].

A time-frequency code (TFC) is used to distribute the coded information over different bands within a band group. There are three different types of time frequency codes defined in [32]. The first one is time-frequency interleaving (TFI) where the coded data is spread over three bands of a band group. The second one is two-band time-frequency interleaving (TFI2) where the coded data is spread over two bands within a band group, and the third is referred to as fixed frequency interleaving (FFI) where the coded data is transmitted over a single band of a band group.

An example of time frequency interleaving, also known as band switching or frequency hopping, for bands in band group 1 is shown in Fig. 1.4 [4]. The switching time of 9.5 ns in Fig. 1.4 is the critical timing for the design of the frequency synthesizer, which we will focus on

in the next chapters.

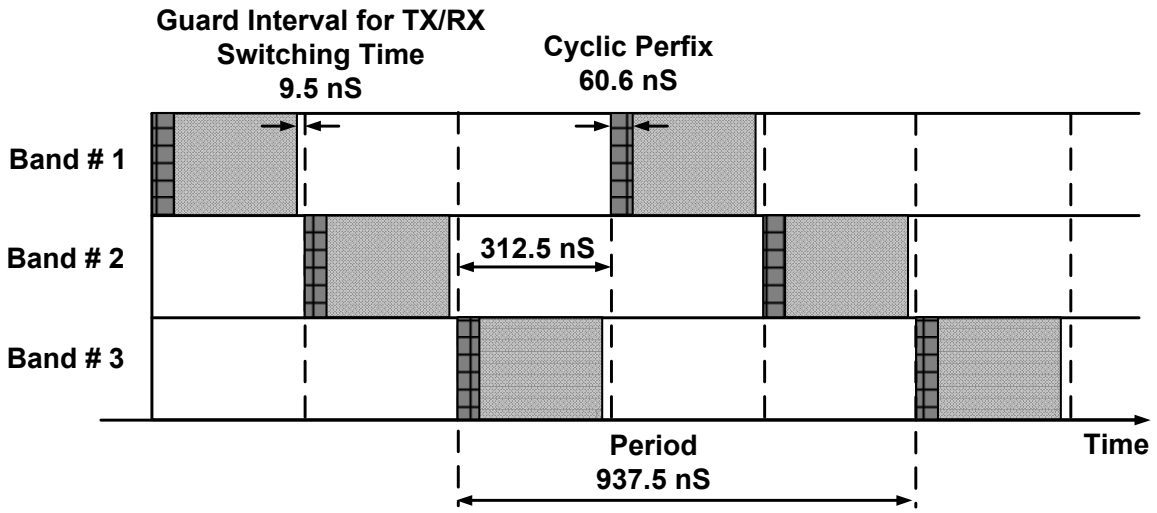

Figure 1.4: An example of time-frequency interleaving for band group 1.

Time frequency codes (TFC) required for different band groups are specified in [32]. TFC codes of band group one are shown in Table 1.3 [4]. This table shows a total of ten TFC codes, hence it can support up to ten different channels. Time frequency codes for other band groups are similar to ones for band group one, with the exception of the fifth and the sixth band groups. The band group 5 only consists of two bands (bands 13 and 14). Hence, it only has one two-band time-frequency interleaving (TFI2) channels and one fixed frequency interleaving (FFI) channel. Band group six shares one band with band group three and two bands with band group four. As a result, all of its FFI codes and one of its TFI2 codes overlap with channels of band groups three and four [4].

1.4.1 Regulatory Limitations

The FCC spectral mask (that is, the operating restrictions for UWB in the United States) specifies 7.5 GHz of usable spectrum bandwidth between 3.1 GHz and 10.6 GHz for communications devices [5]. The FCC also protects existing users operating within this spectrum by limiting the UWB signal's transmit power. The UWB devices' power spectral density levels are limited to -41.3 dBm/MHz. The primary difference between indoor and outdoor operation is the higher degree of attenuation required for the out-of-band region for outdoor operations. This further protects GPS receivers, centered at 1.6 GHz. Previously at an IEEE meeting in July 2003, the Multiband OFDM Alliance (MBOA) and Motorola/XtremeSpectrum groups had argued over whether or not the MBOA can use a frequency-hopping technique and still meet the 802.15.3a's data and range requirements while remaining in compliance with the FCC's stated declarations on how frequency-hopping systems should be tested. While the FCC has set precedents in terms of changing the rules according to newly defined IEEE standards (for example, 802.11), few rules were as strongly debated as those for UWB. Adding to this complexity is the fact that the original UWB opponents are continuing to debate the original FCC rules [22]. In addition, there is limitation on the emission power of UWB in different regions.

Figure 1.5 shows the narrowband wireless systems that exist in the vicinity of the UWB span or are overlapping with them [21, 33, 34]. As can be seen from this figure, certain wireless systems, such as WiMax and different variations of Wi-Fi, overlap with the spectrum of 3.1 - 10.6 GHz. Operation of a UWB device must not cause any performance degradation for other devices that use the UWB spectrum. In addition, UWB must not generate out-of-band spurs that

can affect operation of systems outside the UWB spectrum.

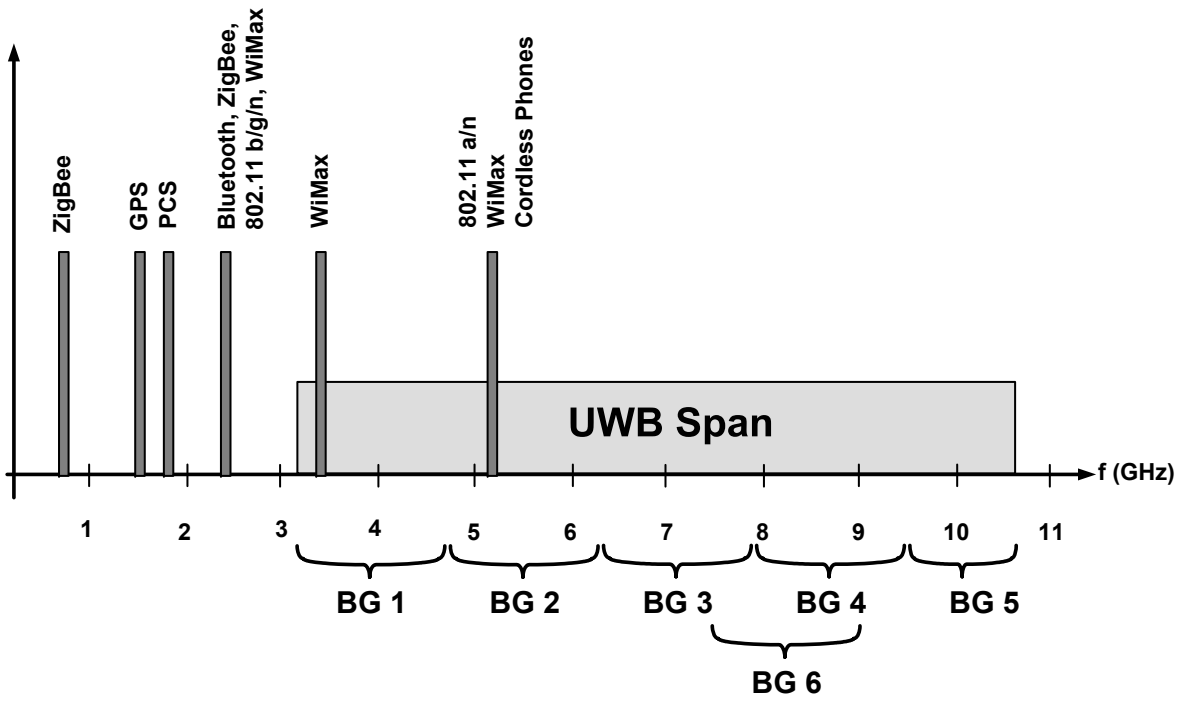

Figure 1.5: Frequency usage of the spectrum of 1 GHz to 11 GHz by wireless communication standards [4].

According to part 15 of FCC regulations, the allowable transmitted signal power of any UWB device needs to be less than -41.3 dBm in 1 MHz bandwidth while using a bandwidth greater than 500 MHz [5]. In addition, the maximum equivalent isotropically radiated power (EIRP) for the operation of indoor and hand held (outdoor) UWB devices are specified by the FCC. The transmitted power should meet the mask spectrum standardized by the FCC, European Conference of Postal and Telecommunications Administrations (CEPT), Japan, and other countries. For example Fig. 1.6 shows the UWB mask for FCC, CEPT, and Japan.

The worldwide regulation of the spectrum of 3.1 GHz to 10.6 GHz is shown in Fig. 1.7

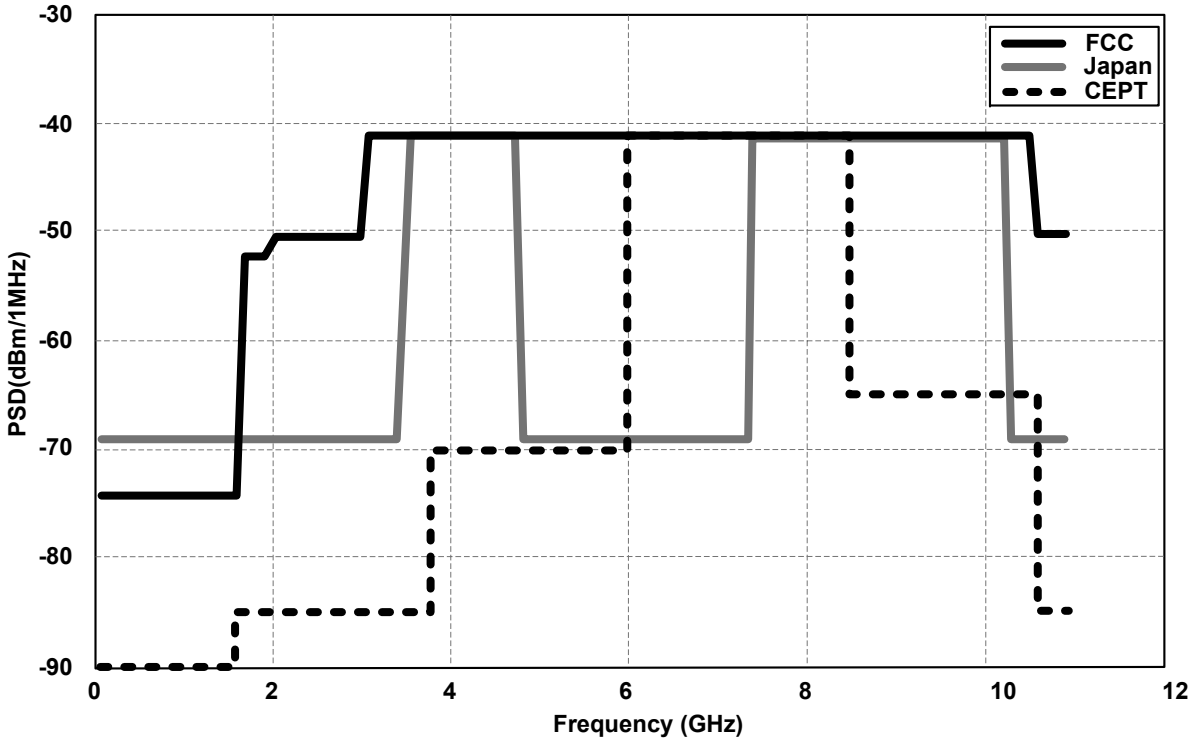

Figure 1.6: UWB mask for FCC, CEPT, and Japan [5].

[32, 6]. As can be seen from Fig. 1.7, this 7.5 GHz of bandwidth is unlicensed in the United States, but not available worldwide. Only band group six is available worldwide. As a result, all the UWB devices need to support band group six. However, band eleven requires detection and avoid (DAA) for operation in Europe.

In the next chapter, we will study frequency synthesizer for UWB systems and we will see that the allocated band groups (Fig. 1.7) will be challenging in the desing of proposed UWB frequency synthesizer. Especially, having a wider tuning range in oscillators helps to achieve a flexible design of UWB frequency synthesizer.

1.4.2 Advantages of UWB

The power requirement by FCC for UWB is $-41.3\ dBm/MHz$ [5] and puts UWB systems in the category of unintentional radiators, such as TVs and computer monitors. Such low power radiation allows UWB systems to reside below the noise floor of a typical narrowband receiver and enables UWB signals to coexist with other radios with minimal or no interference [22]. However, it depends on the type of modulation of UWB system.

Another major advantage of UWB is the improved data rate or channel capacity (C) of the large bandwidth of UWB pulses. Channel capacity is defined as the maximum amount of data that can be transmitted per second over a communication channel by *Hartley-Shannon's* formula [4]:

$$C = Blog_2(1 + SNR) \tag{1.3}$$

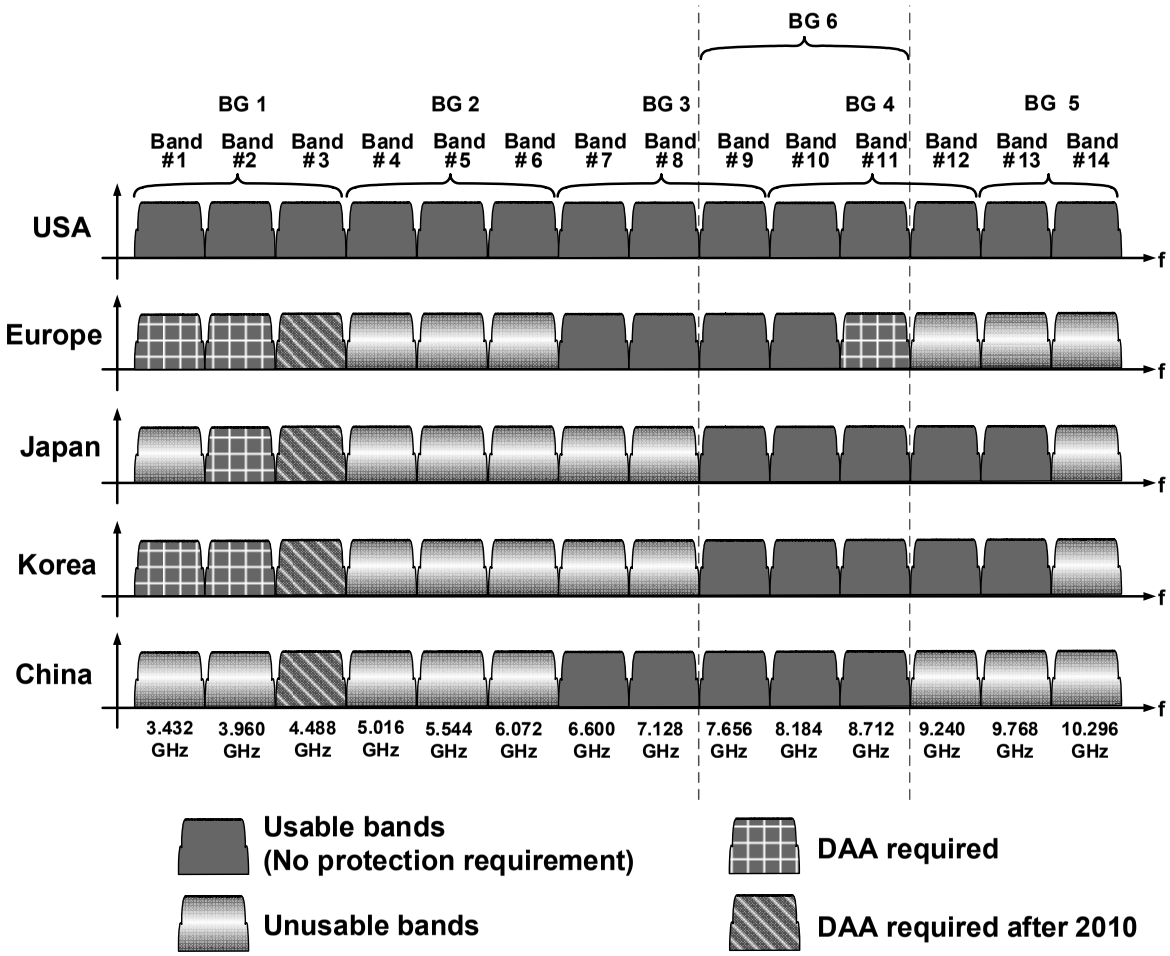

Figure 1.7: Worldwide regulatory for MB-OFDM UWB [6].

where C is the maximum channel capacity, B is the bandwidth, and SNR is the signal-to-noise power ratio. The large bandwidth available in UWB results in a high potential data rate of giga bits per second ($Gbps$). As it is mentioned earlier, the FCC power limitation of -41.3 dBm/MHz for UWB results in Gbps data rate available only for short range applications like WPAN [22].

Equation (1.3) also shows that the channel capacity is logarithmically proportional to SNR. Therefore, UWB communication systems can work in low SNR channels and, as a result of the large bandwidth, still have a large channel capacity.

Resistance to jamming is another advantage of UWB systems. Any intentional and unintentional jammer, can only jam some frequencies in the UWB spectrum at once. Therefore, if some of the frequencies in the spectrum are jammed, there is still a large range of frequencies untouched. The high performance in multipath channels, which is unavoidable in wireless channels, is another advantage of UWB systems.

Table 1.4 shows the main advantages and benefits of UWB systems over narrowband wireless technologies [22].

1.4.3 UWB Transceiver

Fig. 1.8 shows the block diagram of a typical UWB transceiver. The main challenge in UWB is to achieve the requirement of wide bandwidth from 3.1 GHz to 10.6 GHz, for a universal solution, while keeping power consumption low and saving the area of the chip. Among the different blocks in UWB transceiver, the frequency synthesizer needs to be fast enough to hop at the rate of 3.2 MHz, and meet the allocated time of band switching which is only 9.2 ns.

Coexistence of UWB with Wi-Fi and other technologies limits the spurious tones to be smaller than -50 dBc in some frequencies. Also, in-band spurs must be as low as -30 dBc to satisfy the required bit error rate (BER). The phase noise requirement is also challenging to be met. Furthermore, the frequency accuracy of 20 ppm is another critical requirement in the frequency of transmission [4].

The receive (RX) and transmit (TX) path in Fig. 1.8 are quadrature and mixers, driven by a quadrature local oscillator (LO) generated by a frequency synthesizer. Therefore, the quadrature accuracy of the LO is critical to achieve a good image rejection in mixers.

1.5 Thesis Organization

Carrier frequency generation in broadband radios is difficult because they seek operation in a broadband spectrum. Among the building blocks of above mentioned broadband radios, wideband frequency synthesizers are one of the most critical parts which generate the carrier frequency for the radios. Wideband frequency synthesizers enable low-cost low-power multi-standard, multi-band multi-mode radios, SDRs, CRs, and UWB wireless systems to cover a wide frequency range. The core of each wideband synthesizer is the voltage-controlled oscillator (VCO) which needs to cover the required wide frequency range. To make it happen, there are different ways to design oscillators (and frequency synthesizers) including varactor-based oscillators, switched-capacitor oscillators, switched inductor oscillators, synthesizers with multiple VCOs or multiple PLLs, synthesizers using one or more PLLs and dividers, mixers, and multiplexers and ... Quadrature signal generation is essential for modern transceivers which can

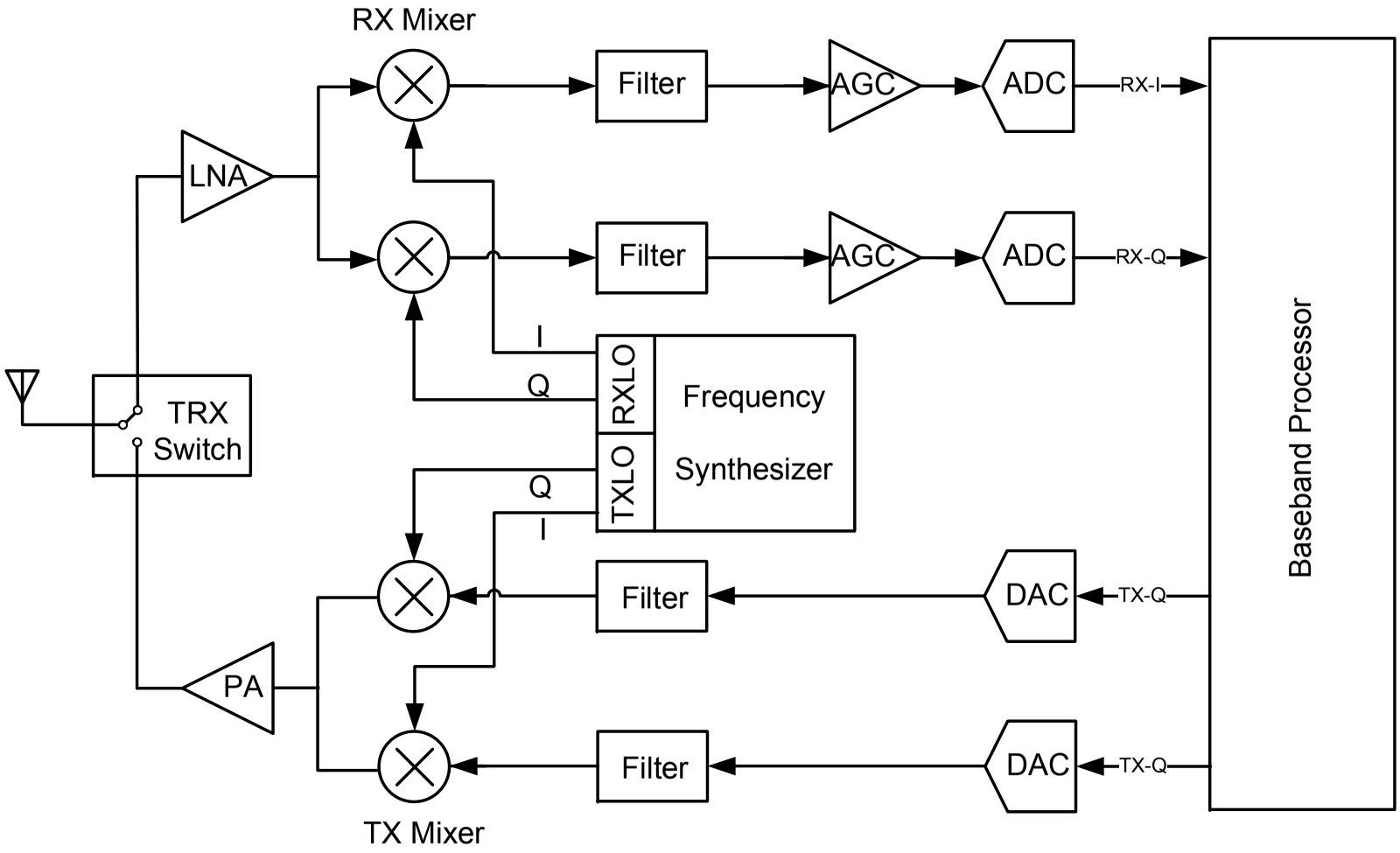

Figure 1.8: Block diagram of a typical UWB transceiver.

be generated with different methods and the best way of generating quadrature signal is using differential oscillators followed by divider by two or using quadrature oscillators.

In this thesis we study broadband oscillators and frequency synthesizers and different topologies to achieve the wide tuning range in Chapter 2. Wide tuning range VCOs including varactor-based VCOs, switched-capacitor VCOs, switched-inductor VCOs, switched coupled-inductor VCOs, self-switching VCOs, switchless multi-band VCOs, and multi-port coupled-inductor VCOs will be reviewed in this chapter. Different wideband frequency synthesizers like multiple VCO synthesizers, multiple fixed frequency PLLs, PLLs with chain of dividers, mixers, and multiplexers, and a UWB fast hopping frequency synthesizer with superior spurious performance will also be reviewed in this chapter. Then we review different quadrature signal generation methods in Chapter 3. Divider by two, poly-phase filters, quadrature ring oscillators, and LC quadrature oscillators will be reviewed in this chapter. Quadrature oscillators are one of the common methods of quadrature signal generation which traditionally suffer from randomness in the quadrature sequence. In this chapter we study different ways to fix the randomness in quadrature phase of quadrature oscillators. Chapter 4 presents the proposed wideband series coupled quadrature oscillator with deterministic output sequence. We study the geometrical analysis of how the proposed quadrature oscillator operates in deterministic way. A linear analysis shows the important parameters for this operation. Then the wide tuning range achieved by series-coupled quadrature oscillator will be presented which is the result of selective mode switching. By linear analysis we explain how this S-QOSC works and center frequency and continuous tuning range will be studied. Phase noise of proposed S-QOSC will be studied and measurement results of different S-QOSCs operating at different center frequencies will be pre-

sented at the end.

In Chapter 5 we study the temperature sensitivity of oscillators as a replacement for crystal (XTAL) oscillators. This chapter studies the temperature behavior of LC tank first, then temperature sensitivity of non-degenerate modes in proposed CMOS LC series-coupled quadrature oscillators. Measurement results will be presented at the end. In Chapter 6 a wideband injection-locked VCO will be studied which has been utilized in a 71-86 GHz phased array transceiver and Chapter 7 will conclude this dissertation.

In Chapter 6 an LO-phase shifting approach based on ILO at frequency range of 71 to 86 GHz will be presented. The implemented oscillators operate at one-fourth of required LO tuning range and provides a power-efficient solution for scalable mm-wave phased array. The measured locking bandwidth of ILO is 250 MHz and phase shift range is ± 300 with less than 1 dB amplitude variation.

Table 1.2: MB-OFDM band group allocation [21].

Band Group	Band ID n	Center Frequency (GHz)	BG Frequency Range (GHz)
1	1	3.432	3.168-4.752
	2	3.960	
	3	4.488	
2	4	5.016	4.752-6.336
	5	5.544	
	6	6.072	
3	7	6.600	6.336-7.920
	8	7.128	
	9	7.656	
4	10	8.184	7.920-9.504
	11	8.712	
	12	9.240	
5	13	9.768	9.504-10.560
	14	10.296	
6	9	7.656	7.392-8.976
	10	8.184	
	11	8.712	

Table 1.3: Time-Frequency Code Patterns for Band Group 1 [4].

TFC number	Base sequence/ Preamble	Band ID (n) for TFC					
1	1	1	2	3	1	2	3
2	2	1	3	2	1	3	2
3	3	1	1	2	2	3	3
4	4	1	1	3	3	2	2
5	5	1	1	1	1	1	1
6	6	2	2	2	2	2	2
7	7	3	3	3	3	3	3
8	8	1	2	1	2	1	2
9	9	1	3	1	3	1	3
10	10	2	3	2	3	2	3

Table 1.4: Advantages and benefits of UWB communications [22].

Advantage	Benefit
Coexistence with current narrowband and wideband radio services	Avoids expensive licensing fees.
Large channel capacity	High bandwidth can support real-time high-definition video streaming.
Ability to work with low SNRs	Offers high performance in noisy environments.
Low transmit power	Provides high degree of security with low probability of detection and intercept.
Resistance to jamming	Reliable in hostile environments.
High performance in multipath channels	Delivers higher signal strengths in adverse conditions.
Simple transceiver architecture	Enables ultra-low power, smaller form factor, and better mean time between failures, all at a reduced cost.

Chapter 2

Broadband Oscillators and Frequency Synthesizers

The explosive growth of mobile wireless communication in the last few years and many new proposed wireless standards raised the need for more research on multi-standard operations. However, building a system configurable for different frequency bands and various system requirements is very challenging. To design carrier generation system covering major communication standards like GSM, WCDMA, WLAN, and Bluetooth multiple works have been done. Broadband VCOs as the heart of carrier generation play an important role in multi-standard system design, specially with lo phase noise and low power consumption [35, 36]. Wide tuning range oscillators are essential for low-cost and low-power multi-band multi-mode radios as well as software defined radios (SDRs), cognitive radios (CRs), and ultra-wideband (UWB) radios. The larger tuning range of the oscillator is, the wider frequency band that a frequency synthesizer can cover with only one voltage controlled oscillator (VCO). Multi-band multi-mode radios can

benefit from wide tuning range oscillators to reduce number of VCOs to cover different bands and modes. SDRs can also take advantage of the wide tuning range oscillators to cover the targeted frequency range of 1 to 6 GHz with less number of VCOs. The same story is valid for CRs and UWB systems.

In this chapter, we will study different design topologies for wide tuning range frequency synthesizers and VCOs including large varactor-based VCOs, switched-capacitor VCOs, switch-inductor VCOs, multi VCO synthesizers, frequency synthesizers with dividers, mixers, and multiplexers, coupled inductor based VCOs. Then we compare the different topologies and present an enhanced tuning range quadrature oscillator (QOSC) based on quadrature mode switching. Most electronic devices need a variety of standard frequencies generated for their operation. A reference frequency is utilized in many systems as the system frequency. The system frequency often provides the foundation of timing in the system. However, there are many subsystems in these devices which need different frequencies. These extra frequencies are different from the reference or they have some requirements that the reference frequency cannot meet. Thus, frequency synthesis from a reference is an important consideration in the design and development of electronic systems. High frequency synthesizers may utilize mixers, which generate spurious products (spurs) over the bandwidth. This is problematic when the bandwidth is restricted by government regulations. Therefore, spurs may limit the usable available bandwidth. There are also other requirements, such as settling time of the synthesizer which makes the design even more challenging. In this chapter we present different methods of frequency synthesis for UWB systems and then explain the proposed fast hopping UWB frequency synthesizer in detail.

2.1 Different Topologies for Broadband Frequency Synthesizer

A frequency synthesizer is a system that generates different frequencies from a frequency reference (usually a crystal oscillator). Mobile phones, televisions, radio transceivers, satellite transceivers, GPS systems, and many other systems are the devices that utilize frequency synthesizers. The output of the frequency synthesizer should be stable and accurate enough over different environment variations (depending to the application). For example, the output frequency must be within the specified range of the application over temperature variation and components aging. Different techniques of frequency multiplication, frequency division, direct digital frequency synthesis (DDFSs), frequency mixing, and phase-locked loops (PLLs) may be used in frequency synthesizers. The application of the frequency synthesizer will define which technique is to be used based on the different specifications of cost, frequency resolution, switching speed (settling time), phase noise performance, power consumption, and spurious performance.

2.2 Phase-locked Loop (PLL)

Phase-locked loop (PLL) is the common way of frequency synthesis which is a feedback system. Fig. 2.1 shows the block diagram of a PLL. The reference frequency (f_{ref}) is usually derived from a crystal oscillator which is very accurate and stable. A voltage controlled oscillator (VCO) generates the output frequency which is locked to the N times the reference frequency and feeds the divider by N. The output of divider by N, f_m is fed back to the phase-frequency

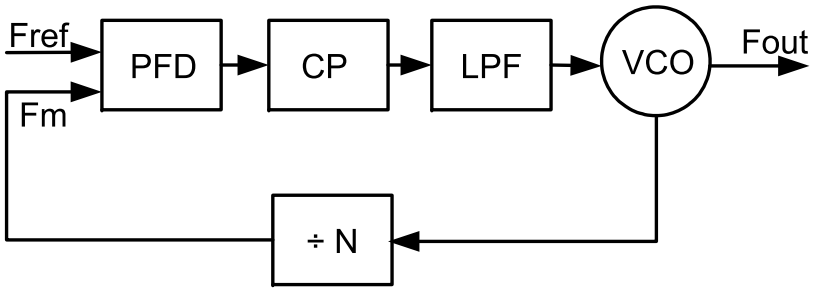

Figure 2.1: Block diagram of a common PLL.

detector (PFD) which creates an error signal proportional to the phase difference of the f_{ref} and f_m. The Charge pump (CP) injects (or sinks) a current proportional to the phase error and drives the loop filter which is low-pass filter (LPF). The output of LPF is filtered voltage ($V_{control}$) which controls the VCO frequency to make it equal to the desired frequency.

The main issue with this type of frequency synthesis is the settling time which is typically few μs and is not directly suitable for UWB applications with hopping time requirement of few ns [37]. Also a fractional-N PLL is required to obtain the 528 MHz channel spacing out of that reference frequency.

2.3 PLLs with Wide Tuning Range VCOs

2.3.1 Varactor-based VCOs

A common practice to design a wide tuning range CMOS VCO is using a large varactor-tuned LC resonator [13]. Fig. 2.2 shows a simple VCO with cross coupled NMOS (M1 and M2)

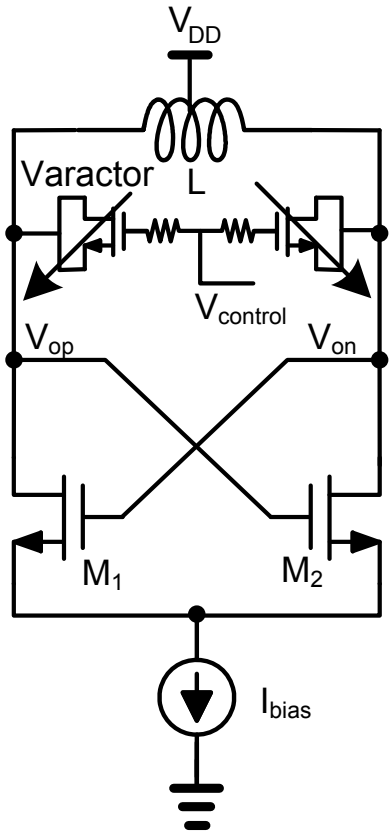

Figure 2.2: Schematic of a simple VCO with MOS varactor.

for negative g_m and a MOS varactor (M3) for tuning the frequency of oscillation.

The oscillation frequency, ω_o, of this VCO is

$$\omega_o = \frac{1}{\sqrt{LC_{tot}}} \tag{2.1}$$

where L is the integrated resonator inductance and C_{tot} is the total capacitance of the tank. We can derive the relation between tuning range of oscillation and tuning range of tank capacitance as

$$\frac{\Delta\omega}{\omega_o} = \frac{1}{2}\frac{\Delta C}{C_{tot}} \tag{2.2}$$

The tuning range of varactors is limited to the ratio of C_{max} to C_{min} which is typically around 5. Therefore, $\frac{\Delta\omega}{\omega_o}$ is limited. Moreover, by using only a large varactor for wide tuning range, the K_{VCO} will be very high, making the VCO phase noise susceptible to the noise of the tuning voltage in $PLLs$. Also the linearity of K_{VCO} would be degraded by departing from center frequency which is a drawback in design of PLLs.

2.3.2 Switched-capacitor VCOs

In order to increase the tuning range of VCOs, the switched capacitor resonators have been proposed [7, 8]. The switched capacitors can be used for coarse and fine tuning while a small varactor can be used in parallel in phase locked loops (PLLs). By using a small varactor, the VCO gain is reduced and the phase noise will be improved. Fig. 2.3 shows the VCO with switched capacitor resonator.

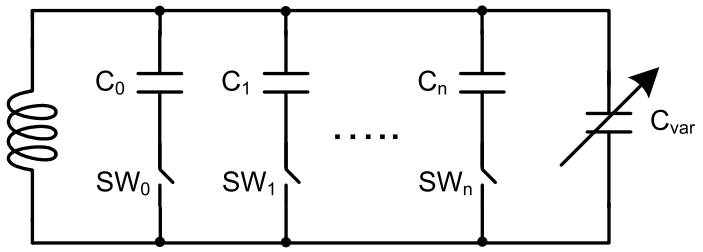

Figure 2.3: Resonating LC tank with switched-capacitors [7].

In switched capacitors the size of switch imposes the quality of the tank. Therefore, the switch should be large enough to keep the quality of the resonator limited to the quality of the inductor of the resonator. On the other side, adding a very large switch will degrade C_{max}/C_{min} of the switched capacitor resulting in a lower frequency tuning range. Having too many of switched capacitors also introduce more routing and again degrades the tuning range. Therefore, there is a limitation in size of switches and number of switched arrays.

2.3.3 Switched-inductor VCOs

The resonator of a VCO can be tuned by switching its inductor [7, 8]. Fig. 2.4 shows the schematic of a VCO with switched inductor. The main problem of this design is the reduced quality factor of the inductor. An on-chip inductor is low quality by itself and by adding the switch loss, the quality will be degraded more. Therefore, the phase noise performance will be degraded. Finally, the chip area of switched-inductor VCOs becomes large due to using several on-chip inductors.

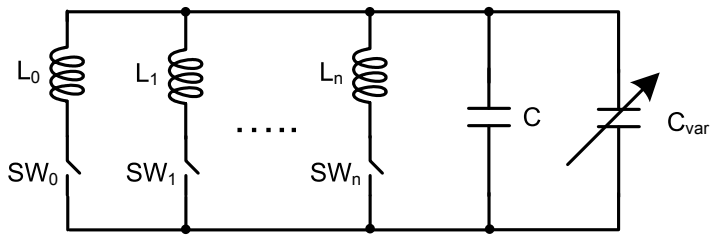

Figure 2.4: Resonating LC tank with switched-inductors [8].

2.3.4 Switched Coupled-inductor VCOs

Multiple resonance can be achieved by using switched-coupled inductors [38, 9, 10]. Fig. 2.5 and Fig. 2.6 show the tanks with switched-coupled balun and switched-coupled inductors.

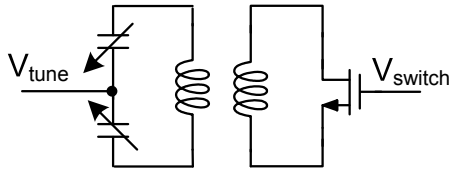

Figure 2.5: Switched balun LC tank [9, 10].

Despite the more resilience of quality factor (Q) to switch loss and the smaller area of the switched-coupled inductors comparing with switched-inductors, the Q is still degraded. Moreover, the parasitic capacitance of the switch limits the tuning range of the oscillator.

Fig. 2.7 shows the block diagram of the multi-standard VCO which supports GSM, DCS, Bluetooth, and WLAN.

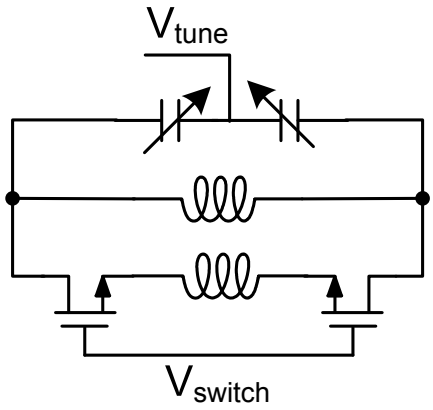

Figure 2.6: Switched LC tank [9].

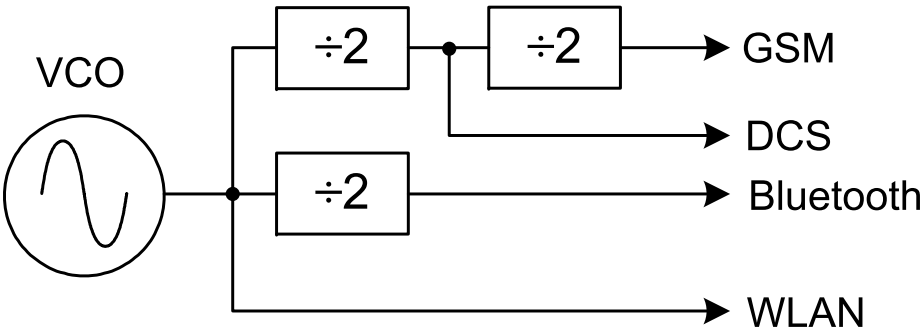

Figure 2.7: Block diagram of multi-standard VCO [9].

2.3.5 Self-switching VCOs

In another approach to increase the tuning range of an oscillator, switches are used in [39, 10] to change the number of turns of the on-chip inductor. Fig. 2.8 shows the resonator with self-switching inductor.

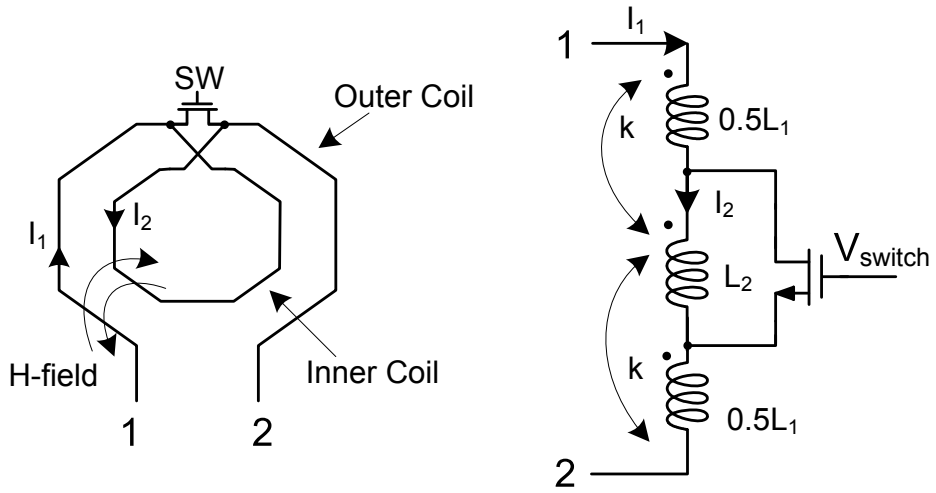

Figure 2.8: Self-inductance switching [10].

In this approach similar to switched-capacitors and switched-inductors switch loss degrades the resonator quality factor resulting in worse phase noise performance. Also, the parasitic capacitance of the switch limits the tuning range of the oscillator.

2.3.6 Switch-less Multi-band VCOs

To cover a wide frequency range switched-less dual-band transformer-based VCOs have been reported [11, 40]. Fig. 2.9 shows the schematic of a VCO with switch-less dual-band

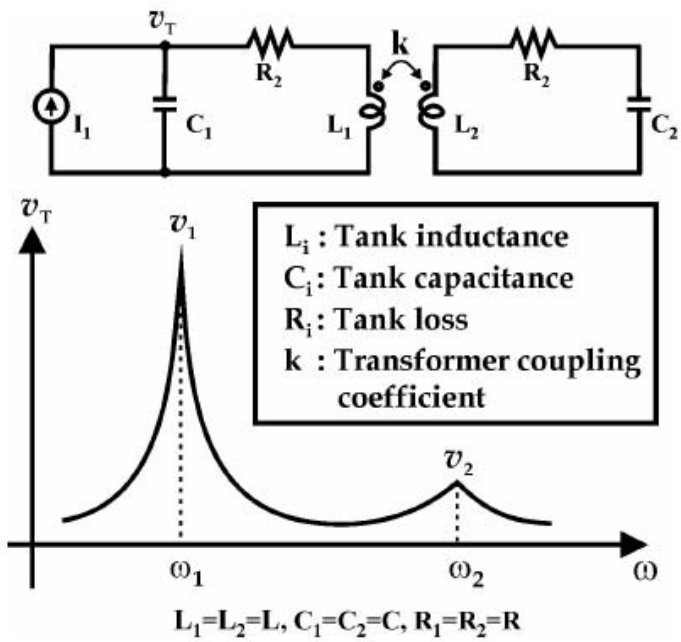

Figure 2.9: Double-tuned single driven transformer [11].

resonator.

A dual-mode oscillators based on multiple active cores and coupled inductors has been presented in [41]. Fig. 2.10 shows the dual-mode oscillator demonstrated in [12] which uses a higher-order resonator with multiple stable oscillation frequencies.

2.3.7 Multi-port Coupled-inductor VCOs

In order to cover a wider tuning range in oscillators, multiple coupled inductor has placed inside each other to reduce the area in [13] for a triple-mode oscillator to cover 1 GHz to 6 GHz. Fig. 2.11 illustrates the simple block diagram of the oscillator. There are three differential VCOs

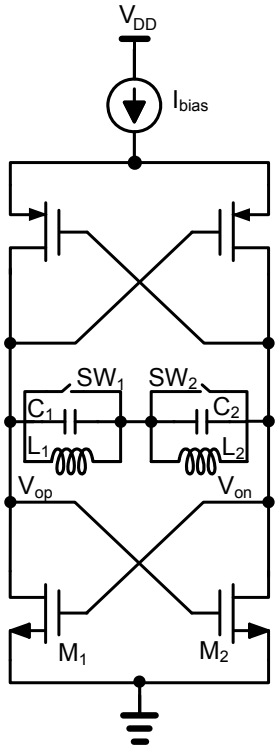

Figure 2.10: A dual-resonance oscillator with cross coupled CMOS active core [12].

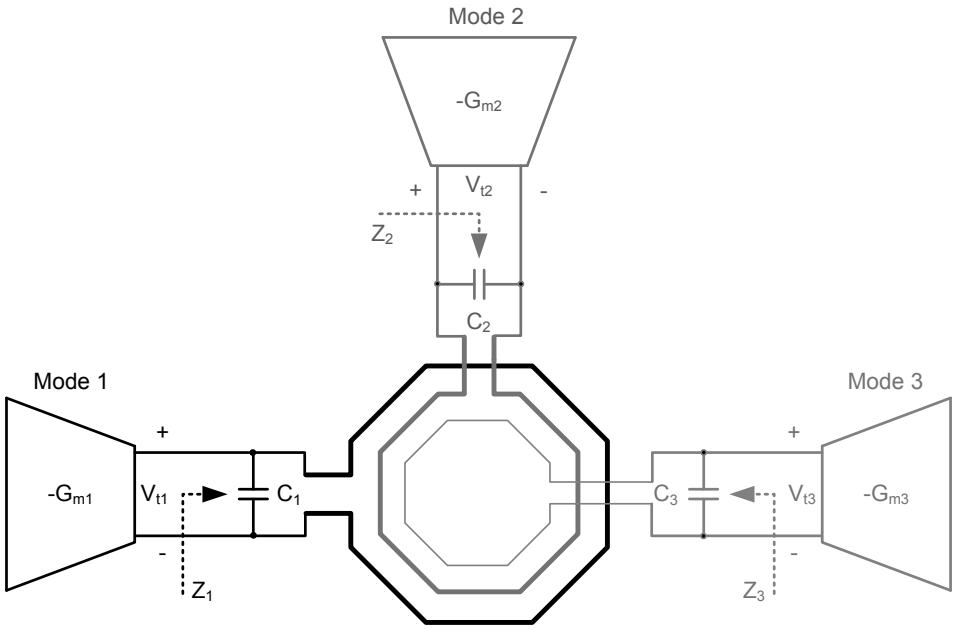

Figure 2.11: Triple-mode oscillator [13].

which have inductors on top of each other to save area.

Fig. 2.12 shows the magnitude of impedances Z_1, Z_2, and Z_3.

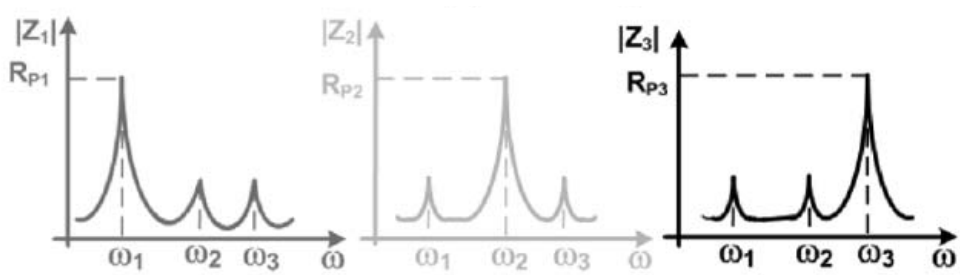

Figure 2.12: The impedance magnitude looking into each port [13].

The frequency band is broken into three complementary bands. The three inductors are placed on top of each other to save the area. The resonance frequencies of the sixth-order

resonator are the roots of

$$\omega^6(k_{12}^2 + k_{23}^2 + k_{31}^2 - 2k_{12}k_{23}k_{31} - 1)$$

$$+\omega^4[\omega_1^2(1 - k_{23}^2 + \omega_2^2(1 - k_{31}^2 + \omega_3^2(1 - k_{12}^2] \tag{2.3}$$

$$-\omega^2[(\omega_1\omega_2)^2 + (\omega_1\omega_3)^2 + (\omega_2\omega_3)^2] \tag{2.4}$$

$$+(\omega_1\omega_2\omega_3)^2 = 0 \tag{2.5}$$

where ω_1, ω_2, and ω_3 are the resonance frequencies of the uncoupled tanks, and $k_{ij}s$ are the coupling factors between ith and jth inductors. The active core at each port of the sixth-order resonator is a standard cross-coupled CMOS differential pair. Therefore, by using three oscillators at three different center frequencies the wideband frequency tuning range has been achieved.

2.4 Wideband Frequency Synthesizers

In order to cover wideband frequencies for multi-standard systems as well as wideband systems, the first option is to design the frequency synthesizers with one broadband VCO. But there are other ways to cover wide frequency range not using broadband VCOs which will be studied here.

2.4.1 Multiple VCOs

It is possible to synthesis wide frequency range by utilizing more than one oscillator [14]. Fig. 2.13 depicts an example of covering frequency range from f_1 to $10f_1$, where four oscillators operating at $5.7f_1$, $16f_1$, $13.3f_1$, and $20f_1$ are used. The fourfold reduction in the maximum oscillation and division frequencies comes at the cost of more complex, yet feasible routing. To generate quadrature phases at $10f_1$, either a $20f_1$ (differential) oscillator or a $10f_1$ quadrature oscillator is necessary. We will cover the quadrature phase generation schemes in following chapters.

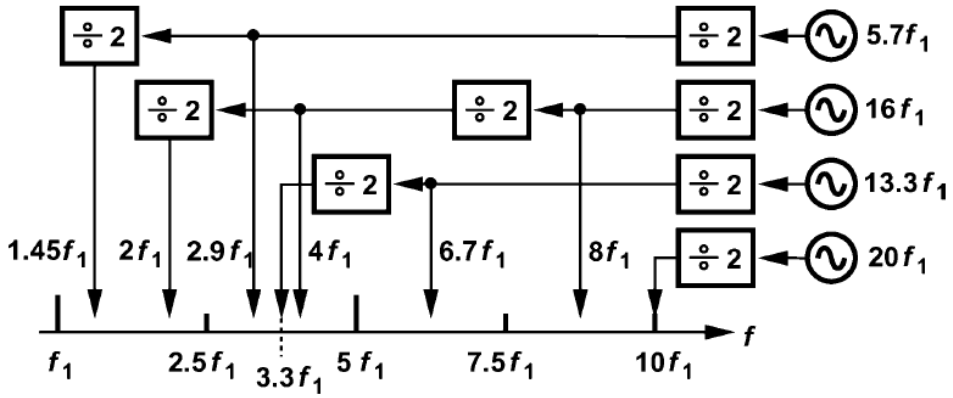

Figure 2.13: Block diagram of wideband synthesis using multiple LOs [14].

2.4.2 Multiple Fixed Frequency PLLs

Multiple PLLs can be used to build a frequency synthesizer for UWB systems. Fig. 2.14 shows the block diagram of a synthesizer using multiple PLLs.

In this type of frequency synthesis there are several PLLs working concurrently, each

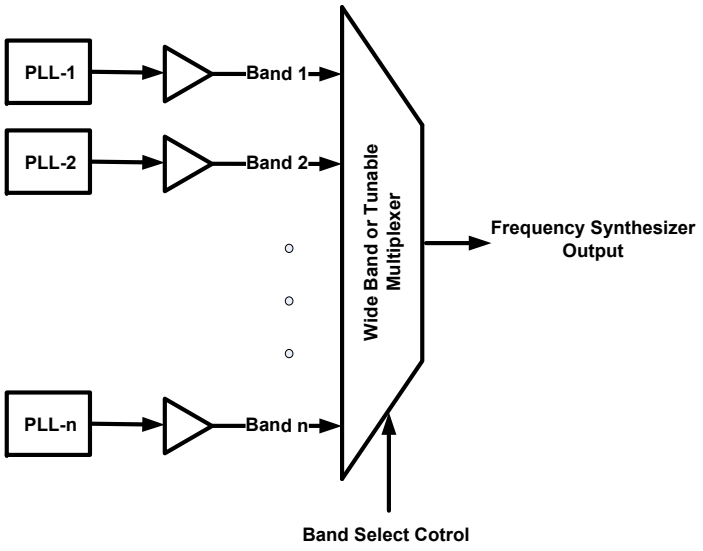

Figure 2.14: Block diagram of a frequency synthesizer using multiple PLLs.

one generating the frequency of one band of interest [37, 14]. A multiplexer (MUX) selects the desired signal and feed it to the next stage. By this way, the hopping time between different channels is only limited to the MUX settling time from one input to another input which is simply around a ns and meets the speed requirement of UWB.

The first drawback of using this synthesizer is the frequency pulling of the PLLs. Increasing the number of desired channels will increase the number of PLLs which will result in a power hungry system. It also increases the area of the chip. Therefore, this type of frequency synthesizer would not be interesting in a multi-band operation.

2.4.3 PLL with Chain of Dividers, Mixers, and Multiplexers

In another way of frequency generation for UWB synthesizer one PLL is followed by dividers, multiplexers, and mixers to generate desired frequencies [15] and [14]. Fig. 2.15 shows the block diagram of one of this type. The novel idea in here is using only one PLL to generate a wideband of frequencies from 3 to $10GHz$.

In this frequency synthesizer the PLL output frequency and its divided versions are combined in mixers to selectively generate desired frequencies. Therefore, there is no need to change the PLL frequency. To save the power consumption the blocks which are not needed in each frequency generation could be turned off. The hopping speed is limited by settling time and turn on time of mixers, dividers, and multiplexers.

The PLL output frequency, f_{PLL}, is $4.224GHz$ which is 16 times the f_o of $264MHz$. After division by two in two dividers the frequencies $8f_o$, $4f_o$, and $2f_o$ are generated. By mixing $8f_o$ and $4f_o$, $12f_o$ is generated. By dividing $12f_o$ by twos the frequencies of $6f_o$ and $3f_o$ are generated. $15f_o$ is generated by mixing $12f_o$ and $3f_o$ which is the center frequency of BG1.

Three bands in BG1 are B1 ($13f_o$), B2 ($15f_o$), and B3 ($17f_o$) which are generated by using a quadrature mixer as following:

$$\begin{aligned} 13f_o &= 15f_o - 2f_o \\ 15f_o &= 15f_o \\ 17f_o &= 15f_o + 2f_o \end{aligned} \tag{2.6}$$

Three Bands in BG2 are generated by shifting BG1 by $6f_o$ in the $4th$ mixer as following:

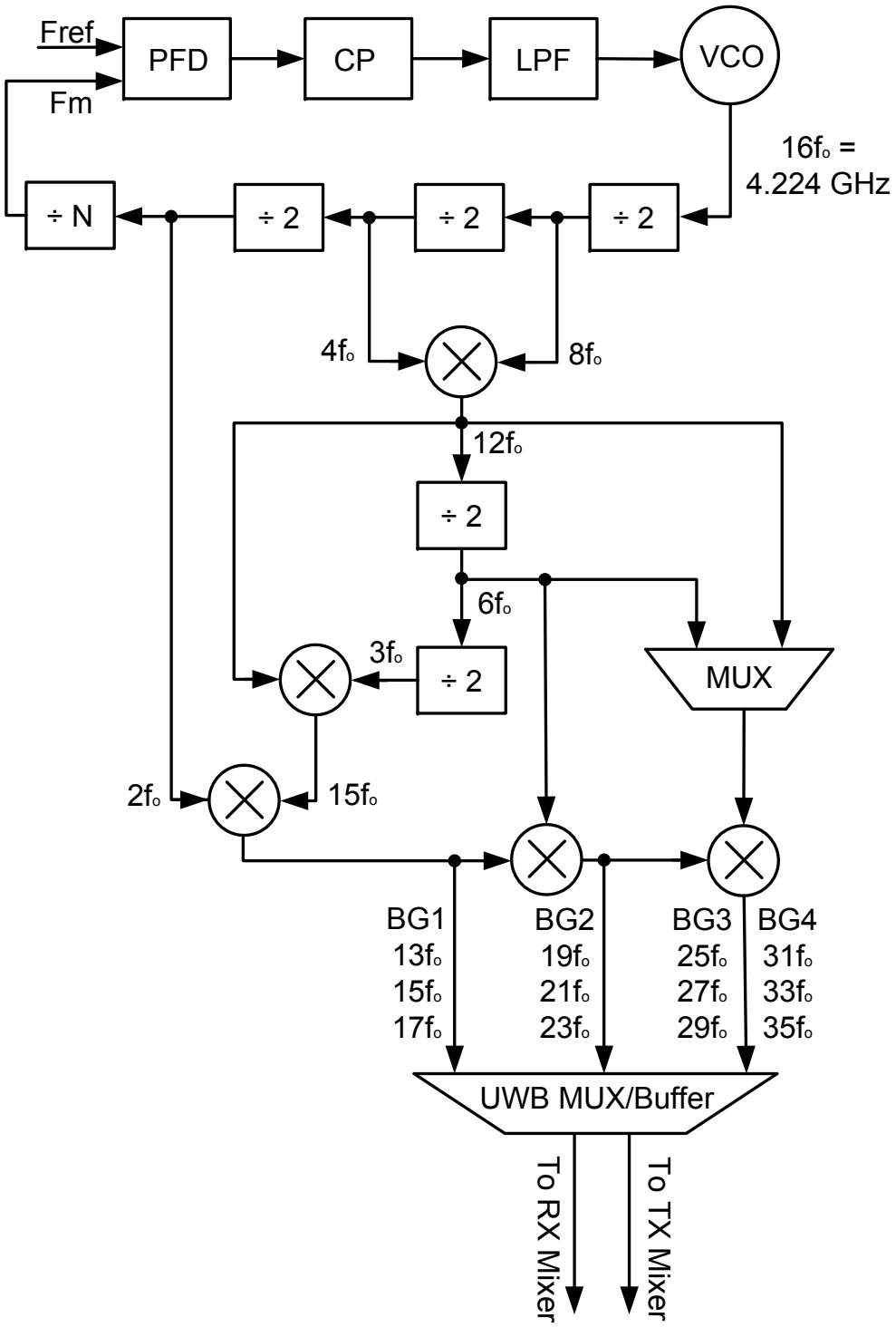

Figure 2.15: Block diagram of a frequency synthesizer with one PLL and chain of dividers, mixers, and multiplexers [15].

$$
\begin{aligned}
19f_o &= 13f_o + 6f_o \\
21f_o &= 15f_o + 6f_o \\
23f_o &= 17f_o + 6f_o
\end{aligned}
\tag{2.7}
$$

BG3 and BG4 are generated by shifting BG2 by $6f_o$ and $12f_o$, respectively. $5th$ Mixer has been used to generate BG3 and BG4.

The main problem with this scheme is using multiple mixers which results in spurious output signal. For example to generate BG3 and BG4 five mixers have been utilized in series. In each mixer, the two inputs generate the desired output. Any mismatch in the mixer's devices and the in-phase (I) and quadrature-phase (Q) of the inputs result in sidebands. Also harmonics of each input will be mixed with other input and harmonics in different ways and create few other unwanted frequencies.

One way to reduce the spurs is to avoid using multiple mixers in series. The frequency synthesizer in [42] requires two PLLs. To generate the center frequencies of band group one it uses only one single SSB mixer while the frequency synthesizer of [**?**] which uses two separate PLLs and one SSB mixer generates seven band center frequencies of MB-OFDM UWB (the old band allocation [43]). The frequency synthesizers which generates the 14-band UWB frequency synthesizers are presented in [44, 45]. In the next section we propose a UWB frequency synthesizer with improved spurious performance. We will go through the detailed of the blocks as well.

2.5 UWB Fast Hopping Frequency Synthesizer with Improved Spurious Performance

In this section we explain the proposed UWB synthesizer which greatly improves the spurious performance. It also meets the requirement of UWB settling time of $9.2\ ns$ between different bands in each BG.

Fig. 2.16 shows the block diagram of the proposed UWB frequency synthesizer ([16]). In this architecture four PLLs have been utilized, two low frequency PLLs (LF PLLs) and two high frequency PLLs (HF PLLs). There are four paths to the output, each path is for one of BG1, BG2, BG3, and BG4 (BG5 and BG6 are generated in the combination of BG3 and BG4) and there is only one mixer in each path. Therefore, the harmonic mixing will happen only in one place and the number of spur frequencies is less than the frequency synthesizer mentioned in previous section. In addition, the inputs to the mixers are quadrature signals and by that the mixing results is only one sideband depending on the input phases. Of course the non-idealities in the input signals (quadrature phase inaccuracy) and mismatch in the devices of the mixer will still result in some unwanted sideband signals, but it is much less than the non-IQ mixers. There are several ways to generate quadrature signals and we chose to use quadrature oscillators which will be discussed in Chapter 3.

In the frequency synthesis each BG is generated by one high frequency PLL and the two low frequency ones (BG5 and BG6 are different). The chain of frequency synthesizer can be divided in two parts, low frequency and high frequency parts. The LF blocks, including dividers, buffers, and multiplexer have low-pass RC load and they are smaller blocks comparing

with HF blocks. The HF blocks have tunable LC load and they are bigger in size and consume more power. Tunable loads in mixers and HF buffers not only help to amplify the signal, but also filter out the unwanted harmonic products (spurs) in the mixers. At the end of the chain there is a combined ultra wideband Mux/Buffer which selects the BGs and drives the TX/RX chain.

The main advantage of this frequency synthesizer over similar type of synthesizers is the frequency planning and selection of PLL frequencies. The PLL frequencies are far from each other and there is no pulling issue. The frequency planning is in a way to use the minimum number of mixers in each frequency path which helps to improve the spurious performance. Also, selection of frequencies to be mixed is in a way to have them equal or bigger than $4f_o$. This selection will result in a spur sideband which is at least $2 \times 4f_o = 8f_o$ far from the main output of the mixer. Therefore, the tunable load can filter out the spur easier. Having one path for each BG enables us to have sharp tunable loads to remove the spurs.

Four PLLs have been used in this frequency synthesizer. LF PLLs are $6f_o = 1.584GHz$ and $8f_o = 2.112GHz$ and HF PLLs are $21f_o = 5.544GHz$ and $27f_o = 7.128GHz$. All PLLs use the same reference frequency of a $40MHz$ temperature controlled crystal oscillator (TCXO). The block diagram of PLLs are shown if Fig. 2.1. The VCO is a series coupled quadrature oscillator (QOSC) which will be explained in detail in the next chapter. In general PLLs are the source inputs of the UWB frequency synthesizer.

In each BG one HF PLL and two LF PLLs are operational and this may cause pulling problem, however since center frequencies are far it is not be a big concern. The root cause of pulling is the signal injection from one PLL to the other, and since the sources of coupling are

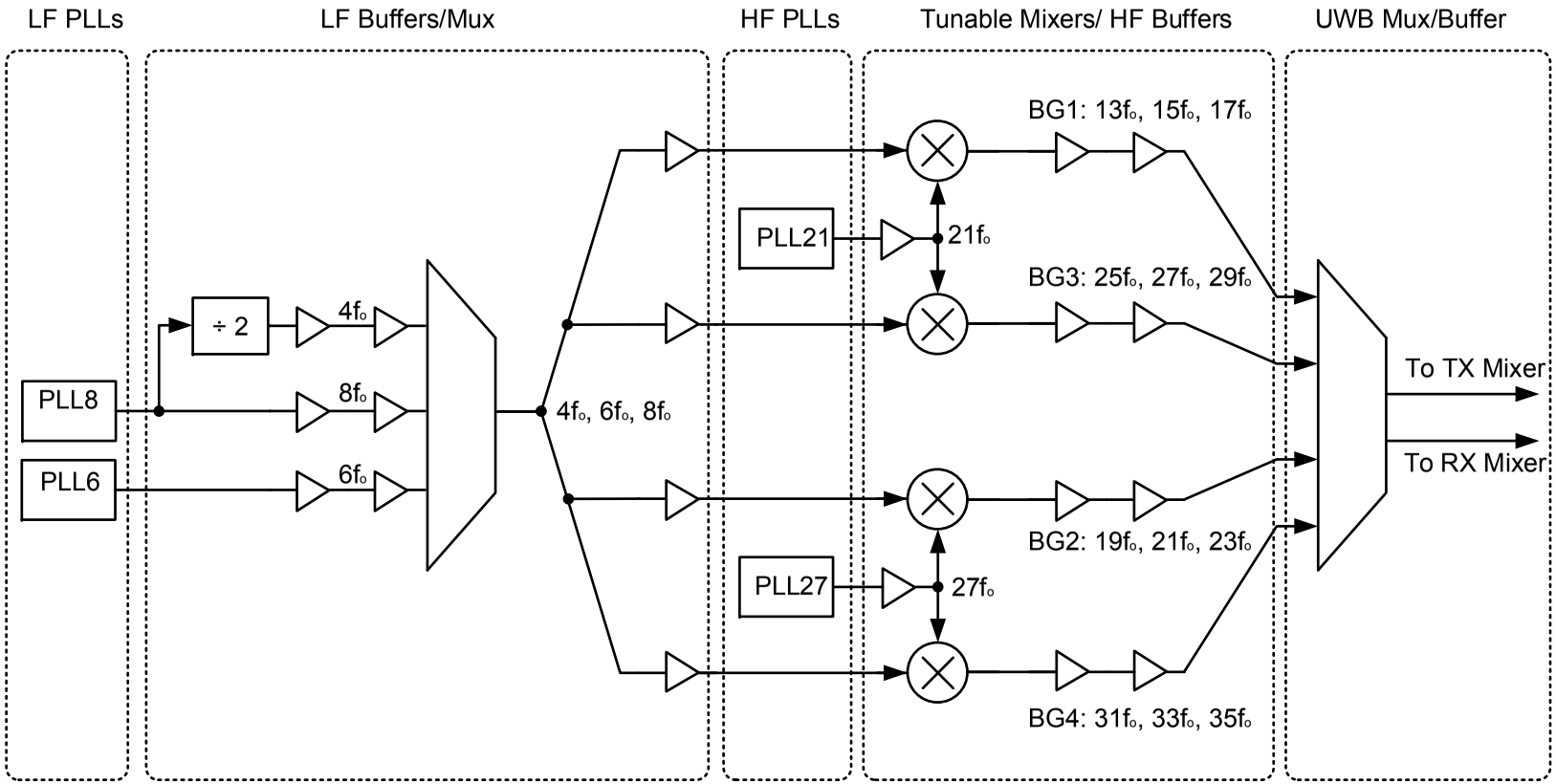

Figure 2.16: Block diagram of proposed frequency synthesizer [16].

not easily predictable the conservative design to minimize the coupling between different PLLs is good enough to prevent the pulling.

2.6 Summary

In this chapter we studied several frequency synthesizers for UWB systems. The main requirement is the ability to settle in less than 9.2 ns for a fast hopping UWN synthesizer. Therefore, the conventional PLLs cannot be utilized as the synthesizer for UWB systems because of the slow settling of few μs. A fast hopping frequency synthesizer was also reviewed, which shows an improved spurious performance. To use this design as a universal 14 band UWB fast hopping frequency synthesizer, there is a need to have wide tuning range quadrature oscillators which will be discussed in next chapters.

Chapter 3

Quadrature Signal Generation Methods

Quadrature signal generation in modern image-reject transceivers is an essential task [46]. In the receiver mixer by using quadrature LO signal, only the desired signal frequency gets down-converted and the image signal gets rejected. In transmitter the quadrature LO signals is essential to only up-convert the desired frequencies and transmit less spurs. In the UWB frequency synthesizer mentioned in Chapter 1 also quadrature signals are used to synthesis the desired LO frequencies for RX/TX chain with less spurs. Therefore, the input and outputs of the mixers in frequency synthesizer are quadrature signals. In this chapter different methods of quadrature signal generation will be reviewed with the advantages and disadvantages of each method. Then we explain the method that we have used in the design of UWB frequency synthesizer.

3.1 Divider by Two

One of the most common ways of quadrature signal generation is using a differential oscillator followed by a divide-by-two circuit [47]. In Fig. 3.1 the frequency of the differential oscillator is $f_{osc} = 2f_{LO}$ and the desired frequency of the quadrature signal is f_{LO}.

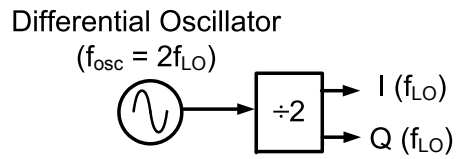

Figure 3.1: Using a differential oscillator followed by a divider-by-two to generate quadrature signal.

The quadrature signal generated by this method is inherently very accurate. This way of quadrature LO generation also eliminates the problem of $pulling$ of oscillator by strong transmitter coupling because the transmitted signal is at f_{LO} while oscillator is oscillating at $f_{osc} = 2f_{LO}$.

This method of quadrature signal generation requires high power consumption; oscillator operates at $2f_{LO}$, and may not be practical at higher frequencies such as millimeter-wave applications. It also needs high frequency dividers which are power hungry.

3.2 Poly-phase Filters

An alternative method to generate quadrature signal is to use a differential oscillator at the desired frequency, $f_{osc} = f_{LO}$, followed by a polyphase filter [48]. Beside the simplicity of the method, the positive point is that the oscillator doesn't need to operate at twice the required

frequency, therefore, power consumption of the oscillator is less, but buffers should be utilized after the oscillator to drive the polyphase filter which adds to the power consumption. Fig. 3.2 shows the schematic of a one stage polyphase filter.

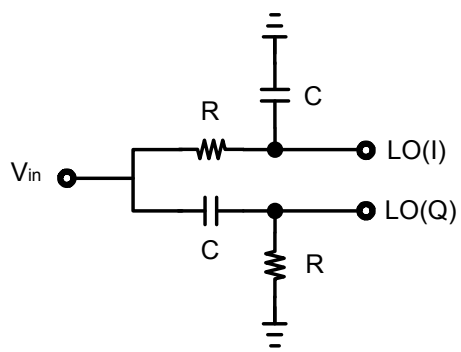

Figure 3.2: Schematic of a polyphase filter to generate quadrature signal out of differential input.

The main problem with this method of quadrature signal generation is the amplitude mismatch and the narrow bandwidth. The polyphase filter has matched IQ amplitude only in one single frequency and by moving from the center frequency ($\omega = \frac{1}{RC}$) the amplitude matching gets degraded. By cascading multiple stages of $RC - CR$ networks the IQ amplitude matching can be improved at the cost of extra loss. Even at the center frequency of ω the quadrature accuracy is a function of RC matching which results in low quadrature accuracy. Therefore, it is not the suitable choice for us.

3.3 Quadrature Ring Oscillators

Ring oscillators are the other option to directly generate quadrature signal with high accuracy [49, 50, 51]. Fig. 3.3 shows the block diagram of an inverter based quadrature ring

oscillator which four differential inverting stages. The number of inverting stages in a ring should be odd or the differential inverting stages should be utilized to get the oscillation condition.

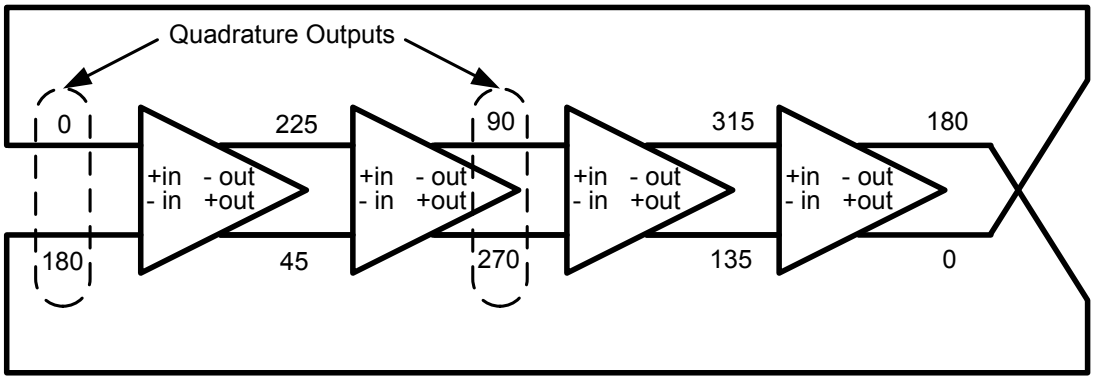

Figure 3.3: Block diagram of an inverter based quadrature ring oscillator.

Although the quadrature phase accuracy is good and it is a compact solution, this method of quadrature oscillation suffers from unacceptable phase noise for many high-frequency applications. Therefore, this method is not acceptable for quadrature signal generation in UWB frequency synthesizer.

3.4 LC Quadrature Oscillators (LC-QOSCs)

LC quadrature oscillators (LC-QOSCs) can also directly generate the quadrature signals. The phase noise performance of LC-QOSCs is much better than inverter based ring oscillators and is preferred for high-frequency and low phase noise applications. [52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63]. Unlike the method of using divide-by-two, in this method the oscillator operates at the desired frequency (not twice the frequency) and, therefore, there is no need for a

high frequency dividers or extra buffering.

To compensate for process, voltage, and temperature (PVT) variations, a wide tuning range is essential for high-frequency LC-QOSCs. In addition to PVT variations, increasing in the multiband and software defined radios ($SDRs$) aggravates the requirements for the tuning range. Replacing multiple narrow-band oscillators by a wide tuning range oscillator in $SDRs$ results in saving the chip area.

The LC-QOSCs are constructed of two differential oscillators coupled through the coupling mechanism. In this section we review two different LC-QOSCs and explain their limitations.

3.4.1 Parallel Coupled LC Quadrature Oscillators ($P - QOSC$s)

The common topology of LC-QOSCs is shown in Fig. 3.4 which is referred to as a Parallel Quadrature Oscillator ($P - QOSC$) [52]. In P-QOSCs the coupling mechanism includes $MOSFET$ devices (M5-M8) which are in parallel with the cross coupled devices (M1-M4).

To reduce the phase noise, Tang *et al.* proposed a phase shift in the coupling path of quadrature oscillator of Fig. 3.4. By this phase shift the phase noise can be optimized by maximizing the quality factor of the tank at resonance [53]. Fig. 3.5 shows the block diagram of the quadrature oscillator with the inserted phase shift in the coupling path.

The peak quality factor of an N-stage LC oscillator (Q_N) is a function of the inserted phase shift at the oscillation frequency(Φ_{res}) and the peak quality factor of the resonator (Q_p):

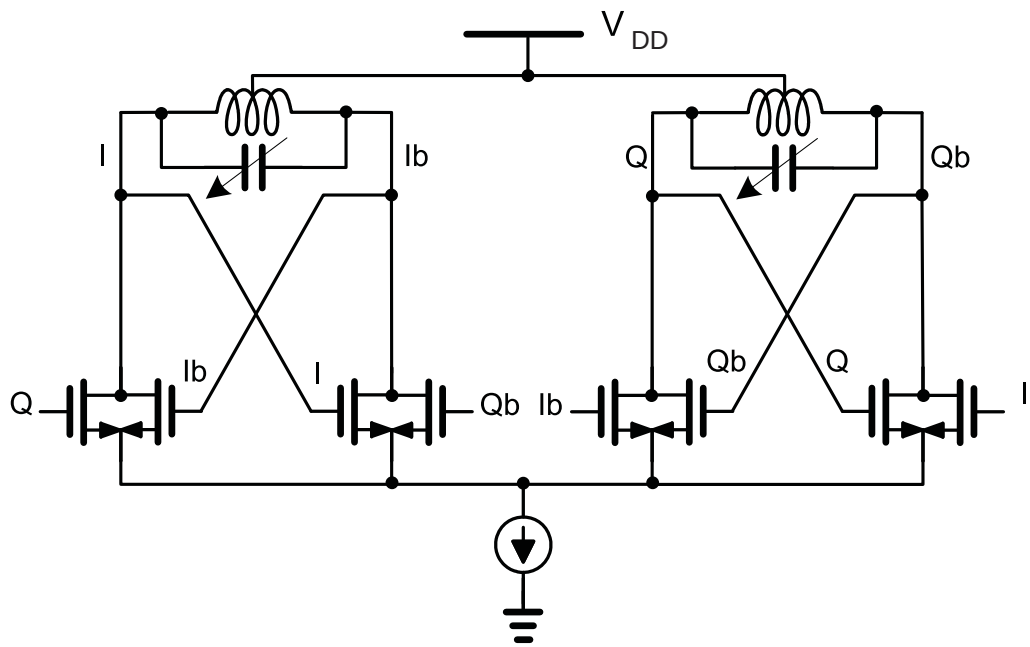

Figure 3.4: Parallel coupled quadrature oscillator (P-QOSC).

$$Q_N(\Phi_{res}) \approx NQ_p cos(\Phi_{res}) \tag{3.1}$$

which for the two-stage quadrature oscillator of Fig. 3.5 can be simplified as:

$$Q(\Phi_{res}) \approx 2Q_p cos(\Phi_{res}) \tag{3.2}$$

The maximum value of $Q(\Phi_{res})$ in (3.2) occurs when Φ_{res} is zero. Therefore, adding a phase shift of $\pm 90°$ to the coupling path optimizes the oscillator Q and, as a result, the phase noise of oscillator will be optimized.

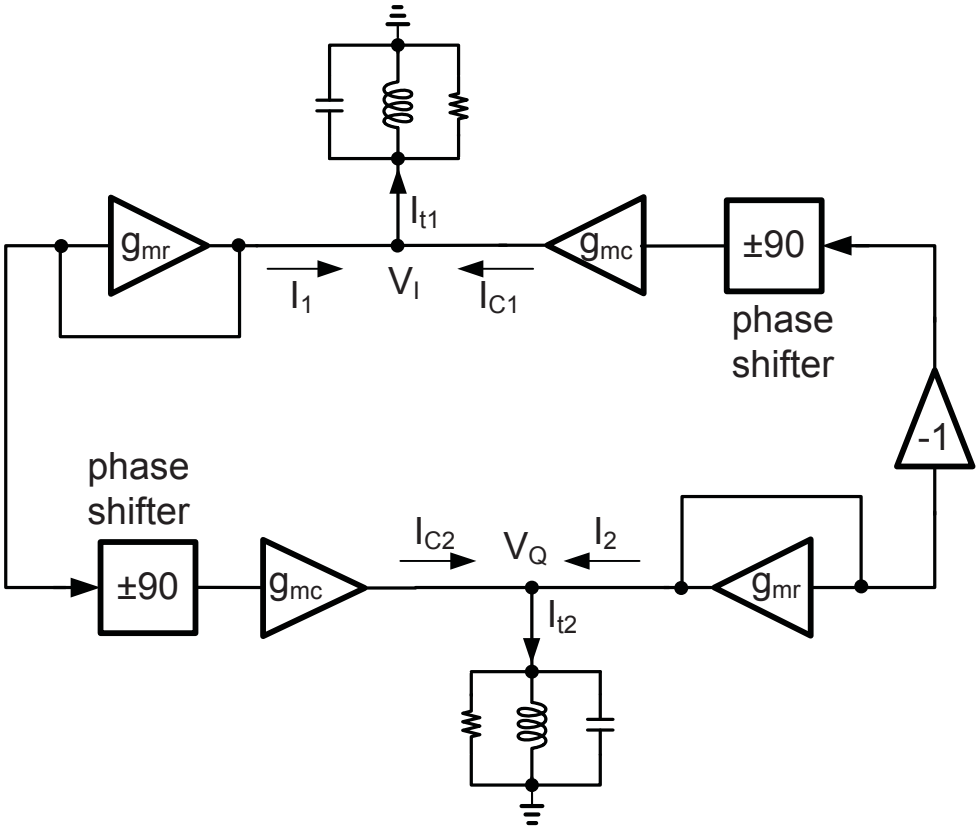

Figure 3.5: Reduced phase noise QOSC.

3.4.2 Series Coupled LC Quadrature Oscillators ($S - QOSC$s)

There is a trade-off between phase noise and quadrature phase accuracy in P-QOSCs, *i. e.* increasing the coupling strength improves the quadrature phase accuracy but worsen the phase noise [54]. Andreani $et\ al.$ proposed the series coupled quadrature oscillators (S-QOSCs), shown in Fig. 3.6, and concluded that there is an improved trade-off between phase noise and quadrature phase accuracy in S-QOSCs as opposed to P-QOSCs [54].

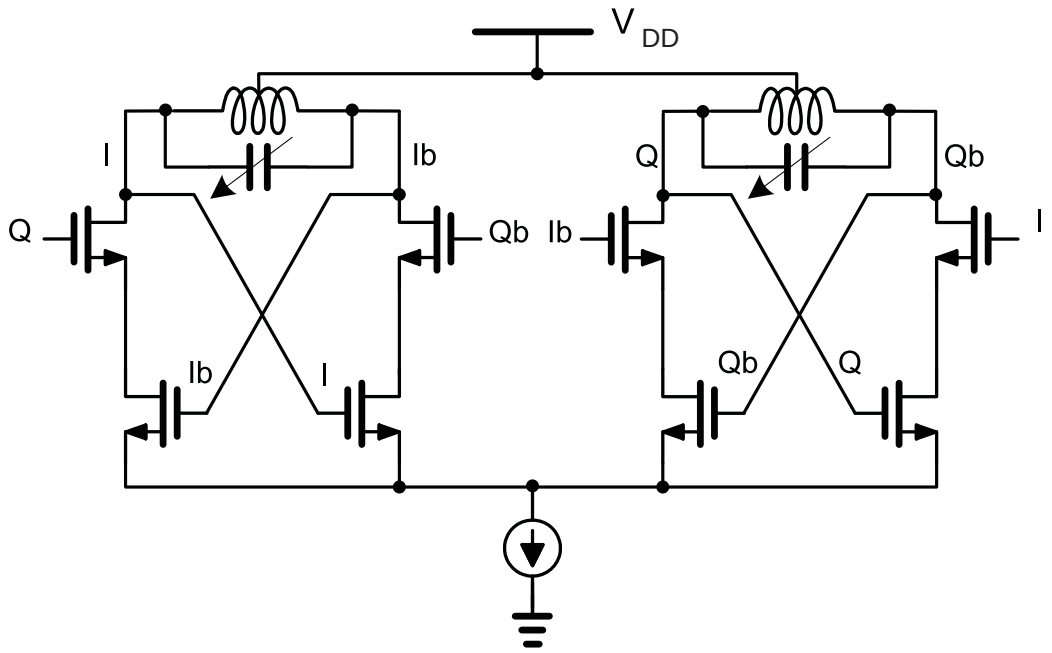

Figure 3.6: Series coupled quadrature oscillator (S-QOSC).

In this type of quadrature oscillators the coupling devices are in series with regenerative devices. The main advantage of this type of oscillator is the reduction of added noise from the coupling devices which results in improved phase noise performance. The coupling devices are in series with the cross-coupled pair, therefore, the noise of coupling devices gets rejected.

In the next section we explain the quadrature phase ambiguity in LC-QOSCs which results in some problems in the system. Then we review some solutions including our solution with S-QOSCs.

3.5 Phase Ambiguity in LC-QOSCs; Problems and Solutions

Series and parallel LC quadrature oscillators suffer from quadrature phase ambiguity; they can oscillate in more than one stable mode of oscillation (I leading Q or Q leading I) which make them ill-suited for practical designs. Fig. 3.7 shows the waveform of two stable mode of quadrature oscillation. It has been shown by Mirzaei [56] that there are several modes of oscillation in a traditional QOSC which two of these modes are stable and under a perturbation will maintain their oscillation. Among these stable modes one mode will dominate. There are also two unstable modes which under perturbation will disperse [56].

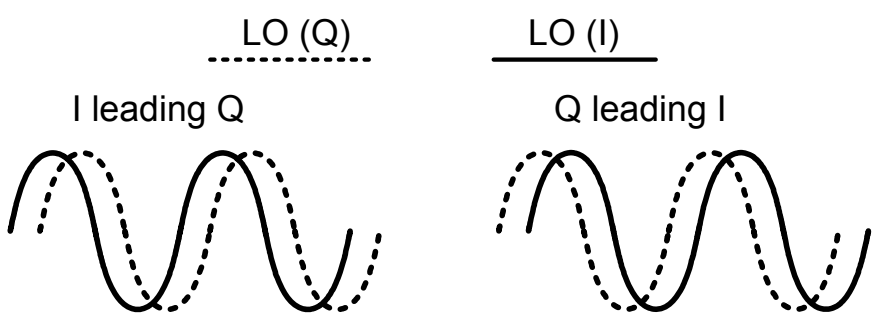

Figure 3.7: Ambiguity in phase of quadrature oscillation, I (solid line) leading Q (dashed line) (a) and Q leading I (b).

The first problem arises from the different quadrature phase of the outputs. If the wrong sequence of LO signal drives an IQ RX-mixer, the result would be up-conversion instead of

down-conversion. Also in the PLL if the wrong sequence of quadrature drives the feedback divider, the divider might fail to divide and the PLL fails to lock.

The existence of more than one stable mode of oscillation introduces more substantial problems for quadrature oscillators [64]. The frequency range of oscillation in one stable mode of quadrature oscillation differs from other modes. Fig. 3.8 shows a possible frequency range of the two modes of quadrature oscillation and their hypothetical tuning ranges. The effective tuning range of the QOSC is only a small range of overlap of the two tuning ranges. This overlap might get smaller or zero in the case of $\omega_{max,2} < \omega_{min,1}$.

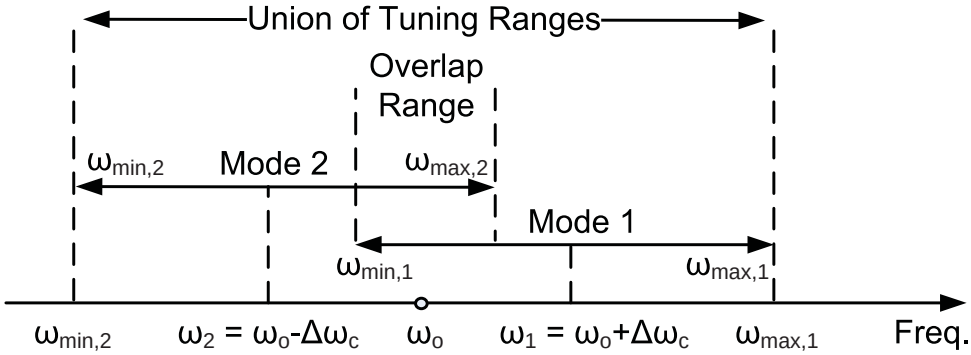

Figure 3.8: Frequency and tuning range of two different quadrature modes of oscillation of a typical QOSC.

Fig. 3.9 shows the simulation result of the tuning range of two modes of QOSC. It can be seen that the tuning range is effectively zero as there is no overlap of tuning ranges.

Therefore, there is a need to solve these problems before utilizing the LC-QOSCs in the practical applications. In here we review some solutions to fix these problems in different ways, partially or completely.

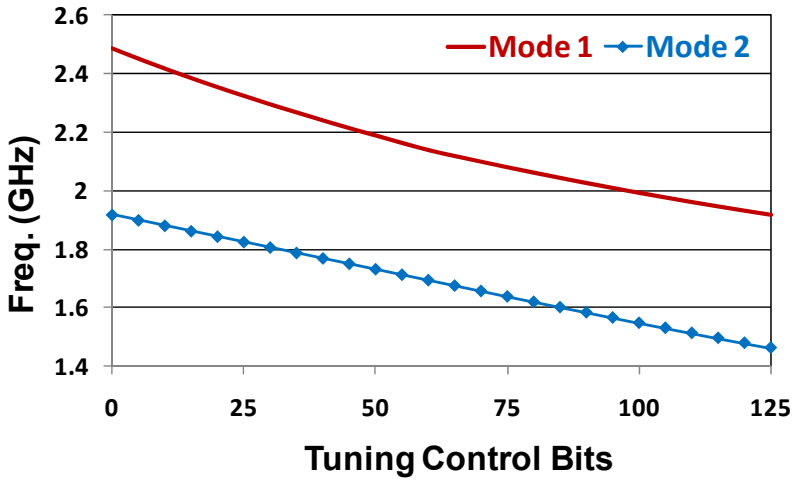

Figure 3.9: Simulation results of tuning range of two modes of QOSC. The effective tuning range iz zero.

3.5.1 Post-VCO Phase Correction

To resolve the quadrature phase (sequence) ambiguity, one can use the post-VCO correction technique in [65]. In this method, a phase detector is used to detect the output sequence of the QOSC shown in Fig. 3.10. The output of the QO drives the multiplexer and, if the sequence is incorrect, the multiplexer switches the outputs to the correct sequence at the output.

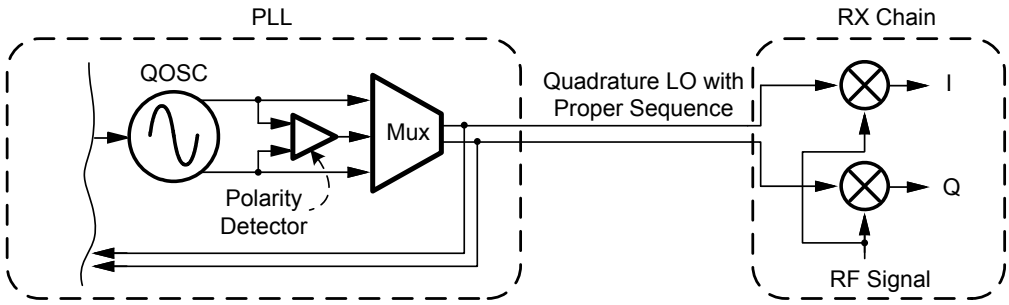

Figure 3.10: QOSC post-VCO phase correction.

By this solution the quadrature phase will be defined and the mixer problem will be vanished. But still the effective tuning range of the QOSC is limited by the small range of the overlap range, therefore, other solutions are needed.

3.5.2 Phase Shifter in QOSCs

The phase shifter that Tang $et\ al.$ [53] introduced in the coupling path to reduce the phase noise (Fig. 3.5) also forces the QOSC to oscillate in only one quadrature mode of oscillation. Heidari [57] has shown how the added phase shift helps to insure only one mode of quadrature oscillation in P-QOSCs. A vector diagram of the voltages and the currents of the circuit of Fig. 3.5 has been shown in Fig. 3.11, where I_1 and I_2 are the regenerative currents going to Tank 1 and 2, respectively. I_{C1} is the coupling current going to Tank 1, and I_{t1} is the total current (summation of I_1 and I_{C1}) going to Tank 1. If the phase shifter $\phi = 0$ as in Fig. 3.11, then I_{t1} for Modes 1 and 2 have equal magnitude and either quadrature mode is possible.

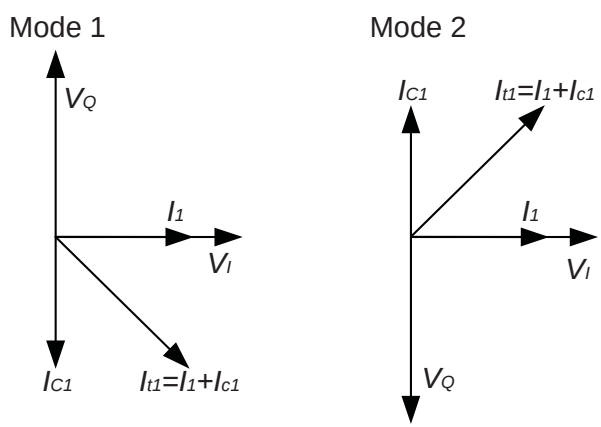

Figure 3.11: Two possible modes of quadrature oscillation for $\phi = 0$. From Fig. 3.5 either mode of oscillation (determined by the magnitude of I_{t1}) is possible.

Fig. 3.12 shows the two possible modes of quadrature oscillation after adding a phase shift to the coupling path. By adding this phase shift (ϕ), I_{t1} in Mode 1 decreases while I_{t1} of Mode 2 increases. Therefore, Mode 2 will be the dominant mode of quadrature oscillation.

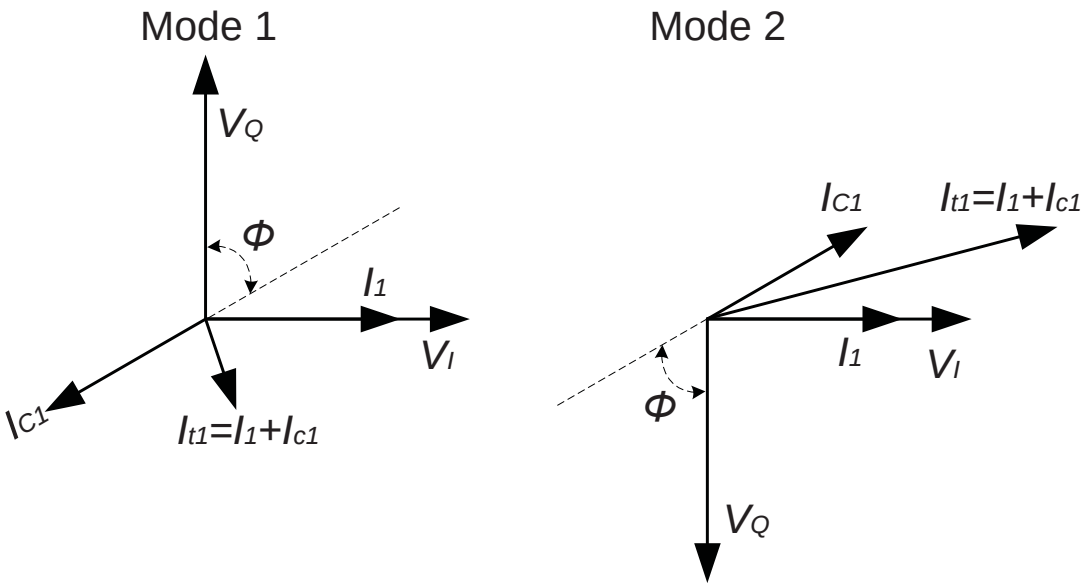

Figure 3.12: Two possible modes of quadrature oscillation (determined by I_{t1} in Fig. 3.5) for $\phi > 0$. In this case, Mode 2 dominates.

Nonetheless, adding the phase shifter complicates the circuit and makes it difficult to implement at higher frequency. With this background, in next chapter we propose a circuit technique that produces a deterministic *LC*-QOSC without the complication and additional noise of a separate phase shifter.

3.6 Summary

In this chapter we studied different techniques of quadrature signal generation. In first study, the main method of quadrature signal generation which is using a differential oscillator

followed by a divider by 2, suffers from power consumption at higher frequencies. Poly-phase filters can generate the quadrature signal at a very limited frequency range and suffer from the mismatch in I and Q channels. Ring oscillators can also generate quadrature signals with good quadrature accuracy, but they suffer from poor phase noise. Finally, LC quadrature oscillators have very good phase accuracy and phase noise performance and are our choice to be used in the frequency synthesizer of previous chapter.

In this chapter we also studied the problems of C quadrature oscillators. We showed that conventional LC quadrature oscillators may operate at several modes which two of them are stable modes of quadrature oscillation, and therefore, the output quadrature phase of them is random, therefore, they cannot drive quadrature mixers properly unless the random sequence is fixed. The frequency ranges of these two stable modes are different and as a result, the effective tuning range of LC quadrature oscillators reduces and may cause some problems in PLL locking. We studied the solution for random phase of quadrature oscillators.

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Chapter 4

Wideband Series Coupled LC Quadrature Oscillators with Deterministic Output Sequence

In Chapter (3) we reviewed the different ways of quadrature signal generation. Using differential oscillator, at twice frequency of the required frequency, followed by a divider by two is the most common way of quadrature generation which suffers from higher frequency operation of oscillator and divider. Using polyphase filter after a differential oscillator is another method which suffers from high loss in RC filter and quadrature accuracy degradation because of mismatch in components. It also generates matched quadrature amplitude only in the center frequency. Quadrature ring oscillators show poor phase noise performance and are not suitable for high-frequency applications. LC quadrature oscillators meet the requirement of phase noise, tuning range, and quadrature phase accuracy. We reviewed the two common topologies

of LC-QOSCs, parallel coupled and series coupled QOSCs which both suffer from quadrature phase (sequence) ambiguity that need to be fixed to be applicable in practical designs. Then we reviewed different solutions to solve this problem. Post-VCO phase correction method could solve the problem in part while adding phase shifter in the coupling path helps the oscillation to happen in only one mode plus improving phase noise of QOSC. In practice this technique is complex to be utilized in high frequency signal generation.

In this chapter we propose a series coupled QOSC with deterministic output sequence which is simple in design. It solves the problem of sequence ambiguity while keep the tuning range acceptable. Then we do some linear analysis to show how this technique helps to have only one dominant mode of quadrature oscillation. With the understanding of the technique and linear analysis, we propose the modified S-QOSC which can selectively operate in both stable modes of quadrature oscillation. By this design we can improve the tuning range of the QOSC which is suitable for applications such as SDRs, multi-band radios, and UWB systems.

4.1 Deterministic Mode S-QOSC

Fig. 4.1 shows the schematic of an S-QOSC. In this circuit the addition of C_4 forces the oscillator into one preferred mode of quadrature oscillation [64].

To explain geometrically how one mode of quadrature oscillation dominates the other in Fig. 4.1, we use the S-QOSC small-signal model shown in Fig. 4.2.

In this case $V_Q = \pm jV_I$ represents the two possible modes of quadrature oscillation. The

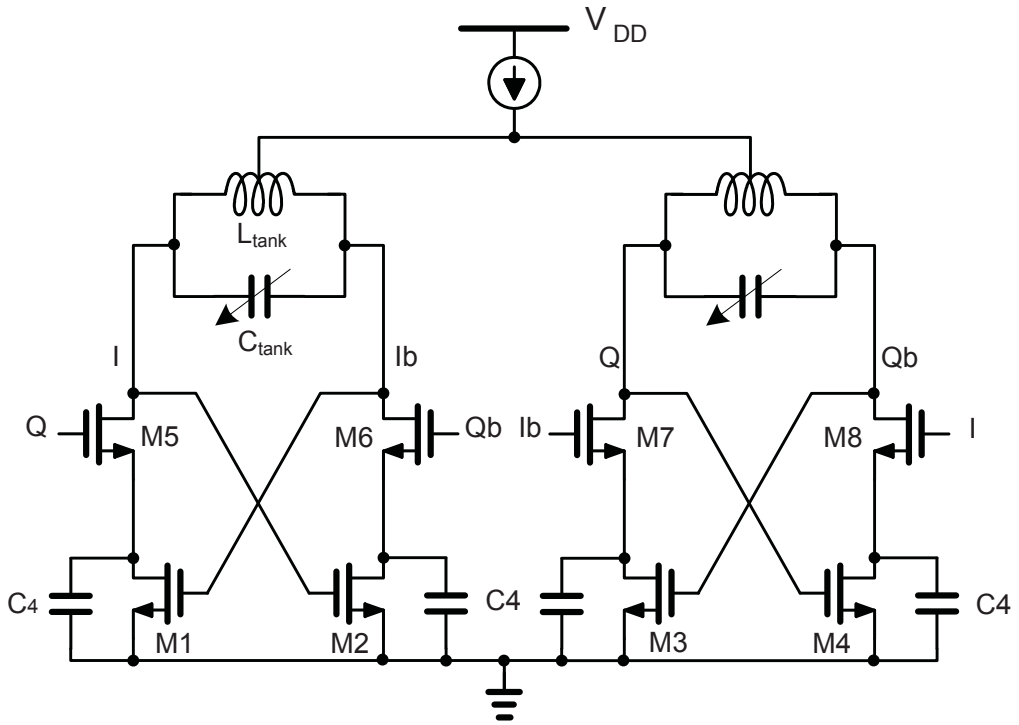

Figure 4.1: Series Quadrature Oscillator with deterministic output sequence.

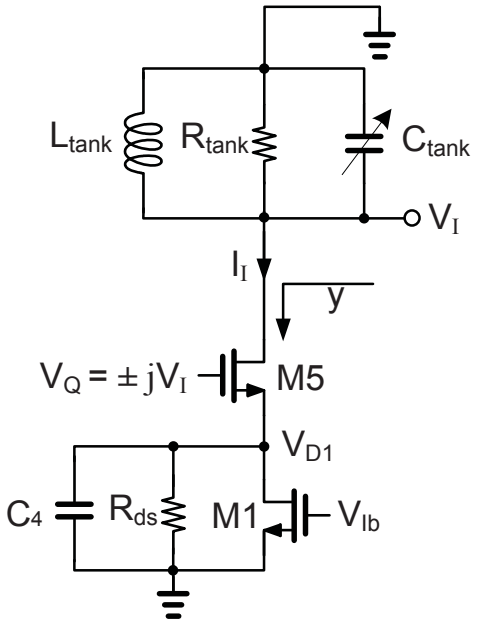

Figure 4.2: Small-signal model of quarter-circuit of the modified S-QOSC.

choice of $-jV_I$ represents Mode 1 (*I* leading *Q*) and $+jV_I$ represents Mode 2 (*Q* leading *I*). In this case,

$$V_{D1} = \frac{|V_I|}{(g_{m5} + g_{ds})^2 + (\omega C_4)^2}(jA + B) \tag{4.1}$$

where

$$A = \pm g_{m5}(g_{m5} + g_{ds}) - g_{m1}\omega C_4$$

$$B = g_{m1}(g_{m5} + g_{ds}) \pm g_{m5}\omega C_4 \tag{4.2}$$

In this analysis we have assumed that $g_{ds,M5} = 0$. In the case where C_4 is zero, V_{D1} becomes

$$V_{D1} = \frac{(\pm j g_{m5}(g_{m5}+g_{ds})+g_{m1}(g_{m5}+g_{ds}))}{(g_{m5}+g_{ds})^2}\,|V_I| \tag{4.3}$$

In (4.3), the real portions of V_{D1} are equal, while the imaginary parts have opposite signs. Fig. 4.3 shows the phasor diagram from Fig. 4.2 based on (4.3). $V_Q = +jV_I$ is for Mode 2 (+j coupling), while $V_Q = -jV_I$ is for Mode 1 (-j coupling). θ_1 and θ_2 are the phase differences between the voltage and current of the tank for Mode 1 and Mode 2 respectively.

As shown in Fig. 4.3 for the case of $C_4 = 0$, $-I_I$ (the tank current) for Modes 1 and 2 are equal and $|\theta_1| = |\theta_2|$. To satisfy the oscillation condition, the tank impedances must have a phase θ_1 and θ_2 for Modes 1 and 2, respectively, therefore, the oscillation frequency occurs

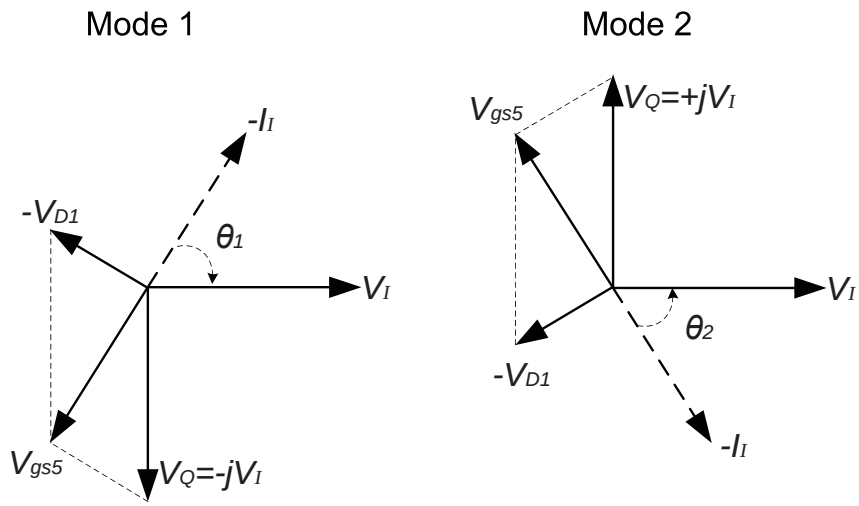

Figure 4.3: Phasor diagram of the voltages for Fig. 4.1 ($C_4 = 0$). Either mode is equally probable. V_{gs5} determines the amplitude of oscillation.

slightly off the resonance frequency of the LC tank. Fig. 4.4 shows the phase and magnitude of the tank impedance as a function of frequency when C_4 is zero. It is clear that when $|\theta_1|$ is equal to $|\theta_2|$ the magnitude of tank impedance for the two modes is the same. Therefore, the two modes of quadrature oscillation are equally likely.

From (4.1), we see that by increasing C_4, the real and imaginary portions of $-V_{D1}$ will change and $-V_{D1}$ will rotate clockwise as shown in Fig. 4.5. In this case, V_{gs5} in Mode 2 is much larger than V_{gs5} in Mode 1, and $|\theta_1|$ and $|\theta_2|$ are not equal. Fig. 4.6 shows the phase and magnitude of the tank impedance for these two modes, where Mode 2 dominates the quadrature oscillation.

4.1.1 Linear Analysis

From [**?**], the real part of the admittance looking into the drain of M5 in Fig. 4.2 is

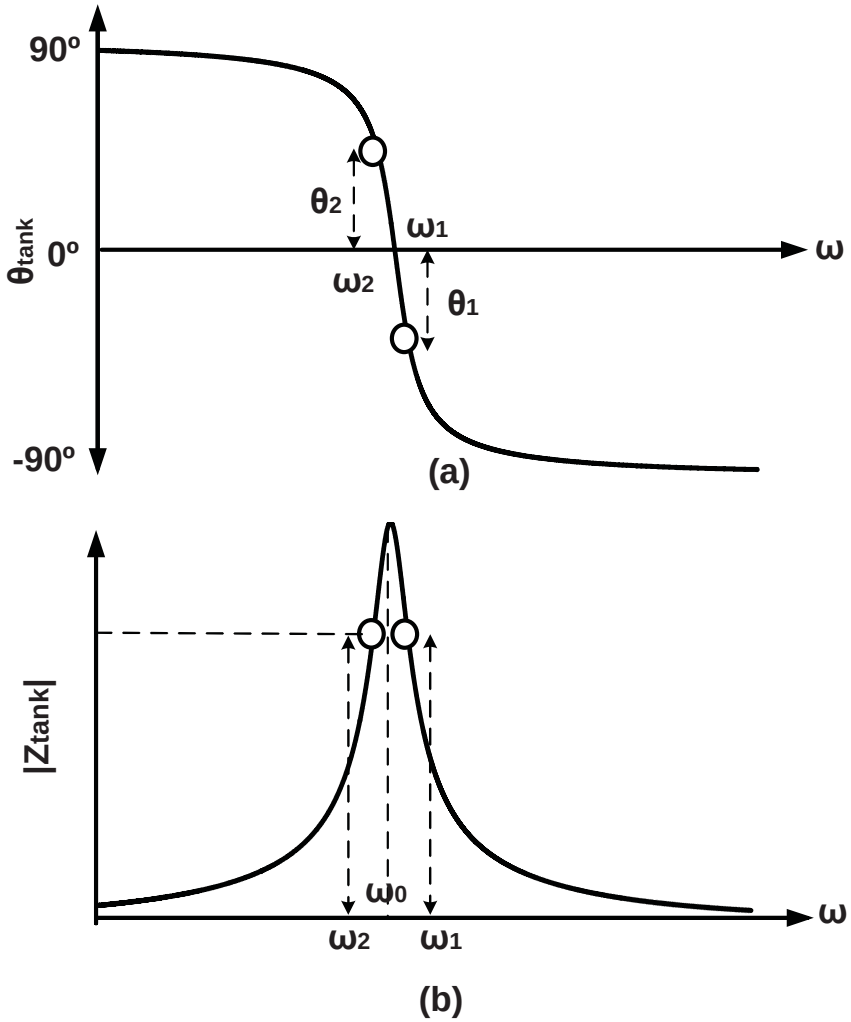

Figure 4.4: Phase (a) and magnitude (b) of *LC* tank impedance as a function of frequency for two different modes of quadrature oscillation, $C_4 = 0$ and $|\theta_1| = |\theta_2|$.

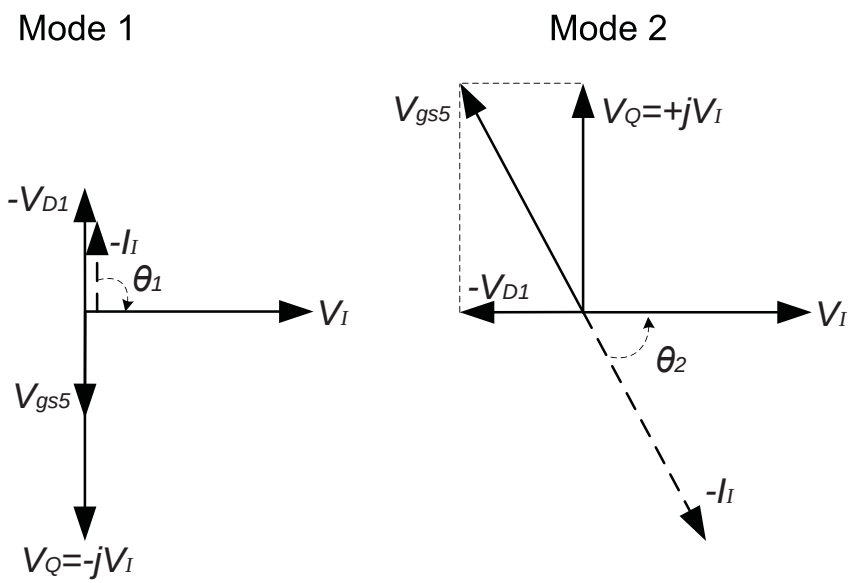

Figure 4.5: Phasor diagram of the voltages for Fig. 4.1 when $C_4 > 0$ and $|\theta_1| > |\theta_2|$. V_{gs5} determines the amplitude of oscillation.

$$g_{d5}(\omega) = -\frac{g_{m5}r_{ds}[g_{m1}(1+g_{m5}r_{ds}) \pm g_{m5}r_{ds}\omega C_4]}{(1+g_{m5}r_{ds})^2 + (r_{ds}\omega C_4)^2} \tag{4.4}$$

Hence, the start-up condition of oscillation is

$$g_{m1} + \frac{g_{m1}}{g_{m5}r_{ds}} \pm \omega C_4 > \frac{(1+\frac{1}{g_{m5}r_{ds}})^2 + (\omega C_4/g_{m5})^2}{R_{tank}} \tag{4.5}$$

If C_4 is zero, (4.5) confirms that the start-up condition for both modes is the same and, therefore, both are equally probable. In [64] we showed that for only one mode of quadrature oscillation, C_4 should be greater than a minimum value ($C_{4,min}$). For $C_4 < C_{4,min}$, both modes of quadrature oscillation have the condition to start, but for $C_4 > C_{4,min}$, only Mode 2 is possible.

With a sufficiently large value of C_4, we can prevent a start-up condition in mode 1. At this point we can say that the QOSC has only one quadrature mode. At higher values of C_4, mode 2 will also lose its start-up condition and none of the quadrature modes will exist. By

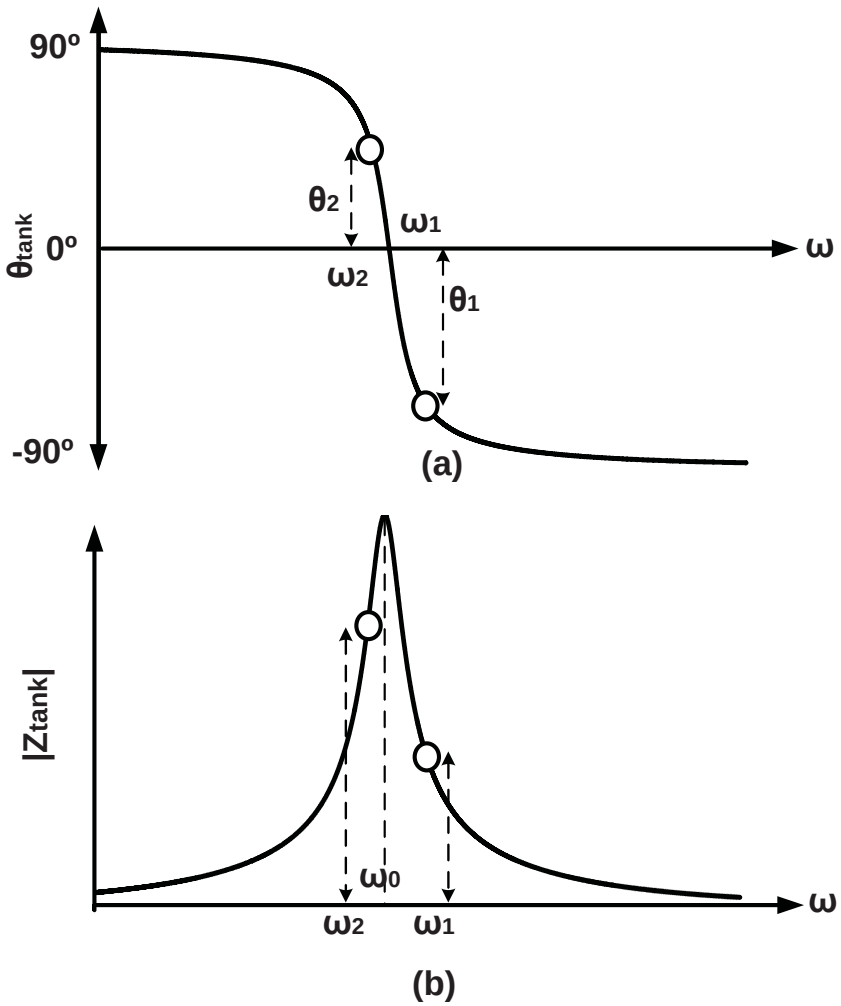

Figure 4.6: Phase (a) and magnitude (b) of *LC* tank impedance as a function of frequency for two different modes of quadrature oscillation, $C_4 > 0$. In this case Mode 2 dominates.

solving (4.5) the upper limit of C_4 for either of the two quadrature modes is:

$$C_{max} = \frac{\pm {g_{m5}}^2 R_{tank} + g_{m5}\sqrt{\Delta}}{2\omega} \tag{4.6}$$

where:

$$\Delta = \frac{({g_{m5}}^2 r_{ds} R_{tank})^2 - 4(1 + g_{m5} r_{ds})(1 + g_{m5} r_{ds} - g_{m1} g_{m5} r_{ds} R_{tank})}{(g_{m5} r_{ds})^2} \tag{4.7}$$

By further increasing C_4, the QOSC will operate in a differential (non-quadrature) mode. A large C_4 bypasses transistor M1, and branches I and Ib in Fig. 4.1 will be in phase and 180° apart from the common signals Q and Qb. In this differential mode, transistor M5 will operate as the regenerative device.

Doing the same analysis for the start-up condition reveals that after $C_4 \geq C_{diff}$ the differential mode will have the necessary condition to start up, i.e.

$$C_{diff} = \frac{1}{r_{ds}\omega}\sqrt{\frac{{g_{m5}}^2 r_{ds} R_{tank}(1 - g_{m1} r_{ds}) - (1 + g_{m5}.r_{ds})^2}{1 - g_{m5}.R_{tank}}} \tag{4.8}$$

To have only one stable quadrature mode we should satisfy the following condition:

$$C_{4,min} \leq C_{4,opt} \leq C_{diff} \tag{4.9}$$

Fig. 4.7 shows the calculated and simulated real admittance of the oscillator for the two quadrature modes and the differential mode of oscillation as a function of the capacitance at node 1. Simulation results agree with the analysis and shows for a QOSC with tuning range of 1.3 to 1.9 GHz and for C from 0.5 pF to 3 pF, the quadrature mode 2 is the only existing mode.

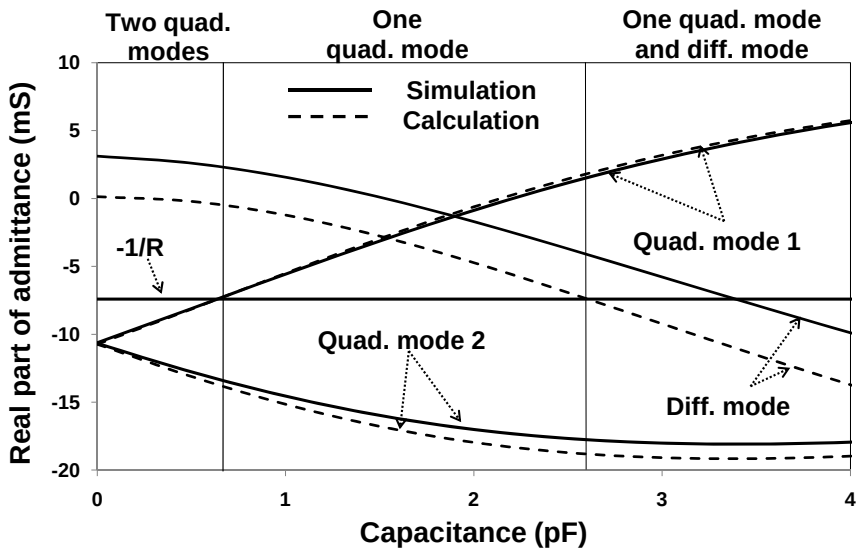

Figure 4.7: Real admittance for different modes of oscillation (at 1.6 GHz) as a function of C_4.

4.2 Measurement Results

The chip is fabricated in a 0.13 μm standard CMOS technology. The microphotograph of the QOSC is shown in Fig. 4.8. All measurements have been performed with a current consumption of 5 mA and supply voltage of 1.2 v.

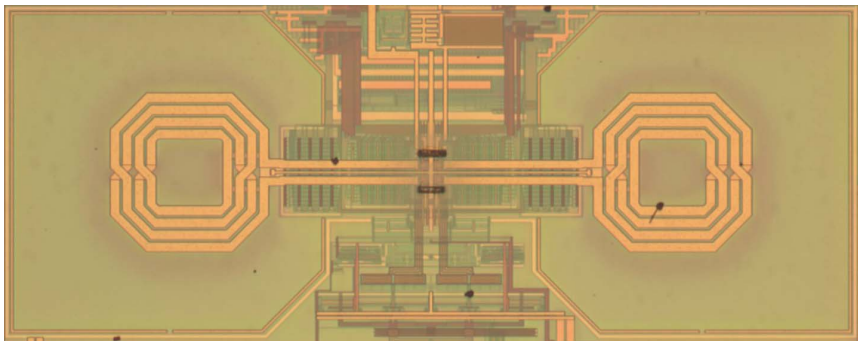

Figure 4.8: Microphotograph of QOSC fabricated in 0.13 μm standard CMOS technology.

To verify that there is no phase ambiguity in the fabricated chip, we repeatedly cycled

on and off the QOSC at different temperature, biasing, and frequency tuning, and captured the frequency and output sequence. Measurement results agreed with the analysis and simulation results, and show that the proposed QOSC has only one quadrature mode of oscillation. Fig. 4.9 shows the measurement and simulation results of the oscillation frequency of fabricated QOSC, and there is a very good agreement. The QOSC has been designed for a wide tuning range and the measured tuning range is 30%.

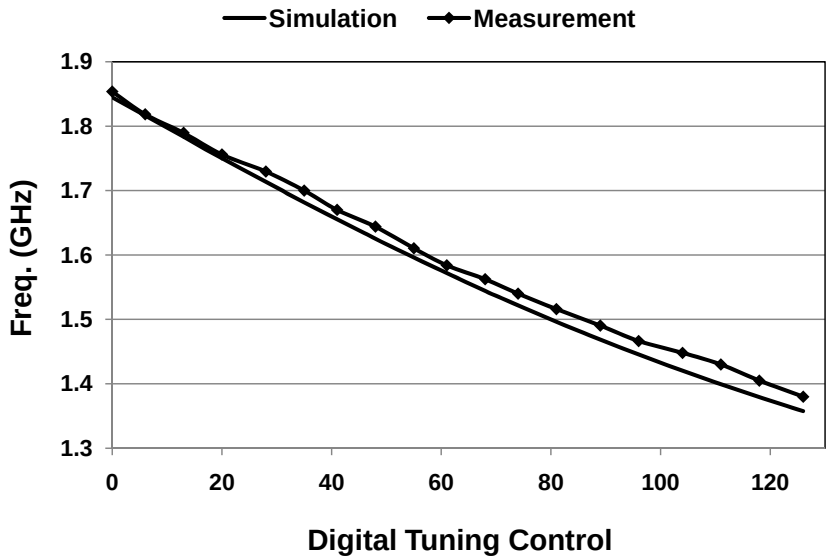

Figure 4.9: Measured oscillation frequency versus tuning control.

Fig. 4.10 shows the measurement and simulation results of phase noise of the QOSC for different carrier frequencies. The results are for a 100 KHz offset frequency, and the agreement is excellent.

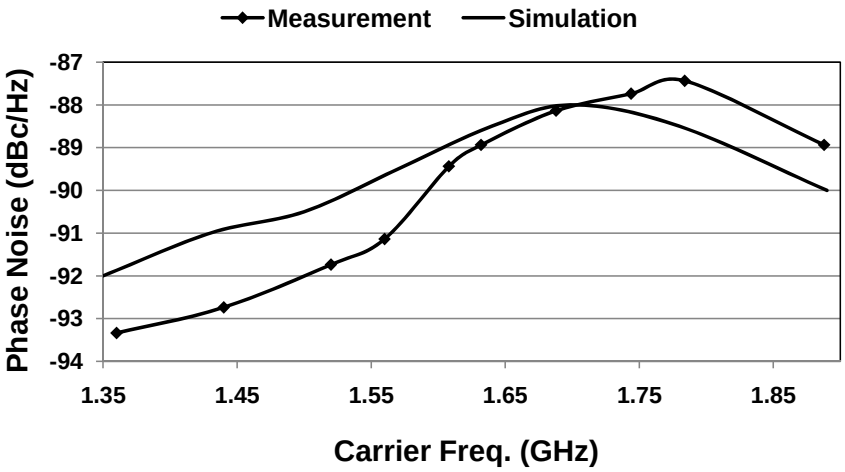

Figure 4.10: Measured phase noise at 100 KHz offset frequency.

4.3 Wide Tuning Range Dual Mode LC S-QOSCs

Emerging multiband devices with very wideband spectrum coverage and the software-defined radios (SDRs) [66] both typically require multiple oscillators, in the absence of high performance wide tuning range VCOs. In this context, wide tuning range oscillators, and particularly wide tuning range quadrature LC-VCOs are finding increasing importance [64, **?**].

Safarian [13] presents a comprehensive summary (Table I of [13]) of wide tuning range VCO designs. The designs are all differential and, among those, the switched inductor resonator designs [67] are easiest to use in a quadrature design, but their phase noise performance suffers from tank quality factor degradation due to series switch loss. Transformer-based resonator [68] and multi-port coupled inductor approaches [13] are immune to switch loss and show better performance. However, it can be challenging to make a small size quadrature layout with low I/Q coupling as recommended in [54], causing poor quadrature phase accuracy or a large area penalty. A more recent method [69] proposes a design with an inherent multi-phase core, using

left-hand LC-ring coupling.

We have previously proposed a novel design method to significantly increase the tuning range of quadrature oscillators (QOSCs), by switching the oscillator quadrature mode (or sequence) [70, **?**].

In section II, we explain the QOSC tuning range dependency on the modes of oscillation and how the tuning range of QOSC can be extended by mode switching. In Section III, we propose a specific circuit topology for extending the tuning range of series QOSCs (S-QOSCs) and present the corresponding analysis and design guidelines. In Section IV, two design examples and their performance based on the experimental and simulation data are presented.

4.3.1 Selective Mode Switching

In previous section we proposed the method to remove the mode ambiguity, where four capacitors were added to nodes 1-4 (Fig. 4.1). It was shown that the additional capacitor C_4 is reflected as a positive resistance in parallel to the tank load in Mode 1, while it adds a negative resistance in Mode 2. Therefore, Mode 2 can dominate and Mode 1 would be suppressed. Both [64] and [58] force the QOSC to have a specific quadrature mode and thus their effective tuning range will be that of the dominant mode, which is significantly increased compared to the overlap range (Fig. 3.8).

With this as background, we observe that it is possible to further increase the tuning range of the QOSC if we can arbitrarily set the oscillation mode of the QOSC. In such a case, the tuning range will be the *union* of the tuning range of the two modes (Fig. 3.8). A multiplexer must also be added to the output of QOSC to correct the quadrature sequence, similar to [65]. In

here we show a specific implementation of this idea, with supporting analysis, simulations, and measurement results.

4.3.2 Proposed Wide Tuning Range LC Quadrature Oscillator Topology

In this section we propose a new series-coupled quadrature oscillator (S-QOSC) (Fig. 4.11) to work in any of the two modes, offering increased effective tuning range. For this purpose, capacitors C4, C5, and switch SW4 are added to the typical S-QOSC [54]. If SW4 is ON, the circuit behaves almost as [64] (in the newly proposed QOSC we have added C5, but when SW4 is ON, the effect of C4 will dominate) with mode 2 (+j coupling) as the dominant mode. If SW4 is OFF, the addition of C5 results in mode 1 (-j coupling) being the dominant mode of oscillation as explained later.

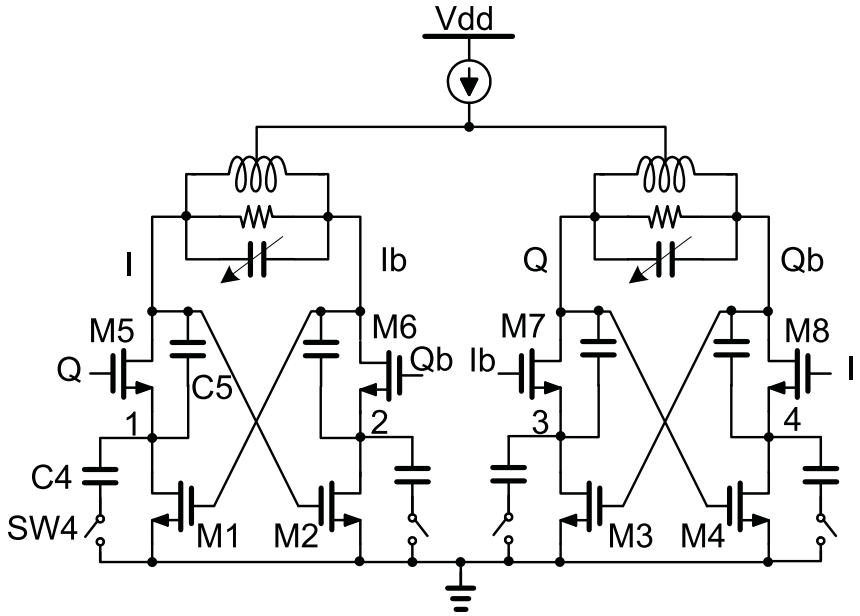

Figure 4.11: Wide tuning range LC quadrature oscillator with selective quadrature mode.

4.4 Analysis of Wide Tuning Range QOSC

In this section we provide a small-signal analysis for the quadrature mode switching, and derive the equations governing the wide tuning range design.

4.4.1 Quadrature Mode Selection of Proposed Quadrature Oscillator

Fig. 4.12 shows the simplified small-signal model for the quarter-circuit of Fig. 4.11. Transistors are represented by the transconductance and parasitic capacitors. Because M1 is always in the triode region, resistor r_{ds} is added to the model. *V* and *Vc* refer to voltages of node *I* and node *1* respectively. The voltage at the other nodes is represented as a function of *V* and *Vc*. The (+/-) signs are related to mode 2 and mode 1, respectively.

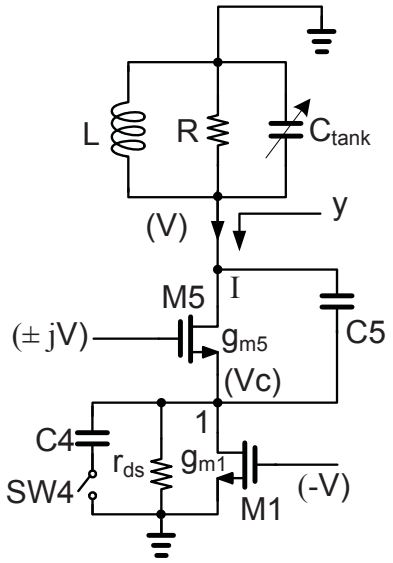

Figure 4.12: Simplified circuit based on symmetry and linearity of the circuit for small signal analysis of quadrature modes. (+) and (-) signs in ± sign correspond to +j coupling for mode 2 and -j coupling for mode 1, respectively.

With this model, the real part of the admittance, looking into all active devices at node I

Table 4.1: Calculation Parameters

g_{m1}	g_{m2}	g_{ds}	R	C_1	C_2	C_3
20 ms	40 ms	40 ms	140 ohm	150 fF	250 fF	100 fF

(the dashed-line section in Fig. 4.12) is:

$$y_{real} = \frac{f(g_{m1}, g_{m2}, g_{ds}, \omega, C_{2,3,4,5})}{(g_{m2}+g_{ds})^2 + (\omega \sum_{i=2}^{5} C_i)^2} \pm \frac{h(g_{m1}, g_{m2}, g_{ds}, \omega, C_{2,3,4,5})}{(g_{m2}+g_{ds})^2 + (\omega \sum_{i=2}^{5} C_i)^2} \tag{4.10}$$

where $1/r_{ds}$ has been replaced with g_{ds}. C_1, C_2, C_3, and C_6 are intrinsic and parasitic capacitances of transistors. C_6 is $200fF$ and C_4 and C_5 are added capacitors to the traditional S-QOSC to have the new wide tuning range S-QOSC. The junction capacitances at darin of M5 and M8 are added to C_{tank}. The functions $f()$ and $h()$ are given by:

$$f() \approx -(g_{m2}+g_{ds})(g_{m1}.g_{m2} - (\omega C_2)^2 - (C_5 - C_3)^2)$$
$$-(\omega)^2(\textstyle\sum_{i=2}^{5} C_i)(g_{m2}(C_2 + C_5 - C_3) - g_{m1}(C_5 - C_3)) \tag{4.11}$$

and

$$h() \approx -g_{m1}\omega C_2(g_{m2}+g_{ds})$$
$$+g_{m2}g_{ds}\omega(C_2 + C_5 - C_3) - (g_{m2})^2\omega(C_3 + C_4) \tag{4.12}$$

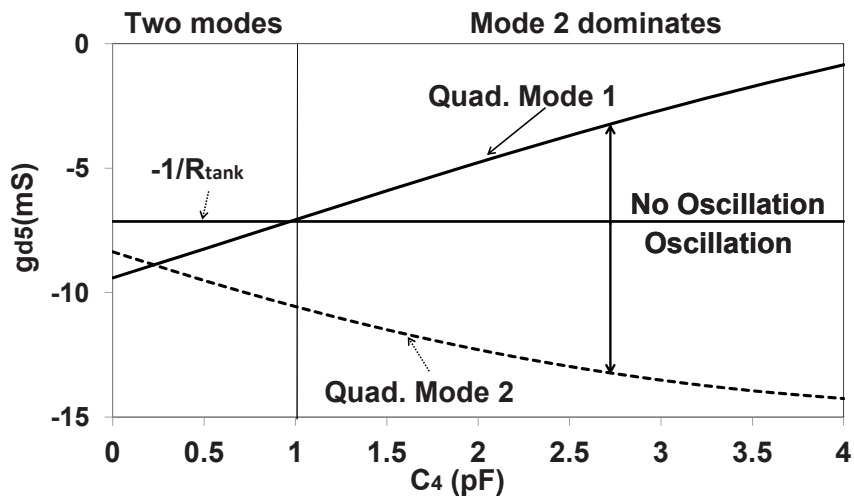

Figure 4.13: Calculated real part of admittance for two quadrature modes of oscillation (at 1.4 GHz) as a function of C_4+C_6 (SW4 is ON).

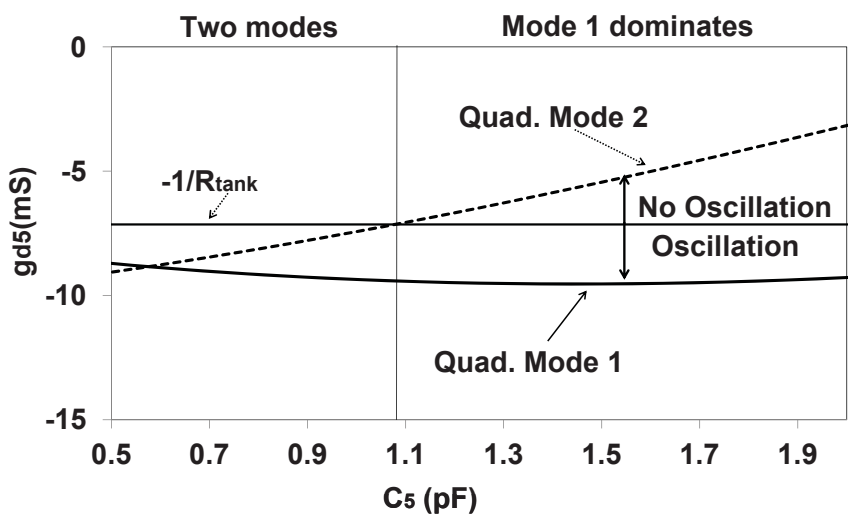

Figure 4.14: Calculated real part of admittance for two quadrature modes of oscillation (at 1.4 GHz) as a function of C_5 (SW4 is OFF).

The oscillator start-up condition for each mode defines that y_{real} should be negative and its absolute value should be larger than the real part of the tank admittance $(1/R)$. The key point is that the function $h()$ in (4.10) has different signs for mode 1 and mode 2, and determines the dominant mode of oscillation.

First we analyze the case where SW4 is ON. From this we can see that C_4 makes mode 2 (+j coupling) stronger while it makes mode 1 (-j coupling) weaker in the start-up condition. In Fig. 4.13, y_{real} is plotted as a function of C_4 for two modes of quadrature oscillation. It is clear that by increasing C_4, y_{real} for mode 2 becomes more negative, while y_{real} of mode 1 has the opposite trend. Therefore, for C_4 values larger than the threshold shown in Fig. 4.13, mode 1 does not meet the oscillation start-up condition and only mode 2 remains. As is seen in Fig. 4.14, the regenerative power in mode 2 is quickly reduced as C_5 increases (in the absence of C4) resulting in weaker and eventually eliminated mode 2, while mode 1 is slightly strengthened.

4.4.2 Center Frequency and Tuning Range of Each Oscillation Mode

The oscillation frequency is determined by the imaginary part of the admittance looking into all active devices (Fig. 4.12) and is given by:

$$y_{imag} \approx \frac{\pm g_{m2} g_{ds}(g_{m2} + g_{ds})}{(g_{m2} + g_{ds})^2 + (\omega \sum_{i=2}^{5} C_i)^2} \tag{4.13}$$

In most cases (5.11) can be reduced to

$$y_{imag} \approx \frac{\pm g_{m2}}{2} \tag{4.14}$$

At oscillation frequency the total y_{imag} is zero, therefore,

$$jy_{imag} + \frac{1}{jL\omega} + j\omega C_{tank} = 0 \tag{4.15}$$

the two center frequencies of each oscillation mode would be

$$\omega \approx \omega_o \mp \frac{g_{m2}}{4C_{tank}} \tag{4.16}$$

where $\omega_o = \frac{1}{\sqrt{LC_{tank}}}$.

It is clear from (4.16) that Mode 1 (-j coupling) oscillates at a higher frequency than the tank resonance frequency, while Mode 2 (+j coupling) oscillates at a lower frequency. The tuning range of each mode can be found from (4.14) and (4.16) as shown by,

$$\Delta\omega \approx (-\frac{1}{2C_{tank}\sqrt{LC_{tank}}} \pm \frac{g_{m2}}{4(C_{tank})^2})\Delta C_{tank} \tag{4.17}$$

From (4.17) it is clear that mode 1 (-j coupling) always has a wider tuning range than mode 2.

4.4.3 Continuous Wide Tuning Range Condition

The condition to have a continuous and optimum coverage through $\omega_{min,2}$ to $\omega_{max,1}$ is to have $\omega_{max,2} = \omega_{min,1}$

$$g_{m2} \approx \frac{4}{\sqrt{L}} \frac{(C_{min})^{-1/2} - (C_{max})^{-1/2}}{(C_{min})^{-1/2} + (C_{max})^{-1/2}} \tag{4.18}$$

where C_{min} and C_{max} are the the tank capacitors when the tunable capacitors are at minimum and maximum values, respectively.

When the S-QOSC is optimized for phase noise and phase accuracy, there is a large flexibility in setting the cross coupling transistors (M5 to M8) [54]. Thus, a g_{m2} close to what was defined in (4.18) could be selected as part of the overall optimization to achieve the widest possible tuning range.

4.5 Phase Noise and Quadrature Phase Accuracy of Wide Tuning Range Dual Mode S-QO

The previous analysis suggests the acceptable range for C_4 and C_5 (Fig. 4.13 and Fig. 4.14) to select each mode of oscillation and consequently extend the combined tuning range. Here we examine the choice of C_4 and C_5 on the S-QO phase noise and quadrature phase accuracy. Table 4.2 shows the circuit parameters of the simulated S-QO.

Table 4.2: Circuit parameters for simulated S-QO

f_o (GHz)	M1 (um)	M5 (um)	C_4 (pF)	C_5 (pF)	L_t (nH)	C_t (pF)
3.7	120	240	1	0.8	1.2	1

4.5.1 Effect of C_4 and C_5 on Phase Noise

The transfer function of noise current (i_n) to PM voltage noise (v_n) varies with C_4 and C_5. The phase noise $\mathcal{L}(\omega_m)$ at a frequency offset of ω_m is [71]:

$$\mathcal{L}(\omega_m) \approx \frac{\overline{v_{nPM}^2}}{\frac{1}{2}A^2} \tag{4.19}$$

where A is the oscillation voltage amplitude, and $\overline{v_{nPM}^2}$ is the additive output noise voltage at ω_m. Assuming that the output noise arising from amplitude fluctuations, $\overline{v_{nAM}^2}$, is negligible at close-in offsets [71] only the phase modulated (PM) component of v_n is included here. Since neither C_4 nor C_5 has a direct impact on the tuning range in (4.17) of the QO, these capacitors provide two independent degrees of freedom to minimize the phase noise.

Fig. 4.15 shows a Mode 2 noise analysis (SW4 closed). Drain noise currents i_{n1} and i_{n5} are generated by M1 and M5, respectively, and i_{nt} represents the noise generated by the tank circuit. Noise voltages v_{fM1} and v_{fM5} represent the $1/f$ noise of M1 and M5, respectively. Also, the path to the output for different noise sources through C_4 and C_5 is shown in Fig. 4.15.

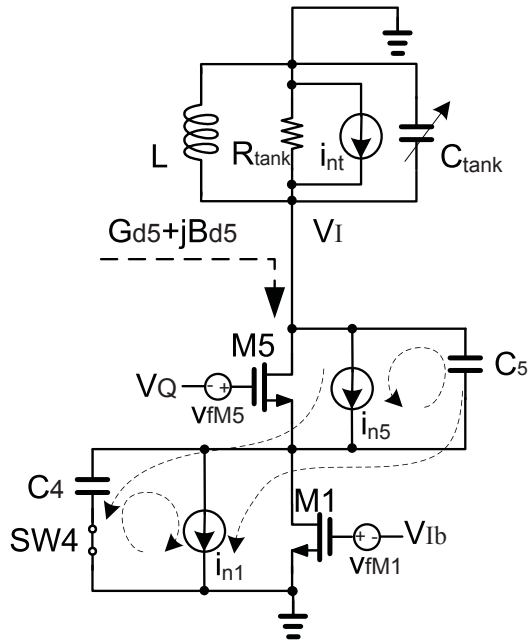

Figure 4.15: Noise sources in the S-QO for noise analysis in Mode 2.

The simplified circuit of Fig. 4.15 is shown is Fig. 4.16 (a) where G_{d5} and B_{d5} are the equivalent large-signal components of the active part looking into the drain of M5. i_n is the equivalent of all noise sources transferred to the drain of M5. [71] shows that Fig. 4.16(a) can be further simplified to Fig. 4.16(b) for a PM noise current (i_{nPM}).

$$v_{nPM} = Z_{eqPM} i_{nPM} \tag{4.20}$$

where v_{nPM} is the PM voltage noise at the output. It should be noted that Fig. 4.16(b) and (4.20) are not valid for AM noise analysis [71].

Therefore, (4.19) can be written as

$$\mathcal{L}(\omega_m) \approx \frac{\overline{i_{nPM}^2} |Z_{eqPM}(\omega_m)|^2}{\frac{1}{2}A^2}. \tag{4.21}$$

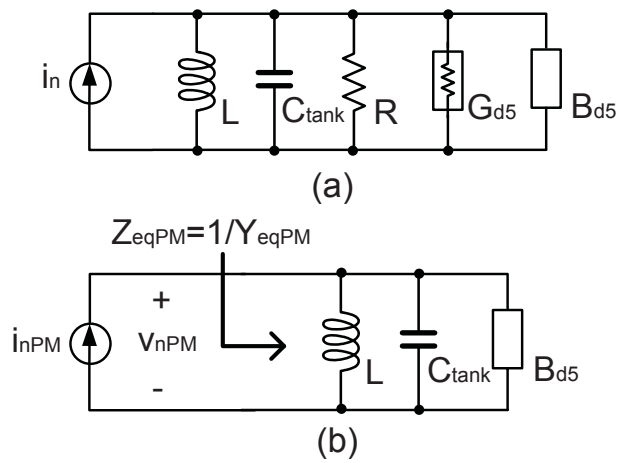

Figure 4.16: (a) Noise current equivalent circuit, (b) simplified equivalent circuit.

At $\omega_o + \omega_m$,

$$Y_{eqPM}(\omega_o + \omega_m) = Y_{eqPM}(\omega_o) + \frac{dY_{eqPM}(\omega)}{d\omega}(\omega_m) \tag{4.22}$$

where ω_o is the oscillation frequency and $Y_{eqPM}(\omega_o)$ must be zero. Therefore,

$$\frac{1}{L\omega_o^2} = C_{tank} + \frac{B_{d5}(\omega_o)}{\omega_o}. \tag{4.23}$$

replacing (4.23), (4.22) simplifies to

$$Y_{eqPM}(\omega_o + \omega_m) = (2C_{tank} + \frac{dB_{d5}}{d\omega} + \frac{B_{d5}}{\omega_o})\omega_m. \tag{4.24}$$

In the case that $B_{d5} = \omega C$, where C is the total capacitance of the active part to the ground, $|Z_{eqPM}(\omega_m)|^2$ simplifies to

$$|Z_{eqPM}(\omega_m)|^2 = \frac{1}{4(C + C_{tank})^2}\frac{1}{\omega_m^2}, \tag{4.25}$$

By replacing (4.25) in (4.21), the negative slope of $-20\ dB/decade$ behavior for phase noise results.

In the case of a S-QO, the B_{d5} is not a simple function of ω and $B_{d5} = \omega C$ does not hold. We calculate B_{d5} from (5.11) and replace all g_m and g_{ds} values with their large-signal equivalents [71], $i.e.$

$$G_{eff} = G[0] - G[2] \tag{4.26}$$

where "G" is either G_m or G_{ds}, and $G[0]$ and $G[2]$ are the DC and second order Fourier series coefficients of the large-signal instantaneous $G(t)$ [71]. To calculate the variation of Z_{eqPM} with C_4, $G_{m5}(t)$, $G_{ds5}(t)$, $G_{m1}(t)$, and $G_{ds1}(t)$ are calculated from $Spectre$ simulations with the parameters of Table 4.2, the Fourier series coefficients are calculated, and substituted into (5.11). Fig. 4.17 shows the calculated $|Z_{eqPM}(10MHz)|^2$ (normalized to its value at $C_4 = 0$ pF) as a function of C_4.

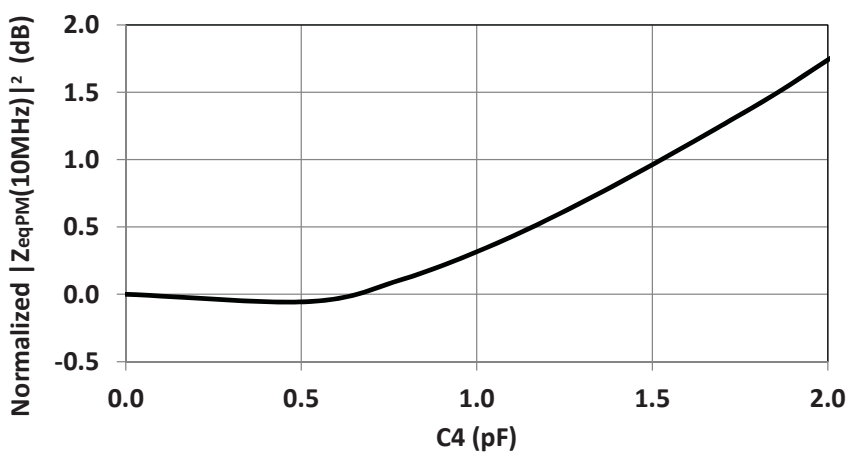

Figure 4.17: Normalized $|Z_{eqPM}(10MHz)|^2$ as a function of C_4.

4.5.2 Amplitude of Oscillation

By deriving the $G_{d5,eff}$ variation with respect to C_4, we can also find the change in the amplitude (A). We approximate the amplitude deviation as

$$\frac{\Delta A}{A} = \frac{\Delta G_{d5,eff}}{G_{d5,eff}}. \tag{4.27}$$

$G_{d5,eff}$ can be calculated using a more precise version of (4.10) and with replacing all g_m and g_{ds} values with their large-signal equivalents. From (4.26), $G_{d5,eff}(C4 = 1pF) = 3.8$ mS and $G_{d5,eff}(C4 = 1.8pF) = 3.2$ mS. Therefore we approximate $\Delta A = -15\%$ (-1.2 dB). Fig. 4.18 plots the simulated variation of oscillation amplitude which agrees with the calculated variation when C_4 increases from 1 to 1.8 pF.

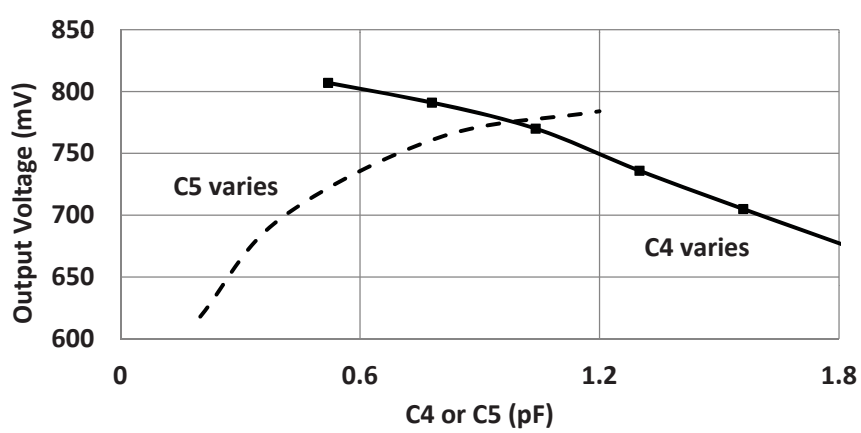

Figure 4.18: Simulated oscillation amplitude of Mode 2 as a function of C_4 (solid line) where $C_5 = 0.8$ pF, and as a function of C_5 (dashed line) where $C_4 = 1$ pF. Oscillation frequency is 3.7 GHz. $L_t = 1.2$ nH. $Q_{tank} = 9$, $M1 = 120$ μm, and $M5 = 240$ μm.

4.5.3 Tank Noise

The noise associated with the tank loss is modeled as a white spectrum noise (independent of C_4 and C_5). If we assume that the phase noise at an offset frequency of 10 MHz is dominated by tank noise, by using (4.21), replacing the calculated $\Delta A = -1.2$ dB and $\Delta|Z_{eqPM}|^2 = 1.1$ dB (Fig. 4.17), the calculated phase noise variation at 10 MHz offset frequency is 2.3 dB when C_4 varies from 1 pF to 1.8 pF.

$1/f$ Noise Contribution of M1

To study the effect of C_4 on the $1/f$ noise contribution of M1 to the close in phase noise, we model the noise as a voltage source (v_f) at the gate of M1 (Fig. 4.19).

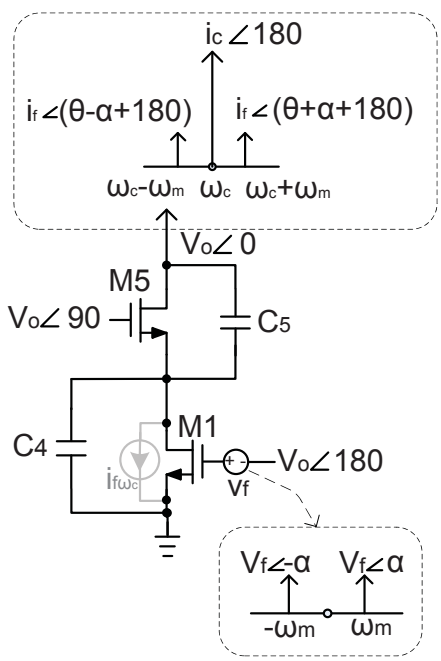

Figure 4.19: Model for up-conversion of flicker noise of M1.

The v_f is modulated and up-converted to the carrier frequency as a current at the drain of M1 ($i_{f\omega c}$). After a phase rotation of θ (due to C_4, C_5, and g_{ds}), it appears as a noise current (i_f) at the output. An important observation is that if $\theta = 0$ in Fig. 4.19, the sum of two sidebands of i_f with phases $\pm\alpha$ relative to i_c, i_{ftot}, is co-linear with i_c which only modulates the amplitude of i_c (Fig. 4.20) and does not contribute to phase noise.

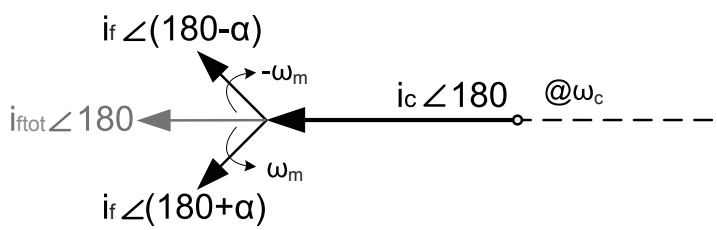

Figure 4.20: $1/f$ noise phasor added to sine-wave i_c for $\theta = 0$.

However, in practice, θ is non-zero due to capacitors C_4 and C_5 and modulation of g_{ds1} by its drain voltage which has a quadrature component. Nevertheless, C_4 shunts the modulated $1/f$ noise current of M1 to ground, so increasing C_4 results in a reduction of the $1/f$ noise contribution of M1 to i_f.

4.5.4 $1/f$ Noise Contribution of M5

Fig. 4.21 shows a model for up-conversion of the $1/f$ noise of M5. We will study the two extreme cases of $\omega C_4 = 0$ and $\omega C_4 >> g_{ds}$. When $C_4 = 0$, $i_f = v_{fx} g_{ds}$, θ is zero, and $i_f \angle \alpha + 90$ is the $1/f$ noise current at the output, which is completely converted to phase noise. For large values of C_4, we can ignore g_{ds} and θ approaches 90 ($i_f \angle \alpha + 180$), converting the noise

to AM rather than PM noise, and the contribution of i_f in phase noise is minimized. Therefore, the $1/f$ noise contribution of M5 is reduced by increasing C_4. The simulation also shows that by increasing C_4 the voltage swing at source of M5 (along with amplitude of oscillation) reduces and changes the $1/f$ noise contribution of M5. C_5 reduces the total noise current going to the tank as it creates a circulation path for $1/f$ noise of M5.

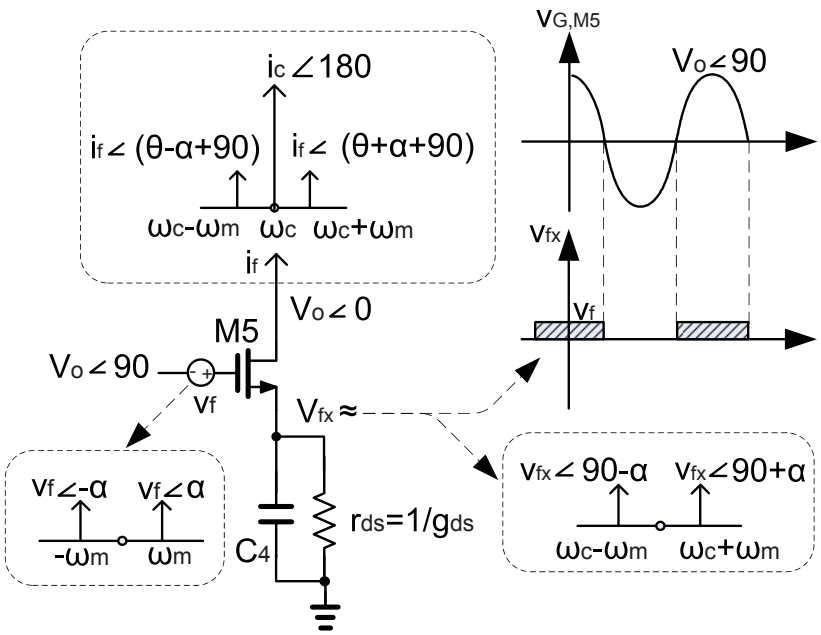

Figure 4.21: Model for up-conversion of flicker noise of M5.

Fig. 4.22 shows the simulated output noise contribution of different noise sources of Fig. 4.15 at an offset frequency of 10 kHz in Mode 2. As C_4 increases, the reduction of $1/f$ noise contribution of M5 is clear. Once $\omega C_4 >> g_{m5}$, C_4 will have little effect on output current. The noise contribution of M1 at this low offset frequency is due to $1/f$ noise and decreases by increasing C_4.

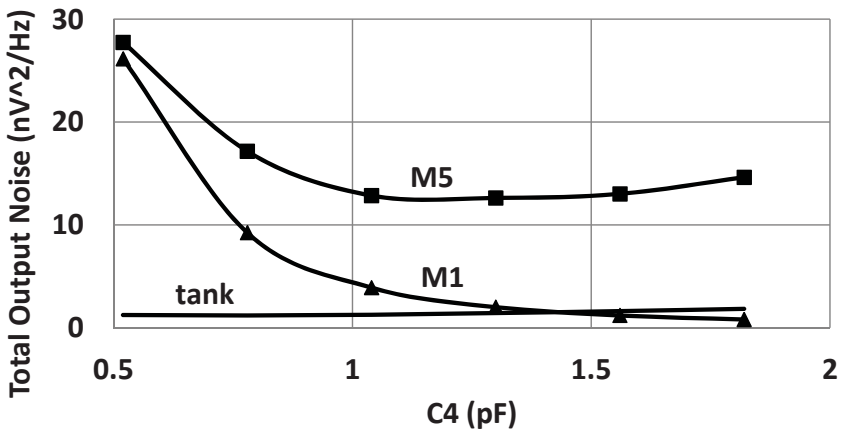

Figure 4.22: Simulated output noise contribution from different noise sources at offset frequency of 10kHz for Mode 2 (oscillation frequency of 3.7GHz). $L_t = 1.2$ nH, $C_t = 140$ fF, and $C_5 = 0.8$ pF. The quality factor of the tank is 9. $M1$ and $M5$ are 120μm and 240μm, respectively.

The effect of C_5 on the $1/f$ noise contribution of M1 is demonstrated in Fig. 4.23. In this simulation, C_4 is fixed to 1 pF while C_5 is variable. The $1/f$ noise contribution of M1 is reduced with increasing C_5.

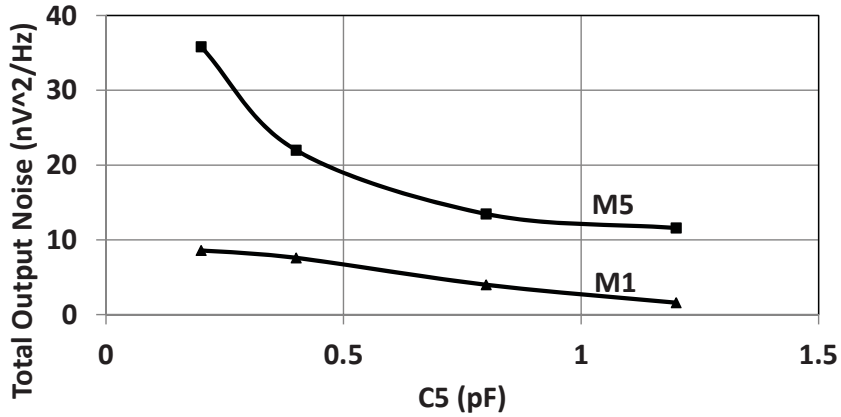

Figure 4.23: Simulated output noise contribution from different noise sources at offset frequency of 10kHz for Mode 2 (oscillation frequency of 3.7GHz). $L_t = 1.2$ nH and $C_4 = 1$ pF. The quality factor of the tank is 9. $M1$ and $M5$ are 120μm and 240μm, respectively.

4.5.5 White Noise of M1 and M5

The white noise contribution of M1 (i_{n1}) to the total phase noise behaves similarly to $1/f$ noise, and decreases as C_4 increases due to C_4 shunting the noise to ground. The white noise contribution of M5 (i_{n5}), however, behaves differently from its $1/f$ noise contribution to the overall phase noise and increases with C_4. In the conversion of white noise to phase noise, the two contributing sidebands are originated from $\omega_o \pm \omega_m$ and thus are uncorrelated. In this case, half of this noise appears as PM and contributes to the phase noise and the other half is AM and is suppressed in oscillator [72]. The noise contribution is not dependent on the phase of the noise transfer function to the oscillator output. The only important effect of the increase in C_4 is to increase the magnitude of the noise transfer function, by providing a lower impedance for M5 noise to flow to the tank load as shown in Fig. 4.21.

The simulated output noise contribution from different noise sources at 10 MHz offset frequency as a function of C_4 is shown in Fig. 4.24 which confirms the above explanations. Similarly, by increasing C_5, i_{n1} contributes more noise, but i_{n5} circulates through C_5 instead of flowing to the output Fig. 4.15.

4.5.6 Phase Noise Simulations

The $Spectre\ RF$ phase noise simulation of Mode 2 at a frequency of 3.7 GHz for different offset frequencies as a function of C_4 is shown in Fig. 4.25. Fig. 4.25(a) shows that by increasing C_4 to 1 pF, the phase noise at 10 kHz offset frequency improves and there is little improvement beyond this, which is in agreement with earlier explanation of $1/f$ noise of M1

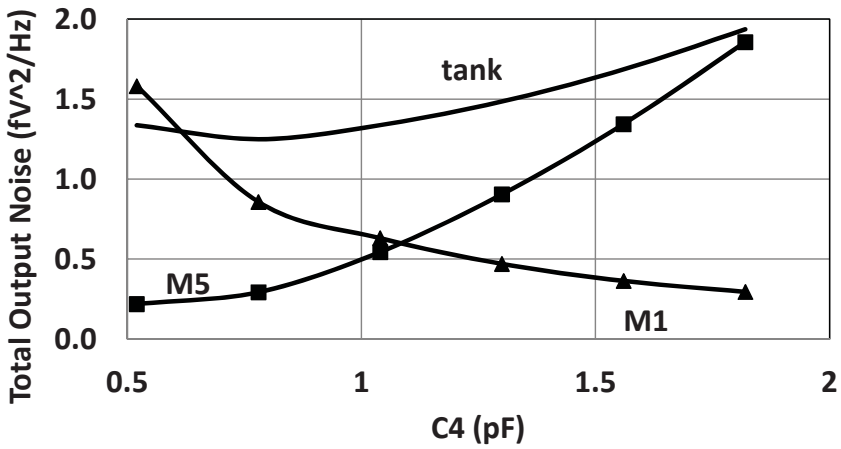

Figure 4.24: Simulated output noise contribution from different noise sources at offset frequency of 10 MHz for Mode 2 (oscillation frequency of 3.7GHz). $L_t = 1.2$nH, $C_t = 140$fF, and $C_5 = 0.8$ pF. The quality factor of the tank is 9. $M1$ and $M5$ are 120μm and 240μm, respectively.

and M5 (the main contributors at offset frequency of 10 kHz). Fig. 4.25(b) shows that at higher offset frequencies there is a minimum phase noise for $C_{4,opt}$ of $\approx$ 1 pF. This minimum phase noise is due to the falling of M1 white noise and increasing M5 white noise along with the rising of tank noise (Fig. 4.24).

The simulated phase noise at offset frequency of 10 MHz as a function of C_4 (Fig. 4.25(b)) shows that phase noise increases by 3.3 dB which is slightly higher than the expected value of 2.3 dB calculated earlier. The error is partly due to the error in approximating Z_{eqPM}(10 MHz) and ΔA, and partly because of ignoring the channel noise contribution of M5 to the output noise which is visible in Fig. 4.24.

Fig. 4.26 shows the simulated phase noise at offset frequencies of 10 kHz and 10 MHz as a function of C_5. The simulation shows that increasing C_5 results in improving phase noise in both offset frequencies. Part of the improvement is due to increase in amplitude of oscillation

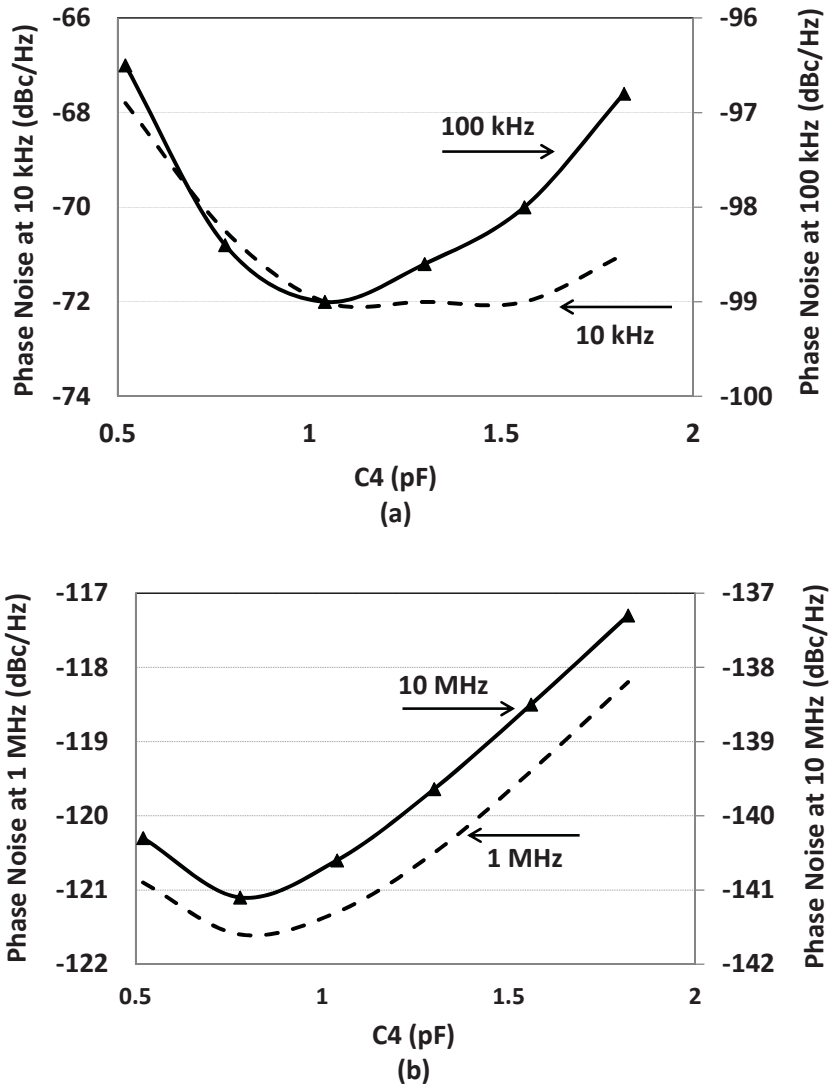

Figure 4.25: Simulated phase noise of S-QO in Mode 2 of quadrature oscillation as a function of C_4 for oscillation frequency of 3.7 GHz; (a) at offset frequencies of 10 kHz (dashed line) and 100 kHz (solid line), (b) at offset frequencies of 1 MHz (dashed line) and 10 MHz (solid line).

(Fig. 4.18) by increasing C_5. At offset frequency of 10 kHz the major improvement is due to reduction of $1/f$ noise of both M1 and M5. At offset frequency of 10 MHz the improvement is mainly due to reduction of tank noise along with white noise of M5.

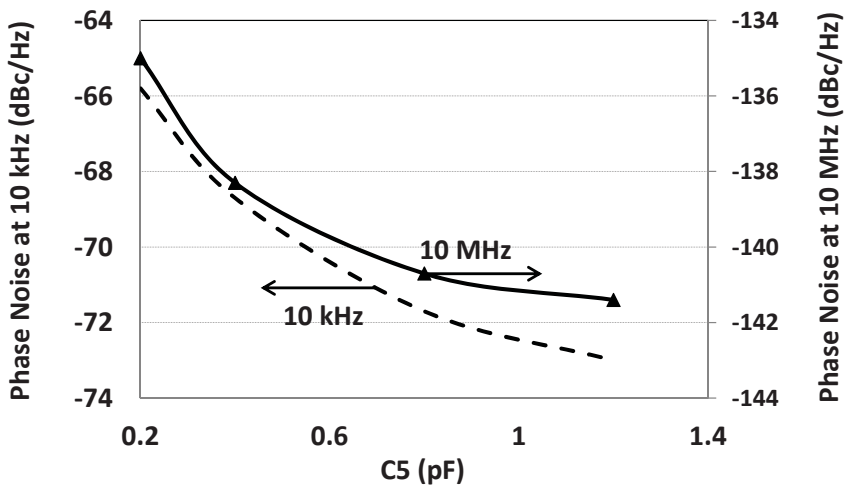

Figure 4.26: Simulated phase noise of S-QO in Mode 2 of quadrature oscillation as a function of C_5 for oscillation frequency of 3.7 GHz; at offset frequencies of 10 kHz (dashed line) and 10 MHz (solid line).

4.5.7 Phase Accuracy

Andreani $et\ al.$ [54] claimed a trade-off between phase noise and quadrature phase accuracy, and this can be evaluated for the proposed dual-mode S-QO. However, a mismatch in C_4 and C_5 will cause quadrature error, which in some applications will be essential to reduce. For example, the newer standards such as 802.11n requires an image rejection of approximately -34 dBc to achieve an EVM of -30 dB [73]. Therefore, achieving such performance for high production yields may require IQ calibration to reduce the quadrature error.

To see the effect of mismatch in C_4 (or C_5) in Fig. 4.11, the value of C_4 (or C_5) in one

branch has been changed and simulation results of quadrature phase has been compared to the case of no additional mismatch. Simulation results show that the quadrature phase error for 5% mismatch in C_4 or C_5 in Mode 2 varies from $0.6°$ to $1.8°$. At higher frequencies, the mismatch in C_4 and C_5 results in more deviation from $90°$, since the capacitance of the tank is lower and C_4 and C_5 contribute more to the overall capacitance.

In Mode 1, a 5% mismatch in C_5 results in $0.9°$ to $2.7°$ error. Again, the higher frequency of oscillation introduces more deviation in quadrature phase. Therefore, Mode 2 offers better quadrature phase accuracy than Mode 1. Figs. 4.27 and 4.28 show the simulated phase error as a function of mismatch in C_4, C_5, and C_t for two modes of quadrature oscillation at 3.7 GHz.

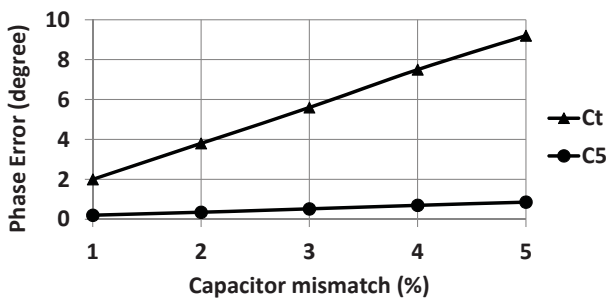

Figure 4.27: Simulated phase error of QO operating at 3.7 GHz (Mode 1). $C_4 = 0$, $C_t = 430$ fF and $C_5 = 0.8$ pF.

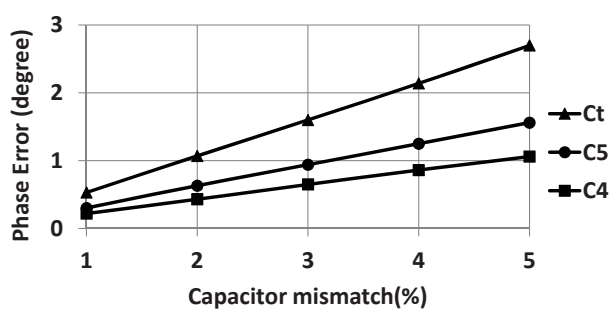

Figure 4.28: Simulated phase error of QO operating at 3.7 GHz (Mode 2). $C_t = 130$ fF, $C_4 = 1$ pF, and $C_5 = 0.8$ pF.

S-QOs were implemented with center oscillation frequencies of 1.3 GHz, 2.1 GHz, 3.7 GHz, and 4.4 GHz. The microphotograph of the fabricated chip in IBM 90-nm CMOS technology is shown in Fig. 5.8. Each S-QO has two modes of quadrature oscillation and each mode can be selected by SW4 which is implemented in series with C_4. The Frequency Tuning Range (FTR) defined as [**?**]

$$FTR = \frac{200(f_{max} - f_{min})}{f_{max} + f_{min}}\% \tag{4.28}$$

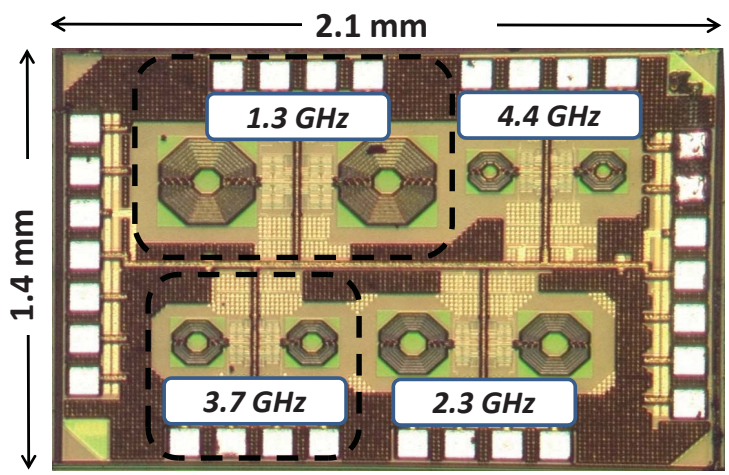

Figure 4.29: Microphotograph of die of four quadrature oscillators (2.1 x 1.4 mm^2).

4.5.8 S-QOs with Center Frequency of 1.3 GHz and 2.3 GHz

The first S-QO consumes less than 12 mA from a 1.2 V power supply and operated from 660 MHz to 1.84 GHz. Fig. 4.30 shows the measured tuning range for each mode of quadrature oscillation.

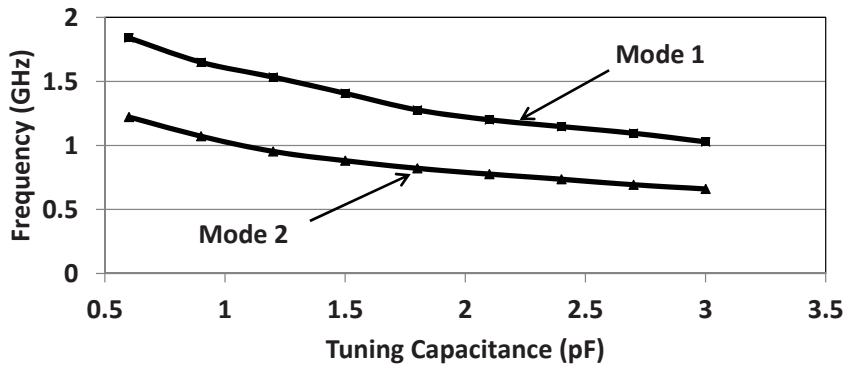

Figure 4.30: Measured tuning range of the two modes of quadrature oscillation for 1.3 GHz design. $L_t = 5.8$ nH, $C_t = 3$ pF, and $C_5 = 0.8$ pF. The size of $M1$ and $M5$ is 120 μm and 240 μm, respectively. C_4 in Mode 2 is 1.4 pF.

There should be enough overlap between the tuning ranges of the two modes of quadrature oscillation to guarantee a continuous tuning range. In other words, from Fig. 3.8, the design should pass the following condition for all the PVT corners:

$$\omega_{max,2} - \omega_{min,1} > 0 \tag{4.29}$$

In this design $\omega_{max,2} - \omega_{min,1} >= 200$ MHz which is sufficient.

Fig. 4.31 shows the simulation and measurement results of the phase noise at a 660 MHz oscillation frequency. The measured value at 3 MHz offset frequency is -142.3 dBc/Hz which is slightly higher than the simulation value.

The second S-QO design consumes 7 mA from a 1.2 V power supply. Fig. 4.32 shows the measured phase noise for Mode 1 of quadrature oscillation. The tuning range measured is 1.8 GHz to 2.8 GHz (FTR of 43%).

The measured phase noise is -135 and -133 dBc/Hz at 3 MHz offset frequency for

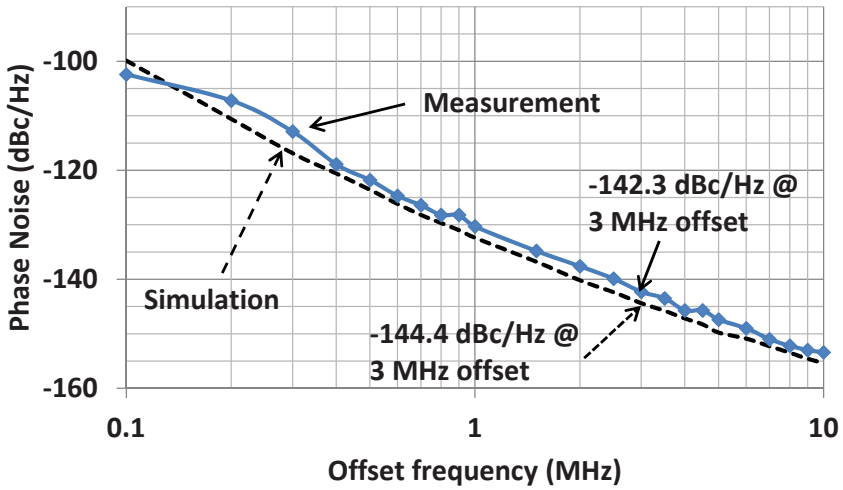

Figure 4.31: Measurement and simulation results of phase noise (at 660 MHz) for 1.3 GHz design.

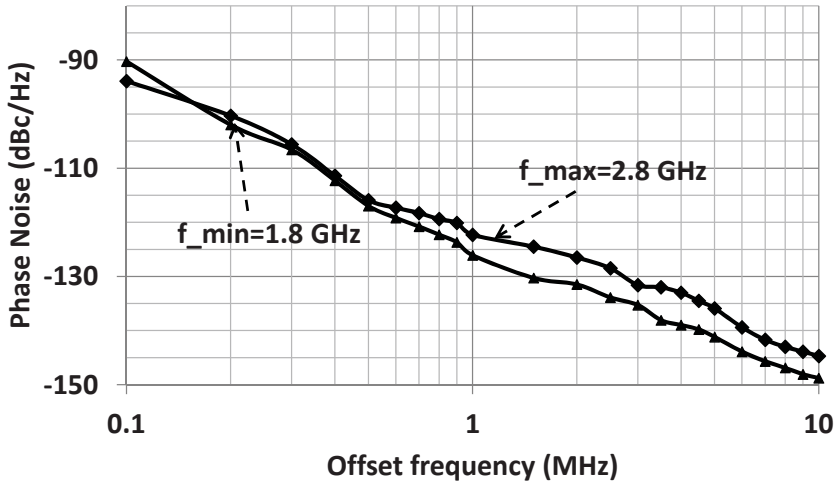

Figure 4.32: Measured phase noise of quadrature oscillation for 2.3 GHz design. $L_t = 2.9$ nH, $C_t = 1$ pF, and $C_5 = 0.8$ pF. The size of $M1$ and $M5$ is 120 μm and 240 μm, respectively.

center frequency of 1.8 GHz and 2.8 GHz respectively.

4.5.9 S-QO with Center Frequency of 3.7 GHz

The simulated differential peak of oscillation amplitude varies from 0.7 to 1.4 V over the tuning range. Fig. 4.33 shows the measurement results of phase noise in the first mode at at minimum frequency of 3.7 GHz and maximum frequency of 4.75 GHz.

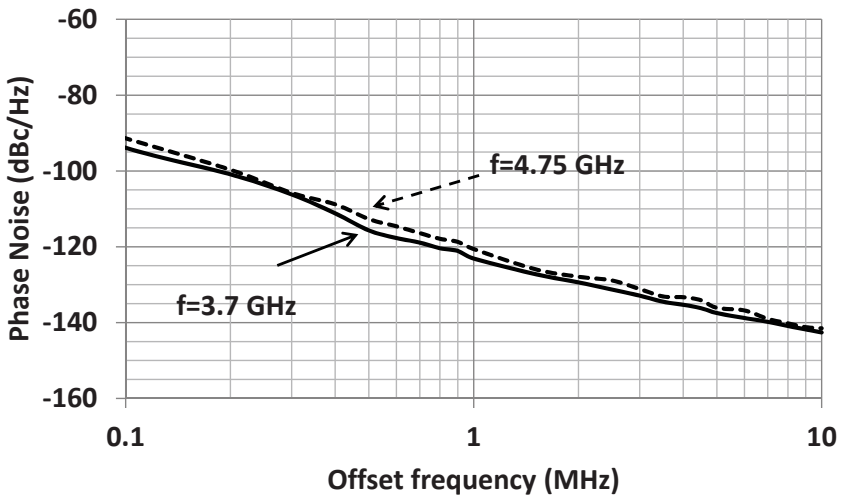

Figure 4.33: Measurement results of phase noise for Mode 1 at minimum frequency of 3.7 GHz and maximum frequency of 4.75 GHz.

Fig. 4.34 shows the measurement of phase noise results in the second mode at minimum frequency of 2.58 GHz and maximum frequency of 3.8 GHz. The phase noise at lower offset frequencies shows worse results for 2.58 GHz.

Simulation results of phase noise for maximum frequency of Mode 1 is shown in Fig. 4.35 which is up to 3 dB better than the measured results at lower offset frequencies. At higher

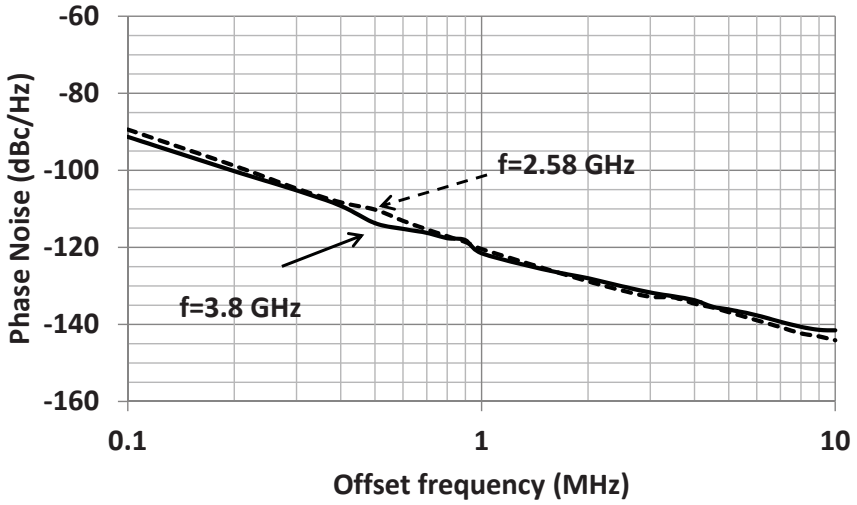

Figure 4.34: Measurement results of phase noise for Mode 2 at minimum frequency of 2.58 GHz and maximum frequency of 3.8 GHz.

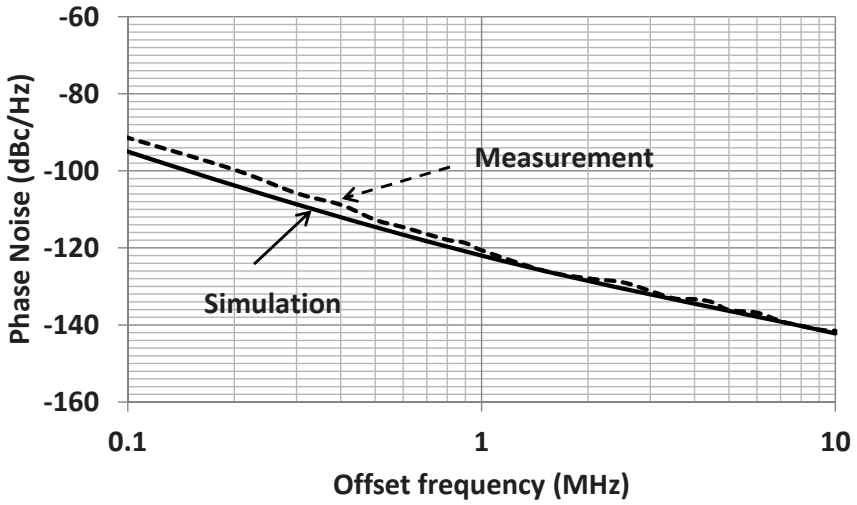

Figure 4.35: Simulation and measurement results of phase noise for Mode 1 at maximum frequency of 4.75 GHz.

Table 4.3: Comparison of Measured Results with other Quadrature and Differential Oscillators

	Tech. (nm)	Freq. (GHz)	FTR (%)	DC Power (mW)	PN (dBc/Hz)	Offset Freq. (MHz)	FOMT (dB)
[74]	65	5.3	46	18	-145	10	200
[75]	65	3.7	57	10	-125	1	201
[76]	65	2.5	10.2	0.25	-113	1	187
[77]	65	3	26	28.8	-147	10	191
[63]	90	13	21	10.6	-108	1	187
[78]	90	1.3	94	11	-138	3	200
[78]	90	3.7	60	12	-133	3	199
[78]	90	4.4	52	10	-128	3	196
[79]	90	5.8	45	14	-108.5	1	185
[13]	130	3.65	129	6.7	-117	1	204

than 1 MHz offset frequencies the measurement and simulation look alike.

4.5.10 S-QO with Center Frequency of 4.4 GHz

The tuning range in Mode 1 is 3.8 GHz to 5.5 GHz (FTR of 36%). The tuning range in Mode 2 is between 3.2 GHz and 4.5 GHz (FTR of 33%). The combined tuning range is from 3.2 GHz to 5.5 GHz for an overall FTR of 52%. The overlap between the two modes is from 3.8 GHz to 4.5 GHz (700 MHz) which can be reduced for further increase in combined tuning

range. Fig. 4.36 shows the measurement of tuning range for the modes of quadrature oscillation.

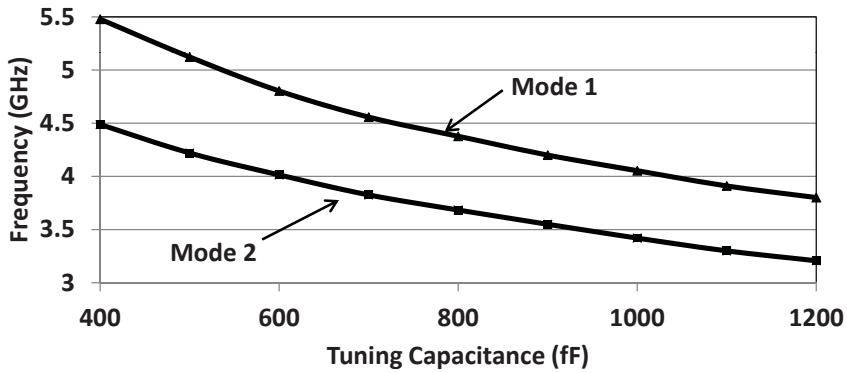

Figure 4.36: Measured tuning range of the two modes of quadrature oscillation for 4.4 GHz design. $L_t = 0.8$ nH, $C_t = 0.8$ pF, and $C_5 = 1.2$ pF. The size of $M1$ and $M5$ is 120 μm and 240 μm, respectively. C_4 in Mode 2 is 0.9 pF.

Fig. 4.37 shows the measurement of phase noise results in the two modes at maximum frequencies of each mode, 4.5 GHz and 5.5 GHz.

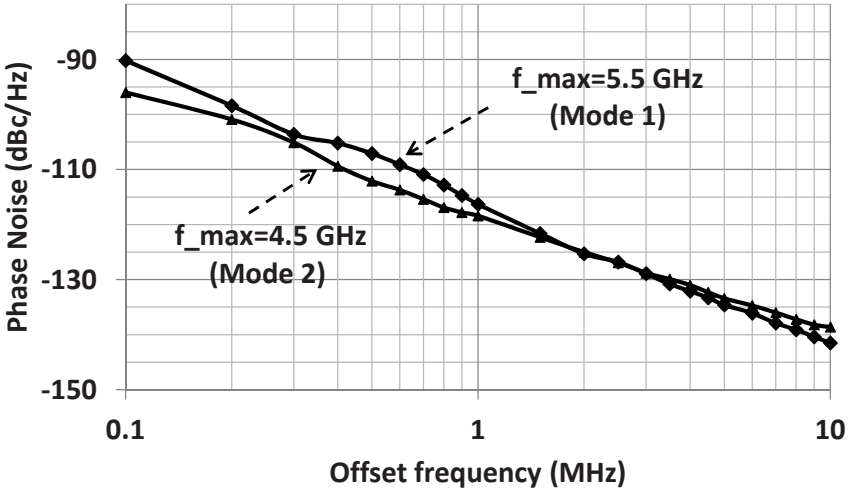

Figure 4.37: Measurement of phase noise in the two modes at maximum frequencies of each mode, 4.5 GHz and 5.5 GHz.

Fig. 4.38 shows the simulated and measured phase noise in Mode 1 at oscillation fre-

quency of 5.5 GHz. At lower offset frequencies, simulation shows 2 dB better better phase noise performance, while at higher offset frequencies the measurement and simulation look alike.

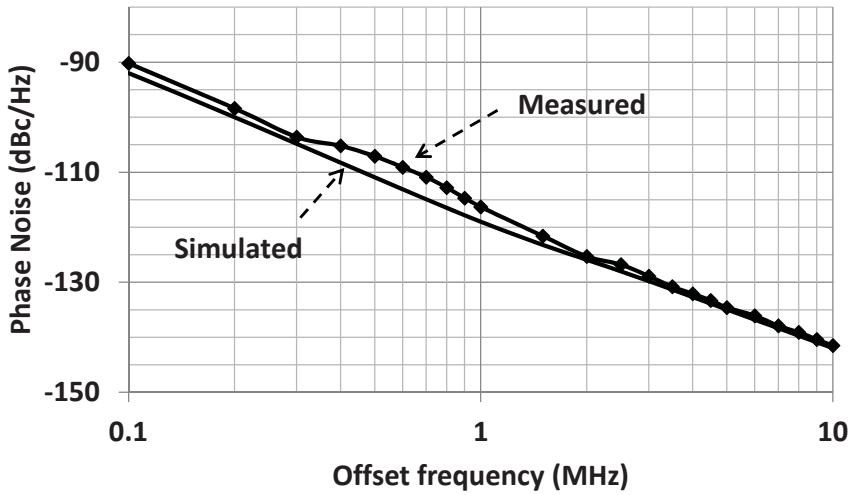

Figure 4.38: Simulation and measurement results of phase noise for Mode 1 at maximum frequency of 5.5 GHz.

4.5.11 Comparison to the State-of-the-Art

A figure of merit is used to compare this work against prior work that considers tuning range as well as phase noise from previous work [**?**]:

$$FOMT = 20log(\frac{f_o}{f_m}\frac{FTR}{10}) - PN(f_m) - 10log(P_{DC}) \tag{4.30}$$

where PN is the phase noise in dBc/Hz, P_{DC} is the dc power consumption in mW, FTR is the frequency tuning range, and f_o and f_m are oscillation frequency and offset frequency, respectively.

Table 4.3 shows the comparison results of this work with other works in 90 nm and 65

nm technologies. We have also compared the results with other differential (non-quadrature) oscillators in Table 4.3.

As stated in section IV (Fig. 4.23), the $1/f$ noise of coupling devices is the major source of phase noise at low offset frequencies. [75] proposed a four stage LC ring oscillator which uses passive coupling network. The passive coupling introduces no extra source of noise, therefore, by removing the coupling transistors, the phase noise at low offset frequencies is improved. On the other side, this design needs four different phases to select the desired mode of quadrature oscillation requiring four inductors which results in a larger die area.

4.6 Summary

A comparison of different architectures for *LC* quadrature oscillators has been reviewed. To solve problems with prior *LC* quadrature oscillators, a modified S-QO has been proposed with analysis of the oscillation conditions. Analysis of the operation frequency and tuning range of the two modes of quadrature oscillation has been demonstrated and the wide tuning range S-QO has been discussed. Phase noise and phase error analysis with simulation results have been presented. Measurement results show a frequency tuning range of 94% for an oscillator operating at center frequency of 1.3 GHz and the achieved FOMT is 200 dB. An FOMT of 199 dB and 196 dB is achieved for S-QOs operating at 4.4 GHz and 3.7 GHz.

This chapter, in parts, is a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Techniques 2015, IEEE Symposium on Radio Frequency Integrated Circuits (RFIC) 2012, and IEEE International Symposium on Circuits and Systems (ISCAS)

2012. The dissertation author was the first author on that publication. I would like to thank the other authors in these publications, Dr. Rahim Bagheri, Prof. James Buckwalter, and Prof. Lawrence Larson for their contribution and support in publishing these papers.

Chapter 5

Temperature Sensitivity of Non-Degenerate Modes in CMOS LC Quadrature Oscillators

Reference frequency generators are critical components in low-power sensors and wireless systems. A typical frequency generator includes a frequency synthesizer that is locked to the reference oscillator. Crystal (XTAL) oscillators are preferred for the reference oscillator due to low phase noise, high precision, low temperature drift, and long term stability. However, XTAL oscillators are large, difficult to manufacture, costly, and, most notably, incompatible with standard CMOS processes. Table 5.1 compares a crystal oscillator (XO), temperature-compensated crystal oscillator (TCXO), oven-controlled crystal oscillator (OCXO) [23], and LC oscillator. Most notably, a size, weight, and power premium exists when high accuracy and low temperature sensitivity are demanded for an application. To reduce the cost, recent work has sought CMOS

Table 5.1: Oscillator Comparison [23]

	XO	TCXO	OCXO	LC Oscillator
Price [$]	< 1	$\sim$2	$\sim$100	$\sim$0
Frequency [MHz]	24	20	10	$10 - 10^4$
Accuracy [ppm]	$\sim$50	$\sim$1	< 0.01	$\sim 10^4$
Sensitivity [ppm/$^\circ C$]	$\sim$0.5	$\sim$0.01	$< 10^{-4}$	$\sim$100
DC Power [mw]	$\sim$40	$\sim$20	$\sim$300	$\sim$10
Size [cm^3]	< 1	< 1	8	$\sim$0

replacements for accurate and stable XTALs [80]. Radio frequency microelectro-mechanical (RF MEMS) resonators [81] and film bulk acoustic resonators (FBARs) [82] provide the high quality frequency references and have been used in RF frequency designs. However, they cannot be integrated in standard CMOS technology, which results in more complexity and higher cost [83].

Wireless sensor nodes (WSNs) demand ultra-low-power, small size, low cost radios, and frequency accuracy of approximately 1% [84, 85]. Therefore, costly XTALs can be replaced with less expensive CMOS frequency generators. In some applications, a modest frequency accuracy ($\pm 500 ppm$) and phase noise can be accommodated [83], but this is not a general purpose solution. Replacing both the XTAL oscillator and PLL with a single CMOS oscillator offers lower power consumption due to faster startup time and lower complexity, compared to the traditional synthesizers, and reduces the manufacturing cost.

LC oscillators exhibit more than 100 $ppm/°C$ frequency drift [17]. The temperature variation can be compensated through sensing the temperature and changing the capacitance of the LC tank of the oscillator to keep the frequency within the desired range [83]. Figure 5.1 shows a simple block diagram for a calibration path to compensate the temperature variation [17]. Compensating an oscillator with a high temperature sensitivity requires complicated and power hungry calibration. The effective number of bits (ENOB) of the ADC increases for an oscillator with higher temperature sensitivity. An LC oscillator with a low temperature sensitivity would be highly desired.

In Section II, we review prior attempts to develop low temperature sensitivity in CMOS reference frequency generators and study the temperature behavior of the LC tank. In Section III, we briefly review previous series coupled quadrature oscillators (S-QOSCs) and explain how the temperature sensitivity of these designs can be reduced. Finally, Section IV reviews the measurement results confirming the temperature sensitivity difference between two modes of quadrature oscillation.

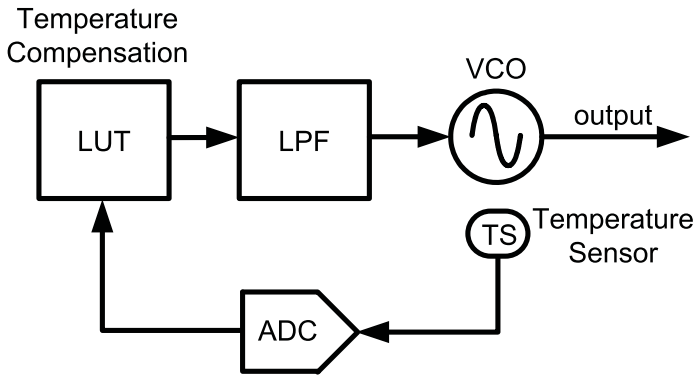

Figure 5.1: Simplified VCO system with calibration path to compensate for temperature variation [17].

5.1 Temperature Compensation in LC Oscillators

Michael [83] replaced the XTAL and phase-locked loop for clock generation in an IC supporting USB 2.0 using a CMOS fabrication process. In this approach, a standard differential LC oscillator is utilized and I_{PTAT} and I_{CTAT} current sources bias the accumulation varactors with either a temperature-dependent or temperature-independent voltage to compensate the frequency drift. With increasing temperature, the free-running frequency of the CMOS oscillator typically decreases and so the varactor control voltage must reduce the tank capacitance and keep the frequency constant.

More recently, Ahmed [17] proposed a quadrature oscillator with low sensitivity to temperature variation. Following this analysis, Fig. 5.2 shows a parallel LC tank with series resistance R_L and R_C representing loss of L and C, respectively.

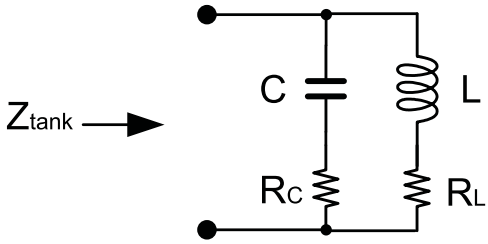

Figure 5.2: Parallel LC tank with series resistance R_L and R_C representing loss of L and C, respectively.

By assuming that $R_C << R_L$ [83], the resonance frequency of the tank is

$$\omega_{res} \approx \omega_o \sqrt{1 - \frac{CR_L^2}{L}} \approx \omega_o(1 - \frac{1}{2Q^2}). \tag{5.1}$$

where $Q = \frac{L\omega_o}{R_L}$ and $\omega_o = \frac{1}{\sqrt{LC}}$. The phase of Z_{tank} can be approximated as

$$\varphi_{tank} = \angle Z_{tank} \approx tan^{-1}(\frac{\omega L}{R_L}) - tan^{-1}(\frac{\omega R_L C}{1-\omega^2 LC}) \tag{5.2}$$

Groves [86] analyzed monolithic spiral inductors and showed that L (and C) are largely independent of temperature and bias and R_L is the only temperature dependent parameter in (5.1) and is modeled as a linear change in resistance,

$$R_L(T) = R_o(1 + \alpha(T - T_o)) \tag{5.3}$$

where R_o is the loss of inductor at T_o and α is the temperature coefficient of R_L [17].

Figure 5.3 shows the calculated phase of the LC tank impedance (L=$0.8nH$, C=$1.2pF$, and Q=6) as a function of frequency for three different temperatures. Increasing the temperature increases R_L decreases the Q of the tank, and reduces the phase slope.

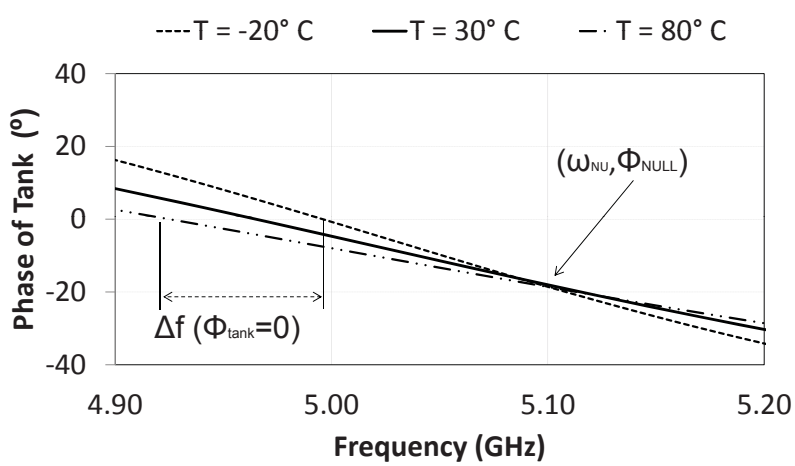

Figure 5.3: Simulated phase of LC tank impedance at different temperatures (L=$0.8nH$, C=$1.2pF$, and Q=6).

If the oscillation occurs at $\varphi_{tank} = 0$, the frequency decreases with increasing temperature from -20^oC to 80^oC. In Fig. 5.3 the different curves intercept at one phase, φ_{NULL}, where

the oscillation frequency is insensitive to temperature variation:

$$\frac{d\omega}{dT}|_{\varphi_{NULL}} \approx 0 \tag{5.4}$$

For phases less than φ_{NULL}, the frequency increases when the temperature rises ($\frac{d\omega}{dT} > 0$) while for phases greater than φ_{NULL}, $\frac{d\omega}{dT} < 0$. Prior work recognized that if a parallel LC quadrature oscillator ($P-QOSC$) oscillates at φ_{NULL}, the frequency drift due to temperature is minimized [17]. Figure 5.4 shows the block diagram of the parallel quadrature oscillator.

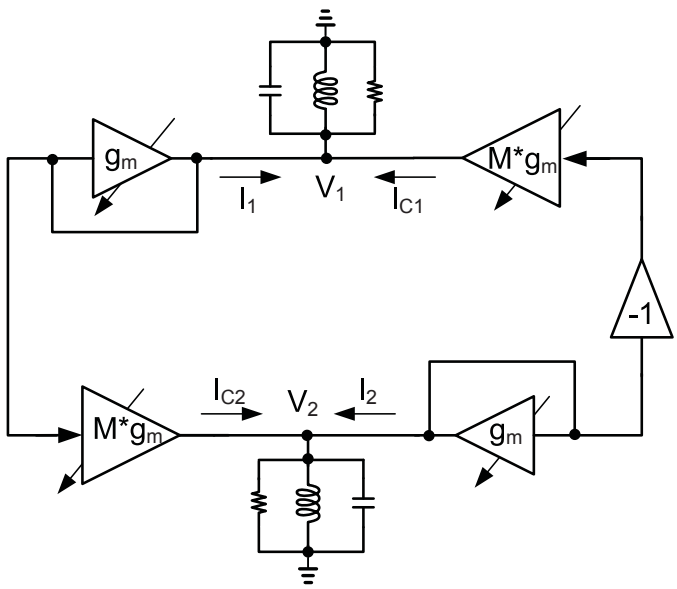

Figure 5.4: Block diagram of a parallel quadrature oscillator (P-QOSC) [17].

The phase of oscillation is determined by ratio $M = I_{c1}/I_1$ ($M = I_{c2}/I_2$) where I_1 and I_{c1} are regenerative and coupling current going to LC tank. Ahmed showed that oscillator frequency occurs under the condition that $\varphi_{osc} = tan^{-1}(M)$ [17], which can be set to the minimum temperature sensitivity point, φ_{NULL}. The value of M is determined by device sizes and

bias current, I and I_c, which represent the regenerative and coupling bias currents, respectively. If temperature varies, both regenerative devices and coupling devices follow each other which guarantees a coupling ratio, M, independent of temperature variation.

However, the order of the quadrature sequence is not determined with this quadrature approach. Generally, LC quadrature oscillators can operate in two different modes with different I-Q sequences, slightly different frequencies, and different tuning ranges [78, 18, 64]. There is no guarantee that the oscillation occurs at φ_{NULL} and instead it may settle at $-\varphi_{NULL}$ ($|\varphi_{osc}| = tan^{-1}(M)$), where the frequency will be highly sensitive to temperature variation.

5.2 Temperature Sensitivity of Series Quadrature Oscillator

The concept governing low-temperature sensitivity in oscillators is based on seeking modes of oscillation that are determinant and satisfy φ_{NULL} over a wide range of temperatures. We propose that the series quadrature oscillator (S-QOSC) shown in Fig. 5.5 and proposed in [78] and [18] has low temperature sensitivity and non-degenerate modes that can produce a determinant phase sequence.

The two modes in the S-QOSC are non-degenerate when capacitor C_5 shown in Fig. 5.5 is added to the circuit. Increasing C_5 favors Mode 1 of the quadrature oscillation (I leads Q in Fig. 5.5) which has a higher frequency. Inserting capacitor C_4 favors Mode 2 (Q leads I) and results in a slightly lower oscillation frequency. For an optimum value of C_4, prior analysis shows that only Mode 2 satisfies oscillation start-up conditions [78]. Switching OFF $SW4$, forces the effective C_4 to be $zero$ and C_5 ensures Mode 1 is dominant.

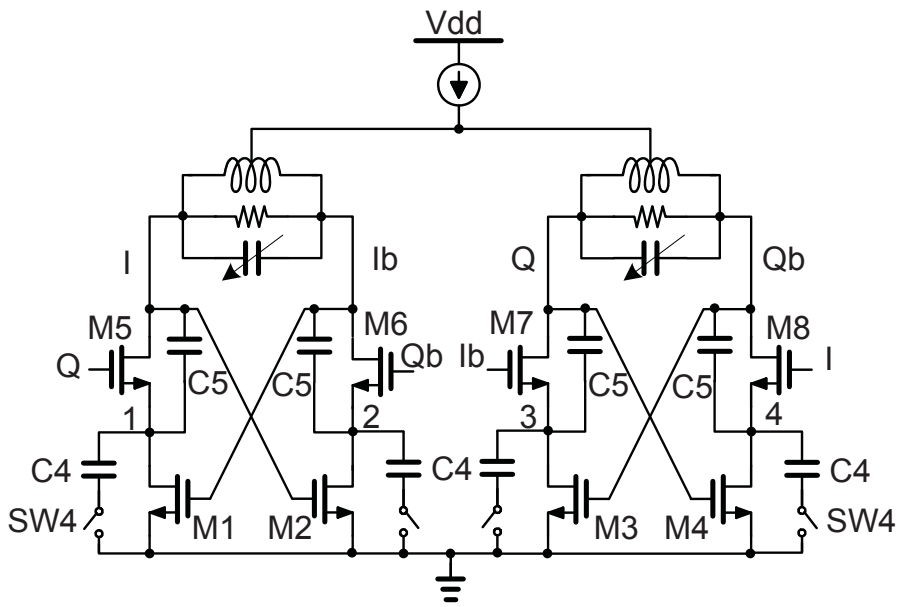

Figure 5.5: The $S-QOSC$ oscillates selectively in desired mode of quadrature oscillation. [18]

To minimize the frequency drift due to temperature variation in S-QOSC, the analysis considers the temperature dependence of the LC tank and the active part of the S-QOSC, separately.

5.2.1 LC Tank Temperature Behavior

By using the the same tank in Fig. 5.2 and assuming that R_C is negligible, the phase response of the tank will be

$$\varphi_{Tank} \approx tan^{-1}(\frac{\beta}{R_L}) \tag{5.5}$$

where $\beta = CR_L^2\omega + CL^2\omega^3 - L\omega$. By using (5.3),

$$\frac{d\varphi_{tank}}{dT} = \frac{d\varphi_{tank}}{dR}\frac{dR}{dT} = \frac{\gamma}{R_L^2 + \beta^2}(\alpha R_{Lo}) \tag{5.6}$$

where $\gamma = CR_L^2\omega - CL^2\omega^3 + L\omega$. The frequency with minimum temperature sensitivity is ω_{NULL} and can be found by setting $\frac{d\varphi_{tank}}{dT} = 0$.

$$\omega_{NULL} \approx \omega_o(1 + \frac{CR_L^2}{2L}) \approx \omega_o(1 + \frac{1}{2Q^2}) \tag{5.7}$$

5.2.2 Impedance Behavior of Active Devices

The complex admittance looking into the drain of M5/M6 (or M7/M8) in Fig. 5.5 also plays a role in the temperature sensitivity. The oscillation condition ideally occurs at ω_{NULL}. The real part of the admittance (g_{d5}) is [78]

$$G_{d5} = \frac{\epsilon \pm \zeta}{(g_{m2} + g_{ds})^2 + (\omega \sum_{i=2}^{5} C_i)^2} \tag{5.8}$$

where

$$\epsilon \approx -(g_{m2} + g_{ds})(g_{m1}.g_{m2} - (\omega C_2)^2 - \omega^2(C_5 - C_3)^2)$$
$$-\omega^2(\sum_{i=2}^{5} C_i)(g_{m2}(C_2 + C_5 - C_3) - g_{m1}(C_5 - C_3)) \tag{5.9}$$

and

$$\zeta \approx -g_{m1}\omega C_2(g_{m2} + g_{ds})$$
$$+g_{m2}g_{ds}\omega(C_2 + C_5 - C_3) - (g_{m2})^2\omega(C_3 + C_4) \tag{5.10}$$

C_4 and C_5 are explicitly added to select the mode of quadrature oscillation [64, 18, 78]. C_3 is the C_{gd} of $M1$, C_1 and C_2 are the C_{gd} and C_{gs} of transistor $M5$, respectively. For simplification the junction capacitor (C_{jd}) at the drain of M5 has been absorbed in the LC tank. Other intrinsic and parasitic capacitances of transistors are absorbed in C_4 and C_5.

The imaginary part of admittance looking into drain of M5 is [78]

$$B_{d5} \approx \frac{\pm g_{m2} g_{ds}(g_{m2} + g_{ds})}{(g_{m2} + g_{ds})^2 + (\omega \sum_{i=2}^{5} C_i)^2} \tag{5.11}$$

The oscillation frequency is found by placing the LC tank in parallel with B_{d5}

$$B_{d5} + C\omega - \frac{Q^2}{L\omega(1 + Q^2)} = 0 \tag{5.12}$$

where L has been replaced by its parallel equivalent. Solving for ω yields

$$\omega_{osc} \approx -\frac{B_{d5}}{2C} + \frac{1}{2}\sqrt{(\frac{B_{d5}}{C})^2 + 4\omega_o^2(1 - \frac{1}{Q^2})} \tag{5.13}$$

The ω_{osc} achieved from (5.13) should be equal to ω_{NULL} from (5.7) to have the minimum sensitivity to temperature variation. In (5.11) B_{d5} is a function of g_{m1}, g_{m2}, g_{ds}, C_4, and C_5. Therefore, by changing C_4, B_{d5} can be adjusted to make the oscillator frequency equal to ω_{NULL} in Mode 1.

Equations (5.11) and (5.13) show that Mode 2 (the $+$ in $\pm$ sign) oscillates below ω_o while Mode 1 oscillates above ω_o. Therefore, Mode 1 is preferred to produce an oscillation at ω_{NULL}.

When the oscillator operates in Mode 1, the frequency of oscillation is ω_{NULL}. At the start-up of the oscillation, C_4 should be OFF (zero) to make Mode 1 the dominant mode (not Mode 2 with $\omega < \omega_o$). After starting the oscillation, the optimized C_4 will be switched into the circuit. Mode 1 is a stable mode of oscillation and adding C_4 only affects the phase and frequency of oscillation, not the mode of oscillation. It would be part of the sequences of the start up of the system. Further calibration could be done by fine tuning of the bias current to achieve the optimum behavior.

5.3 Circuit Implementation

$SpectreRF$ simulation was used to verify the temperature behavior of the quadrature oscillator. Table 5.2 shows the parameters of the simulated $S - QOSC$. By starting the oscillation in Mode 1 ($C_4 = 0$) then switching C_4 into the circuit, the sensitivity of oscillation to temperature variation is minimized.

Fig. 5.6 shows the simulated oscillation frequency as a function of temperature for two modes. The frequency of oscillation in Mode 1 is approximately constant while in Mode 2 frequency decreases sharply.

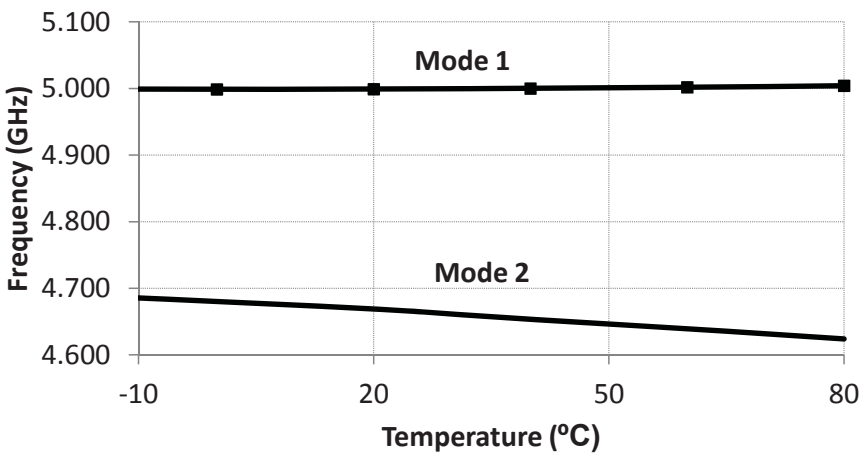

Figure 5.6: Simulated oscillation frequency in Mode 1 and Mode 2 of quadrature oscillation versus temperature.

Figure 5.7 shows simulation results for two different bias currents of 7mA and 8mA in Mode 1. For Ibias=7mA, the minimum sensitivity occurs at $T = 0\ ^\circ C$ while for Ibias=8mA it occurs at $T = 40\ ^\circ C$. (5.7) shows the ω_{NULL} for a limited range of temperature. For temperature range of T_1 to T_2, $\omega_{NULL,12}$ happens at T_{12} ($T_1 < T_{12} < T_2$). For higher temperatures of T_2 to T_3, $\omega_{NULL,23}$ happens at $T_{23} > T_{12}$. The $\varphi_{NULL,12}$ and $\varphi_{NULL,23}$ are different too. By increasing

the $Ibias$ of the oscillator, the phase of active part changes slightly and T_{NULL} moves. Also the junction capacitor of M5, C_{jd}, increases which results in a slight variation of the oscillation frequency. The combination of the variation in LC tank and active part results in different T_{NULL} and ω_{NULL} for different Ibias (Fig. 5.7).

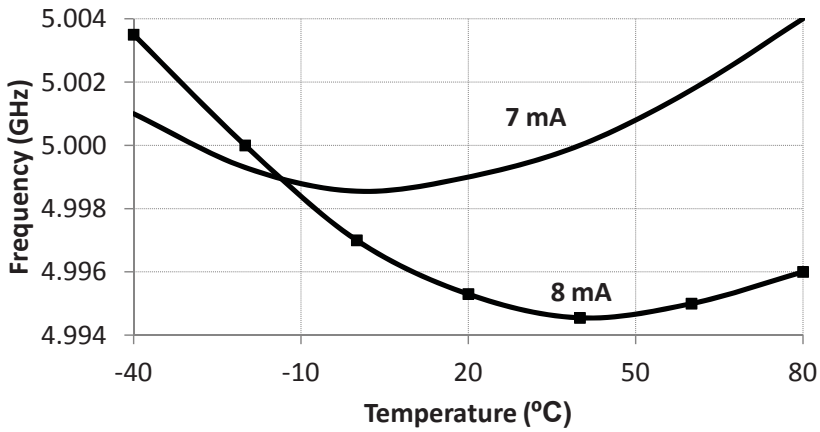

Figure 5.7: Simulated oscillation frequency in Mode 1 of quadrature oscillator versus temperature for Ibias=7mA and Ibias=8mA.

Simulation results shows that phase noise has a small variation of 2 dB over the temperature range of -20 $°C$ to 80 $°C$ for both modes of quadrature oscillation. In [78] we have analyzed the effect of different noise contributors on the phase noise performance. Simulation also shows that $SW4$ is not a main contributor in phase noise.

Table 5.2: Circuit parameters for the proposed QOSC

f_o	M1	M5	C_4	C_5	L_t	C_t
5 GHz	120 um	240 um	800 fF	860 fF	0.8 nH	1.2 pF

5.3.1 Measurement Results

The microphotograph of the fabricated chip in IBM 90-nm CMOS technology is shown in Fig. 5.8.

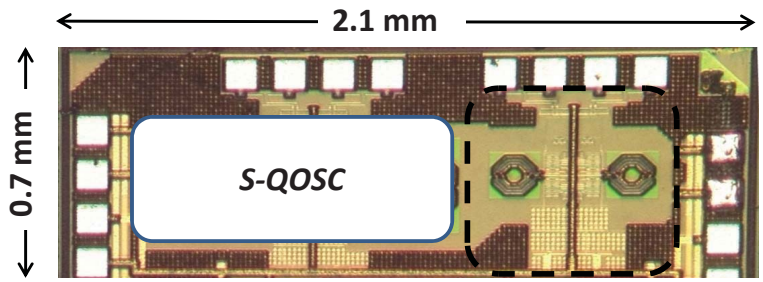

Figure 5.8: Microphotograph of the fabricated chip in IBM 90-nm CMOS technology.

The measured frequency variation as a function of temperature for Ibias=7mA and Ibias=8mA is shown in Fig. 5.9. In setting of $I_{bias} = 7mA$, the frequency is within 1 MHz around center frequency of 5.020 GHz for temperatures from $0\ ^{\circ}C$ to $30\ ^{\circ}C$. The oscillation frequency for $I_{bias} = 8mA$ from $10\ ^{\circ}C$ to $60\ ^{\circ}C$ is within 1 MHz. By combining the two current settings the variation can be bounded over the range of $\pm 10ppm/^{\circ}C$. Therefore, the oscillation frequency shift (for example 5.02GHz) is maintained to under 1 MHz with only a few adjustments which gives us $\pm 100ppm$ for temperature variation of zero to $T = 60\ ^{\circ}C$. By keeping the variation in this range, a look-up table (LUT in Fig. 5.1) for fine tuning will help to adjust the frequency within ppm accuracy.

The measured oscillation frequency and frequency variation as a function of temperature in Mode 1 is also shown in Fig. 5.10.

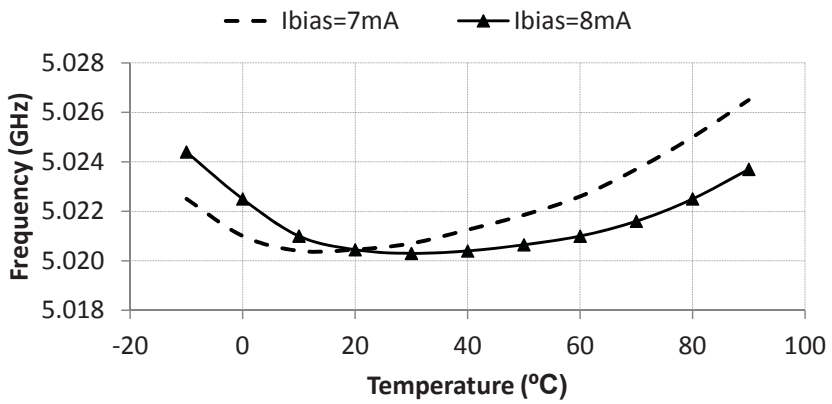

Figure 5.9: Measured oscillation frequency as a function of temperature for two different bias setting in Mode 1 of quadrature oscillation

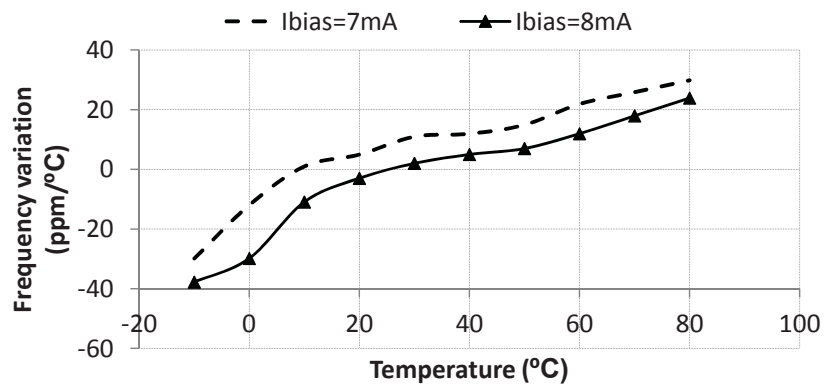

Figure 5.10: Measured oscillation frequency and its variation as a function of temperature in Mode 1 of quadrature oscillation

The measured oscillation frequency and frequency variation as a function of temperature in Mode 2 is also shown in Fig. 5.11. The sensitivity of oscillation in Mode 2 is around $-150ppm/°C$ which is much higher than Mode 1.

The measured phase noise at frequency of $5GHz$ with optimum setting of frequency accuracy is $-118dBc/Hz$ at $1MHz$ offset frequency. The current consumption is $8mA$ from a power supply of $1.2V$.

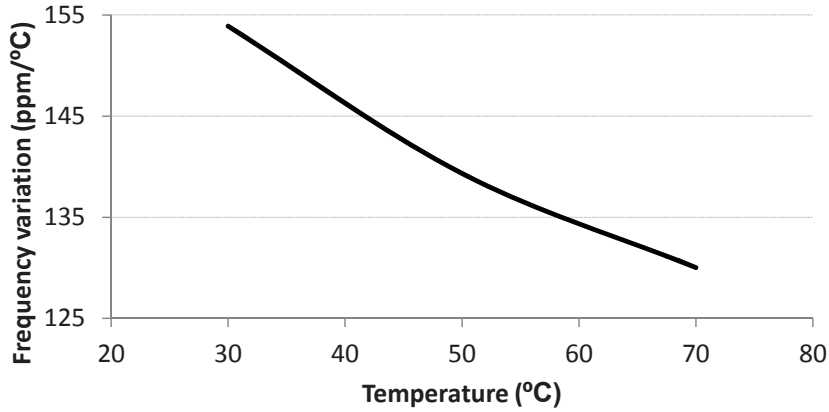

Figure 5.11: Measured oscillation frequency and its variation as a function of temperature in Mode 2 of quadrature oscillation

5.3.2 Comparison to the State-of-the-Art

Table 5.3 shows the different reference frequency generators which are $CMOS$ compatible in different process technologies. The new figure-of-merit, $FOM - Temp$, which includes the frequency sensitivity in ppm and temperature range of operation (ΔT) is introduced to compare the different works:

$$FOMT = FOM + 10\log\left(\frac{\Delta T}{Sensitivity}\right) \tag{5.14}$$

where sensitivity is frequency variation in ppm and FOM is the conventional figure-of-merit of oscillators defined as [54]:

$$FOM = 10\log\left(\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{L(\Delta f)P}\right) \tag{5.15}$$

Notably, this work matches the best FOM at an RF frequency.

Table 5.3: Comparison To State-of-the-Art References

	Freq.	FOM	ΔT	Sensitivity	FOM-Temp
	Hz	dB	$^{\circ}C$	ppm	dB
[87] (RC)	6M	172	120	8.8k	153
[85] (Relax)	70k	NS[1]	120	4k	-
[88] (Ring)	0.7M	NS[1]	80	47k	-
[89] (Ring)	24-80M	NS[1]	190	0.6-1.4k	-
[90] (Mobility)	100K	NS[1]	110	10k	-
[91] (Relax.)	1.2M	136	120	18k	113
[92] (Relax.)	2M	NS[1]	120	25k	-
[83] (LC)	48M	180	95	200	177
[17][2] (LC)	125M	150	70	100	149
[93] (LC)	62.5M	NS[1]	145	80	-
[94] (Ring)	4G	136	120	12k	116
This Work (LC)	5G	182	60	200	177

[1]Not specified. [2]Includes the chain of dividers

5.4 Summary

CMOS reference frequency generators are discussed, which can potentially replace XOs in applications with a low frequency accuracy requirement. A modified S-QOSC has been proposed and analyzed, which shows a reduced temperature sensitivity. Measured results at frequency of 5 GHz show $\pm 100ppm$ frequency accuracy over 0^oC to 60^oC which can be improved over wider temperature range by calibration.

This chapter, in parts, is a reprint of the material as it is appears in IEEE Transactions on Circuits and Systems II, 2018 [24]. The dissertation author was the first author on that publication. I would like to thank the other authors in this publication, Dr. Rahim Bagheri, Prof. James Buckwalter, and Prof. Lawrence Larson for their contribution and support in publishing this paper.

Chapter 6

Wideband Injection-locked Oscillator for E-band Application

Different communication systems take advantage of millimeter-wave phased arrays such as 60 GHz short-range communication and point-to-point communication at the $E-$band (71-76 and 81-86 GHz) and the $W-$band (75-110 GHz) [95, 96, 97, 98, 99, 100]. LO phase shifting is one of few architectures for scalable phased arrays [95, 98] which avoids loss and noise in the RF signal path and is well suited for bidirectional operation [19]. LO phase shifter proposed by [101] utilizes a central multiphase VCO that generates discrete phase states distributed to each array element at the cost of area and power consumption and limited number of distributed phases. Injection-locked oscillators were proposed at CMOS as a low-power alternative to LO phase shifting [102] and injection-locked oscillator (ILO) is the source of phase shift. ILO-based phase shifting has technical challenges at high frequency applications like millimeter-wave bands due to tradeoffs between phase noise and parasitic capacitances of the injection

circuitry. In this chapter we present injection-locked VCOs operating at 15.5 to 18.2 GHz which will be used by a following multiplier by 4 to provide frequency range of 62-72.8 GHz. This wideband injection-locked VCO has been utilized in 71 to 86 GHz phased array tranceiver. The main advantage of this LO phase shifting is the low frequency phase shifting and distributing the low frequency signal across the chip and multiplying inside the transceiver element. By this the LO tuning range is also multiplied (the fractional bandwidth is constant) and provide wider coverage. Also the pulling from power amplifier will be avoided [19].

6.1 Scalable LO-shifting Transceiver

The block diagram of a four-element bidirectional phased array proposed in [19] is shown in Figure 6.1. Four VCOs are locked to an external reference in this heterodyne transceiver and provide phase shifting through injection locking. VCOs operate at frequency range of 15.5 to 18.2 GHz and multiplied by four to cover a broader range of 62 to 72.8 GHz which also results in a wider phase shift.

The wideband mixers are driven by IF and LO signals shown in Figure 6.2 and output of the mixers is the E-band RF signal at 71 to 76 GHz and 81 to 86 GHz for lower LO signal band and upper band LO signal, respectively.

In the next section the injection-locked oscillator which has been utilized in this transceiver will be studied.

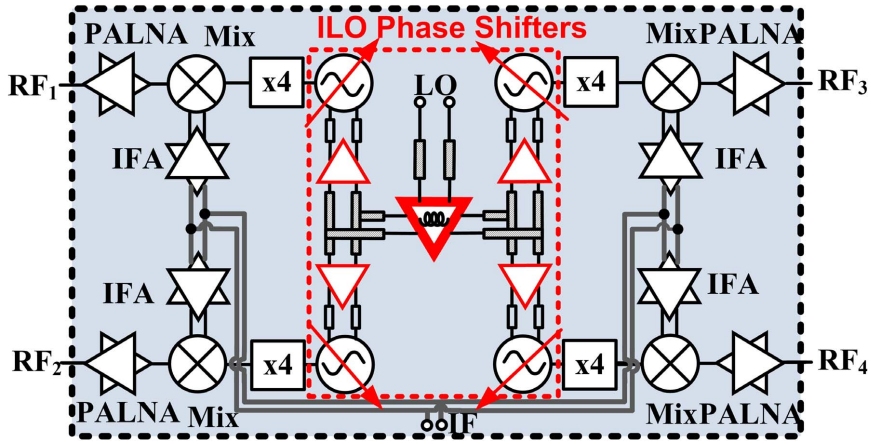

Figure 6.1: The block diagram of the 2x2 bidirectional LO-path phased array [19].

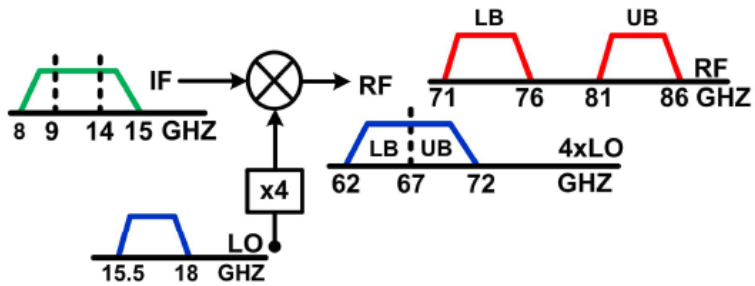

Figure 6.2: Frequency planning of the $E-$band system [19].

6.2 Injection-locked Oscillator Phase Shifting

Fig. 6.3 shows the simplified model of an LC oscillator under injection [20, 19]. The natural oscillation frequency, at $I_{inj} = 0$ is

$$\omega_0 = 1/\sqrt{LC} \tag{6.1}$$

where L and C are the tank inductance and capacitance, respectively. By injecting a

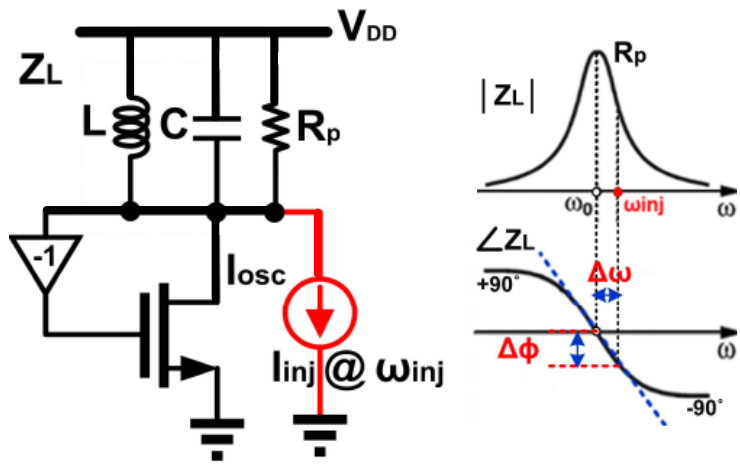

Figure 6.3: Simplified model of an LC oscillator under injection [20].

current, I_{inj}, at frequency of $\omega_{inj} \neq \omega_0$, the oscillator frequency will be pulled to ω_{inj} under some conditions. The amount phase shift, $\Delta\Phi$, due to locking to the injected signal, is a function of quality factor of the LC tank, Q, the frequency difference of $\Delta\omega$, and the ratio of the injected current to the oscillator current, I_{inj}/I_{osc} [20, 19] as following

$$\Delta\Phi = arcsin[2Q \times \frac{\Delta\omega}{\omega_0} \times \frac{I_{osc}}{I_{inj}}] \tag{6.2}$$

and the locking range of the oscillator to the injected frequency is

$$\omega_L = \frac{\omega_0}{2Q} \times \frac{I_{inj}}{I_{osc}} \tag{6.3}$$

To increase the locking range either Q should be reduced, or I_{inj} should be increased. The former, results in phase noise degradation and usually is not an option. The latter can be done by increasing the size of injection transistors at the cost of extra parasitic capacitors, which by itself, degrades the tuning range of the ILO.

The linear phase shift can be achieved by Taylor series of (6.2) as

$$\Delta\Phi = \frac{\Delta\omega}{\omega_L} + \frac{1}{6}(\frac{\Delta\omega}{\omega_L})^3 + ... \tag{6.4}$$

The range of linear phase shift can be derived by bounding the third-order term of (6.4) to a boundary deviation. Therefore, by setting the deviation from the linear region, $\Delta\omega$ can be found and by using (6.2). For a typical locking range of around 10% of the nominal frequency, Q of 10, and I_{inj}/I_{osc} of 0.5, to achieve 30° linear phase shift, the frequency variation is around 5%. To achieve more linear phase shift frequency multiplier should be used to cover the desired phase shift of $360\circ$ in a phased array.

The other requirement in addition to linear phase shift is to have an oscillation with a constant amplitude over the range of the frequency since amplitude variation affects the conversion gain and degrades the peak-to-null ratio of array pattern [19].

6.3 Circuit Implementation of ILO Phase Shifter

The proposed ILO phase shifter consists of oscillator core and injection circuitry is shown in Fig. 6.4. The injection signal drives the M_4 devices differentially. The drain current of the M_4, ac coupled injection current, goes to common-gate PMOS transistors the M_2 devices. The M_3 devices are to bias the M_2 devices. By using this configuration, the parasitic of the injection circuit is minimized at the injection nodes of oscillator, $Out+$ and $Out-$.

The schematic of the oscillator core is shown in Fig. 6.5. The frequency tuning range of oscillator is 16.5-19.8 GHz corresponding to 21%. Four bits of metal-insulator-metal (MIM) ca-

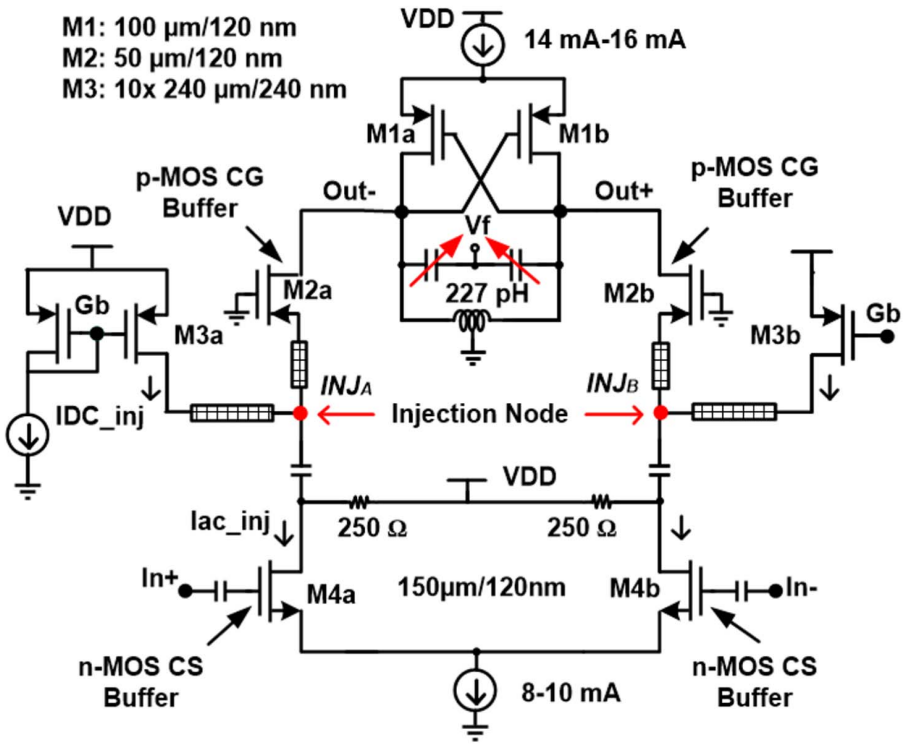

Figure 6.4: ILO phase shifter; oscillator core and injection circuitry [19].

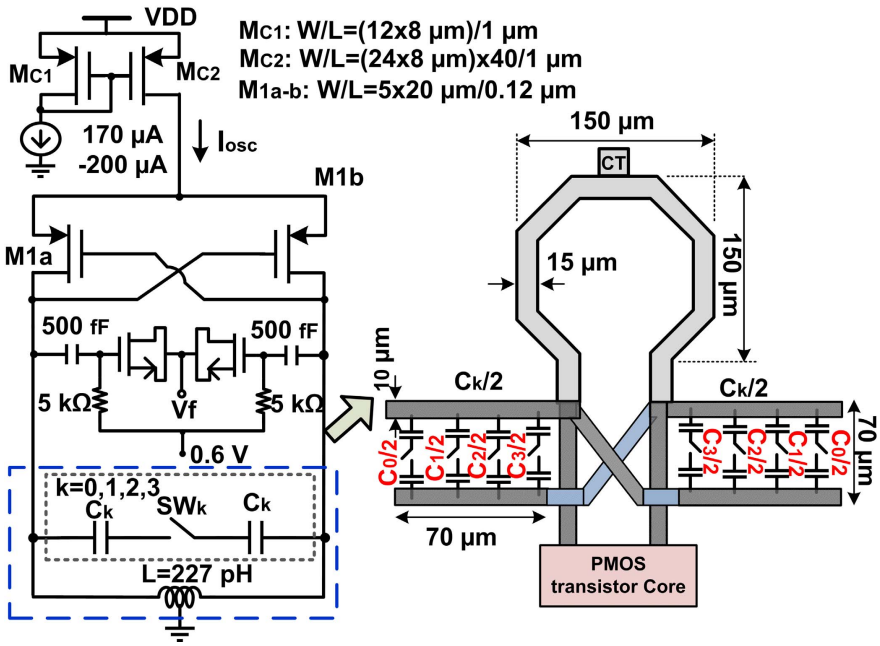

Figure 6.5: Schematic of oscillator core and layout illustration of LC tank [19].

pacitors have been used for coarse tuning which offer around 3 $fF/\mu m^2$ density, Q of around 25, and C_{max}/C_{min} of 3. Main inductor is 270 pH. The routing parasitic capacitance and inductance are minimized by the proper placement of the elements as shown in Fig. 6.5. The capacitors are placed in a way that the bigger ones are closer to inductor to maximize energy transfer to the inductor. The varactors are controlled by an analog voltage from 0 to 1.2 V to provide phase shifting by detuning the tank resonance frequency and frequency tuning. The varactor covers 300-350 MHz which is around twice the LSB of coarse tuning (120-180 MHz).

The simulated transient response of the proposed ILO phase shifter for different varactor voltages is shown in Fig. 6.6. In this simulation, the LO is locked to the external source at -10 dBm power and 19.3 GHz. The coarse tuning is set to zero. By tuning the varactors the

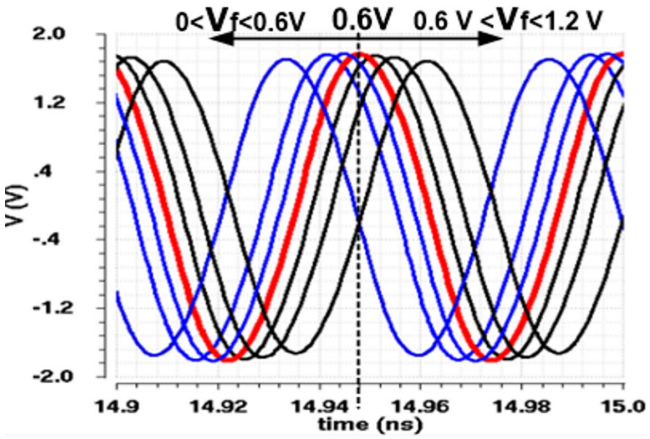

Figure 6.6: Simulation results of ILO phase shifter using SpectreRF [19].

frequency detuning happens and $\Delta\Phi$ of 50° is resulted with less than 10% amplitude mismatch.

Fig. 6.7 (a) shows the phase shift simulation results of proposed ILO phase shifter at 19.3 GHz as a function of $\Delta\omega$ for different values of I_{inj}/I_{osc} using parasitic extraction and EM simulator. Amplitude variation as a function of $\Delta\omega$ for different values of I_{inj}/I_{osc} is shown in Fig. 6.7 (b) [19]. Simulation results show a 300 MHz locking bandwidth with $\pm 50^o$ phase shift and less than 0.5 dB amplitude variation for I_{inj}/I_{osc} of 0.5.

6.4 Measurement Results

The RF port of each element of Fig. 6.1 is probed for characterization of the ILO performance under free-running and locked condition. The measured tuning range is from 15.5 to 18.2 GHz as shown in Fig. 6.8. The LSB of coarse tuning is 140 MHz and 170 MHz for low-frequency band (LB) and high-frequency band (HB), respectively. The varactor tuning range is

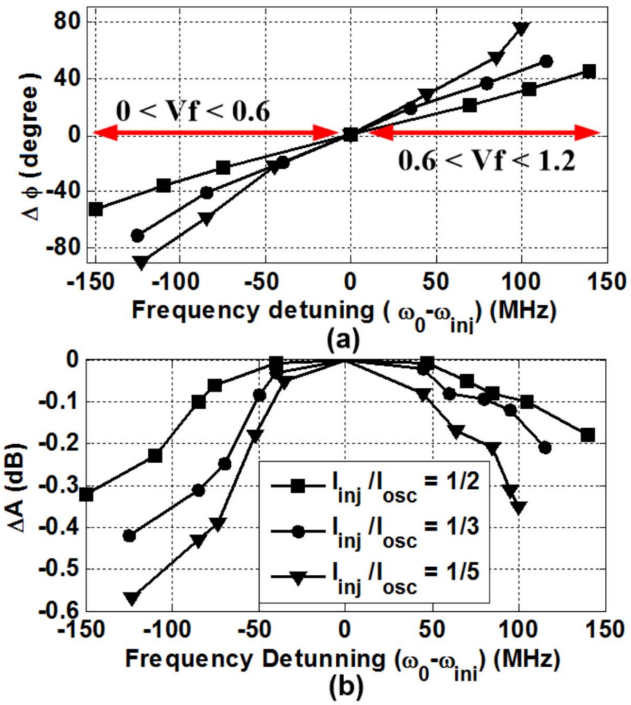

Figure 6.7: Simulation results of proposed ILO phase shifter at 19.3 GHz using parasitic extraction and EM simulator (a) Phase shift as a function of $\Delta\omega$ for different values of I_{inj}/I_{osc} and (b) Amplitude variation for different values of I_{inj}/I_{osc} [19].

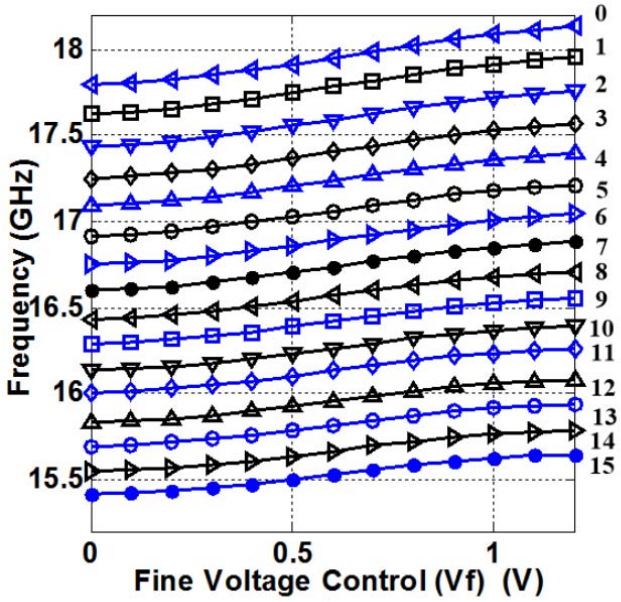

Figure 6.8: ILO measurement of free-running tuning range [19].

280 and 350 MHz for LB and HB, respectively.

The locking range is also shown in Fig. 6.9 for LO injected power of 3 dBm. Average locking range is around 220 MHz which is close to simulation results of 300 MHz.

The ILO phase shifter measured transient response from oscilloscope for single element locked at f_{inj}=16.5 GHz under different phase shifts is shown in Fig. 6.10. The down-converted signal is captured with a real-time oscilloscope (DSO80604b) and compared with a reference signal as a trigger.

The measured phase shift and amplitude variation under 3-dBm injection power are shown in Fig. 6.11. The amplitude variation is under 1 dB and the phase shift range is $\pm 300^o$ as the ILO is detuned over the locking range.

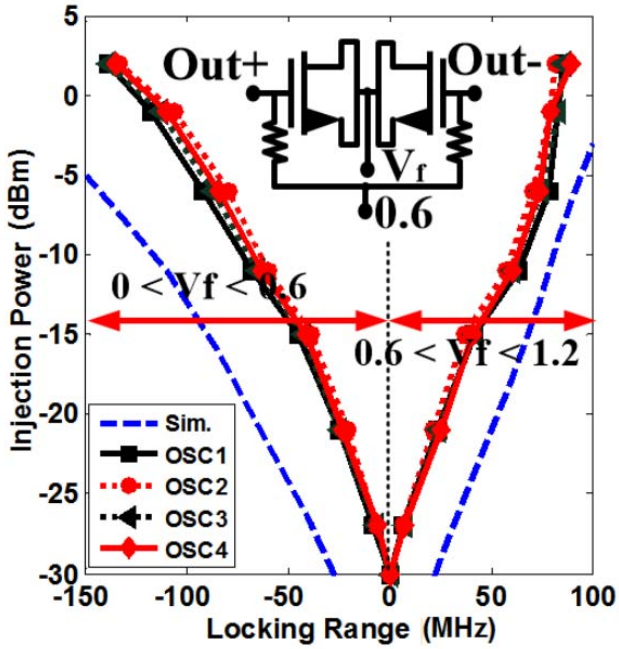

Figure 6.9: ILO measurement of locking range [19].

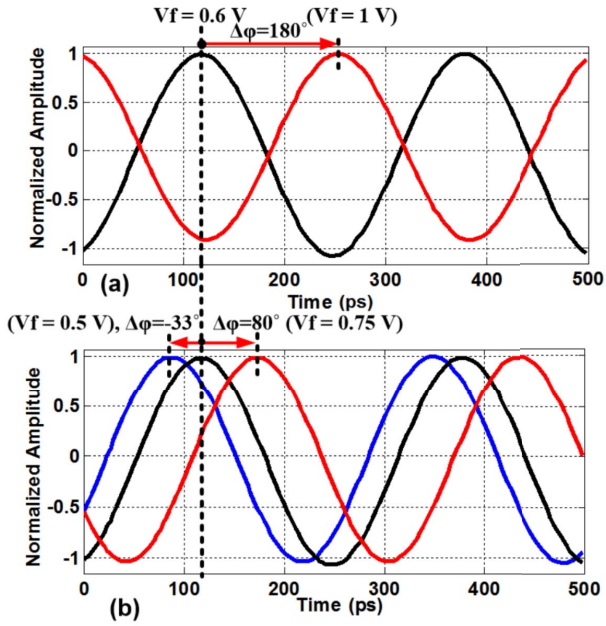

Figure 6.10: ILO phase shifter measured transient response from oscilloscope for single element locked at f_{inj}=16.5 GHz under different phase shifts of (a) $+180^o$, and (b) -330° and $+80^o$ [19].

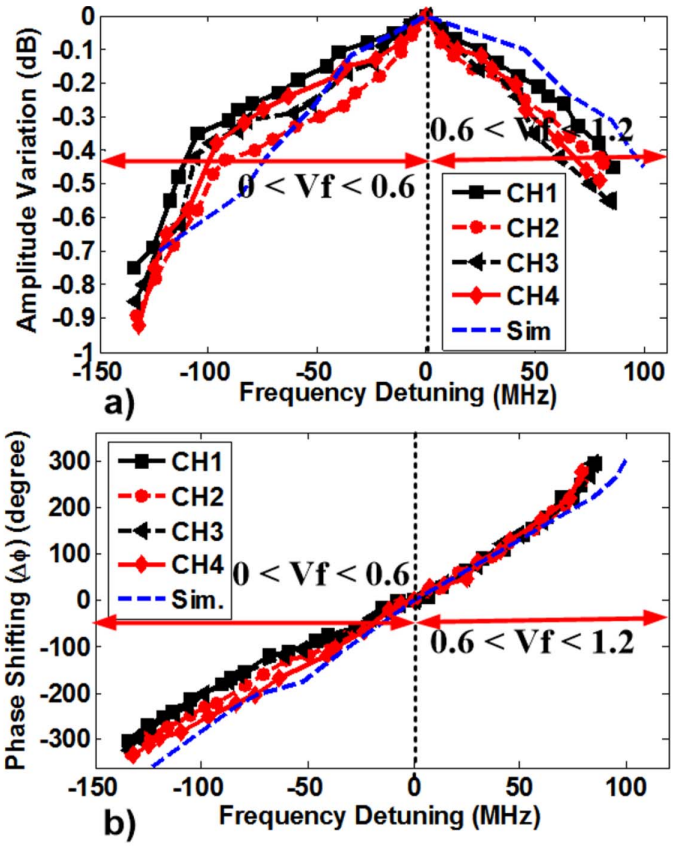

Figure 6.11: Measured result of ILO phase shifter [19]. (a) Amplitude variation as a function of $\Delta\omega$. (b) Phase shift as a function of $\Delta\omega$.

6.5 Summary

In this chapter an LO-phase shifting approach based on ILO at frequency range of 71 to 86 GHz is presented. The implemented oscillators operate at one-fourth of required LO tuning range and provides a power-efficient solution for scalable mm-wave phased array. The measured locking bandwidth of ILO is 250 MHz and phase shift range is ± 300 with less than 1 dB amplitude variation.

This chapter, in parts, is a reprint of the material as it has been published IEEE Transactions on Microwave Theory and Techniques, 2017 [19] and IEEE Symposium on Radio Frequency Integrated Circuits (RFIC), 2017 [25]. I would like to thank the other authors in these publications, Prof. James Buckwalter, Dr. Najme Ebrahimi (first author of these publications), and Dr. P. Wu for their support and contribution in above published papers.

Chapter 7

Conclusion

The timing requirement and spurious performance in UWB transceivers are the major challenges in design of frequency synthesizers. The agile settling of UWB in switching between different bands which should be less than 9.2 ns requires the new techniques rather than conventional PLL based frequency synthesis. Also, the limitation on the frequency spectrum forces the UWB transceiver and its frequency synthesizer to improve the spurious performance and meet the regulatory mask assigned by different organizations in different parts of the world. The different available band frequency in different countries also forces the design of the frequency synthesizer to cover the entire band from 3.1 GHz to 10.6 GHz resulting in a universal solution. This universal 14 band solution should be flexible and low power to be successfully utilized in wireless applications such as WUSB and WPAN. Quadrature signals are essential part of all modern transceivers and this UWB synthesizer. One way of quadrature signal generation is to use LC quadrature oscillators. Common type of these oscillators suffer from random sequence of quadrature output which not only introduce some difficulty in mixer, PLL, and divider op-

eration, but also it might $zero$ the effective tuning range of the oscillators. Therefore, there is a need to fix the phase ambiguity in LC quadrature oscillators. Also, to reduce the number of oscillators in UWB and multi-band radios, wider tuning range of oscillators has a big advantage and tuning range enhancement of quadrature oscillator will be very important. Finally, replacing the external crystal (XTAL) oscillators by on-chip CMOS frequency generators, which is less expensive and less power hungry, require an stable oscillator with different accuracy for different applications. Therefore, a CMOS solution for reference frequency generation is desirable to reduce the complexity of the systems by replacing XTALs with tiny footprint CMOS oscillators.

Therefore, in this dissertation the focus is on

- Proposing an architecture for fast hopping frequency synthesizer for UWB that can operate in whole spectrum of WiMedia UWB and implementing in standard CMOS technology.
- Proposing deterministic output sequence series coupled quadrature oscillators and implementing in 90 nm CMOS technology which makes the LC oscillators a practical solution in quadrature signal generation.
- Improving the tuning range of LC quadrature oscillators by mode switching which is beneficial in UWB and multi-band radios.
- Proposing a method to reduce the frequency drift due to temperature in LC quadrature oscillators to replace external crystal oscillators resulting in less complex systems and saving power.

To achieve meet the settling time requirement of UWB frequency synthesizers, after re-

viewing different frequency synthesizer topologies, a fast hopping topology with superior spurious performance is introduced which covers the whole UWB spectrum and is flexible to achieve any band group by simply tuning the wide tuning range oscillators. On the other hand, the proposed UWB frequency synthesizer utilizes only one mixer which improves the spurious performance. Quadrature signal are essential part of image rejection mixers, therefore, different methods quadrature signal generation are also presented and quadrature LC oscillators, as an excellent choice of quadrature signal generation , was the main focus of this dissertation. Also the problem of phase ambiguity in LC quadrature oscillators was discussed by using the solution of deterministic output sequencing in S-QOSCs. By this technique the quadrature oscillators, which usually have more than one stable mode of oscillation, will be forced to selectively work in any modes of quadrature oscillation. Furthermore, selective operation of the quadrature oscillator was presented which provided us with the opportunity to improve the tuning range of the oscillators up to twice more than one single mode which is beneficial in the proposed 14 band frequency synthesizer as well as other applications such as multi-band radios. Finally, in this dissertation we discussed the possibility to replace external XTALs by CMOS reference frequency generators resulting in a compact design with less complexity and lower power consumption and the proposed method to reduce the frequency drift in LC quadrature oscillators was also studied.

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