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For Reference

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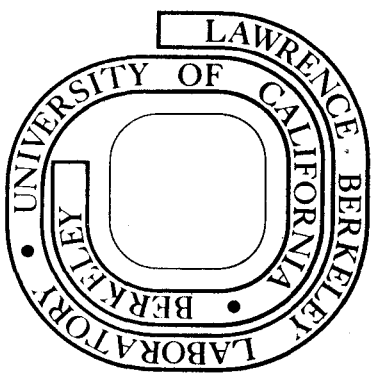

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A LARGE-SCALE DIGITIZER SYSTEM (LSD) FOR CHARGE AND TIME DIGITIZATION IN HIGH-ENERGY PHYSICS EXPERIMENTS*

R. F. Althaus, F. A. Kirsten, K. L. Lee, S. R. Olson,
L. J. Wagner, and J. M. Wolverton
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Abstract

A large-scale digitizer (LSD) system for acquiring charge and time-of-arrival particle data from high-energy-physics experiments has been developed at the Lawrence Berkeley Laboratory. The objective in this development was to significantly reduce the cost of instrumenting large-detector arrays which, for the 4π-geometry of colliding-beam experiments, are proposed with an order of magnitude increase in channel count over previous detectors.

In order to achieve the desired economy (~$65 per channel), a system was designed in which a number of control signals for conversion, for digitization, and for readout are shared in common by all the channels in each 128-channel bin. This paper describes the overall-system concept, and the distribution of control signals that are critical to the 10-bit charge resolution and to the 12-bit time resolution. Also described is the bit-serial transfer scheme, chosen for its low component and cabling costs.

Summary

The performance specifications of the large-scale-digitizer system are summarized in Figure 1. Those specifications which are felt to be not self-evident are discussed in the overall system description which follows. The system is general in character; that is, not designed uniquely to meet the needs of a specific detector assembly, but to be used wherever many channels of charge of time parameter(s) are to be converted and digitized. Economic design goals are achieved with completely operational 256-channel systems; however, even 64-channel systems are cost effective.

LARGE SCALE DIGITIZER

Economical Large Scale* Charge and Time-of-Arrival Digitizer System

***128 Converter Channels per Bin to 8192 Channels Maximum per System**

SYSTEM CHARACTERISTICS

Charge Converter

- 10-bit digitization
- ¼ pCoulomb/count
- ±2 counts linearity fit to two straight lines
- $\sigma \leq 0.7$ channels
- Pedestal temperature coefficient: ≤ 0.05 pCoulombs/°C @ 1 μsec Q-gate
- Hit pattern logic
- Calibrate facility

Time Converter

- 12-bit digitization
- 125 psec/count
- ±2 counts linearity
- Hit pattern logic
- Common start or common stop
- Self abort
- Converter multiplexing
- Calibrate facility

Overall System

- 50-200 μsec. digitization time
- "Smart" readout via CAMAC
  - Fast discretionary
  - Read-All
- Wire multiplexing (time only)
- System abort
- L-Synchronized, Q-Terminated CAMAC Block transfer capability (ULS)

Exploits Economies of:

- Large scale (quantity)
  - Development cost amortization
  - Production techniques

Shared Elements:

- Conversion Control Signals
- Digitization Control Signals
- Readout Control Signals
- Calibration Source
- Multiplexed Time Converters
- Temperature Stabilization
- Serial Readout Bus
- Power Distribution

Figure 1. Specifications

*This work was done with support from the U.S. Energy Research and Development Administration.

Overall System Description

The overall large-scale-digitizer system is illustrated in Figure 2. Figure 3 is a photograph of an operational system. The design concept of economy through shared resources and controls is emphasized through the following salient points:

1. Packaging economics--128 channels per LSD bin share common power, control card, and readout cabling.

2. Charge and time converter cards contain eight converter-digitizer channels each.

3. Event trigger and calibration voltages/pulses are fed to the control cards which distribute them to all 128 channels in each bin.

A conversion-digitization-readout sequence is initiated for either an event or a calibration run upon the receipt of a signal at the control card of the LSD bin: A charge gate triggers bins loaded with charge converters. A pulse for common start or for common stop, whichever configuration is in use, is required for bins loaded with time converters. The control card then generates the control signals required for conversion and for digitization, and drives all 128 converter-digitizer channels in the bin.

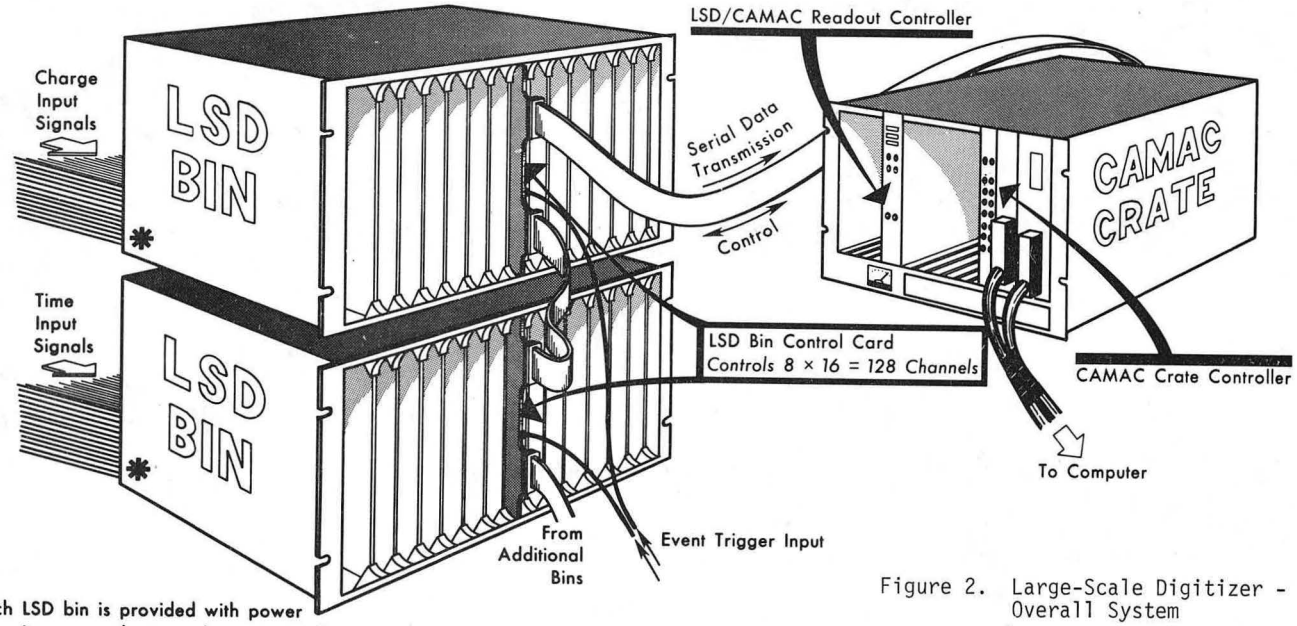


Figure 2. Large-Scale Digitizer - Overall System

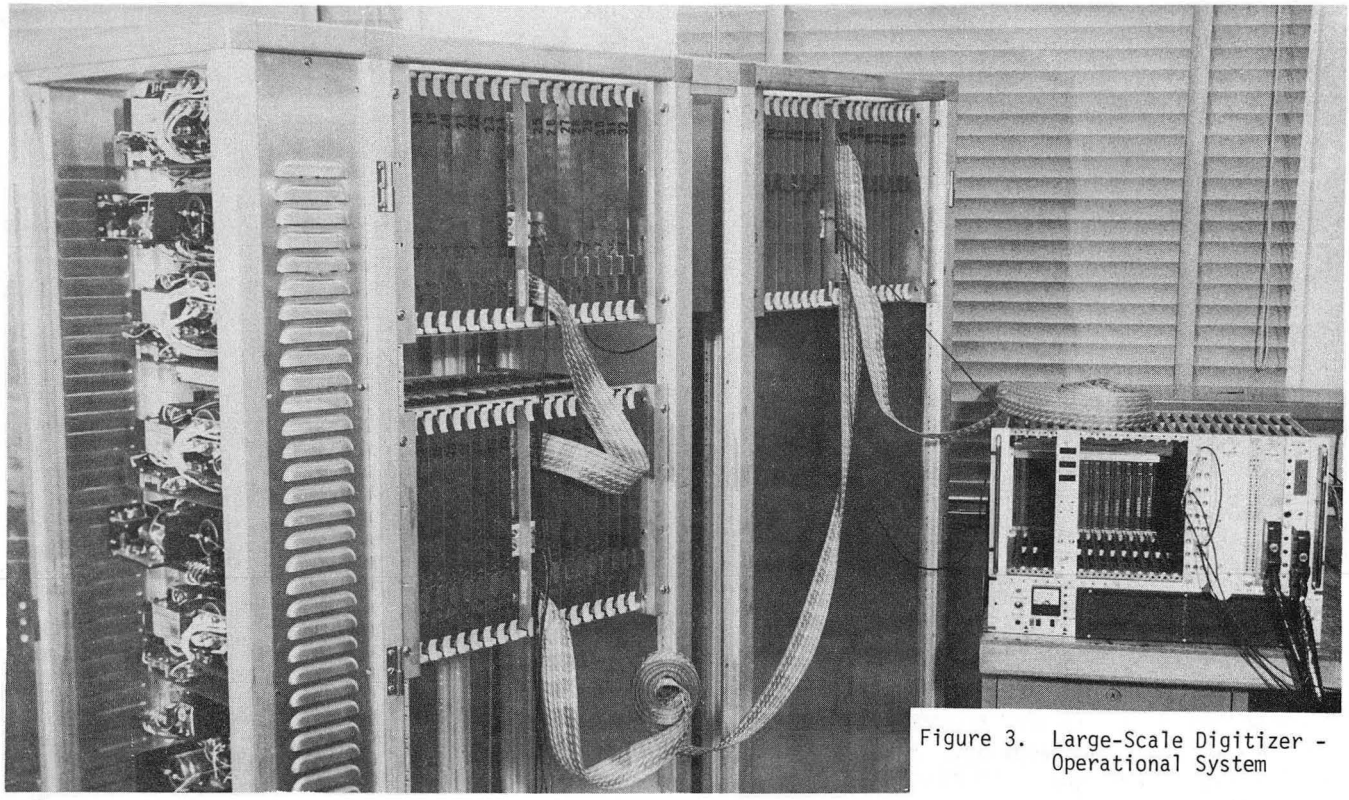


Figure 3. Large-Scale Digitizer - Operational System

Under this control, each channel converts, digitizes, and stores a digital representation of its input charge or time signal. (Individual channel input signals, for charge or time, are brought into each channel via multiple-contact connectors which mate with wire wrap posts at the rear of the bin.) At "digitization complete", the control card initiates a serial data transfer to the CAMAC readout module. The CAMAC readout module then requests computer service and facilitates the complete readout of all LSD channels.

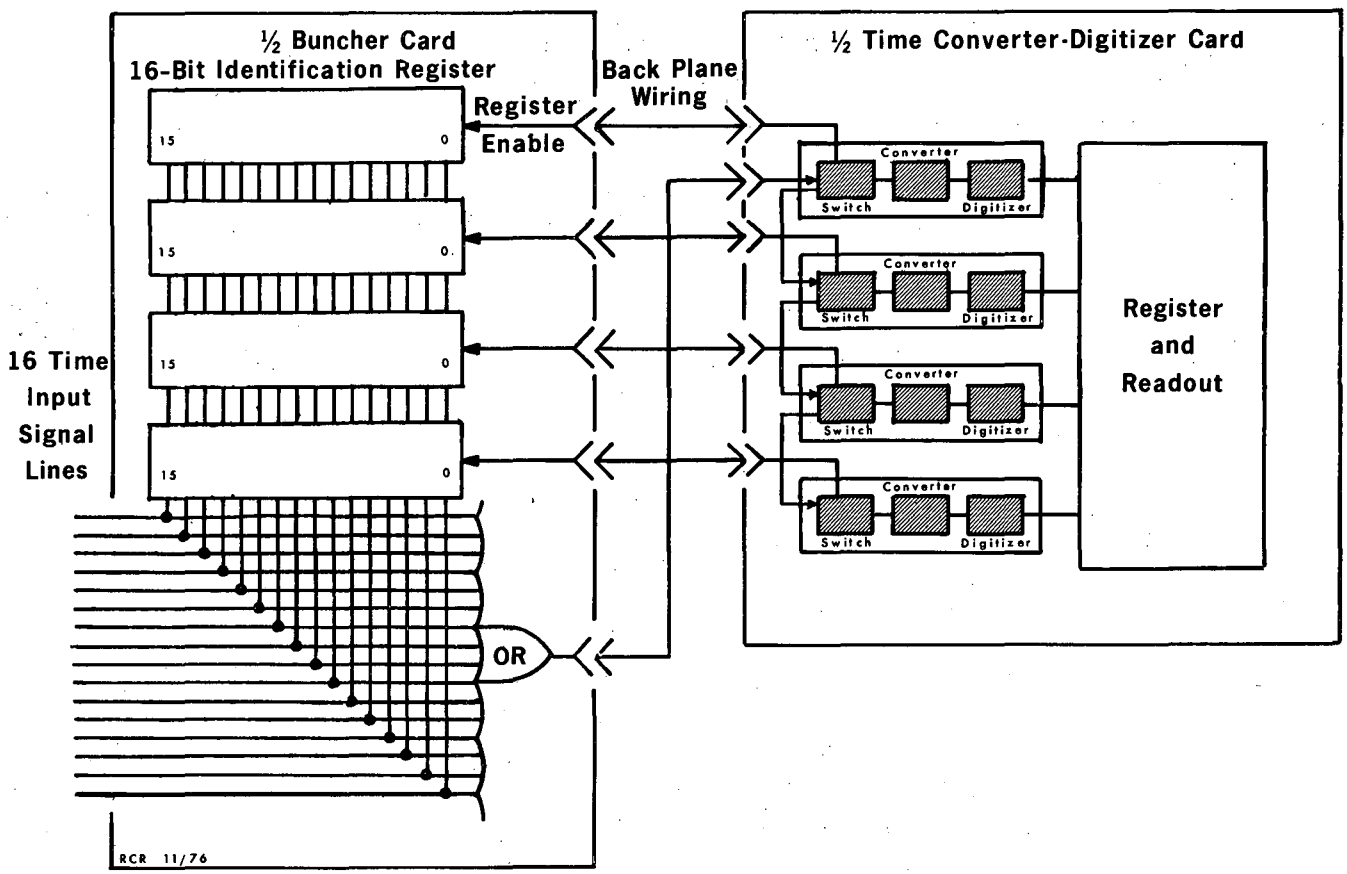
"Hit pattern" bits, indicating which channels have received over-threshold signals, are provided on card-edge connectors on the front of each converter-digitizer card. These bits are provided for the purpose of performing external medium-speed logic operations.

Another system capability which offers significant potential for economical utilization is the sharing of time converters by multiple wires.

Fundamental to each eight-channel time converter card is the capability of arranging for converters (in groups of two or four, by means of wire links) to automatically sequence the inputs from converter-to-converter upon each receipt of an input signal. Thus, multiple hits on a wire can be digitized in successive converter channels. This configuration is functionally attractive, and is economical in that one does not have to provide fast external channel-switching logic to perform this task.

But the real economy comes into play by incorporating another card in the LSD system, called the "Buncher", which allows the grouping (bunching) of up to 16 input lines into each half of a converter-digitizer card which has been appropriately wire-linked to sequence upon receipt of multiple hits. (Figure 4.) The buncher contains four 16-bit hit identifier registers, which accept sequencing control from the four converter-digitizer channels. Thus, where the kinematics of an experiment will allow, 16 wires on which no more than four hits are anticipated during the same event can be serviced by four time converter-digitizer channels. The result is that four inexpensive hit identifier registers and four converter-digitizers can be used in place of 16 converter-digitizers. Though not diagrammed in Figure 4, the hit identifier registers are readout with the converter-digitizer cards.

In addition to the selectable 1, 2, or 4 auto-sequencing of time converters, the 16 channels of the Buncher can also be manipulated by wire links into groups of 4, 8, or 16. Thus, the combination of multiple wires and auto-sequenced converters best suited to each experiment can be configured.



(A Duplicate Arrangement can be Configured with the 2nd-half of the two cards)

Figure 4. Diagram of Buncher/Converter Multiplexing

Converter Card Common Control Functions

The conversion and digitization circuits are described in detail in a companion report[1]. In Figure 5 the degree to which the control functions are carried out with common control signal lines is emphasized. The economy in not having to provide separate conversion control signals, digitization control signals, and readout logic for each converter channel seems self-evident. Amortization of each of the control signal generators over 128 channels per bin is indeed cost effective. But it is not without some technical challenge (and some cost) in control signal distribution.

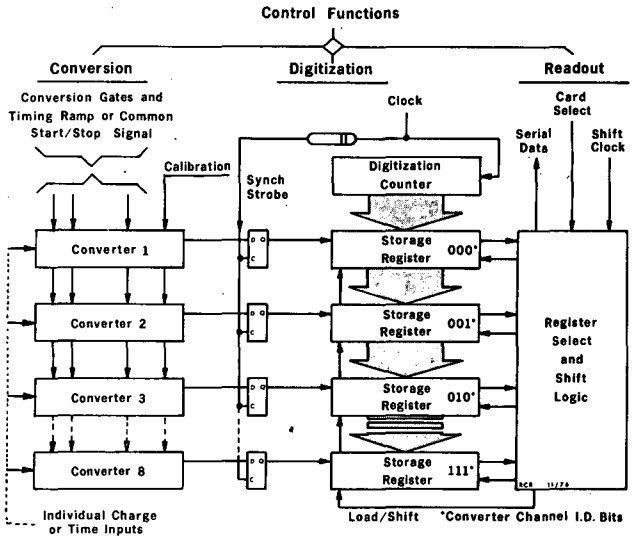


Figure 5. Converter Card Control Logic

The slope of the charge conversion timing ramp is 5 mV per bit period. The digitization clock swings through TTL logic levels. How does one avoid cross-talk? At full scale calibration input, the system sensitivity to Q-gate width is 50 ps per least count. How does one achieve a standard deviation of 0.7 channels for calibration? How does one tolerate line reflections from taps on twisted-pair transmission lines, when signal rise-times are critical to timing? The answer to each of these questions is: by well planned control signal distribution techniques. Physical separation of ramp signal from digital logic signals, and good ground-plane shielding techniques provide adequate stability for the ramp. On the eight-channel converter cards, differential drive on balanced lines provides excellent Q-gate width stability. Radial distribution of matched-length twisted-pair control-signal lines in small groups achieves reasonable impedance match, thus preserving signal rise-time integrity.

Control Card and Control Signal Distribution

Care in control signal distribution is emphasized again in Figure 6. The use of twisted-pair lines for signals that either are critically sensitive or are grossly obnoxious noise transmitters is one technique utilized. To the extent possible, incompatible signals are kept physically separated.

System operational sequence, as described earlier, can be read directly from Figure 6. An event trigger initiates conversion, followed by digitization, followed finally by readout. When

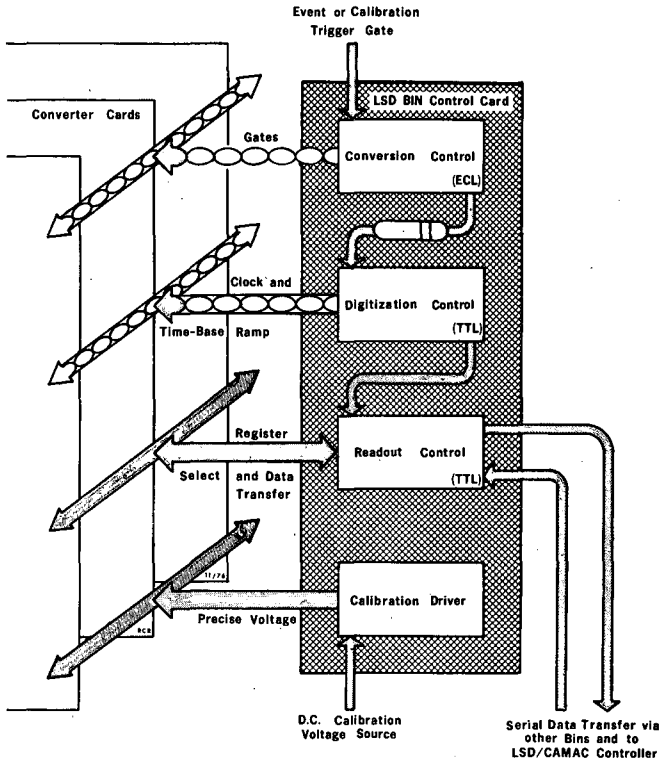


Figure 6. Bin Control Card Logic

calibrating the charge converter channels, a dc calibration voltage is required (usually a DAC output, under computer control).

LSD System Readout

Readout of the LSD system is accomplished via the standard CAMAC data bussing system. Figure 7 illustrates the functional blocks of the readout sequence. In addition to the expected task of performing the handshake manipulation between the serial transfer from the LSD system and the parallel transfer on the CAMAC dataway, the LSD/CAMAC Readout Controller provides format translation, i.e.: arranging converter address and data, to minimize the tasks required of the recipient computer.

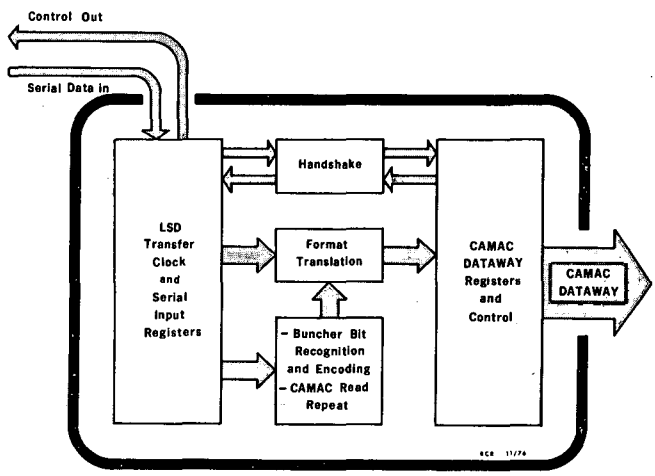


Figure 7. LSD/CAMAC Readout Controller - Functional Block Diagram

The controller also completely unscrambles the addressing and the data when buncher cards are used for multiplexing multiple wires into few converter-digitizer channels; leaving the computer oblivious to this potentially complicating system configuration.

Readout transfer speed is controlled by the recipient computer system; the LSD system will transfer at rates up to the limit of the CAMAC specification for dataway transfer. Readout can be selected by computer to Read All mode, where all channels are regardless of their data content; or to Discretionary Readout mode, in which data only from over-threshold channels are transferred.

Calibration Voltage Distribution

In the calibrated mode the LSD system sensitivity to the calibrate input voltage is 10 mV per least count. Since the calibrate voltage is a controllable external source, the system is subject to the usually problems of common-mode noise (such as 60-cycle ground currents) between chassis powered from different ac receptacles. Figure 8 illustrates how this problem is avoided; by treating the input signal as though it were differential at the input. The receiving amplifier converts the input from differential to single-ended.

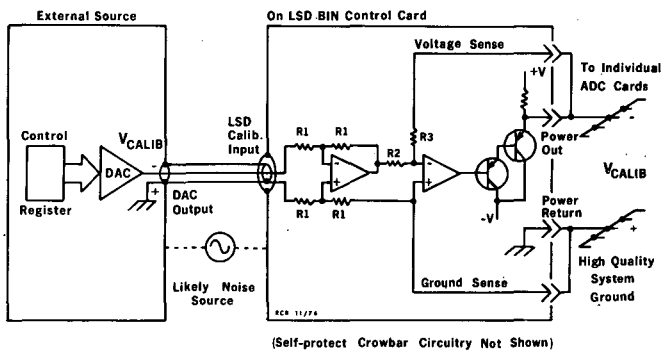


Figure 8. Calibration Voltage Distribution

A second problem for calibration is the distribution of the calibration voltage to all 128 converter channels per bin. Since each channel draws 5 mA at full scale; the calibration voltage driver must provide a current from 0 mA at the origin to 640 mA at full scale. Also diagrammed in Figure 8 is the technique for compensating for the V_{be}'s of the Darlington power driver and for the IR drops of the control-board card-edge connector; by extending the sense points of the feedback loop around these points.

Conclusion

To date 896 channels of charge digitizer and 336 channels of time digitizer are deployed in various physics systems. The Pb-glass wall scintillation detectors at the SPEAR colliding-beam ring at Stanford Linear Accelerator Center (SLAC) are instrumented with 320 channels of charge converters. For another proposed detector system, 320 channels are being used to measure charge in dx segments of particle tracks. A 128-channel time digitizer system is being used in a large drift chamber study program.

Early concerns about circuit stability, as we contemplated the physical separation of control signals from the controlled conversion-digitization circuits, were dispelled as the design concept of shared control proved to be effective for temperature compensation as well as for functional operation. Cost economies were achieved without limiting performance in relation to present state-of-the-art charge and time converter-digitizer systems.

Reference

1. R. F. Althaus, et al., "Large-Scale Digitizer System, Analog Converters," published in these proceedings.

This report was done with support from the United States Energy Research and Development Administration. Any conclusions or opinions expressed in this report represent solely those of the author(s) and not necessarily those of The Regents of the University of California, the Lawrence Berkeley Laboratory or the United States Energy Research and Development Administration.

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