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Los Angeles

Physical Mechanism and Fundamental Performance Limits on Graphene Non-Volatile Memory Technologies

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

Emil Beom Song

2012

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ABSTRACT OF THE DISSERTATION

Physical Mechanism and Fundamental Performance Limits

on Graphene Non-Volatile Memory Technologies

by

Emil Beom Song

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2012

Professor Kang L. Wang, Chair

Non-volatile memory (NVM) constitutes a vital portion in electronics to retain information for both archiving and data processing. Limitations encountered in flash technology upon increasing density and reducing cost by scaling necessitates alternative memory structures beyond complementary-metal-oxide-semiconductor (CMOS). The single atomic two-dimensional profile and the superior physical properties of graphene allow advancements in a variety of memory metrics when implemented into several types of memory architectures. In this dissertation, two prototype NVM memory technologies: graphene floating-gate flash memory and graphene ferroelectric memory is thoroughly analyzed and the performance advancements and challenges that arise compared to its predecessors are discussed.

The dissertation of Emil Beom Song is approved.

Richard B. Kaner

Benjamin Williams

Diana Huffaker

Kang L. Wang, Committee Chair

University of California, Los Angeles

2012

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Vita

EDUCATION

University of California, Los Angeles (UCLA) — June 2009
***MS** in Electrical Engineering*

Pohang University of Science & Technology (POSTECH), South Korea — March 2004
***BS** in Physics*

RESEARCH EXPERIENCE

Quantum-Functional Semiconductor Research Center, Dongguk University, South Korea — Summer 2010
Representative for California Nano Systems Institute (CNSI)

Space Materials Laboratory, Aerospace Corporation, El Segundo, CA — 2009-current
Scientific Research Associate

Device Research Laboratory, Electrical Engineering Department, UCLA — 2006-current
Graduate Student Researcher

Physics Department, POSTECH — 2001-2004
Undergraduate Researcher

TEACHING EXPERIENCE

High School Summer Research Program, School of Engineering & Applied Science, UCLA — Summer 2011
Laboratory Supervisor

Electrical Engineering Department, UCLA — 2009-current
Graduate Student Mentor

Nanoscience Outreach Program, CNSI, UCLA — 2007-2010
Program Trainer

Electrical Engineering Department, UCLA — 2007
Teaching Assistant

Dr. Yang Education Group, Inc, Torrance, CA — 2004-2006
Private Tutor

HONORS AND AWARDS

Student Travel Grant — 2009
US Army and Air Force

National Science Foundation (NSF) - Material Creation Training Program Fellowship — 2007-2009
Integrative Graduate Education and Research Traineeship Program (IGERT)

Dean's List — 2001-2003
POSTECH

Honors Scholarship — 2001
POSTECH

TECHNICAL SKILLS

Chemical Vapor Deposition System (CVD), Low Temperature Transport Measurements (Lock-in), Multi-mode Optical Microscopy, Raman Spectroscopy, Ellipsometer, Atomic Force Microscopy (AFM), Scanning Electron Microscopy (SEM), UV/Vis/NIR Spectrophotometer

PUBLICATIONS

Journal (* first/co-first/corresponding author)

- Submitted

1. **Emil B. Song*** et al., *"Graphene Nonvolatile Memory: Overview and Prospect"*, (2012).
2. Sejoon Lee et al., *"Gate-tunable Selective Operation of SET/SHT in a Single Si Quantum Dot at Room Temperature"*, (2012).
3. Mirko Poljak et al., *"Influence of Edge Defects, Vacancies, and Potential Fluctuations on Transport Properties of Extremely-Scaled Graphene Nanoribbons"*, (2012).
4. Mirko Poljak et al., *"Influence of Quantum Hopping on the Bandgap of Extremely-Scaled Graphene Nanoribbons with Edge Defects"*, (2012).
5. Cher X. Zhang et al., *"Total Ionizing Dose Effects on Graphene-based Non-volatile Memory Devices"*, (2012).

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7. Haider I. Rasool, **Emil B. Song*** et al., Journal of American Chemical Society, 133, 12536, (2011).
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10. Guangyu Xu, et al., Nano Letters, 11, 1082, (2011).
11. Jiyoung Kim et al., Nanotechnology, 22, 254006, (2011).
12. **Emil B. Song*** et al., Applied Physics Letters, 96, 081911, (2010).
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Conference

1. **Emil B. Song** et al., European Materials Research Society (EMRS) Conference, Strasbourg, France, (2012) (Invited Speaker).
2. Mirko Poljak, et al., European Solid-State Device Research Conference (ESSDERC), Bordeaux, France, (2012).
3. Sung Min Kim, et al., IEEE International Memory Workshop (IMW), Milano, Italy, (2012).
4. En Xia Zhang et al., American Vacuum Society (AVS) International Symposium, Tampa, Florida, (2012).
5. Cher X. Zhang et al., IEEE Nuclear and Space Radiation Effects Conference (NSREC), Miami, Florida, (2012).
6. Sung Min Kim et al., International Display Workshops (IDW), Nagoya, Japan, (2011).
7. Sung Min Kim, et al., Symposium on VLSI Technology, pp 118-119, (2011).
8. Guangyu Xu, et al., Device Research Conference (DRC), Indiana, (2010).
9. **Emil B. Song** et al., Nanoelectronic Device for Security and Defense (Nano-DDS) Conference, Florida, (2009).
10. Sung Min Kim et al., Silicon Nanoelectronics Workshop, Kyoto, Japan, (2009).
11. Jiyoung Kim et al., Symposium on VLSI Technology, pp 186-187, (2009).
12. Jiyoung Kim et al., Symposium on VLSI Technology, pp 122-123, (2008)

1. Introduction

1-1. Rise of Graphene

In carbon-based systems, the diversity in the way carbon atoms can form bonds leads to various atomic structures with different physical properties; a result of the dimensionality and symmetry of the particular carbon system. Among carbon allotropes (Figure 1), graphene, a two-dimensional (2D) honeycomb lattice, has been theoretically studied for several decades as a building block for graphite (3D), carbon nanotubes (1D), and fullerenes (0D).

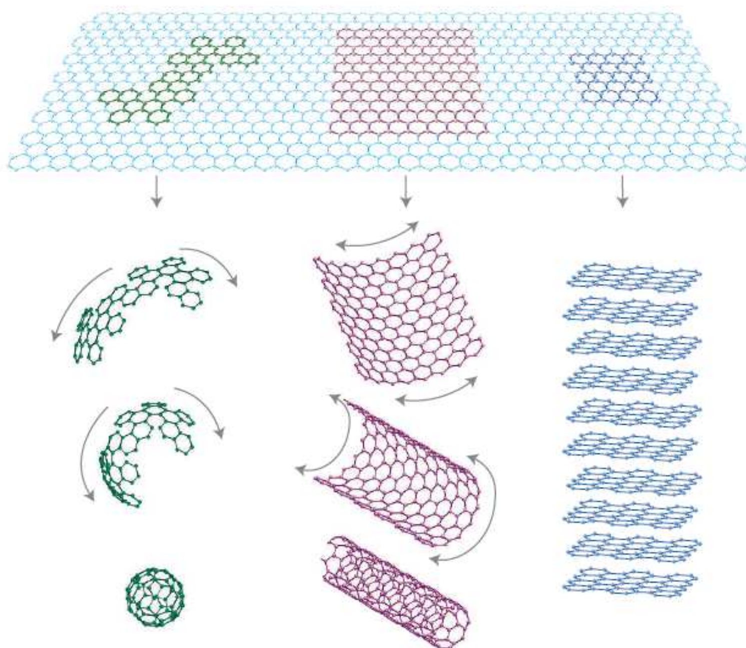


Figure 1. (Top) Graphene is a honeycomb lattice of carbon atoms. (Left) Fullerenes (C_{60}) are molecules consisting of wrapped graphene by the introduction of pentagons on the hexagonal lattice. (Middle) Carbon nanotubes are rolled-up cylinders of graphene. (Right) Graphite can be viewed as a stack of graphene layers.[1]

Only until 2004, the existence of graphene was experimentally proven and prompted enormous attention to the scientific and engineering community, which led to the Nobel Prize in physics at 2010. Before 2004, scientists thought graphene cannot be thermodynamically stable. According to the Mermin-Wagner theorem, long-range crystalline order of two-dimensional crystals should collapse through long-wavelength fluctuations (i.e. thermal fluctuations) and lead to scrolling and segregation in a three-dimensional space. Soft condensed matter membranes are known to bend and form ripples. As shown in Figure 2, however, graphene exhibits high thermodynamic stability when intrinsically incorporated with ripples or when extrinsically supported by a solid substrate. For the first time, graphene was spotted from a subtle optical effect on top of a 300nm thick SiO_2 substrate through an optical microscope (Figure 3).[2-6]

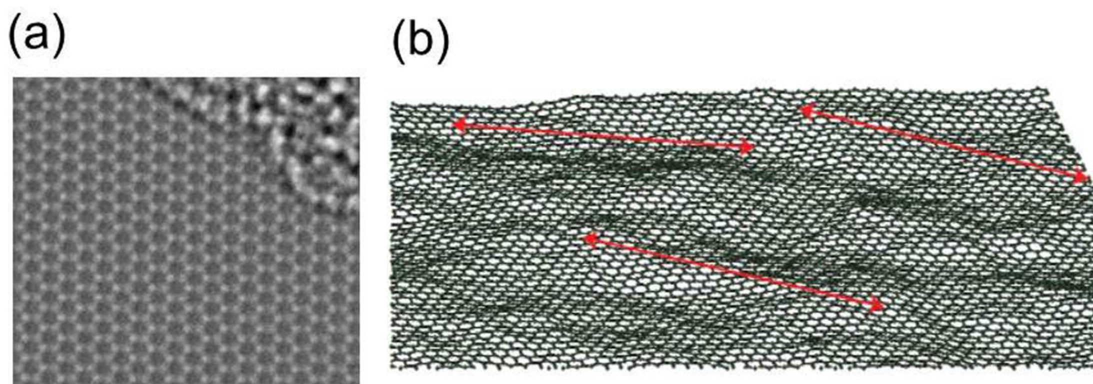


Figure 2. (a) Graphene, a one atom thick sheet, remains as a perfect crystal. The hexagonal atomic structure of graphene was taken from a high resolution transmission electron microscope with an aberration corrected lens from Lawrence Berkeley National Laboratory (LBNL). (b) Simulated graphene sheet showing mesoscopic corrugations for thermodynamic stability. The red arrows are 8nm long.[7]

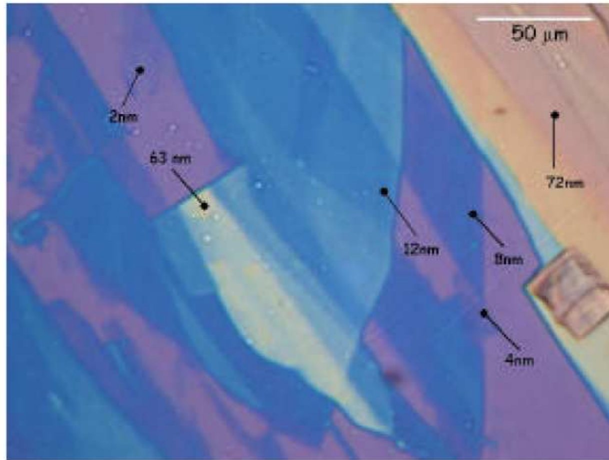


Figure 3. Optical image in white light of graphitic films of various thicknesses obtained through mechanical exfoliation of graphite onto a 300nm SiO2. The indicated values of the thickness were measured by Atomic Force Microscopy (AFM).[8] The colors are also used as a high-throughput method to identify the thickness of graphitic films; an addition of graphene or single layer graphite atop of a graphitic flake enhances the contrast between the graphitic film and the SiO2 substrate through an interference effect.

1-2. Electronic Properties of Graphene

Graphene's unique band structure has led to copious fascinating phenomena; half-integer quantum Hall effect at room temperature,[9] Klein tunneling,[10] Kohn anomaly,[11,12] and most importantly from an engineering aspect the electric-field effect.[8] Therefore, it is crucial to understand the band structure of graphene, which describes the possible energy states that the material's constituent electrons could occupy.

In graphene, there are four valence electrons in each carbon atom, one from the s-orbital and the other three from the p-orbitals. Three electrons hybridize into sp^2 orbitals and form three covalent carbon-carbon bonds, which refers to the σ bond (Figure 4a). These bonds are responsible for the high mechanical strength of the two-dimensional carbon structure. The remaining valence electron extends out-of-plane and forms a π bond, which accounts for the electronic conduction in graphene.

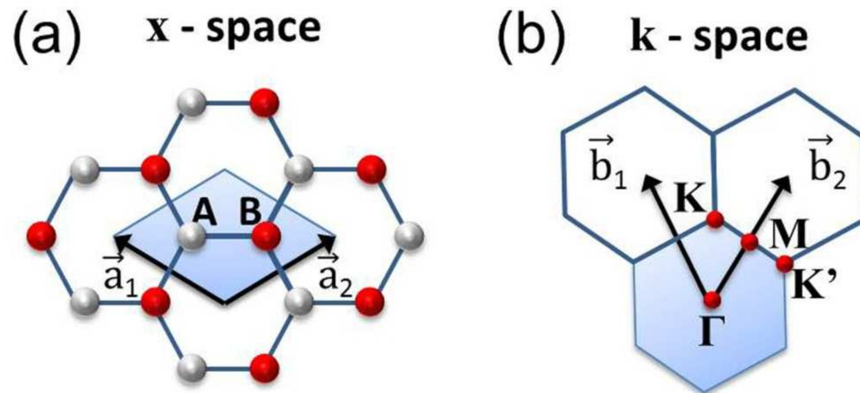


Figure 4. Honeycomb lattice and Brillouin zone of graphene. (a) Two interpenetrating triangular lattice that forms graphene's lattice structure, where a_1, a_2 are the unit vectors and the shaded region is the unit cell. (b) The corresponding Brillouin zone (shaded region), where the Dirac points are located on K and K' and accounts for the two valley degeneracy (i.e. three vertices of the BZ, which are connected through a reciprocal lattice vector are equivalent). $b_{1,}$ b_2 are the unit vectors, K, M, K', Γ are the high symmetry points.

For comparison, diamond consumes all four valence electrons to form σ bonds, leading to an insulator. On the other hand, silicon also being a member of the fourth column (i.e. four valence electrons) in the periodic table has exactly the same structure as diamond. However, the greater overlap between the valence electrons in Si (i.e. silicon atom is larger than carbon) results in a thicker band, and smaller bandgap, therefore leading to a semiconducting behavior.

Now let's take a look at the electronic band structure of graphene. Graphene has a hexagonal lattice structure that is associated with a basis of two carbon atoms. Using the tight binding model and allowing nearest, and next-nearest-neighbor hopping for electrons in the π orbitals of graphene, under the second quantization form, the Hamiltonian of a single layer graphene can be written as

$$H = -t \sum_{<i,j>,\sigma} \left(a^*_{\sigma,i} b_{\sigma,j} + b^*_{\sigma,j} a_{\sigma,i} \right) - t' \sum_{<<i,j>>,\sigma} \left(a^*_{\sigma,i} a_{\sigma,j} + b^*_{\sigma,i} b_{\sigma,j} + a^*_{\sigma,j} a_{\sigma,i} + b^*_{\sigma,j} b_{\sigma,i} \right)$$

where $a_{i,\sigma}$ ($a^*_{i,\sigma}$) annihilates (creates) an electron with spin σ ($\sigma = \uparrow, \downarrow$) on site R_i on sublattice A (an equivalent definition is used for sublattice B), t is the nearest-neighbor hopping energy (i.e. hopping between different sublattices), and t' is the next-nearest-hopping energy (i.e. hopping in the same sublattice).[13] The energy bands derived numerically from the above Hamiltonian is shown in Figure 5(a) (See section 4. Appendix for an analytical derivation of the single-electron band structure of graphene, based on the tight-binding approximation that only considers the nearest-neighbors). If we take a close look at the energy dispersion near K and K' (Figure 5b), the energy band can be approximated as

$$E = v_F \hbar k$$

where v_F is the Fermi velocity, $\hbar$ is the Plank's constant, and k is the linear momentum of the electrons in graphene.

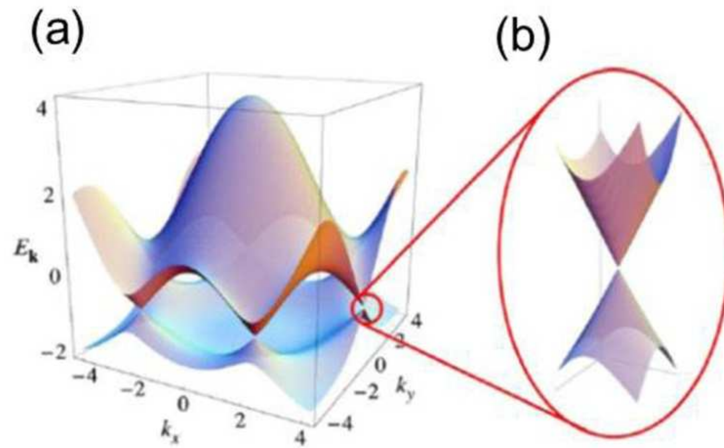


Figure 5. (a) Electronic band structure of graphene. Electronic dispersion in units of t (t = 2.7eV, t' = -0.2t). (b) Zoom in picture near the Dirac point (K and K' points), which displays a linear dispersion analogous to photons.[13]

Based on the electronic band structure, graphene is electronically categorized as a semimetal or zero-bandgap semiconductor (i.e. the density of states at the Dirac point is zero). The Fermi level in graphene lies within the Dirac point, when excluding any doping effects. This means that at zero temperature the bottom cone is filled with electrons and is interpreted as the valence band, and the top cone is empty and is called to the conduction band similar to a

semiconductor. The major difference of graphene compared to any other types of materials is that near the Dirac point, the quasi-particles (i.e. electrons in graphene) are massless (i.e. the effective mass associated with the curvature is zero) and have a constant Fermi velocity of approximately c/300, where c is the speed of light, independent of energy and momentum. Thus, the electrons in graphene are called massless Dirac fermions near the Dirac point.

Because of the low density of states near the Dirac point, the carrier concentration can be linearly modulated through means of capacitive coupling, also known as the electric-field effect (Figure 6). This allows the resistance to be tuned by a factor or 10, which is limited by the absence of an energy bandgap.

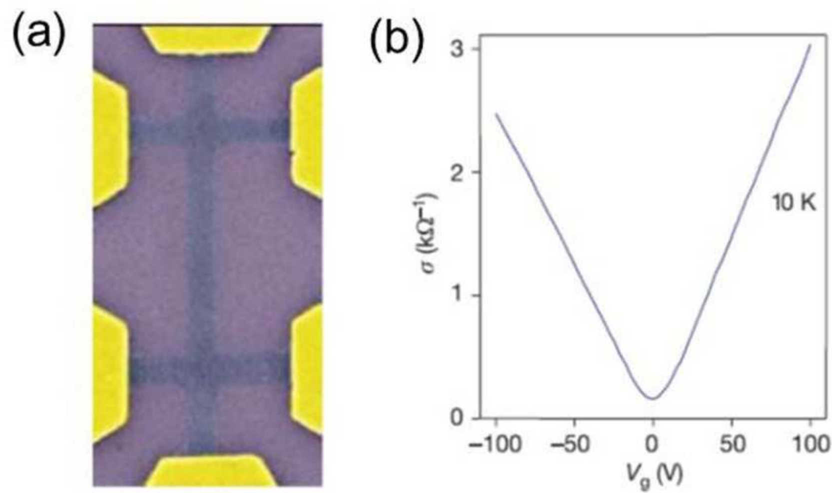


Figure 6. (a) Scanning electron microscope image of a graphene field-effect transistor (gFET). The blue stripe is the graphene with a width of 2μm. The underlying purple substrate is a 300nm SiO_2 thermally grown on top of a highly doped silicon wafer. The back Si layer serves as a gate electrode. (b) Ambi-polar field-effect behavior of a gFET. The increase of conductivity with gate voltage shows that the carrier concentration (proportional to the conductivity) can be modulated. The minimum conductivity point indicates that the Fermi level is at the Dirac point.[14]

The intrinsic carrier mobility in graphene is by far the highest among materials that exhibit electric field-effect behavior. The high intrinsic mobility originates from the high Fermi velocity (c/300) and the absence of back-scattering (Klein tunneling),[10] which are both fundamental characteristics of the linear electron energy dispersion. Room temperature mobility of 200,000 cm^2/Vs has been observed[15] in suspended graphene, and 500~15,000 cm^2/Vs are reported in supported graphene.[16] The extremely high mobility of graphene combined with the capability of modulating the resistance is the main reason engineers are considering graphene as a potential candidate to replace silicon technology.

Although only in its first decade, graphene research has yielded copious discoveries and innovations in science and technology. Amazingly, new physical phenomena are still being revealed at a rapid pace encompassing a broad range of fields from fundamental science to technological applications. In the past few years, the growing interest and studies of graphene and potentials as well as challenges have resulted in multiple review articles (e.g., materials and chemistry,[17-24] electronic,[25,26] optical,[27,28] thermal,[29] Raman,[30,31] spin,[32] gauge fields,[33] transistor,[34,35] NEMS,[36] nanostructures,[37-39] transparent conductor,[40] sensor,[41,42] energy[43-45]); these review articles have discussed many important advances, which are of great interest for the vast newcomers.

The hexagon in Figure 7 displays the progress and current status of graphene research, where each vertex represents a representative research field. Starting from 12 o'clock in Figure 7, enormous amount of effort has been put in to understand the scattering mechanisms that govern the electronic transport properties in graphene to experimentally achieve the intrinsic high mobility value. Next, moving clockwise within Figure 7, an energy bandgap has been created in this otherwise gapless material through quantum confinement or by lifting the degeneracy via

symmetry breaking for logic applications. In addition, the high young's modulus and low mass density of graphene has shown great opportunities for high speed MEMS applications. Furthermore, the 97% of transparency and semi-metallic property of graphene has offered an unprecedented opening for transparent electronics. Meanwhile, many engineers are exploiting newly found properties of graphene to construct novel device structures for various applications, such as transistor, non-volatile memory, energy storage, and transducer. At last and not the least, researchers have demonstrated multiple synthetic methods to produce large-scale graphene for mass production.[46,47]

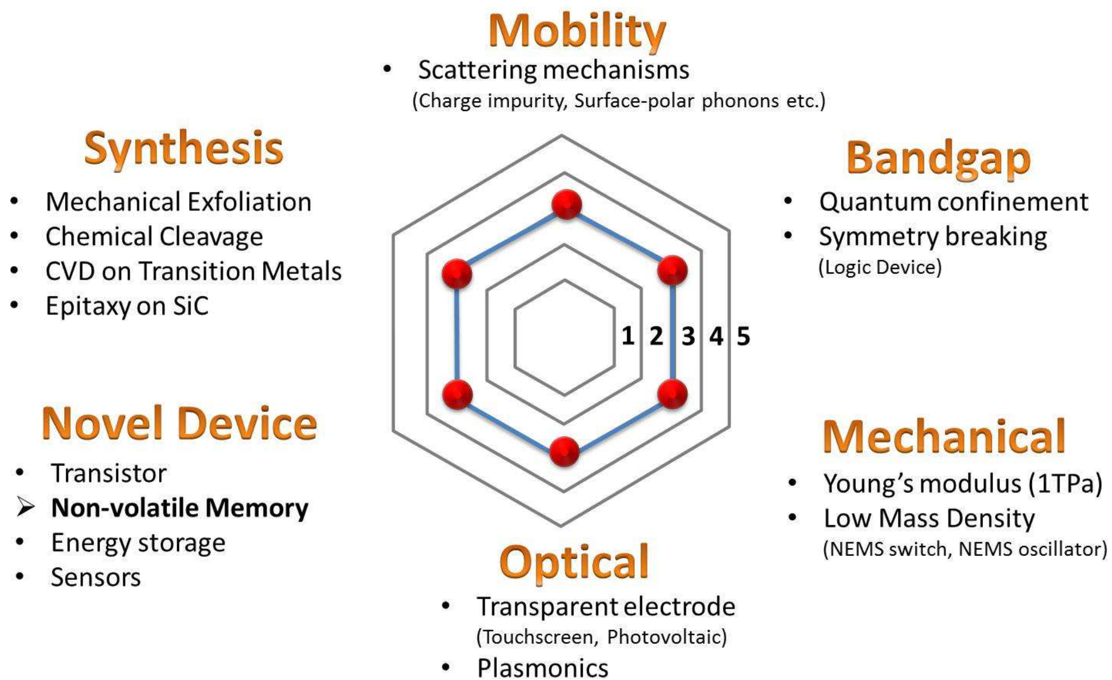


Figure 7. A hexagonal chart representing the progress and current status of graphene research in six representative fields: carrier mobility, electron energy bandgap, mechanical property, optical property, novel device application, and growth methods. The numbers indicate a rough estimate of the amount of research that has been conducted relative to each category based on my personal opinion. The bullet points under each category provide additional information and specifics that has been exploited and are currently being explored.

1-3. Nonvolatile Memory

Nonvolatile memory requires two fundamental elements – distinguishable states and nonvolatility. Whenever a material or structure exhibits two or more relatively stable switchable states, it may be considered a candidate for memory applications. In general, a stable switchable state is represented by a hysteresis in the device characteristics. A reproducible and reliable hysteresis must be obtained in a deliberate and controlled manner. Nonvolatility refers to information being stored without it having to be maintained by an extrinsic energy source. Data retention during void action implies that the method used to retain information must withstand at least the ubiquitous 26meV of thermal energy from disturbing the stored datum. Each NVM technology makes use of some physical or chemical attribute to satisfy the two necessary conditions, and the particular mechanism involved brings a number of technology specific features.

NVM technology evolved to the high demands of large storage density, low power consumption, and low cost per bit by continuous scaling. While floating-gate flash memory is the major NVM technology today, it will reach fundamental scaling limits because of the inherent limitations encountered during miniaturization. Various emerging technologies (Figure 8) have been studied in an attempt to replace floating-gate flash memory. An evolutionary approach to floating-gate is charge-trap based flash memories where a minor change in the charge layer is involved, while the revolutionary approach exploits state variables aside from electronic charge (e.g. polarization, magnetization, redox processes, atomic and electromechanical motion).[48-50]

The long list of distinct physical properties in graphene, such as, the atomic thinness,[51] high mobility,[52-54] electrically tunable resistance,[8] large Young's modulus,[55] high carbon reactivity with maximum surface to volume ratio,[56] and large transparency[57] offer a new type of

material that may be advantageous when integrated into a NVM structure. Nowadays, numerous ways of achieving graphene via mechanical exfoliation,[8] chemical vapor deposition (CVD),[47,58] SiC sublimation,[59] and chemical routes,[20] have opened great possibilities for graphene to be easily integrated in these NVM technologies.

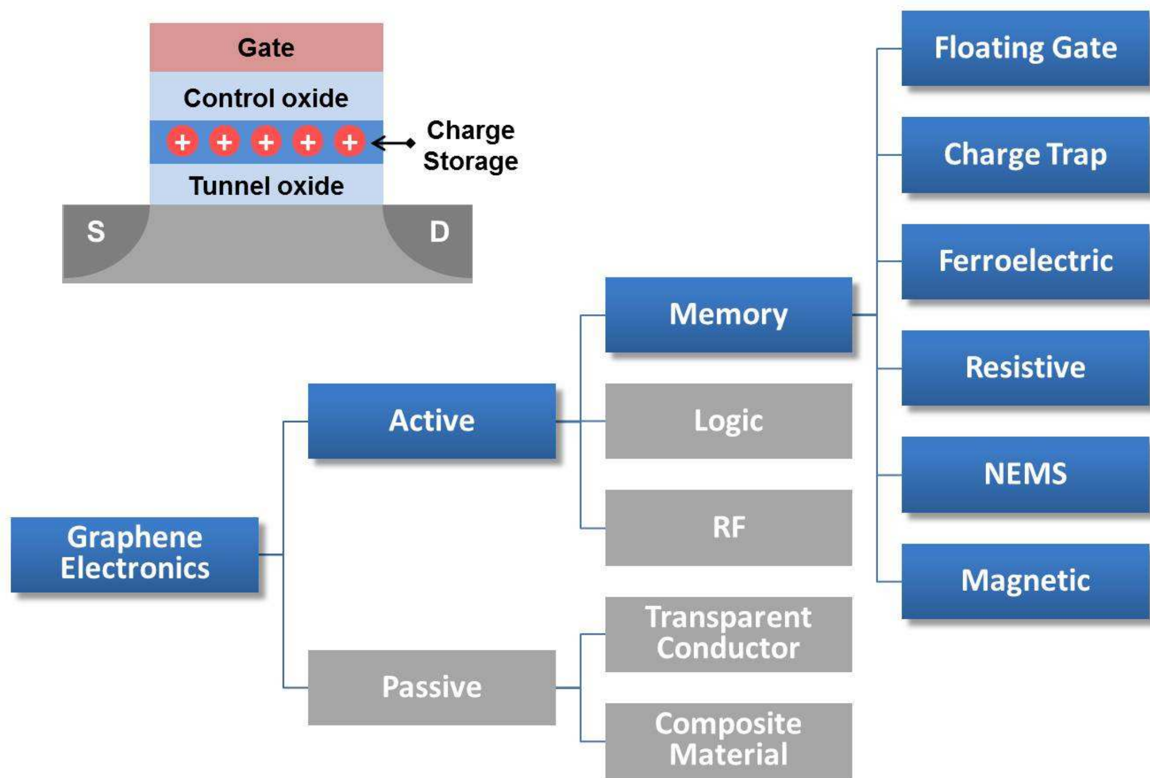


Figure 8. Classification of graphene based nonvolatile memory architectures: floating-gate, charge-trap, ferroelectric, resistive, NEMS, and magnetic. (Top-Left) Device structure of a conventional flash memory composed of a semiconducting channel, a tunnel oxide, a charge storage layer, a control oxide, a gate and a source/drain.

2. Graphene Nonvolatile Memory

2-1. Graphene Flash Memory (GFM)

Graphene has emerged as a fascinating platform because its planar atomic structure and high symmetry lead to a variety of superlative electronic and physical properties. Most recent achievements fall broadly into one of two categories: those that elucidate or exploit the intrinsic in-plane characteristics of graphene (e.g. transistors[8,60] and high tensile strength films[55,61]) and second, those that utilize the material's single atomic profile as the low-thickness limit of some scalable thin-film system such as ultracapacitors[62,63] or transparent conductors.[57,64] Here we show that graphene is an excellent platform for flash memory; one that may indeed help overcome several challenges faced by current industry standards.[5,65] Specifically, we address the benefits of graphene-based devices with an eye towards the width of the memory window, the retention time, and the cell-to-cell interference (Figure 9).

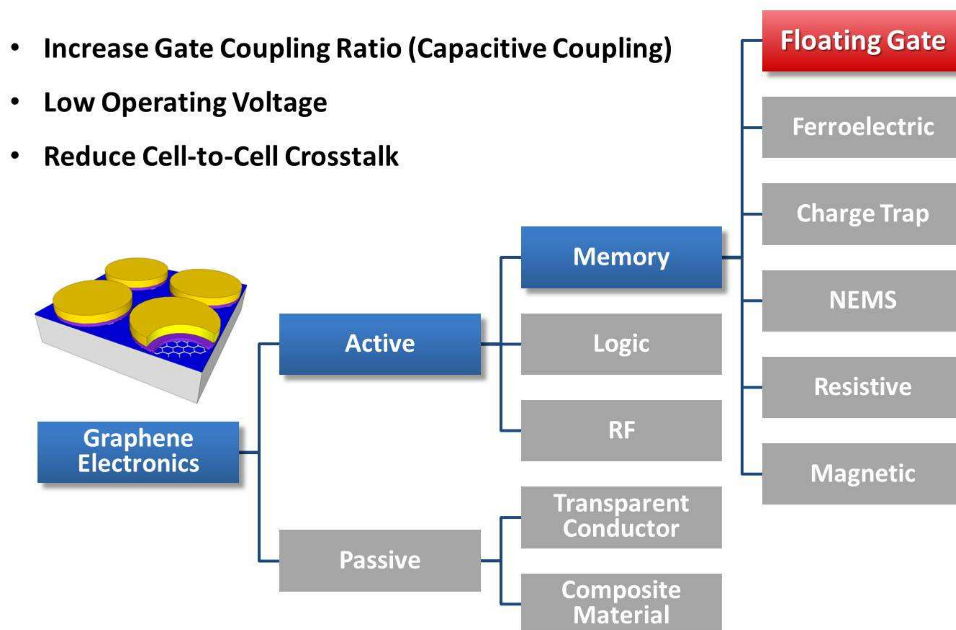


Figure 9. Graphene Floating-gate Flash Memory – Objectives; increase capacitive coupling, reduce operating voltage, and reduce cell-to-cell interference.

Flash memory is a key non-volatile element in a variety of modern electronic devices including USB drives, digital cameras, cell phones, gaming consoles, and music players. Recently, flash memory has started to replace conventional hard disk drives, providing a solid-state alternative with lower power consumption, greater reliability, and reduced size and weight for mobile applications. High demand has led to rapid innovation in the design of flash memory elements, with high scalability resulting from the fact that each cell consists of only a single transistor and a corresponding storage element buried inside the gate stack.

The current industry standard is floating gate flash memory, comprised of a p-type silicon substrate, a tunnel oxide, a highly doped n-type polysilicon data storage layer, a control oxide, and a top-side electrode. Writing is achieved by applying a voltage pulse on the top-side electrode, which allows electrons to tunnel through the tunnel oxide from the silicon substrate to the storage layer. This causes a positive shift in the threshold voltage of the silicon substrate and is simply the additional voltage required to compensate the stored charges underneath the control oxide. The binary values are defined by the current upon a read cycle at a voltage within the width of the threshold voltage shift.

The primary goal of most research in flash memory is to increase the density of storage elements such that their parent devices can be miniaturized. This leads to confronting several challenges that would normally jeopardize device performance at the reduced scale. Nonvolatility imposes a strict condition when the devices dimensions become smaller.[66] If we consider 50% charge loss over 10 years as the minimum requirement for nonvolatility, the tunnel oxide can be only reduced to 6-8nm. This requires programming voltages exceeding 10V, which increases cell-to-cell interference, and hence limits the minimum cell size. One way to alleviate this is to lower the operating voltage by increasing the coupling ratio of the control gate to the

floating gate through the adoption of a surrounded gate structure (a.k.a. FinFET). However, the side wall capacitance among neighboring cells increases and careful optimization is required.

Graphene offers a unique solution to this problem. Graphene's high density of states away from the Dirac point compared to polysilicon may reduce the operating voltage due to the low field requirement for charging. Simultaneously, the atomic thinness of graphene makes cell-to-cell cross talk to be considerably less. Furthermore, the stored data may retain longer since the graphene's high work function increases the potential barrier between the storage layer and Si channel, making it very difficult for the stored electrons to leak.

Although devices can be characterized along a wide variety of metrics, we concentrate on three principal figures of merit: width of the window, the retention time, and cell-to-cell crosstalk.[5,65] Width of window refers to the shift in threshold voltage of source to drain upon switching from the 0 to 1 memory states. Industry standards suggest that a minimum width of 1.5 V is necessary to produce a reasonable on/off ratio and hence, achieve reliable memory function.[5] For polycrystalline silicon floating gate devices, this requires a write/erase voltage of around ±20 V. This large voltage requirement is due to the low density of states (DOS) in the degenerately doped regime. This low DOS in polysilicon also leads to a strong emphasis on the gate coupling ratio (GCR), which corresponds to the portion of the overall programming voltage that occurs across the tunnel oxide. In contrast, graphene offers a semi-metallic band structure, with a high DOS away from the Dirac point. The same can be said for any metal, which begs the question of why metals are not implemented as charge storage layers. The answer lies in the fact that high migration of metal atoms renders them unsuitable for many device applications compared to graphene's inert covalently bonded honeycomb structure. Graphene's higher DOS lowers the field required for programming, which permits a greater range of engineering

solutions. For example, one can think of planar device structures, which produce lower GCRs, but may still be sufficient given the lower field requirement.

In order to investigate the voltage needed to achieve an adequate width of window using graphene, a number of devices were fabricated. Device process flow for GFM in capacitive structure is shown (Figure 10). A 4-inch boron doped ($10^{15}cm^{-3}$) Si wafer was cleaned sequentially by Piranha (H_2SO_4+H_2O_2) and RCA2 (HCl +H_2O_2+H_2O) solutions and then dipped into a buffered oxide etchant (BOE, HF+NH_4F+H_2O) to remove any residual native oxide. A 5nm tunnel oxide was grown by a rapid thermal oxidation system at 1000°C, at an oxygen flow of 40 sccm for seven seconds. After the graphene sheets were transferred onto this surface, 11 Å of Al was deposited by e-beam evaporation (CHA 30) and then oxidized in the air for 2 days before depositing 30nm of additional Al_2O_3 by atomic layer deposition (Cambridge Nanotech). Top electrodes with various areas (2.5×10^{-5} cm^2 to 7×10^{-4} cm^2) were lithographically defined using positive photo-resist (AZ 5214), a chrome mask and a Karl Seuss aligner. 500 nm of Al and 50nm of Au were deposited within the windows by e-beam evaporation, followed by the removal of the photoresist in acetone. In order to isolate each memory device, Au was used as a mask to etch the gate stacks. Thirty seconds of Cl_2 reactive ion etching (UNAXIS SLR770) was used to remove 35nm of Al_2O_3 followed by 3 minutes of O_2 plasma to remove any remaining graphene outside the device area. Finally, a 50nm thin Pt back contact was made by e-beam evaporation after another 30 seconds of backside etching in the Cl_2 etcher.

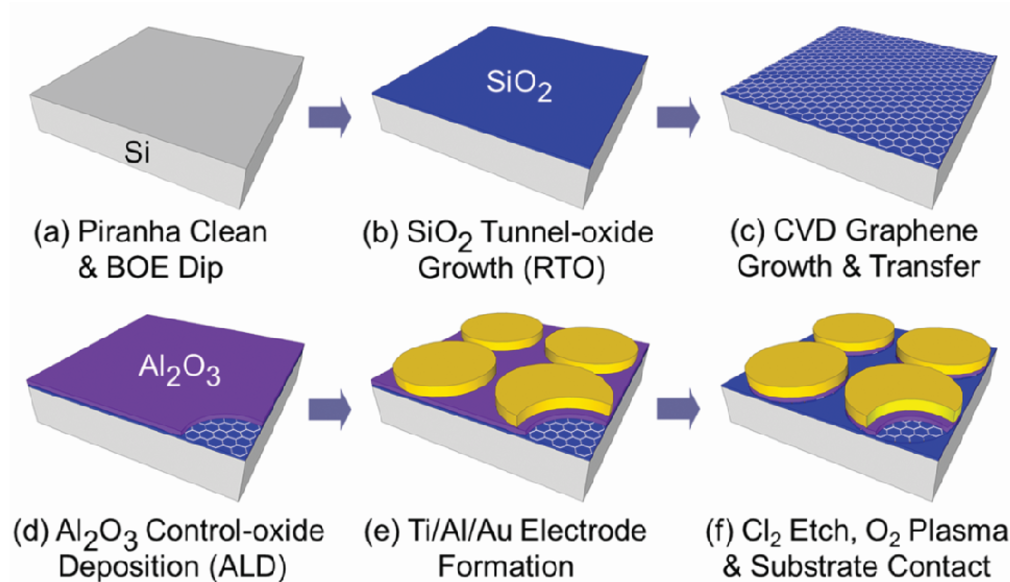


Figure 10. Graphene flash memory device fabrication processes. (a) Wafer cleaning by piranha solution to remove organic materials and then dipping into the buffered oxide etchant (BOE) to remove native oxide (b) Tunnel oxide growth by rapid thermal oxidation (RTO) (c) Graphene growth by chemical vapor deposition (CVD) and graphene transfer through chemical etching of Ni films and Cu foils. (d) High k dielectric (Al_2O_3) deposition by atomic layer deposition (ALD) (e) Electrode formation by photolithography, e-beam evaporation of Ti/Al/Au and lift off processes (f) Device isolation by dry etching Al_2O_3 and graphene suing Cl_2 etcher and O_2 plasma. Finally, Pt backside contact was made by e-beam evaporation.

Figure 11 shows a schematic of the device structure and transmission electron micrograph (TEM) cross-sections of both single (SLG) and multilayer (MLG) devices. In both cases, graphene was grown using chemical vapor deposition (CVD) on copper[47] or nickel[67] and subsequently transferred onto silicon substrates with a pre-grown SiO_2 tunnel oxide (~4nm). An Al_2O_3 control oxide (~30 nm) was then deposited through a two-step process[68] where a 1-2 nm thick layer of aluminum was evaporated and oxidized onto the surface of graphene followed by the deposition of Al_2O_3 by atomic layer deposition (ALD). Finally, an Al top gate was deposited by evaporation.

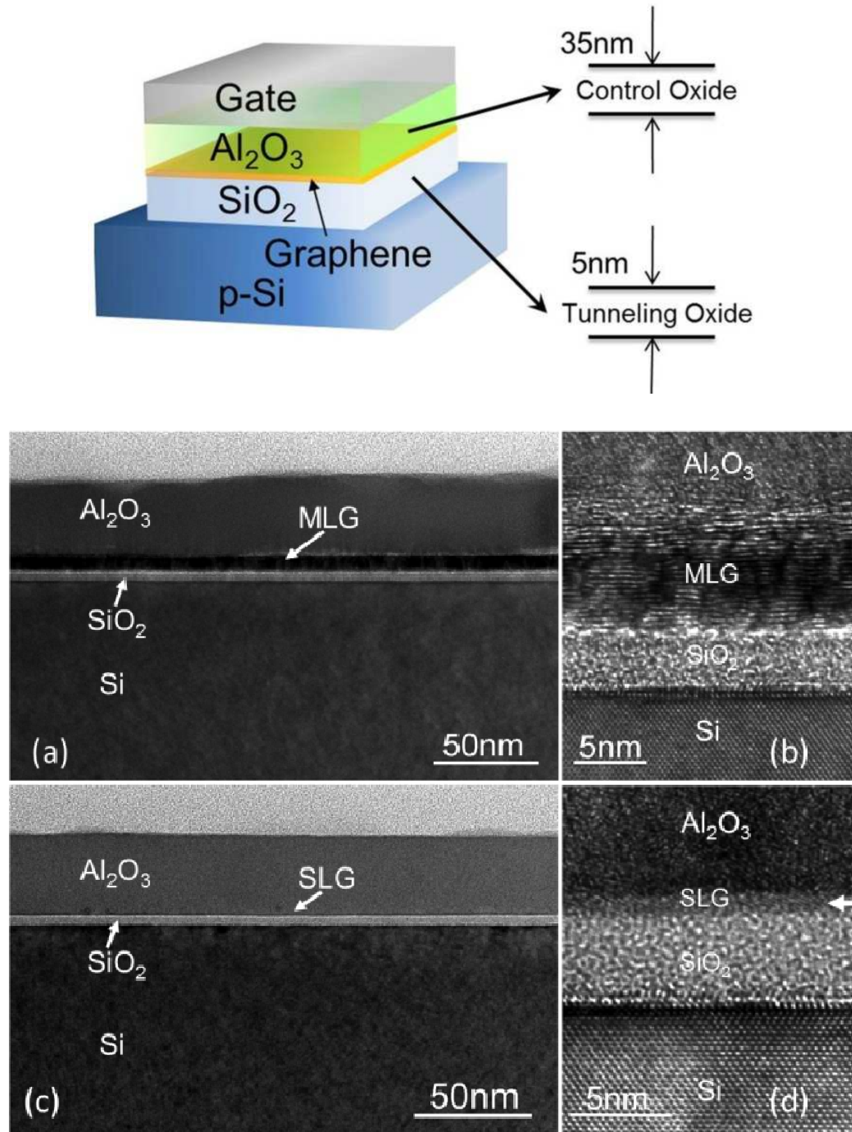


Figure 11. (Top) Device structure of graphene floating-gate flash memory. (Bottom) Cross-sectional TEM images of multi-layer graphene (MLG) flash memory and single layer graphene (SLG) flash memory devices. (a) A TEM image of MLG flash memory with 35 ± 1 nm Al_2O_3 control oxide grown on an approximately 9 nm multi-layer graphene. (b) A HR-TEM image of MLG flash memory shows graphene layers and the 5 ± 0.2 nm thick SiO_2 tunnel oxide. (c) A TEM image of SLG flash memory with 35 ± 1 nm Al_2O_3 control oxide. (d) A HR-TEM image of SLG flash memory shows the contrast difference between SLG and 5 ± 0.2 nm thick SiO_2 tunnel oxide.

Figure 12 shows the performance of as fabricated devices along with a control. While the SLG devices exhibit a window width of ~2V using a write/erase voltage of ±7 V (Figure 12b), MLG devices show a window width of >6V (Figure 12a). The greater memory window of the MLG devices is directly attributable to a larger thickness present in MLG as compared to that in SLG. The smaller memory window in SLGFM compared to MLGFM is a result of the SLG being only one atom thick (~0.35 nm), which is thinner than the inter-layer screening length of the MLG (λ = 0.6~1.2 nm).[69-71] In a metallic capacitor, the stored charges redistribute themselves on the surface to minimize the coulomb potential energy, and the characteristic thickness in which the charges reside is called the Thomas-Fermi (T-F) screening length. In general, metals have an extremely short T-F screening length of about several atomic layers; however, graphene is only one atom thick, thus restricting the charge storage capacity to one layer. By adopting a theoretical model[69] and using the ratio of the stored charges (memory window) between our MLGFM and SLGFM, $Q_{MLGFM} / Q_{SLGFM} \approx 1.6 \times 10^{-6}$ C/cm^2 / 5.33×10^{-7} C/cm^2 ~ 3 ($\approx \Delta V_{MLG}$ / $\Delta V_{SLG} \approx$ 6V / 2 V ~ 3), we find the screening length to be λ = 0.8 nm, which is consistent with the reported values (See section 2-2. Materials and Methods for Graphene Flash Memory, which contains the extraction method of stored charge carrier density). The insignificant memory effect of 20mV observed in the control device further confirms that the charges are being stored in the graphene layer(s).

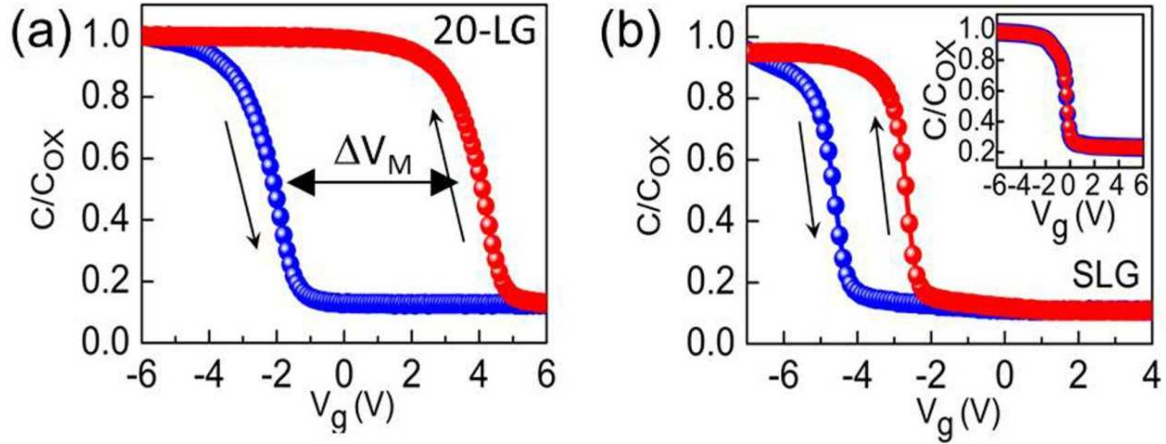


Figure 12. Capacitance-Voltage (C-V) measurements on graphene flash memory devices. (a) MLG flash memory exhibits an excellent counter-clockwise memory effect with a 6 V memory window. (b) SLG flash memory shows a 2 V memory window at a negative threshold voltage, which results from hole charge carriers in graphene. (Inset) C-V characteristics of the control device without graphene show negligible memory effect. In all figures, the forward/backward bias sweep ranges were ±7 V with a step time and step voltage of 0.1 second and 0.1 V, respectively, during all measurements. The capacitance of the devices was normalized to the capacitance of the control oxide (C_{ox}).

The counter-clockwise memory effects, as indicated by arrows in each plot, show that electron transfer through the tunnel oxide dominates the electron charge-discharge rate. Conversely, a clockwise memory effect can arise due to a leaky control oxide resulting in electron transfer through the control oxide.[72] Consequently, devices with a clockwise memory effect cannot be used in integrated circuits. Therefore, having a control oxide with a low leakage current on graphene is one of the most critical aspects to fabricate graphene flash memory. A minimal leakage current of 7×10^{-7} A/cm^2 at -10 V corroborates charge transfer through the tunnel oxide (See section 2-2. Materials and Methods for Graphene Flash Memory for methods to improve leakage current characteristics).

We noticed that the initial threshold voltage (forward bias regime) of the SLGFM shows a large negative value (-3.89 V) compared to the threshold voltage of the MLG flash memory (-1.33 V). This large negative threshold voltage in the SLG flash memory is observed as we need to apply an additional electric field to compensate for the holes and invert the p-type Si substrate. This indicates that single layer graphene is inherently p-type. This is consistent with reports that graphene is doped by atmospheric molecules, photoresist residue, and metal etchants and becomes heavily p-type.[73-75] Also, interfacial states at the oxide/graphene interface created by defects in graphene (the D band in Raman spectroscopy[3]) or dangling bonds of the oxide can induce additional positive charges inside the gate stack. All of the above can be applied to both SLG and MLG. However, MLG will be less sensitive to charge doping effects since the additional layers will screen and lessen the charge. Accurate contributions from defects and doping to initial threshold voltages should be further investigated.

The next figure of merit for flash memory devices is retention time, which refers to the potential lifetime of non-volatile storage. Generally, retention time requirements are more than 10 years before the device loses 50% of stored charge.[5] Loss of storage is typically the result of charge tunneling from the floating gate through the tunnel oxide. The rate of tunneling is dependent on the height and thickness of the electronic barrier presented by the tunnel oxide. In traditional polysilicon/SiO_2 devices, the barrier height ($\phi_{b\text{-}Si/SiO2}$ ~3.07) is fixed and simply the difference between the SiO_2 conduction band edge (0.95eV) and that of polysilicon (4.02 eV). This means that the minimum tunnel oxide thickness is limited to 7-8nm. In contrast, the graphene/SiO_2 system offers a larger electronic barrier height due to the higher work function of graphene (~4.6 ± 0.05 eV near the Dirac point).[76] This allows the tunnel oxide to be further thinned.

Figure 13 shows the energy band diagram of our MLG/SiO2/Si junction and experimental data for retention time of MLGFM at room temperature with a SiO_2 tunnel oxide of only 5 ± 0.2 nm (*i.e.* a 30 to 40 % thinner tunnel oxide than that used for polysilicon devices). Measurements indicate that a charge loss of only 8% should occur after 10 years (Figure 13a), which is more than adequate for practical devices. In order to understand the long retention time, multiple charge loss mechanisms can be considered; Schottky emission (SE), Fowler-Nordheim tunneling (FNT), Poole-Frenkel tunneling (PFT), and direct tunneling (DT) (See 4. Appendix for analytical expressions of various conduction processes in insulators). Under a normal retention state ($V_g = 0$), the electronic structure at the device interface is different before and after programming, which is illustrated in the band diagrams of Figure 13b. This is a result of the creation of an internal field across the tunnel oxide by stored charges in MLG (N_{MLGFM} ~10^{13} cm^{-2}). Both the existence of the large barrier height ($\phi_{b\text{-}G/SiO2}$ ~3.65eV) and low electric-field across the tunnel oxide make DT ($\propto \exp[-(\phi_b)^{1/2}]$) the most likely candidate for charge loss since the other mechanisms require high electric-fields to contribute significantly.[77] The increase in barrier height of $\Delta\phi_b$ ~0.58eV will reduce the DT probability by $\exp[-(3.65)^{1/2} + (3.07)^{1/2}] \approx 0.85$. However, DT is a low probability event. Thus, we believe that the DT mechanism is attributable to the long retention time of the constructed GFM devices.

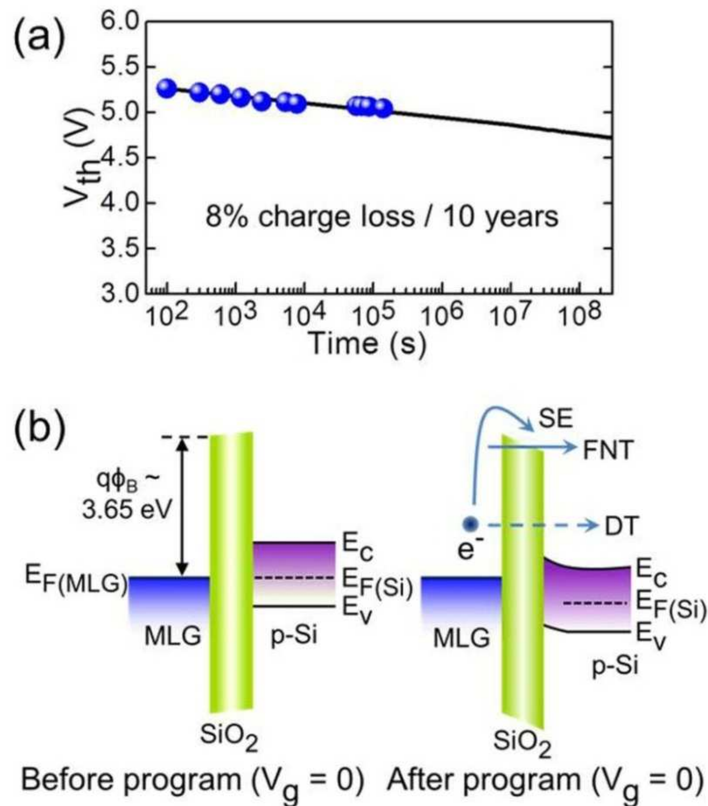


Figure 13. Retention characteristics of graphene flash memory: (a) Three possible mechanisms for charge loss during retention are Schottky emission (SE), Fowler-Nordheim Tunneling (FNT), and Direct Tunneling (DT). All three mechanisms depend exponentially on the barrier height (Φ_B) between the work function of graphene and the dielectric. (b) Retention measurement at room temperature shows only 8 % of charge loss in 10 years with a 5 nm thick tunnel oxide.

The final figure of merit for flash memory devices is cell-to-cell interference. For a 2D planar configuration, a given storage element is mainly influenced by its two nearest neighbors which share a same word line to their gates. This leads to variability in threshold voltage, and accordingly a bit error can easily occur between nearest neighbors when interference is significant. This is a complex interplay because the increasing thickness of the charge storage layer increases the gate coupling ratio and hence lowers the operating voltage, but also increases

the interference mainly due to an increase in side wall capacitance. A careful optimization must take place in order to minimize both the operating voltage and the cell-to-cell interference. Graphene offers a unique solution to this problem due to its thinness. This minimizes the resulting field upon charging by nearest neighbors and hence lowers the crosstalk between nearest neighbors. In some sense, lower interference is a result of graphene's lower GCR.

Simulations of both traditional polysilicon/SiO_2 and thin film metal-based devices are presented in Figure 14. The simulation is based on a thin film metal of 1nm, which is the T-F screening length of MLG with a work function of graphene corresponding to 4.6eV (See section 2-2. Materials and Methods of Graphene Flash Memory for detailed simulation conditions and parameters). The simulation results provide an upper limit for graphene devices, since graphene's DOS is less than conventional metallic systems. To understand the maximum interference on a given cell, we simulate the situation where two nearest neighbors are programmed at high gate voltages, while a given cell remains unprogrammed. We then monitor the threshold voltage shift of the unprogrammed cell due to its nearest neighbors. Simulation results show that the floating-gate flash memory experiences abruptly increasing interference as the device is scaled down below the 25 nm node. However, our graphene flash memory shows negligible interference down to a 10 nm gate length. The weakening of this interference effect shows that graphene indeed displays a huge advantage over polysilicon for this application.

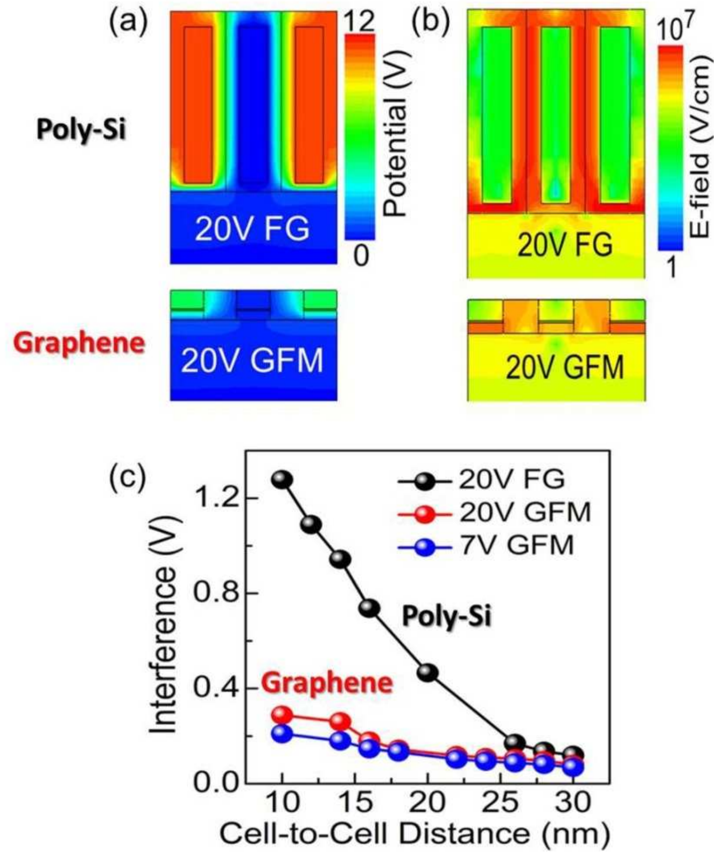


Figure 14. Cell-to-cell crosstalk in conventional poly-silicon floating gate (FG) flash memory and graphene flash memory (GFM). (a) Simulated electrostatic potential profile of three flash memory cells in series for FG (Top) and GFM (Bottom) at a program voltage of 20V. (b) Simulated electric-field profile of three flash memory cells in series for FG and GFM. (c) Cell-to-cell crosstalk of FG and GFM. Interference is defined as the threshold voltage (V_{TH}) shift of the unprogrammed cell (middle) influenced by the two nearest neighbor cells. Simulation results show significant interference that can cause a bit error in FG flash memory because of the large side wall capacitance. In contrast, the thinness of graphene lowers the crosstalk and makes it desirable for miniaturization.

Based on our device performance, we can roughly estimate the power reduction and increase in storage density compared to polysilicon floating gate flash memory. Graphene flash memory requires half the operating voltage to achieve a 1.5V memory window, which potentially reduces the operation energy per bit by ~75%, assuming the capacitive charging

energy is the limiting factor of such a device. Furthermore, the reduction of cell-to-cell crosstalk shows potential for twice the charge storage density at current industry standards of 0.2V cell-to-cell interference.[78]

In summary, our experiments demonstrate the benefits of graphene as a platform for flash memory. The high density of states, high work function, and low dimensionality positively influence device performance, leading to a wide window of operation, long retention time, and low cell-to-cell interference. The simulations pertaining to cell-to-cell interference further suggest that graphene may be instrumental in the next round of miniaturization of flash memory, far beyond the conventional limitations of current leading edge technology.

2-2. Materials and Methods for Graphene Flash Memory

(a) Graphene Growth by Chemical Vapor Deposition (CVD)

Single layer graphene was grown by a chemical vapor deposition (CVD) method (Figure 15 and Figure 16) using a tube furnace at 1000 ºC. Flow rates of 25 sccm for H_2 and 100 sccm for CH_4 were used at pressures of 1.5 Torr and 6 Torr, respectively. 25 µm thick copper foils, purchased from Alfa-Aesar, were loaded into the tube and annealed for 10 minutes at 1000 ºC to remove the oxide before introducing the precursor and carrier gases. Growth was complete after 15 minutes. Multi-layer graphene was grown on metal catalysts such as 400 nm thick Ni/SiO_2 using a separate CVD system for Ni catalysts only under the flowing precursors, CH_4:H_2 (50 sccm: 250 sccm) at 950°C for 3 min. The annealing process was performed at 1000°C for 1 hr under H_2/Ar gas prior to the growth. The rate of cooling down was approximately 20°C/min with Ar gas under ambient conditions.

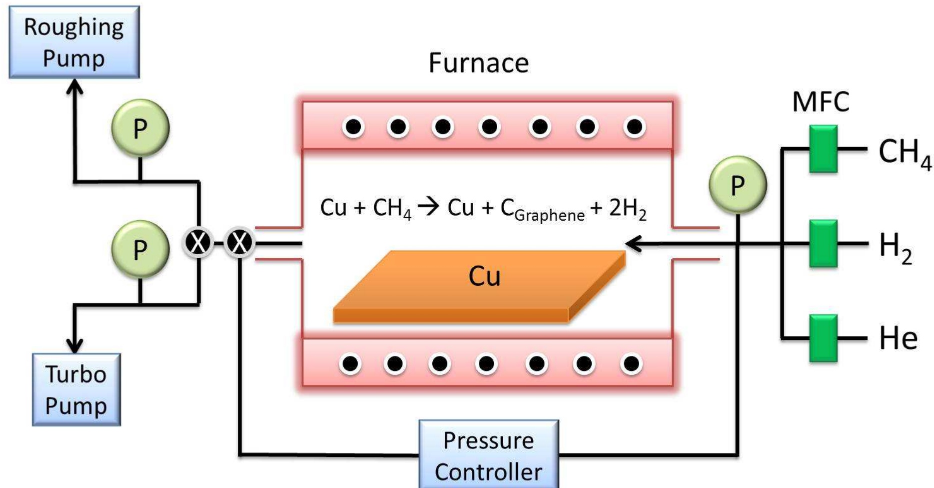


Figure 15. Schematic of CVD system for graphene growth on Cu. The mass flow controllers (MFC) regulate the gases that enter the growth chamber (furnace). The turbo pump is used to set the chamber under high vacuum (10^{-6} Torr) to remove any contaminants in the chamber. The turbo pump regulates the anneal and growth pressure by means of a pressure controller, which utilizes a feedback loop by reading the pressure gauges (P).

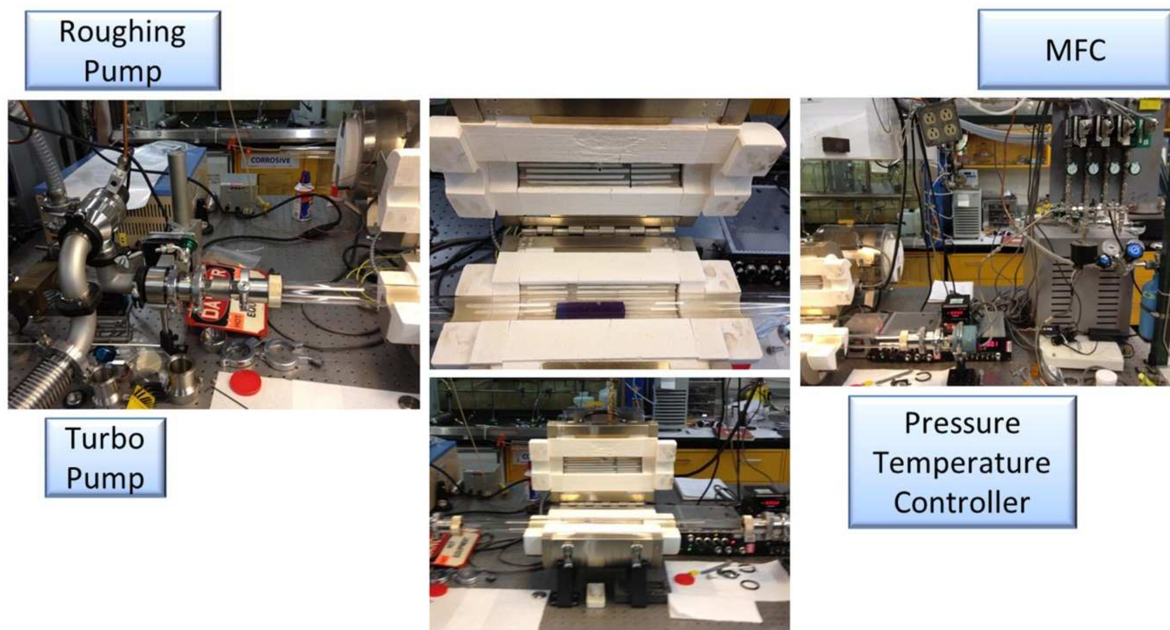


Figure 16. Custom-built CVD system for graphene growth on Cu. The left image shows the T-junction that is used to isolate the turbo pump from the roughing pump. The center two images display the furnace, the two-inch quartz tube, and the sample within the chamber. The right image shows the pressure and temperature controllers, the MFCs, and the gas lines.

(b) Graphene Transfer onto Arbitrary Substrates

As shown in Figure 17, a PMMA, purchased from Micro-Chem, was spin-coated onto the resulting graphene-coated foil to protect the graphene layer and act as a rigid support after the copper was etched away in an aqueous bath of $FeCl_3$, H_2O and HCl (3.5 g, 100 ml and 10 ml, respectively). After the transfer was complete, a second layer of PMMA was used to dissolve the first PMMA layer and relax the strain in the underlying graphene layer. After curing, the PMMA was removed in acetone.

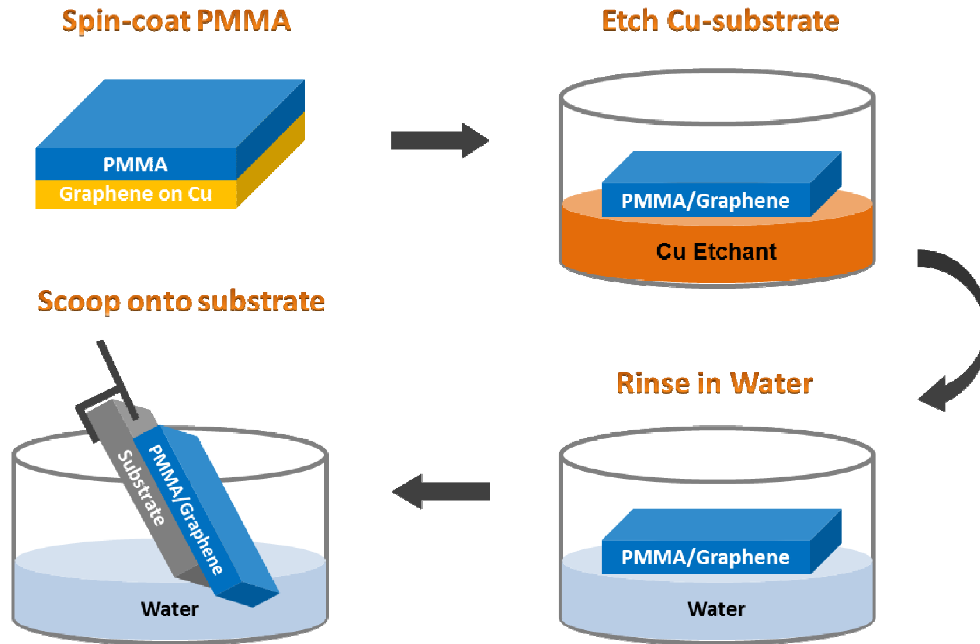


Figure 17. Process of CVD graphene transfer to arbitrary substrates. First, PMMA is spin-coated onto graphene. Then, the PMMA/graphene/Cu sample is placed floating on the Cu etchant to etch the underlying Cu substrate. Next, the bottom of the PMMA/graphene sample is rinsed through water. Finally, the PMMA/graphene sample is scooped from the water surface onto the targeted substrate.

(c) Graphene Characterization through Raman Spectroscopy

Prior to device fabrication, SLG and MLG were characterized via Raman spectroscopy (Figure 18) to ensure the quality of the materials. After transferring MLG and SLG sheets onto Si substrates with tunnel oxide, a quick and direct method to identify the quality and quantity of graphene is to analyze its "fingerprint" with Raman spectroscopy (Figure 19) on SiO_2 (See section 4. Appendix for a detailed description of Raman active phonon modes and corresponding Raman spectrum of graphene). A Raman spectrum of graphene grown by the nickel CVD method is shown in Figure 18a. Here, the large G:2D band ratio is representative of multilayer graphene. In contrast, for graphene grown by CVD on copper, the intensity of the 2D band is at

least twice that of the G band (Figure 18b) indicative of single layer graphene. Both MLG and SLG Raman spectroscopy show a small disorder (D) band.

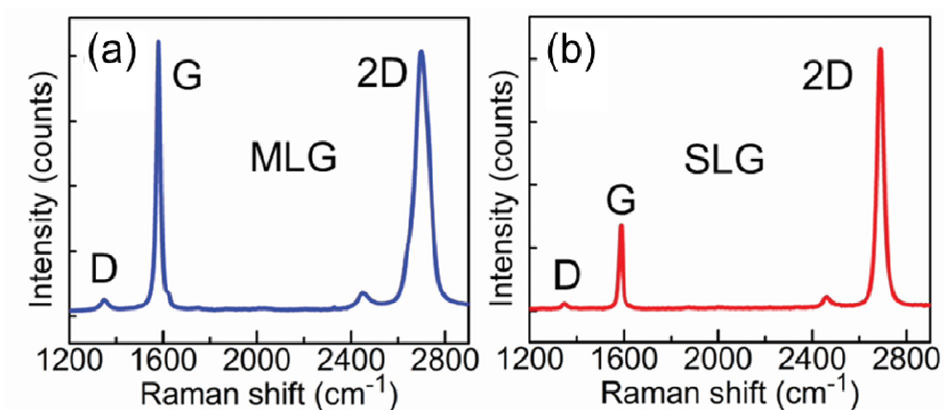


Figure 18. Raman spectrum of CVD graphene. Graphene grown on a metal catalyst in a CVD system was transferred and characterized with Raman spectroscopy. (a) A Raman spectrum of the graphene sheet grown on Ni. Multi-layer graphene (MLG) sheets formed because Ni has much higher carbon solubility than Cu, which resulted in carbon precipitation during the cooling process. (b) A Raman spectrum of the graphene sheet grown on Cu. Mainly single layer graphene (SLG) formed because of the low carbon solubility in Cu.

Figure 19. Renishaw micro-Raman spectrometer.

(c) Creation of Nucleation sites for Al_2O_3 Deposition on Graphene

To prevent loss of data in flash memory, it is imperative to reduce the amount of leaked current from the gate. We describe a simple method using an Al passivation layer, which reduces the number of pinholes on the surface and enhances the uniformity of barrier layer. We find that simply depositing aluminum oxide produces a non-uniform oxide layer. We attribute this result to the hydrophobicity and absence of dangling bonds of graphene because this type of surface is not conducive for providing appropriate nucleation sites for metals grown through ALD (i.e. ALD utilizes chemical reaction for a controlled layer by layer deposition). To achieve a high quality dielectric layer on graphene, Kim et. al.[79] demonstrated a high mobility top-gated graphene field effect transistor using a two-step gate stack process where a 1-2 nm thick layer of aluminum was evaporated onto the surface of graphene followed by the deposition of Al_2O_3 by ALD. We utilize a slightly modified two-step gate stack process in which we prepare an aluminum oxide layer. Our aluminum oxide passivation layer is made by e-beam evaporating an 11 Å layer of aluminum, which we allow to completely oxidize (within two days). Subsequently, Al_2O_3 is deposited by ALD on this surface to produce a high quality control oxide for our GFM.

With this process, we observe a significant reduction in leakage current in our GFM devices. Figure 20a shows typical leakage current characteristics in the absence of the aluminum oxide passivation layer. Here we find that there is an extremely large leakage current and a dielectric breakdown when only -4.4 V is applied to the gate. Additionally, memory effects from GFM devices with leaky oxides are negligible. GFM prepared with the Al oxide passivation layer shows a significant reduction of leakage current. We attribute the observed memory effects from MLGFM and SLGFM to the enhanced interface between the graphene and aluminum oxide. Figure 20b shows a minimal leakage current of 7×10^{-7} A/cm^2 at -10 V for our GFM device.

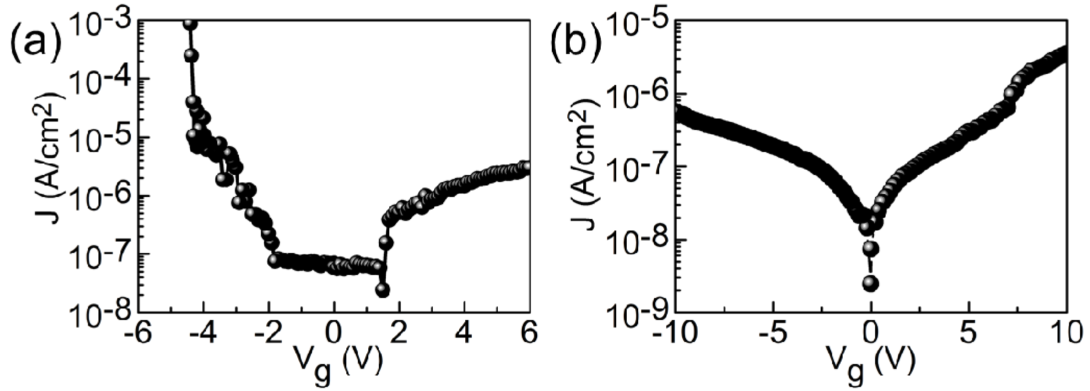


Figure 20. Gate leakage current density of GFM. (a) Gate leakage characteristics of GFM without an oxidized Al nucleation layer before Al_2O_3 deposition by ALD. (b) Gate leakage characteristics of GFM with an oxidized Al nucleation layer prior to Al_2O_3 deposition by ALD shows minimal leakage current of 7×10^{-7} A/cm^2 at -10 V gate voltages.

(d) Electrical Measurement Conditions

All capacitance-voltage measurements were carried out using a Keithley CV 590 at f = 100 kHz with ramping rate (1 V/s), voltage step (0.1 V), and step interval (100 ms).

(e) Electrostatic Device Simulations

The simulation on potential distribution and cell-to-cell interference was obtained through Sentaurus (Version D-2010.03) from Synopsys. A 1nm thick conductor (~trilayer graphene) with a work function of 4.6eV was used to simulate graphene. The device dimensions and materials were identical on both devices except for the charge storage layers. The parameters used in the simulation were a 5 nm SiO_2 tunnel oxide, a 10 nm SiO_2 control oxide, 10^{17} cm^{-3} silicon substrate doping, 10^{20} cm^{-3} source/drain doping, and a SiO_2 insulation material between adjacent cells. For cell-to-cell interference, the floating-gate material and the insulation material

present between adjacent cells are the dominant factors in FG structure. The usage of 10nm SiO_2 control oxide instead of 35 nm Al_2O_3 does not substantially affect the interference between cells nor diminish capacitive coupling on the channel. A high substrate doping and the maximum transconductance (g_m) method were used to circumvent short channel effects, particularly drain induced barrier lowering (DIBL), and determine the V_{th}, respectively.

(f) Calculation Method of Charge-Storage-Density per Unit-Cell in GFM

The amount of stored charges in GFM can be derived using electrostatic analysis on the floating gate capacitor structure. The following equation shows the basic relationship between material parameters

$$V_{TH} = \Phi_{ms} - \frac{Q_d}{C_{OX}} + 2\Phi_F$$

where Φ_{ms} is the work function difference of the metal (Φ_m) and the semiconductor (Φ_s), Φ_F is the potential difference between the Fermi level (E_F) and the intrinsic Fermi level (E_i), Q_d is the depletion charge, and C_{OX} is the capacitance of the oxide (Figure 21a). The V_{TH} of a MOSFET can be defined as the gate voltage where the inversion layer forms. To turn "on" the MOSFET, the applied voltage must be large enough to achieve the flat band condition (Φ_{ms}), accommodate the charges on the depletion region (Q_d/C_{OX}), and further induce strong inversion ($2\Phi_F$).

Figure 21b illustrates how flash memory defines its Data 1 and Data 0 using V_{TH} shift (ΔV_{TH}). Electrons tunnel through the oxide and reside on the charge storage layer when a

sufficient positive voltage is applied to the gate. In FG flash memory, the ΔV_{TH} is simply the additional voltage required to compensate the stored charges underneath the control oxide induced by the programming. In our GFM devices, two capacitors are in series and the ΔV_{TH} can be expressed as

$$\Delta V_{TH} = \frac{d_{CON}}{\varepsilon_{CON}} \times \frac{1}{A} \times \Delta Q$$

where d_{con}, ε_{con} are thickness and permittivity of the control oxide, A is the device area and ΔQ is the stored charge after programming. Using this relation between ΔV_{TH} and ΔQ, we calculate the stored charge in MLG flash memory ($\Delta Q_{MLGFM} = 1.12 \times 10^{-11}$ C) and SLG flash memory ($Q_{SLGFM} = 3.73 \times 10^{-12}$ C) at ±7 V Program/Erase voltages.

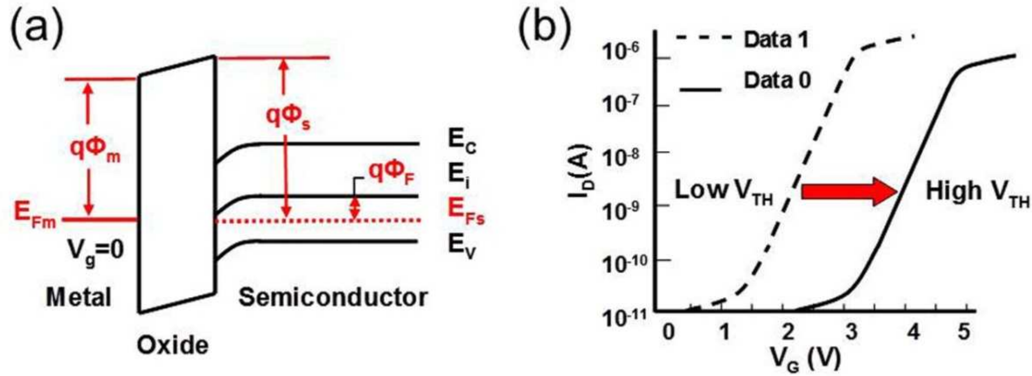


Figure 21. Conventional Flash Memory (a) Energy band diagram of a generic MOS structure. Φ_m and E_{Fm} refers to the work function and Fermi level of the metal, Φ_F is the potential difference between the Fermi level (E_{Fs}) and the intrinsic Fermi level (E_i) of the semiconductor, and Φ_s is the work function of the semiconductor. (b) Definitions of Data 1 and Data 0 using I_D-V_G characteristics of flash memory; the position of the onset in current flow (V_{th}) determines the binary datum.

(g) Extraction Method of V_{TH} in GFM

The ideal V_{TH} (Φ_m = 4.6V) of GFM can be estimated using

$$V_{TH} = \Phi_{ms} + 2\Phi_F + \frac{\sqrt{4\varepsilon_{si} q N_a \Phi_F}}{C_{OX}}$$

where ε_{si} is the silicon permittivity (= 1.04×10^{-12} F/cm), and N_a is the substrate doping concentration (= 10^{15} /cm^3). The Φ_F can be calculated using the following equation,

$$\Phi_F = \frac{kT}{q} \ln(\frac{N_a}{n_i})$$

where k is the Boltzman's constant (= 1.38×10^{-23} J/K), T is the temperature (K), q is the electronic charge (= 1.6×10^{-19} C), and n_i is the intrinsic carrier concentration of silicon (= 1.4×10^{10} /cm^3, at room temperature). The ideal V_{TH} of GFM is calculated to be -1.14V.

In our experiments, the V_{TH} of GFM were extracted from the C-V curves by calculating the flat band voltage (V_{FB}) from the flat band capacitance (C_{FB}).[S1]

$$\frac{1}{C_{FB}} = \frac{1}{C_{OX}} + \sqrt{\frac{kT}{\varepsilon_{si} q^2 N_a}}$$

This can be approximated to $V_{TH} \sim V_{FB} + 2\Phi_F$, since the low substrate doping N_a results in a small depletion charge Q_d. The extracted V_{TH} for MLGFM is -1.33 V and for SLGFM is -3.89 V.

2-3. Graphene Ferroelectric Memory (FeFET)

Graphene is considered to be a novel material with high potential for future electronics, owing to its excellent electronic properties. For example, the linear electron energy dispersion leads to both Klein tunneling[10] and high room temperature mobility,[75] which are beneficial for high speed electronics. If feasible, an all graphene-based circuit, including logic, analog, and memory devices, would be of great interest to further extend the performance of current Si-based electronics. In addition to achieving such goals, there has been an enormous amount of effort to better understand and resolve current limitations that are inherent in graphene for electronic applications. For instance, a bandgap has been introduced in graphene through quantum confinement[80,81] or symmetry breaking of the stacking order[82] for logic applications. In particular, a graphene transistor operating at 300GHz[60] has been demonstrated for analog applications. Furthermore, graphene has been artificially synthesized by thermal evaporation of Si on SiC[83] and chemical vapor deposition (CVD) of carbon precursor molecules on metal catalysts[46,47] for large scale production. Graphene based memory structures, however, are still in their infancy in comparison to its logic and analog applications. To date, graphene memory has been demonstrated through chemical modification[84] and atomic electromechanical switches,[85,86] all of which modify the graphene's electronic properties through a reversible destructive mechanism creating potential challenges for its long term operation.

One prospective candidate for a nondestructive graphene based memory device is a graphene ferroelectric-field-effect-transistor (FeFET)[87] for nonvolatile ferroelectric-random-access-memory (FRAM), which has remarkable advantages over existing nonvolatile memories. The superior characteristics of a FeFET include a small memory cell size, low power consumption, fast write speed, and nondestructive readout operation.[88-90] The fundamental

mechanism of a FeFET exploits two distinct properties, which come from both the hysteretic ferroelectric gate oxide and the transconducting channel. A binary datum of an FeFET memory cell can be programmed on the ferroelectric material as an electric polarization direction by applying a voltage between a gate electrode and a transconducting material. Depending on the stored polarization direction (i.e. up-poled or down-poled), the channel conductance changes and the stored datum can be read out by sensing a source-drain current in the absence of an applied bias on the gate.

For the past few decades, various FeFET structures have been made with different ferroelectrics and semiconductors to improve memory performance.[91,92] One of the biggest challenges is to increase the gate coupling strength without degrading the hysteresis effect from depolarizing fields and intrinsic voltage drops, which originates from insertion of an additional dielectric layer to resolve the poor interface between the ferroelectric and semiconductor channel.

Graphene provides a distinctive advantage over semiconductor materials because of its two-dimensional nature and the nonexistence of dangling bonds, which offers a non-reactive robust interface for the transconducting channel of a FeFET. In addition, graphene can be placed directly on the ferroelectric material, eliminating the need for an additional sacrificial dielectric layer. Furthermore, the 2D nature of graphene renders an absence of depletion capacitance, which can further restrict the amount of capacitive coupling between the ferroelectric oxide and channel material. This high coupling strength can enable high On/Off ratios and reduce the operating voltage (Figure 22). Current work on single-layer graphene (SLG) FeFET has been limited to the use of ferroelectric polymers due to the visibility of graphene on specific substrates.[93-95]

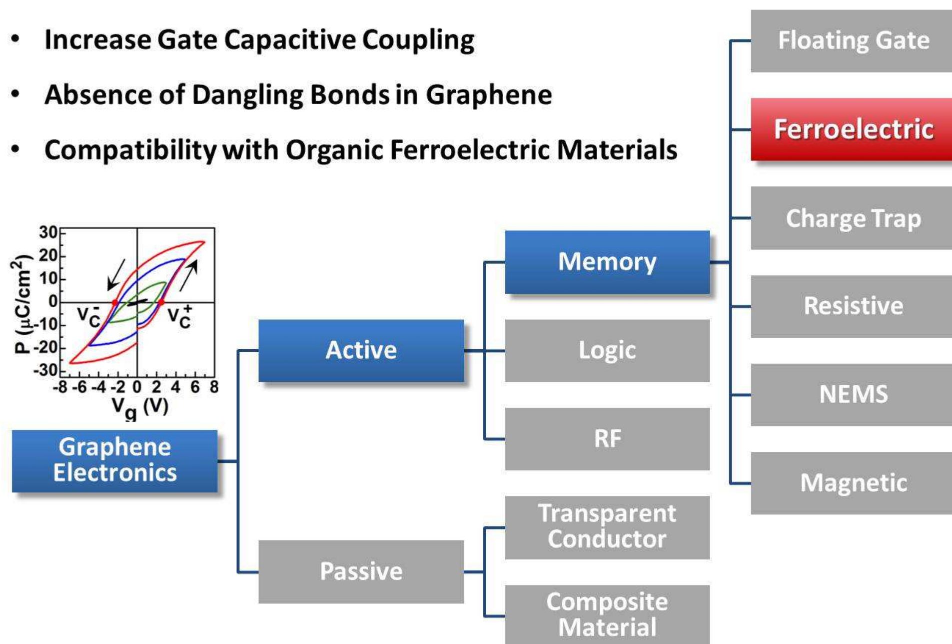


Figure 22. Graphene Ferroelectric Nonvolatile Memory – Objectives; reduce operating voltage by increasing capacitive coupling.

Here we demonstrate a SLG-FeFET with the solid-state ferroelectric material, lead zirconate titanate (PZT). Among the solid-state ferroelectric materials, PZT is of particular interest because of its high remnant polarization and low coercive field values, which is well suited for low power nonvolatile FRAM application. We show that mechanically exfoliated SLG can be optically identified on a ferroelectric PZT substrate and exhibit a hysteresis of the V-shape conductance with a large memory window at low operating gate voltages. Furthermore, we compare exfoliated SLG-FeFETs with CVD SLG-FeFETs and show that devices made of CVD SLG exhibit a robust bi-stable feature with long retention time, which are ideal for high performance memory applications.

In order to construct the SLG-FeFET we first engineered a ferroelectric substrate to identify SLG. It is known that SLG is invisible under the optical microscope unless the underlying layers are optimized for high contrast.[3,96] In order to make graphene visible on the ferroelectric PZT substrate, theoretical contrasts values were calculated depending on the incident wavelength and PZT thickness by applying Fresnel's model of a three layer system SLG/PZT/Pt (Figure 23a).

$$I(\lambda) = \left| \frac{r_1 + r_2 e^{-i\Delta_1} + r_3 e^{-i(\Delta_1+\Delta_2)} + r_4 e^{-i(\Delta_1+\Delta_2+\Delta_3)} + r_1 r_2 r_3 e^{-i\Delta_2} + r_1 r_3 r_4 e^{-i\Delta_3} + r_1 r_2 r_4 e^{-i(\Delta_2+\Delta_3)} + r_2 r_3 r_4 e^{-i(\Delta_1+\Delta_3)}}{1 + r_1 r_2 e^{-i\Delta_1} + r_1 r_3 e^{-i(\Delta_1+\Delta_2)} + r_1 r_4 e^{-i(\Delta_1+\Delta_2+\Delta_3)} + r_2 r_3 e^{-i\Delta_2} + r_3 r_4 e^{-i\Delta_3} + r_2 r_4 e^{-i(\Delta_2+\Delta_3)} + r_1 r_2 r_3 r_4 e^{-i(\Delta_1+\Delta_3)}} \right|^2$$

where, $r_i = (n_i\text{-}1\text{-}n_i)/(n_i\text{+}n_i\text{-}1)$ are the reflection coefficients for different interfaces, and $\Delta_j = 4\pi n_j d_j/\lambda$ are the path differences for different layers. $d_G = 0.34$nm (extension of the π-orbital) and $n_G = 2.6\text{-}1.3i$ was used for the thickness of MLG and the complex refractive index, independent of wavelength, respectively.

In this model, a 150nm Pt thin film was used as the terminating layer because of its shallow skin depth of 25nm at a wavelength of 700nm. The optical constants, refractive index, *n*, and extinction coefficient, *k*, of PZT films were obtained through ellipsometry measurements (See section 2.4 Materials and Methods for Graphene Ferroelectric Memory which contains the experimental values of the optical constants in PZT). Upon normal incidence, 97% of the light penetrates through graphene and undergoes multiple reflections creating an interference enhancement in the PZT layer, resulting in a high optical contrast. Based on simulation results, an optimal PZT thickness of 180nm was chosen to have a large capacitive coupling for field

effect and to allow SLG to exhibit high contrast under 600nm wavelength visible light (Figure 23b).

PZT substrates were prepared by a conventional sol-gel process (see section 2-4. Materials and Methods for Graphene Ferroelectric Memory, which explains the details of the sol-gel process) on a thermally oxidized SiO_2/Si wafer with Ti/Pt as buffer layers. A 180nm PZT thickness was obtained through 6-layers of PZT films to decrease the surface roughness and increase the van der-Waals interaction between graphene and the PZT for better adhesion. This allowed large SLGs with areas of more than 20 μm^2 to be easily isolated and located under an optical microscope at λ = 600nm when mechanically exfoliated onto the surface of the PZT substrate (Figure 23c). Finally, Raman spectroscopy was used to characterize both exfoliated and CVD graphene samples which exhibit single Lorentzian peaks at the G and 2D bands. An absence of the D band, and a high 2D/G ratio (>2) clearly confirms the existence of high-quality monolayer graphene (Figure 23d).[47,97]

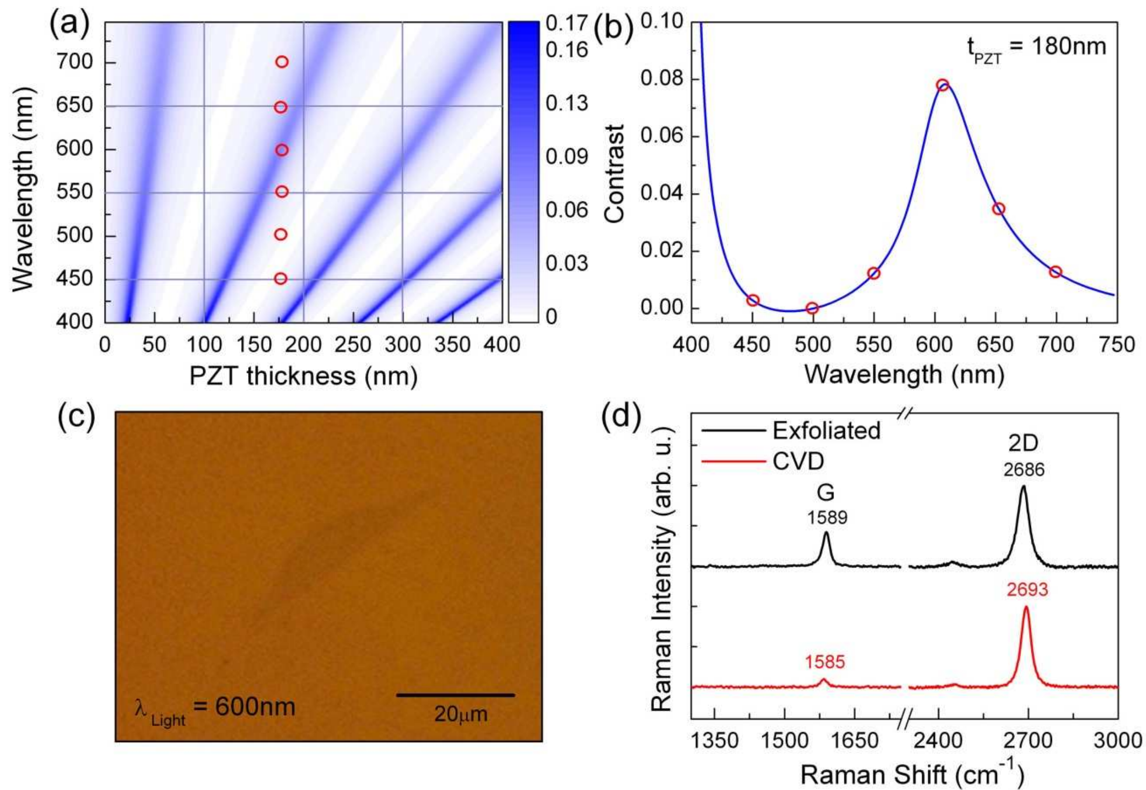


Figure 23. Visibility and Raman spectrum of graphene on PZT (a) 3D color plot of the contrast as a function of wavelength and PZT thickness. The color scale on the right shows the expected contrast. (b) 2D plot of the contrast as a function of the wavelength at 180nm PZT thickness. The red circles indicate equivalent points in figures at top row. (c) Optical micrograph of a large exfoliated single-layer graphene on 180nm thick PZT substrate at 600nm visible wavelength. A variable interference filter with a FWHM of 10nm was used. (d) Raman spectrum of exfoliated single-layer graphene and CVD single-layer graphene on a PZT substrate. The absence of the D band (~1350cm-1) and the high 2D/G (> 10) ratio indicates high quality CVD grown single-layer graphene.

Two-terminal SLG-FeFETs were then fabricated using standard e-beam lithography and photolithography for exfoliated graphene (Figure 24b) and CVD graphene, respectively, to deposit Ti/Au metals as source and drain electrodes. The Pt layer underneath the PZT was used as the gate electrode (Figure 24a). Leakage currents were less than 1nA when 7V was applied between the channel and gate electrodes (See Materials and Methods). The channel lengths

ranged from 0.8 ~ 10μm with a length to width ratio of 0.5 ~ 2. Electrical measurements were performed at room temperature in a vacuum environment with a pressure of $1.1x10^{-6}$ Torr. In order to characterize device behavior, a source-drain bias (V_{ds}) was kept constant while the gate voltage (V_g) was swept in a closed loop from 0V → $+V_{g\,(sweep)}$ → $-V_{g\,(sweep)}$ → 0V, where $V_{g\,(sweep)}$ is the maximum sweep voltage of the gate. All I_d-V_g measurements were repeatable with current values following the same paths.

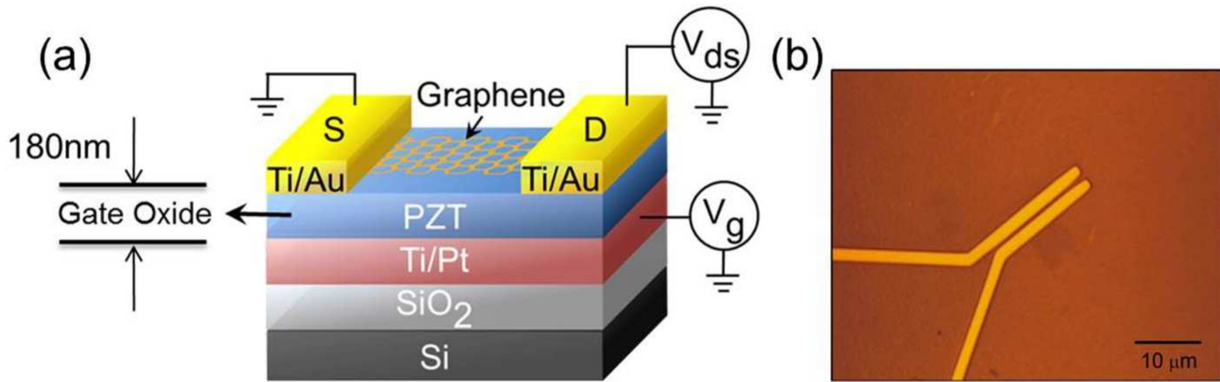


Figure 24. (a) Schematic device structure of graphene FeFET on the PZT substrate. Au/Ti was used for source/drain electrodes and the Pt layer was used for the back gate. (b) Optical micrograph of two-terminal graphene FeFET fabricated by e-beam lithography.

For the exfoliated SLG-FeFETs, a hysteretic behavior of the drain current is clearly observed with a double minimum symmetry when the gate voltage is swept, which results from the nonlinear hysteretic characteristics of the ferroelectric PZT (Figure 25a). In order to understand the observed conductance behavior we use the continuity condition of the electric displacement field at the interface of graphene and PZT, which is expressed as

$$n(V_g, n_0)e = n_0 - \alpha P(V_g),$$

where $\alpha P(V_g)$ is the electric-field induced carrier concentration from the nonlinear ferroelectric polarization, α is the capacitive coupling efficiency between graphene and PZT, and n_0 is the residual doping of graphene from the environment.[95] The two minimum conductance points occur at both the positive V_g and negative V_g sweep, which we define as V^+_{gmin} and V^-_{gmin}, respectively. At V^+_{gmin} and V^-_{gmin}, the Fermi level aligns with the Dirac point, and is satisfied when the electrostatic potential from the ferroelectric dipoles compensate the preexisting potential caused by the residual dopants (i.e. $n_0 \approx \alpha P(V_g)$). Furthermore, the minimum conductivity has a value of $4e^2/h$, which is related to the high dielectric constant (κ ~ 510, see section 2-4. Materials and Methods for Graphene Ferroelectric Memory, which contains experimental values of the dielectric constant of PZT) of PZT and coincides with previous values in high-κ environments.[98]

Several observations of the transport behavior should be noted to better understand practical device operation. We observe the ratio of hysteretic switching between maximum and minimum conductance of 250%. The maximum conductance occurs where the current saturates in the high carrier density regime ($n > 10^{12}/cm^2$) and is determined by short-range scatterers, such as, defects, ripples, and phonons.[99] The asymmetry of the saturation between hole and electron conduction, as seen at maximal negative or positive gate voltages, respectively, is attributed to a doping effect of the contact metals near the graphene/metal interface.[100] In addition, the dissimilar electrode materials form capacitive contacts to PZT, here graphene and

Pt, which are known to create a positive offset on the hysteresis behavior through ferroelectric domain pinning near the metal/ferroelectric interface.[101]

In the case of CVD SLG-FeFETs, the main difference in comparison to the exfoliated SLG is the initial doping level n_0 and the presence of carrier dependent scattering sources,[102,103] where heavy chemical doping is introduced from the etchant solution during the process of removing the copper catalyst.[104,105] The chemical doping shifts the Fermi level below the Dirac point and suppress the modulation of electron charge carriers. These effects give rise to the observed hysteresis behavior, which is shown in Figure 25b. This is analogous to what is observed for dual-gated graphene polymer-FeFETs.[95]

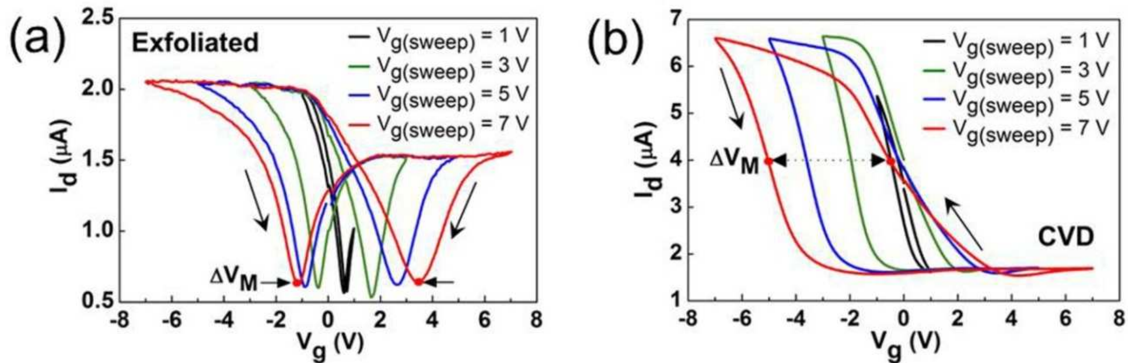


Figure 25. (a) Hysteresis characteristics of the exfoliated single-layer graphene FeFET with varied $V_{g\ (sweep)}$. Electrical measurements were performed at V_{ds} = 0.5mV. (b) Hysteresis characteristics of CVD single-layer graphene FeFET with varied $V_{g\ (sweep)}$. Electrical measurements were performed at V_{ds} = 5mV.

A desirable condition for a functional memory device is a bi-stable current state. Although, one can operate the exfoliated graphene FeFET's by using an asymmetrical loop sweep on the gate voltage[94] to achieve memory functionality, the ambipolar conduction behavior

of graphene creates a minimum conductance point within a small voltage range (0.1 ~ 0.3V) and produces an unstable current state, $d^2I/dV_g^{\ 2} < 0$ near $V_g \approx$ Dirac point. The doped CVD graphene, however, offers an advantage by suppressing the electron modulation and creating a bi-stable state that can operate at a large voltage range with an enhanced stability.

A logical question is whether the hysteresis of the devices comes from the ferroelectric property of PZT alone or other unintentional effects, such as adsorption and desorption of atmospheric molecules on graphene. In order to relate the electrical hysteresis characteristics of the graphene FeFET directly to the ferroelectric properties of PZT, subsequent I_d-V_g measurements were taken at varying $V_{g\ (sweep)}$ (Figure 25) and corresponding polarization measurements were performed under the same $V_{g\ (sweep)}$ (inset of Figure 26). This was done on a capacitor structure of Pt/PZT/Ti/Au on the same PZT substrate as the device. As $V_{g\ (sweep)}$ was increased, both the coercive voltage (V_C) and remnant polarization (P_R) nearly saturated at $V_{g\ (sweep)}$ = 7V with E_C ~130 kV/cm and P_R ~ 25 μC/cm^2, which are inherent material properties dependent on the fabrication method of thin film PZT.

In a FeFET, the memory window (ΔV_M) is theoretically equal to twice the V_C of the ferroelectric dielectric medium. In our capacitor structure, however, the V_C's are not identical for opposite polarization directions. Thus, we define the degree of hysteresis as $\Delta V_M = V_C^+ - V_C^-$. For the exfoliated graphene FeFET, it is rational to define the degree of hysteresis as the voltage difference of the minimum conductance points. In the case of CVD graphene FeFET, we define the memory window as the difference in gate voltages that occur at the current value corresponding to the midpoint of the maximum and minimum possible current values of the device. These are clearly labeled in figure 25a and 25b. With these definitions, we compare the memory window obtained at subsequent sweeping voltages between the SLG-FeFET and PZT

capacitor (Figure 26). As $V_{g\ (sweep)}$ is incrementally increased, both the memory windows increases and nearly saturates near 7V. These observations confirm that the electrical hysteresis of the graphene FeFET originates from the ferroelectric property of the underlying PZT material. In traditional semiconductor FeFETs the memory window is less than $2\times V_C$.[106,107] However, in our work, both the exfoliated and CVD SLG show a significant advantage since the window width is nearly identical to the hysteresis of the PZT.

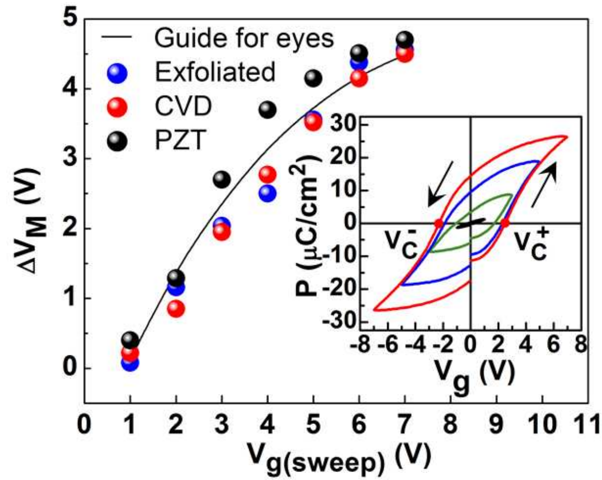


Figure 26. Degree of capacitive coupling for graphene FeFET illustrated by the memory window as a function of $V_{g\ (sweep)}$. The blue and red circles correspond to the memory windows extracted from transfer characteristics of exfoliated graphene and CVD graphene FeFET, respectively. The black circles corresponds to the memory window ($\Delta V_M = V_C^+ - V_C^-$) extracted from the P-V relations of the PZT capacitor next to the device on the same substrate. (Inset) Polarization characteristics of a 180nm thick PZT capacitor depending on $V_{g\ (sweep)}$. The coercive voltage (V_C) is defined as the intercept of the *x*-axis.

Another important factor to consider when characterizing a nonvolatile memory device is its retention time. The retention time of a memory device is a measure of the devices ability to produce high fidelity output after writing stored data. Figure 27b displays the retention

characteristics of the bi-stable state device, which has a large memory window of 4.2V and a high/low current ratio of 420% (Figure 27a) at V_g = 6V. The data points represent the drain currents after applying a writing voltage of ±6V. The read operation was done at a gate voltage of -1V (< V_C), since the high/low current states were accessible at this voltage without affecting the pre-programmed polarization state. As shown in Figure 27b, both states show good retention times up to 1000 seconds.

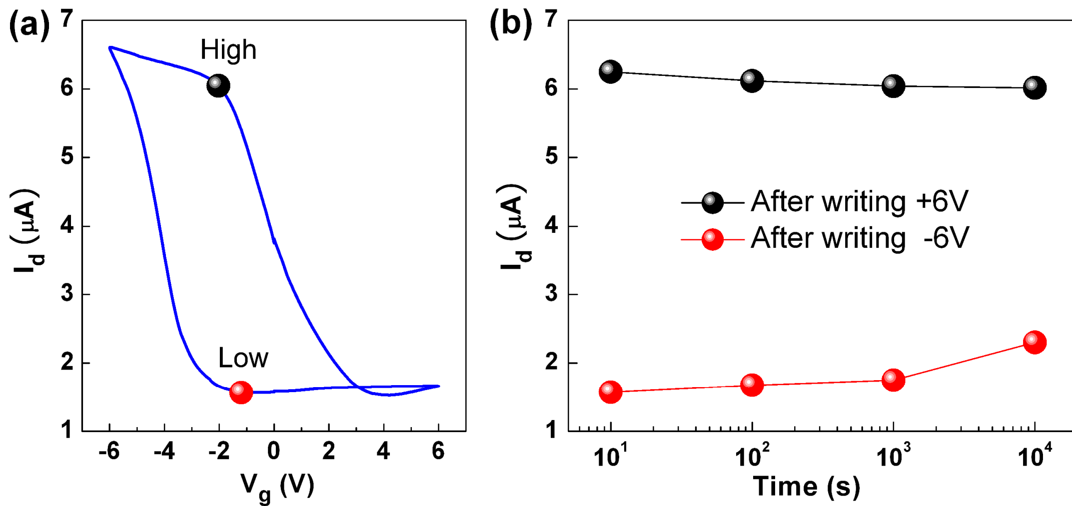


Figure 27. (a) Hysteresis characteristics of CVD grown single-layer graphene FeFET. Electrical measurements were performed with a $V_{g\ (sweep)}$ of 6V and a V_{ds} of 5mV. The black and red circles corresponds to the high and low states, respectively, of the memory device. (b) Retention time characteristics of CVD single-layer graphene FeFET after applying writing voltages of ±6V. Readout was performed at V_g = -1V and V_{ds} = 5mV.

Here, we note that the observed current hysteresis has an opposite direction from the polarization direction of the PZT as illustrated by arrows on Figure 25 and 26. Two possible mechanisms can lead to such observation; one is due to charge trapping in the interface states[108]

and the other is polarization screening from water molecules located between graphene and PZT.[109] To investigate the effect of graphene on the interface of PZT and gate-electrode, we compare the capacitance-voltage characteristics (C-V) (Figure 28) of a ferroelectric capacitor with (Pt/SLG/PZT/Pt) and without graphene (Pt/PZT/Pt). As indicated in Figure 28, the position and value of the normalized capacitance maxima drastically changes (ΔV_{max}), which can be either caused by the work function difference of the two metal plates and/or charges at the interface states.[110]

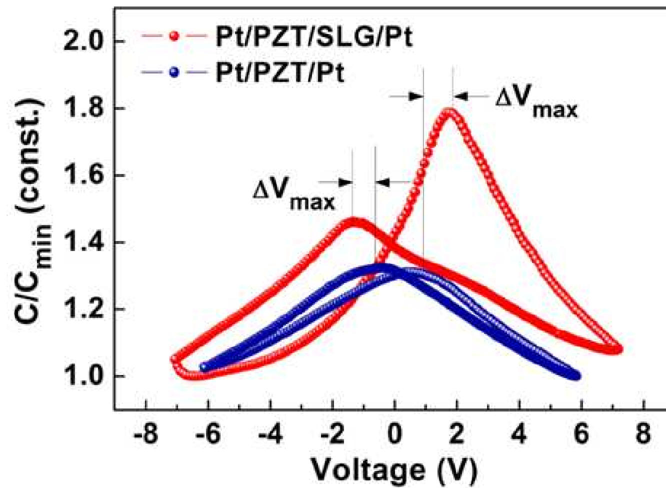


Figure 28. C-V characteristics of Pt/PZT/Pt and Pt/PZT/SLG/Pt capacitors. The position and value of the normalized capacitance maxima (ΔV_{max}) is not identical; an indication of work function difference on the two metal plates and/or charges at the interface states.

Based on above results, we explain one possible mechanism for the anti-hysteresis effect. As we positively increase the V_g beyond the Dirac point (e.g. $V_g = V_{G1}$), the external electric filed (E_{EX}) and the dipole moments (E_p) of PZT induce electrons in graphene (Figure 29a). When E_{EX} and E_p increase (e.g. $V_g = V_{G2} > V_{G1}$), the electrons become trapped by the interface states

(Figure 29b). Once V_g reaches $V_{g(sweep)}$, the trapped electrons remain at the interface states by E_p and reduce the electrochemical potential ($\Delta\mu \propto \Delta V_{max}$) of PZT (Figure. 29c).[111] Therefore, upon reversing the V_g direction, the number of electrons induced in graphene would be less than that at the same V_g (e.g. $V_g = V_{G1}$) (Figure. 29d). As a result, the I_d-V_g shows anti-hysteretic behavior contrary to the P-V_g hysteresis. Further investigation will be necessary to better understand the potential use of such effects in graphene FeFET.

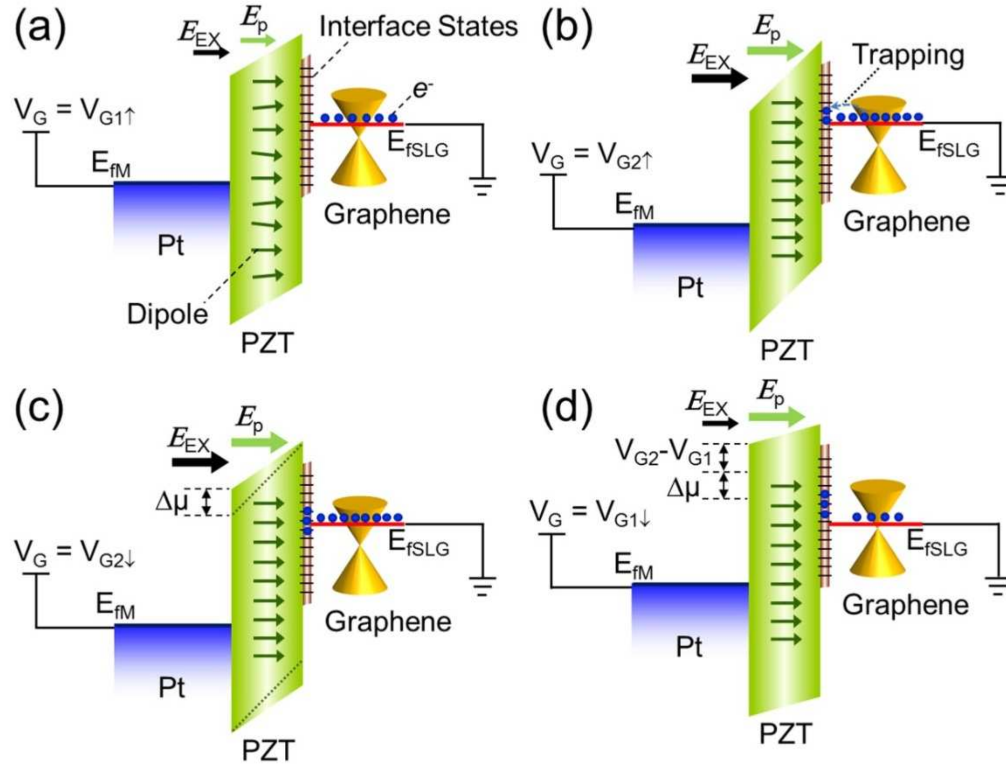


Figure 29. Origin of anti-hysteresis. Band diagram of SLG-FeFET at various bias conditions depending on sweep direction: (a) $V_g = V_{G1}$; the external electric filed (E_{EX}) and the dipole moments (E_p) of PZT induce electrons in graphene. (b) $V_g = V_{G2}$; the electrons become trapped by the interface states. (c) $V_g = V_{G2}$, the trapped electrons remain at the interface states by E_p and reduce the electrochemical potential ($\Delta\mu \propto \Delta V_{max}$) of PZT. (d) $V_g = V_{G1}$; upon reversing the V_g direction, the number of electrons induced in graphene would be less than that at the same V_g (e.g. $V_g = V_{G1}$).

Graphene based FeFET is also considered a radiation hard memory technology for aerospace applications. Every satellite utilizes electronics to maintain its directed travel route and to perform certain tasks, either it be for sensing the outer-space environment or keeping track of the time and locations of certain objects (GPS). However, conventional electronics that are used on the earth does not function properly when used outer-space. This is because the high energy particles (proton, etc.) or electromagnetic radiation (UV, X-ray) abundant in space tends to ionize the charges and create a fatal error in the electronic modules (e.g. transistor, memory, etc.) responsible for information storage and processing. Thus, there has always been a constant search for radiation hard electronic technology.

Graphene ferroelectric memory has an advantage over other memory architectures for space application. Ferroelectric memory utilizes a correlated effect of charge particles rather than a single charge particle effect, which is the dominant mechanism for electronic modules. The energy required to break the correlated effect is greater than disrupting a single particle effect, thus making it very difficult to create an error.

In order to check the feasibility of using graphene ferroelectric memory for aerospace applications, we have irradiated the memory devices with controlled dosage of X-ray. The graphene FeFETs were irradiated with a 10-keV ARACOR x-ray source at a dose rate of 31.5 krad (SiO2) / min at room temperature with applied gate biases of 2 V and –2 V. Device responses to biased annealing after radiation exposure were evaluated in-situ at room temperature. Device characterization was performed with a HP 4156A Semiconductor Parameter Analyzer in air.

As shown in Figure 30, no significant change in memory window with total dose or annealing time was observed. Hence, the charge trapping within the PZT does not affect the

ability of the ferroelectric domains to switch when the electric field is charged nor influences graphene transport; the trapped charge only shifts the center of the operating voltage range slightly, for 10-keV x-ray doses up to 1 Mrad (SiO2).

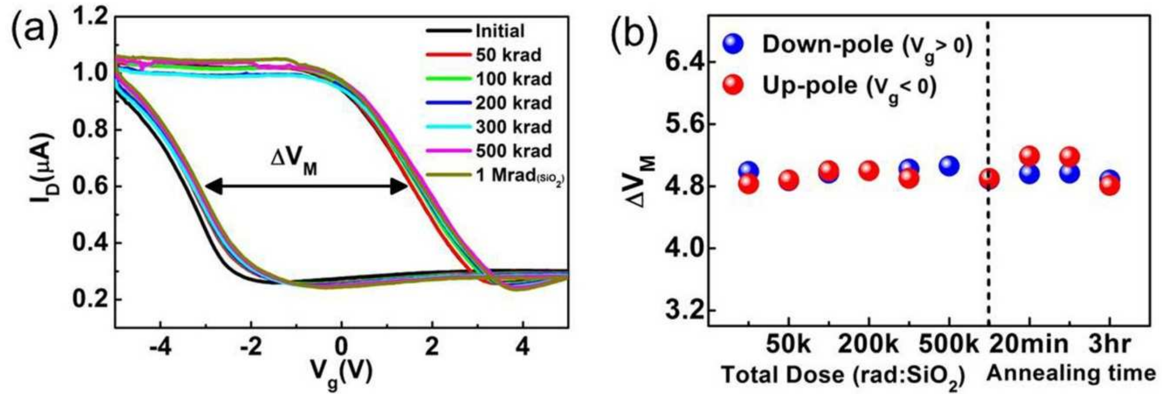


Figure 30. X-ray irradiation effects on graphene ferroelectric memory. (a) Hysteresis characteristics upon controlled dosage of x-ray irradiation. (b) Memory window change after x-ray irradiation for the down-pole state ($V_g > 0$, blue circle) and the up-pole state ($V_g < 0$, red circle).

In conclusion, we demonstrate the visibility of pristine graphene on a PZT substrate. The PZT is found to be responsible for the observed hysteretic behavior of constructed memory devices. In comparison to exfoliated graphene, CVD graphene shows a desirable bi-stable current state behavior. Using CVD graphene we were able to make a FeFET with a large memory window and reasonable retention times for low power memory applications. Furthermore, we have investigated the irradiation and annealing responses on graphene-based FeFETs irradiated with 10-keV x-rays to 1 Mrad (SiO2). The memory windows of these devices were stable before and after radiation exposure, which demonstrates potential use in space radiation environments. Currently, the bottleneck of graphene FeFETs is the small high/low

current ratio resulting from the intrinsic zero bandgap of graphene. We believe this problem can be resolved, similar to other logic devices, by inducing a bandgap through quantum confinement or symmetry breaking of the graphene atomic structure. We believe this work in parallel with current developments in all graphene based circuits should provide new avenues for exploring novel graphene based memory structures.

2.4. Materials and Methods for Graphene Ferroelectric Memory

(a) Growth of Lead Zirconium Titanate $Pb(Zr,Ti)O_3$ (PZT)

The PZT film was deposited on a $Pt/Ti/SiO_2/Si$ wafer by Chemical Solution Deposition (CSD). The details of PZT-film fabrication are described as follows. A 500 nm thick SiO_2 buffer layer was grown on the Si wafer by thermal oxidization. This serves as a diffusion barrier for Si to avoid interaction between Si and Pb in the PZT layer.[112] A bi-layer Ti/Pt with a thickness of 10 nm/100 nm was subsequently deposited onto the SiO_2 layer by e-beam evaporation. The Ti layer acts as both an adhesion layer between Pt and SiO_2 and as nucleation sites to promote the growth of fine PZT grains.[113,114] The Pt layer serves as a bottom electrode for PZT and provides lattice matching with the Pt_3Pb layer (lattice constant of Pt, Pt_3Pb, and PZT are 3.92 Å, 4.05 Å, and 4.03 Å, respectively).[114,115] After fabricating the $Pt/Ti/SiO_2/Si$ substrate, 10 wt% PZT (115/52/48) sol-gel was filtered with a 0.2 µm PTFE filter and spin-coated onto the substrate at 500 rpm for 5 seconds followed by 7000 rpm for 30 seconds. This first layer was dehydrated on a hot plate at 150 °C for 5 minutes, pyrolyzed on a hot plate at 300 °C for 5 minutes, and subsequently annealed in a furnace under ambient conditions at 700 °C for 30 seconds. During the annealing process, the pyrochlore phases were transformed into perovskite phases. This first PZT layer was used as a seed layer to grow crystallized PZT. To accomplish this, PZT sol-gel spin-coating, dehydrating, pyrolyzing, and annealing processes (all parameters are the same as in the seed layer fabrication) were repeated 6 times. Finally, a crack-free PZT film with a thickness of approximately 180nm was obtained.

To expose the Pt electrode beneath the PZT, a two-step wet etching process[116] (1st etchant: $1BOE:2HCl:4NH_4Cl:4H_2O$, 2nd etchant: $2HNO_3:1H_2O$) was used to open a channel through the PZT film.

(b) Optical Constants of PZT

The optical constants of PZT (Figure 31), both the refractive index, *n*, and the extinction coefficient, *k*, were acquired using a Sopra ellipsometer.

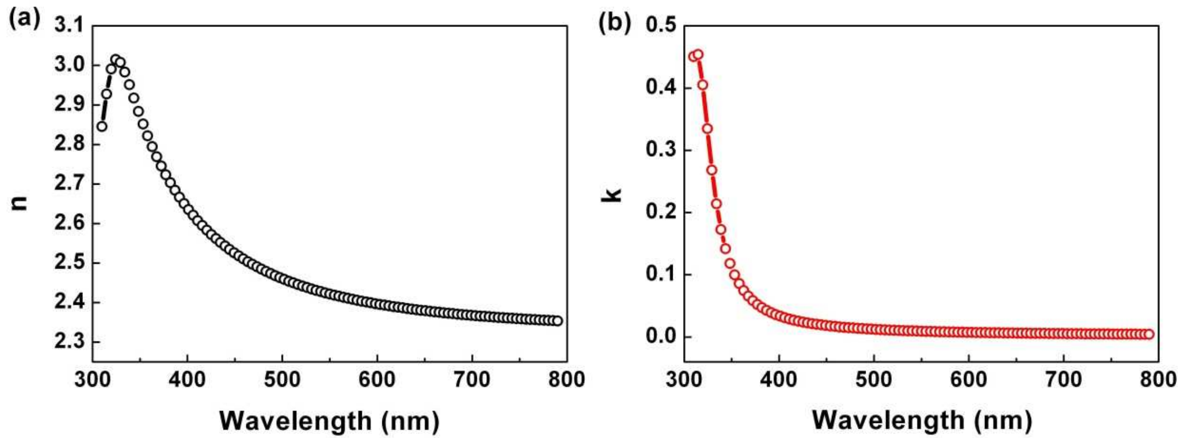


Figure 31. Optical constants of PZT. (a) Refractive index, *n*, of PZT. (b) Extinction coefficient, *k*, of PZT.

(d) Polarization Characteristics of PZT

The ferroelectric hysteresis, polarization vs. voltage, of PZT was characterized by Radiant Technology Ferroelectric Test System.

(c) Dielectric constant of PZT

The dielectric constants (Figure 32) of 180nm thick PZT films were extracted from CV measurements at f = 100Hz using an Agilent LCR meter.

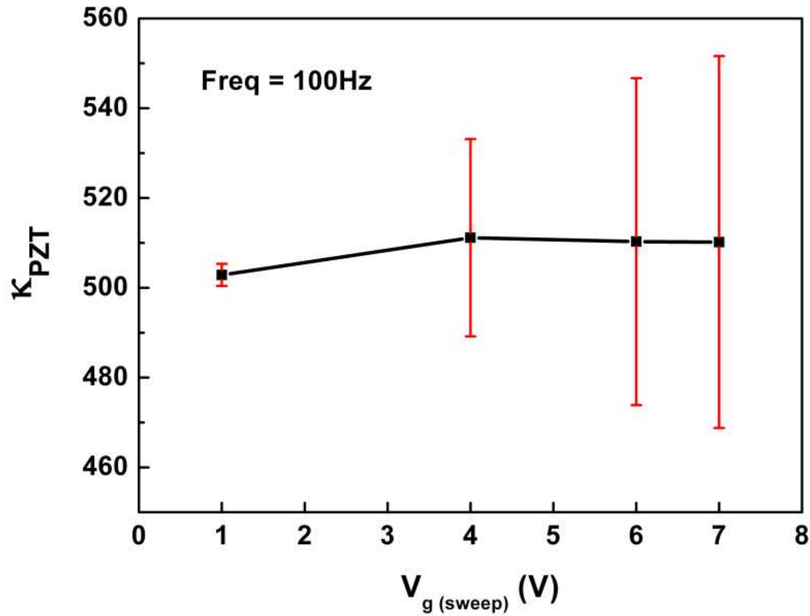


Figure 32. Dielectric constant of PZT depending on $V_{g\ (sweep)}$ measured at a frequency of 100Hz. The scale bar represents the change of the dielectric constant from the polarization.

(e) Leakage Current of 180nm thick PZT

Gate leakage current densities (Figure 33) were measured using a Keithley 4200 semiconductor characterization instrument. All electrical measurements on the single-layer graphene FFETs were performed at gate leakage current of < 1 nA and current density of $< 10^{-6}$ A/cm2.

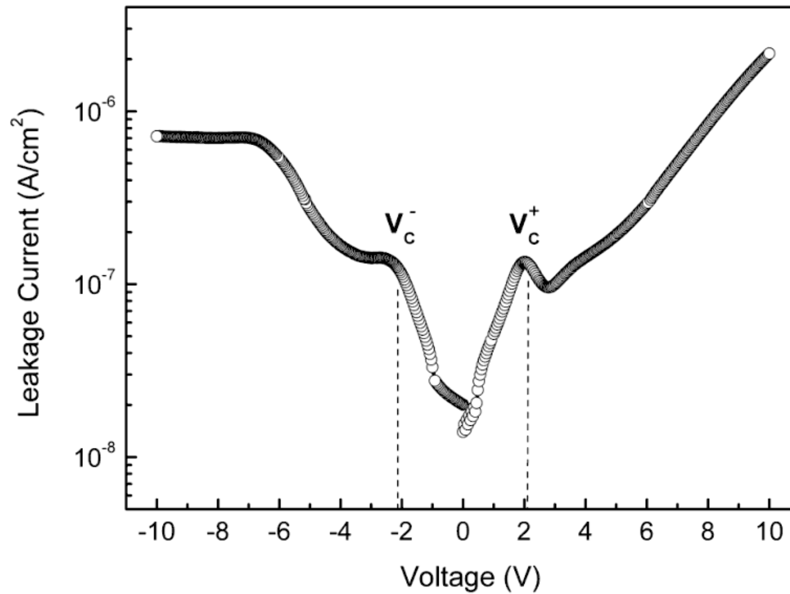


Figure 33. Leakage current of 180 nm thick PZT. Note that near the coercive voltage ($V^{\pm}_C \sim \pm 2V$) the dipoles flip (poling) and results in an increase of the leakage current (addition of transient AC current). The leakage was measured with a 2 second hold time per point.

(g) Exfoliated Graphene

Figure 34 shows the exfoliation method to obtain high quality single crystal graphene films. First, a thick graphite flake is adhered onto a piece of scotch tape. Then, the tape with the graphite flake is pressed onto a targeted substrate and removed. Next, we place the sample with an abundance of graphitic flakes under an optical microscope. Finally, the flakes are located and the thickness is identified by the color contrast between the graphite film and targeted substrate.

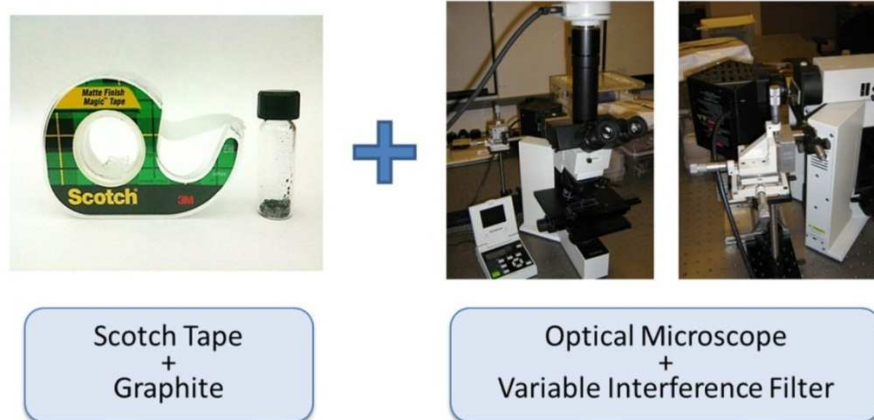


Figure 34. Mechanical exfoliation of graphene from graphite. (Right) The first image shows the Olympus BX40 microscope and Olympus DP12 CCD camera. The second image displays the variable interference filter positioned in front of the white halogen lamp.

(f) CVD Graphene Growth and Transfer

The CVD graphene was prepared by depositing a Cu thin film of 500nm thickness, using electron-beam evaporation, on a SiO_2/Si wafer and placed in an inductively coupled plasma CVD chamber. The substrate temperature was increased to 650 °C at a base pressure of $5x10^{-7}$ Torr and hydrogen plasma was applied for a surface treatment at 650 °C. The monolayer graphene was then grown under an Ar + C_2H_2 gas plasma mixture at 50 mTorr. The as-grown graphene film was then transferred to the synthesized PZT film after removal from the copper SiO_2/Si wafer. A spin-coated polymethylmethacrylate (PMMA) and adhesive ultraviolet-tape was placed over the graphene as a protective layer. After peeling the Cu/graphene/PMMA/tape from the growth substrate, the Cu thin film was removed in a dilute $FeCl_3$ solution and remains were transferred onto the PZT film. Then, the PMMA and tape were removed by organic solvents.

(g) Raman Spectroscopy Conditions

Raman spectroscopy was acquired using a Renishaw Micro Raman microscope. An acquisition time of 600 seconds was used with a 514 nm laser. The laser power density irradiating the sample was less than $2 mW/\mu m^2$.

3. Prospective and Conclusion

Up to now, we have looked into two potential NVM applications for graphene; floating-gate flash memory and ferroelectric memory. Let's take a look at alternative NVM architectures where graphene might be beneficial.

Graphene Charge-Trap Flash Memory

Charge trap memory has a very similar structure and operating principle to floating-gate memory. The only difference is that the charges are stored in the localized traps of a nitride oxide layer rather than in a conductive/semi-conductive material with delocalized charges. One advantage is that the positions can be specified, thus enabling placement dependent multi-level memory functionality.[117,118] The insulating nature of the charge storage layer in charge-trap flash memory also permits a high gate coupling and an insignificant cell-to-cell interference, thus eliminating the scaling issues in floating-gate flash memory. However, when the device dimensions shrink charge-trap based memories can suffer from variability in V_{th} caused by the stochastic property of traps. The memory window is also limited by the maximum number of traps that can be implemented without distorting the material. Furthermore, the interface states near the trap energy levels can severely degrade the retention characteristics.

The high reactive carbon nature of graphene makes functional groups easily attachable on the basal plane or edges, which creates partially reversible conversion between sp^3 and sp^2 bonds. Graphene oxide (GO) contains oxygen-containing functional groups with high electron affinity that can naturally act as a trap site. The density of oxygenated trap sites can be readily tuned and controlled to some extent by various deposition and reduction methods.[24] One of the simplest

forms to implement graphene in a charge trap flash memory is replacing the nitride charge trap layer with graphene oxide. Wang and his colleagues[119] reported a charge trap flash memory with graphene oxide as the storage layer (TaN/Al_2O_3/GO/SiO_2/Si-channel). They show a large memory window of 7.5V upon sweeping the voltage from -4V to 15V and a hysteresis of 1.5V when converted to reduced graphene oxide.

Another form is to use graphene as a channel material of a FET (gFET). The ambipolar conduction property of graphene can provide a larger memory window compared to CMOS NVM. Because of the unipolar transport characteristics in CMOS, the V_{th} shift can only be observable in either the positive or negative direction depending on the charge polarity of majority carriers. On the contrary, the V_{th} shift of a gFET can come from the sum of both positive and negative shifts of the minimum conductance point (Dirac point), enabling a larger memory window. Imam and coworkers[120] investigated a gFET adjacent to the Si_3N_4 charge trap layer. They suggested that the charging and discharging is governed by the thermionic or Poole-Frenkel emission of charge carriers from the graphene channel to the Si_3N_4 layer. The device displays a memory window of 90V at operating voltages of ±100V, and a 66% charge loss over 10^3s. In order to increase the retention characteristics and reduce the operating voltage, Lee et al.[121] devised a gFET charge-trap memory with a triple high-k stack of Al_2O_3/HfO_x/Al_2O_3. The device shows a memory window of 9.1V at operating voltages of ±30V and a 30% charge loss over 10 years. They further show that the work function of the gate material modifies the energy band alignment and strongly affects the memory performance.

Graphene Resistive Memory

For a memory device to be truly viable to compete with polysilicon floating gate flash memory not only does it has to be improved in certain aspects but all of the necessary metrics have to be satisfied. One of the biggest challenges for gFET based NVM is to increase the R_{on}/R_{off} ratio. Many efforts have been made to obtain a bandgap in this otherwise gapless material. For instance, researchers have used the quantum confinement effect by making graphene nanoribbons,[122-125] nanomesh,[81,126] or quantum dots.[127,128] A gap is created also by breaking the symmetry of the stacking orders in Bernal bi-layer graphene or in rhombohedral (ABC) tri-layer graphene. Several research groups have optically confirmed a tunable bandgap up to 250meV in bi-layer[82] and 120meV in tri-layer[129] structures. However, especially in low mobility graphene samples, present studies show non-ideal transport behaviors that are governed by the non-uniform potential profiles along the graphene channel.[130,131] Exotic phenomena, such as the strain-induced pseudo magnetic fields of 300 Tesla,[132,133] may be another option to generate a sizeable band gap in the quantum hall regime.

One way to overcome this problem is to exploit the properties of graphene oxide. The sp^3 nature of graphene oxide gives rise to a sizeable energy bandgap. Furthermore, the solution friendly and low temperature process makes it attractive for a two terminal resistive structure, which can be employed in large density cross-bar architecture. An abrupt conductance change, in the electrical characteristics of a resistive system, so called memristive effect, can be obtained through various chemical mechanisms.[134] Graphene oxide systems, in particular, exhibit a change of conductivity by more than two orders of magnitude through the redox process between sp^3 and sp^2 bonds of carbon. Several researchers[135-139] reported on numerous types of graphene oxide based resistive memory structures, in which the transfer of oxygen ions from the insulating

graphene oxide to the metal electrode forms a conductive path either through the reduction of graphene oxide in the bulk or the reduction of the metal/GO interface layer. These studies show that the transport mechanism is based on a space limited charge transfer principle.[140] In order to promote the redox process, a number of groups[141-144] have engineered the layered metal/GO/metal structure by inserting an additional conducting layer with abundance of oxygen vacancies or electron donors adjacent to GO.

Resistive switching can also be obtained in sp^2 graphene via electromigration of carbon atoms.[86,145] When the graphene is subject to high current densities, atomic motion is created by both an external electric field and the momentum transfer from the charge carriers to the carbon atoms, and hence breaks the covalent bond of a sp^2 carbon. This phenomenon yields a physical gap (<10nm) across the graphene channel in a self-limited way and significantly reduces the current compared to that before breakdown. An astonishing aspect of this phenomenon is that the effect is reversible. According to Standley and coworkers,[86] the recovery mechanism is governed by a two-step process where it first rips a carbon atom from the graphene sheet, then forms a linear chain bridging the gap. The model is corroborated by observing the increase of conductance in a series of quantized conductance ($2e^2/h$) steps (i.e., parallel quantum channels).

Graphene Nano-Electromechanical Switch (NEMS)

Another application would be obtaining memory functionality from electromehcanical switches (NEMS). NEMS based switches exhibit hysteresis between their pull-in and pull-out operations due to the surface forces[146,147] (i.e. quantum effects, surface states, and defects) or between an upward and downward bent in a mechanical bi-stable buckle beam.[148] Three-

dimensional (3D) materials, such as metals or poly-Si, become brittle when they are scaled down to nanometers. In contrast, 1D and 2D materials, such as carbon-nanotubes and graphene, sustain their mechanical properties even at the nanoscale. The low mass density (7.4×10^{-19} g/μm^2) and high Young's modulus (1TPa)[55] makes graphene a strong candidate for high speed NEMS based NVM. The fundamental speed limit for a single electromechanical switch operation is roughly half the time for the membrane to oscillate. Graphene exhibits resonant oscillations at 70MHz,[149] which corresponds to a switching time of few tens of nanoseconds. From a few-layer graphene electromechanical switch, Milaninia and coworkers demonstrated a hysteresis effect between pull-in and pull-out operations for a few cycles,[150] while Kim and colleagues reported operating voltages as low as 1.85V.[151] However, both studies show unrepeatable operations due to a non-hermetic environment. A more reliable method to obtain a controlled hysteresis would be desirable either by integrating a floating gate[152] or a charge trap structure[153,154] into an electromechanical switch.

Graphene Magnetic Memory

Besides utilizing the charge degree of freedom for information storage, other state variables such as the spin degree of freedom may be considered. Researchers have shown a long spin lifetime (770ps for SLG,[32] 2ns for BLG[155] at 300K) in graphene as a consequence of its weak spin-orbit coupling. Furthermore, many theoretical studies have predicted that graphene can be converted to a half-metal in a graphene nanoribbon with well-defined edge structures[156] or become topologically insulating (quantum spin hall effect) when the basal plane is functionalized

by adatoms.[157] These spin properties of graphene can be exploited for unprecedented memory structures.

Graphene Transparent and Flexible Memory

One last property of graphene in which we would like to mention is its transparency and flexibility. The atomic thickness of graphene leads to a transmittance of 97% near visible wavelengths.[57] Graphene's high breaking strength of 130GPa,[55] which is 200 times greater than steel, makes it difficult to fracture under stress. The extra degree of freedom perpendicular to the in-plane honeycomb lattice makes graphene also extremely flexible. Such intrinsic properties of graphene can provide a platform for transparent and flexible NVM technology.

Conclusion

We examined how the properties of graphene can be applied to various NVM structures, and summarized recent progress of graphene based NVM technology (Table 1). When looking back from 2004, tremendous amount of new techniques and fundamental understanding of graphene has been achieved in a very fast pace in various areas. In this perspective, it will be interesting to see what kind of impact graphene will create for the next generation electronics.

Memory Architecture		Floating Gate	FeFET	Charge Trap	NEMS	Resistive	Spin
Storage Mechanism		Charge on Floating Gate	Polarization	Charge Trapped in Gate Insulator	Mechanical Motion	Redox, Electromigration	Magnetization, Spin Dynamics
Graphene NVM		g-FGM g-FET	g-FET	go-CTM g-FET	g-NEMS	go-REM g-ACM	N/A
Compatibility	**Inorganic**	Yes	Yes	Yes	Yes	Yes	Yes
	Organic	Yes	Yes	Yes	No	Yes	N/A
Viability for Flexible-Transparent Electronics		Yes	Yes	Yes	No	Yes	N/A
Advantages		Low Voltage & Interference, Long Retention	Large Capacitive Coupling	Large Memory Window	Fast Switching Speed	Simple Material Preparation, High Endurance	Low Power Dissipation
Challenges		On/Off Ratio	Anti-hysteresis, On/Off Ratio	Retention On/Off Ratio	Endurance	Reproducibility	Understand Spin Properties & Dynamics
Scaling		Interference <20nm[a]	Nano-ferroelectrics <10nm[b]	Reduced Short Channel Effects[c]	<10nm[d]	<10nm[d]	N/A

Table 1. Overview of graphene based NVM. g-FGM refers to graphene floating-gate memory, go-CTM refers to graphene oxide charge-trap memory, go-REM refers to graphene oxide resistive memory, and g-ACM refers to graphene atomic chain memory.[a: ref. 158, b: ref. 159, c: ref. 35, d: ref. 48]

4. Appendix

(a) Single-electron Band-Structure of graphene using Tight-binding Approximation

As shown in Figure 35, graphene is made out of carbon atoms arranged in a hexagonal lattice structure. We select

$$a_1 = \frac{a}{2}\left(3, \sqrt{3}\right), \qquad a_2 = \frac{a}{2}\left(3, -\sqrt{3}\right),$$

as the basis vectors for the underlying triangular Bravais lattice, where a ≈ 1.42 Å is the carbon-carbon distance. The nearest neighbors are shifted by vectors

$$\delta_1 = \frac{a}{2}\left(1, \sqrt{3}\right), \qquad \delta_2 = \frac{a}{2}\left(1, -\sqrt{3}\right), \qquad \delta_3 = -a(1, 0).$$

Here we will use the tight-binding approximation, also known as the LCAO (linear combination of atomic orbitals) method, which assumes that the deeper orbitals are screened by the outer orbitals and does not feel the crystal field (potential). Also, to simplify the calculation, the Hamiltonian will be expressed in the second quantization form, where the wave fields are "quantized" to describe the problem in terms of quanta or particles (contrary to the first quantization, where the classical particles are assigned with wave amplitudes). To calculate the band structure of the outermost electron's π band (disregarding the spin degeneracy), we denote the electronic orbitals of the A triangular sublattice by a_i annihilation operator (i labeling lattice sites of A) and those of the B triangular sublattice by b_i annihilation operator (j labeling lattice sites of B). If we only consider the nearest-neighbor hopping, the Hamiltonian is given by

$$H = -t \sum_{<i,j>} (a_i^\dagger b_j + b_j^\dagger a_i) ,$$

where $<i, j>$ refers to all nearest-neighbor pairs and t is the hopping amplitude . The eigenstate can be written as

$$\psi_{\mathbf{k}} = \left(A \sum_i e^{i\mathbf{k}\cdot\mathbf{r}_i} a_i^\dagger + B \sum_j e^{i\mathbf{k}\cdot\mathbf{r}_j} b_j^\dagger \right) |0\rangle ,$$

where A and B are two unknown coefficients and the two summations are taken over the respective sublattices. By applying the Hamiltonian and carefully using the fermionic commutation relations

$$\{a_i, a_{i'}^\dagger\} = \delta_{ii'} , \qquad \{b_j, b_{j'}^\dagger\} = \delta_{jj'} , \qquad \{a_i, b_j^\dagger\} = 0 ,$$

We find

$$H\psi_{\mathbf{k}} = -t \left(AC \sum_j e^{i\mathbf{k}\cdot\mathbf{r}_j} b_j^\dagger + BC^* \sum_i e^{i\mathbf{k}\cdot\mathbf{r}_i} a_i^\dagger \right) |0\rangle ,$$

$$C = e^{i\mathbf{k}\cdot\boldsymbol{\delta}_1} + e^{i\mathbf{k}\cdot\boldsymbol{\delta}_2} + e^{i\mathbf{k}\cdot\boldsymbol{\delta}_3}$$

The eigenvalue problem is now

$$H\psi_{\mathbf{k}} = \varepsilon_{\mathbf{k}}\psi_{\mathbf{k}}$$

and can be reduced to the following 2x2 matrix eigenvalue problem

$$-t\begin{pmatrix} 0 & C^* \\ C & 0 \end{pmatrix}\begin{pmatrix} A \\ B \end{pmatrix} = \varepsilon_{\mathbf{k}}\begin{pmatrix} A \\ B \end{pmatrix}.$$

The solution for the energy dispersion follows to be

$$\varepsilon_{\mathbf{k}} = \pm t|C| = \pm t\sqrt{3 + 2\cos\left(\sqrt{3}k_y a\right) + 4\cos\left(\frac{\sqrt{3}k_y a}{2}\right)cos\left(\frac{\sqrt{3}k_y a}{2}\right)}\ .$$

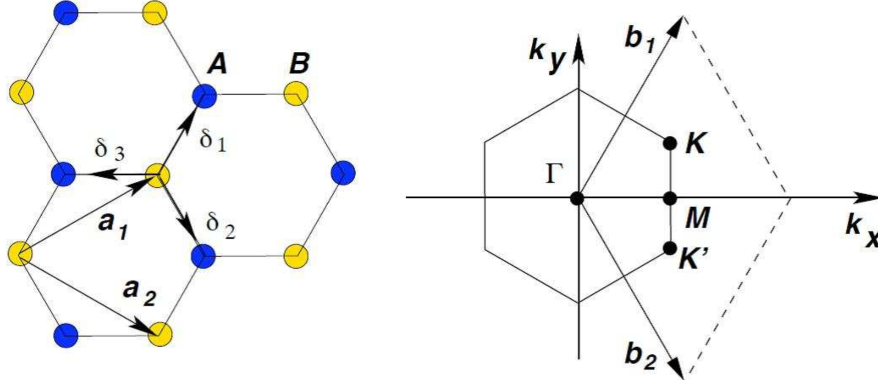


Figure 35. (Left) Lattice structure of graphene, made from two-interpenetrating triangular Bravais lattices (A and B sublattices). $\mathbf{a}_1$ and $\mathbf{a}_2$ are the Bravais lattice unit vectors, and $\boldsymbol{\delta}_i$ (i = 1, 2, 3) are the nearest-neighbor vectors. (Right) The hexagonal Brillouin zone corresponding to the triangular Bravais lattice, where $\mathbf{b}_1$ and $\mathbf{b}_2$ are the reciprocal lattice unit vectors defined by $\mathbf{a}_i \cdot \mathbf{b}_j = 2\pi\delta_{ij}$. The Γ, K, M, and K' points correspond to the high symmetry points within the Brillouin zone.[13]

(b) Phonon Dispersion and Raman Spectroscopy of Graphene

Raman spectroscopy is widely used to characterize the vibrational modes of a molecule or crystal. In the case of crystalline solids, the density fluctuation (first sound) of atoms creates a sound wave called phonons. The phonon modes of each crystal have its unique resonant frequency, depending on the bonding energy of the atoms that constitute the crystal. Upon illumination of a monochromatic laser on a crystal, the interaction between photons and phonons results in a unique frequency shift of the laser frequency. The frequency shift corresponds to the frequency of the phonon mode of the crystal.

The numbers and types of phonon bands are determined by the physical dimension and the number of basis orbitals within a unit cell, which is the smallest cell that is required to represent the whole crystal structure due to the spatial periodicity (translational symmetry). For a 3D structure with a single basis, there exist three acoustic branches, each for every degree of freedom (one longitudinal and two transverse). For a 3D structure with two bases, there exist three additional optical branches, each for every degree of freedom, which in total are six branches.

Graphene, since it is a 2D material with two bases, will theoretically have a total of four branches; two acoustic and two optical. However, in practice, it does exist in a 3D space, which leads to two additional out-of-plane branches, one acoustic and one optical (Figure 36 and Figure 37).

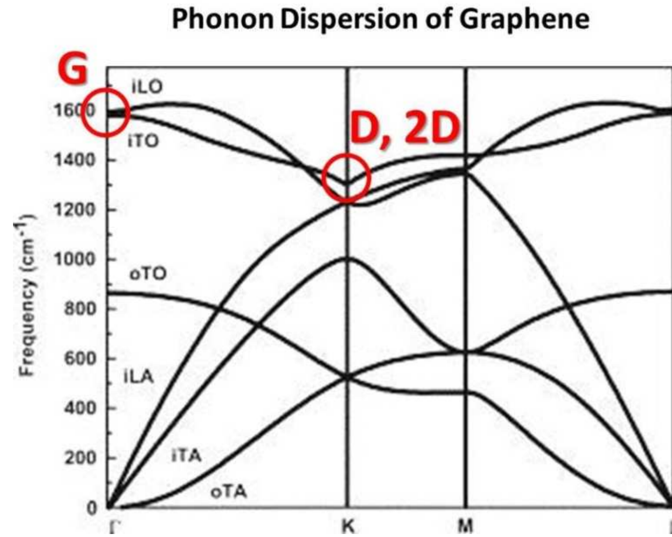


Figure 36. Phonon dispersion of graphene. The 'i' refers to the in-plane phonons, 'o' refers to the out-of plane phonons, LO refers to the longitudinal optical modes, TO refers to the transverse modes, LA refers to the longitudinal acoustic modes, and TA refers to the transverse acoustic modes.[30] The red circles represent the high density of states at the Γ point near 1600 cm^{-1} and K point near 1350 cm^{-1}, which corresponds to the G and D (2D) band respectively.

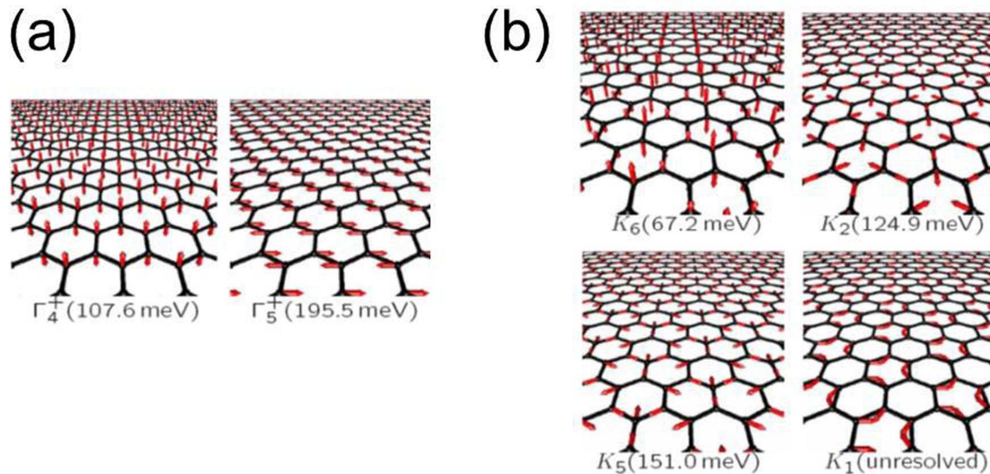


Figure 37. Raman active phonon modes of graphene. (a) Optical phonon modes at the Γ point. (b) Phonon modes at the K point. The red arrows indicate the vibrational directions of each phonon modes. The phonon energies are experimental values.[160]

The Raman spectrum of graphene (Figure 38a) shows two unique peaks with high intensity. The 1580 cm^{-1} peak is called the G band and the 2700 cm^{-1} is called the 2D band. The G stands for graphene band and the 2D stands for the double resonant defect band. Figure 36 shows that the phonon density of states is extremely high at 1580 cm^{-1} and 1350 cm^{-1}. Thus, the origin of the G band is from the highest optical phonons (LO) near the Γ point, and the 2D band is from the highest optical phonons (TO) near the K point.

For the past few decades, the 2D band was considered to be a second-order Raman process. Only recently, the origin of the 2D band was identified as a double resonant process.[97] The double resonant model is a fourth-order process involving virtual transitions. (1) excitation of electron-hole pair induced by the laser [a → b] (2) electron-phonon scattering with an exchanged momentum q close to K [b → c] (3) electron-phonon scattering with an exchanged momentum –q (momentum conservation) [c → b] (4) electron-hole recombination [b → a]. The double resonant condition is achieved when the energy is conserved in these transitions. Thus, the resulting 2D frequency is twice the frequency of the scattered phonon with q.

The double resonant 2D band serves as a great characterization tool for identifying the number of layers. Since the double resonant process involves phonon-electron interaction, the evolution of the electronic band structure from mono-layer to bi-layer would be depicted in the 2D peak of the Raman spectrum. In the mono-layer case (Figure 38), the 2D peak has only one phonon involved (momentum conservation) resulting in a single Raman frequency. However, in the bi-layer case (Figure 39), there are four possible routes that satisfy the double resonant conditions, resulting in four phonon frequencies. Thus, Raman spectroscopy of graphene is the most accurate method to determine the number of layers for mono and bi-layer graphene. In general, the Atomic Force Microscopy (AFM) is used often to characterize the morphology of a

sample, which includes the height. However, upon measuring the height of the first layer (mono-layer or multi-layer having stair-like boundaries) on top of a substrate, the height varies from 0.4nm ~ 1nm depending on the environmental condition (e.g. water molecules in between the substrate and first layer), showing ambiguities.

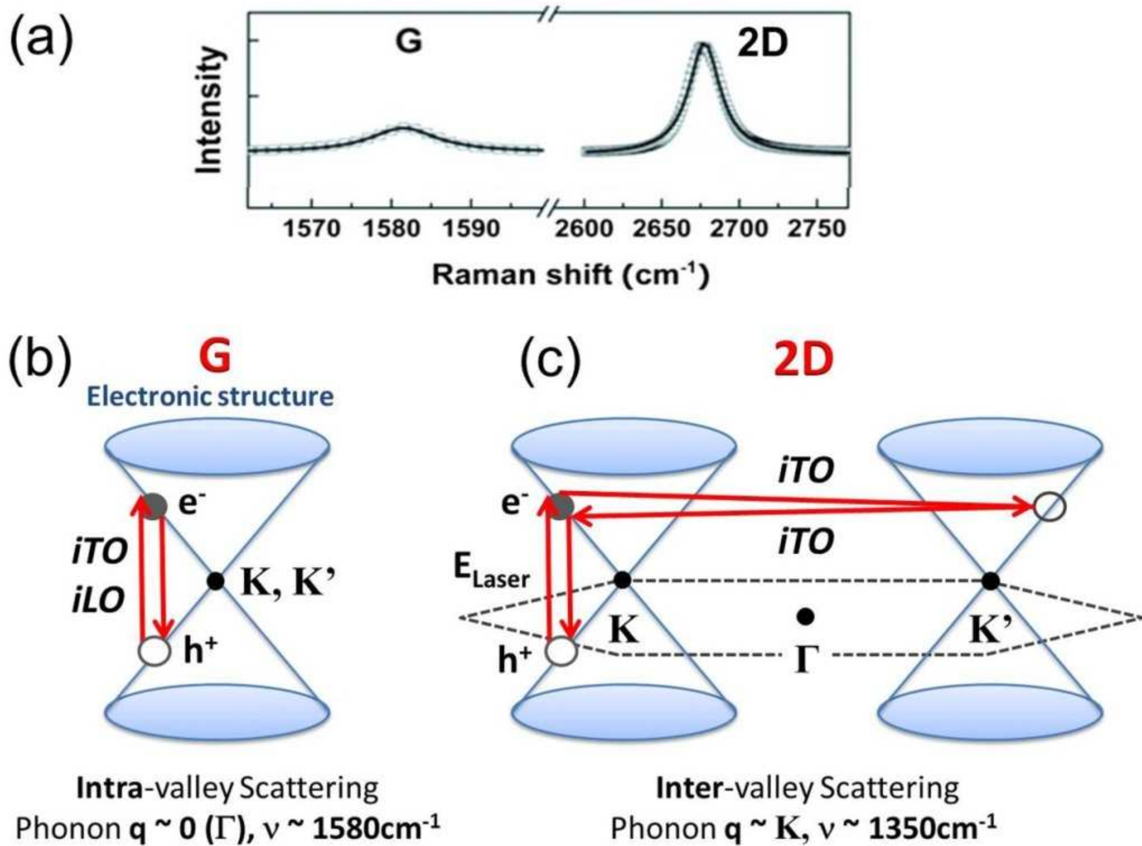


Figure 38. (a) Raman spectrum of graphene (excitation laser: 514nm). Two major peaks are observable for graphene, G (Pos ~1580 cm^{-1}, FWHM ~10 cm^{-1}) and 2D (Pos ~2680 cm^{-1}, FWHM ~26 cm^{-1}). (b) Raman scattering mechanism accountable for the G peak phonon mode. (c) Raman scattering mechanism accountable for the 2D peak phonon mode.

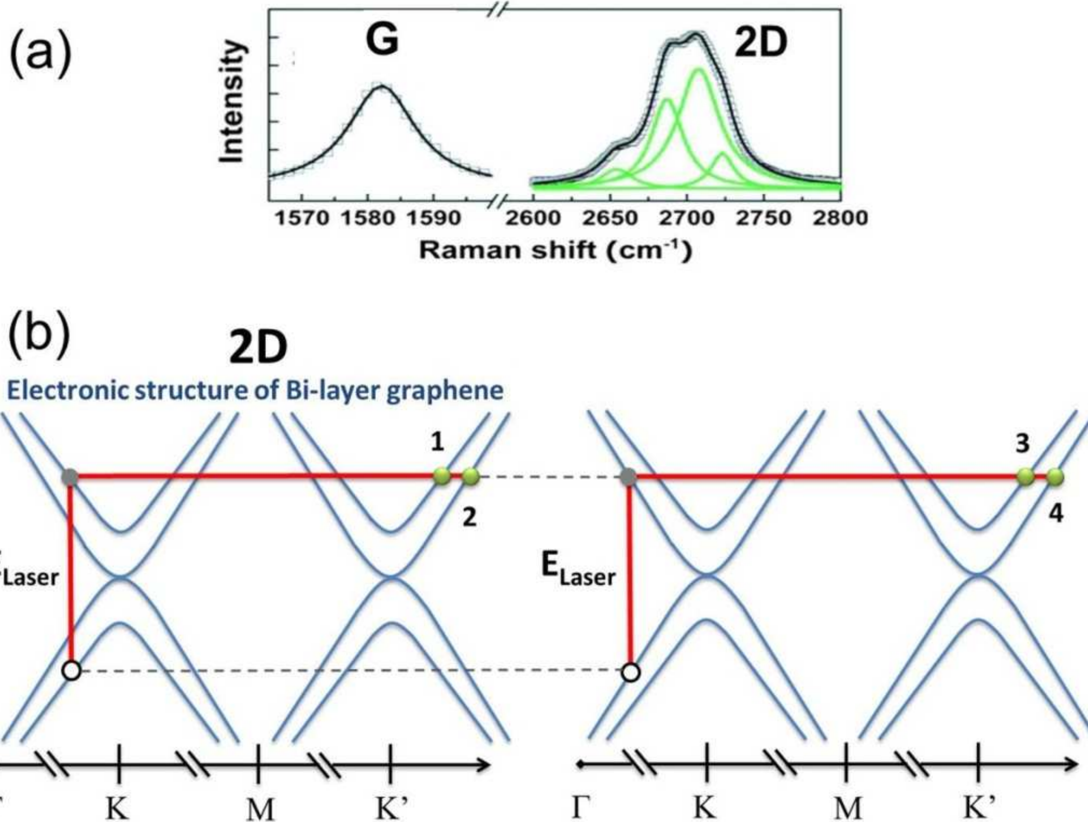


Figure 39. (a) Raman spectrum of bi-layer graphene (excitation laser: 514nm). The G band position (~1580cm^{-1}) is similar to graphene. The 2D band was accurately fitted with four Lorentzian functions (Pos^{1} ~2654cm^{-1}, Pos^{2} ~2685cm^{-1}, Pos^{3}_2706 cm^{-1}, and Pos^{4}_2723 cm^{-1}). The four peaks depict the band structure of a BLG through the double resonant process. This allows the 2D band of graphene to be an excellent characterization tool for determining the number of layers. (b) Raman scattering mechanism accountable for the 2D peak phonon mode (double resonant process).

(c) Atomic-scale characterization of CVD graphene grown on Cu[161]

Knowledge of material growth mechanisms on solid supports allows scientists to grow materials with highly desired properties. In heteroepitaxy, lattice matching between deposited materials and single crystal substrates dramatically affects the properties of grown materials. Small atomic lattice mismatches between substrates and growth materials creates significant strain in single crystal films,[162] which can result in highly desired electronic properties or harmful defects.[163] In addition, when growing ionic films on metallic single crystals, the initial facet identity and mobility of the underlying substrate greatly influence resulting surface structures. In these systems, a strong interfacial binding between surface charges on vicinal metal surfaces and ionic overlayers[164,165] drives massive surface restructuring and selective growth on specific metal facets.[166,167] These exemplary studies illustrate the significant role of substrate – overlayer interactions.

Here we show scanning tunneling microscope (STM) topographs of as-grown graphene produced by the thermal decomposition of methane on high purity polycrystalline copper disks and foils. The STM allows us to observe the morphology of samples over several hundred square nanometers and obtain atomic resolution of graphene's carbon lattice at specific surface features of interest in a single experiment. The pristine graphene lattice is shown to exist over the copper substrate despite underlying features that are generally thought to create defects in a growing overlayer. As shown in Figure 40, defect-free graphene is observed over edges and vertices of the copper substrate where line and point defects are expected under conventional wisdom. Furthermore, the perfect lattice is observed over crystalline facets of a different symmetry than graphene and over highly stepped surfaces, both of which should inhibit efficient sheet extension.

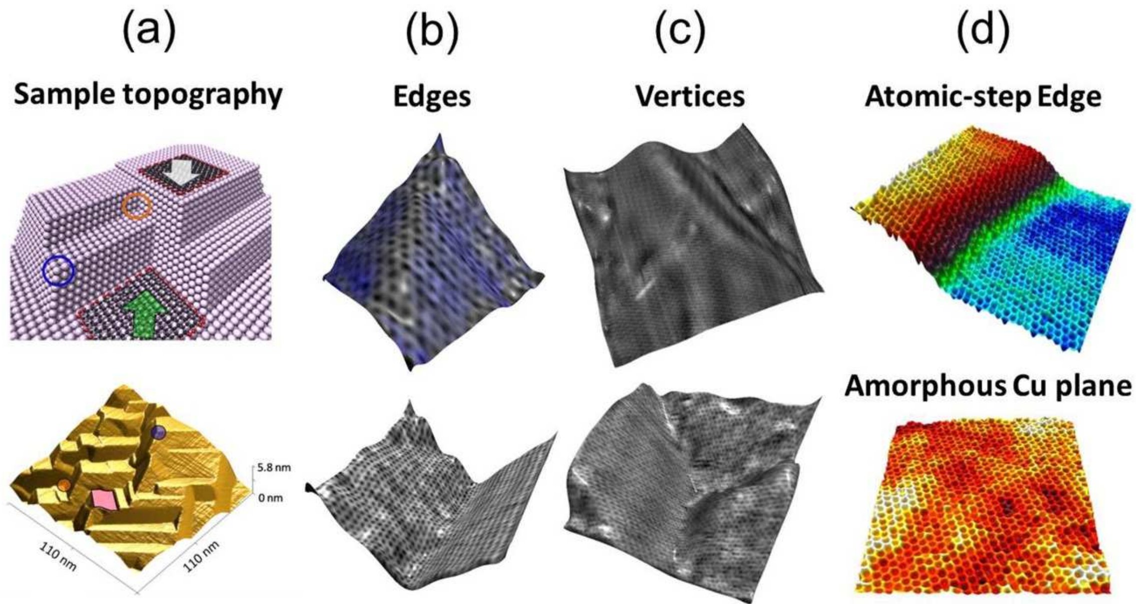
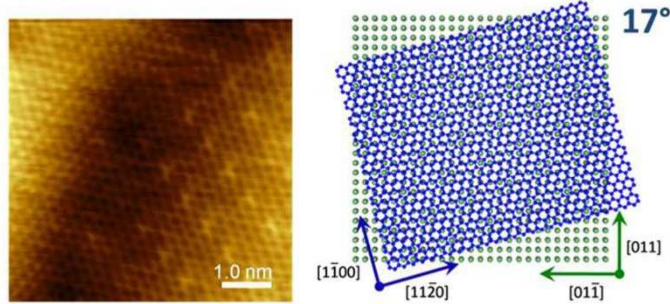


Figure 40. STM topography of CVD graphene grown on Cu. (a) (Top) Schematic illustration of graphene growth "down" (white arrow) positive edges and vertices and "up" negative edgesand vertices. Carbon atoms are represented by black spheres, foremost carbon atoms of the growing sheet expected to interact with edgesand vertices are highlighted with red spheres, the blue circle illustrates where three positive edges unite at a positive vertex, and the orangecircle illustrates where three negative edges unite at a negative vertex. (Bottom) STM topograph of a highly corrugated region of the sample. The magenta rectangle highlights an atomically flat plane, the blue circle highlights where three positive edges meet to form a positive vertex, and the orange circle highlights where three negative edges meet to form a negative vertex. (b) – (d) STM images illustrating defect-free growth of graphene over (b) (Top) a positive edge, (Bottom) a negative edge, (c) (Top) a positive vertex, (Bottom) a negative vertex. (d) (Top) a copper monatomic step, and (Bottom) an amorphous copper plane. Imaging parameters are as follows: (a) (Bottom) $I_t = 0.5$ nA, $V_s = -500$ mV, (b) (Top) $I_t = 0.9$ nA, $V_s = -75$ mV, (Bottom) $I_t = 5.0$ nA, $V_s = -75$ mV, (c) (Top) $I_t = 1.0$ nA, $V_s = -500$ mV, (Bottom) $I_t = 5.0$ nA, $V_s = -75$ mV, (d) (Top) $I_t = 30$ nA, $V_s = -75$ mV, and (Bottom) $I_t = 0.9$ nA, $V_s = -65$ mV.

A natural question that arises when analyzing the STM topographs is whether the underlying copper planes belong to crystallographic facets of different identities. As shown in Figure 41, using higher order periodic modulations to the graphene sheet, we find that unique sets of modulations to graphene's atomic structure appear along sets of parallel planes of the sample. The modulations span the entirety of an atomically flat region and fade when the edge of

one plane meets another plane oriented in a different direction. The two-dimensional spatial modulation frequency and apparent height of a unique pattern does not depend on the size or shape of the flat region. This indicates that the patterns are not a result of electron standing waves created from geometrical confinement as has been observed in graphene nanoribbons.[168] Additionally, it is possible to image these modulations with “moiré defects,” where portions of the pattern are absent and replaced by slight depressions of approximately 10 pm with the graphene layer maintaining a pristine structure. The origin of the periodic modulations is, hence, attributed to the presence of different crystalline copper facets interacting with the graphene sheet to produce unique moiré superstructures in an analogous manner to what has been observed for graphene on metal single crystals.[169-171]



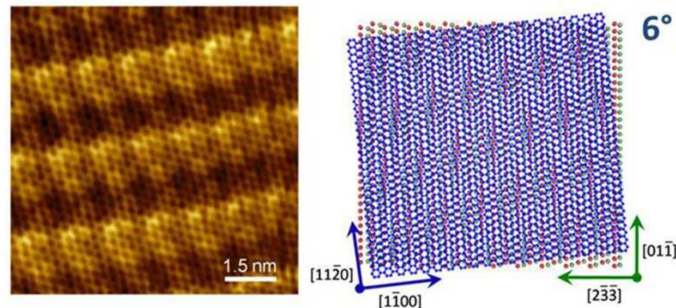


Figure 41. Moire´ patterns of CVD graphene grown on Cu. (a) (Left) Atomic resolution STM image of graphene growth over a Cu (100) facet. The graphene [1120] direction makes a 17° angle with the copper [011]direction. (Right) Moire´ pattern analysis, where the green spheres and axis belong to copper and the blue lattice and axis belong to graphene. (b) (Left) Atomic resolution STM image of graphene growth over a Cu(311) facet. The graphene [1120] direction makes a 6° angle with the copper [011] direction. (Right) Moire´ pattern analysis, where the red and green spheres belong to planes 1 and 2 of the Cu (311) facet. Imaging parameters are as follows: (a) I_t= 0.99 nA, V_s= -85 mV, and (b) I_t= 5.1 nA, V_s= -75 mV.

(d) Various current conduction processes in insulators

Conduction Process	Current Density	Voltage & Temperature Dependence
Thermionic Emission (Schottky Emission)	$J = R^{*}T^{2}\exp\left[\frac{-q(\phi_b - \sqrt{q\mathcal{E}/4\pi\varepsilon_i})}{kT}\right]$	$\propto T^{2}\exp\left[\frac{q}{kT}(a\sqrt{V} - \phi_b)\right]$
Direct Tunneling (low-field approx.)[172]	$J \propto \sqrt{\phi_b}\mathcal{E}\exp\left[\frac{-2d\sqrt{2m^{*}\phi_b}}{\hbar}\right]$	$\propto V$
Fowler-Nordheim Tunneling	$J \propto \mathcal{E}^{2}\exp\left[\frac{-4\sqrt{2m^{*}}(q\phi_b)^{3/2}}{3q\hbar\mathcal{E}}\right]$	$\propto V^{2}\exp\left[\frac{-b}{V}\right]$
Poole-Frenkel Tunneling	$J \propto \mathcal{E}\exp\left[\frac{-q(\phi_b - \sqrt{q\mathcal{E}/\pi\varepsilon_i}}{kT}\right]$	$\propto V\exp\left[\frac{q}{kT}(2a\sqrt{V} - \phi_b)\right]$
Ohmic	$J \propto \mathcal{E}\exp\left(\frac{-\Delta E_{ac}}{kT}\right)$	$\propto V\exp\left(\frac{-c}{T}\right)$
Ionic Conduction	$J \propto \frac{\mathcal{E}}{T}\exp\left(\frac{-\Delta E_{ai}}{kT}\right)$	$\propto \frac{V}{T}\exp\left(\frac{-d'}{T}\right)$
Space-Charge-Limited	$J = \frac{9\varepsilon_i\mu^{*}V^{2}}{8d^{3}}$	$\propto V^{2}$

q = electron charge. $\hbar$ = reduced Plank constant. R^* = effective Richardson constant. ϕ_b = potential barrier height. $\mathcal{E}$ = electric field in insulator. ε_i = insulator permittivity. m^* = effective mass. d = insulator thickness. ΔE_{ac} = activation energy of electrons. ΔE_{ac} = activation energy of ions. $V \approx \mathcal{E}d$. $a \equiv \sqrt{q/4\pi\varepsilon_i d}$. b, c, and d' are constants.[173]

Table 2. Various conduction processes in insulators. A current density expression and voltage, temperature dependence.

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